Instructions:

- This is an individual assignment. No collaboration is allowed. There will be vivas in the last week of the semester.
- You will submit one file titled u2021xxx.zip where xxx are last 3 digits of your registration number.
- Inside the file make a label for each question and paste that question code below that label.
- Missing the deadline will cost you 30 marks and then 20 on each 24-hour delay.
- Submission will be on MSTeams.
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Implement a single-cycle RISC-V processor in Verilog supporting the following 14 instructions:

`add, sub, and, or, addi, beq, blt, bge lw, sw, lb, sb, jal, jalr.`

Methodolgy:

You will write Verilog modules for various processor components we studied in chapter 4, e.g., PC, Instruction Memory, Data Memory, ALU, Muxes, etc. Write code for each module in as separate .v file.

There should be a test bench for each module, in a separate *modulename_tb.v* file which thoroughly checks and verify the working of that module for different inputs.

A separate overall *processor.v* file should combine and connect these module instances to make a full processor.

A separate *processor_tb.v* file to verify the working of the final processor.

The processor should be able to correctly execute any combination of the above mentioned instructions. It should not execute any instruction other than the above mentioned ones.

Make the instruction and data memories of at least 1024 bytes.

Submission:

The submission will be on MS Teams. You will make a folder titled u2021xxx where xxx are the last three digits of your registration number. You will put all the *module.v* and *module_tb.v* file in this folder and nothing else, zip this folder, and upload it on MS Teams.

Rubric:

This is an individual assignment. You are not allowed to take help from anywhere except from books.

Overall working	50
Test benches are comprehensive	50
Followed submission instructions	20
Submission on time	30
Total	150 marks.

The End.