SOLAR POWER & BATTERY MANAGEMENT

SOLAR_1
Sheet: SOLAR_INPUT
File: SOLAR_INPUT.sch
GND PWR ADC
VRAW_SOLAR
SOLAR_ADC1

SOLAR_2
Sheet: sheet61651500
File: SOLAR_INPUT.sch
GND PWR ADC
SOLAR_ADC2

SOLAR_3
Sheet: sheet6165EBDF
File: SOLAR_INPUT.sch
GND PWR ADC
SOLAR_ADC3

SOLAR_4
Sheet: sheet6166C2B6
File: SOLAR_INPUT.sch
GND PWR ADC
SOLAR_ADC4

SOLAR_5
Sheet: sheet61679A31
File: SOLAR_INPUT.sch
GND PWR ADC
SOLAR_ADC5

SOLAR_6
Sheet: sheet616870B0
File: SOLAR_INPUT.sch
GND PWR ADC
SOLAR_ADC6

Roughly 150mA from one solar panel under good conditions.
MAYBE 200mA with multiple sides

Solar MPPT 5V output
Sheet: SOLAR_MPPT_5V
File: LTC3130.sch
VIN VOUT PGOOD MPPC VCC VS1 VS2 GND
in stock
PG_SOLAR
5V output
R9 224K
R10 100K
R17 100K
GND

Power Good Load Switch
U5 TPS270
VIN VOUT EN VOUT R2 R1/C1
R48 10K
R49 10m
GND

External Power
J14 USB_B_Micro
VBUS D+ D- ID Shield GND
ESD9B5.0ST5G
D18
R329 330
D19 LED_SMD_RED
R328 10m
R327 0
GND

Battery Charger 1
Sheet: BATTERY_CHARGER
File: BATTERY_CHARGER.sch
VEXT SOLAR_5V BC_1_SHDN BC_1_SUSP BC_1_CLDIS BC_1_ISTAT BC_1_CHRG BC_1_VEXT BC_1_POL
EXT VIN SHDN SUSP CLDIS ISTAT CHRG ACPR POL
VOUT BAT VNTC NTC GND
VOUT1
Sheet: BATTERY
File: BATTERY.sch
VHEAT VBAT VNTC NTC GND
GND
R53 10m

Battery 1

Battery Charger 2
Sheet: sheet5F4CFCDE
File: BATTERY_CHARGER.sch
VEXT SOLAR_5V BC_2_SHDN BC_2_SUSP BC_2_CLDIS BC_2_ISTAT BC_2_CHRG BC_2_VEXT BC_2_POL
EXT VIN SHDN SUSP CLDIS ISTAT CHRG ACPR POL
VOUT BAT VNTC NTC GND
VOUT2
Sheet: 5F4CFCDF
File: BATTERY.sch
VHEAT VBAT VNTC NTC GND
GND
R54 10m

Battery 2

Ideal Diode
Sheet: sheet5F71F776
File: IDEAL_DIODE.sch
VIN1 EN1 GND EN2 VIN2
VOUT1 STAT1 WARN1 WARN2 STAT2 VOUT2
IDEAL_EN1
IDEAL_EN2
IDEAL_STATUS1
IDEAL_WARN1
IDEAL_WARN2
IDEAL_STATUS2
R55 10m
R56 10m
VBUS

Voltage Regulators

3.3V Regulator
300mA Output Max
Sheet: sheet5FCD3934
File: LTC3130.sch
VBUS VIN VOUT PGOOD MPPC VCC VS1 VS2 GND
R8 100K
PG_3V3
3.3V output
U4 TPS270
VIN VOUT EN VOUT R2 R1/C1
R11 10K
+3.3V
Power Good Load Switch

5.0V Regulator
2A @ 4Vin Max
Sheet: 5V_BOOST
File: MP3414A.sch
VBUS VIN EN GND VOUT
HPWR_EN
+5V

Power Management IC (PMIC)

Sheet: PMIC
File: PMIC.sch
3.3V_EPS_STM 3.3V_EPS_CAN 3.3V_EPS_MRAM GND
3V3_STM_CORE 3V3_CAN 3V3_MRAM GND
CANH CANL UART_TXO UART_RXI RST
CANH CANL UART_TXO UART_RXI EPS_WATCHDOG

OUT=0.6*IN
VOUT1 100K R33 GND 150K R34
VOUT2 100K R42 GND 150K R43
SOLAR_ADC1 SOLAR_ADC2 SOLAR_ADC3 SOLAR_ADC4 SOLAR_ADC5 SOLAR_ADC6
ADC1_IN1 ADC1_IN2 ADC1_IN3 ADC1_IN4 ADC1_IN7 ADC1_IN8 ADC1_IN9 ADC1_IN10 ADC1_IN11 ADC1_IN12

3.3V_EPS_STM
R16 100K R32 100K R47 100K
R12 100K R18 100K R46 100K
R13 100K GND
PG_SOLAR BC_1_CHRG BC_2_CHRG BC_1_SHDN BC_2_SHDN BC_1_SUSP BC_2_SUSP BC_1_POL BC_2_POL HPWR_EN PG_3V3 IDEAL_EN1 IDEAL_EN2
GPIO_1 GPIO_2 GPIO_3 GPIO_4 GPIO_5 GPIO_6 GPIO_7 GPIO_8 GPIO_9 GPIO_10 GPIO_11 GPIO_12 GPIO_13 GPIO_14

PWR1_1_ON PWR1_2_ON PWR1_3_ON PWR1_4_ON PWR1_5_ON PWR1_6_ON PWR1_7_ON PWR1_8_ON PWR1_9_ON PWR1_10_ON PWR1_11_ON PWR1_12_ON PWR1_13_ON PWR1_14_ON PWR1_15_ON PWR1_16_ON PWR2_1_ON PWR2_2_ON
INT_1 INT_2 INT_3 INT_4 INT_5 INT_6 INT_7 INT_8 INT_9 INT_10 INT_11 INT_12 INT_13 INT_14 INT_15

IDEAL_WARN2 IDEAL_WARN1 IDEAL_STATUS1 IDEAL_STATUS2
R50 100K R51 100K R52 100K
3.3V_EPS_STM

Current Monitors & Load switching

Sheet: CURRENT_MONITORS
File: CURRENT_MONITORS.sch
+3.3V +3.3V
PWR1 VIO
PWR1_1_ON PWR1_2_ON PWR1_3_ON PWR1_4_ON PWR1_5_ON PWR1_6_ON PWR1_7_ON PWR1_8_ON PWR1_9_ON PWR1_10_ON PWR1_11_ON PWR1_12_ON PWR1_13_ON PWR1_14_ON PWR1_15_ON PWR1_16_ON
PWR1_1 PWR1_2 PWR1_3 PWR1_4 PWR1_5 PWR1_6 PWR1_7 PWR1_8 PWR1_9 PWR1_10 PWR1_11 PWR1_12 PWR1_13 PWR1_14 PWR1_15 PWR1_16
3.3V_STM_CORE 3.3V_GPS 3.3V_MRAM 3.3V_AVI_CAN 3.3V_ACS_LOGIC 3.3V_GYRO 3.3V_MAG 3.3V_CLK 3.3V_9 3.3V_10 3.3V_11 3.3V_12 3.3V_EPS_STM 3.3V_EPS_CAN 3.3V_EPS_MRAM 3.3V_16
RST1_1 RST1_2 RST1_3 RST1_4 RST1_5 RST1_6 RST1_7 RST1_8
RST1_9 RST1_10 RST1_11 RST1_12 RST1_13 RST1_14 RST1_15 RST1_16
AVI_EXTRN_RST
+5V
PWR2
PWR2_1_ON PWR2_2_ON
PWR2_1 PWR2_2
GND

Interboard Connector

Sheet: INTERBOARD_CONNECTOR
File: INTERBOARD_CONNECTOR.sch
3V3_1 3V3_2 3V3_3 3V3_4 3V3_5 3V3_6 3V3_7 3V3_8 3V3_9 3V3_10 3V3_11 3V3_12
5V0_1 5V0_2
CANH CANL UART_RXI UART_TXO
UART_A_TXO UART_A_RXI SPARE_1 SPARE_2 SPARE_3 SPARE_4 UART_B_TXO UART_B_RXI
SPARE_5 UART_B_CTS UART_B_RTS
AVI_RESET EPS_RESET
GND
AVI_EXTRN_RST 0 R57
EPS_EXTRN_RST 0 R58

EPS Reset Triggers
+3.3V
C19 0.1uF 25V GND
C20 0.1uF 25V GND
EPS_WATCHDOG
U6 74LVC1G07
U7 74LVC1G07
GND

H1 MountingHole
H2 MountingHole_Pad
H3 MountingHole_Pad
H4 MountingHole_Pad
H5 MountingHole_Pad
GND
FID4 Fiducial

Sheet: /
File: EPS.sch
Title: EPS
Size: B | Date: 2020-10-11 | **Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1 | Id: 1/39

NRVB120VLSFT1G

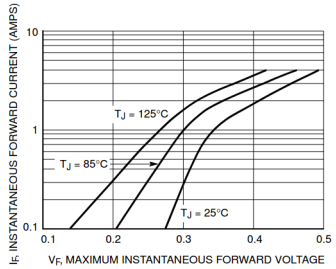


Figure 2. Maximum Forward Voltage

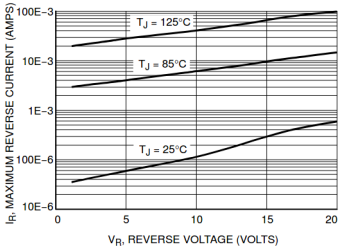
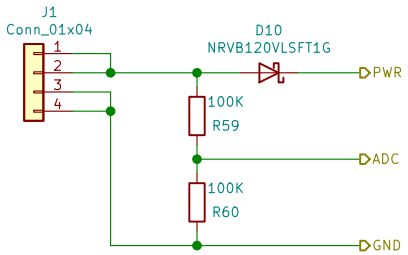
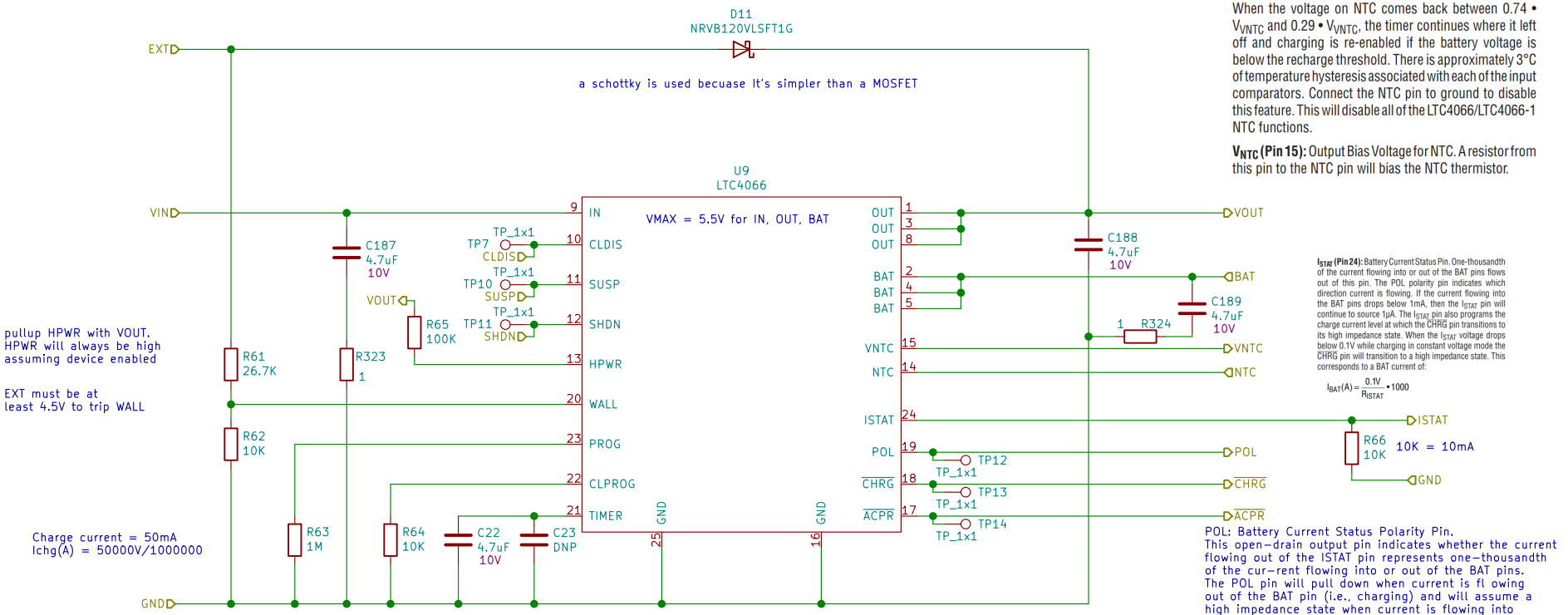


Figure 4. Maximum Reverse Current



I used to use Molex Pico Lock:
5040500491
https://www.digikey.com/en/products/detail/molex/5040500491/4357649

Sheet: /SOLAR_INPUT/ File: SOLAR_INPUT.sch		
Title: Solar Input		
Size: A	Date: 2020-08-09	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 2/39



NTC (Pin 14): Input to the NTC Thermistor Monitoring Circuits. Under normal operation, tie a thermistor from the NTC pin to ground and a resistor of equal value from NTC to V_{NTC}. When the voltage on this pin is above 0.74 • V_{VNTC} (Cold, 0°C) or below 0.29 • V_{VNTC} (Hot, 50°C) the timer is suspended, but not cleared, the charging is disabled and the $\overline{CHRG}$ pin remains in its former state. When the voltage on NTC comes back between 0.74 • V_{VNTC} and 0.29 • V_{VNTC}, the timer continues where it left off and charging is re-enabled if the battery voltage is below the recharge threshold. There is approximately 3°C of temperature hysteresis associated with each of the input comparators. Connect the NTC pin to ground to disable this feature. This will disable all of the LTC4066/LTC4066-1 NTC functions.

V_{NTC} (Pin 15): Output Bias Voltage for NTC. A resistor from this pin to the NTC pin will bias the NTC thermistor.

I_{STAT} (Pin 24): Battery Current Status Pin. One-thousandth of the current flowing into or out of the BAT pins flows out of this pin. The POL polarity pin indicates which direction current is flowing. If the current flowing into the BAT pins drops below 1mA, then the I_{STAT} pin will continue to source 1µA. The I_{STAT} pin also programs the charge current level at which the $\overline{CHRG}$ pin transitions to its high impedance state. When the I_{STAT} voltage drops below 0.1V while charging in constant voltage mode the $\overline{CHRG}$ pin will transition to a high impedance state. This corresponds to a BAT current of:

$$I_{BAT}(A) = \frac{0.1V}{R_{ISTAT}} \cdot 1000$$

POL: Battery Current Status Polarity Pin.
This open-drain output pin indicates whether the current flowing out of the ISTAT pin represents one-thousandth of the cur-rent flowing into or out of the BAT pins. The POL pin will pull down when current is fl owing out of the BAT pin (i.e., charging) and will assume a high impedance state when current is flowing into the BAT pin (i.e., ideal diode).

CHRG: Open-Drain Charge Status Output.
When the battery is beingcharged, the CHRG pin is pulled low by an internal N-channel MOSFET. When the timer runs out or the charge current drops below a programmable current level or the input supply or output supply is removed, the CHRG pin is forced to a high impedance state.

ACPR: Wall Adapter present. Active Low open drain.
Indicates wall adapter present.
Disabled if IN==OUT==BAT==0V or shutdown

CLDIS (Pin 10): Current Limit Disable. This logic input is used to disable the input current limit programmed by CLPROG. A voltage greater than 1.2V on the pin will set the current limit to $I_{IN(MAX)}$ (typically 2.6A). A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the input is not being driven externally.

SUSP (Pin 11): Suspend Mode Input. Pulling this pin above 1.2V will disable the power path from IN to OUT. The supply current from IN will be reduced to comply with the USB specification for Suspend mode. Both the ability to charge the battery from OUT and the ideal diode function (from BAT to OUT) will remain active. Suspend mode will reset the charge timer if V_{OUT} is less than V_{BAT} while in suspend mode. If V_{OUT} is kept greater than V_{BAT}, such as when a wall adapter is present, the charge timer will not be reset when the part is put in suspend. A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the pin is not being driven externally.

SHDN (Pin 12): Shutdown Input. Pulling this pin greater than 1.2V will disable the entire part and place it in a low supply current mode of operation. All power paths will be disabled. A weak pull-down current is internally applied to this pin to ensure it is enabled at power-up when the pin is not being driven externally.

HPWR (Pin 13): High Power Select. This logic input is used to control the input current limit. A voltage greater than 1.2V on the pin will set the input current limit to 100% of the current programmed by the CLPROG pin. A voltage less than 0.4V on the pin will set the input current limit to 20% of the current programmed by the CLPROG pin. A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the pin is not being driven externally.

TIMER (Pin 21): Timer Capacitor. Placing a capacitor, C_{TIMER}, to GND sets the timer period. The timer period is:

$$t_{TIMER}(Hours) = \frac{C_{TIMER} \cdot R_{PROG} \cdot 3Hours}{0.1\mu F \cdot 100k}$$

Charge time is increased if charge current is reduced due to load current, thermal regulation and current limit selection (HPWR). Shorting the TIMER pin to GND disables the battery charging functions.

CLPROG (Pin 22): Current Limit Program and Input Current Monitor. Connecting a resistor, R_{CLPROG}, to ground programs the input to output current limit. The current limit is programmed as follows:

$$I_{CL}(A) = \frac{1000V}{R_{CLPROG}}$$

In USB applications the resistor R_{CLPROG} should be set to no less than 2.1k.

The voltage on the CLPROG pin is always proportional to the current flowing through the IN to OUT power path. This current can be calculated as follows:

$$I_{IN}(A) = \frac{V_{CLPROG}}{R_{CLPROG}} \cdot 1000$$

PROG (Pin 23): Charge Current Program. Connecting a resistor, R_{PROG}, to ground programs the battery charge current. The battery charge current is programmed as follows:

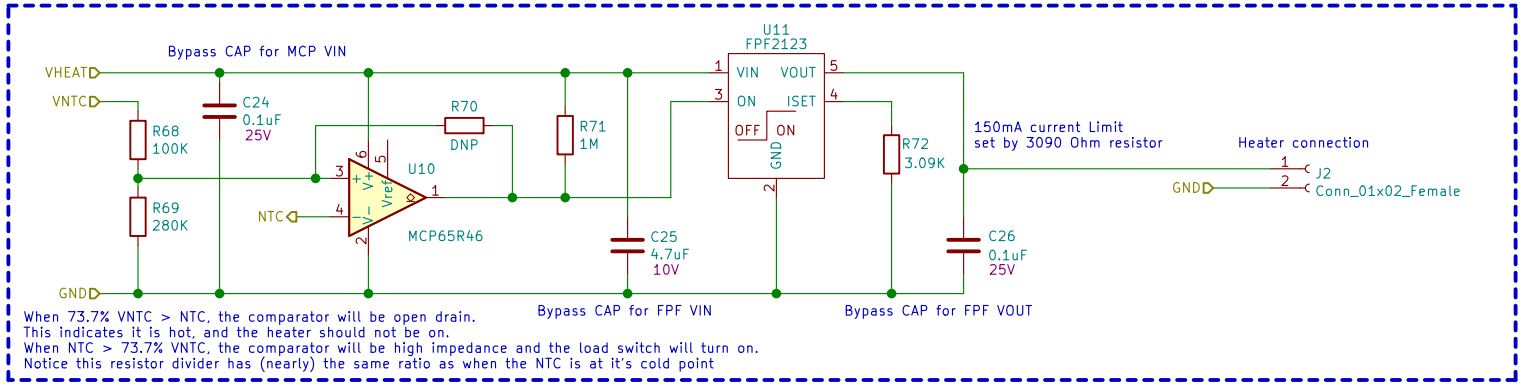
$$I_{CHG}(A) = \frac{50,000V}{R_{PROG}}$$

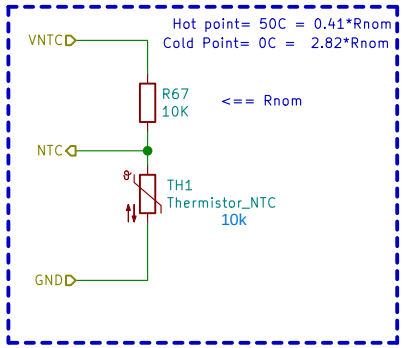
Sheet: /BATTERY_CHARGER/
File: BATTERY_CHARGER.sch

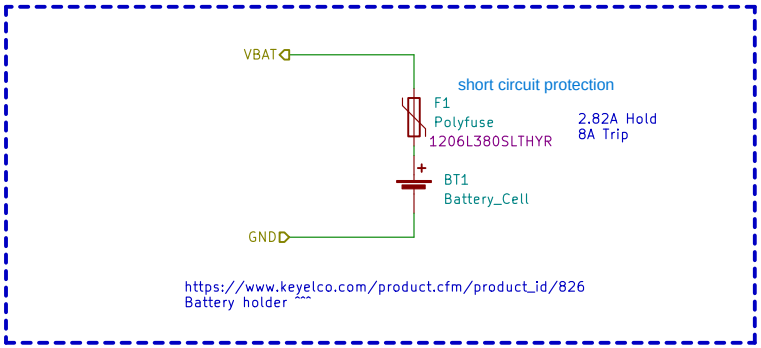
Title: LTC4066

Size: A	Date: 2020-08-09	Rev:
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 3/39

Battery heater control circuit



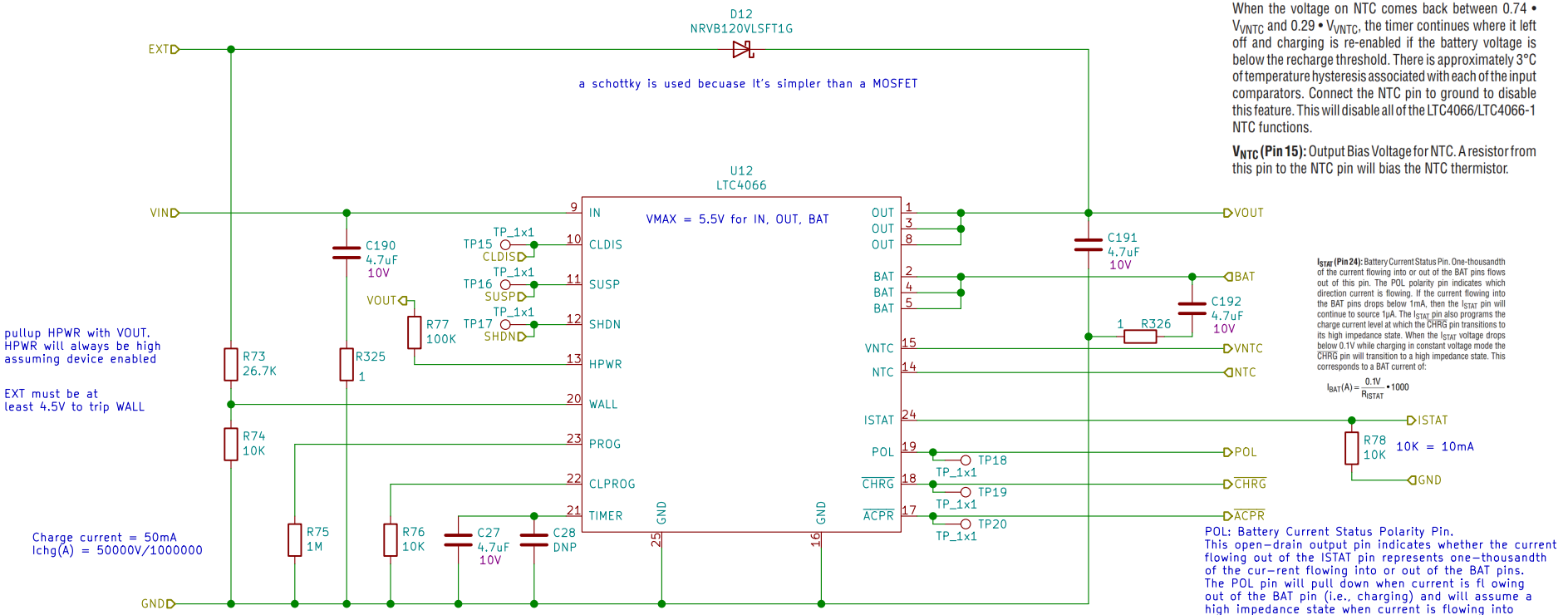




Battery & Fuse

NTC output for battery charger
and heater circuit (see above)

Sheet: /BATTERY/		
File: BATTERY.sch		
Title: Battery, Battery Heater, NTC		
Size: A	Date: 2020-08-11	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 4/39



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V_{NTC} (Pin 15): Output Bias Voltage for NTC. A resistor from this pin to the NTC pin will bias the NTC thermistor.

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Disabled if IN==OUT==BAT==0V or shutdown

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SUSP (Pin 11): Suspend Mode Input. Pulling this pin above 1.2V will disable the power path from IN to OUT. The supply current from IN will be reduced to comply with the USB specification for Suspend mode. Both the ability to charge the battery from OUT and the ideal diode function (from BAT to OUT) will remain active. Suspend mode will reset the charge timer if V_{OUT} is less than V_{BAT} while in suspend mode. If V_{OUT} is kept greater than V_{BAT}, such as when a wall adapter is present, the charge timer will not be reset when the part is put in suspend. A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the pin is not being driven externally.

SHDN (Pin 12): Shutdown Input. Pulling this pin greater than 1.2V will disable the entire part and place it in a low supply current mode of operation. All power paths will be disabled. A weak pull-down current is internally applied to this pin to ensure it is enabled at power-up when the pin is not being driven externally.

HPWR (Pin 13): High Power Select. This logic input is used to control the input current limit. A voltage greater than 1.2V on the pin will set the input current limit to 100% of the current programmed by the CLPROG pin. A voltage less than 0.4V on the pin will set the input current limit to 20% of the current programmed by the CLPROG pin. A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the pin is not being driven externally.

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$$t_{TIMER}(Hours) = \frac{C_{TIMER} \cdot R_{PROG} \cdot 3Hours}{0.1\mu F \cdot 100k}$$

Charge time is increased if charge current is reduced due to load current, thermal regulation and current limit selection (HPWR). Shorting the TIMER pin to GND disables the battery charging functions.

CLPROG (Pin 22): Current Limit Program and Input Current Monitor. Connecting a resistor, R_{CLPROG}, to ground programs the input to output current limit. The current limit is programmed as follows:

$$I_{CL}(A) = \frac{1000V}{R_{CLPROG}}$$

In USB applications the resistor R_{CLPROG} should be set to no less than 2.1k.

The voltage on the CLPROG pin is always proportional to the current flowing through the IN to OUT power path. This current can be calculated as follows:

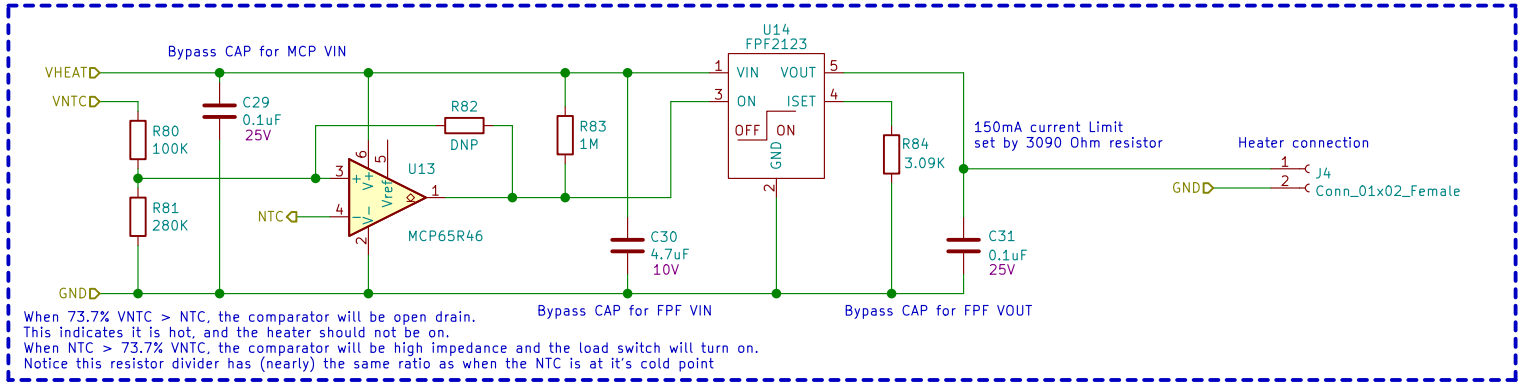
$$I_{IN}(A) = \frac{V_{CLPROG}}{R_{CLPROG}} \cdot 1000$$

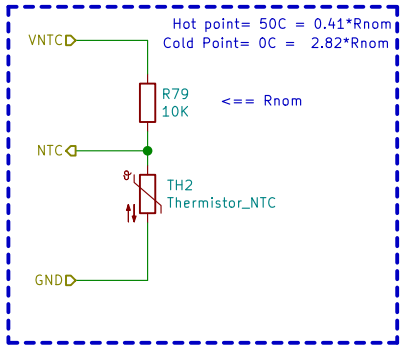
PROG (Pin 23): Charge Current Program. Connecting a resistor, R_{PROG}, to ground programs the battery charge current. The battery charge current is programmed as follows:

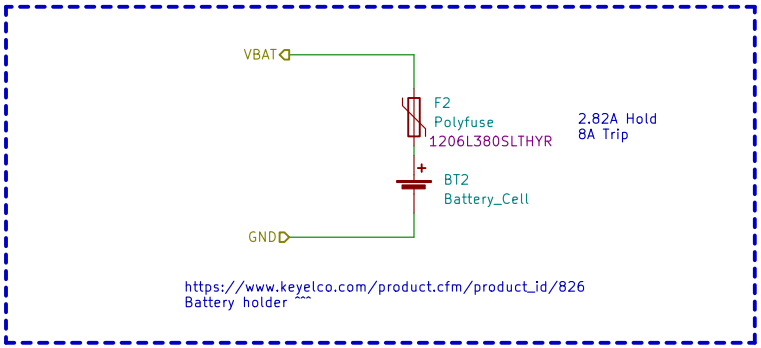
$$I_{CHG}(A) = \frac{50,000V}{R_{PROG}}$$

Sheet: /sheet5F4CFCDE/		
File: BATTERY_CHARGER.sch		
Title: LTC4066		
Size: A	Date: 2020-08-09	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 5/39

Battery heater control circuit







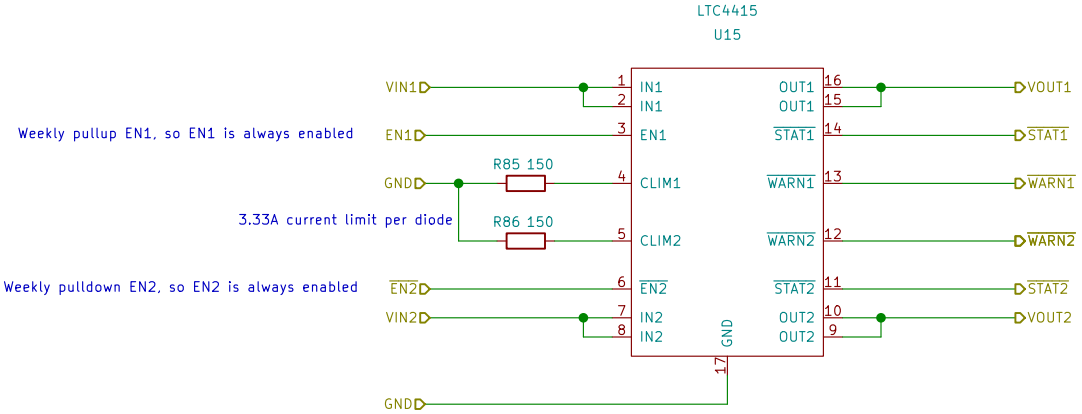
Battery & Fuse

NTC output for battery charger
and heater circuit (see above)

Sheet: /sheet5F4CFCDF/		
File: BATTERY.sch		
Title: Battery, Battery Heater, NTC		
Size: A	Date: 2020-08-11	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 6/39

STAT
Open−drain output pulls down during forward diode conduction.
This pin can be left open or grounded when not used.

WARN
Open−drain output pulls down when the diode current exceeds its current limit or die temperature is close to thermal shutdown.



Maximum 4A current limit for each diode

Voltage Threasholds for the Enable pins:
Venth = 0.8V with Venhyst = 0.055V

Current Limit Setting

The output current limit of each diode can be set independently by connecting resistors from the current limit adjust pins CLIM1 and CLIM2 to ground. The current out of the CLIM1 and CLIM2 pins are 1/1000 of the ideal diode output currents I_{OUT1} and I_{OUT2} respectively. When the load currents increase so that the CLIM1 or CLIM2 pin voltages exceeds 0.5V the LTC4415 detects an overcurrent condition and regulates the current to a fixed value. The required value of resistor R_{CLIM} for output current limit of I_{LIM} is calculated as follows:

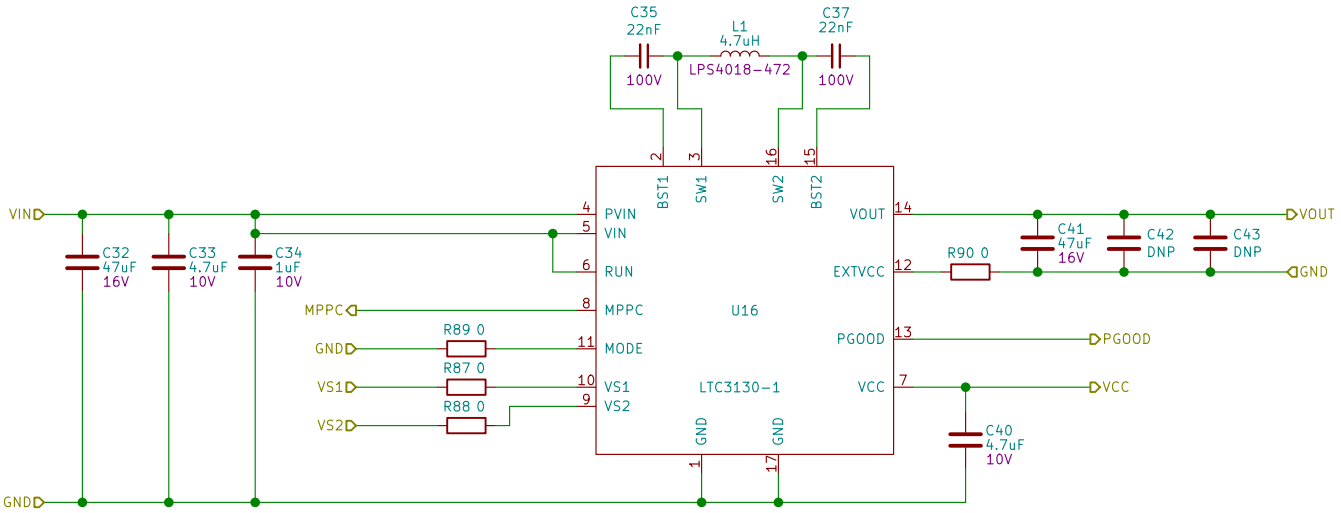
$$R_{CLIM} = 1000 \bullet \frac{0.5V}{I_{LIM}}$$

The allowed range of R_{CLIM} is 125Ω to 1000Ω unless the CLIM1/CLIM2 pins are shorted to GND, in which case the LTC4415 limits the load current using a fixed internal current limit of 6A.

Sheet: /sheet5F71F776/
File: IDEAL_DIODE.sch

Title: LTC4415

Size: A	Date: 2020−09−06	**Rev:**
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1		Id: 7/39



Maximum Power Point Control (MPPC)

The MPPC input of the LTC3130/LTC3130-1 can be used with an optional external voltage divider to dynamically adjust the commanded inductor current in order to maintain a minimum input voltage when using high resistance sources, such as photovoltaic panels, so as to maximize input power transfer and prevent V_{IN} from dropping too low under load.

Referring to Figure 4, the MPPC pin is internally connected to the noninverting input of a g_m amplifier, whose inverting input is connected to the 1.0V reference. If the voltage at MPPC, using the external voltage divider, falls below the reference voltage, the output of the amplifier pulls the internal VC node low. This reduces the commanded average inductor current so as to reduce the input current and regulate V_{IN} to the programmed minimum voltage, as given by:

$$V_{IN(MPPC)} = 1.00V \bullet \left(1 + \frac{R5}{R6}\right)$$

Note that external compensation should not be required for MPPC loop stability if the input filter capacitor, C_{IN}, is at least 22µF.

The MPPC divider resistor values can be in the MΩ range so as to minimize the input current in very low power applications. However, stray capacitance and noise pickup on the MPPC pin must also be minimized. If the MPPC function is not required, the MPPC pin should be tied to V_{CC}.

Beware of adding a noise filter capacitor to the MPPC pin, as the added filter pole may cause the MPPC control loop to be unstable.

Note that because Burst Mode operation will be inhibited if the MPPC loop takes control, the converter will be operating in fixed frequency mode, and will therefore require a minimum of about 6mA of continuous input current to operate. For operation from weaker sources, such as small indoor solar panels, refer to the Applications Information section to see how the RUN pin may be programmed to control the converter in a hysteretic manner while providing an effective MPPC function by maintaining V_{IN} at the desired voltage. This technique can be used with sources as weak as 3µA (enough to power the IC in UVLO and the external RUN divider).

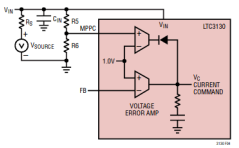
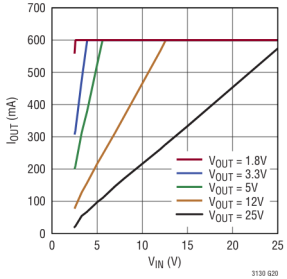


Figure 4. MPPC Amplifier with External Resistor Divider

Maximum Output Current vs V_{IN} and V_{OUT}



PGOOD is open drain.
Pulled low when VOUT is less than 7.5% programmed value
High-Z when VOUT is within 5% programmed value

MODE (Pin 11/Pin 11): Mode Select Pin.

MODE = Low (ground): Enables automatic Burst Mode operation

MODE = High (tie to V_{CC}): Fixed frequency PWM operation

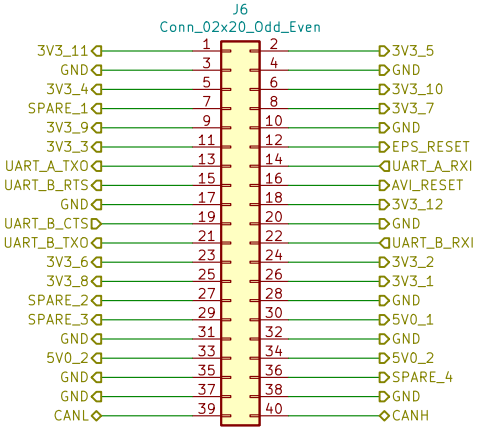
Table 1. V_{OUT} Program Settings for the LTC3130-1

VS2	VS1	V_{OUT}
0	0	1.8V
0	V_{CC}	3.3V
V_{CC}	0	5.0V
V_{CC}	V_{CC}	12V

Sheet: /SOLAR_MPPT_5V/
File: LTC3130.sch

Title: LTC3130

Size: A	Date: 2020-08-09	Rev:
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 8/39

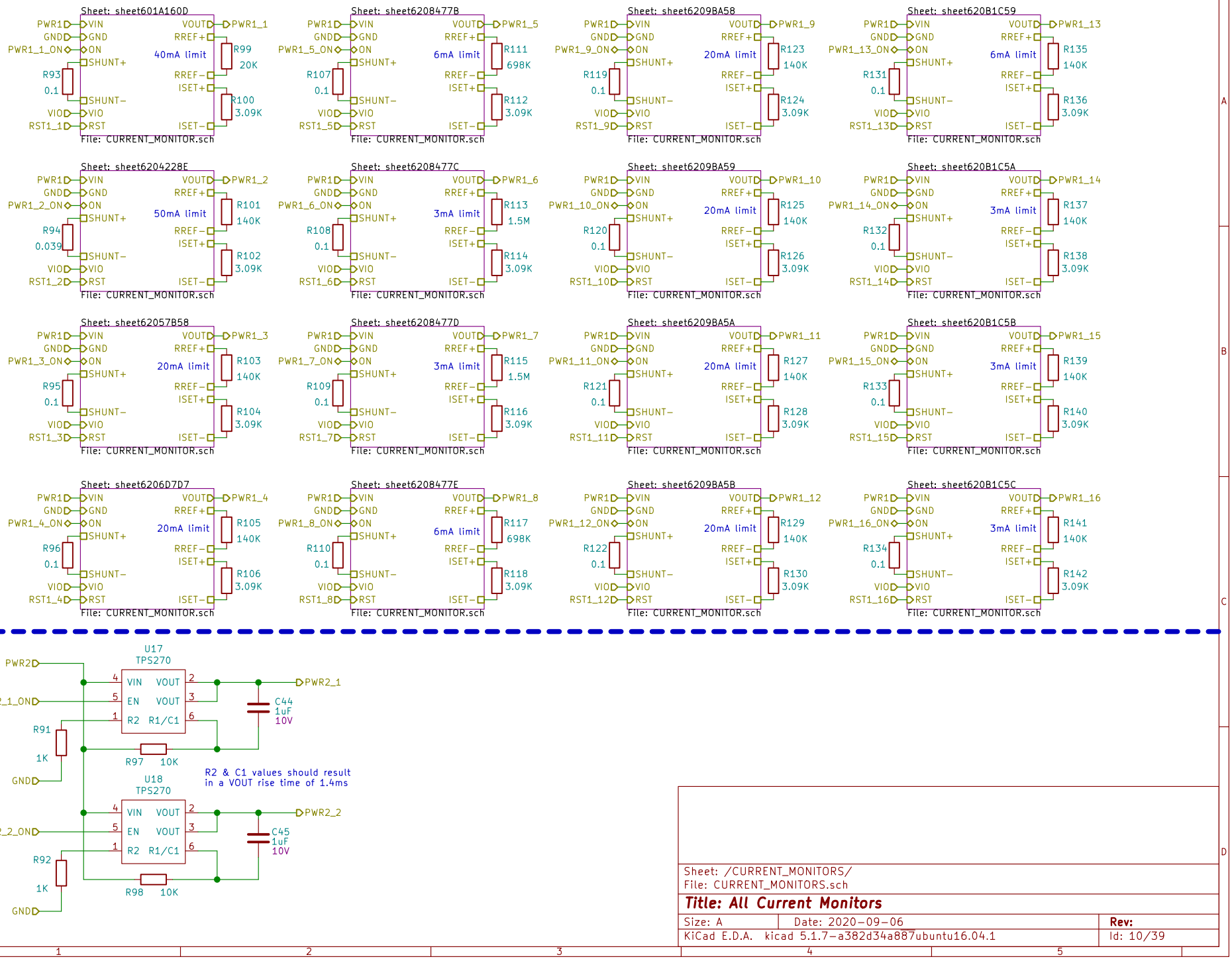


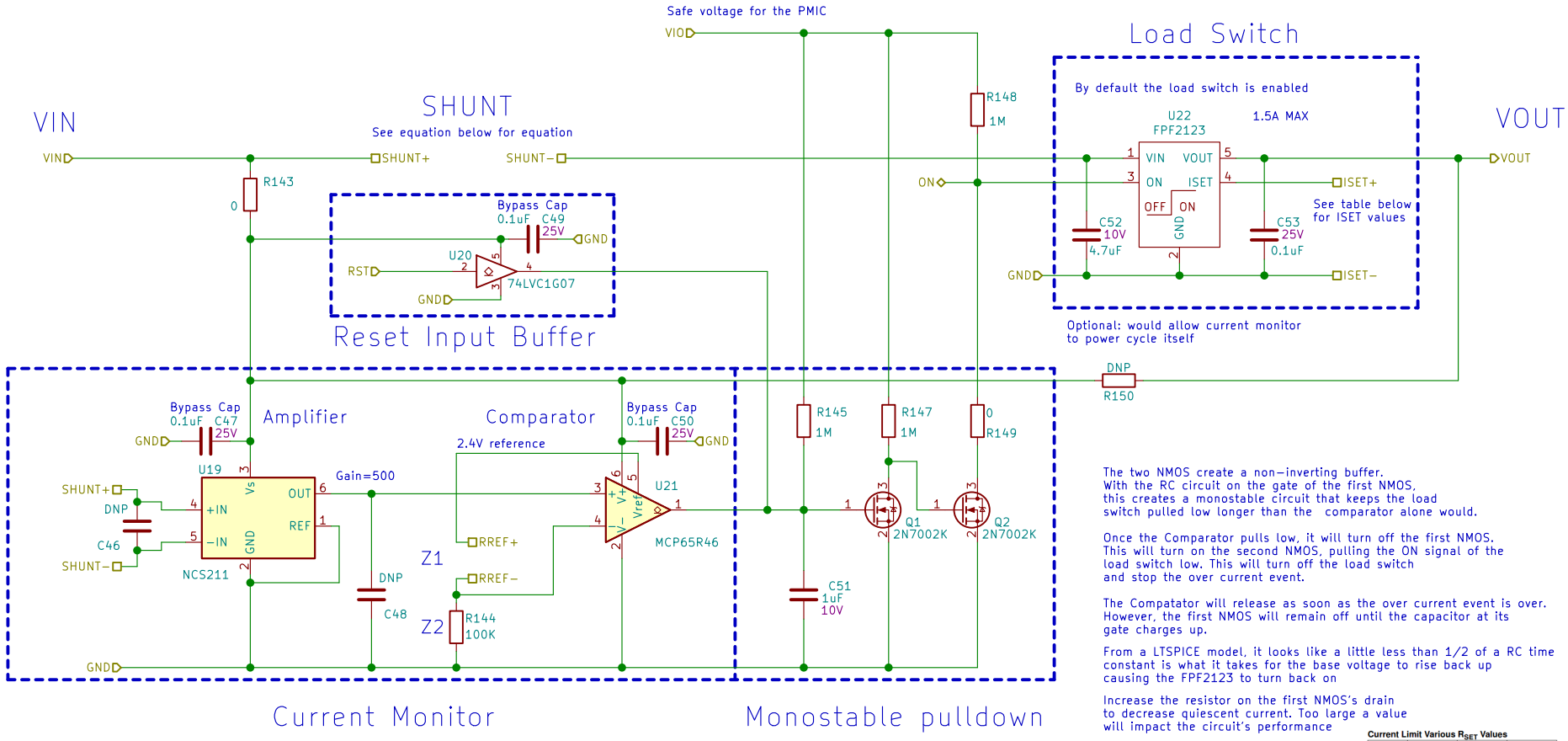
There are a lot of options that could work:
https://www.digikey.com/short/znc31r

Sheet: /INTERBOARD_CONNECTOR/
File: INTERBOARD_CONNECTOR.sch

Title: Current Monitor

Size: A	Date: 2020-05-25	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 9/39


Sheet: sheet601A160D
PWR1
VIN
GND
PWR1_1_ON
ON
SHUNT+
R93
0.1
SHUNT−
VIO
RST1_1
VOUT
PWR1_1
RREF+
40mA limit
R99
20K
RREF−
ISET+
R100
3.09K
ISET−
File: CURRENT_MONITOR.sch
Sheet: sheet6208477B
PWR1_5_ON
RST1_5
PWR1_5
6mA limit
R111
698K
R107
R112
Sheet: sheet6209BA58
PWR1_9_ON
RST1_9
PWR1_9
20mA limit
R123
140K
R119
R124
Sheet: sheet620B1C59
PWR1_13_ON
RST1_13
PWR1_13
6mA limit
R135
140K
R131
R136
Sheet: sheet6204228E
PWR1_2_ON
RST1_2
PWR1_2
50mA limit
R101
140K
R94
0.039
R102
3.09K
Sheet: sheet6208477C
PWR1_6_ON
RST1_6
PWR1_6
3mA limit
R113
1.5M
R108
R114
Sheet: sheet6209BA59
PWR1_10_ON
RST1_10
PWR1_10
20mA limit
R125
140K
R120
R126
Sheet: sheet620B1C5A
PWR1_14_ON
RST1_14
PWR1_14
3mA limit
R137
140K
R132
R138
Sheet: sheet62057B58
PWR1_3_ON
RST1_3
PWR1_3
20mA limit
R103
140K
R95
R104
Sheet: sheet6208477D
PWR1_7_ON
RST1_7
PWR1_7
3mA limit
R115
1.5M
R109
R116
Sheet: sheet6209BA5A
PWR1_11_ON
RST1_11
PWR1_11
20mA limit
R127
140K
R121
R128
Sheet: sheet620B1C5B
PWR1_15_ON
RST1_15
PWR1_15
3mA limit
R139
140K
R133
R140
Sheet: sheet6206D7D7
PWR1_4_ON
RST1_4
PWR1_4
20mA limit
R105
140K
R96
R106
Sheet: sheet6208477E
PWR1_8_ON
RST1_8
PWR1_8
6mA limit
R117
698K
R110
R118
Sheet: sheet6209BA5B
PWR1_12_ON
RST1_12
PWR1_12
20mA limit
R129
140K
R122
R130
Sheet: sheet620B1C5C
PWR1_16_ON
RST1_16
PWR1_16
3mA limit
R141
140K
R134
R142
U17
TPS270
PWR2
PWR2_1_ON
EN
R2
R1/C1
PWR2_1
C44
1uF
10V
R91
1K
R97
10K
GND
U18
PWR2_2_ON
PWR2_2
C45
R92
R98
R2 & C1 values should result
in a VOUT rise time of 1.4ms
Sheet: /CURRENT_MONITORS/
File: CURRENT_MONITORS.sch
Title: All Current Monitors
Size: A
Date: 2020-09-06
Rev:
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1
Id: 10/39



The two NMOS create a non−inverting buffer.
With the RC circuit on the gate of the first NMOS,
this creates a monostable circuit that keeps the load
switch pulled low longer than the comparator alone would.

Once the Comparator pulls low, it will turn off the first NMOS.
This will turn on the second NMOS, pulling the ON signal of the
load switch low. This will turn off the load switch
and stop the over current event.

The Compatator will release as soon as the over current event is over.
However, the first NMOS will remain off until the capacitor at its
gate charges up.

From a LTSPICE model, it looks like a little less than 1/2 of a RC time
constant is what it takes for the base voltage to rise back up
causing the FPF2123 to turn back on

Increase the resistor on the first NMOS's drain
to decrease quiescent current. Too large a value
will impact the circuit's performance

Current Limit Various R_{SET} Values

R_{SET} [Ω]	Min. Current Limit [mA]	Typ. Current Limit [mA]	Max. Current Limit [mA]
309	1120	1490	1860
340	1010	1350	1690
374	920	1230	1540
412	840	1120	1400
453	760	1010	1270
499	690	920	1150
549	630	840	1050
576	600	800	1000
604	570	760	950
732	470	630	790
887	390	520	650
1070	320	430	540
1300	260	350	440
1910	180	240	300
3090	110	150	190

Use this equation to select the current limit

Z1 = (Z2*(1−g/vref*r*i)) / (g/vref*r*i)

Where:
g = Gain
r = shunt resistance
i = max/trip current (in Amps)
Z1 = 'top' resistor in reference divider leg
Z2 = 'bottom' resistor in reference divider leg

When IN+ is greater than the reference voltage,
the comparator's open drain output turns on.

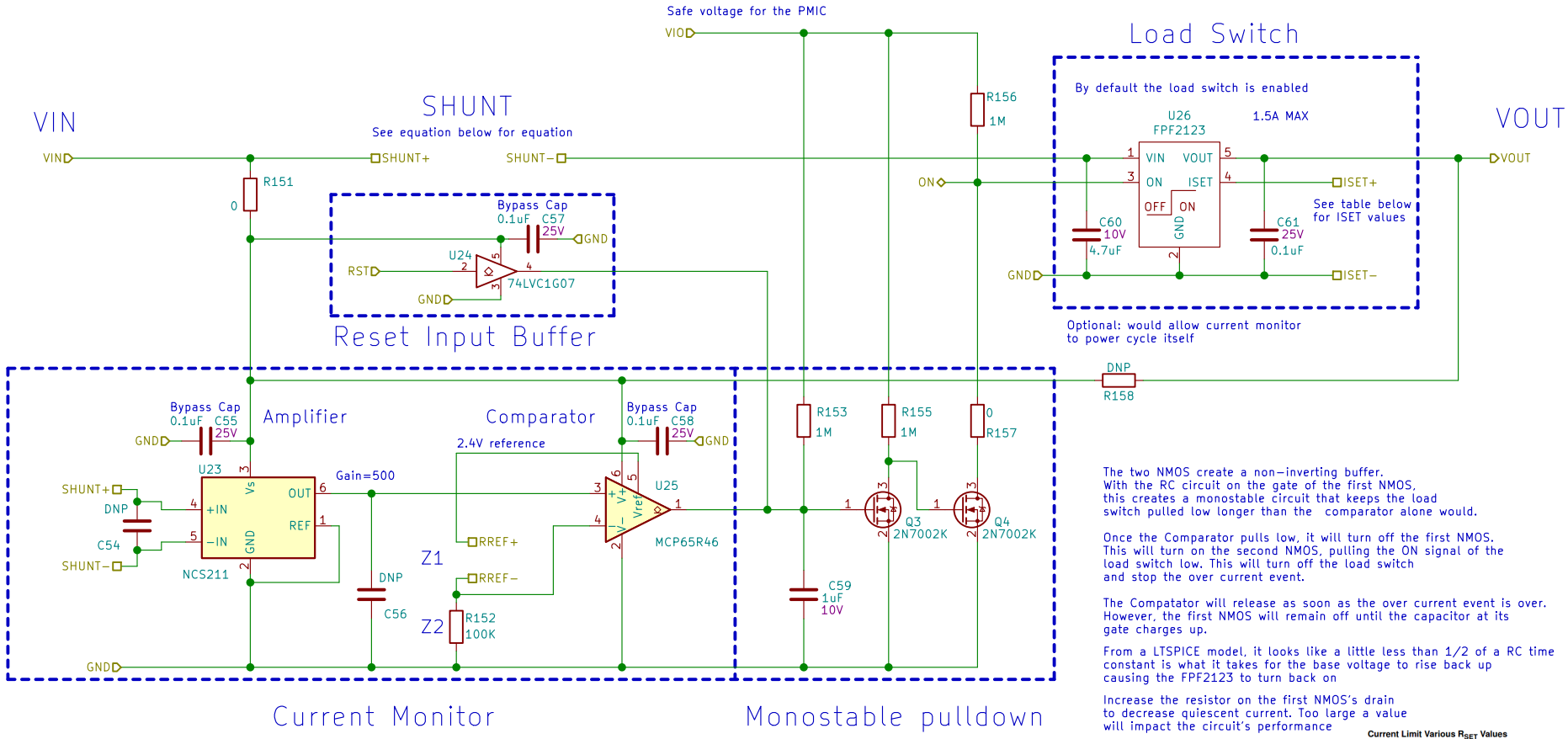
The MCP65R46 has two VRef voltages based on the package you get.
Either 2.4V or 1.2V

It's slightly adventageous to use the higher 2.4V Reference
instead of the 1.2V reference because we can get a larger range
of configurable trip currents

Sheet: /CURRENT_MONITORS/sheet601A160D/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A | Date: 2020−09−06 | **Rev:**
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1 | Id: 11/39



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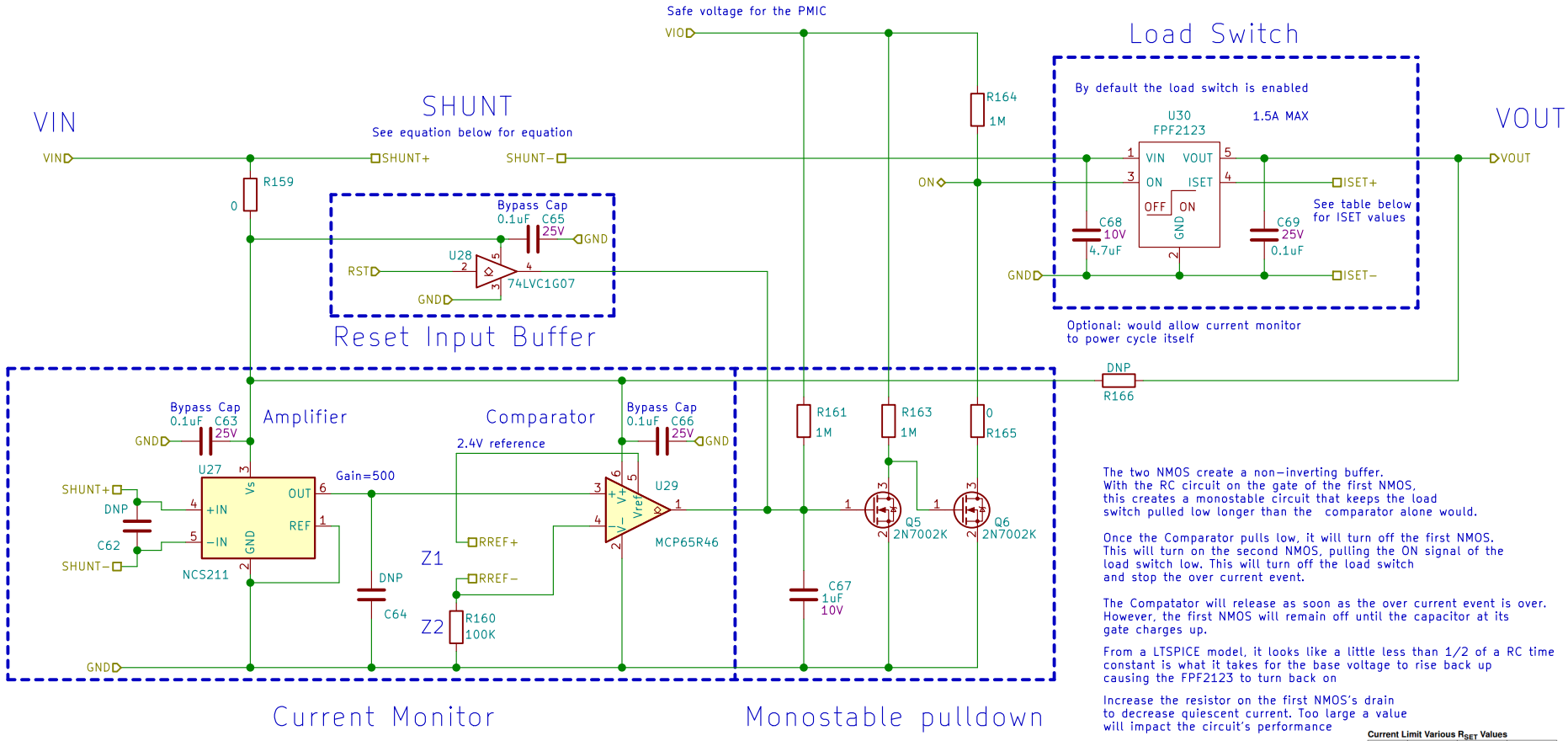
Sheet: /CURRENT_MONITORS/sheet6204228E/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A | Date: 2020−09−06 | **Rev:**
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1 | Id: 12/39



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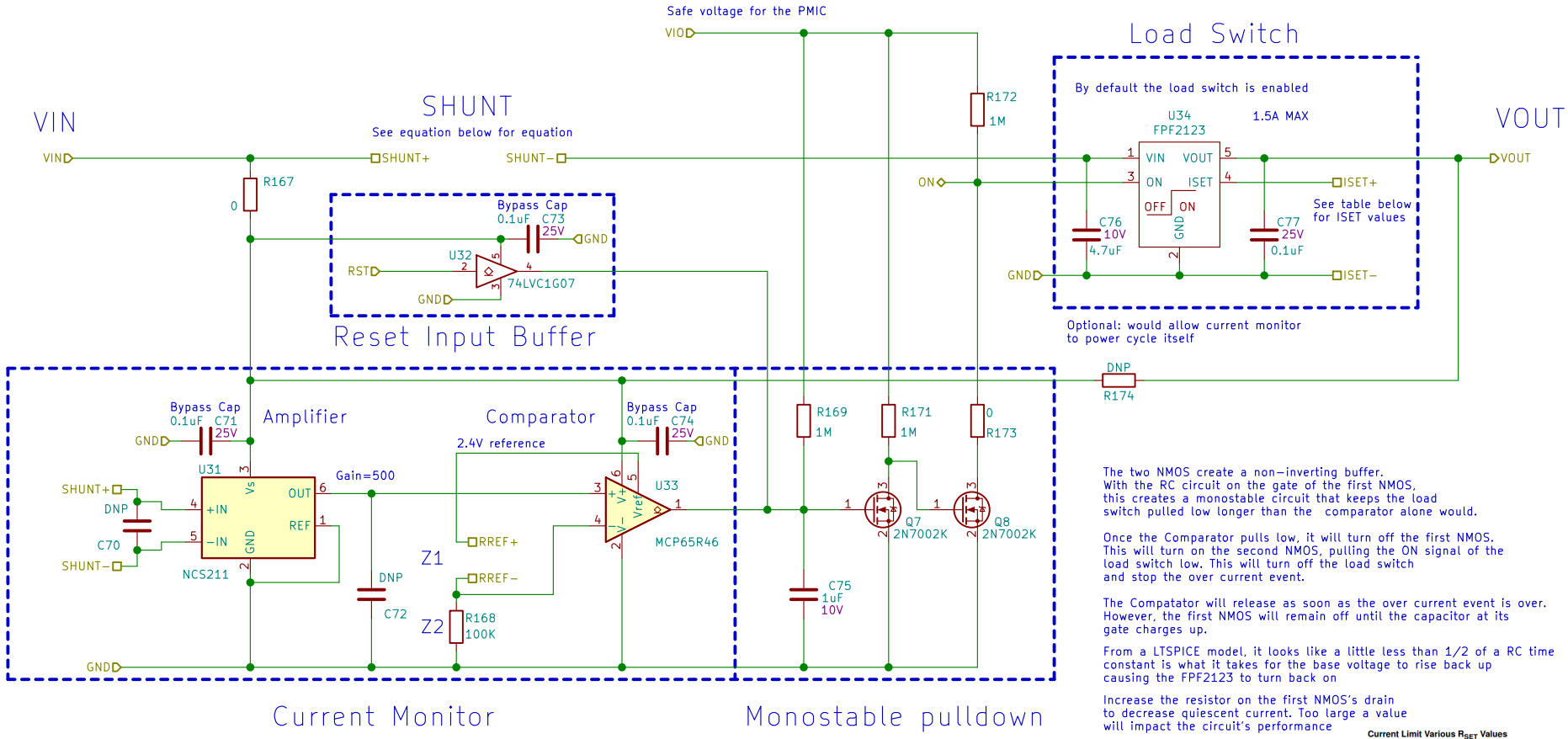
Sheet: /CURRENT_MONITORS/sheet62057B58/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A	Date: 2020−09−06	Rev:
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1		Id: 13/39



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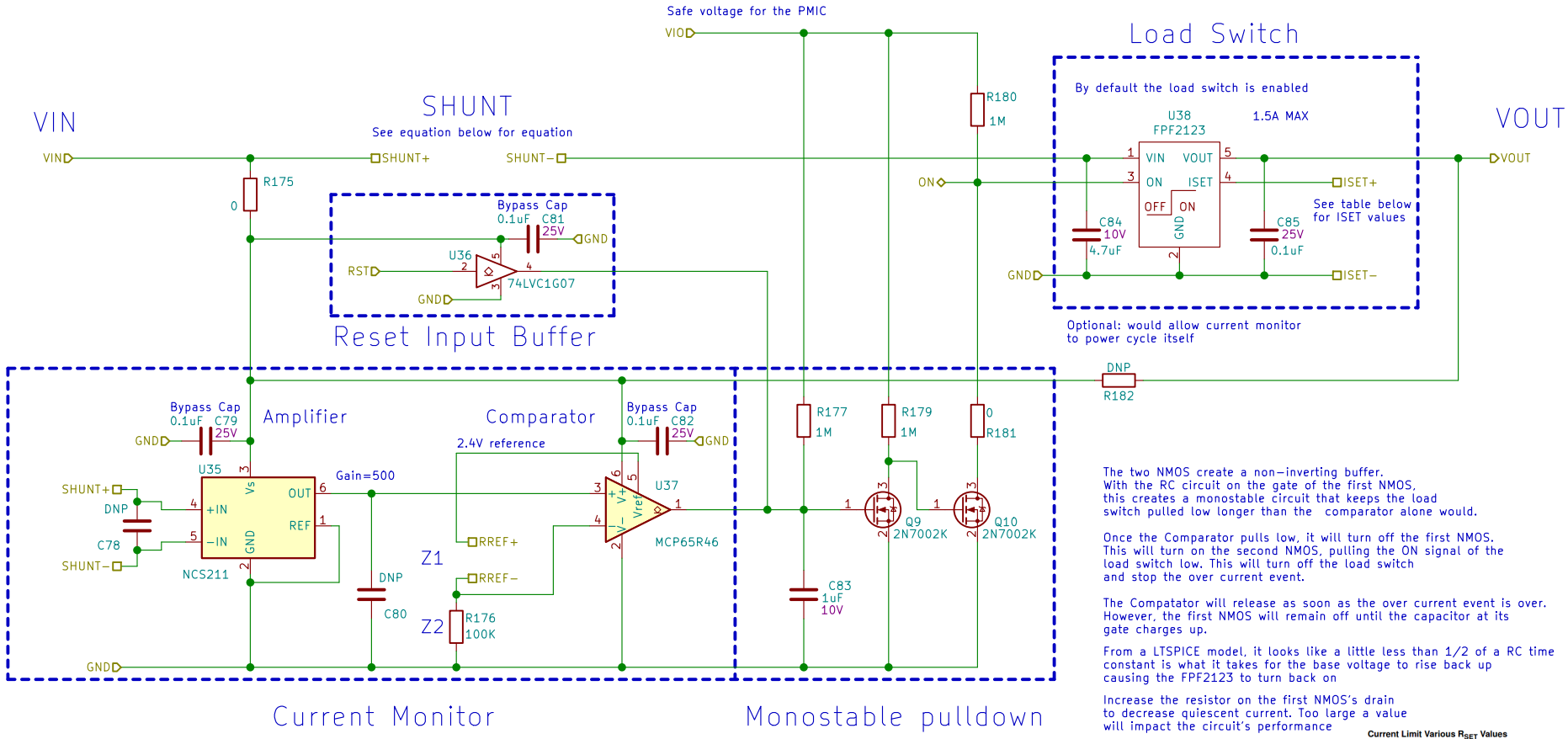
Sheet: /CURRENT_MONITORS/sheet6206D7D7/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A | Date: 2020−09−06 | **Rev:**
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1 | Id: 14/39



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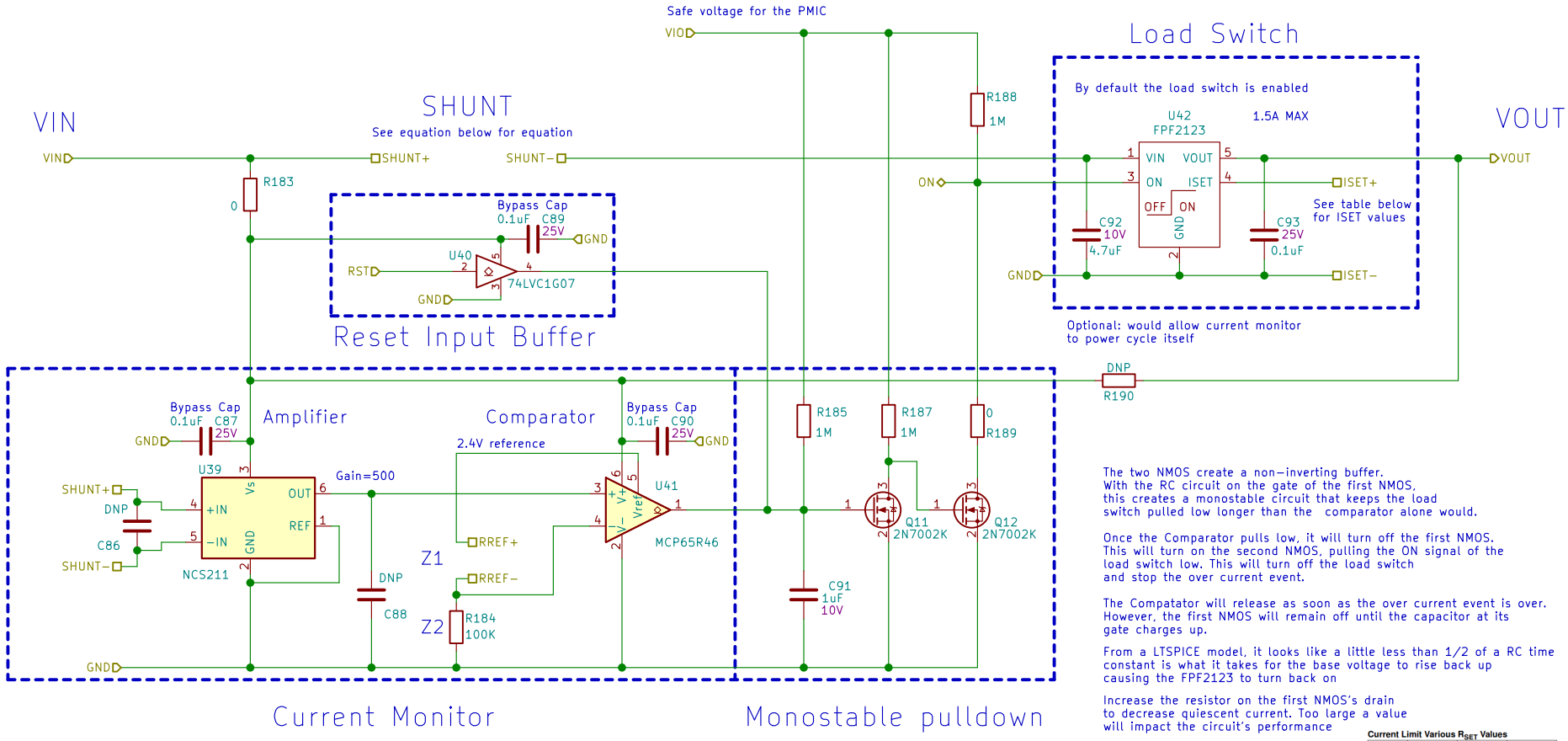
Sheet: /CURRENT_MONITORS/sheet6208477B/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A	Date: 2020−09−06	Rev:
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1		Id: 15/39



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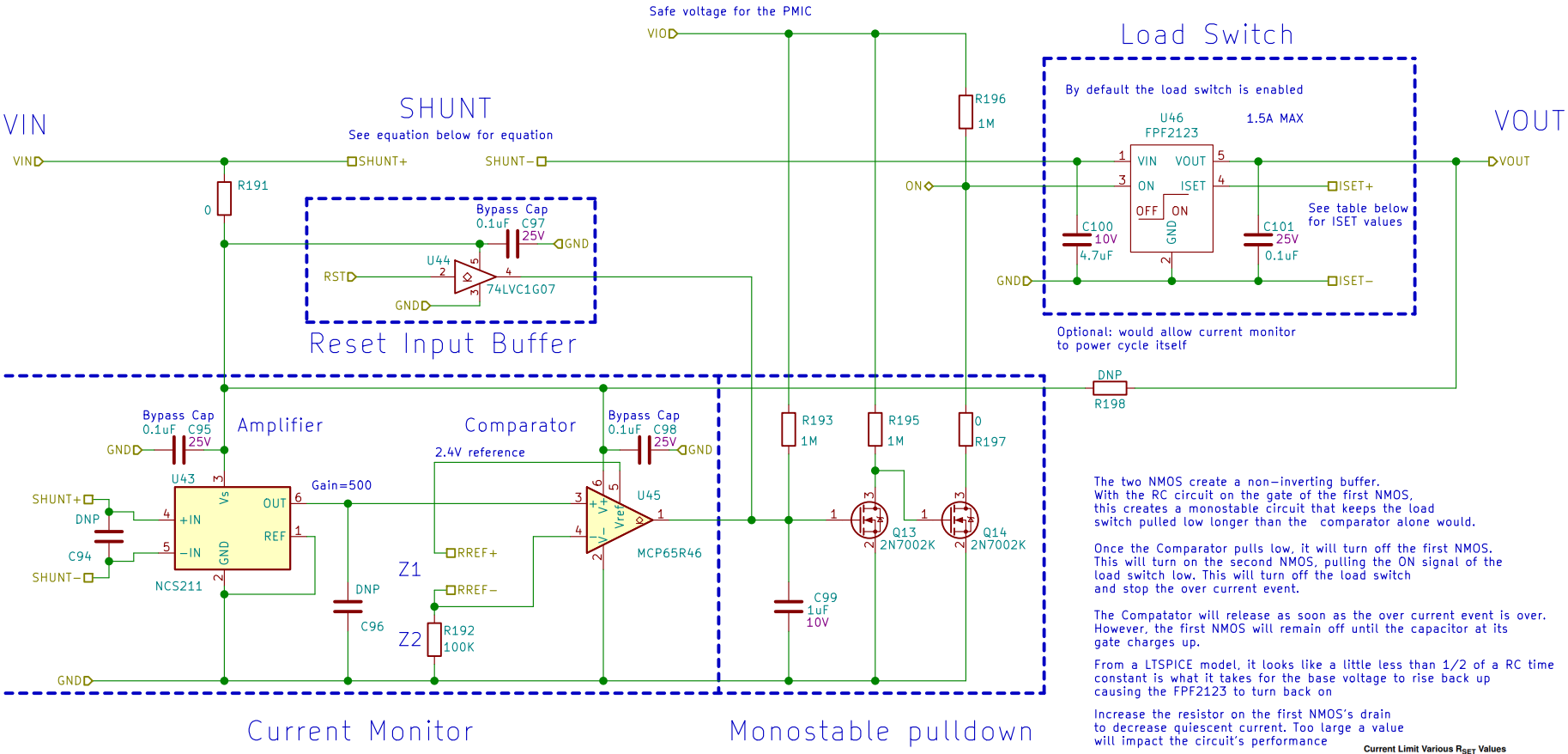
Sheet: /CURRENT_MONITORS/sheet6208477C/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A | Date: 2020−09−06 | **Rev:**
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1 | Id: 16/39



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From a LTSPICE model, it looks like a little less than 1/2 of a RC time
constant is what it takes for the base voltage to rise back up
causing the FPF2123 to turn back on

Increase the resistor on the first NMOS's drain
to decrease quiescent current. Too large a value
will impact the circuit's performance

Current Limit Various R_{SET} Values

R_{SET} [Ω]	Min. Current Limit [mA]	Typ. Current Limit [mA]	Max. Current Limit [mA]
309	1120	1490	1860
340	1010	1350	1690
374	920	1230	1540
412	840	1120	1400
453	760	1010	1270
499	690	920	1150
549	630	840	1050
576	600	800	1000
604	570	760	950
732	470	630	790
887	390	520	650
1070	320	430	540
1300	260	350	440
1910	180	240	300
3090	110	150	190

Use this equation to select the current limit

Z1 = (Z2*(1−g/vref*r*i)) / (g/vref*r*i)

Where:
g = Gain
r = shunt resistance
i = max/trip current (in Amps)
Z1 = 'top' resistor in reference divider leg
Z2 = 'bottom' resistor in reference divider leg

When IN+ is greater than the reference voltage,
the comparator's open drain output turns on.

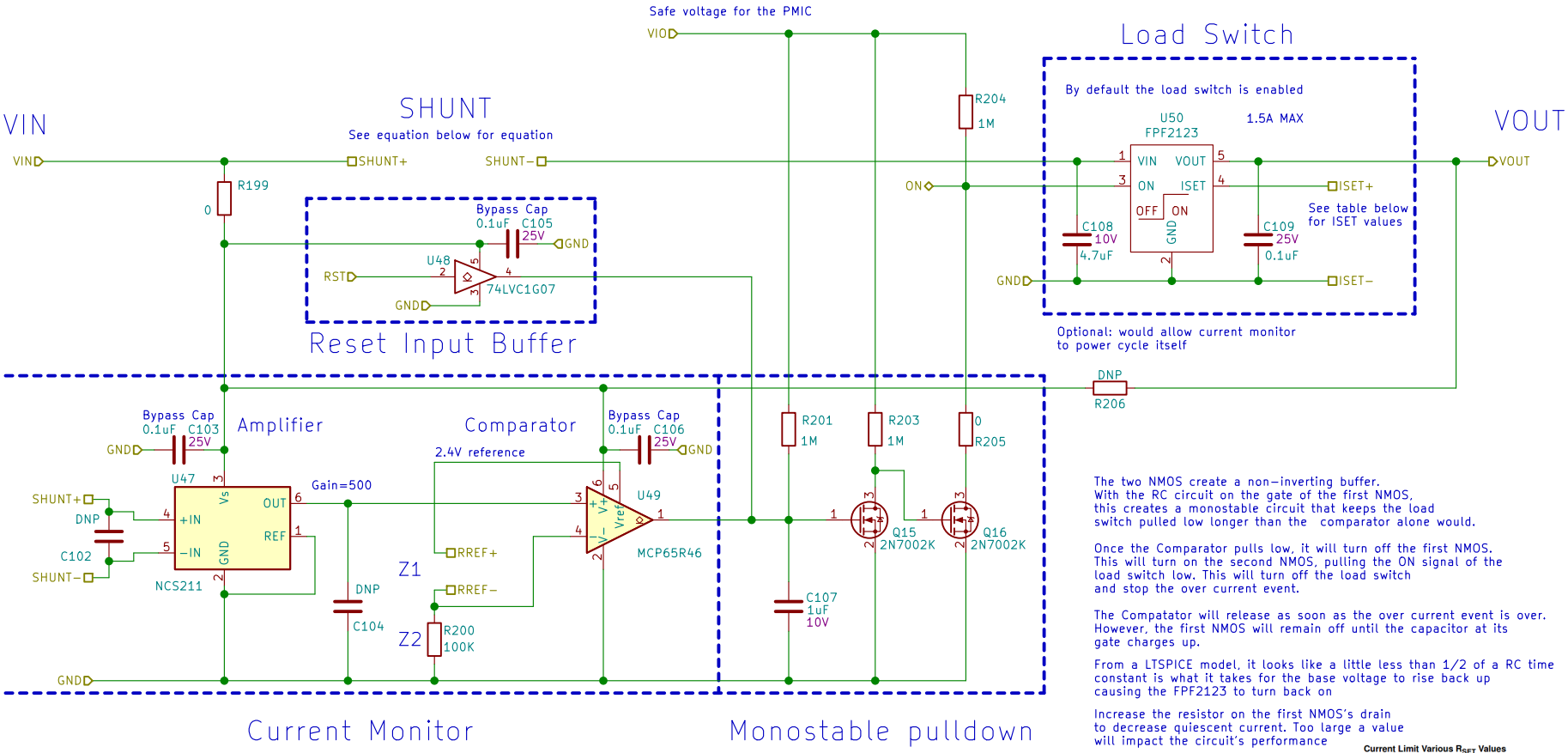
The MCP65R46 has two VRef voltages based on the package you get.
Either 2.4V or 1.2V

It's slightly adventageous to use the higher 2.4V Reference
instead of the 1.2V reference because we can get a larger range
of configurable trip currents

Sheet: /CURRENT_MONITORS/sheet6208477D/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A	Date: 2020−09−06	Rev:
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1		Id: 17/39



The two NMOS create a non−inverting buffer.
With the RC circuit on the gate of the first NMOS,
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switch pulled low longer than the comparator alone would.

Once the Comparator pulls low, it will turn off the first NMOS.
This will turn on the second NMOS, pulling the ON signal of the
load switch low. This will turn off the load switch
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The Compatator will release as soon as the over current event is over.
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576	600	800	1000
604	570	760	950
732	470	630	790
887	390	520	650
1070	320	430	540
1300	260	350	440
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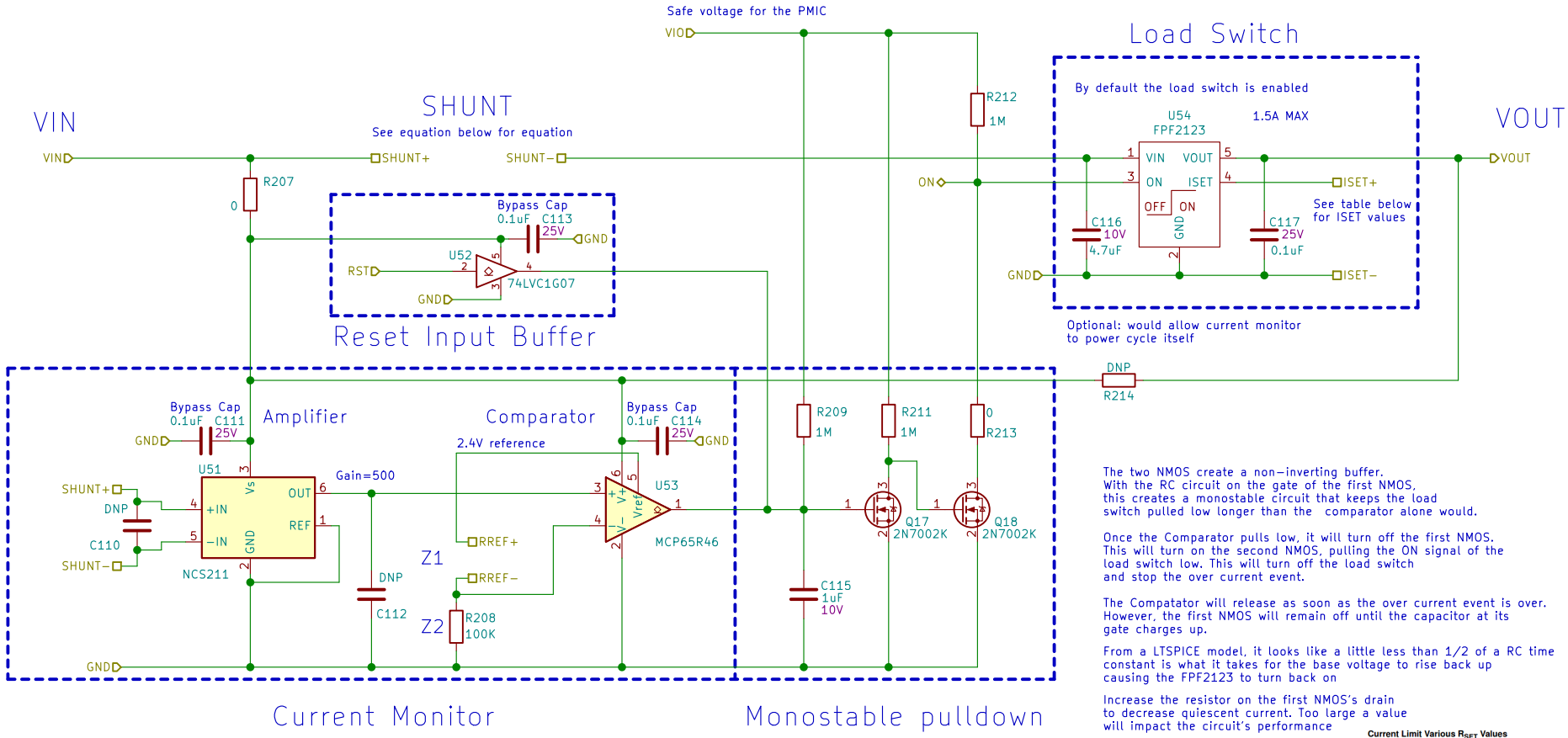
Sheet: /CURRENT_MONITORS/sheet6208477E/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A	Date: 2020−09−06	Rev:
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1		Id: 18/39



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R_{SET} [Ω]	Min. Current Limit [mA]	Typ. Current Limit [mA]	Max. Current Limit [mA]
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412	840	1120	1400
453	760	1010	1270
499	690	920	1150
549	630	840	1050
576	600	800	1000
604	570	760	950
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1070	320	430	540
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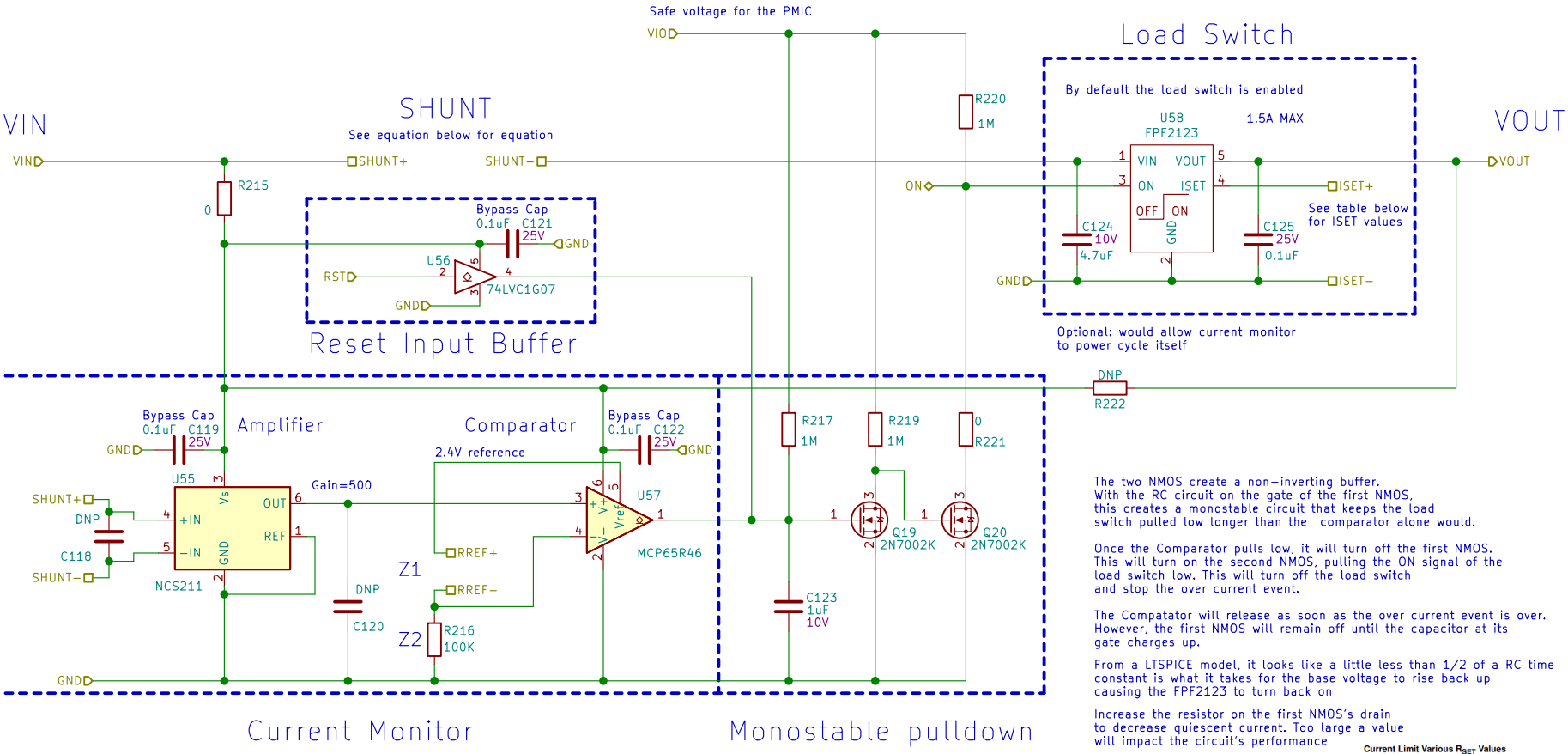
Sheet: /CURRENT_MONITORS/sheet6209BA58/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A	Date: 2020−09−06	Rev:
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1		Id: 19/39



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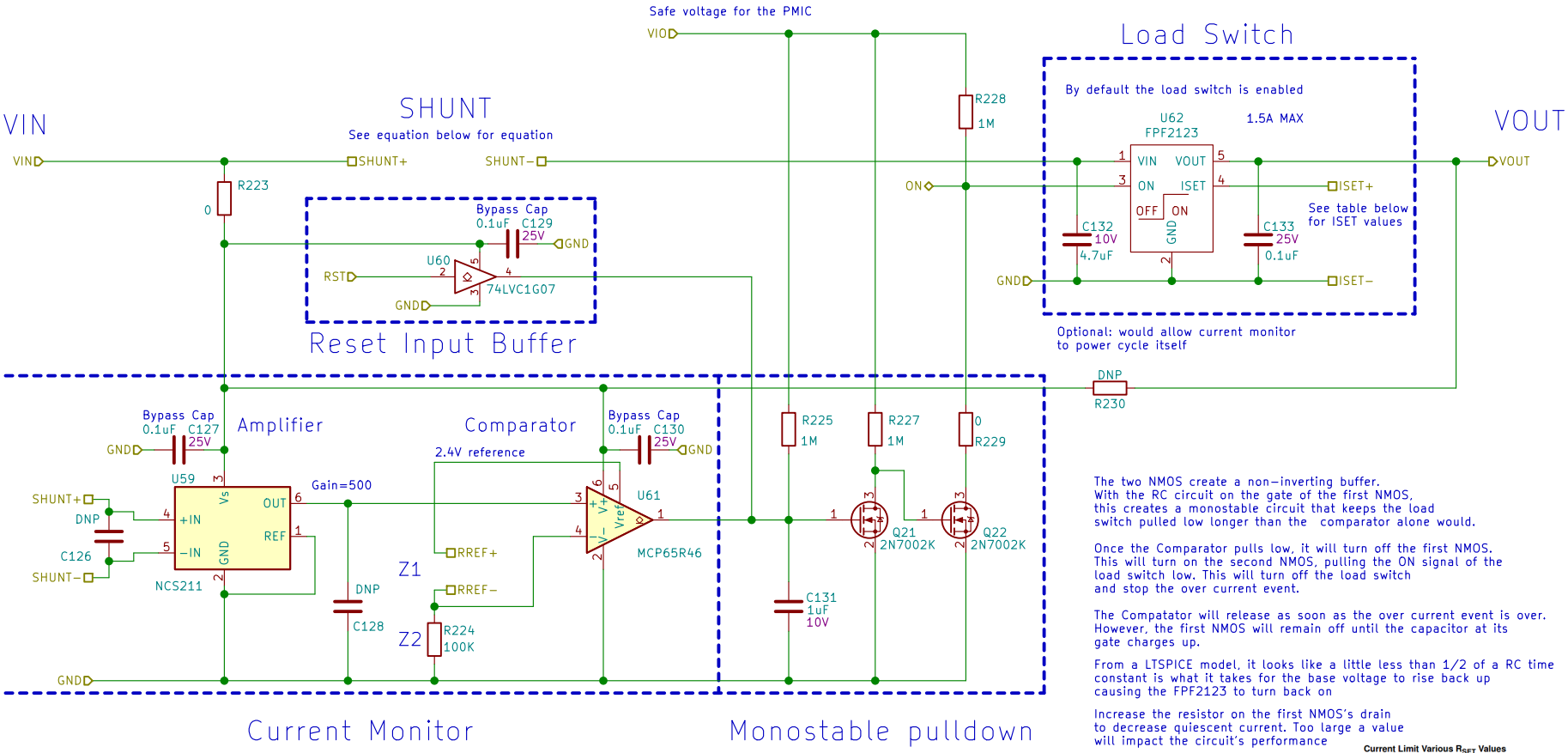
Sheet: /CURRENT_MONITORS/sheet6209BA59/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A	Date: 2020−09−06	Rev:
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1		Id: 20/39



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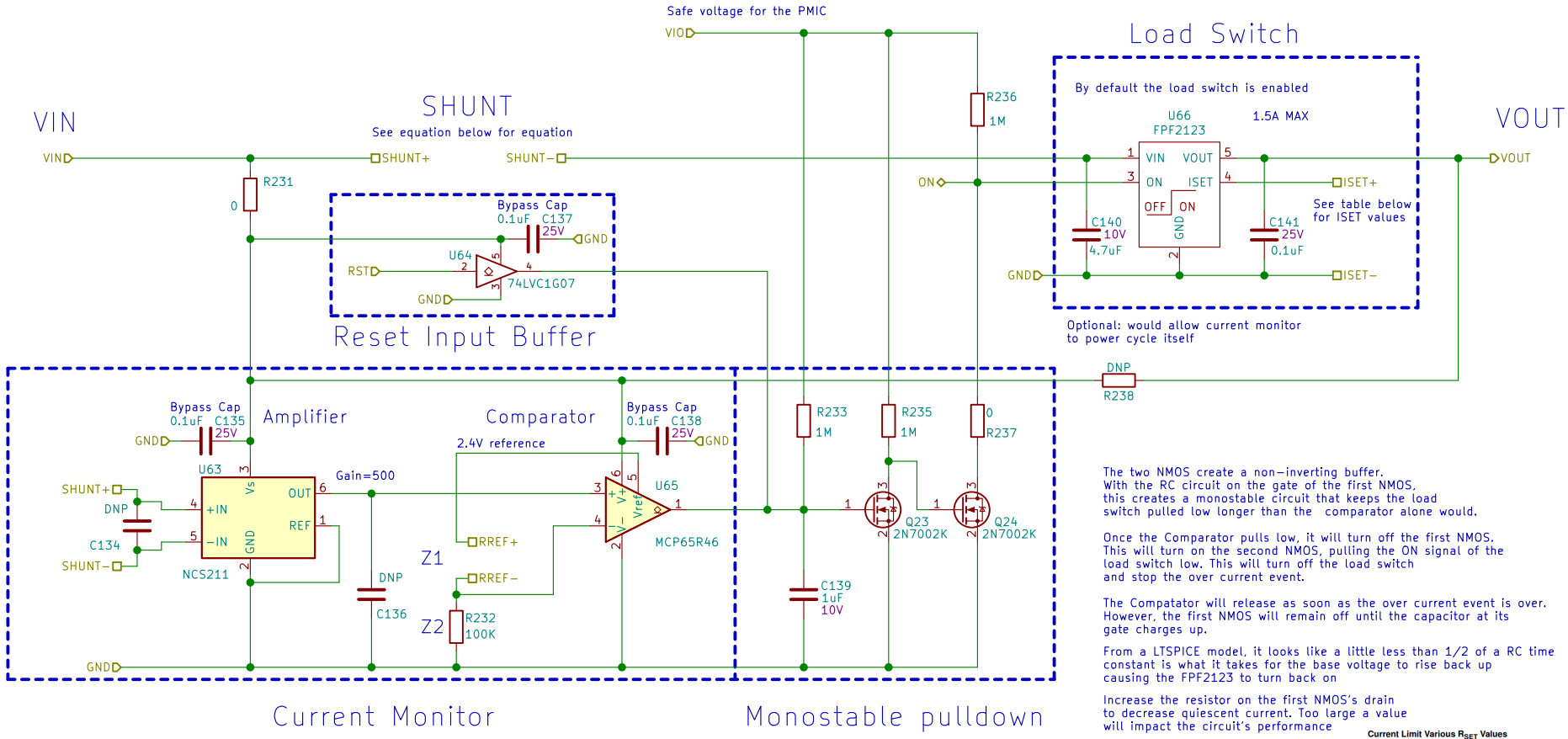
Sheet: /CURRENT_MONITORS/sheet6209BA5A/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A | Date: 2020−09−06 | **Rev:**
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1 | Id: 21/39



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340	1010	1350	1690
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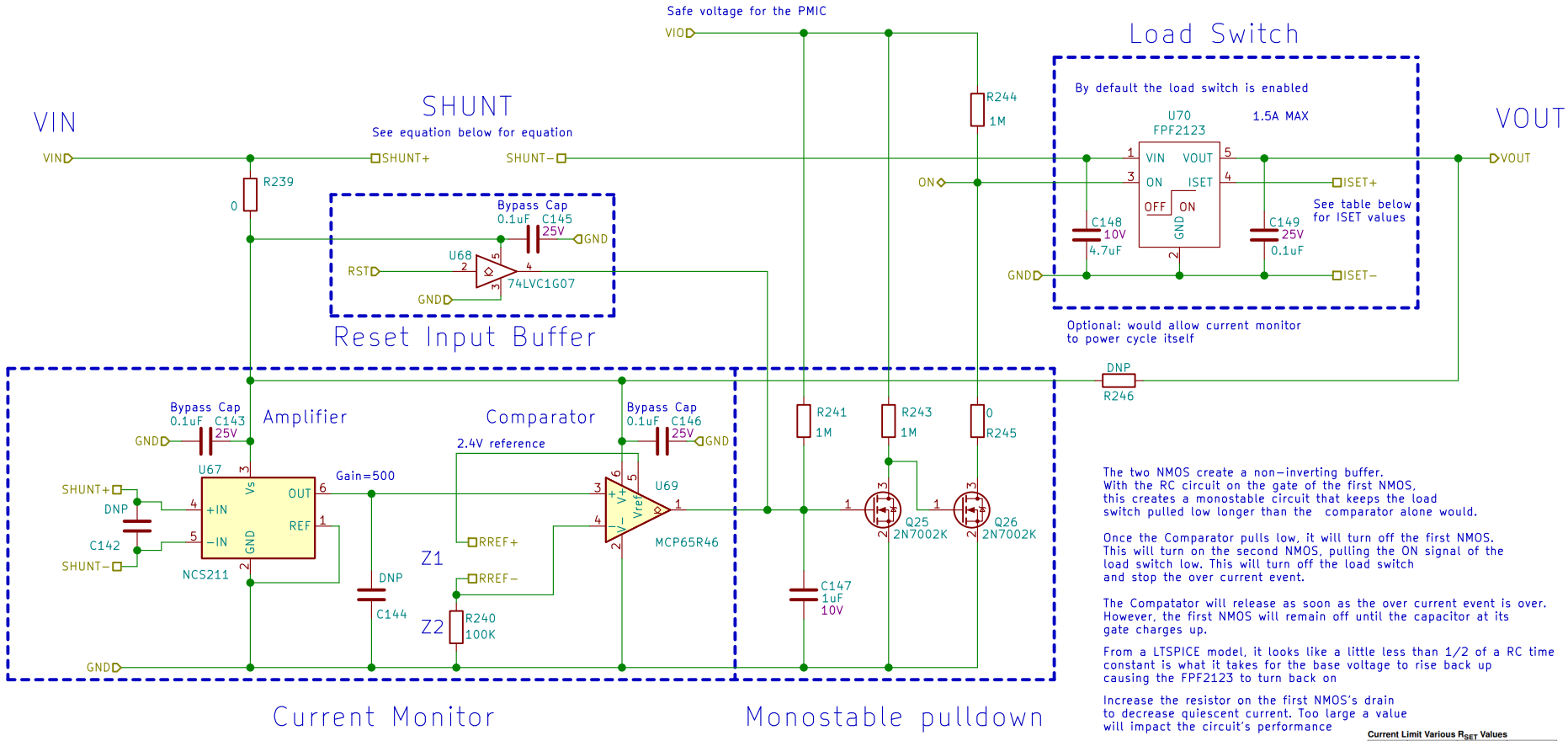
Sheet: /CURRENT_MONITORS/sheet6209BA5B/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A | Date: 2020−09−06 | **Rev:**
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1 | Id: 22/39



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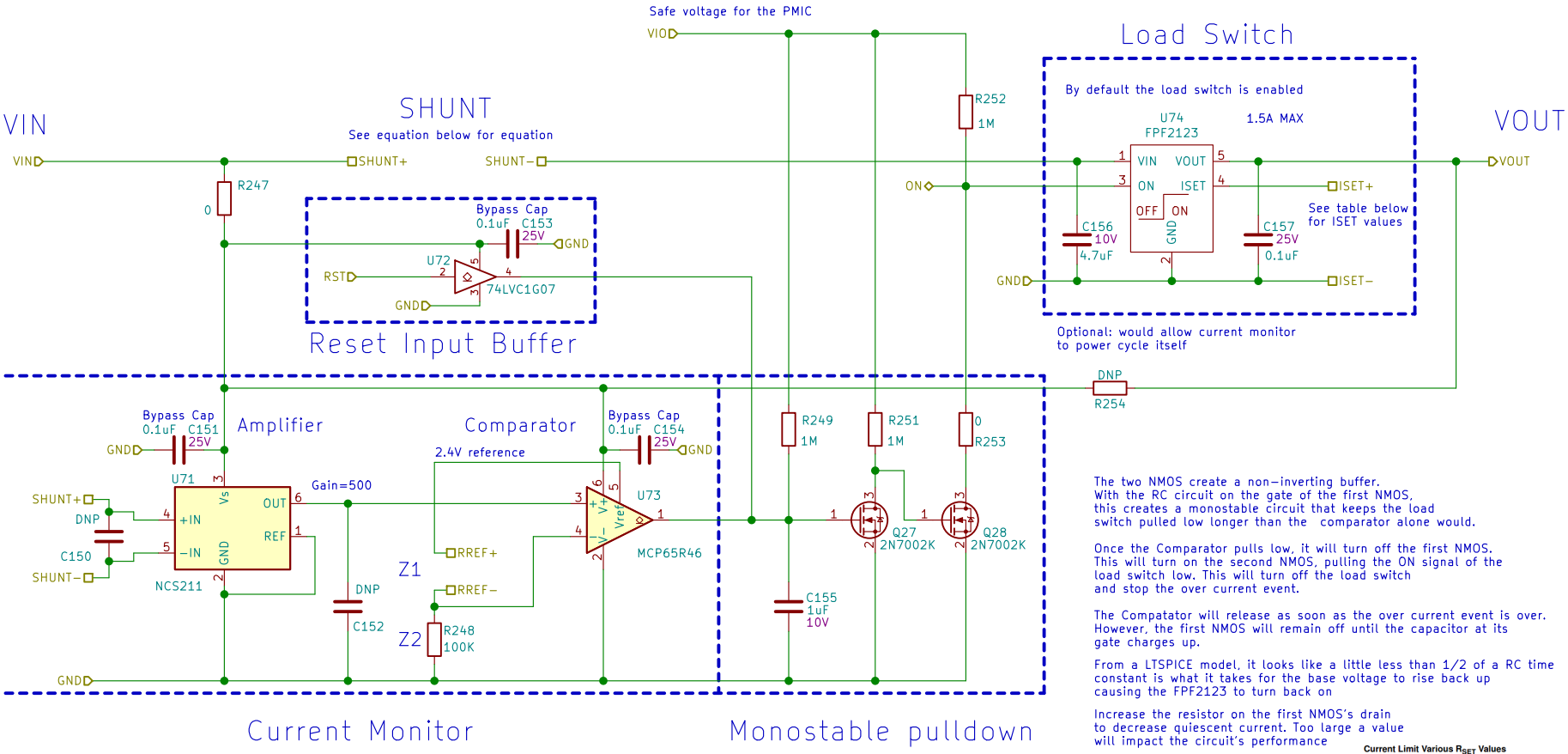
Sheet: /CURRENT_MONITORS/sheet620B1C59/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A | Date: 2020−09−06 | **Rev:**
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1 | Id: 23/39



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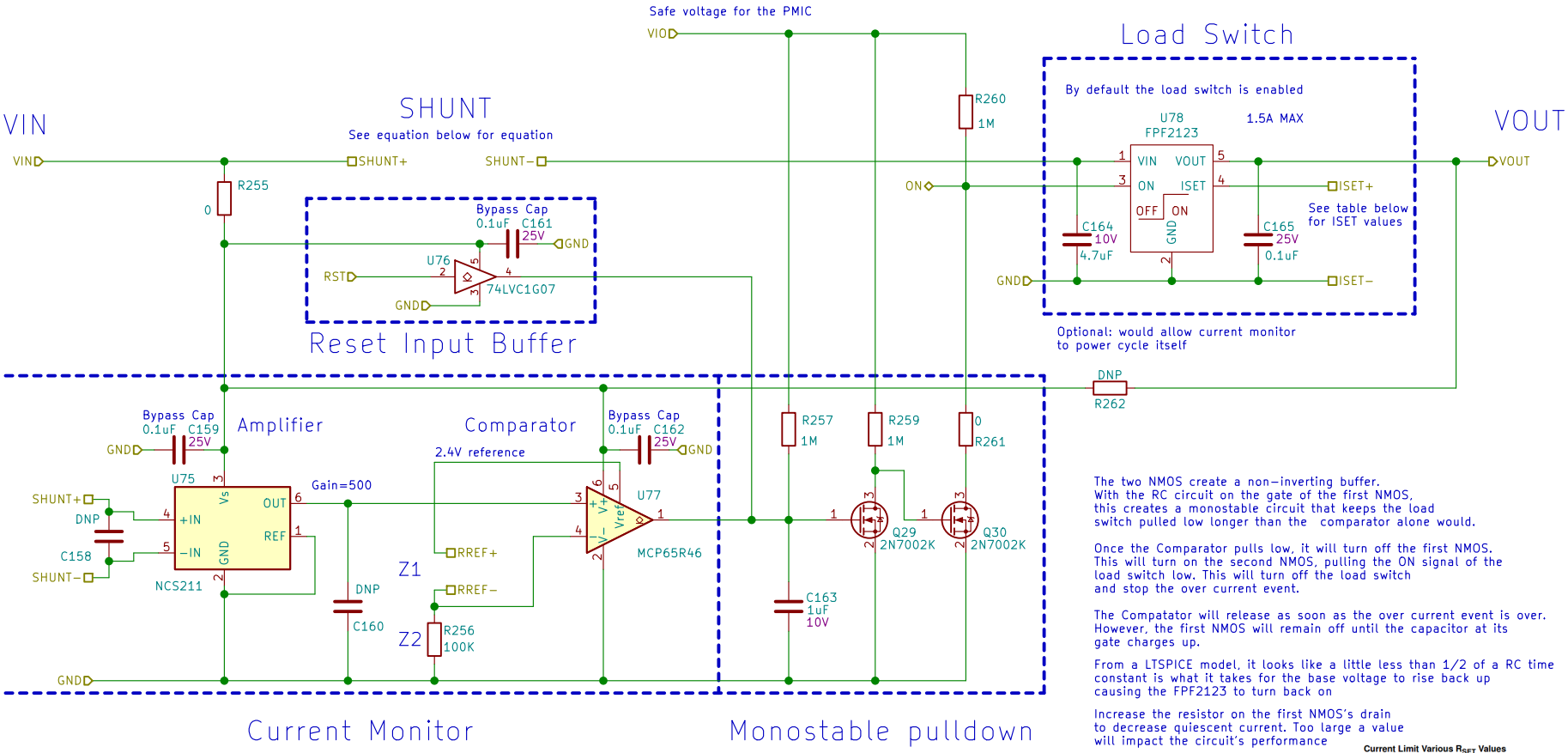
Sheet: /CURRENT_MONITORS/sheet620B1C5A/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A | Date: 2020−09−06 | **Rev:**
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1 | Id: 24/39



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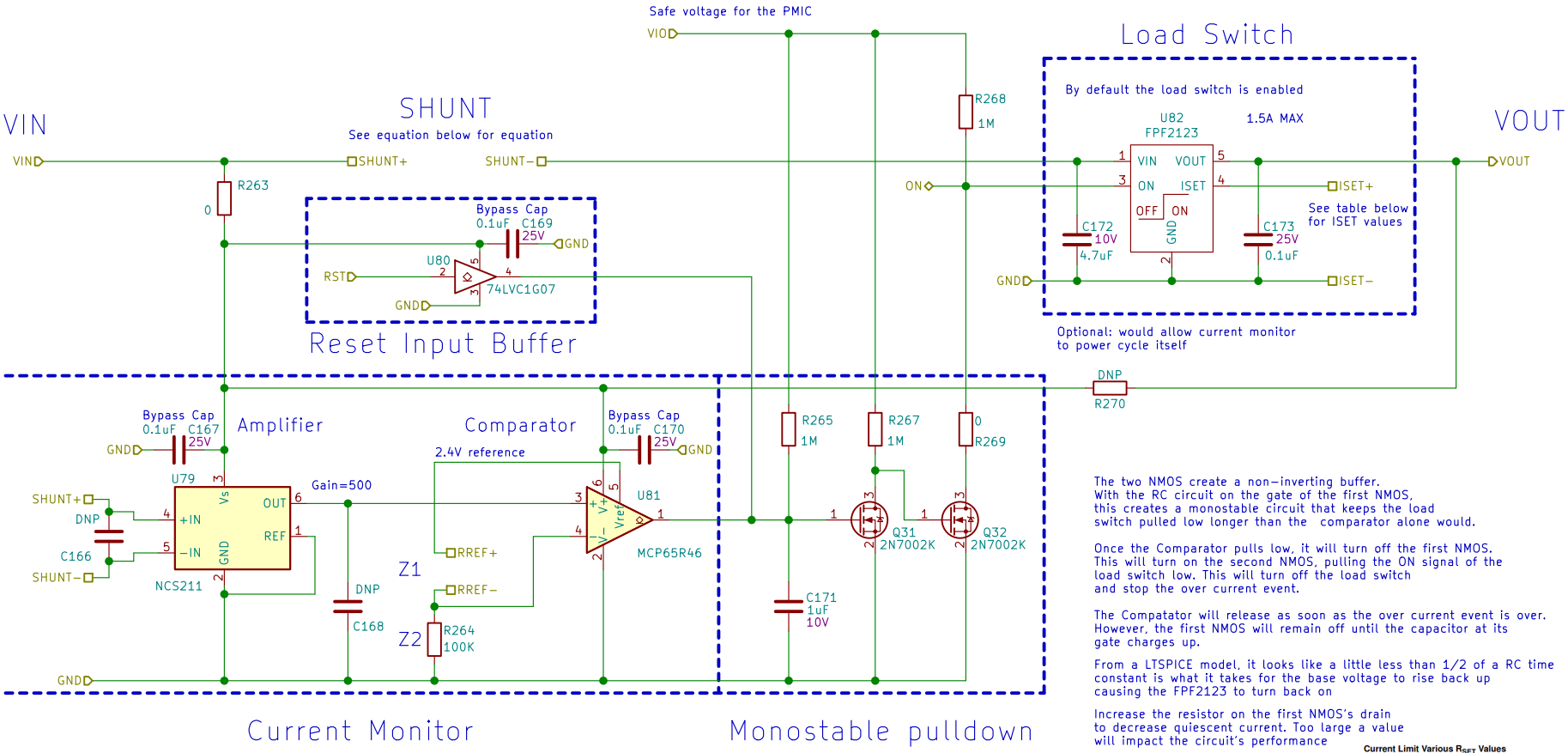
Sheet: /CURRENT_MONITORS/sheet620B1C5B/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A | Date: 2020−09−06 | **Rev:**
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1 | Id: 25/39



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Sheet: /CURRENT_MONITORS/sheet620B1C5C/
File: CURRENT_MONITOR.sch

Title: Current Monitor

Size: A | Date: 2020−09−06 | **Rev:**
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1 | Id: 26/39

VDD & VDDIO2:
Use one 0.1uF cap per power pin.
Use one 4.7uF cap per power pin group.

VDDA:
Use one 0.01uF & one 1uF

VREF:
Use one 0.1uF & one 1uF

There are only 16 EXTI GPIO inputs
P[a-z][1-15]

And I need one for the watchdog

Sheet: WATCHDOG
File: ../avionics_board/WATCHDOG.sch

Sheet: CAN_TRANSCEIVER
File: ../avionics_board/CAN_TRANSCEIVER.sch

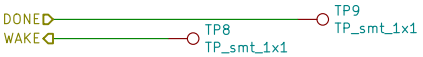
Sheet: DEBUG_INTERFACE
File: ../avionics_board/DEBUG_INTERFACE.sch

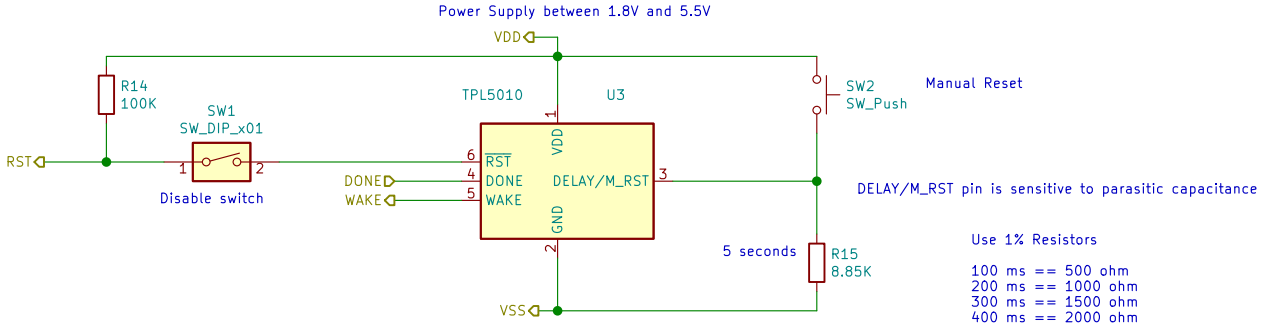
Sheet: OSC32_TCXO
File: ../avionics_board/OSC32_TCXO.sch

Sheet: MRAM
File: ../avionics_board/MRAM.sch

Sheet: /PMIC/		
File: PMIC.sch		
Title: PMIC		
Size: B	Date: 2020-09-08	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 27/39

The DONE, WAKE and RSTn signals are used to implement the watchdog function. The TPL5010−Q1 is programmed to issue a periodic WAKE pulse to a µC which is in sleep or standby mode. After receiving the WAKE pulse, the µC must issue a DONE signal to the TPL5010−Q1 at least 20 ms before the rising edge of the next WAKE pulse. If the DONE signal is not asserted, the TPL5010−Q1 asserts the RSTn signal to reset the µC. A manual reset function is realized by momentarily pulling the DELAY/M_RST pin to VDD

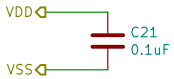




Use 1% Resistors

100 ms == 500 ohm
200 ms == 1000 ohm
300 ms == 1500 ohm
400 ms == 2000 ohm
500 ms == 2500 ohm
1 s == 5.2 Kohm
2 s == 6.79 Kohm
5 s == 8.85 Kohm
10 s == 11.20 Kohm

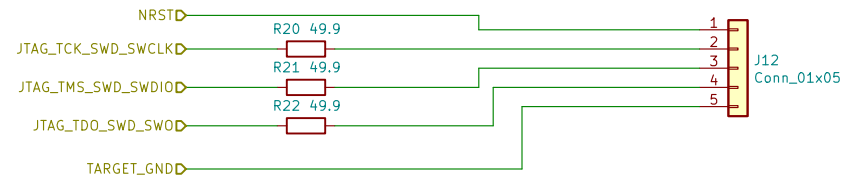
Layout Note: Decoupling



A multilayer ceramic bypass X7R capacitor of 0.1µF is recommended

Sheet: /PMIC/WATCHDOG/		
File: WATCHDOG.sch		
Title: EXTERNAL WATCHDOG		
Size: A	Date: 2020−05−02	**Rev:**
KiCad E.D.A. kicad 5.1.7−a382d34a887ubuntu16.04.1		Id: 28/39

JTAG / SWD



The TDI and TDO pins here match with the target's (the STM32's) TDI and TDO pins.

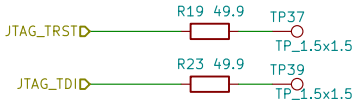
SRST = System Reset
TRST = JTAG specific reset

The series resistors are useful on high-speed traces.
https://electronics.stackexchange.com/questions/7709/why-put-a-resistor-in-series-with-signal-line

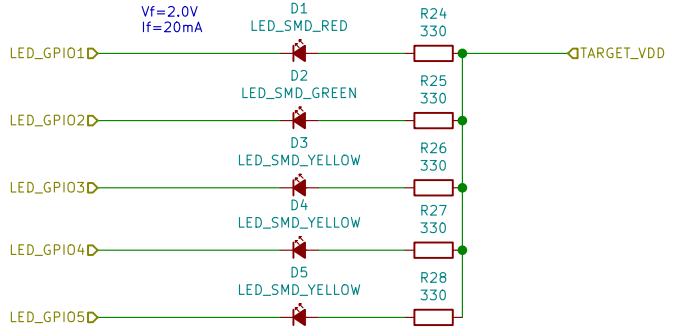
So I'm going with 50 ohm

JTAG
- TDI (Test Data In)
- TDO (Test Data Out)
- TCK (Test Clock)
- TMS (Test Mode Select)
- TRST (Test Reset) optional.

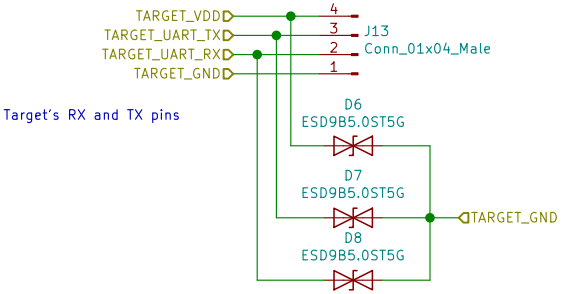
SWD
- SWCLK (Clock signal to target CPU)
- SWDIO (Bi-directional data pin)
- SWO (Serial Wire output) optional



DEBUG LED

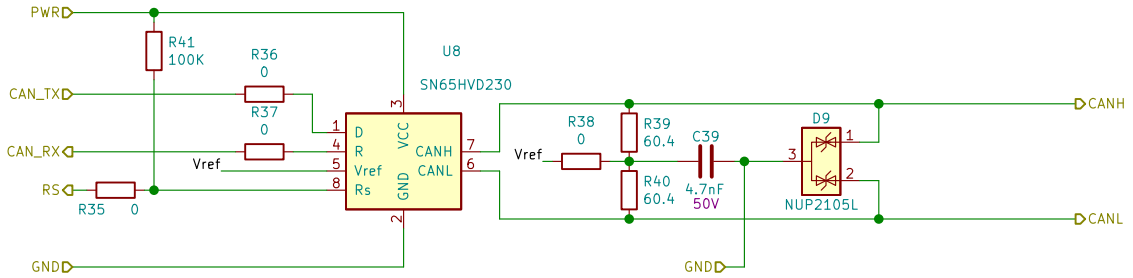


DEBUG UART



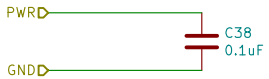
Sheet: /PMIC/DEBUG_INTERFACE/		
File: DEBUG_INTERFACE.sch		
Title: DEBUG INTERFACE		
Size: A	Date: 2020-05-02	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 29/39

D = CAN transmit data input, also called TXD, driver input
R = CAN receive data output, also called RXD, receiver output
Vref = Vcc/2 reference output pin
RS = Mode select. Strong pull down to GND = high speed mode.
Strong pull up to Vcc= low power mode. 10k to 100k to GND = slope control mode. Strong pull down to GND = High Speed

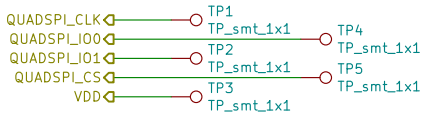


See SN65VD230 Datasheet for layout & more information about split termination

Layout Note: Decoupling



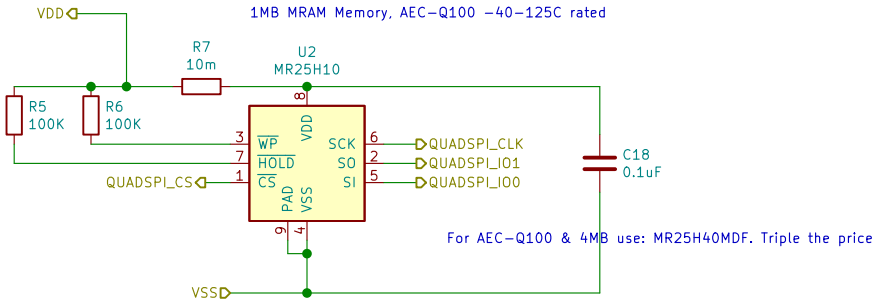
Sheet: /PMIC/CAN_TRANSCEIVER/		
File: CAN_TRANSCEIVER.sch		
Title: CAN Transceiver		
Size: A	Date: 2020-05-25	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 30/39



WP is write protect. Low active
HOLD suspends operation. Low active. Only available when CS is low
CS is chip select. Low active
SCK is SPI cock
SO is output
SI is input
VDD is from 3.0V to 3.6V
Connect pad only to VSS

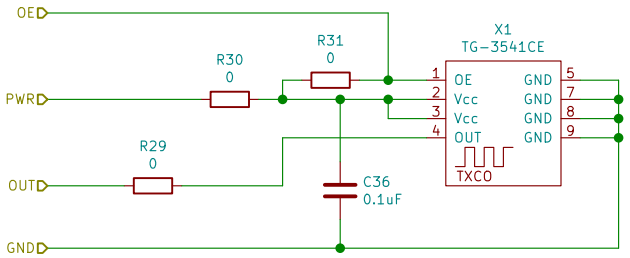
https://www.cypress.com/file/196526/download for layout guide

0.1uF decoupling cap



Sheet: /PMIC/MRAM/		
File: MRAM.sch		
Title: MRAM		
Size: A	Date: 2020-05-03	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 31/39

By default, OE is tied high so the chip is enabled immediatly



Sheet: /PMIC/OSC32_TCXO/		
File: OSC32_TCXO.sch		
Title: 32kHz TCXO		
Size: A	Date: 2020-05-25	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 32/39

NRVB120VLSFT1G

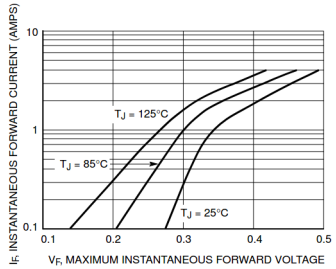


Figure 2. Maximum Forward Voltage

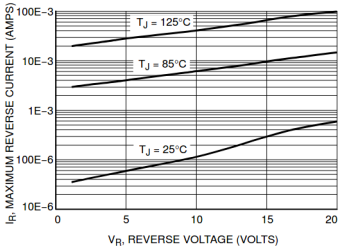
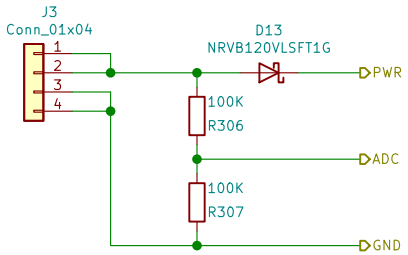


Figure 4. Maximum Reverse Current



I used to use Molex Pico Lock:
5040500491
https://www.digikey.com/en/products/detail/molex/5040500491/4357649

Sheet: /sheet61651500/ File: SOLAR_INPUT.sch		
Title: Solar Input		
Size: A	Date: 2020-08-09	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 33/39

NRVB120VLSFT1G

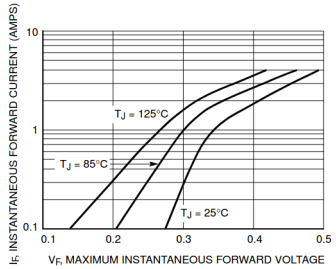


Figure 2. Maximum Forward Voltage

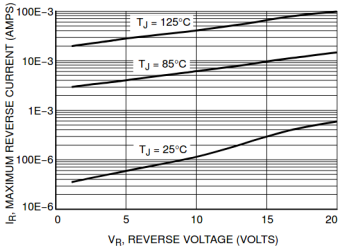
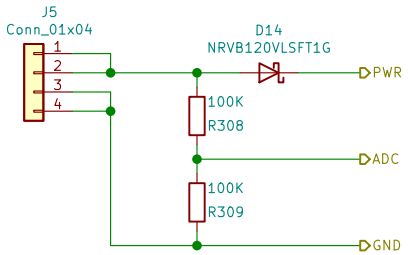


Figure 4. Maximum Reverse Current



I used to use Molex Pico Lock:
5040500491
https://www.digikey.com/en/products/detail/molex/5040500491/4357649

Sheet: /sheet6165EBDF/ File: SOLAR_INPUT.sch		
Title: Solar Input		
Size: A	Date: 2020-08-09	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 34/39

NRVB120VLSFT1G

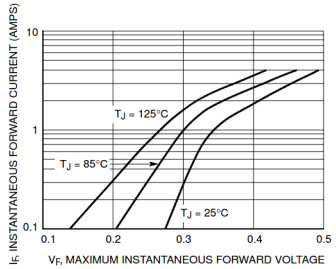


Figure 2. Maximum Forward Voltage

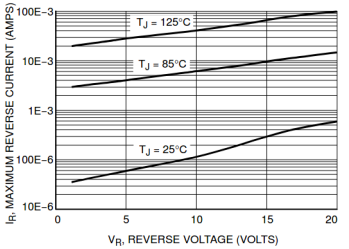
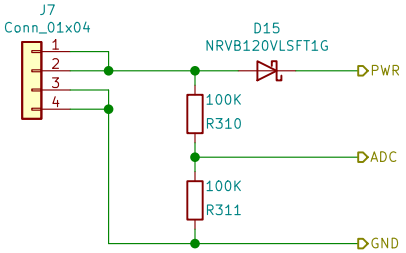


Figure 4. Maximum Reverse Current



I used to use Molex Pico Lock:
5040500491
https://www.digikey.com/en/products/detail/molex/5040500491/4357649

Sheet: /sheet6166C2B6/ File: SOLAR_INPUT.sch		
Title: Solar Input		
Size: A	Date: 2020-08-09	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 35/39

NRVB120VLSFT1G

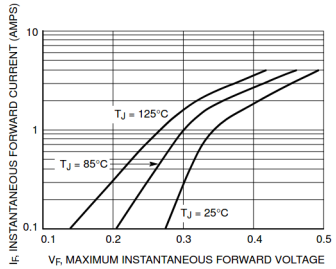


Figure 2. Maximum Forward Voltage

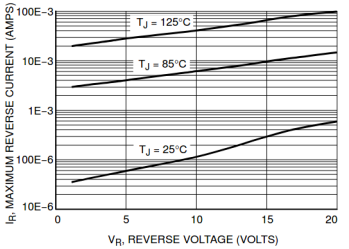
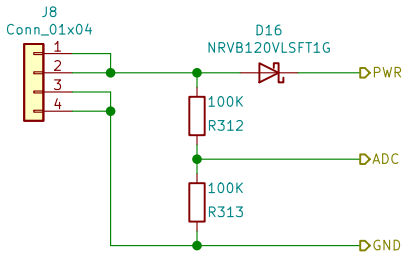


Figure 4. Maximum Reverse Current



I used to use Molex Pico Lock:
5040500491
https://www.digikey.com/en/products/detail/molex/5040500491/4357649

Sheet: /sheet61679A31/		
File: SOLAR_INPUT.sch		
Title: Solar Input		
Size: A	Date: 2020-08-09	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 36/39

NRVB120VLSFT1G

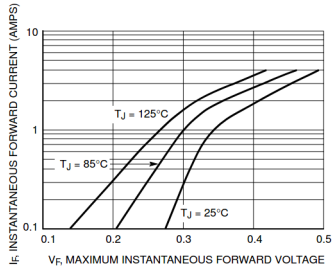


Figure 2. Maximum Forward Voltage

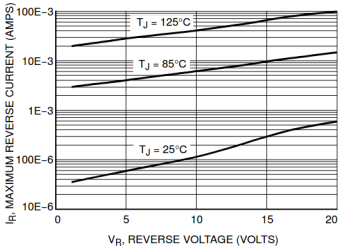
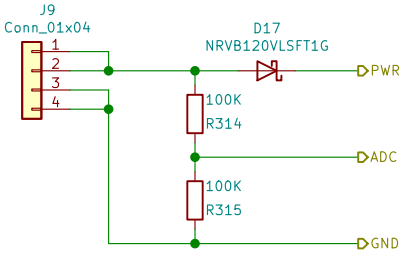


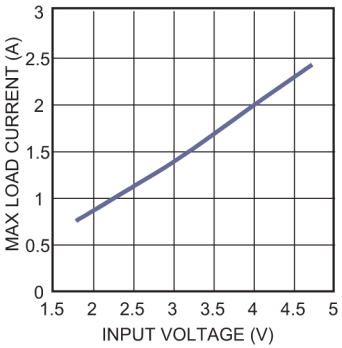
Figure 4. Maximum Reverse Current

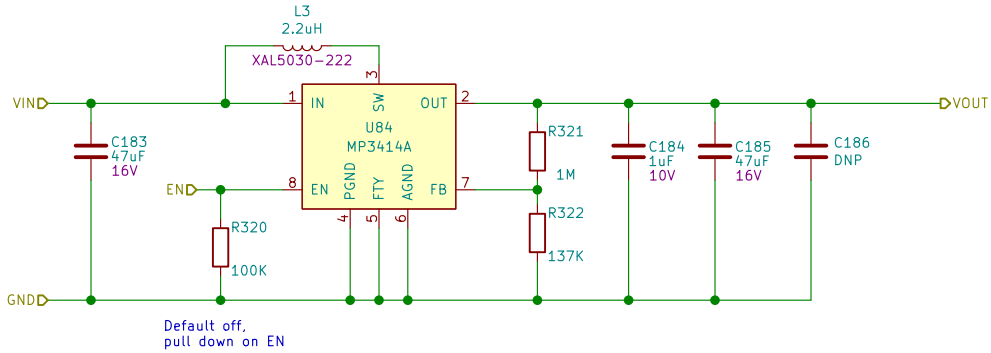


I used to use Molex Pico Lock:
5040500491
https://www.digikey.com/en/products/detail/molex/5040500491/4357649

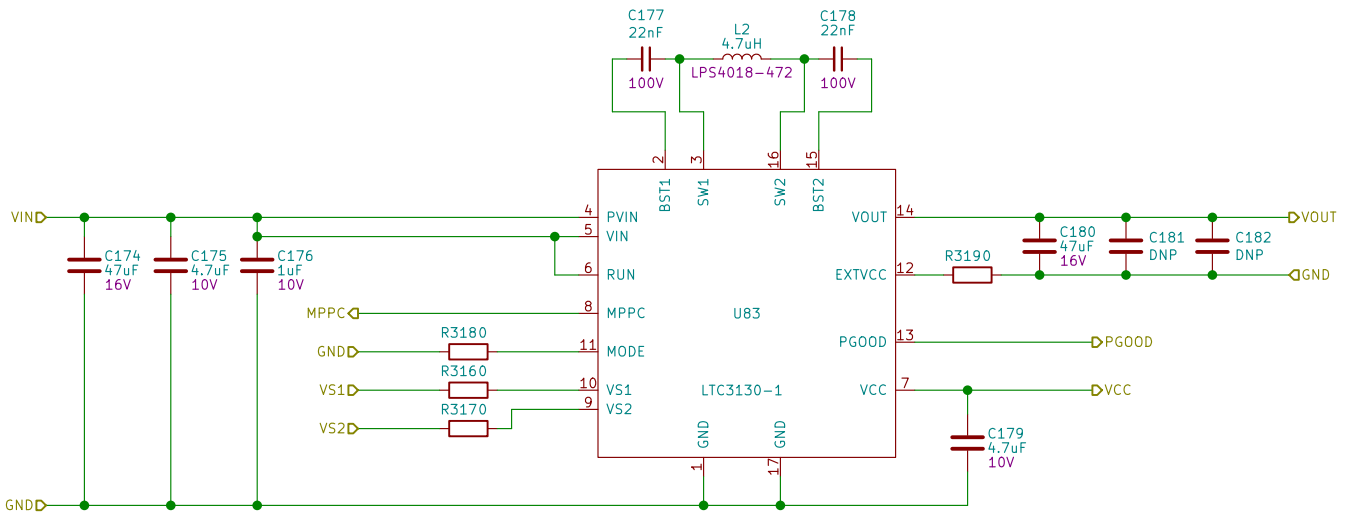
Sheet: /sheet616870B0/		
File: SOLAR_INPUT.sch		
Title: Solar Input		
Size: A	Date: 2020-08-09	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 37/39

Load Capability vs. Input Voltage (7)





Sheet: /5V BOOST/ File: MP3414A.sch		
Title: 5V Boost		
Size: A	Date: 2020-10-04	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 38/39



Maximum Power Point Control (MPPC)

The MPPC input of the LTC3130/LTC3130-1 can be used with an optional external voltage divider to dynamically adjust the commanded inductor current in order to maintain a minimum input voltage when using high resistance sources, such as photovoltaic panels, so as to maximize input power transfer and prevent V_{IN} from dropping too low under load.

Referring to Figure 4, the MPPC pin is internally connected to the noninverting input of a g_m amplifier, whose inverting input is connected to the 1.0V reference. If the voltage at MPPC, using the external voltage divider, falls below the reference voltage, the output of the amplifier pulls the internal VC node low. This reduces the commanded average inductor current so as to reduce the input current and regulate V_{IN} to the programmed minimum voltage, as given by:

$$V_{IN(MPPC)} = 1.00V \bullet \left(1 + \frac{R5}{R6}\right)$$

Note that external compensation should not be required for MPPC loop stability if the input filter capacitor, C_{IN}, is at least 22µF.

The MPPC divider resistor values can be in the MΩ range so as to minimize the input current in very low power applications. However, stray capacitance and noise pickup on the MPPC pin must also be minimized. If the MPPC function is not required, the MPPC pin should be tied to V_{CC}.

Beware of adding a noise filter capacitor to the MPPC pin, as the added filter pole may cause the MPPC control loop to be unstable.

Note that because Burst Mode operation will be inhibited if the MPPC loop takes control, the converter will be operating in fixed frequency mode, and will therefore require a minimum of about 6mA of continuous input current to operate. For operation from weaker sources, such as small indoor solar panels, refer to the Applications Information section to see how the RUN pin may be programmed to control the converter in a hysteretic manner while providing an effective MPPC function by maintaining V_{IN} at the desired voltage. This technique can be used with sources as weak as 3µA (enough to power the IC in UVLO and the external RUN divider).

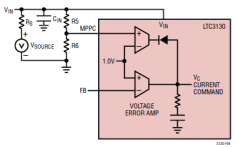


Figure 4. MPPC Amplifier with External Resistor Divider

MODE (Pin 11/Pin 11): Mode Select Pin.

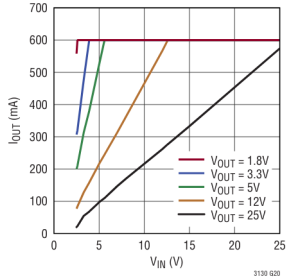
MODE = Low (ground): Enables automatic Burst Mode operation

MODE = High (tie to V_{CC}): Fixed frequency PWM operation

Table 1. V_{OUT} Program Settings for the LTC3130-1

VS2	VS1	V_{OUT}
0	0	1.8V
0	V_{CC}	3.3V
V_{CC}	0	5.0V
V_{CC}	V_{CC}	12V

Maximum Output Current vs V_{IN} and V_{OUT}



PGOOD is open drain.
Pulled low when VOUT is less than 7.5% programmed value
High-Z when VOUT is within 5% programmed value

Sheet: /sheet5FCD3934/
File: LTC3130.sch

Title: LTC3130

Size: A	Date: 2020-08-09	**Rev:**
KiCad E.D.A. kicad 5.1.7-a382d34a887ubuntu16.04.1		Id: 39/39