1. 单选
2. In register indirect addressing mode , the operand is in the \_\_\_\_\_\_
3. general-purpose B. memory location C.instruction D.
4. the capacity of a kind of SRAM chip is 8k\*16, so , the address lines and data lines of this chip are \_\_\_\_\_\_ respectively.

A.8,16 B.13,16 C.13,4 D,8,4

1. By \_\_\_\_\_\_ technique , a main memory black can be placed into only one possible cache block position.
2. Direct-mapping B. associative-mapping

C. full associative-mapping D.set associative-mapping

1. about benefit of virtual memory is not true?
2. Provide large address space B.relieve progremmers from barden of overlags

C.reslove internal fragmentation D.simplify relocation

1. A hard disk with 5 double-sided platters has 2048 tracks/platter , how many movable heads does it have?
2. 5 B.10 C.2048\*5 D.2048\*10
3. The range of an 8-bit signed 2’s complement integer is
4. -256~+256 B. -256~+255 C. -128~+128 D. -128~+127
5. 1001010 and 01110111 , to be multiplied using a multiplier that uses Booth’s ~~ , How many additions will be performend by the Booth’s ~~multiplier .
6. 6 B. 4 C. 2 D. 8
7. The cause of overflow in signed addition .
8. If there is a carry out of the least significant bit
9. Most results in a positive result .
10. Adding two negative numbers
11. If the magnitude of the result is smaller than the magnitude of the smaller added.
12. The range and accuracy of floating-point numbers depend on ---- respectively.
13. The size of exponent and the representation of mantissa.
14. The size of mantissa and the representation of exponent.
15. The size of exponent and the representation of mantissa.
16. The size of mantissa and the representation of exponent
17. Branch instruction is at location 2000，and the offset of the instruction is 46，then the branch target address is -----

2046 2048 2050 2002

1. Use -----to differentiate memory location and I/O devices

Different address address buses instruction control signals

1. Interput system is implement by ---

H S H S No

1. The device that is allowed to initiate data transfers on the bus at any given time is called ----

Bus transceiver/ slave /receiver/master

1. Use to prevent branch hazard

Bypassing / forwarding / duplication of resources/ Freeze or Flnsh

二.

1. An interrupt is serviced by a prediefined interrupt service routine(ISR)

The user desires that the device is serviced by a user defined ISR instead of the predefined ISR.

What steps should the user take?

2. Under what circumstances do page fault occur?Describe the actions take by the operating system when a page fault occurs.

3.Using 32-bit IEEEE 754 single precision floating point format ,show the representation of -11/16

4.point out which instructions are dependent?Can we eliminate the data dependencies using bypassing(Note:LD means Load in~~~

ST Store in~~~~)

LD R7，（R8）

SUB R10,R11,R12

MVL R13,R7,R11

ST (R9),R13

ADD R13,R2,R1

LD R5,(R6)

SUB R3,R4,R5

三.

1. two types of static memory chips: 128k \*8 bit(total 8 chips) 512k \* 8 bit (total 8 chips)

Use these memory chips to implement a 512k \*32 bit memory.

Draw the figure of the memory organization.

2.A given processor has 32 registers , uses 16-bit immediate , and has 142 instructions in its instruction set . In a given program , 20 percent of the instruction take one input register and have one output register ; 30 percent have two input registers and one output register; 25 percent , have one input register , one output . and take an immediate input as well , the remaining 25 percent have one immediate input and one output register .

For each of the four types of instructions , how many bits are required;

( the instructions be a multiple of 8 bits in length )

3. The non-restoring division algorithm ， perform the operations A/B on the unsigned numbers A=1000 and B=11. Write the computation processs in a computer machine .

4. part of the microinstruction sequence corresponding to one of the machine instructions of a microinstruction computer .

Microinstruction B is followed by C , D , F or I .

Depending on bits IR6 , IR5 , and IR4 of the machine instruction register.

Give implementation . Microinstruction sequencing is accomplished by means of a micropromram counter . Braning is achieved by microinstructions of the form : Branch to X ,OR .

Where X is a base bit-ORing of bits IR4, IR5 , IR6 with the apprioriate bits with X.

5.A byte-address computer has a small data cache capable of holding eight 32-bit words .

Each cache block consists of two 32-bit words . When a given program is executed , the processor read . data ~~~~hex add 200 , 204 , 208 , 20C , 2F4 , 2F0 , 200 , 204 , 218 , 21C , 24C , 2F4 .

This pattern is repeated four times .

Assume the cache is initially empty .

Show the contents of the cache at the end of each pass through the loop for a two-way set associative cache that uses the LRU replacement algorithem , and compute the hit rate .