计算机组成与体系结构期末考试样题答案

一、单项选择题

1. The part of machine instruction, which tells the central processor what was to be done is .

A. operation code B. address C. operand D. none of the above

1. Which of the following is not the basic I/O method in a computer system? .

A. DMA approach B. interrupt-driven

C. event-driven D. program-controlled I/O

3. In carry-lookahead adder, the expression is called the propagate function Pi for stage i.

A. xi+yi B. xi⊕yi C. xiyi D. xi⊕yi⊕ci

4. In hardwired control unit, the required control signals are determined by the following information except .

A. contents of the control step counter B. contents of the instruction register

C. contents of the condition code flags D. contents of the program counter

5. When I/O devices and the memory share the same address space, the arrangement is called .

A. memory-mapped I/O B. mixed I/O C. separated I/O D. relative I/O

6. Suppose that a 2M x 16 main memory is built using 256K x 8 RAM chips and memory is word-addressable. How many RAM chips are necessary? .

A. 4 B. 8 C. 16 D. 32

二、简答题

1. What is the difference between a subroutine and an interrupt-service routine?

Solution:

A subroutine is called by a program instruction to perform a function needed by the calling program.

An interrupt-service routine is initiated by an event such as an input operation or a hardware error. The function it performs may not be at all related to the program being executed at the time of interruption. Hence, it must not affect any of the data or status information relating to that program.

1. What are the advantage(s) and disadvantage(s) of hardwired control unit?

Solution:

The main advantage of hardwired control is fast operation. The disadvantages include: higher cost, inflexibility when changes or additions are to be made, and longer time required to design and implement such units. Microprogrammed control is characterized by low cost and high flexibility. Lower speed of operation becomes a problem in high-performance computers.

三、综合题

1. Consider the memory system with the following specifications:

* Byte-addressable
* Virtual address space: 4G bytes
* Main memory size: 16M bytes
* Cache size: 256K bytes
* Page size: 64K bytes
* Block size: 128bytes
* Mapping Strategies: Main Memory to Cache: 4-way set associative; Hard Disk to Main Memory: fully associative

Virtual address is first translated to physical address. Then, it accesses the cache memory using the physical address.

1. How many sets are there in the cache memory?
2. How long is the tag field of the cache?
3. Given a virtual address 0B45DA12 (hexadecimal), its corresponding virtual page is stored in physical page 3E (hexadecimal).
   * + 1. What is its physical address under such mapping?
       2. Which set can this address be possibly found in the cache?
       3. Which byte does this address point to out of the 128 bytes in a block?

Solution:

(1)(512k/32)/8=2K

There are 2K sets in the cache memory.

(2)Because the main memory is byte-addressable and the main memory size: 16M bytes, so the main memory address is 24-bit long. From (1) there are 2K sets in the cache memory, so the set field of the main memory address is 11-bit long. And because the block size: 32 bytes, so the byte field of the main memory address is 5-bit long. Finally, the tag field of the cache is 24－11－5 =8-bit long.

(3)①There are 4G/64K=216 virtual pages ,so the virtual page number is 16-bit long. Because the virtual address is 32-bit long, so the offset field of it is 32-16=16-bit long.

The virtual address 0547AF33 can be divided into two parts, the highest 16-bit virtual page number and the lowest 16-bit offset. So the offset field of this virtual address is AF33. Concatenate it with the physical page number. So the physical address under such mapping is 3BAF33

②3BAF33=(0011 1011 1010 1111 001 10011)2

So this address can be found in 57916 set in the cache.

③3BAF33=(001110111010111100110011)2

The byte number is 19.

1. Give the sequence of steps needed to fetch and execute the instruction

SUB R1, R2, R3

on a 5-stage RISC processor. Assume 32-bit operands.

Solution:

1. Memory address←[PC], Read memory, IR←Memory data, PC←[PC]+4
2. Decode instruction, RA←[R2], RB←[R3]
3. RZ←[RA]-[RB]
4. RY←[RZ]
5. R1←[RY]
6. Consider the following instructions at the given addresses in the memory:

***1000 Add R3, R2, #20***

***1004 Subtract R5, R4, #3***

***1008 And R6, R3, #0x3A***

***1012 Add R7, R2, R4***

Assume that the pipeline provides forwarding paths to the ALU from registers RY and RZ and that the processor uses forwarding of operands.

1. Draw a diagram that represents the flow of the instructions through the pipeline.
2. Describe the contents of registers IR, PC, RA RB, RY, and RZ in the pipeline during cycles 2 to 8.

Solution:

这是作业6.2题，请看作业答案。