UNIVERSITY OF TEXAS AT AUSTIN, COCKRELL SCHOOL OF ENGINEERING

Senior Design Design Review
Team 25 - Security in Autonomous Vehicles

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1 Paper Overview

An overview of our proposed design and deliverables for senior design will be covered below. Our overarching design will be broken down into three core subsections: (1) the CAN protocol and subsequent network hardening, (2) DSRC communication with high speed encryption, and (3) the robotics testbed.

1.1 CAN Design

A FPGA (currently the Xilinx Zedboard) will act as a vital core to our system. DSRC transmissions will go through the FPGA for encryption and data buffering before being sent to the bus. Towards the end of hardening out CAN bus, protocol changes will be implemented to CAN on the FPGA through message validation using embedded firmware keys. Vulnerable nodes will be created within the FPGA fabric to act as a testing point for standard CAN versus our hardened system.

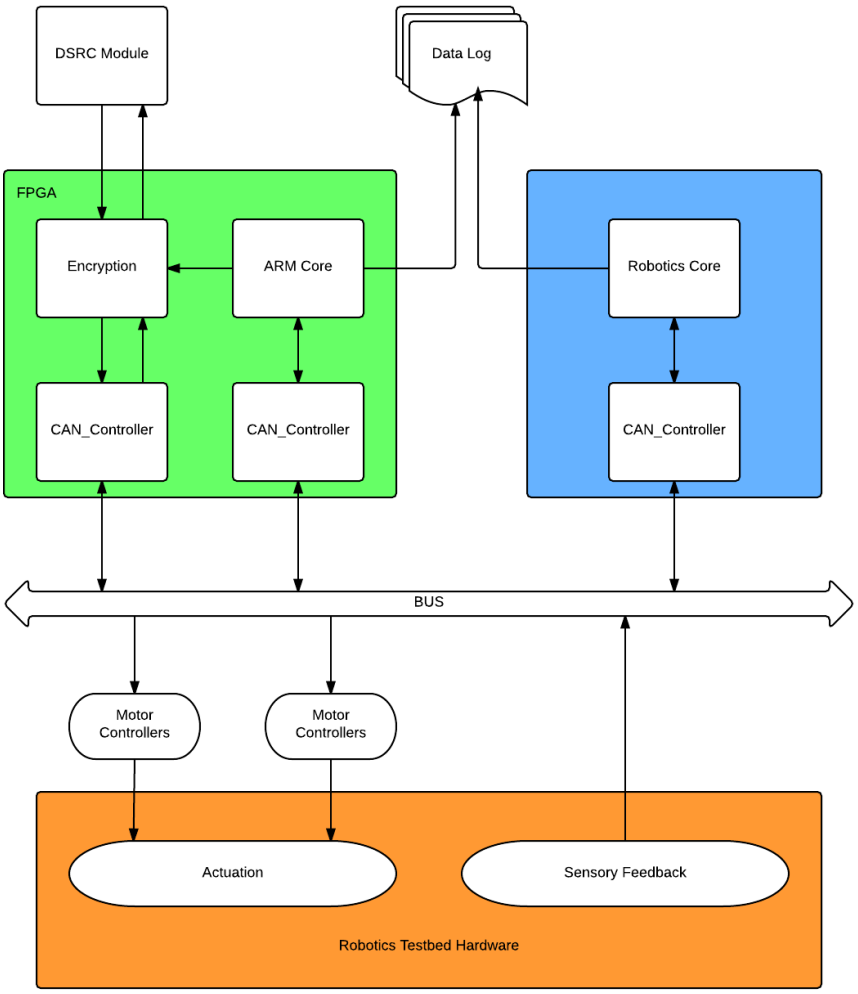
1.2 High Speed Encryption

Our system will require high speed data encryption and sender validation through message signatures.

1.3 Robotics Testbed

1.3.1 Control Algorithm

We can use an Extended Kalman Filter (EKF) to collect information from our system being supplied by the DSRC and external feedback sensors and generate a reliability matrix.


DSRC Module
Data Log
FPGA
Encryption
ARM Core
Robotics Core
CAN_Controller
CAN_Controller
CAN_Controller
BUS
Motor Controllers
Motor Controllers
Actuation
Sensory Feedback
Robotics Testbed Hardware