UNIVERSITY OF TEXAS AT AUSTIN, COCKRELL SCHOOL OF ENGINEERING

Senior Design Design Review
Team 25 - Security in Autonomous Vehicles

Kevin Gilbert, Gilberto Rodriguez, Christopher Haster, Hao Chen, Young Chou, Joshua Bryant

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1 Design Overview

An overview of our proposed design and deliverables for senior design will be covered below. Our overarching design will be broken down into three core subsections: (1) the CAN protocol and subsequent network hardening, (2) DSRC communication with high speed encryption, and (3) the robotics testbed.

1.1 CAN Design

A FPGA (currently the Xilinx Zedboard) will act as a vital core to our system. DSRC transmissions will go through the FPGA for encryption and data buffering before being sent to the bus. Towards the end of hardening out CAN bus, protocol changes will be implemented to CAN on the FPGA through message validation using embedded firmware keys. Vulnerable nodes will be created within the FPGA fabric to act as a testing point for standard CAN versus our hardened system. Figure 1 in Appendix A shows the layout of our bus system within the robotics testbed.

1.2 High Speed Encryption

Our system will require high speed data encryption and sender validation through message signatures.

1.3 Robotics Testbed

The robotics core in Figure 1 refers to the central processing unit that will control our robotics system. The two primary devices being considered for this core will be either an LM4F Launchpad for simple control algorithms, or a Beaglebone Black embedded device that would allow us to utilize a ROS framework and more advanced data filtering.

1.3.1 Control Algorithm

We can use an Extended Kalman Filter (EKF) to collect information from our system being supplied by the DSRC and external feedback sensors and generate a reliability matrix. This allows us to

2 Bandwidth Bottlenecks

The primary bottleneck concern lies with the large disparity between our DSRC channel's communication speed versus the baudrate of modern CAN buses in addition to the small data segments in each transmission frame. CAN was not designed for large data transmissions and has a clock rate several orders of magnitude smaller than that of our DSRC. How far we will need to deviate from the standard protocol will need to be determined.

Development of a simulator, as well as collected data from our hardware implementation, will provide us with a solid basis to determine if current CAN buses are too restrictive and need to

be further developed. We intend to stick as closely as possible to current implementations to allow for devices to be minimally adjusted to work with our system.

APPENDIX A

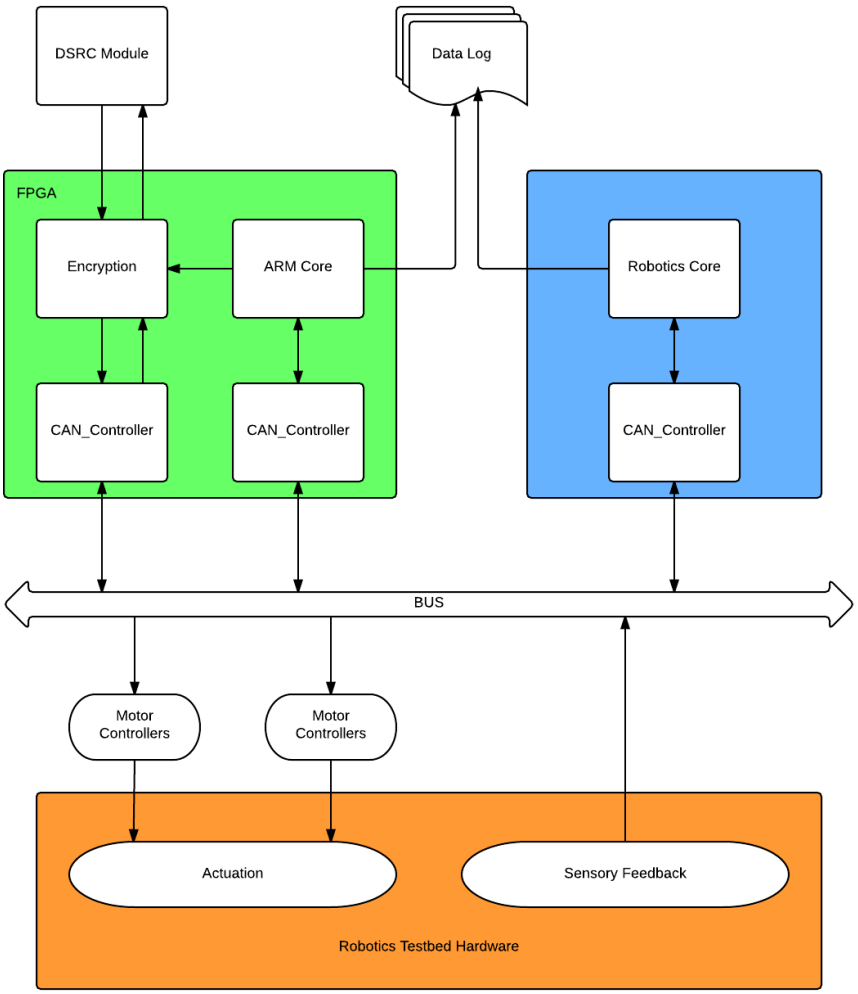

Figure 1: System bus layout