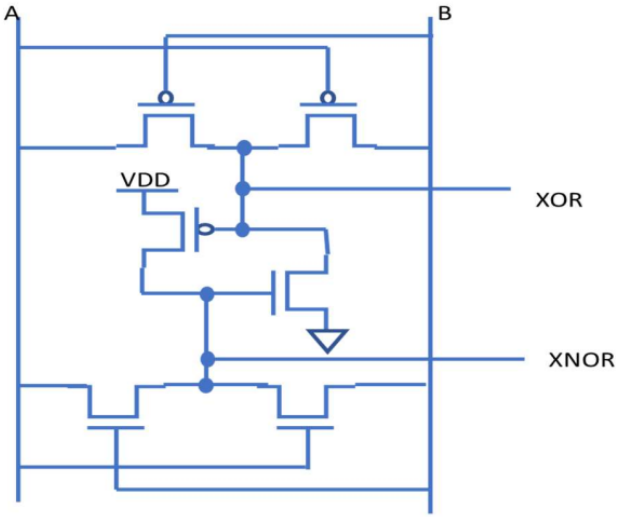
A NEW 6-TRANSISTOR XOR-XNOR CIRCUIT BASED ON THE PASS TRANSISTOR LOGIC

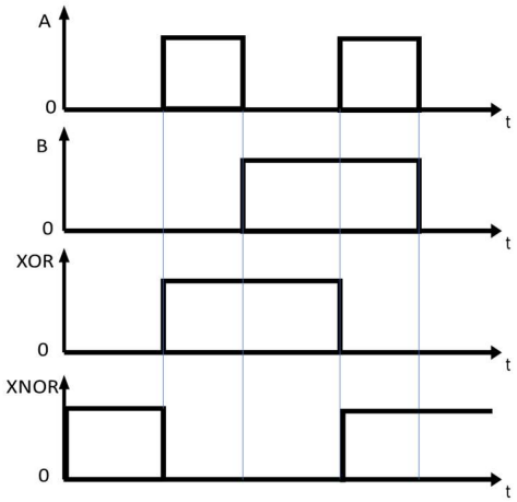
Abstract

XOR-XNOR circuits are the basic building block of many arithmetic and encryption circuits. This paper proposes a low-power 5 transistor XOR-XNOR circuit. This paper also evaluates and compares the performance of various XOR-XNOR circuits. The performance of these circuits are based on 90nm process model at all range of supply voltage starting from 0.6V to 1.2V is evaluated more power efficient and faster than the best available XOR–XNOR circuit in literature. The proposed circuit utilizes the least number of transistors and no complementary input signals is used.

Reference Circuit Diagram



Reference Waveform



Truth Table

Input A	Input B	Output XOR	Output XNOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

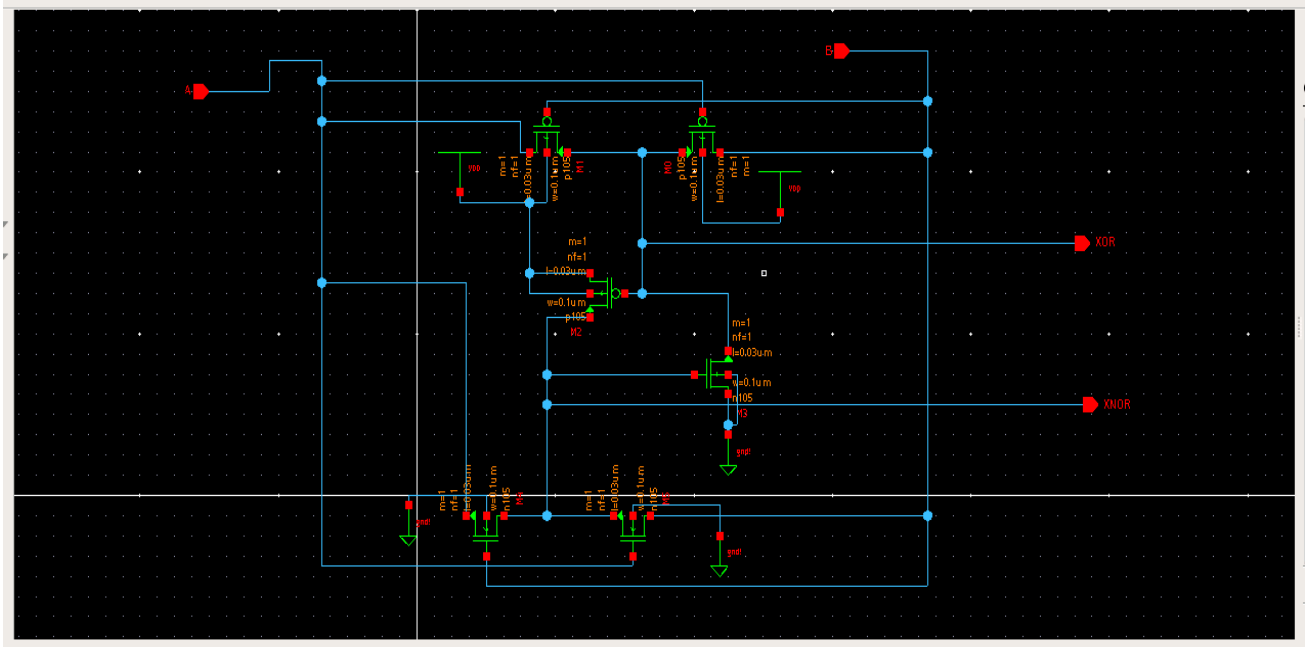
Circuit Details

As shown in the figure we have two cross coupled circuits of PMOS logic and NMOS logic. On the PMOS logic we are getting the output as XOR while in the NMOS block we get the output as XNOR. The transistors M4 and M3 behave as a pass transistor and pass the output of M1, M2 and M5, M6 respectively. The advantage of the above circuit is that it uses only 6 transistors and gives both outputs of XOR and XNOR while the general circuit uses 8 transistors with only one output either XOR or XNOR. This way it consumes less space and less power and is efficient in many ways.

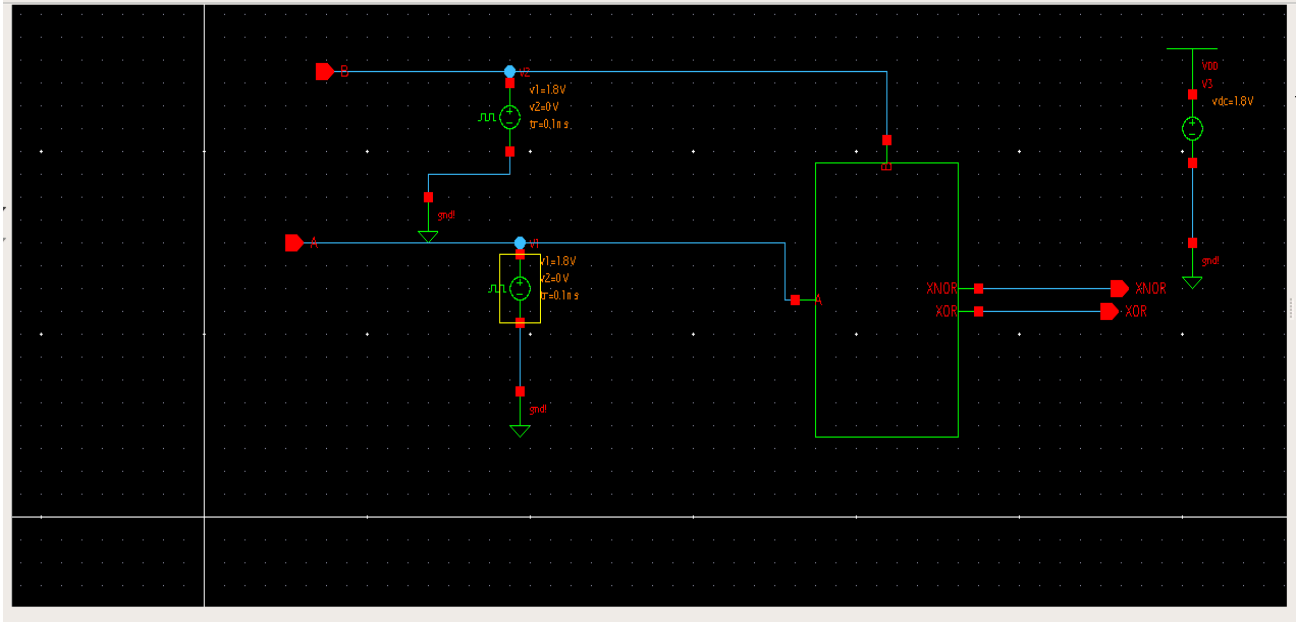
Therefore, careful design and analysis is required for XOR-XNOR circuits to obtained –full output voltage swing, lesser power consumption and delay in the critical path. Additionally, the design should have a lesser number of transistors to implement XOR-XNOR circuits. We propose and compare new XOR-XNOR circuit designs which produce the XOR-XNOR outputs simultaneously with full output voltage swing. The NMOS and PMOS transistors are added to the basic circuits to alleviate the threshold voltage loss problem commonly encountered in pass transistor logic design.

In the past two decades, a number of circuit techniques have been reported with a view to improve the circuit performance of XOR XNOR gates [3]-[4]. A wide variety of XOR-XNOR implementations are available to serve different speed and density requirements. Transistor count and full output voltage swing are, of course, a primary concern that largely affects complexity of many digital functional units drag them to the first column. Make the graphic wider to push out any text that may try to fill in next to the graphic.

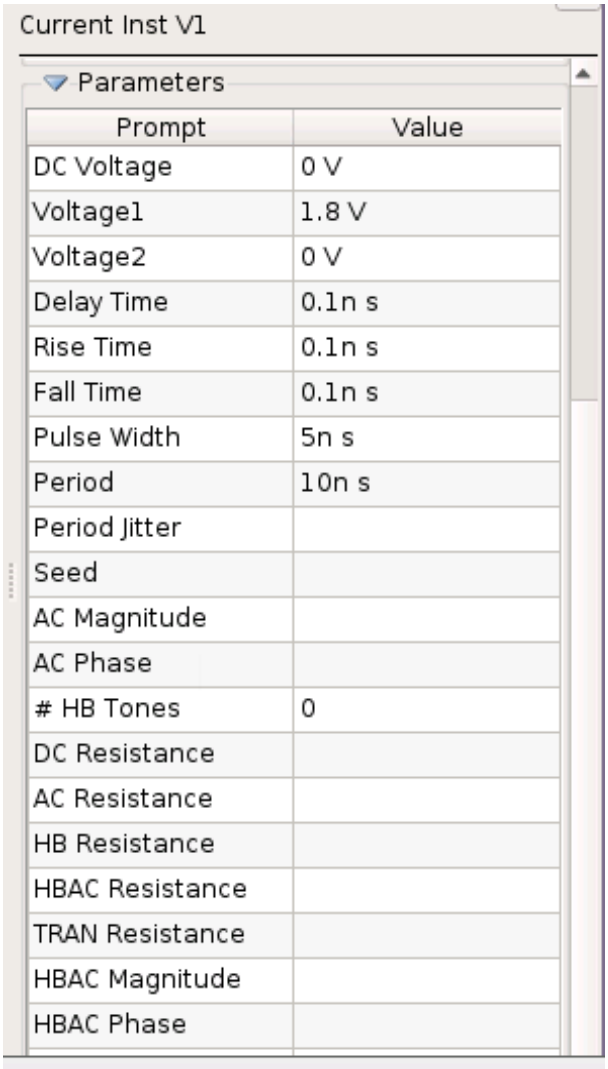
Circuit Diagram



Symbol Diagram



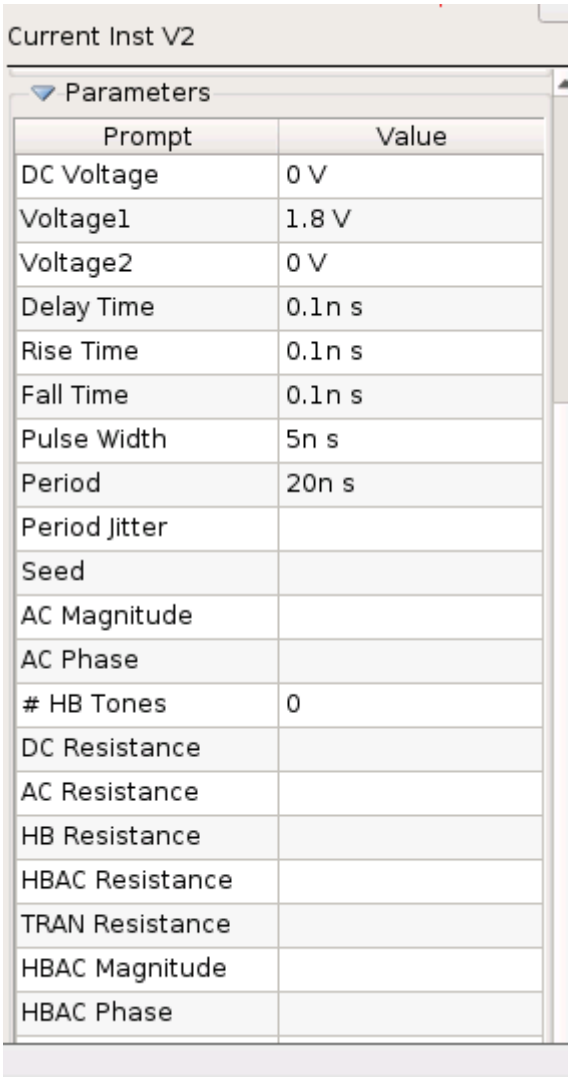
Parameters set for voltage Source for input A


Current Inst V1

Parameters

Prompt	Value
DC Voltage	0 V
Voltage1	1.8 V
Voltage2	0 V
Delay Time	0.1n s
Rise Time	0.1n s
Fall Time	0.1n s
Pulse Width	5n s
Period	10n s
Period Jitter	
Seed	
AC Magnitude	
AC Phase	
# HB Tones	0
DC Resistance	
AC Resistance	
HB Resistance	
HBAC Resistance	
TRAN Resistance	
HBAC Magnitude	
HBAC Phase	

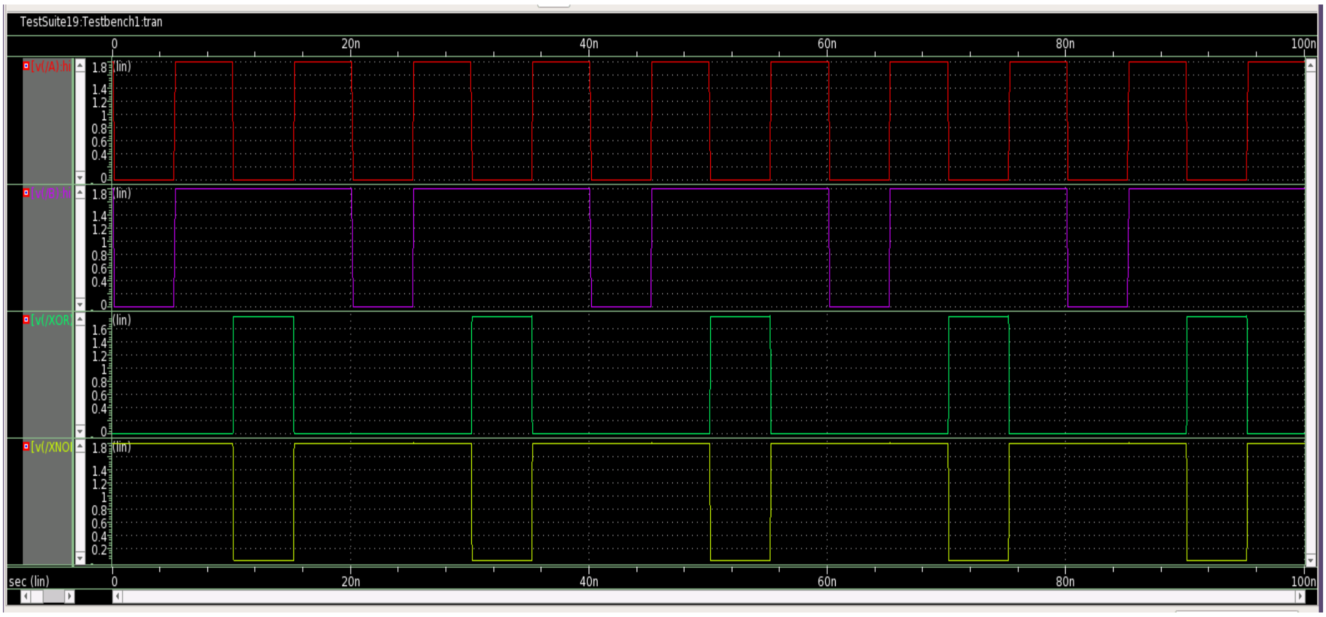
Parameters set for voltage Source for input B


Current Inst V2

Parameters

Prompt	Value
DC Voltage	0 V
Voltage1	1.8 V
Voltage2	0 V
Delay Time	0.1n s
Rise Time	0.1n s
Fall Time	0.1n s
Pulse Width	5n s
Period	20n s
Period Jitter	
Seed	
AC Magnitude	
AC Phase	
# HB Tones	0
DC Resistance	
AC Resistance	
HB Resistance	
HBAC Resistance	
TRAN Resistance	
HBAC Magnitude	
HBAC Phase	

Output Waveforms



Netlists

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*** Design cell name: xorxnor_tb**

*** Design view name: schematic**

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***Custom Compiler Version S-2021.09**

***Fri Feb 25 06:24:42 2022**

. global vdd gnd!

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*** Library   : cp_lib1**

*** Cell   : xorxnor**

*** View   : schematic**

*** View Search List : hspice hspiceD schematic spice veriloga**

*** View Stop List : hspice hspiceD**

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.subckt xorxnor a b xnor xor

xm2 vdd xor xnor vdd p105 w=0.1u l=0.03u nf=1 m=1

xm1 a b xor vdd p105 w=0.1u l=0.03u nf=1 m=1

xm0 b a xor vdd p105 w=0.1u l=0.03u nf=1 m=1

xm5 b a xnor gnd! n105 w=0.1u l=0.03u nf=1 m=1

xm4 xnor b a gnd! n105 w=0.1u l=0.03u nf=1 m=1

xm3 gnd! xnor xor gnd! n105 w=0.1u l=0.03u nf=1 m=1

.ends xorxnor

****

*** Library : cp_lib1**

*** Cell : xorxnor_tb**

*** View : schematic**

*** View Search List : hspice hspiceD schematic spice veriloga**

*** View Stop List : hspice hspiceD**

****

xi0 a b xnor xor xorxnor

v2 b gnd! dc=0 pulse (1.8 0 0.1n 0.1n 0.1n 5n 20n)

v1 a gnd! dc=0 pulse (1.8 0 0.1n 0.1n 0.1n 5n 10n)

v3 vdd gnd! dc=1.8

.tran '5n' '100n' name=tran

.option primesim_remove_probe_prefix = 0

.probe v(*) i(*) level=1

.probe tran v(xnor) v(xor) v(net5) v(net7)

.temp 25

.option primesim_output=wdf

.option parhier = LOCAL

.end

Acknowledgments

1. Kunal Ghosh, Co-founder, VSD Corp. Pvt. Ltd. - kunalpghosh@gmail.com
2. SFAL HACKATHON TEAM
3. Synopsys Team/Company.

Conclusion

In this paper, we proposed the new design of combination XOR-XNOR circuit configuration is based on the Pass Transistor Logic and CMOS inverter. The performances of this circuit have been compared to previous reported XOR XNOR design based on delay, power dissipation and PDP. According to the simulation results, the proposed circuit offers a better and more competitive than other design. It offers the lowest power dissipation at a low supply voltage. It has a good driving capability with good output signal in all input combinations and better performance especially in low supply voltage compared to the previous designs. Thus, the proposed circuit is suitable for low-voltage and low power application.

References

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circuits”, IEEE Transactions on Circuits and Systems– Regular Papers, Vol. 53, No. 4, 2006, pp. 867-878.