ESc201 : Introduction to Electronics

Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs)

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Introduction

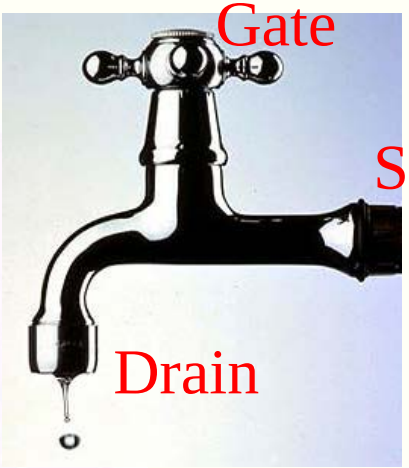
Classification of MOSFET

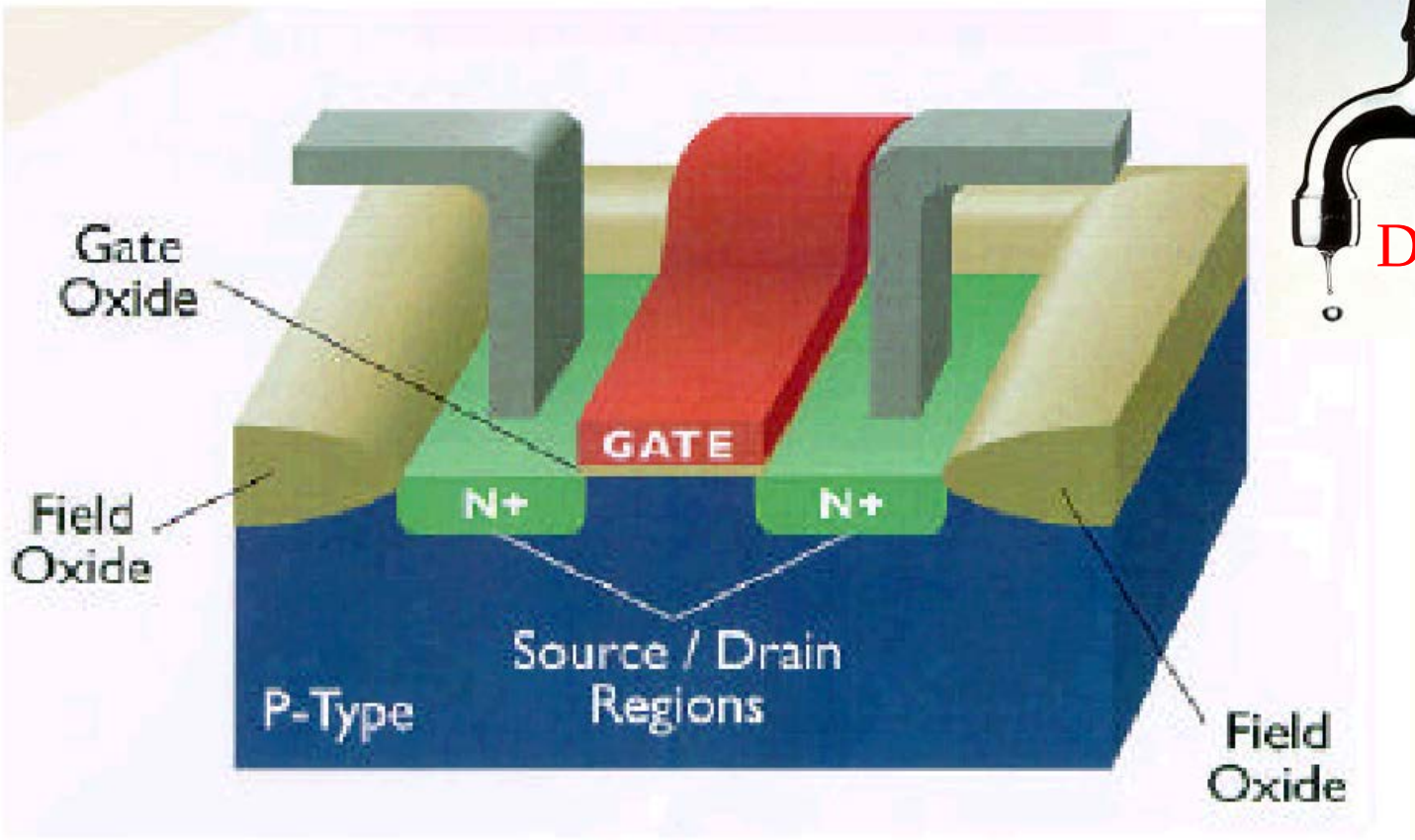
- P channel
  - ✓Enhancement type
  - ✓Depletion type
- N channel
  - ✓Enhancement type
  - ✓Depletion type

Widely used in IC circuits

MOSFET

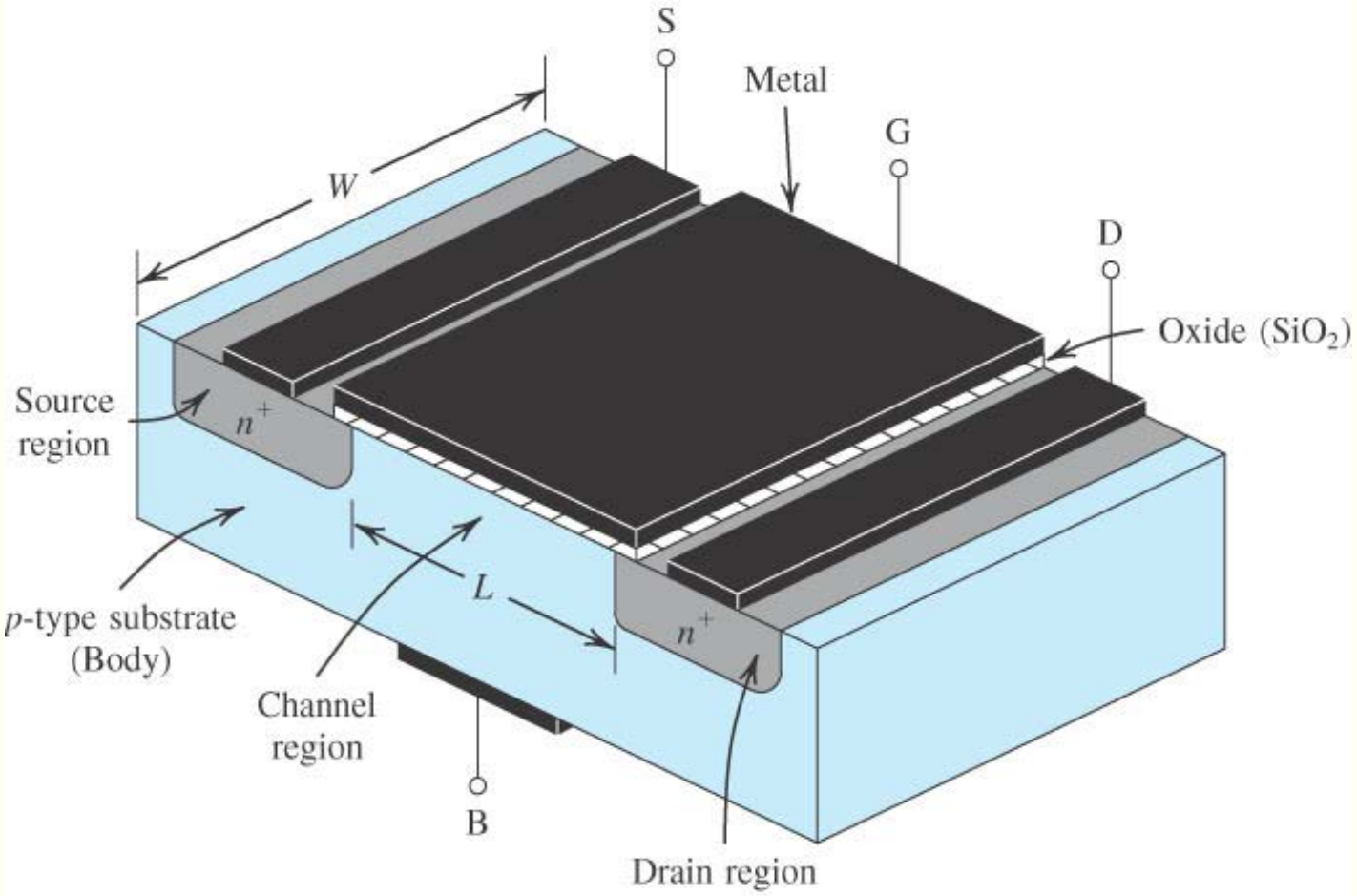
Metal Oxide Semiconductor Field Effect Transistor





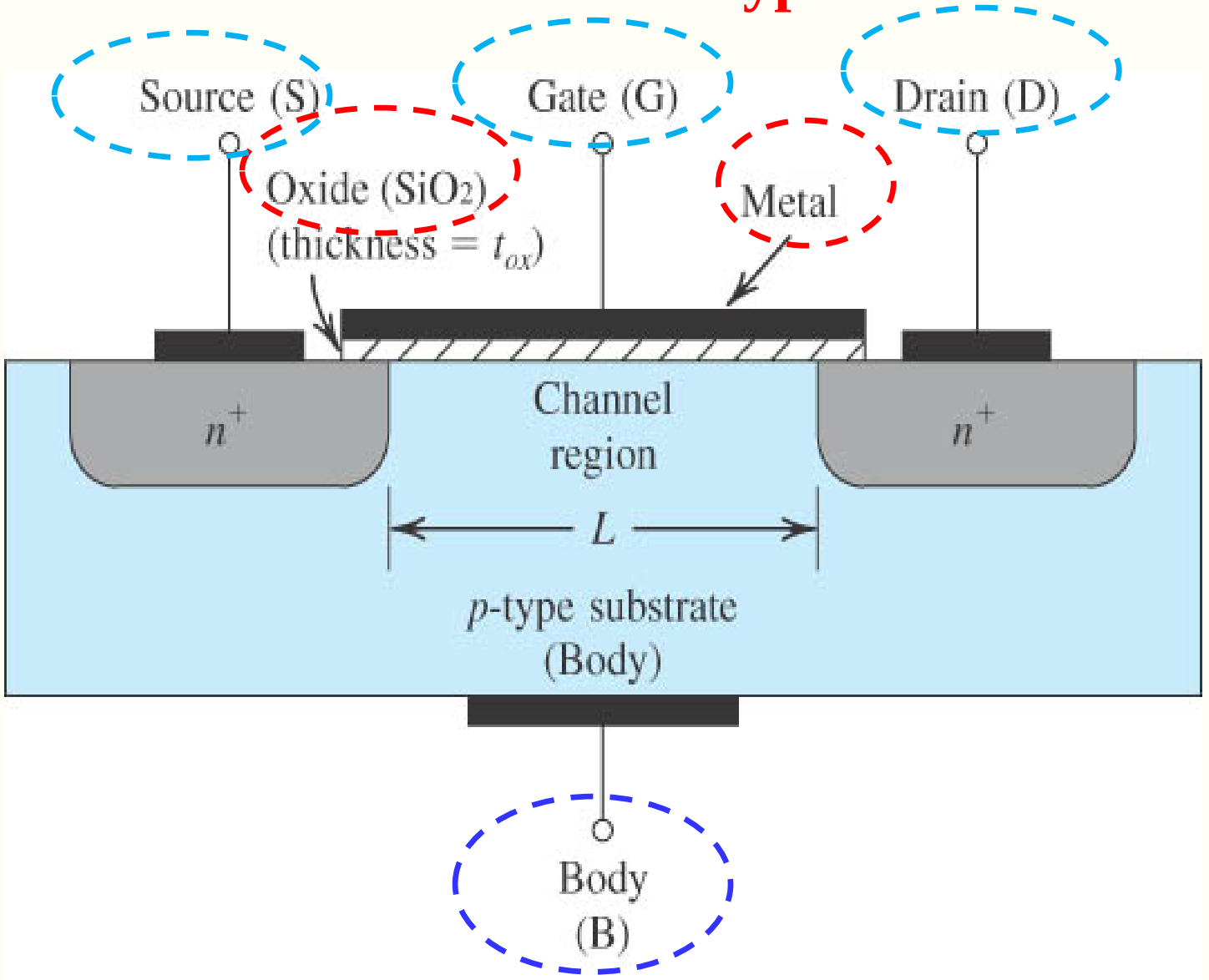
An NMOSFET

Device Structure of Enhancement-Type NMOS

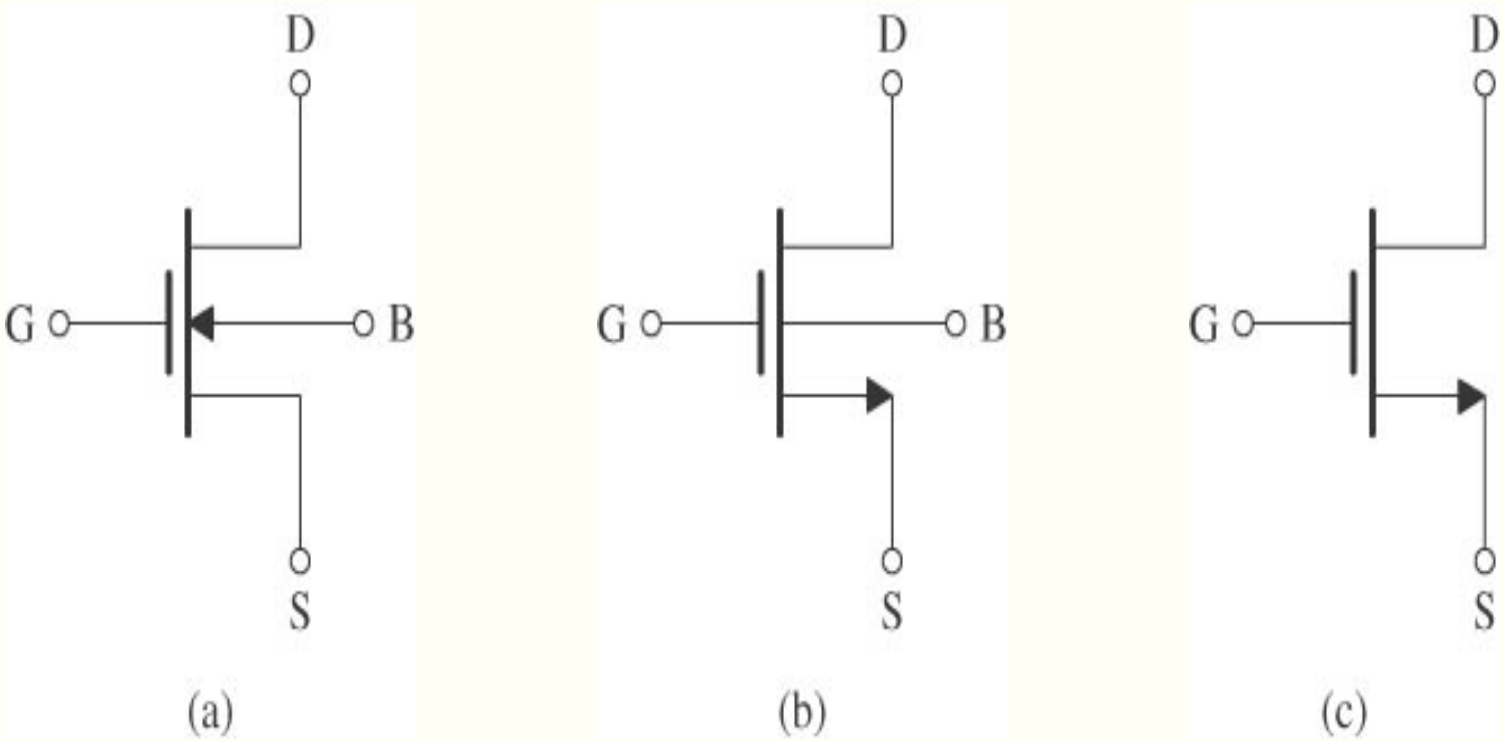


L: 1 to 10 μm
W: 2 to 500 μm
Thickness of oxide layer: 0.02 to 0.1 μm

Device Structure of Enhancement-Type NMOS



Symbols



NMOSFET

(a) Circuit symbol for the *n*-channel enhancement-type MOSFET.

(b) Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel).

(c) Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

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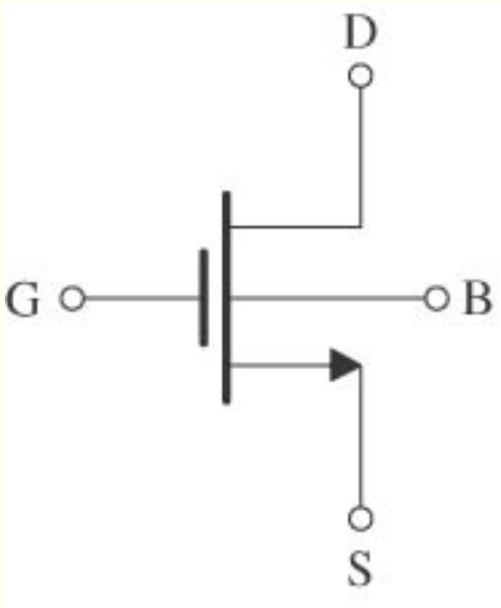
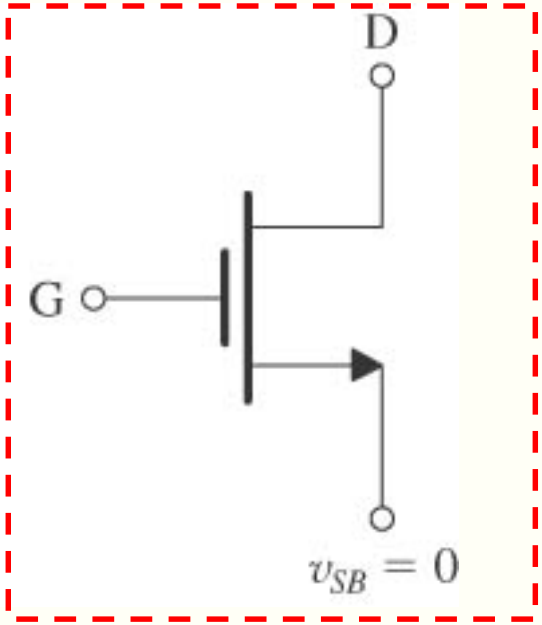
Symbols

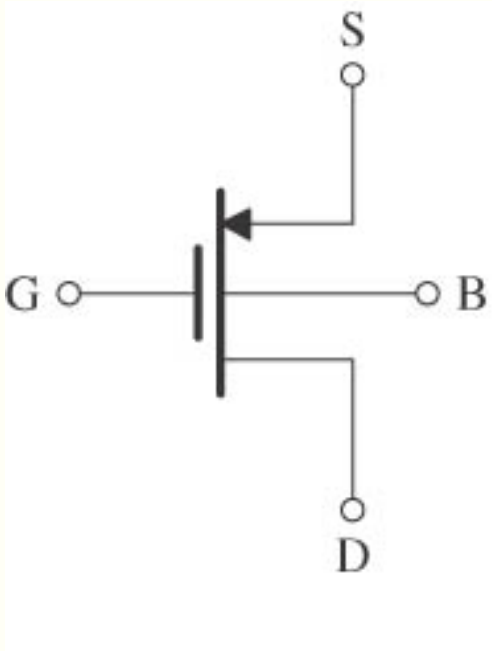
NMOSFET

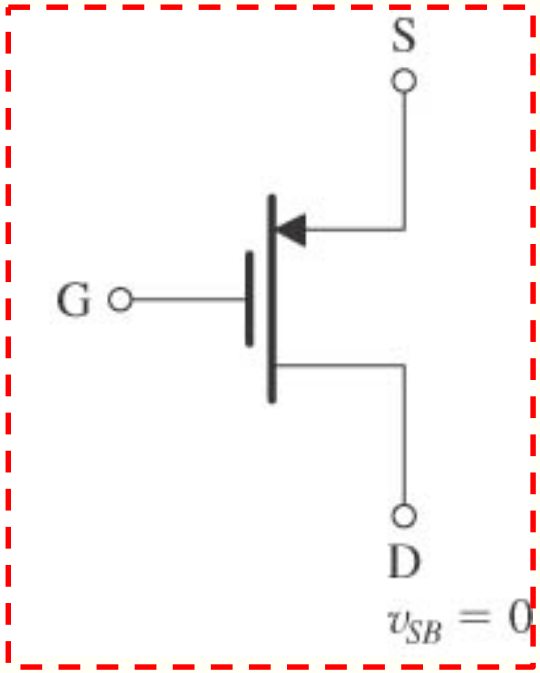




Mostly Used

PMOSFET

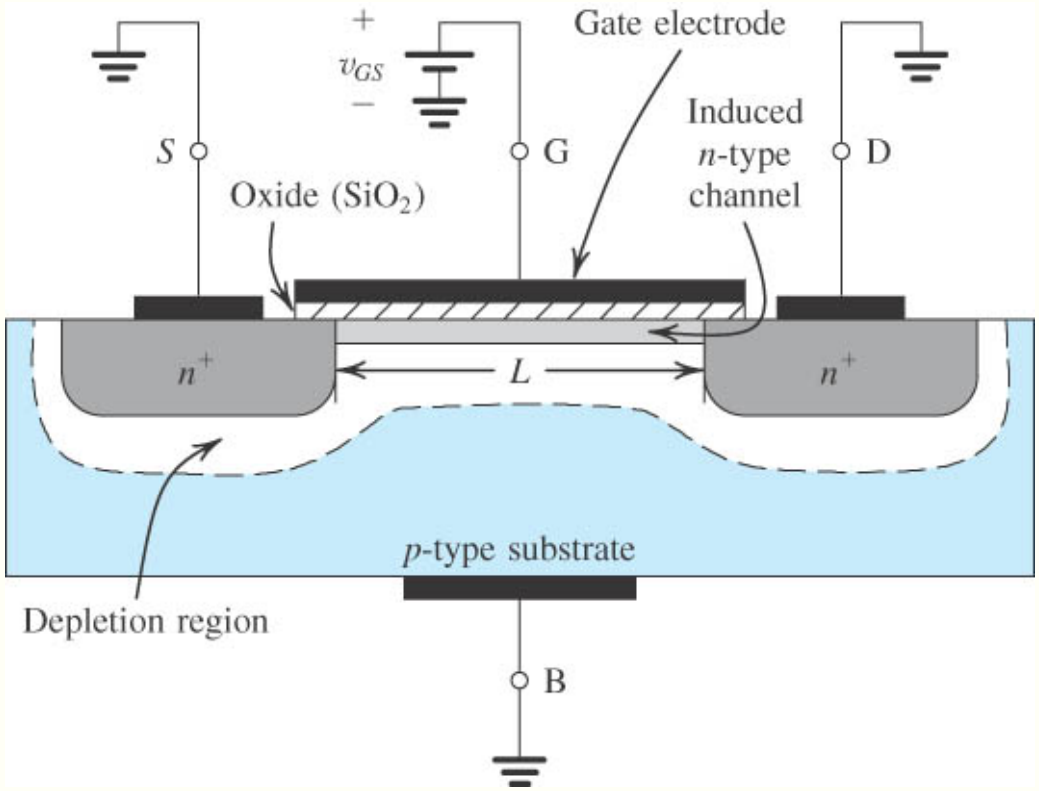




Physical Operation

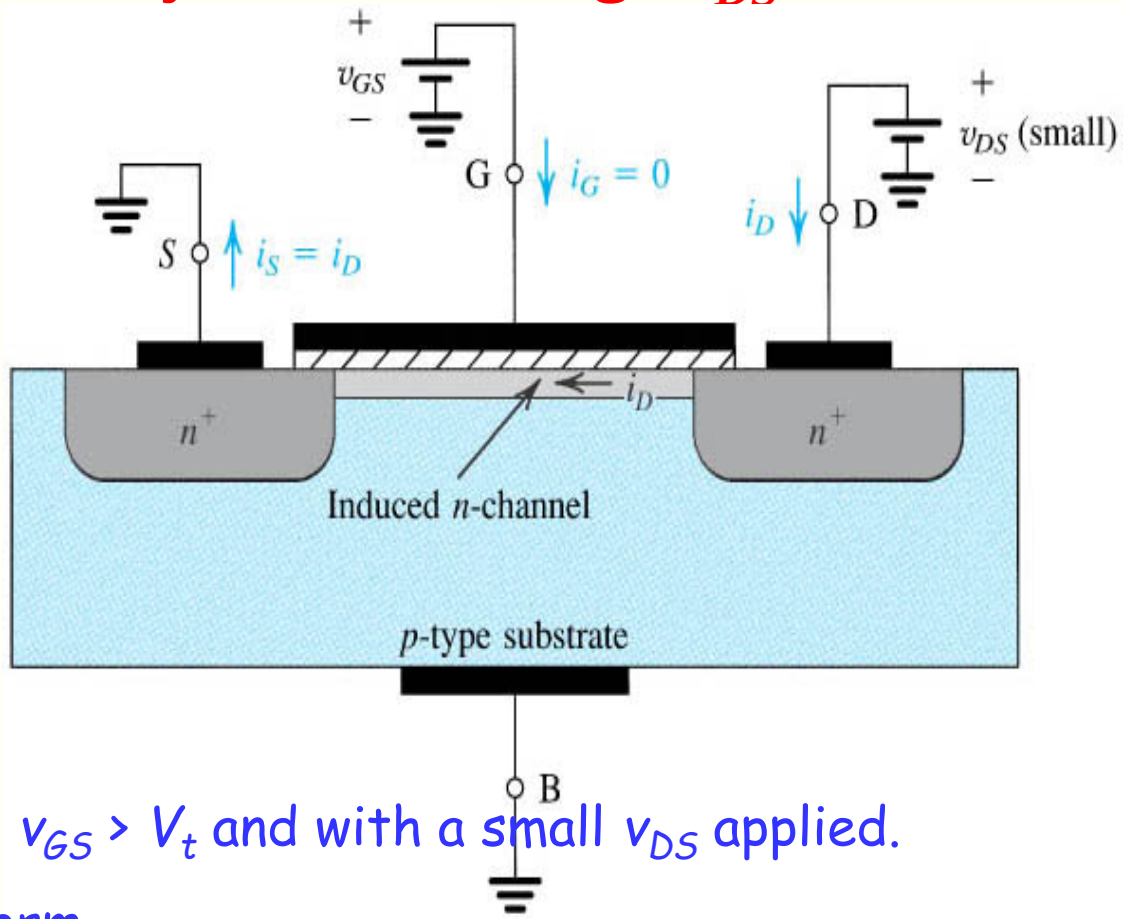
- Creating an *n* channel
- Drain current controlled by v_{DS}
- Drain current controlled by v_{GS}

Creating a Channel for Current Flow



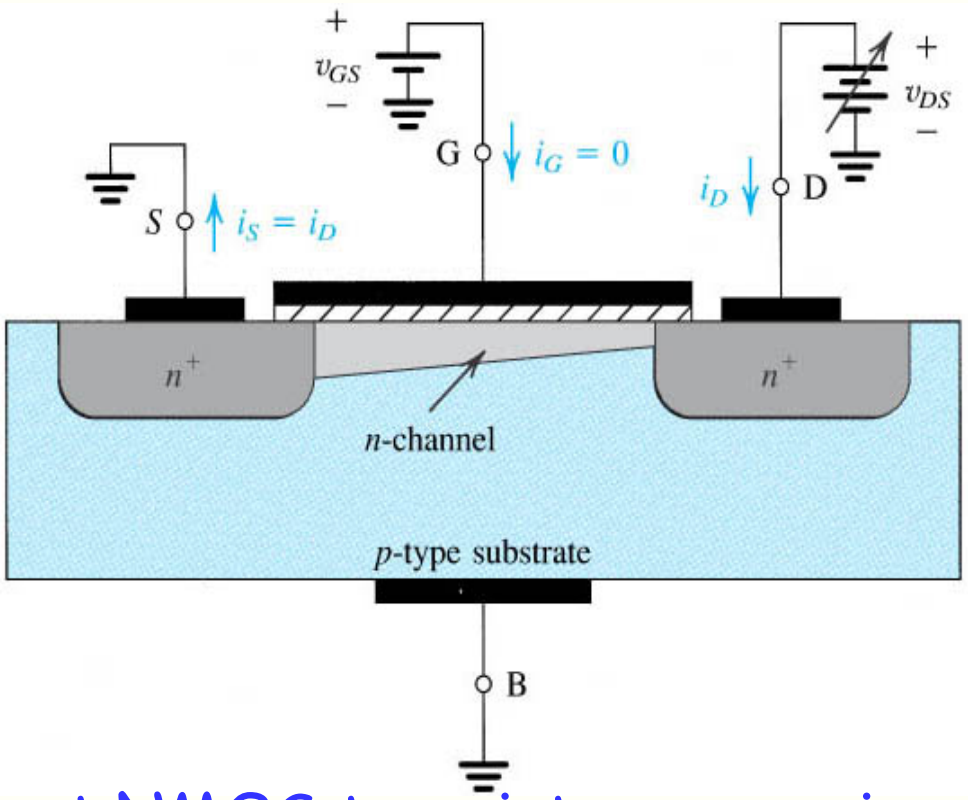
- The enhancement-type NMOS transistor with a positive voltage applied to the gate.
- An *n* channel is induced at the top of the substrate beneath the gate.

Drain Current Controlled by Small Voltage v_{DS}



- An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied.
- The channel depth is uniform.
- The device acts as a resistance.
- The channel conductance is proportional to effective voltage.
- Drain current is proportional to $(v_{GS} - V_t)\, v_{DS}$.

v_{DS} is increased



- Operation of the enhancement NMOS transistor as v_{DS} is increased.
- The induced channel acquires a tapered shape.
- Channel resistance increases as v_{DS} is increased.
- Drain current is controlled by both of the two voltages.

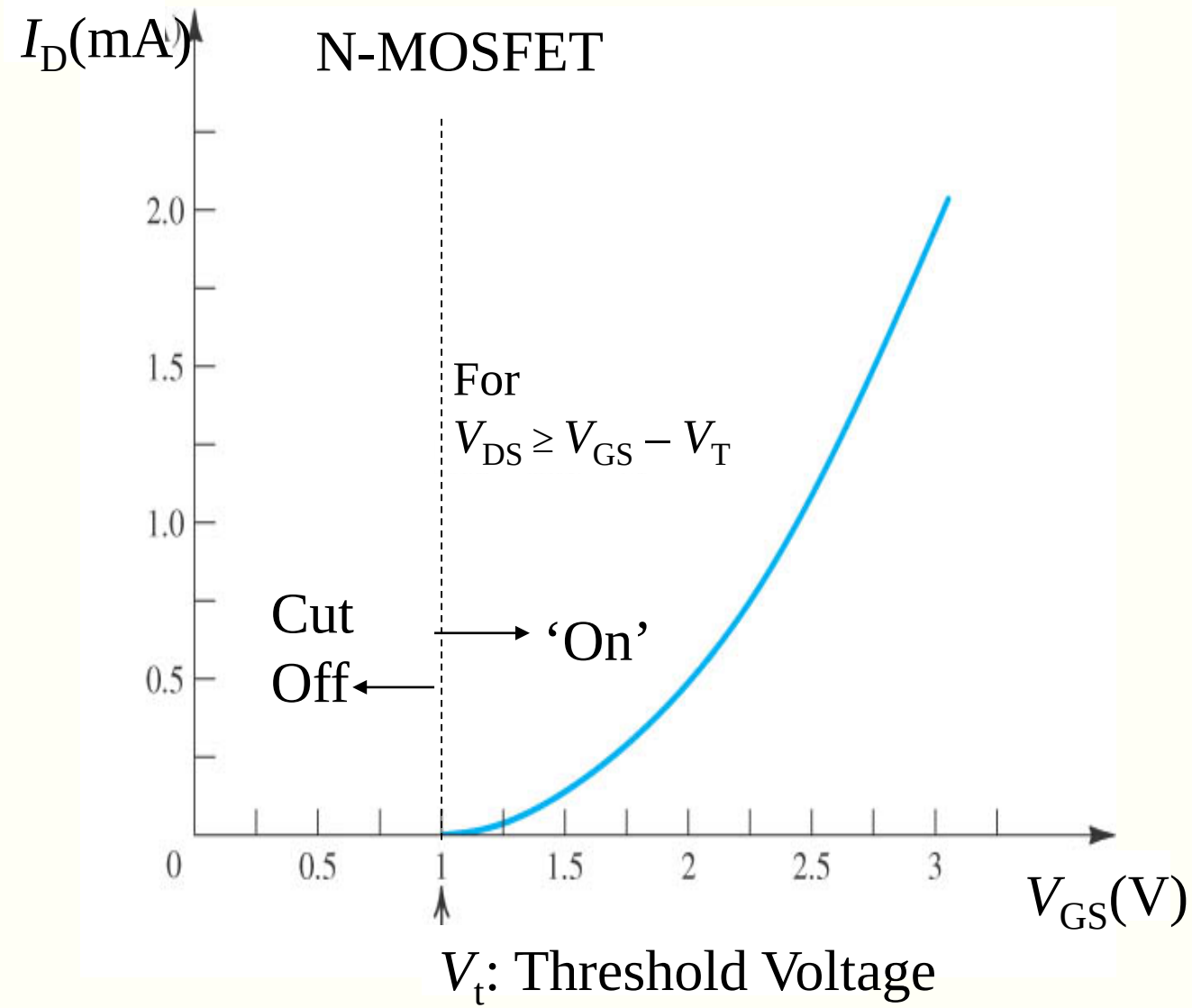
Channel Pinch- Off

- Channel is pinched off
  - Inversion layer disappeared at the drain point
  - Drain current is n't disappeared
- Drain current is saturated and only controlled by the v_{GS}
- Triode region and saturation region

Drain Current Controlled by v_{GS}

- v_{GS} creates the channel.
- Increasing v_{GS} will increase the conductance of the channel.
- At saturation region only the v_{GS} controls the drain current.
- At subthreshold region, drain current has the exponential relationship with v_{GS}

Transfer Characteristics



V_t: Threshold Voltage

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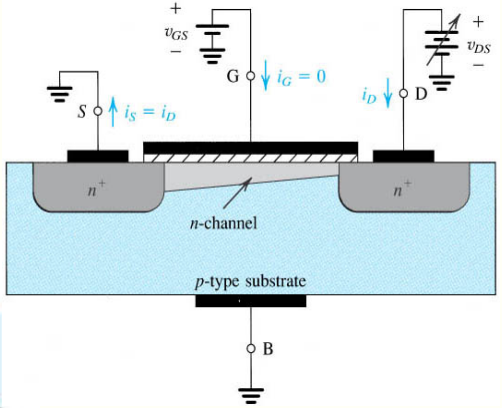
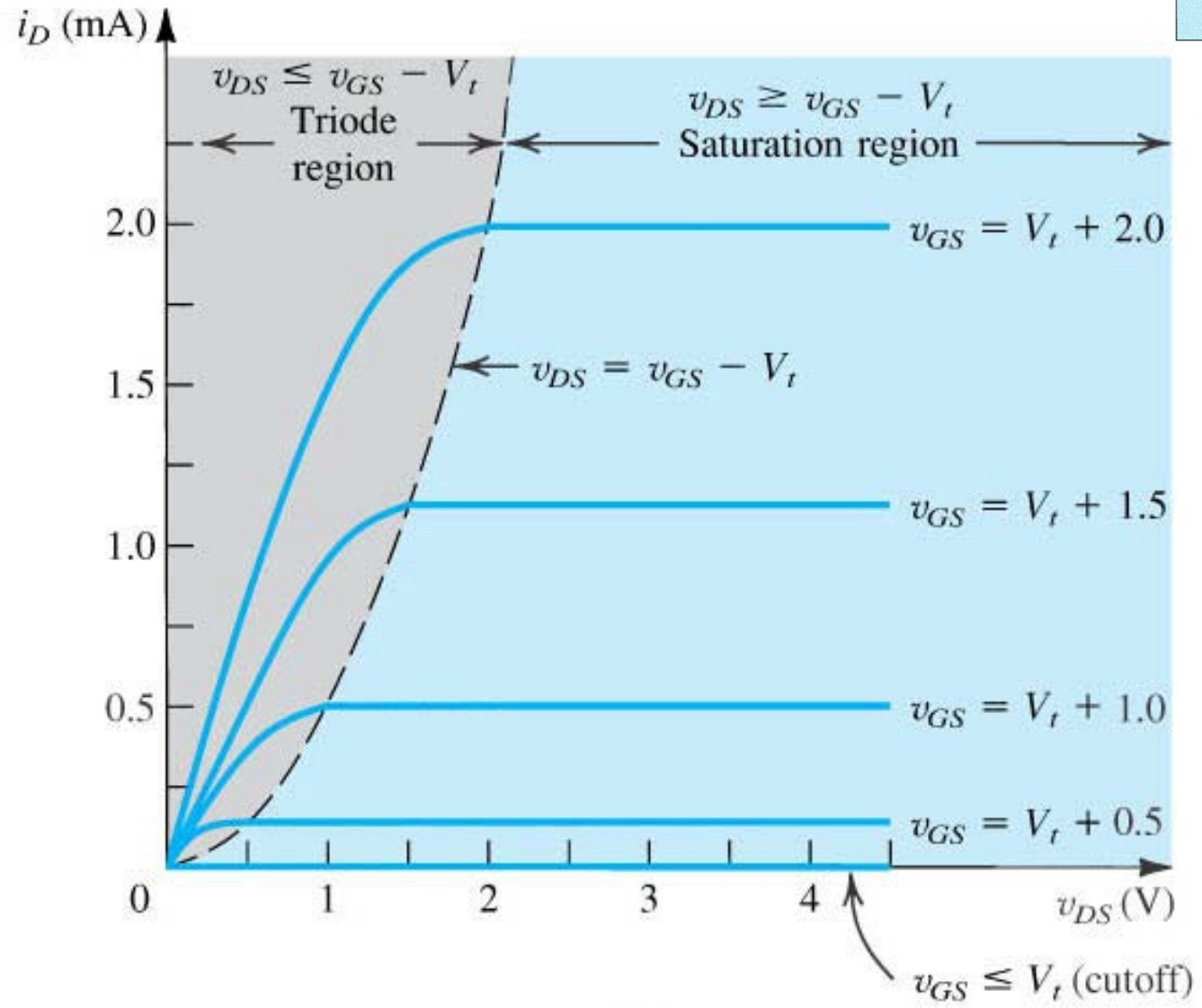
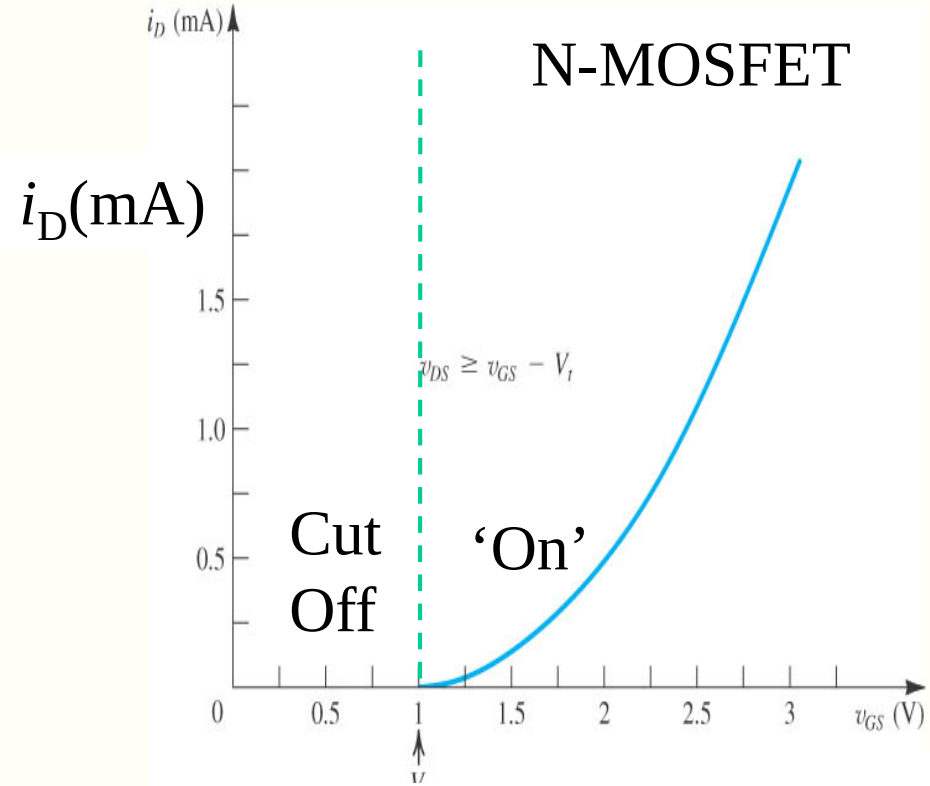
I-V Characteristics

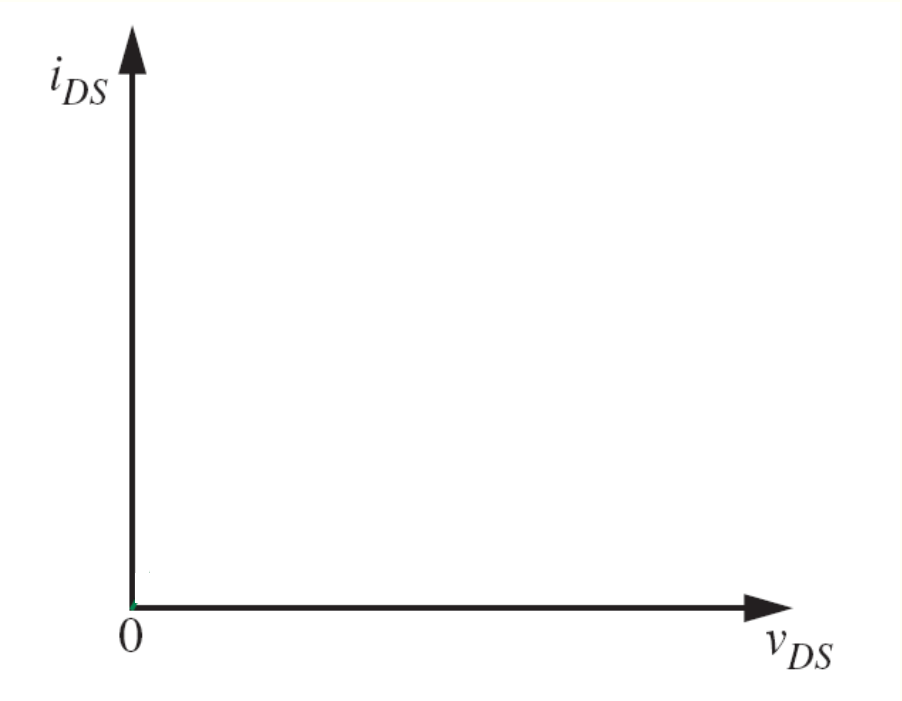




Regions of Transistor 'Operation'

- **Cut off region ($v_{GS} < V_t$)**
  - Input voltage less than threshold voltage





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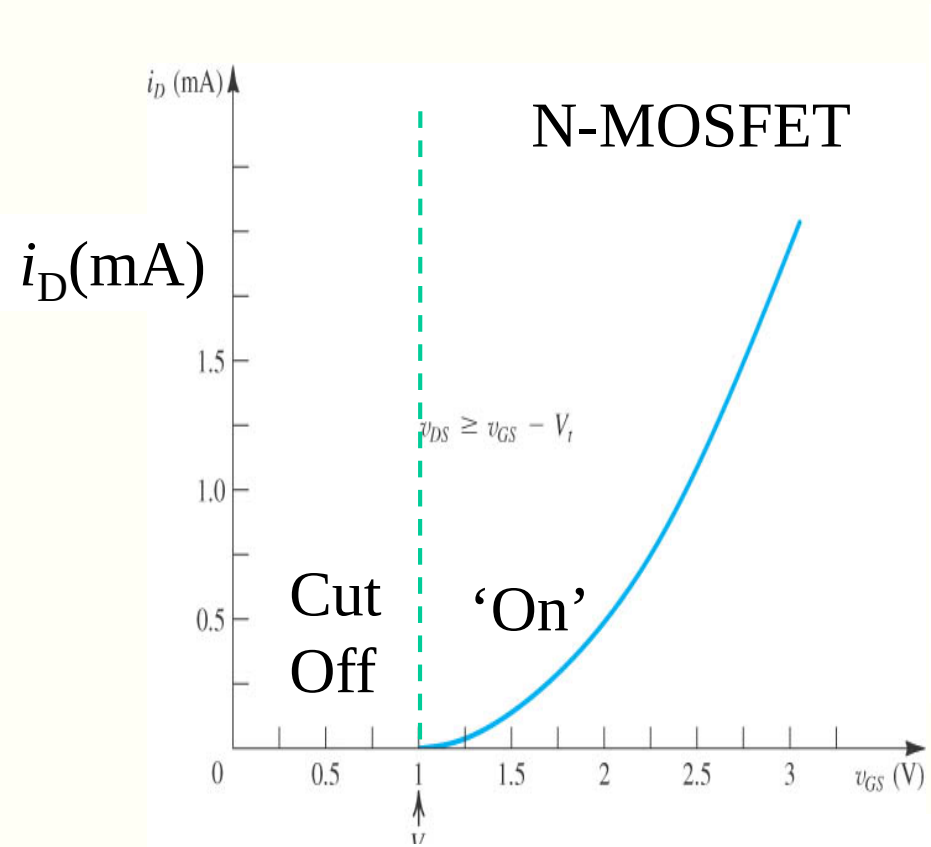
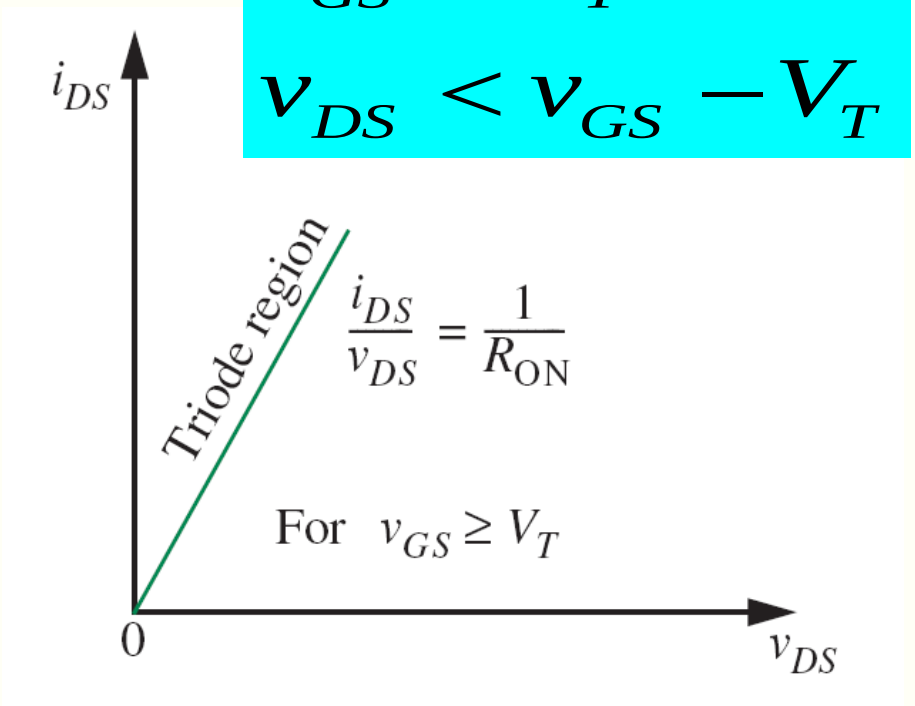
Regions of Transistor 'Operation'

- **Triode region ($v_{GS} > V_T$ and $v_{DS} < v_{GS} - V_T$)**
  - Linear relationship between i_{DS} and v_{DS} reflects resistive behaviour for small v_{DS}

$$v_{GS} > V_T$$

$$v_{DS} < v_{GS} - V_T$$





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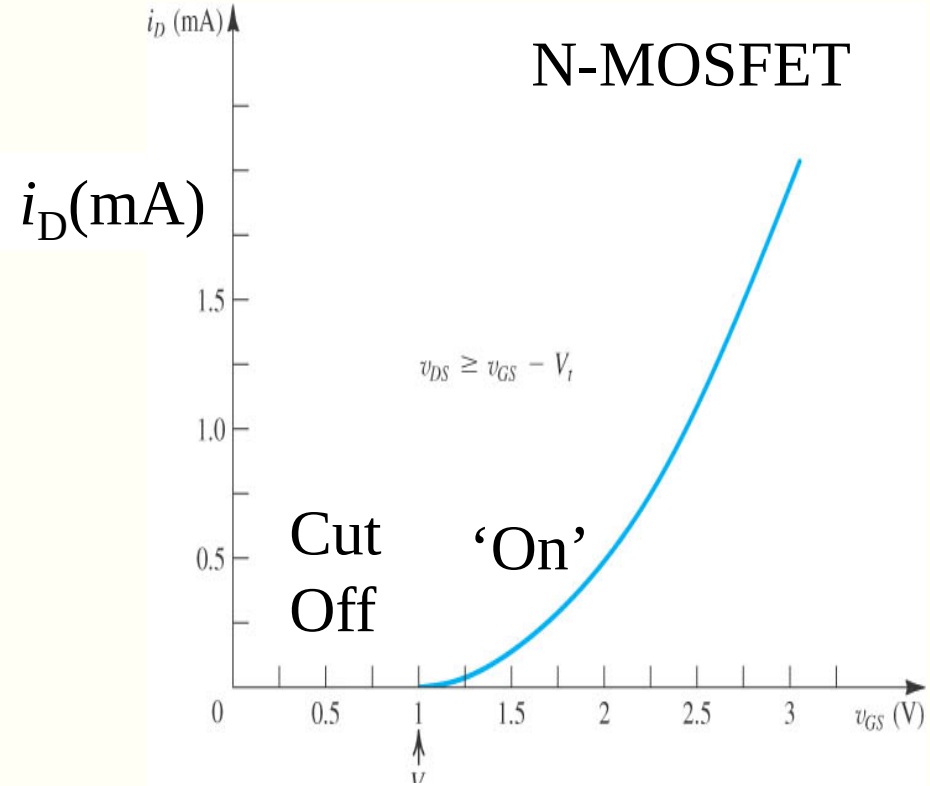
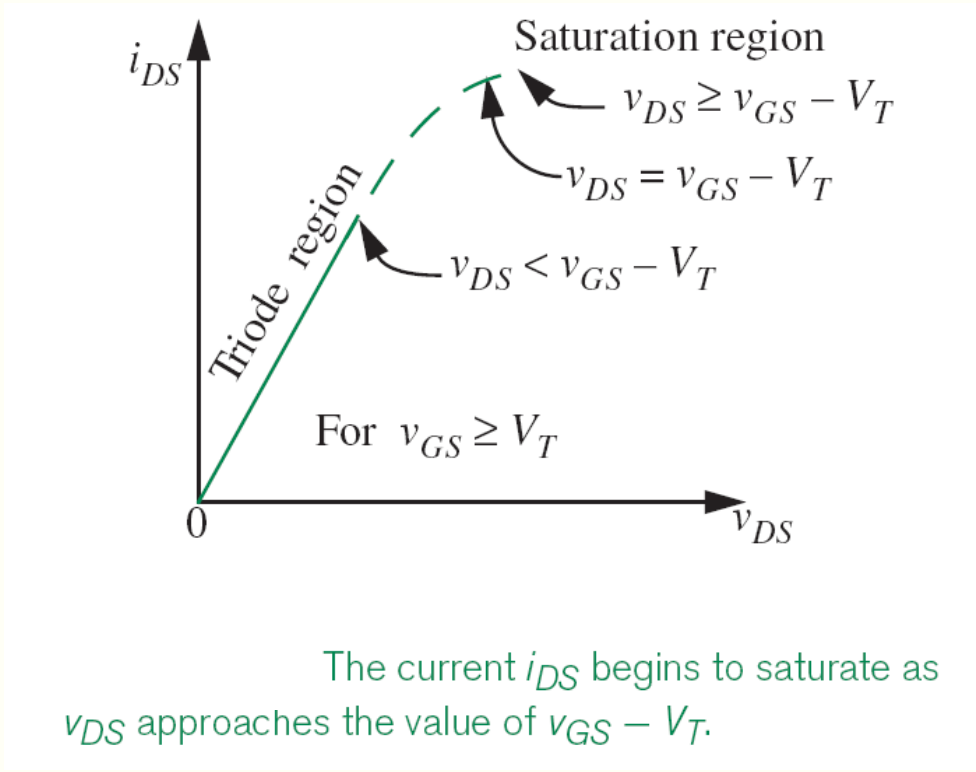
Regions of Transistor 'Operation'

- **Saturation region ($v_{GS} > V_T$ and $v_{DS} \geq v_{GS} - V_T$)**
  - Transistor is 'on'
  - Drain bias is above saturation voltage
  - Amplifier should operate in this region

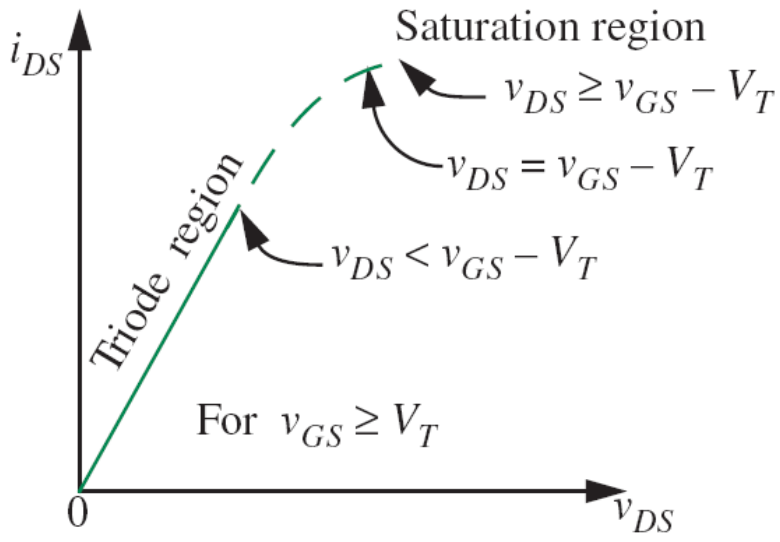
$$v_{GS} > V_T$$
$$v_{DS} > v_{GS} - V_T$$

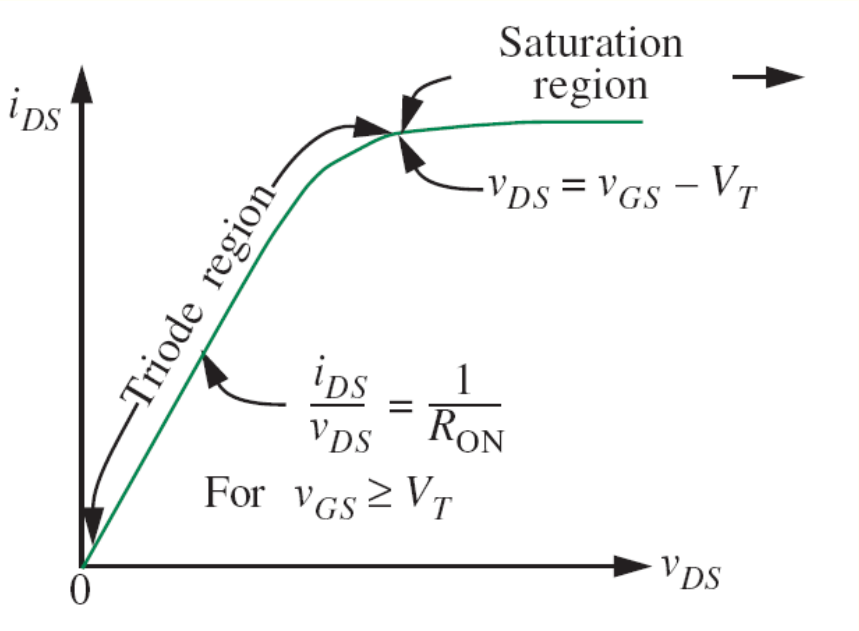


V_T: Threshold Voltage



Saturation region ($v_{GS} > V_T$ and $v_{DS} > v_{GS} - V_T$)





The current i_{DS} *begins to saturate as* v_{DS} *approaches the value of* $(v_{GS} - V_T)$.

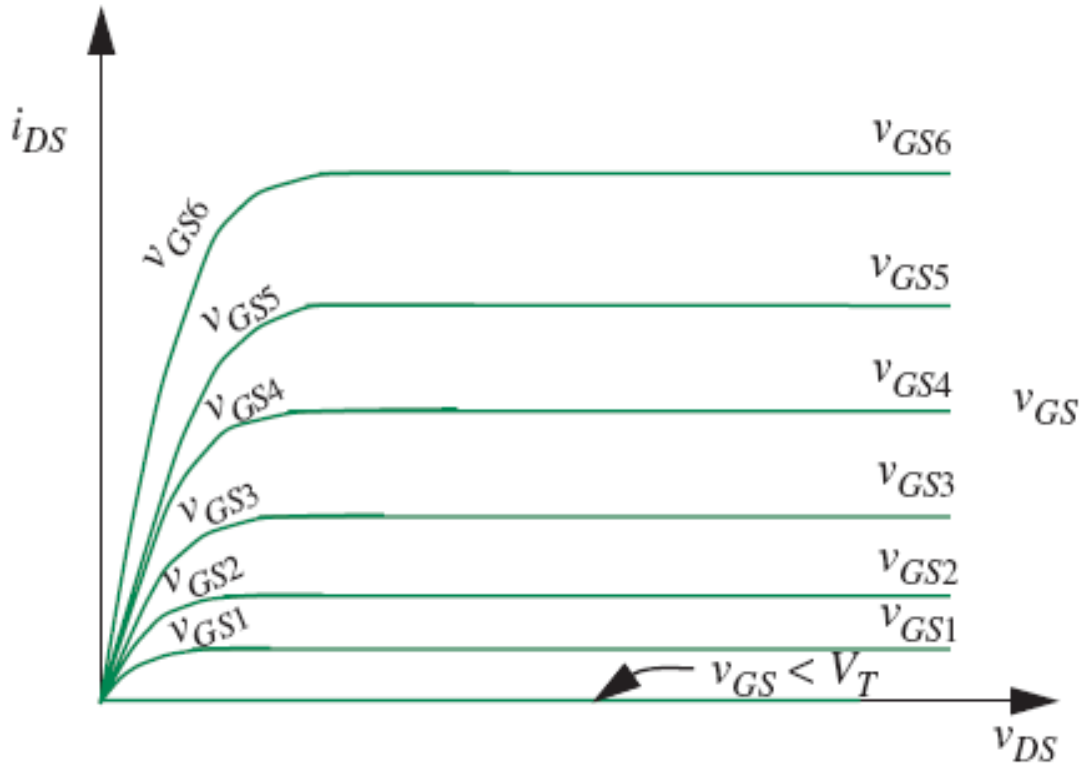
The saturation region of MOSFET Operation

MOSFET operates in saturation region when following two conditions are met:

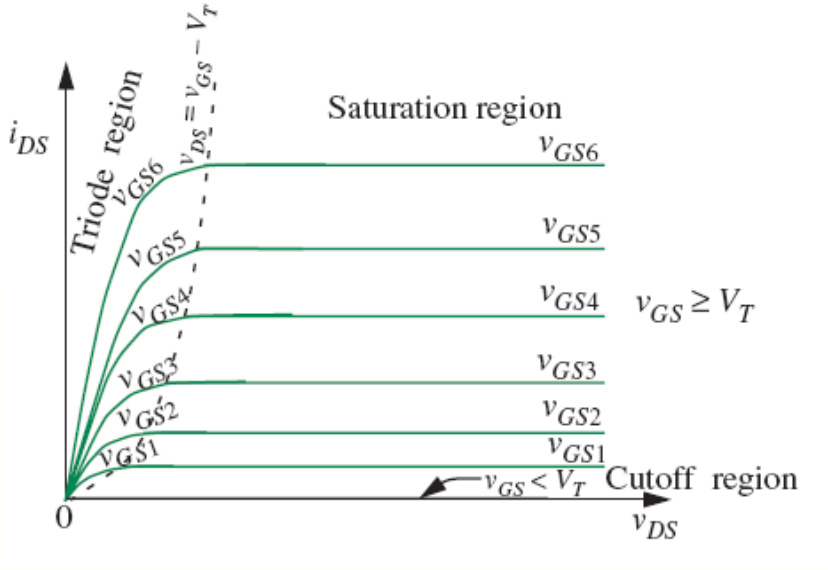
$$v_{GS} > V_T$$

$$v_{DS} > v_{GS} - V_T$$

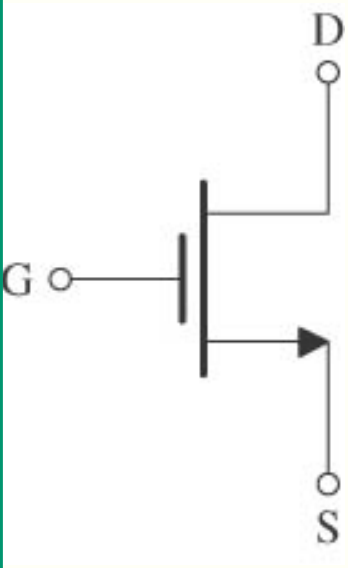
Different values of v_{GS} (> V_t) provides different $i_{DS}$and v_{DS} Characteristics



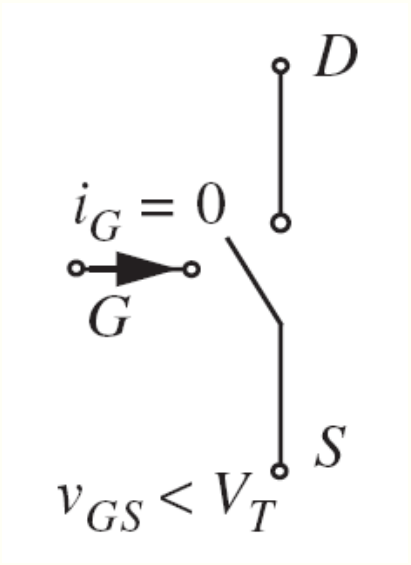
$v_{GS} \geq V_T$



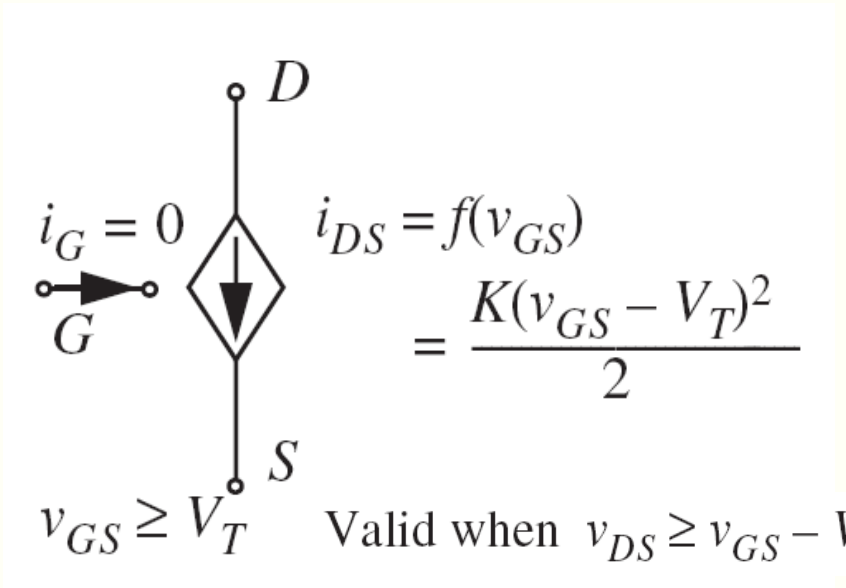
The Switch Current Source MOSFET Model



MOS Device



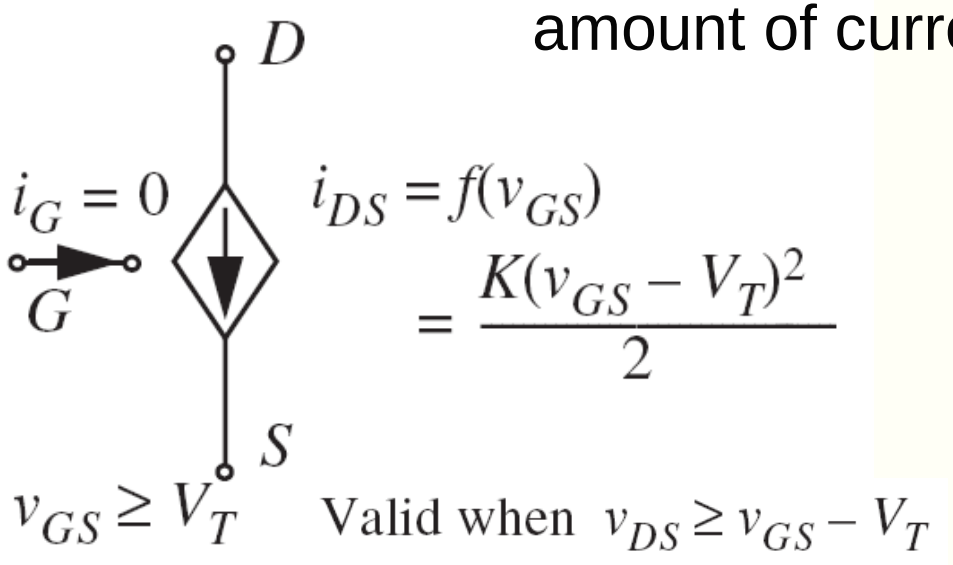
Open State



Closed State

The Switch Current Source MOSFET Model

When $v_{GS} > V_T$ and $v_{DS} > v_{GS} - V_T$ the amount of current provided by the source is



$$i_D = \frac{K}{2}\left(v_{GS} - V_T\right)^2$$

Unit of K: A/V^2

where $K = k_n' \frac{W}{L} = \mu_n C_{ox}$

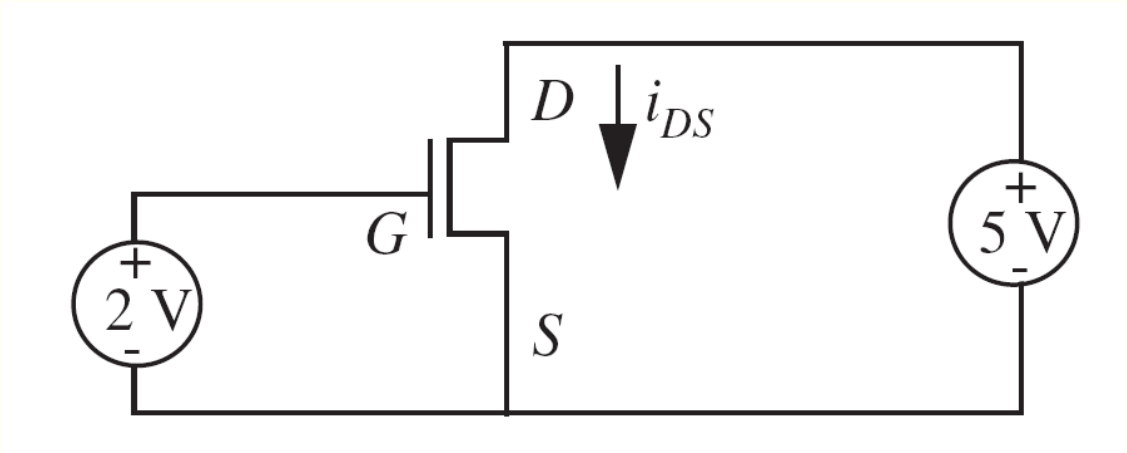
W: gate width; **L:** gate Length

k'_n: Constant related to MOSFET properties (A/V^2)

μ_n: Electron mobility in channel

Cox: Capacitance per unit area of parallel plate capacitor by gate electrode and channels

Example-1: Determine the current i_{DS} for the circuit shown below.
Assume: K= 1mA/V^2 and V_T = 1V

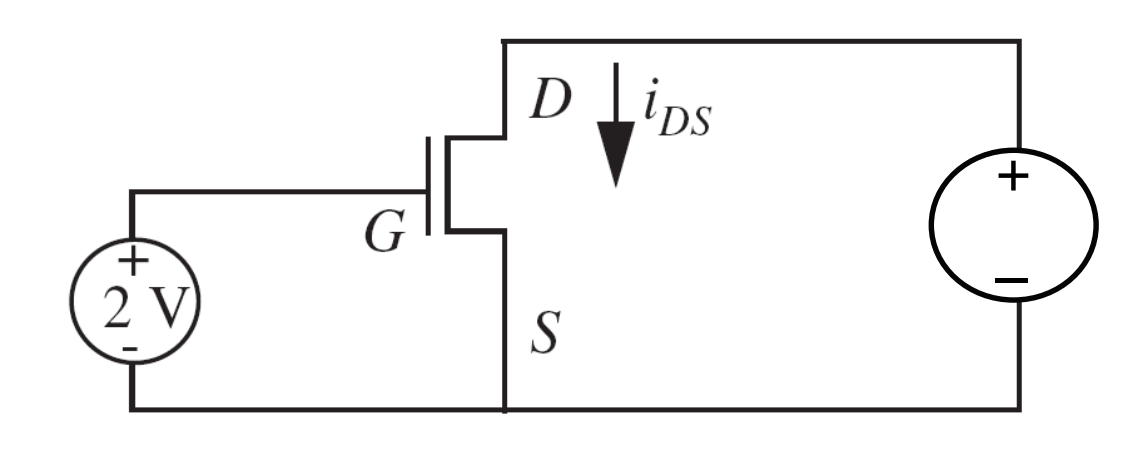


$$i_D = \frac{K}{2}\left(v_{GS} - V_T\right)^2$$

$$i_D = \frac{1}{2}(2-1)^2$$

$$i_D = 0.5 \quad \text{mA}$$

Example-2: Assume: K= 1mA/V^2 and V_T = 1V



What should be the minimum value of the drain to source v_{DS} for which MOSFET will operate in saturation region. (Assume V_{GS} is 2V)

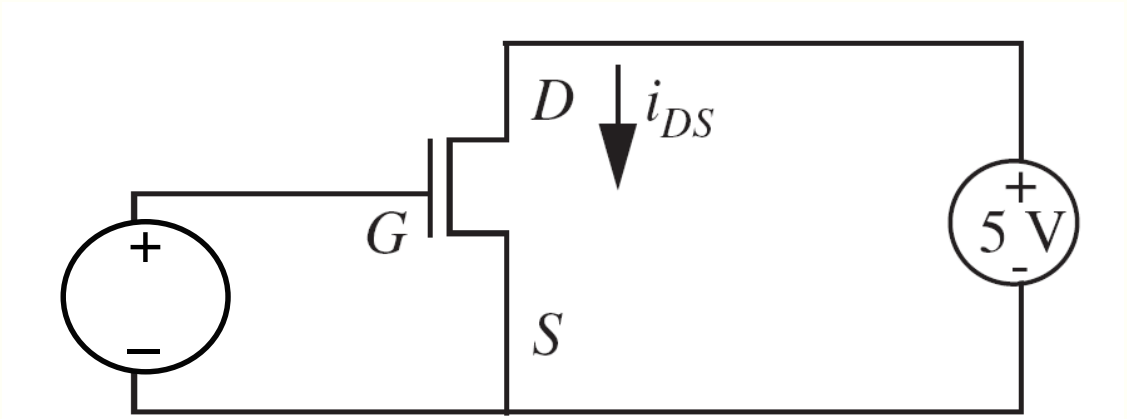
For the MOSFET to operate in saturation:

$$v_{GS} > V_T$$

$$v_{DS} > v_{GS} - V_T$$

$$v_{DS} > 1 \quad \text{V}$$

Example-3: Assume: K= 1mA/V^2 and V_T = 1V



What is maximum value of v_{GS} for which MOSFET will operate in saturation region

For the MOSFET to operate in saturation:

$$v_{GS} > V_T$$

$$v_{DS} > v_{GS} - V_T$$

$$5 > v_{GS} - 1$$

$$v_{GS} < 6 \quad \text{V}$$

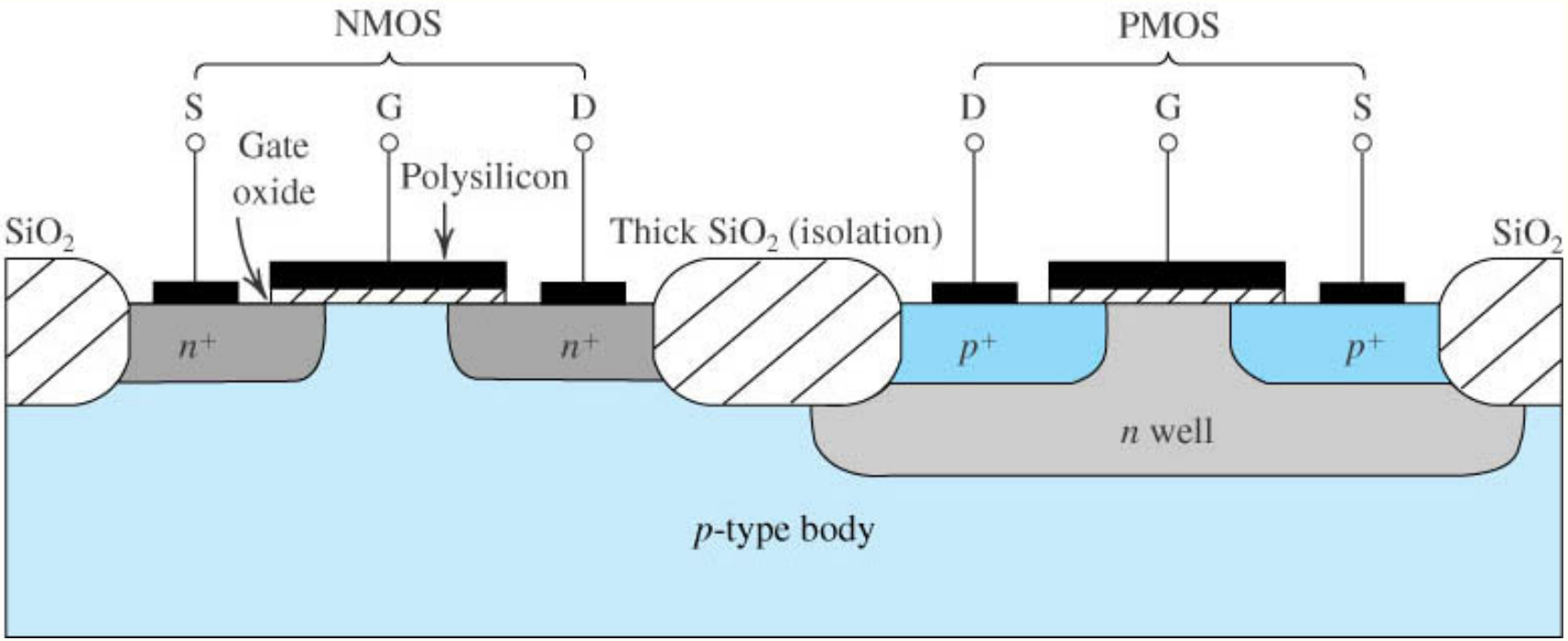
$$v_{GS} > 1 \quad \text{V}$$

$$1 \ \text{V} < v_{GS} < 6 \quad \text{V}$$

p Channel Device

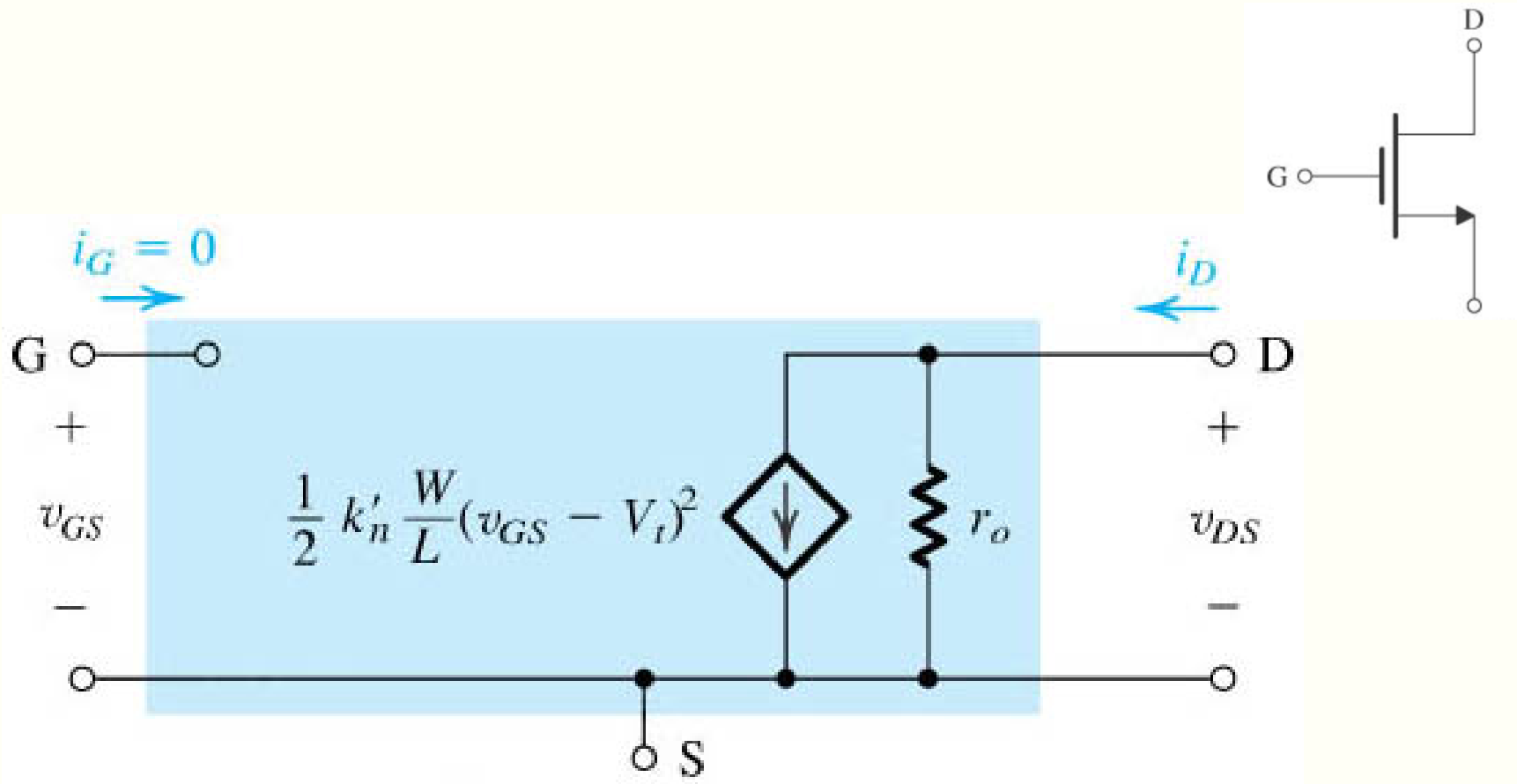
- Structure of p channel device
  - The substrate is *n* type and the inversion layer is *p* type.
  - Carrier is hole.
  - Threshold voltage is negative.
  - All the voltages and currents are opposite to the ones of *n* channel device.
  - Physical operation is similar to that of *n* channel device.

Complementary MOS or CMOS



- The PMOS transistor is formed in *n* well.
- Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a *p* well.
- CMOS is the most widely used of all the analog and digital IC circuits.

Large Signal Equivalent Circuit Model for NMOS



Large Signal Equivalent circuit model of the *n*-channel MOSFET in saturation, incorporating the output resistance r_o. The output resistance models the linear dependence of i_D on v_{DS}

MOSFET Circuit: DC Analysis

a. Assuming device operates in saturation thus i_D satisfies with $i_D \sim v_{GS}$ equation.

b. According to biasing method, write voltage loop equation.

c. Combining above two equations and solve these equations.

d. Usually we can get two value of v_{GS}, only the one of two has physical meaning.

e. Checking the value of v_{DS}

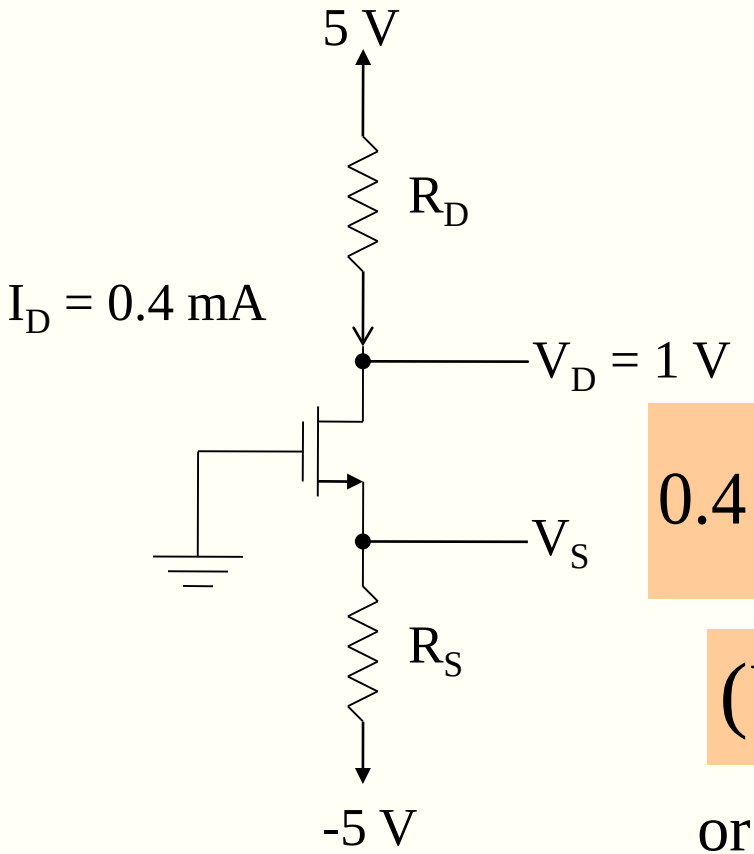
   i. if $v_{DS} \geq v_{GS} - V_t$, assumption is correct.

   ii. if $v_{DS} \leq v_{GS} - V_t$, assumption is not correct.

Example 4 (DC Analysis of MOSFET Circuits)

Design the circuit shown in figure so that the MOSFET operates in saturation region with $I_D = 0.4$ mA and $V_D = 1$ V. The MOSFET has $V_t = 2$ V, $\mu_n C_{0x} = 20\ \mu A/V^2$, $L = 10\ \mu m$ and $W = 400\ \mu m$.

$r_0 \rightarrow \infty$



$$R_D = \frac{5-1}{0.4\,\text{mA}} = 10\,\text{K}\Omega$$

$$I_D = \frac{1}{2}\mu_0 C_{0x}\frac{W}{L}(V_{GS}-V_t)^2$$

$$0.4\,\text{mA} = \frac{1}{2}20\times10^{-6}\,\frac{\text{A}}{\text{V}^2}\cdot\frac{400}{10}(V_{GS}-2)^2$$

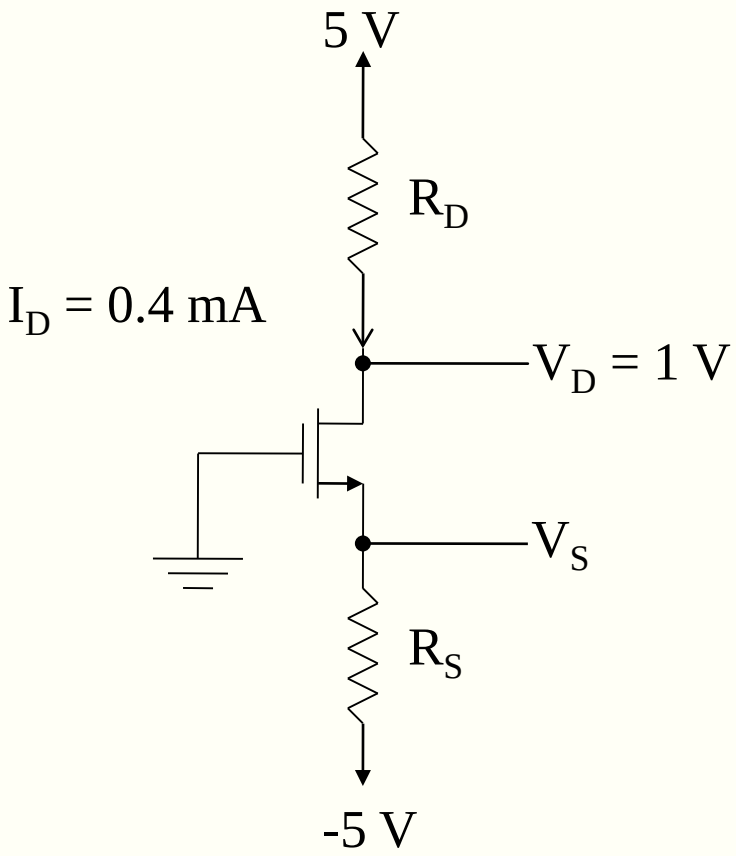
$$(V_{GS}-2)^2 = 1 \quad \Rightarrow \quad V_{GS}-2 = \pm 1$$

or $V_{GS} = +1$ V or $+3$ V

V_{GS} = +1 V or +3 V

$$v_{GS} > V_T$$

- The first solution is not consistent with our initial assumption of operation in the saturation mode V_t (=2 V)
  Therefore



$$V_{GS} = 3\ \text{V}$$

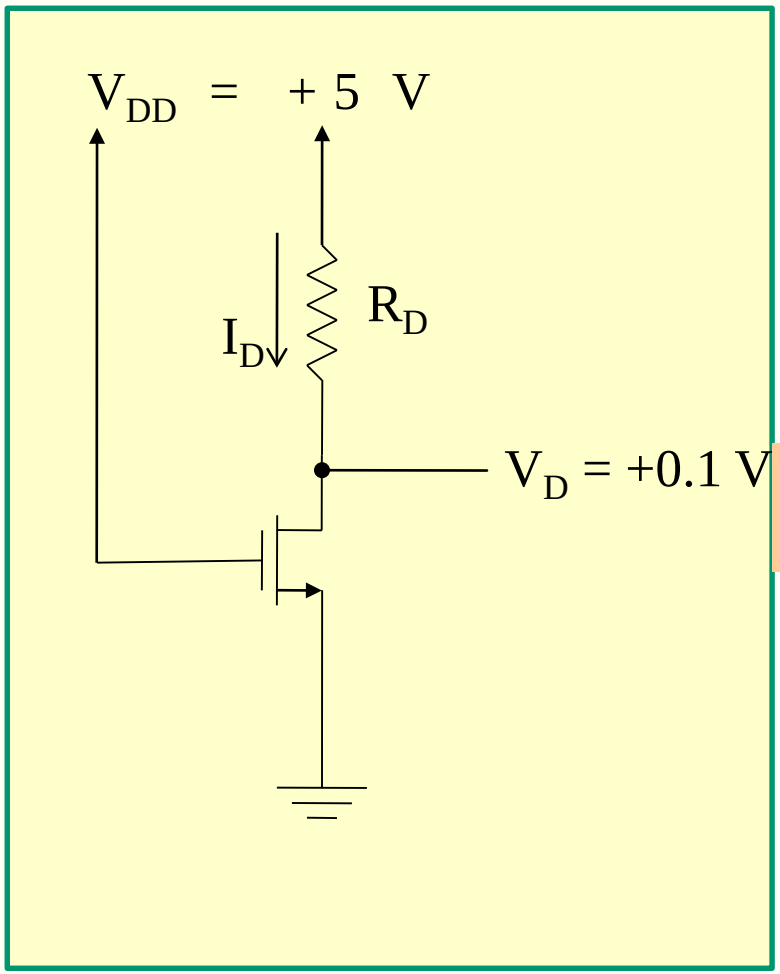
$$\Rightarrow \quad V_S = -3\ \text{V}$$

$$R_S = \frac{V_S - (-5)}{I_S} = \frac{V_S + 5}{I_D}$$

$$= \frac{-3+5}{0.4\,\text{mA}} = 5\,\text{K}\Omega$$

Example 5 (DC Analysis of MOSFET Circuits)

Design the circuit shown in figure for MOSFET to operate in saturation with drain voltage of 0.1 V. Determine R_D. The MOSFET has V_t = 1 V and kn`W/L = 1 mA/V^2 . Neglect $r_{0.}$



$$v_{GS} > V_T$$

$$v_{DS} > v_{GS} - V_T$$

$$V_T > v_{GD}$$

$V_{GS} = 5$ V $(>V_T)$ **MOSFET is ON**

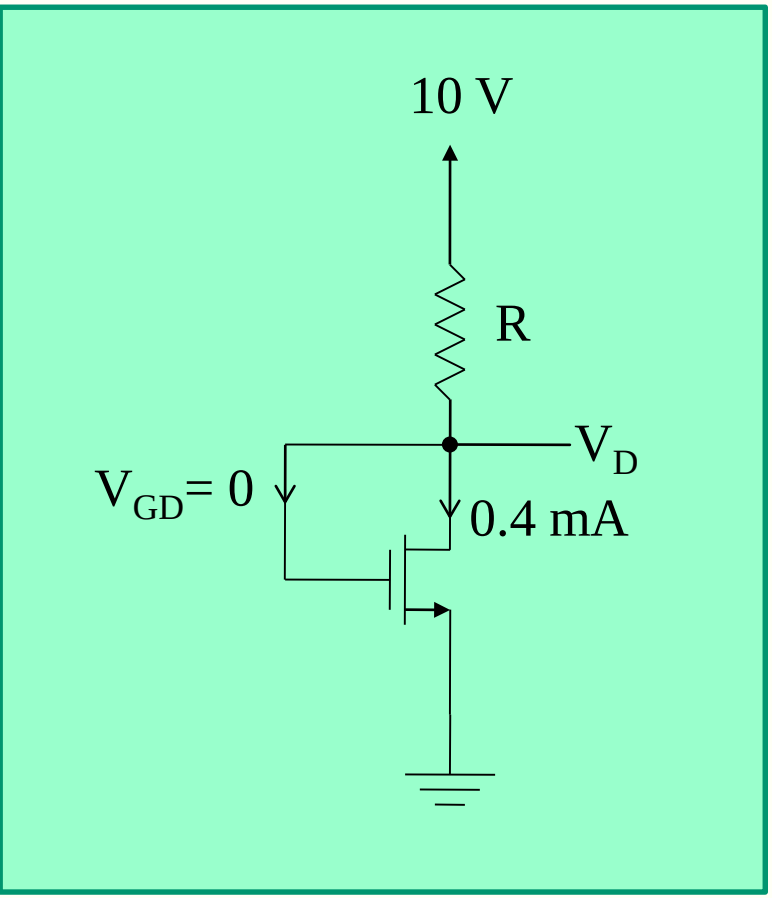
$V_{GD} = 5 - 0.1 = 4.9$ V

$$V_T < v_{GD}$$

MOSFET is not in saturation

Example 6 (DC Analysis of MOSFET Circuits)

Design the circuit as shown in figure so that the MOSFET operates in saturation region with $I_D = 0.4$ mA. The MOSFET has $V_t = 2$ V, $\mu_n C_{0x} = 20\ \mu A/V^2$, L = 10 μm and W = 100 μm. Neglect r_0 .



$$v_{GS} > V_T$$

$$v_{DS} > v_{GS} - V_T$$

$$V_T > v_{GS} - v_{DS}$$

$$V_T > v_{GD}$$

$$V_{GD} = 0 \quad \Rightarrow V_{GD} < V_t$$

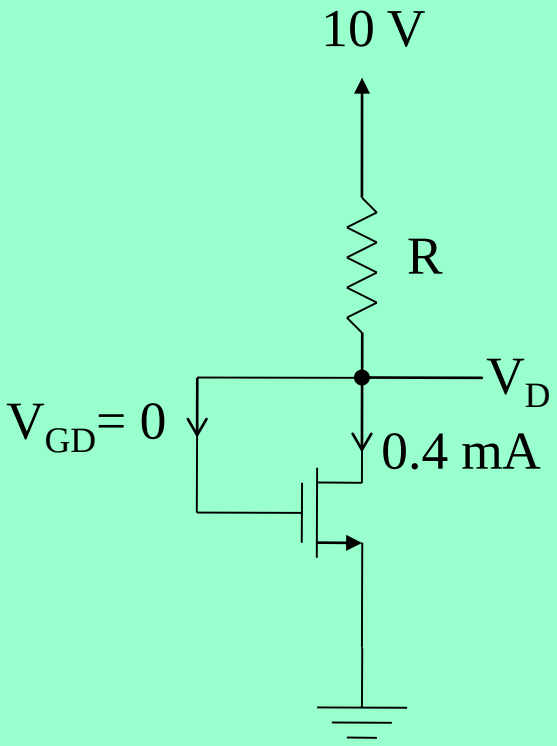
$I_D = 0.4$ mA, $V_t = 2$ V, $\mu_n C_{0x} = 20\ \mu A/V^2$ L = 10 µm and W = 100 µm.

$$I_D = \frac{1}{2}\mu_0 C_{0x}\frac{W}{L}(V_{GS} - V_t)^2$$

$$0.4\,\text{mA} = \frac{1}{2}20\times10^{-6}\cdot\frac{100}{10}(V_{GS} - 2)^2$$

$$(V_{GS} - 2)^2 = 4 \quad \Rightarrow \quad V_{GS} - 2 = \pm 2$$

$V_{GS} = 0$ or **4 V**



$$\Rightarrow V_{GD} < V_t$$

$$v_{GS} > V_T$$

MOSFET is in saturation

$V_{GS} =$ **4 V**

$$\Rightarrow V_D = 4\ \text{V}$$

$$R = \frac{10 - V_D}{0.4\,\text{mA}} = \frac{10-4}{0.4\,\text{mA}} = 15\,\text{K}\Omega$$