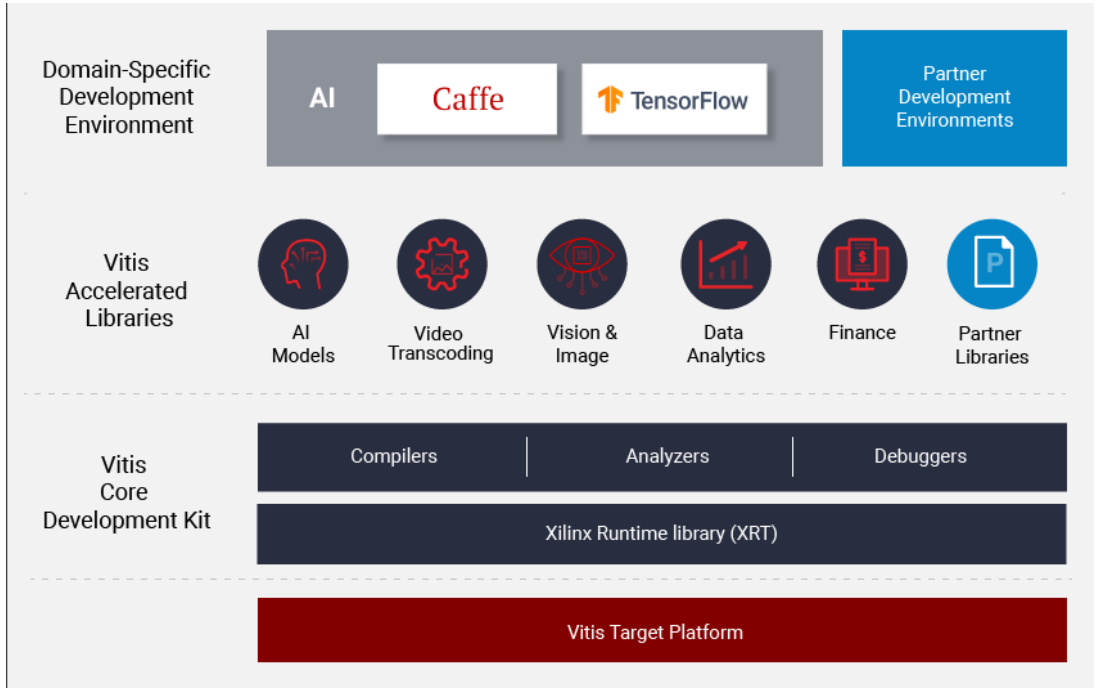
Getting to grips with Vitis

Adam Taylor

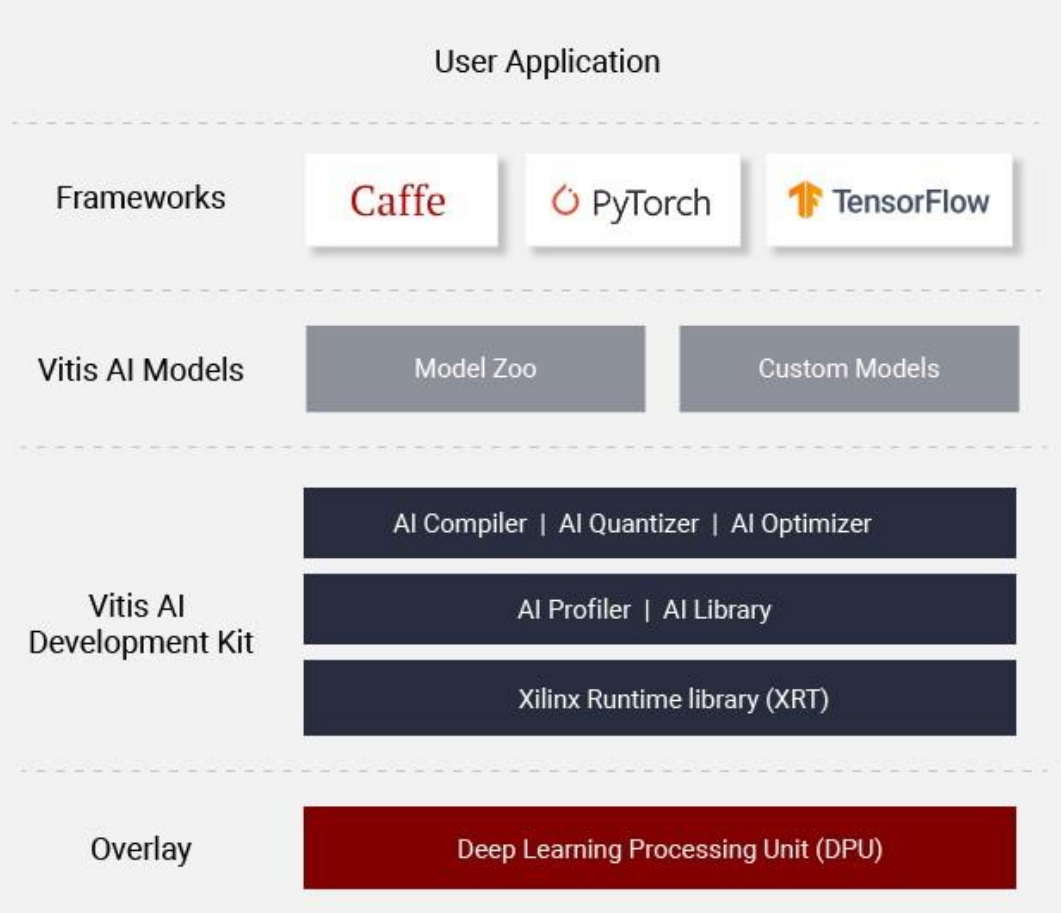
What is Vitis

- Vitis is unified software development environment from Xilinx
- Offers Unified edge and cloud development methodologies
- Support embedded and accelerated flows



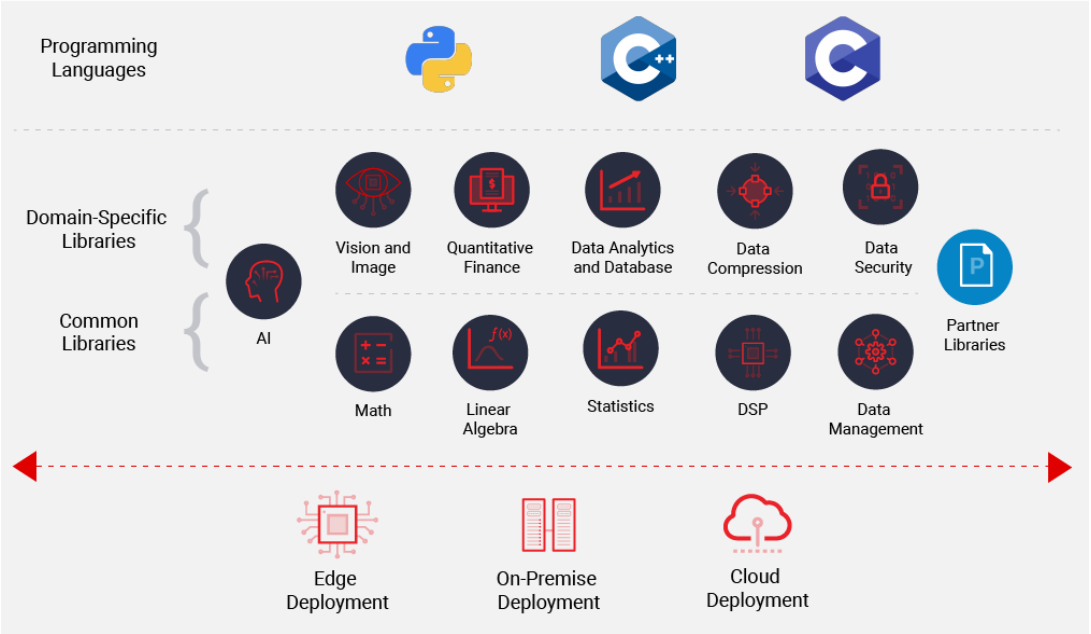
Vitis AI Development Environment

- Vitis AI enables acceleration of AI inference at edge & Cloud
- Supports leading frameworks such as TensorFlow, Caffe and Pytorch
- Works with fixed point representation and Xilinx Deep Learning Processor Unit



Vitis Accelerated Libraries

- Several Open Source acceleration ready libraries
- Common Libraries – offer a set of common functionality
- Domain specific libraries – offer out of the box functions for specific domains e.g. vision

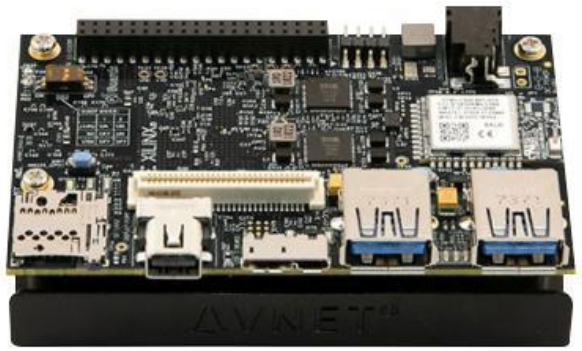


Vitis Core Development Kit

- GUI & Command line tools for compilation, debug and analysis of C, C++ and OpenCL designs.
- Can use preferred GUI or integrated GUI
- Supports embedded and accelerated flows

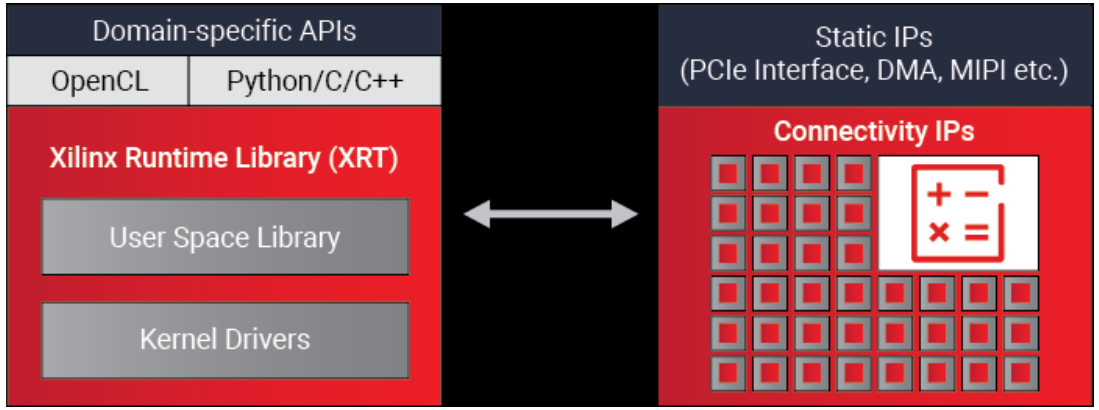
Vitis Target Platforms

- Embedded
  - SoC – MPSoC, RFSoC, Zynq
  - FPGA – MicroBlaze
- Cloud – Alveo / AWS F1 Instance
- Embedded SoC and Cloud applications can use acceleration flow.
- All required files and boot elements are generated



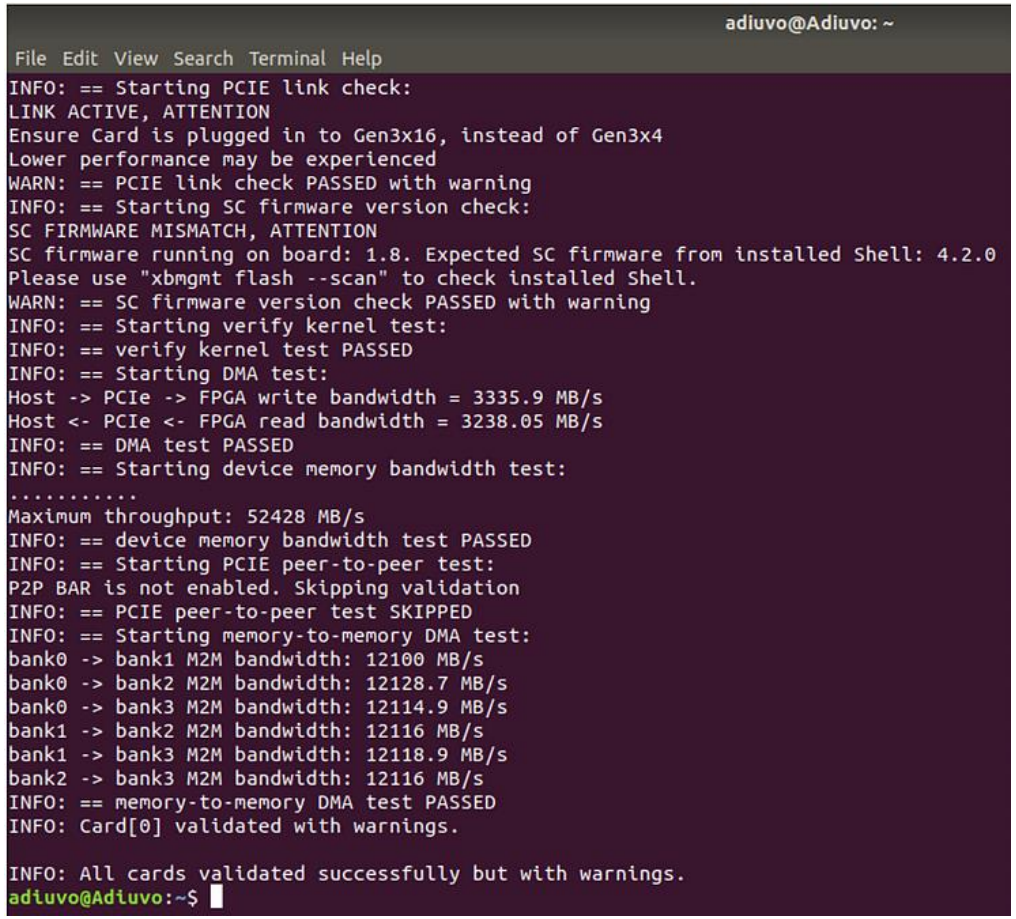
Xilinx Runtime library

- Xilinx Runtime library (XRT) enables communication between the host and accelerator
- Cloud based – Host x86
- Embedded – Arm A9 or A53
- Provides all libraries, APIs, drivers and utilities.



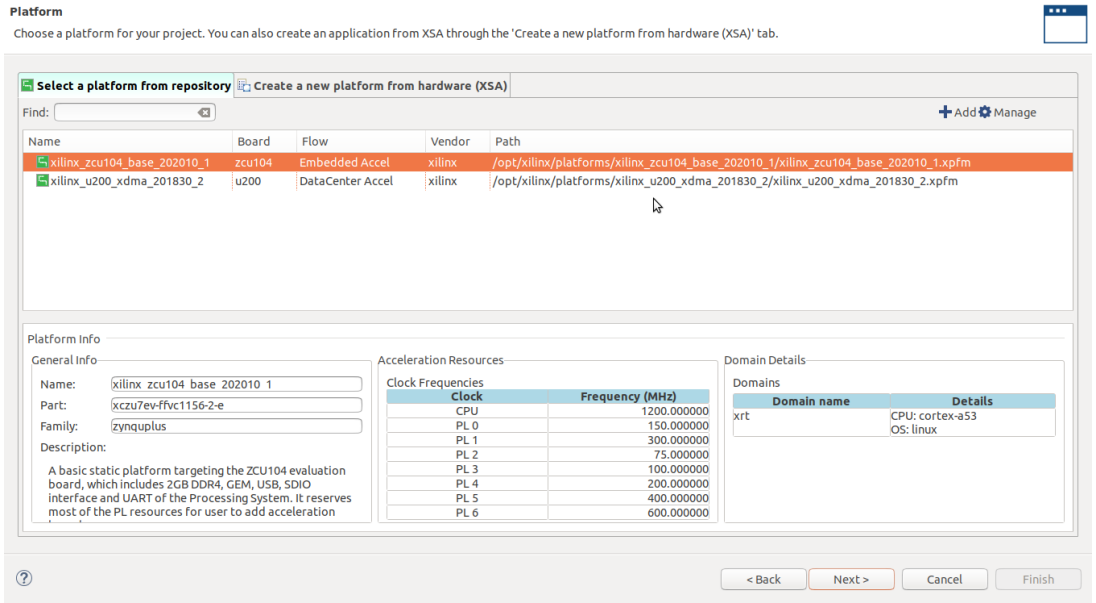
Xilinx Runtime library

- Key Functions of the Runtime include
- Downloading the FPGA binary
- Memory Management between Host and Accelerator
- Execution Management
- Board Management



Element of Vitis

- All projects required a platform
  - Hardware element – makes available AXI connections, clocks and Interrupts in the PL to Vitis Compiler
  - Software element – provides boot, XRT and QEMU support
  - Linux element – FS, Image and SysRoot



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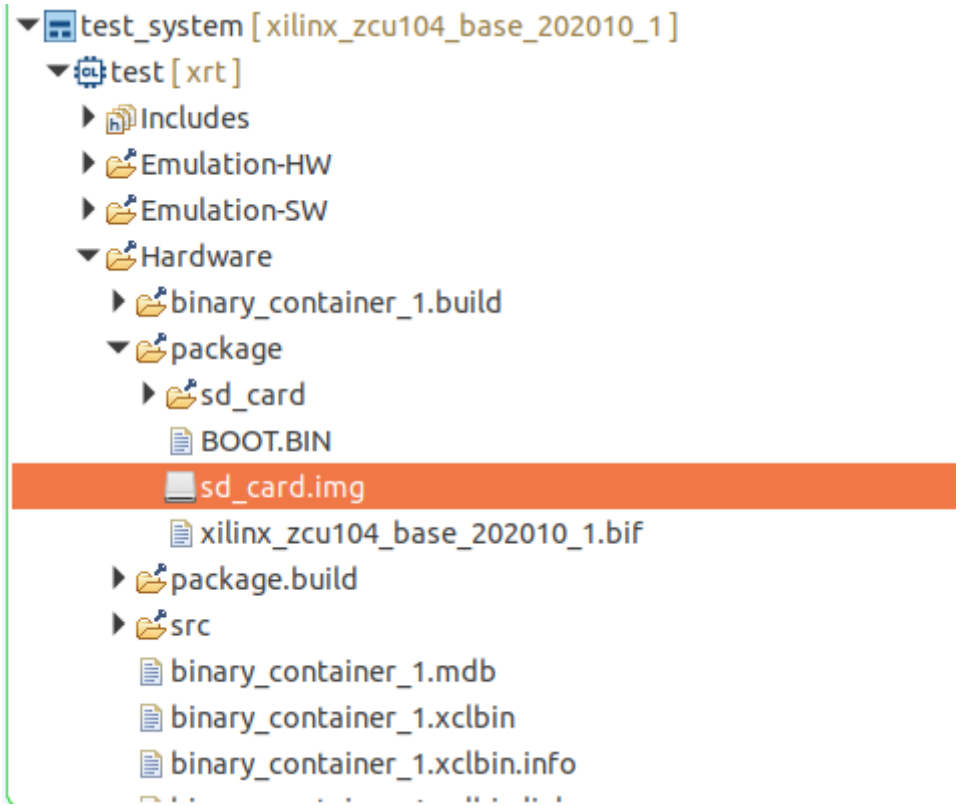
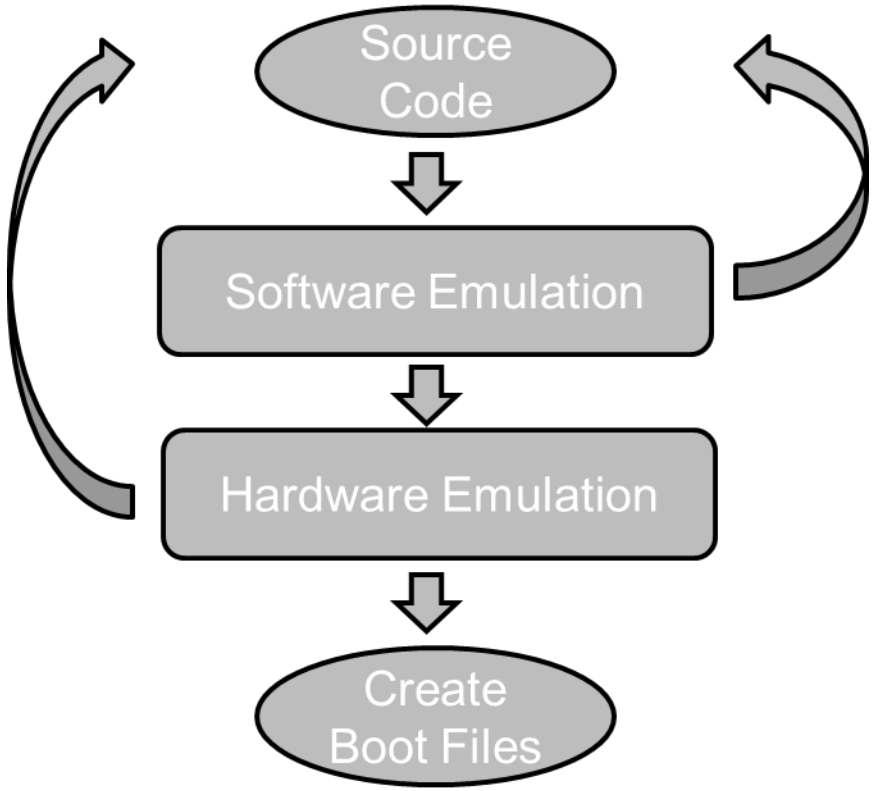
Vitis Output

- Compiled binary (host) and XCLbin (accelerator)
- Embedded System Output
  - SD Card Image
    - Image
    - File System
    - Binary and XCLBin
- Cloud output
  - Binary and XCLBin



Vitis Development Flow

- Software Emulation – Syntax errors & algorithm verification
- Hardware Emulation – Optimize Performance, Interfacing & Resources



OpenCL Framework

An open industry standard
- For parallel computing
- Of heterogeneous systems

Enables cross-platform functional portability
- No code changes
- Portable across CPU, GPU, FPGA, DSP, etc.
  - Can run on cell phones, laptops, super computers
- Important: No performance portability

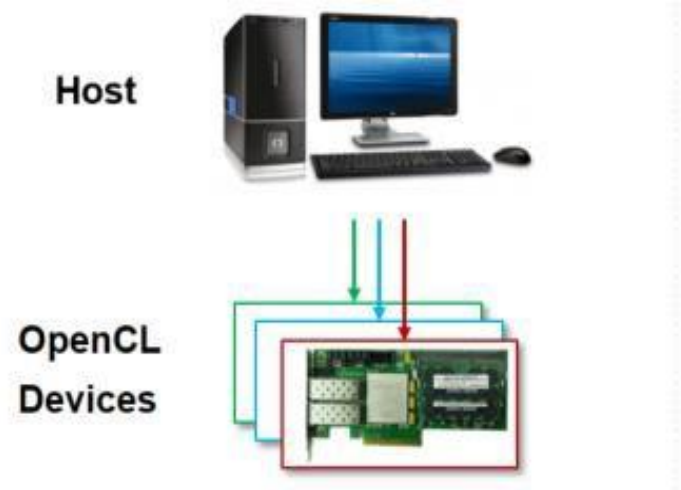
OpenCL

Khronos Group

www.khronos.org

Wide market adoption
- Support implemented by
  - Apple, AMD, Xilinx, Intel, ARM, Nvidia, Qualcomm, etc.
- Many companies developing applications
  - Image, video, audio processing, scientific calculations, medical imaging, and more

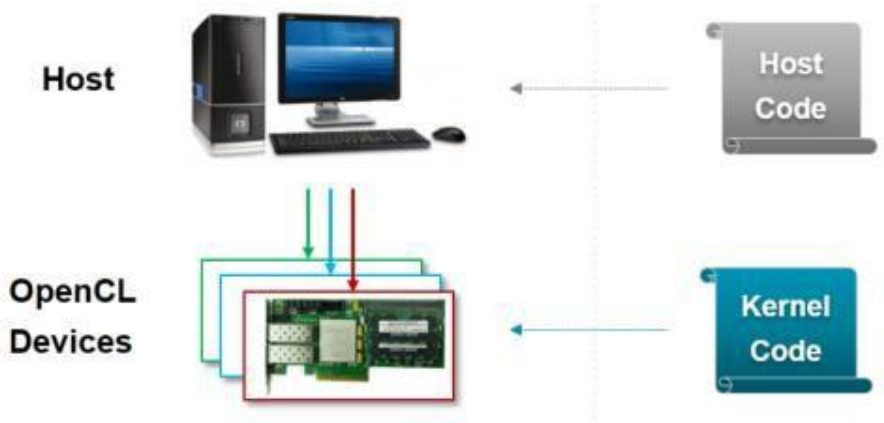
OpenCL Framework



Platform model

- –Defines representation of ANY platform
- –Contains
  - Single host
  - One or more OpenCL devices (compute device)

OpenCL Framework



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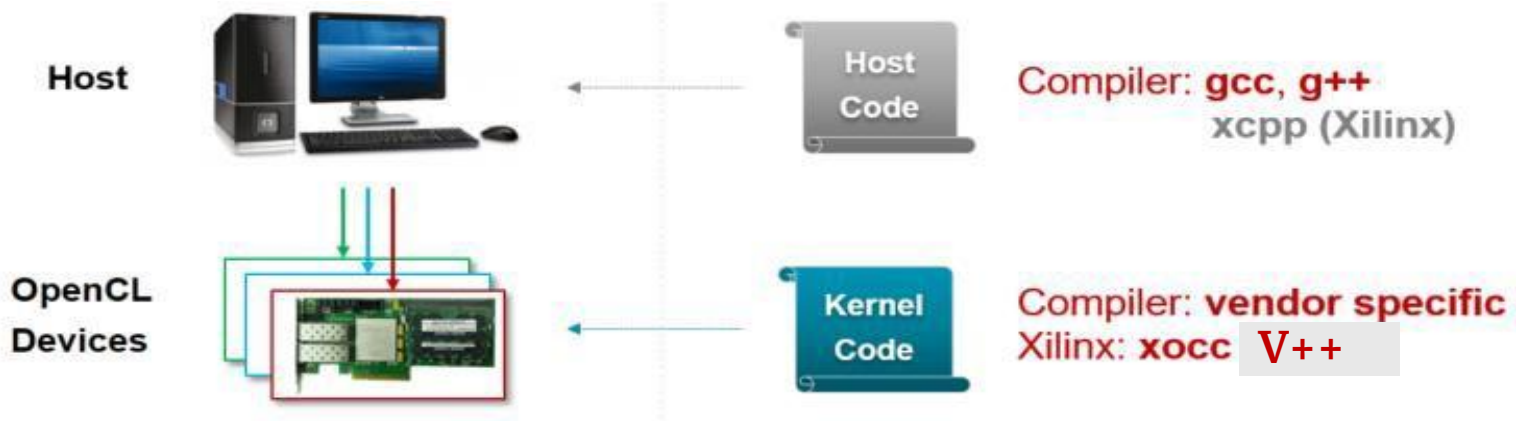
Execution model

OpenCL application: Two parts

- Host program
  - Manages the entire application: OpenCL APIs
- Kernels (OpenCL C language)
  - Functions to accelerate, run on OpenCL devices

OpenCL Framework



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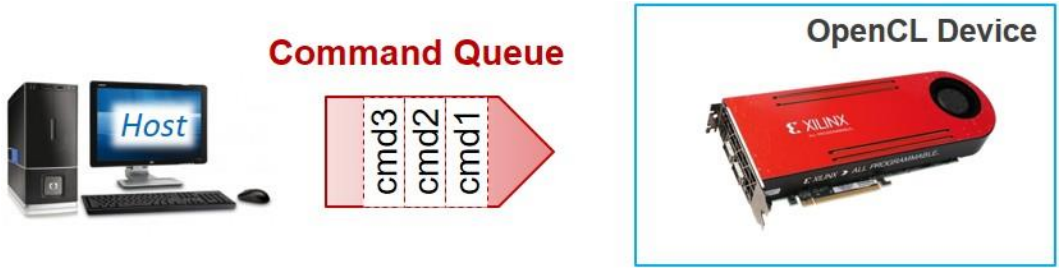
Execution Model – Command Queues

Interaction between host and device occurs via command queues

- Created by host
- Attached to a single device
  - **Note:** Multiple command queues can be active within context



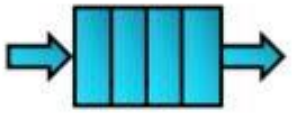
Three command types

- Kernel execution commands
- Memory commands
  - Transfer data between host and different memory objects
- Synchronization commands
  - Put constraints on in the order in which commands are executed

Memory Model

Three types of memory objects

- Buffer objects
  - Contiguous block of memory
  - Available to kernels for read/write
  - Programmer can write data to buffers
  - Access to data via pointers
- Image objects (not a part of embedded profile)
  - Hold images only
  - Storage/format can be optimized for specific OpenCL device
  - OpenCL framework provides functions to manipulate images
- Pipes
  - Data organized as FIFO
  - Accessed (read/write) via built in
  - Pipe not accessible from the host



Five Sub-regions of Memory Objects

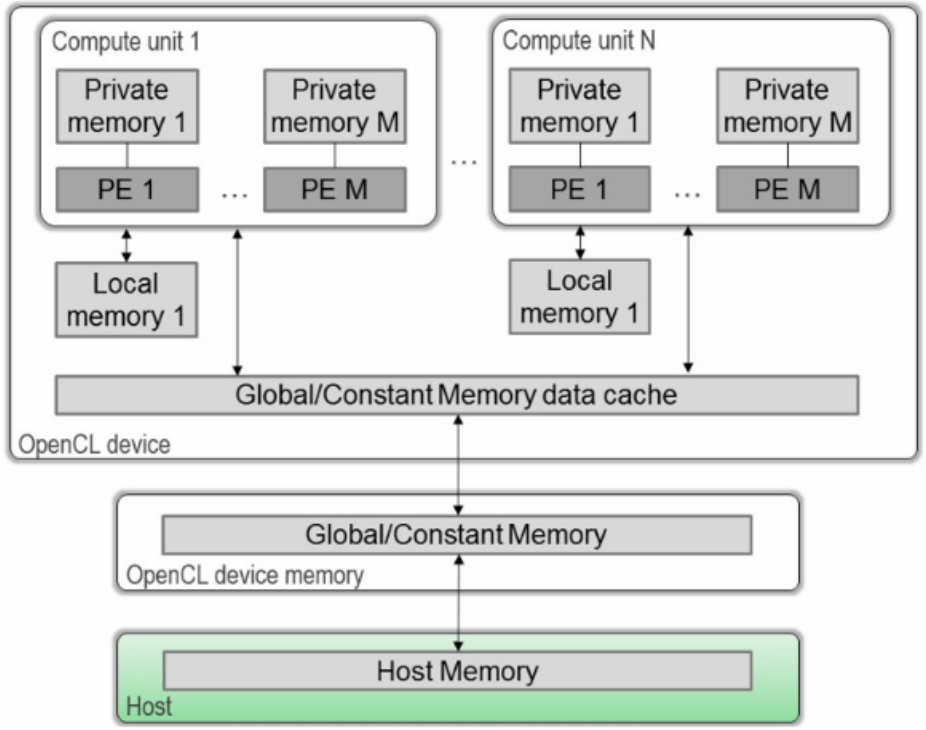
Host memory
- Visible to host only
- OpenCL framework only defines how host memory interacts with OpenCL objects

Global memory
- Visible to host and device
- All work items in all workgroups can read/write there
- Global on-chip memory – visible to device only

Constant memory
- Region of global memory
- Work items – read access only

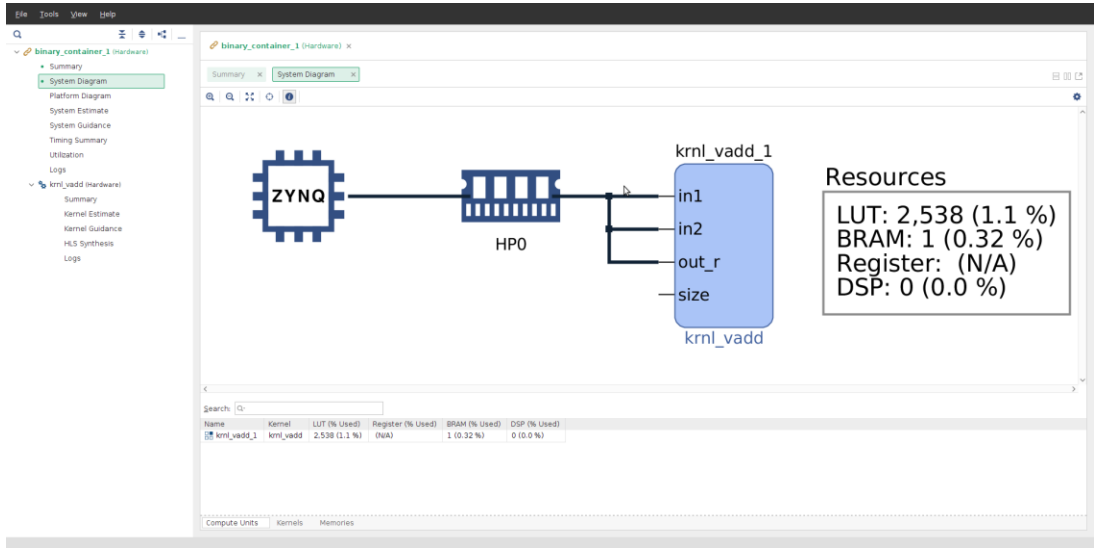
Local memory
- Local to workgroup (shared by all work-items in a group)

Private memory
- Accessible by a work-item



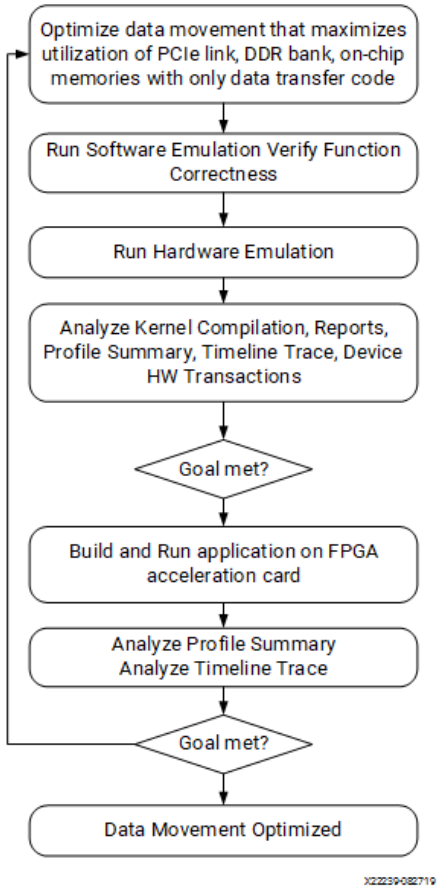
Optimization

- Optimization Possible at both Host and Kernel
- Enables most responsive solution
- Host optimization
- Kernel optimization possible in OpenCL and C/C++
  - Optimization Syntax differs



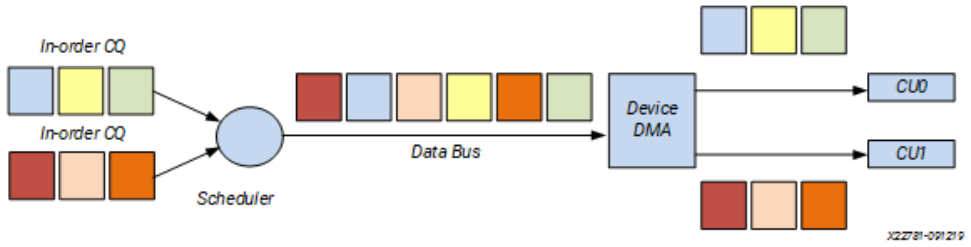
Host Optimization

- Optimize the data movement in the application before optimizing computation
- Compute Unit Scheduling
  - Multiple In-Order Command Queues
  - Single Out-of-Order Command Queue

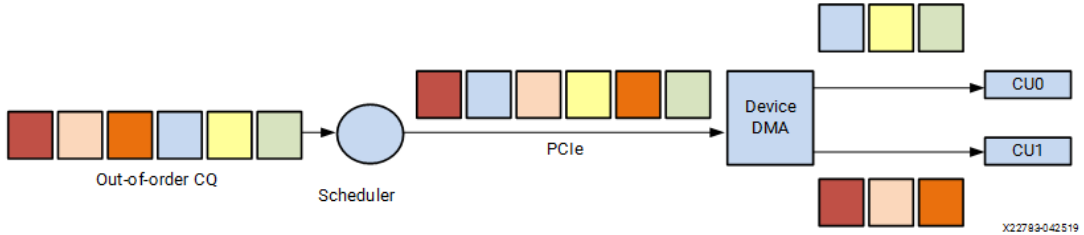


Host Optimization

- Multiple In-Order Command Queues

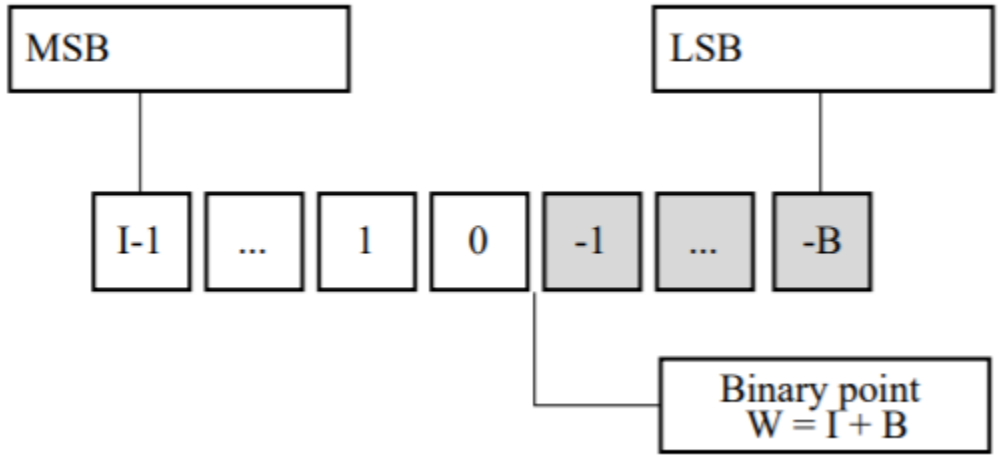


- Single Out-of-Order Command Queue



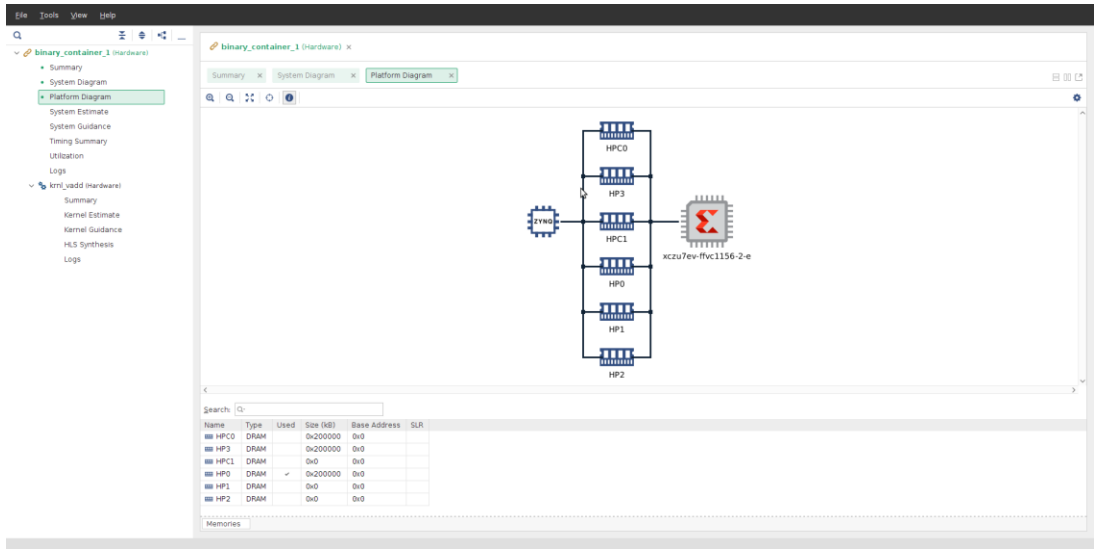
Kernel Optimization – Data Types

- Avoid native C data types e.g. int, float, double
- Best performance is using bit accurate types (C/C++ Kernels)
  - Arbitrary Precision Integer
  - Arbitrary Precision fixed point
- Enables smaller & faster logic implementations



Kernel Optimization – Interfacing

- Two types of data transfer
  - Data Pointers via global memory (M_AXI)
  - Scalar direct to kernel (AXI_LITE)
- Vitis automatically selects interface type
- Max data width is 512 bits – maximum performance leverages this



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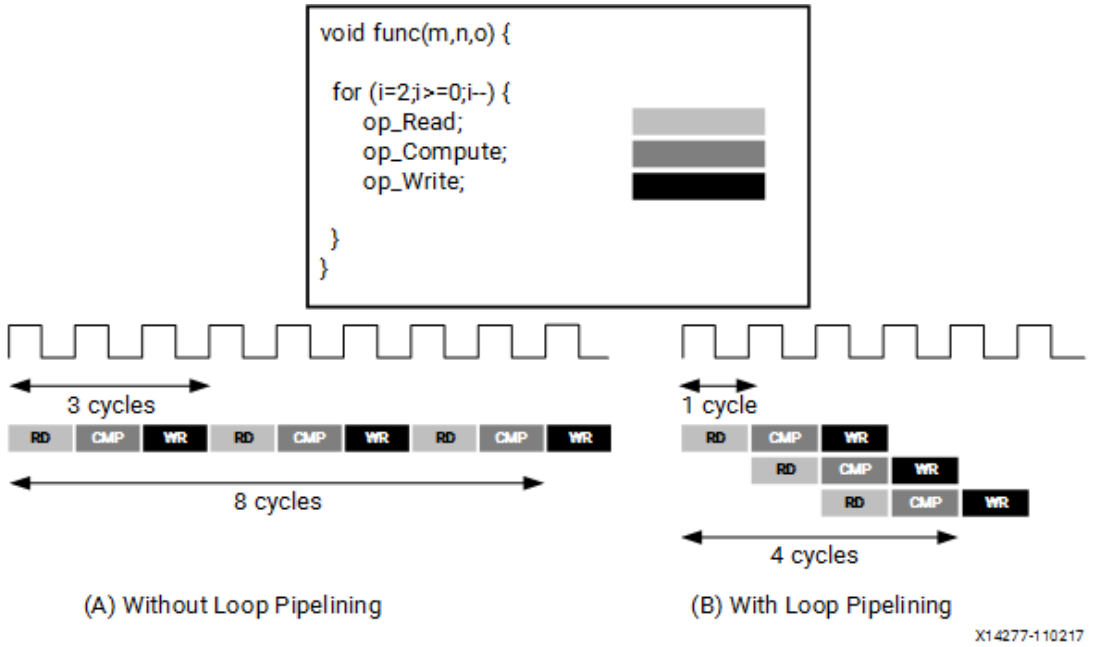
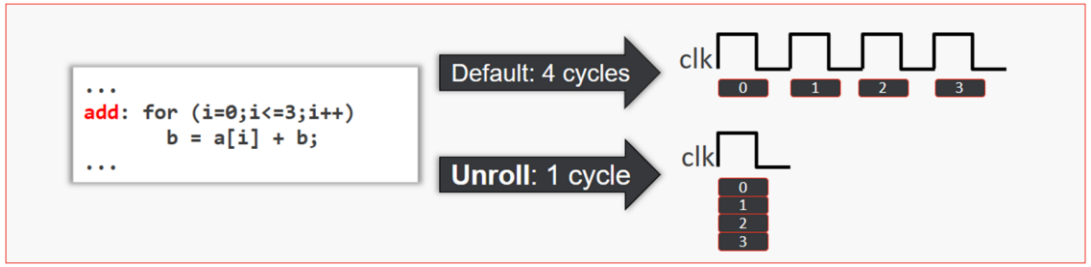
Kernel Optimization – Pipelining

- By default, every iteration of a loop only starts when the previous iteration has finished
- Pipelining the loop executes subsequent iterations in a pipelined manner



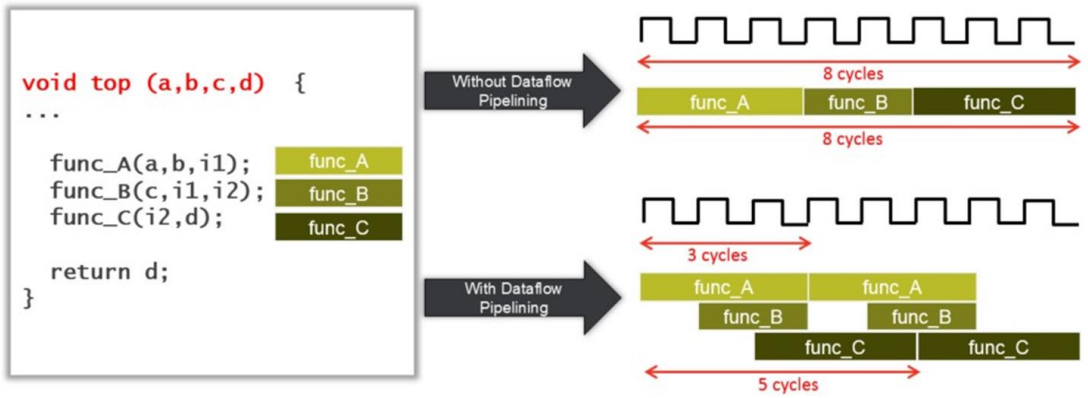
Kernel Optimization – Unrolling

- Unrolling a loop enables the full parallelism
- Full or Partial Unroll
- Data dependencies in loops can impact the results of loop pipelining or unrolling



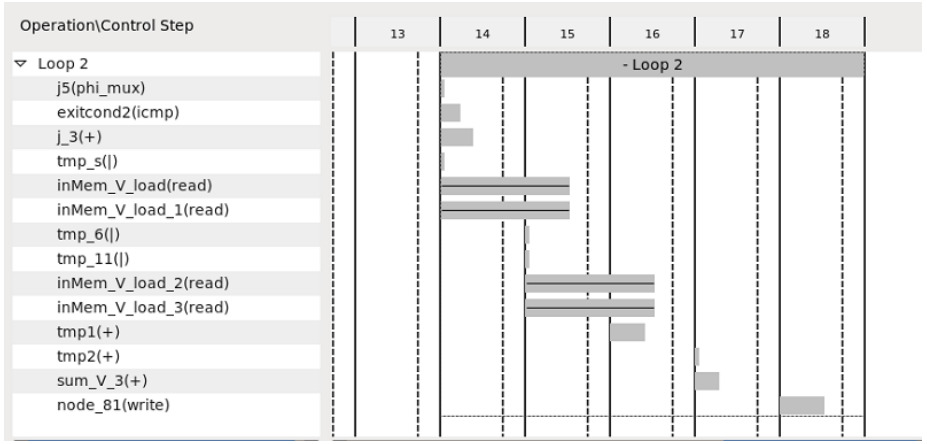
Kernel Optimization – DataFlow

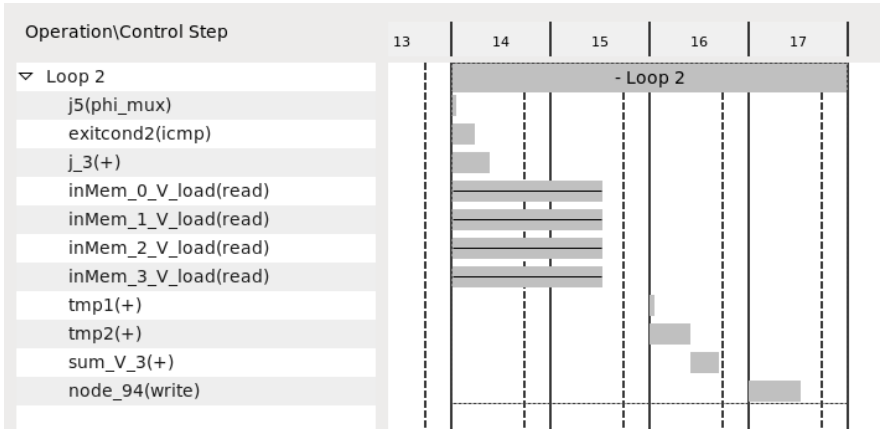
- Improve kernel performance by enabling task-level pipelining
- Be careful of
- Single producer-consumer violations.
  - Bypassing tasks.
  - Feedback between tasks.
  - Conditional execution of tasks.
  - Loops with multiple exit conditions or conditions defined within the loop



Kernel Optimization – Memory

- Limited BRAM access bandwidth, can heavily impact the overall performance
- Ability to partition and reshape arrays can increase bandwidth
- Partition – Separates into different BRAMS
- Reshape – allows combination of words



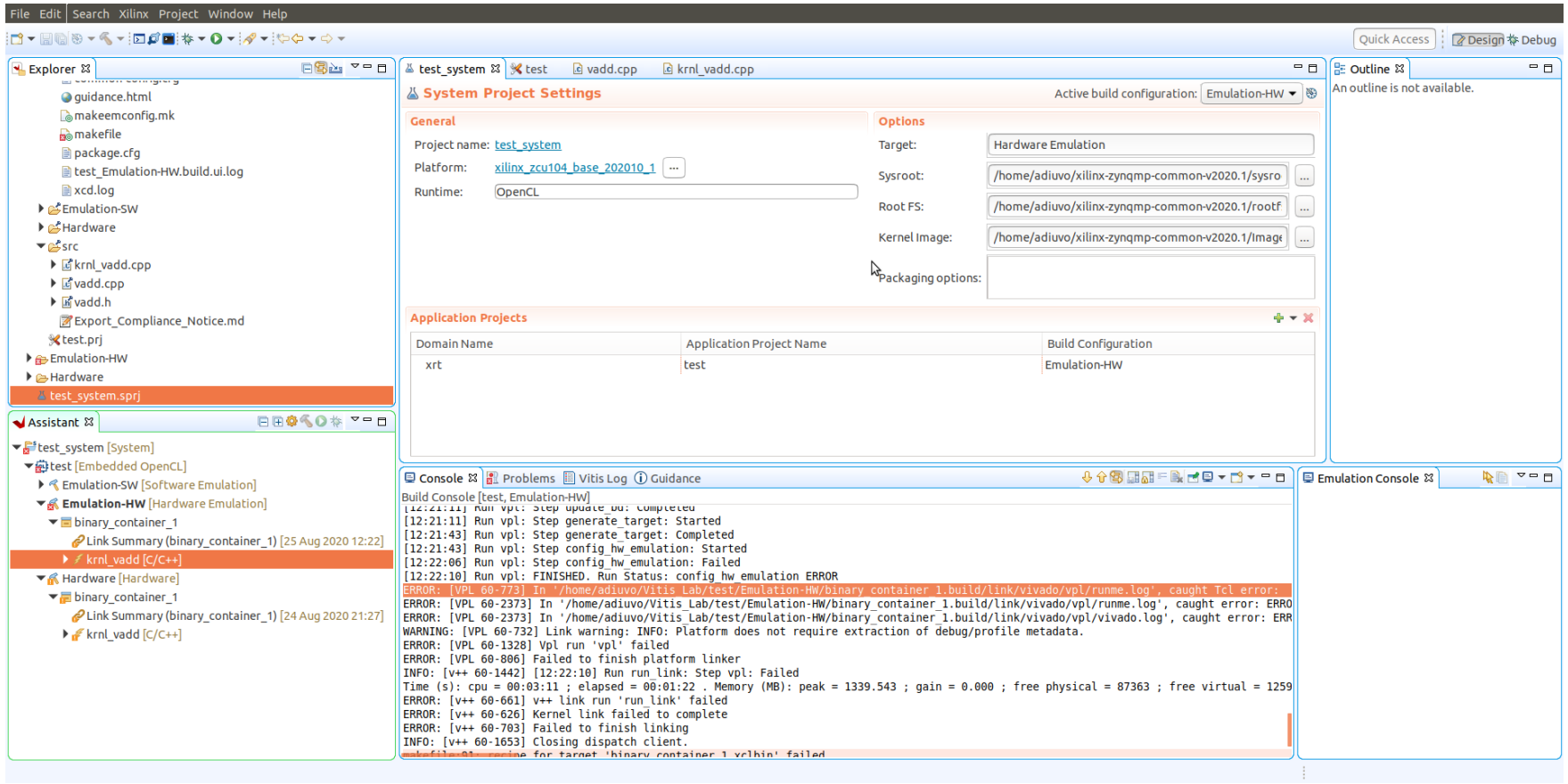


Kernel Optimization - Pragmas

Optimization	C/C++	OpenCL
Pipeline	#pragma HLS PIPELINE	___attribute___((xcl_pipeline_loop))
Unroll	#pragma HLS UNROLL	___attribute___((opencl_unroll_hint))
DataFlow	#pragma HLS DATAFLOW	___attribute___ ((xcl_dataflow))
Memory	#pragma HLS ARRAY_PARTITION	

Further information can be found at
https://www.xilinx.com/html_docs/xilinx2020_1/vitis_doc/optimizingperformance.html#fhe1553474153030

Vitis GUI – Project Settings



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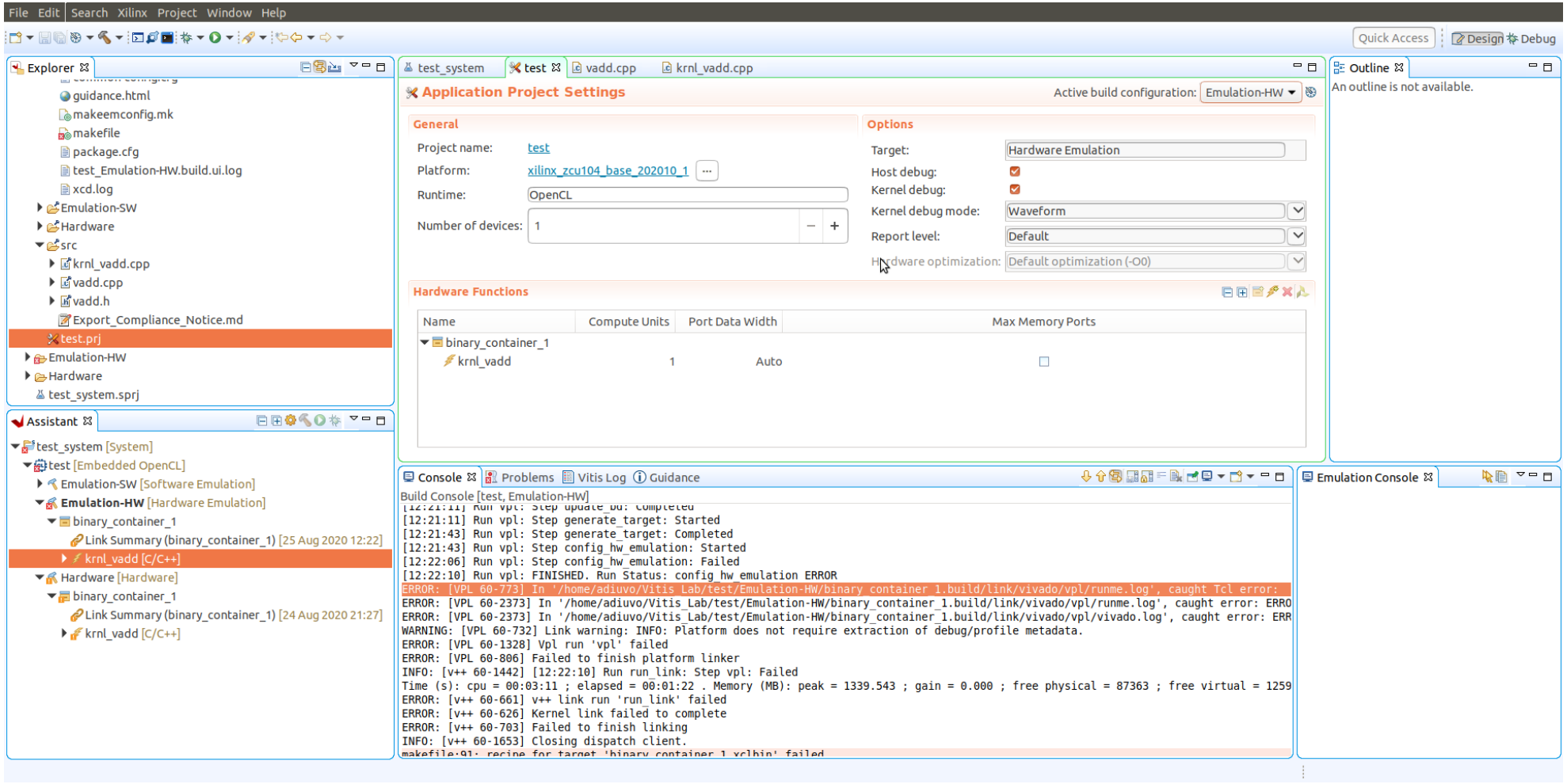

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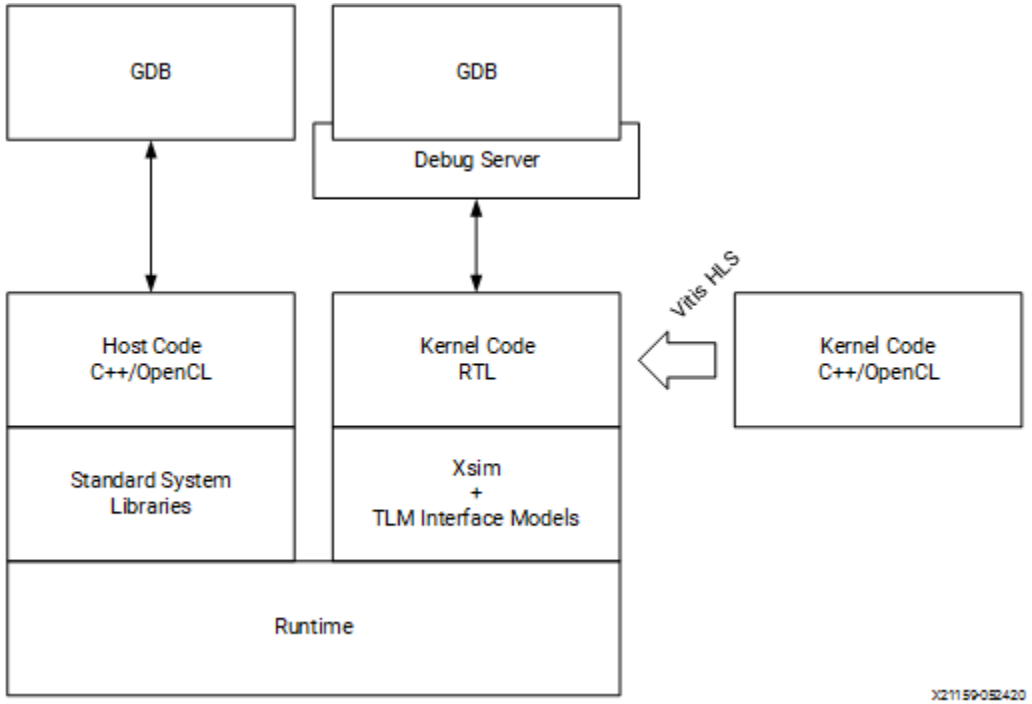
Vitis-Debug

- Can Debug
  - Software Emulation
  - Hardware Emulation
- Hardware flow insert ILA
- Debugging will use QEMU and Logic Simulator



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