

Building Accelerated Applications with Vitis

Course Workbook

Table of Contents

About this Workbook	Page 3
Pre-Lab: Workshop Pre-requisites	Page 4
Lab 1: Understanding Vitis Project creation & Flow	Page 7
Lab 2: Instantiating Xilinx Deep Learning Processor	Page 48

About this Workbook

This workbook is designed to be used in conjunction with the Building Accelerated Applications with Vitis course.

The contents of this workbook are created by Adiuvo Engineering & Training, Ltd.

If you have any questions about the contents, or need assistance, please contact Adam Taylor at adam@adiuvoengineering.com.

Pre-Lab

Workshop Pre-requisites

Required Hardware

There is no required hardware for this course.

Downloads and Installations

Step 1 – Download and install the following at least 1 day prior to the workshop. This may take a significant amount of time and drive space.

Watch the video available [here](#) to show how to configure the installation

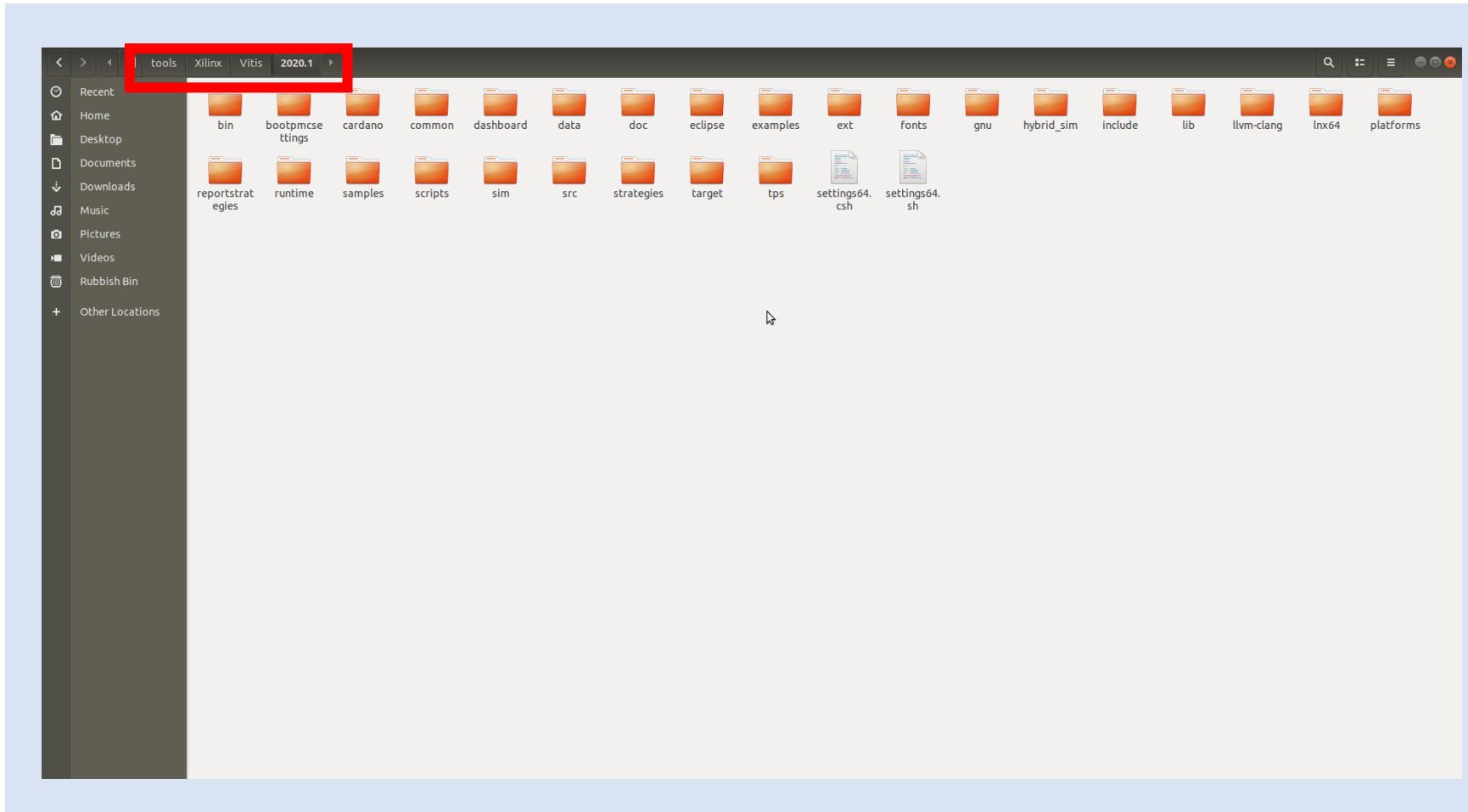
Vitis 2020.1	Download
XRT	Download
Embedded Platforms	Download
Common Images for Embedded Platforms	Download

Lab 1

Understanding Vitis Project creation & Flow

Lab 1: Understanding Vitis Project creation & Flow

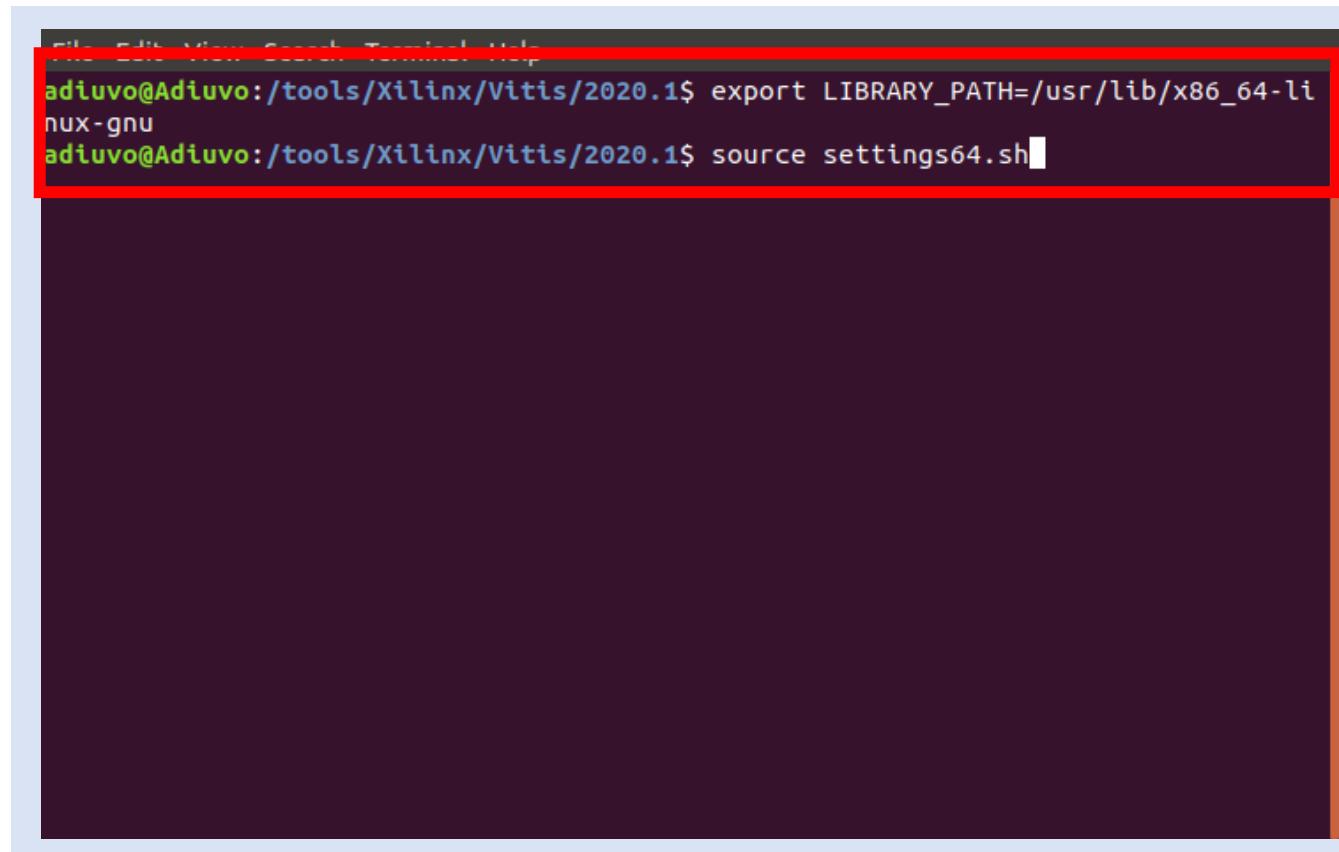
Step 1 – Open a file browser and navigate to /tools/Xilinx/Vitis/2020.1



Lab 1: Understanding Vitis Project creation & Flow

Step 2 – Open a terminal window, set the path of the LIBRARY_PATH and source the settings64.sh

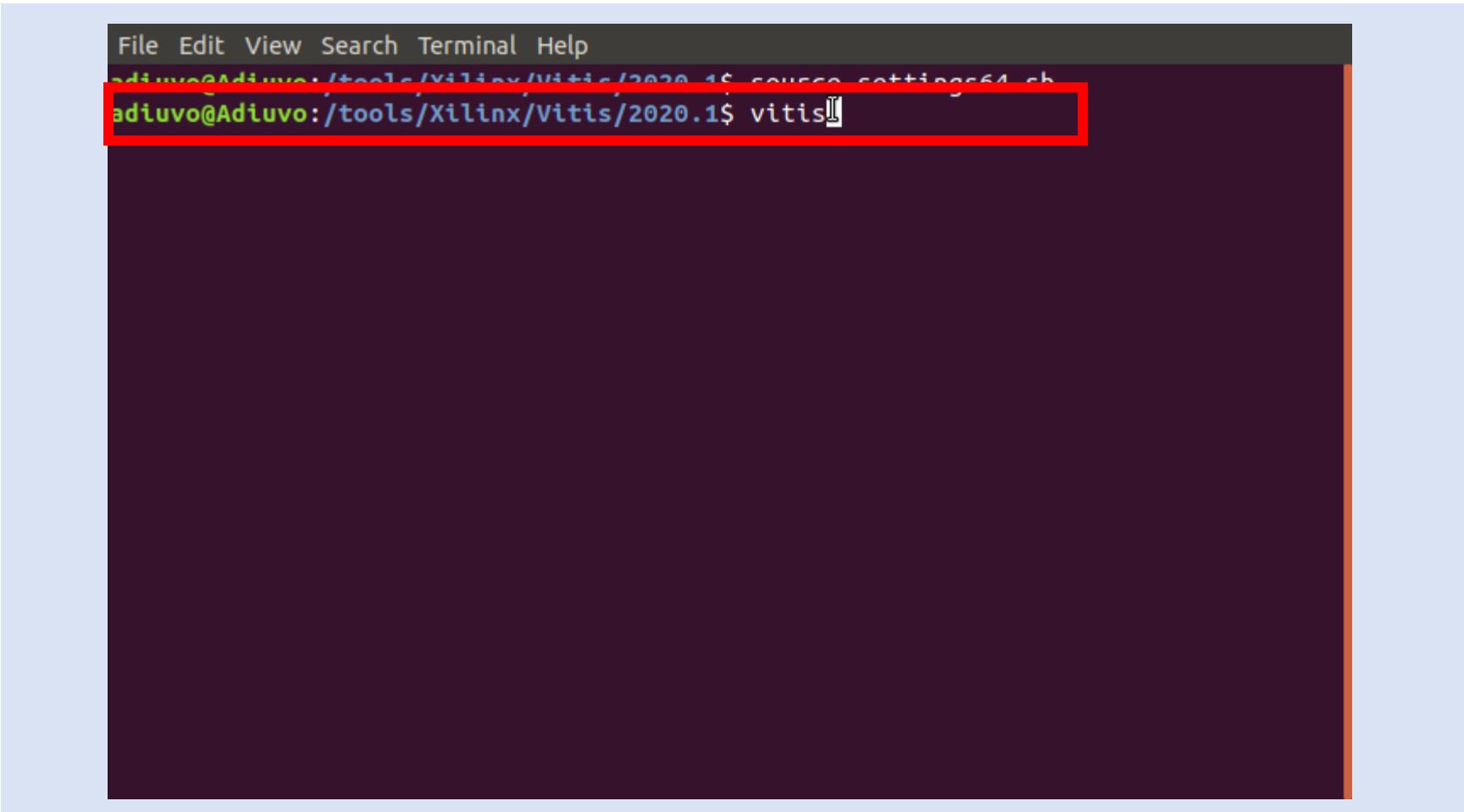
```
export LIBRARY_PATH=/usr/lib/x86_64-linux-gnu
```



The screenshot shows a terminal window with a dark background and light-colored text. At the top, there is a menu bar with options like File, Edit, View, Search, Terminal, Help. Below the menu, the terminal prompt is shown as `adiuvo@Adiuv0:/tools/Xilinx/Vitis/2020.1$`. The user has entered two commands: `export LIBRARY_PATH=/usr/lib/x86_64-linux-gnu` and `source settings64.sh`. The entire command block is highlighted with a thick red border.

Lab 1: Understanding Vitis Project creation & Flow

Step 3 – Start Vitis from the command prompt by typing “vitis”

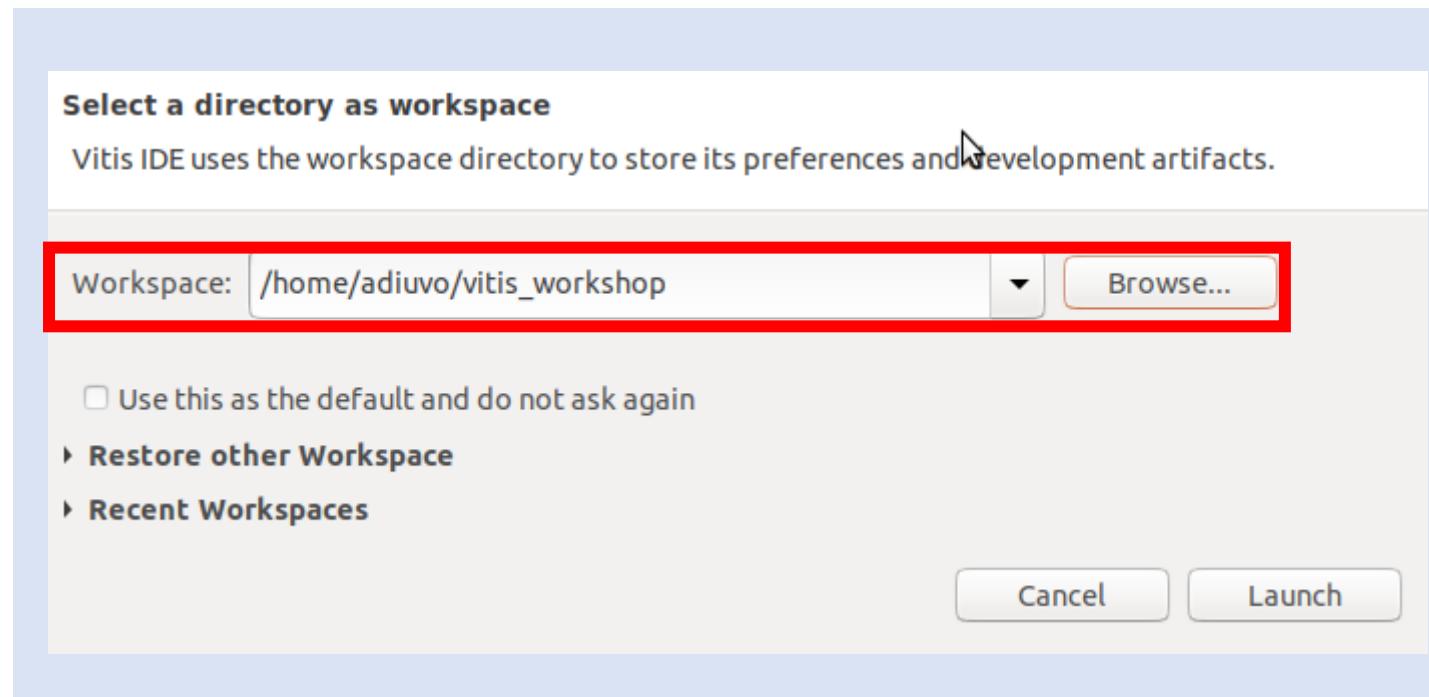


A screenshot of a terminal window titled "File Edit View Search Terminal Help". The window shows a command-line interface with a red box highlighting the command "vitis" as it is being typed. The path "/tools/Xilinx/Vitis/2020.1\$" is visible above the command.

```
File Edit View Search Terminal Help
adiuvo@Adiuvo:/tools/Xilinx/Vitis/2020.1$ source settings64.sh
adiuvo@Adiuvo:/tools/Xilinx/Vitis/2020.1$ vitis
```

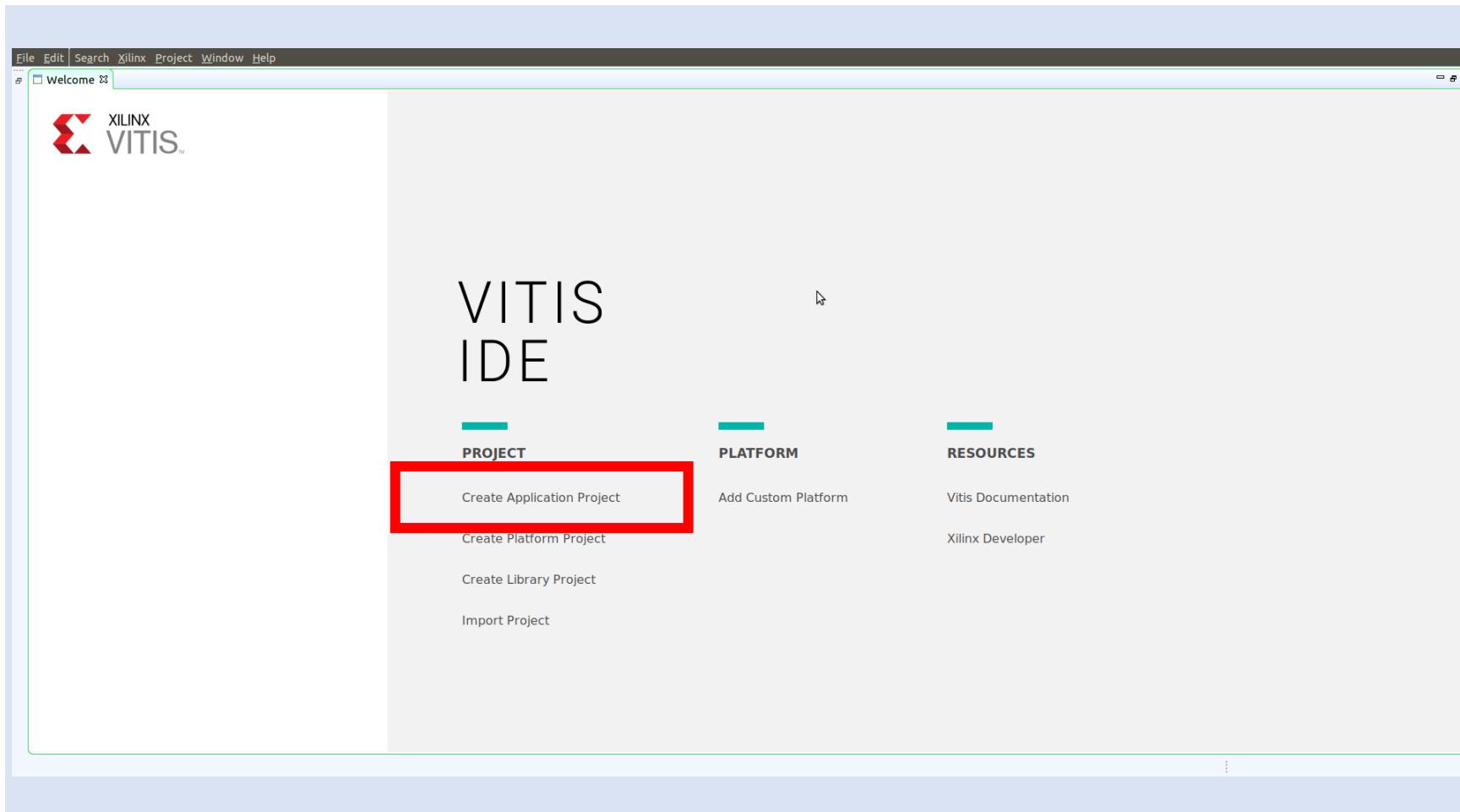
Lab 1: Understanding Vitis Project creation & Flow

Step 3 – Select the directory you which to use as your workspace, click launch



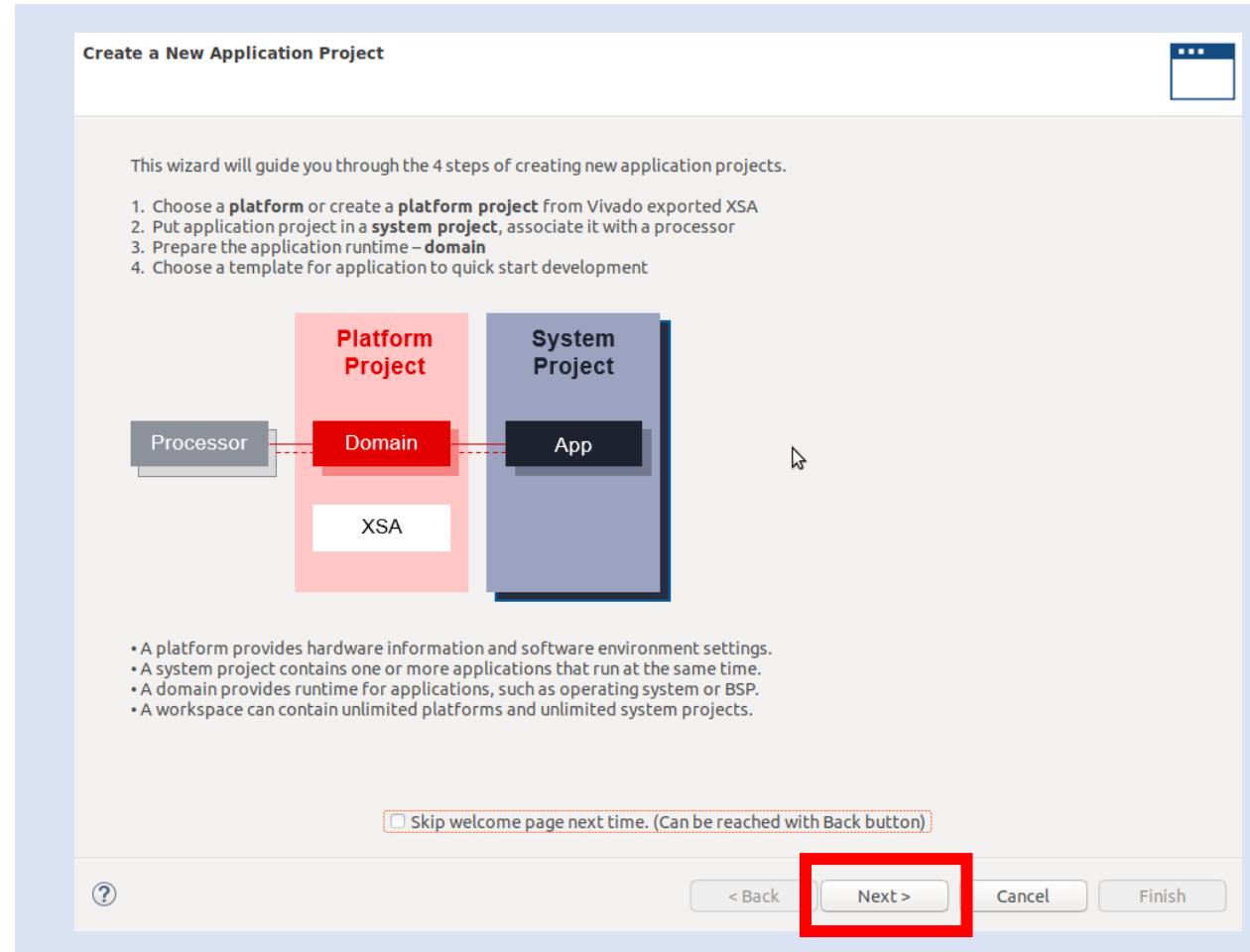
Lab 1: Understanding Vitis Project creation & Flow

Step 4 – When the IDE launches, select “Create Application Project”



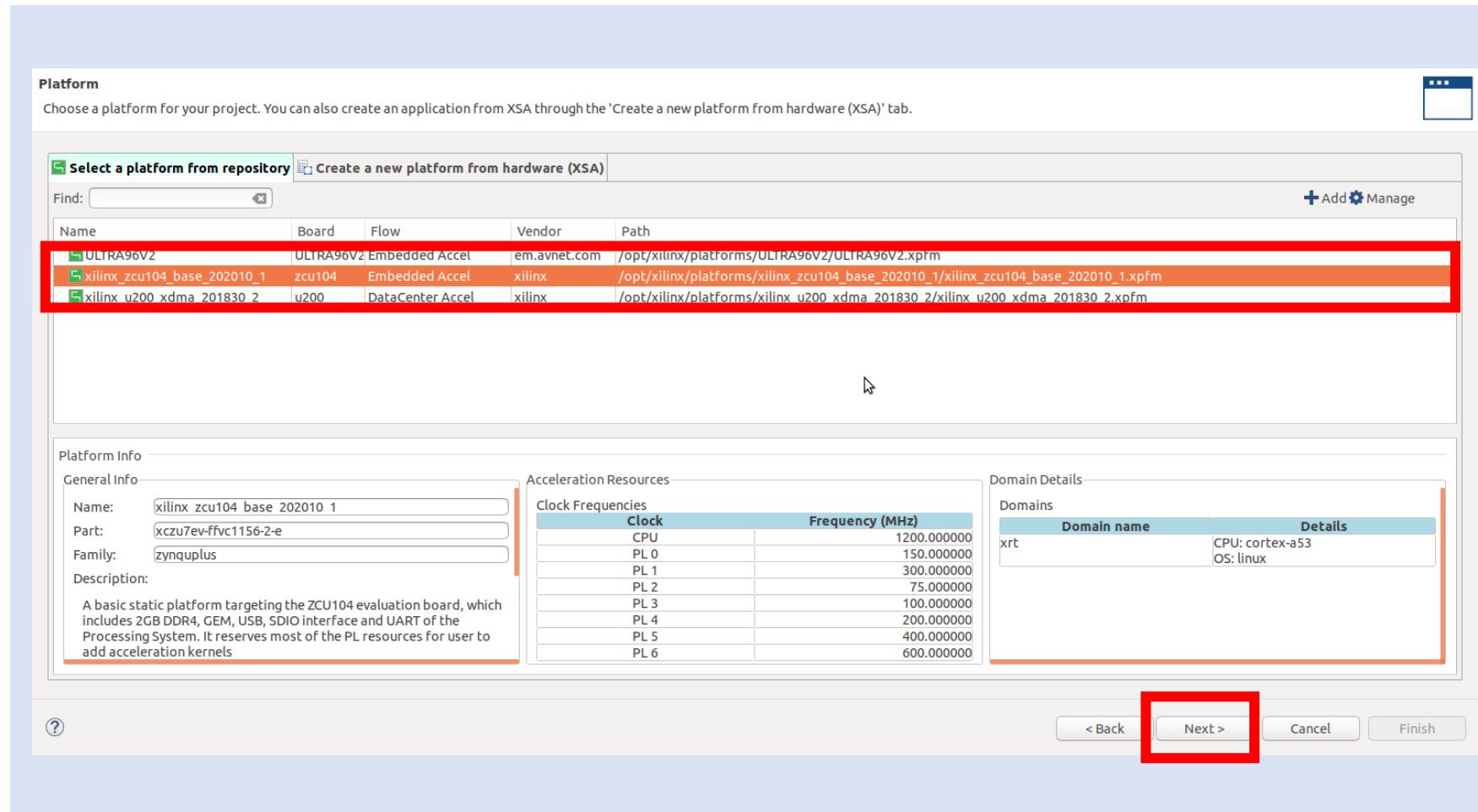
Lab 1: Understanding Vitis Project creation & Flow

Step 5 – This will launch the project creation wizard, click next on the first dialog



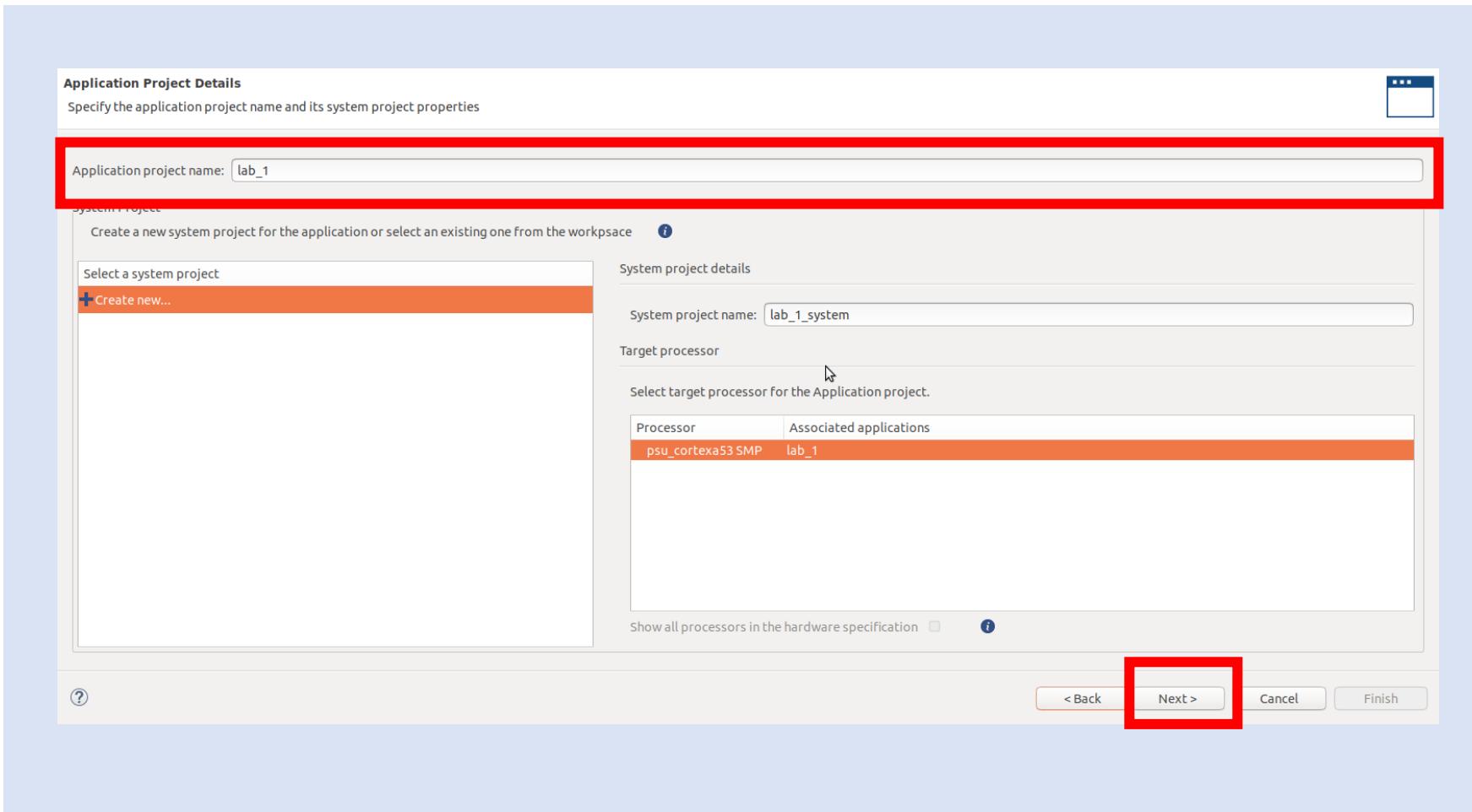
Lab 1: Understanding Vitis Project creation & Flow

Step 6 – You should see the platforms you installed; I will select ZCU104, click next



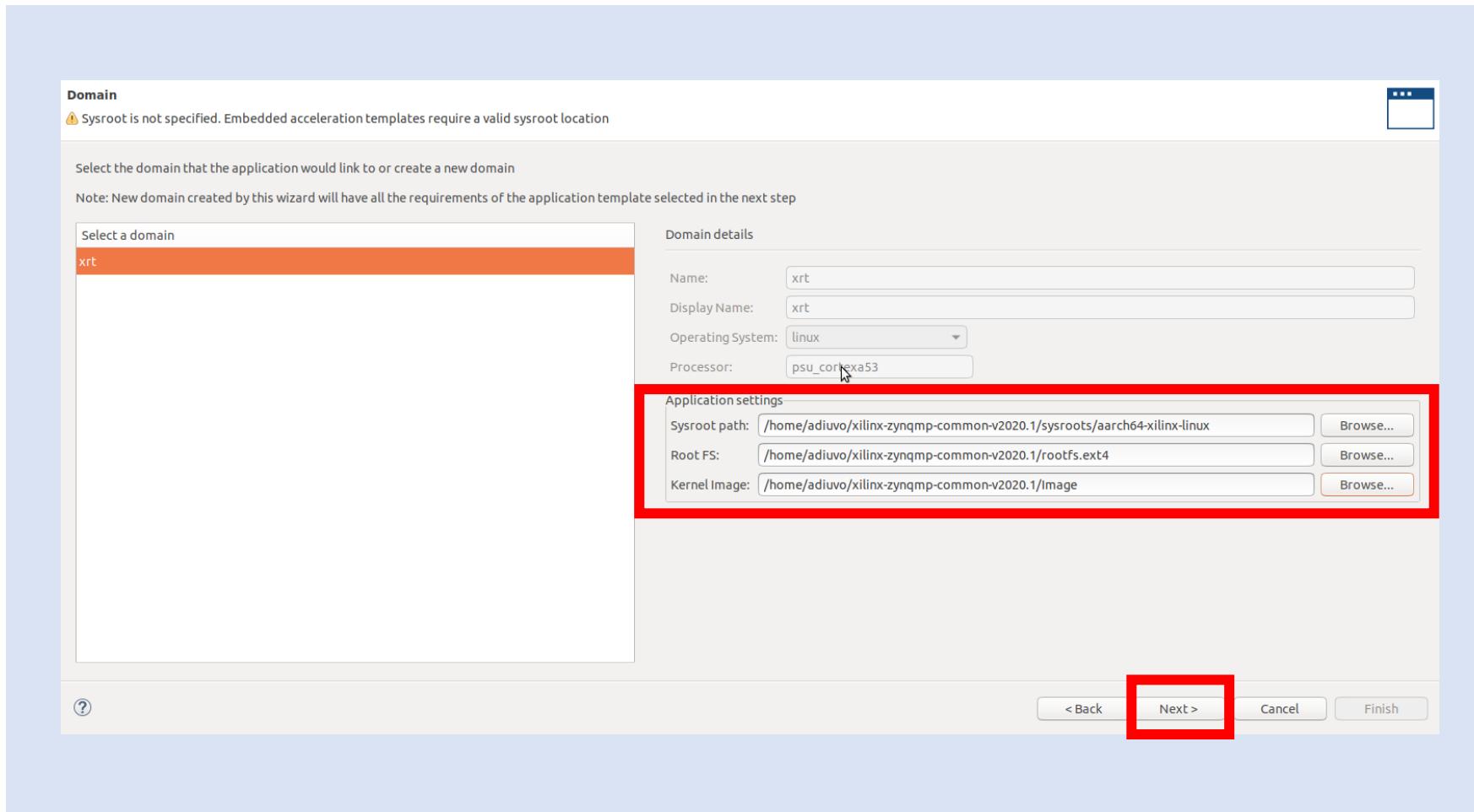
Lab 1: Understanding Vitis Project creation & Flow

Step 7 – Enter the name lab_1 for the project name and click next



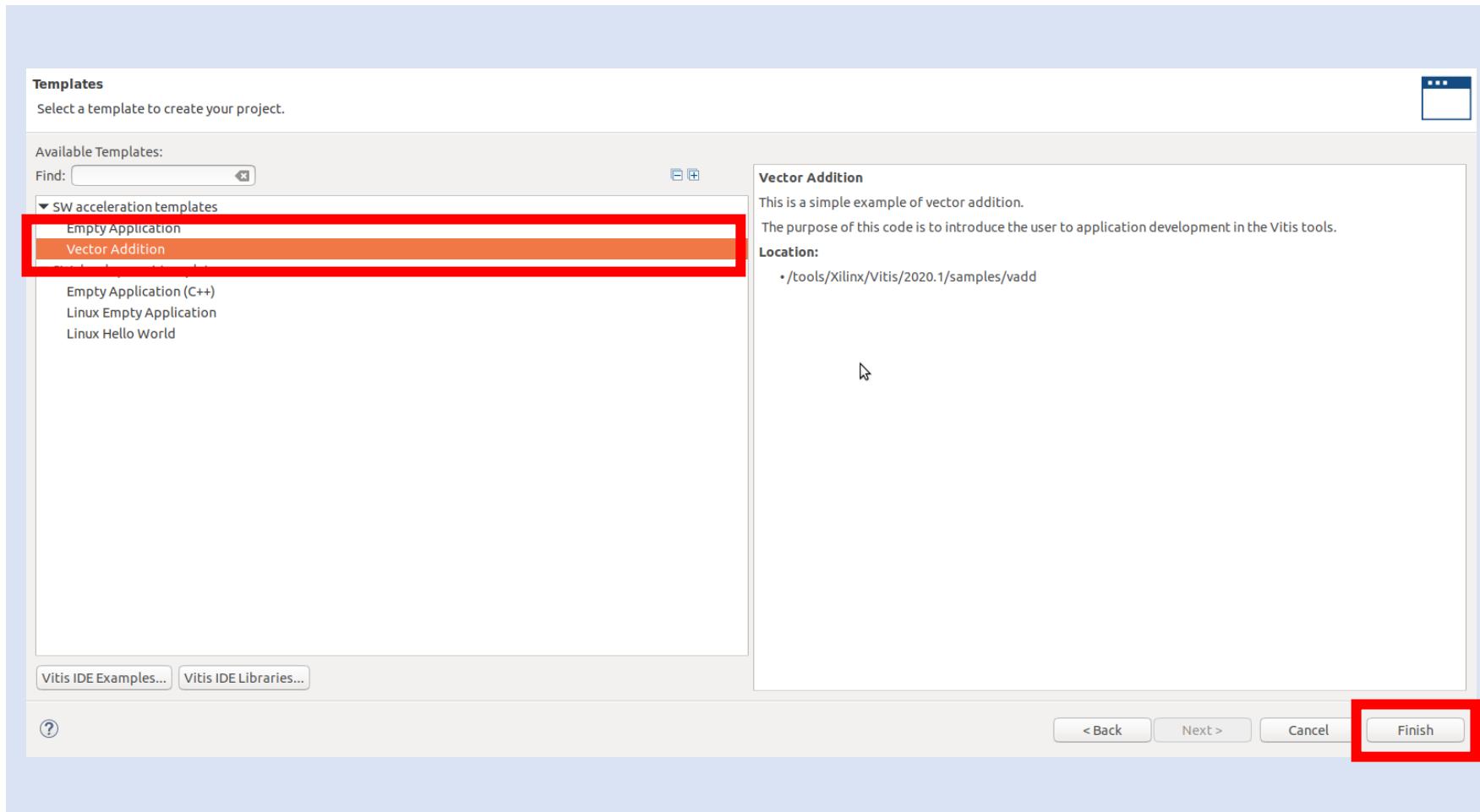
Lab 1: Understanding Vitis Project creation & Flow

Step 8 – Enter the Sysroot, Root FS and Kernel image previously installed, click next



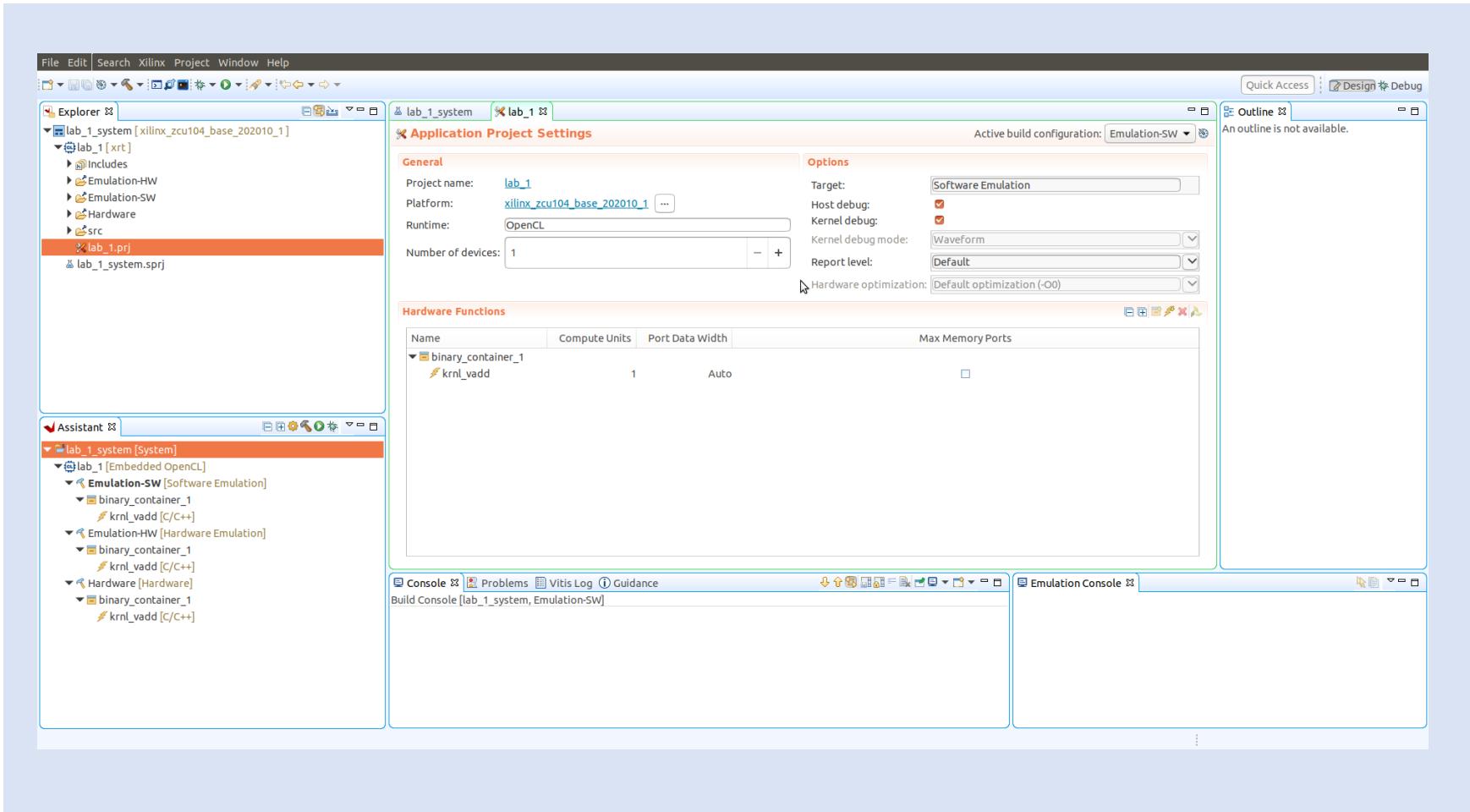
Lab 1: Understanding Vitis Project creation & Flow

Step 8 – Select the Vector Addition example and click finish



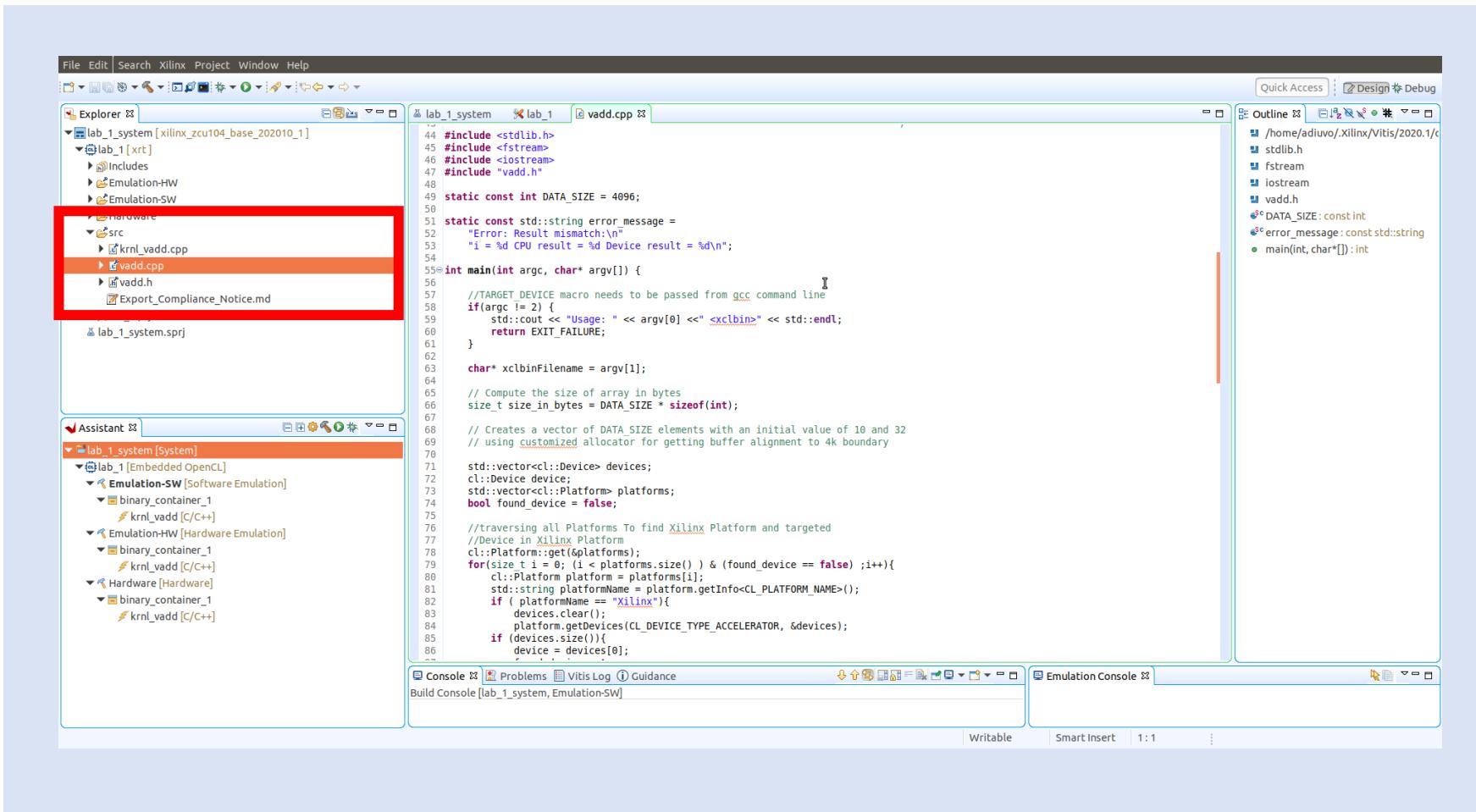
Lab 1: Understanding Vitis Project creation & Flow

Step 9 – This will open the project in the Vitis IDE



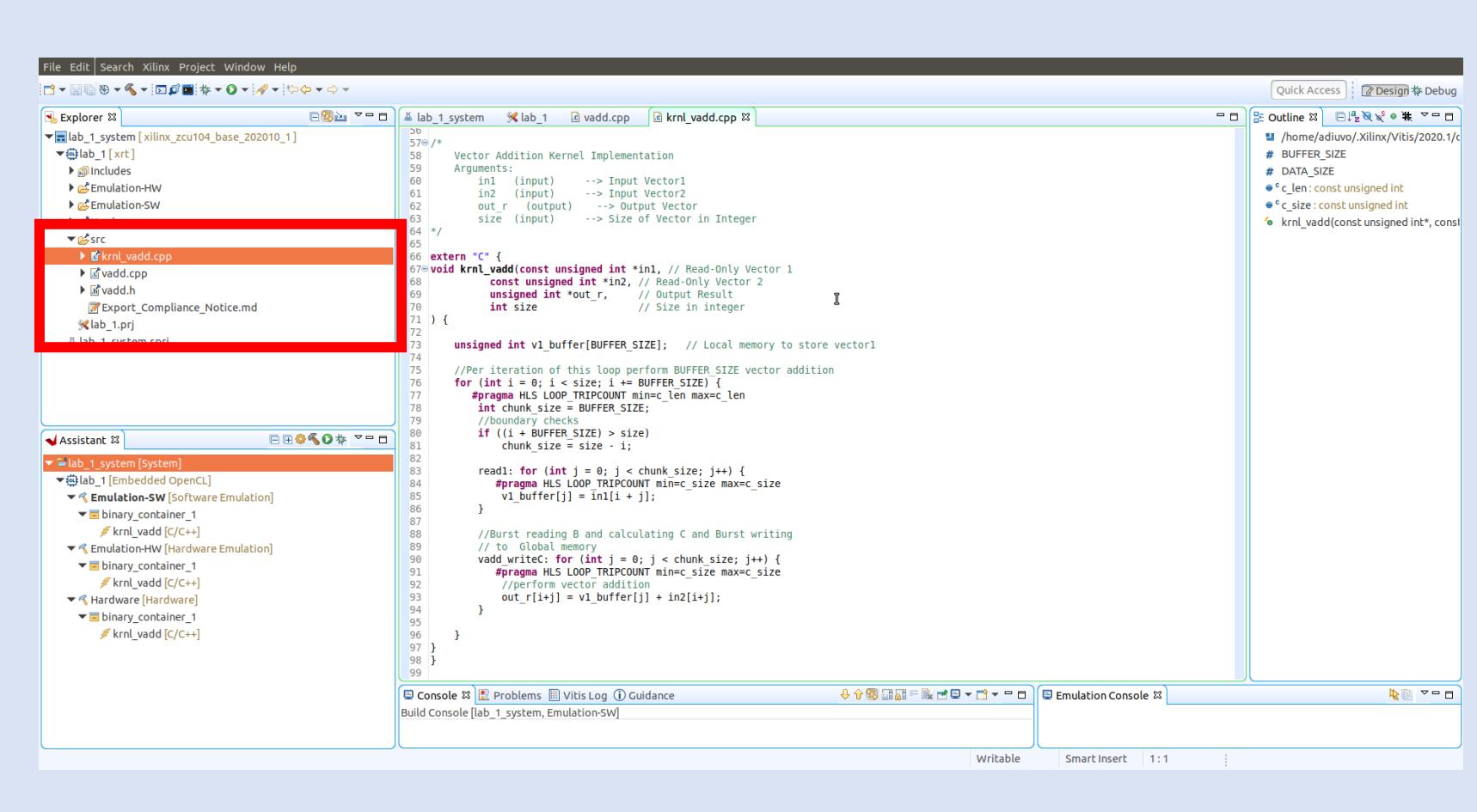
Lab 1: Understanding Vitis Project creation & Flow

Step 10 – Expand the src directory and double click on the Vadd.cpp file – this is the host SW



Lab 1: Understanding Vitis Project creation & Flow

Step 11 – Double click on the krnl_vadd.cpp file – this is the accelerator

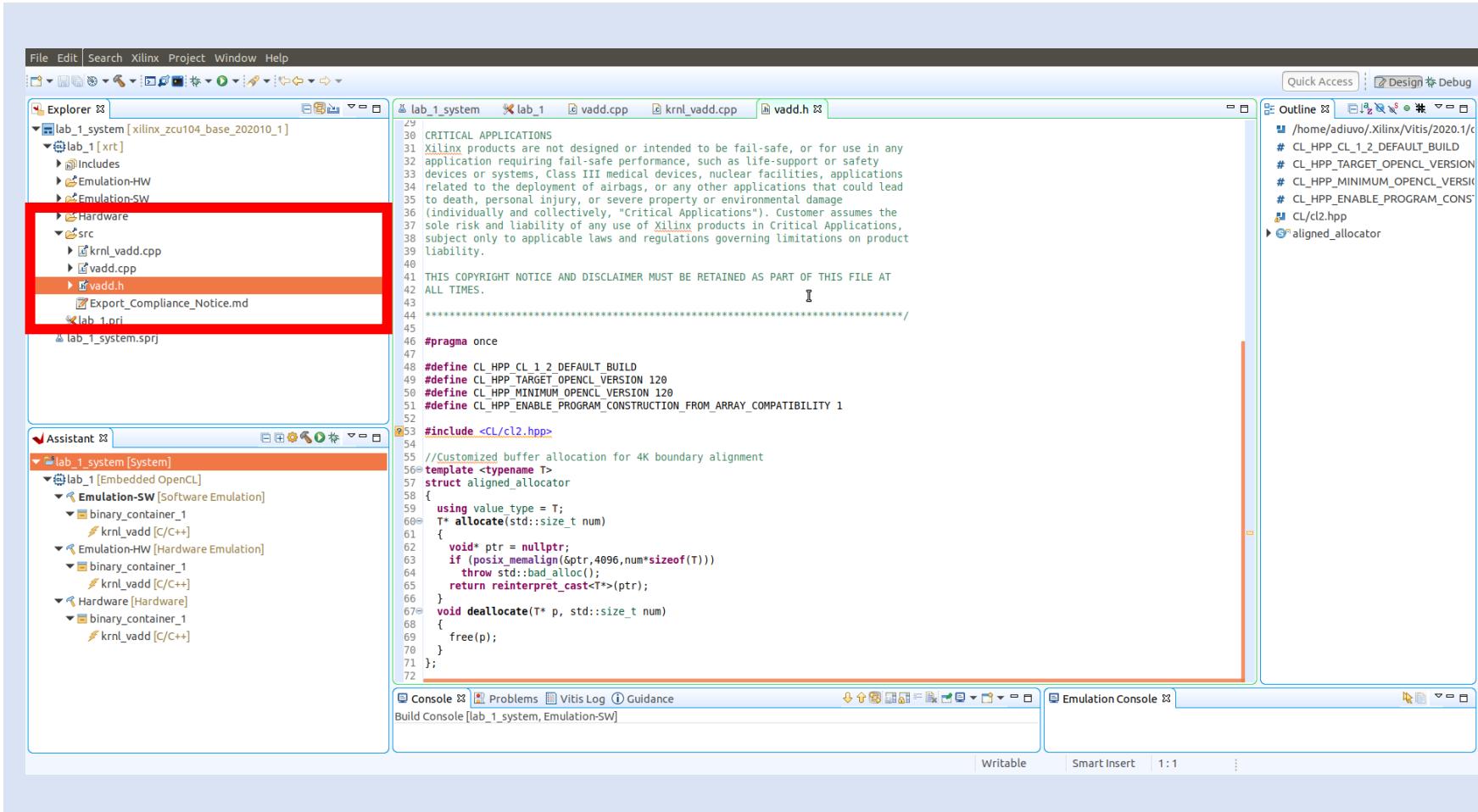


The screenshot shows the Vitis IDE interface with the following components:

- File Bar:** File, Edit, Search, Xilinx, Project, Window, Help.
- Toolbars:** Standard toolbar with icons for file operations, search, and project management.
- Explorer View:** Shows the project structure under "lab_1_system [xilinx_zcu104_base_202010_1]". A red box highlights the "src" folder, which contains "krnl_vadd.cpp", "vadd.cpp", "vadd.h", and "Export_Compliance_Note.md".
- Editor View:** Displays the content of "krnl_vadd.cpp". The code is an HLS implementation for vector addition, defining a function "krnl_vadd" that takes four arguments: two input vectors (in1, in2), one output vector (out_r), and a size integer (size). It uses local memory (v1_buffer) to store intermediate results and performs a loop from 0 to size-1 to add elements.
- Outline View:** Shows the symbols defined in the code, including "# BUFFER_SIZE", "# DATA_SIZE", and the "krnl_vadd" function.
- Assistant View:** Shows the system configuration under "lab_1_system [System]". It includes sections for "Emulation-SW [Software Emulation]" and "Emulation-HW [Hardware Emulation]", each containing a "binary_container_1" with "krnl_vadd [C/C++]".
- Console View:** Displays the build console output for "lab_1_system, Emulation-SW".
- Emulation Console:** An empty window for monitoring hardware emulation activity.

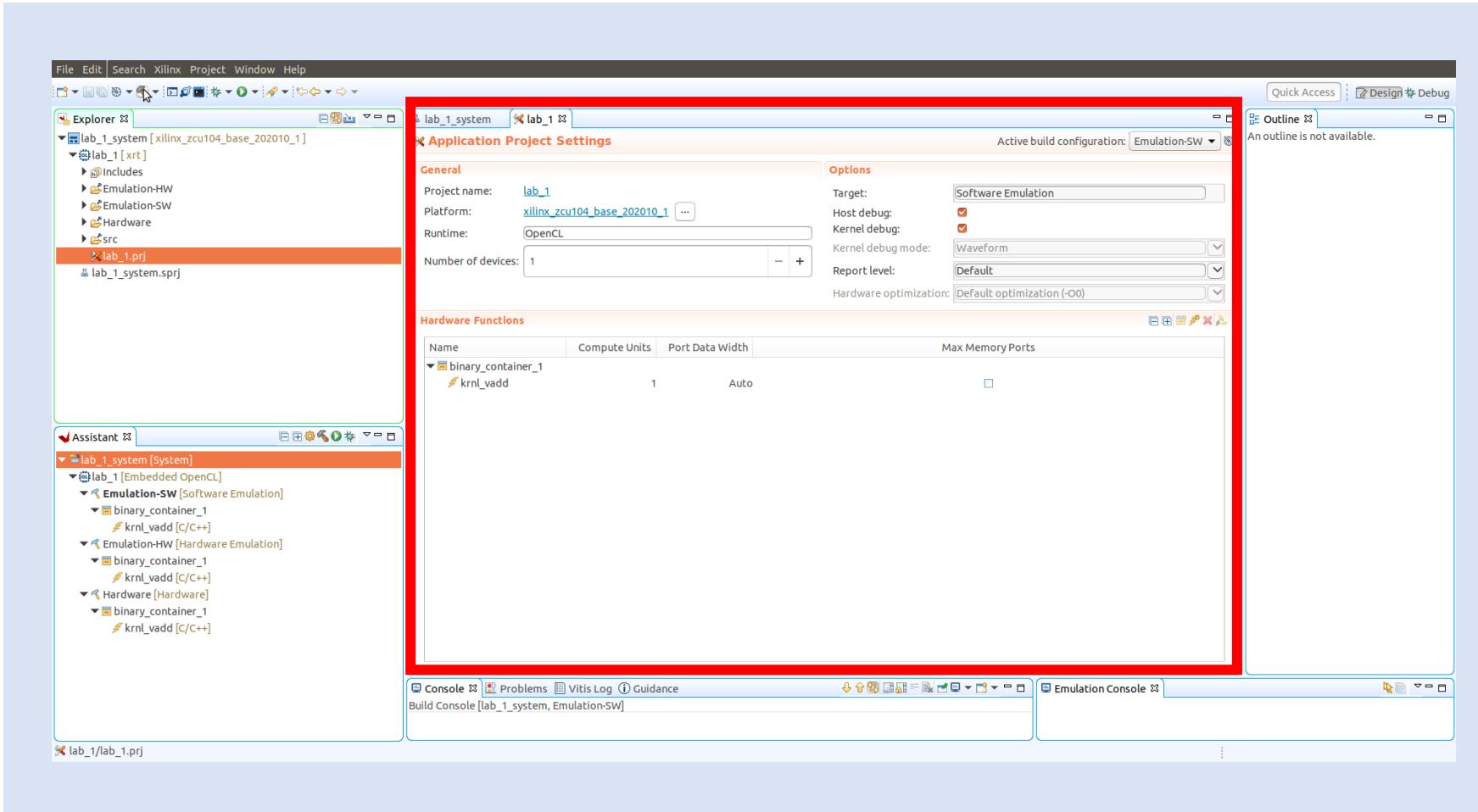
Lab 1: Understanding Vitis Project creation & Flow

Step 12 – Double click on the vadd.h



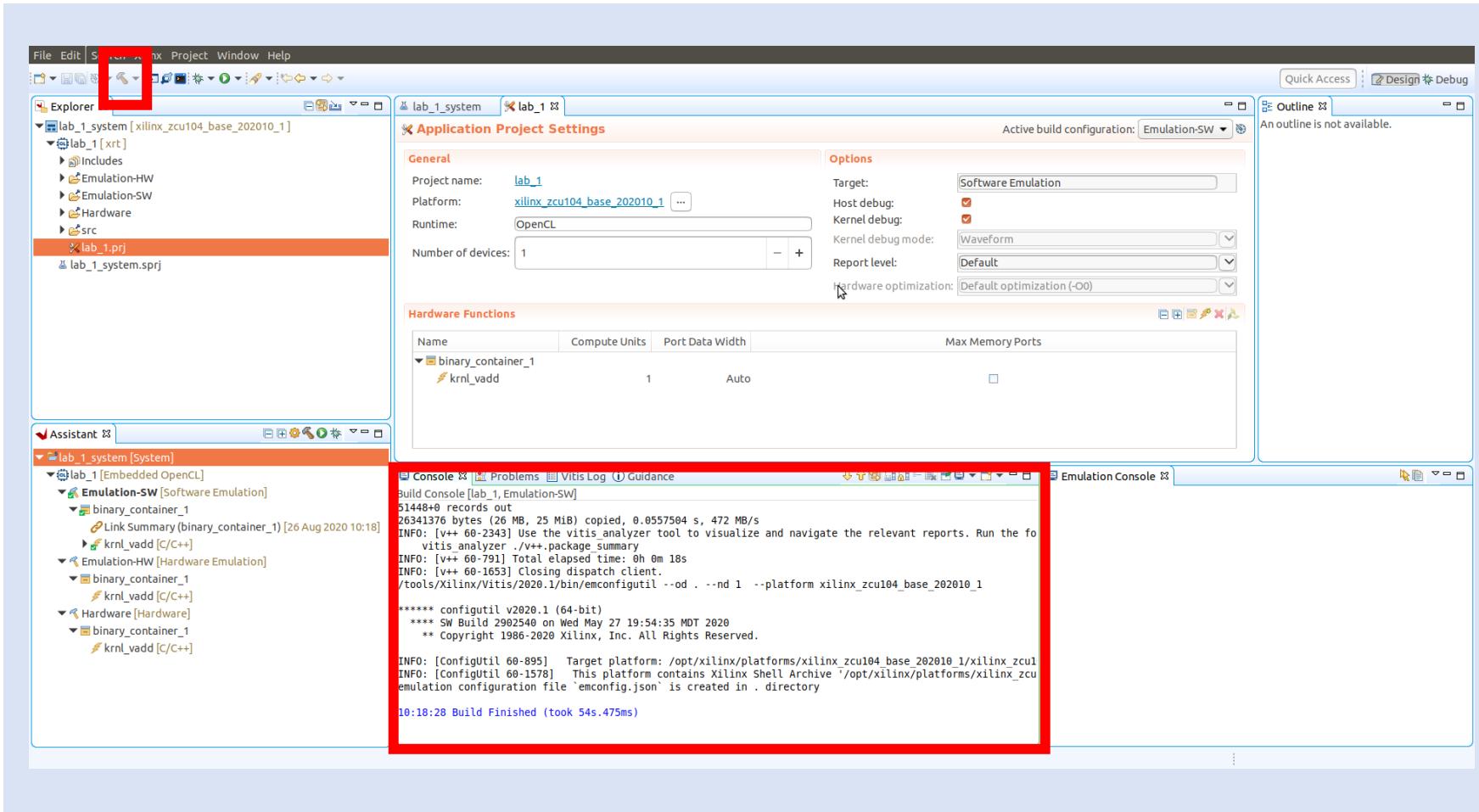
Lab 1: Understanding Vitis Project creation & Flow

Step 13 – Click on the lab_1 tab this where we set most configurations for building – make sure the active build configuration is set at Emulation-SW



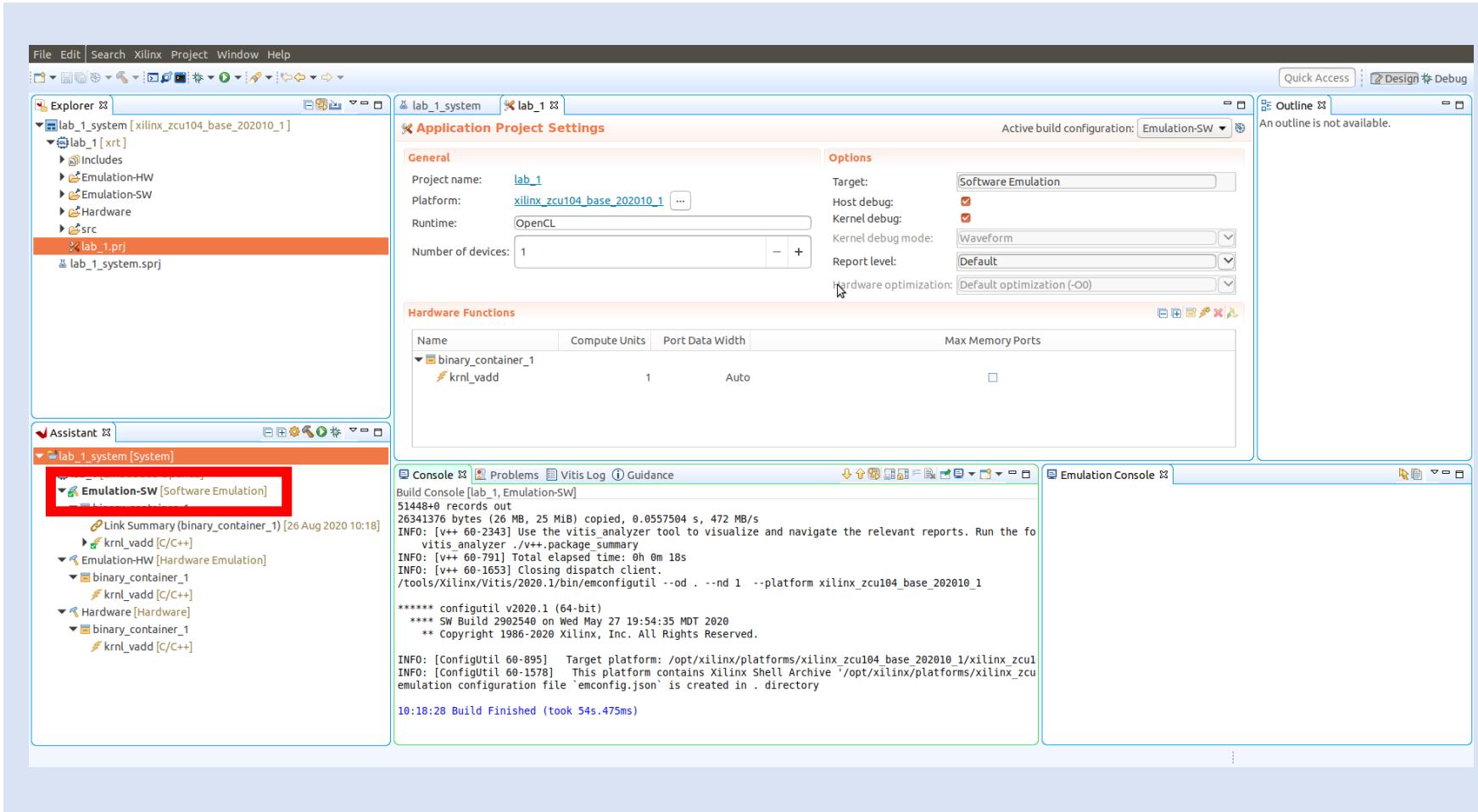
Lab 1: Understanding Vitis Project creation & Flow

Step 14 – Build the SW Emulation by clicking on the hammer



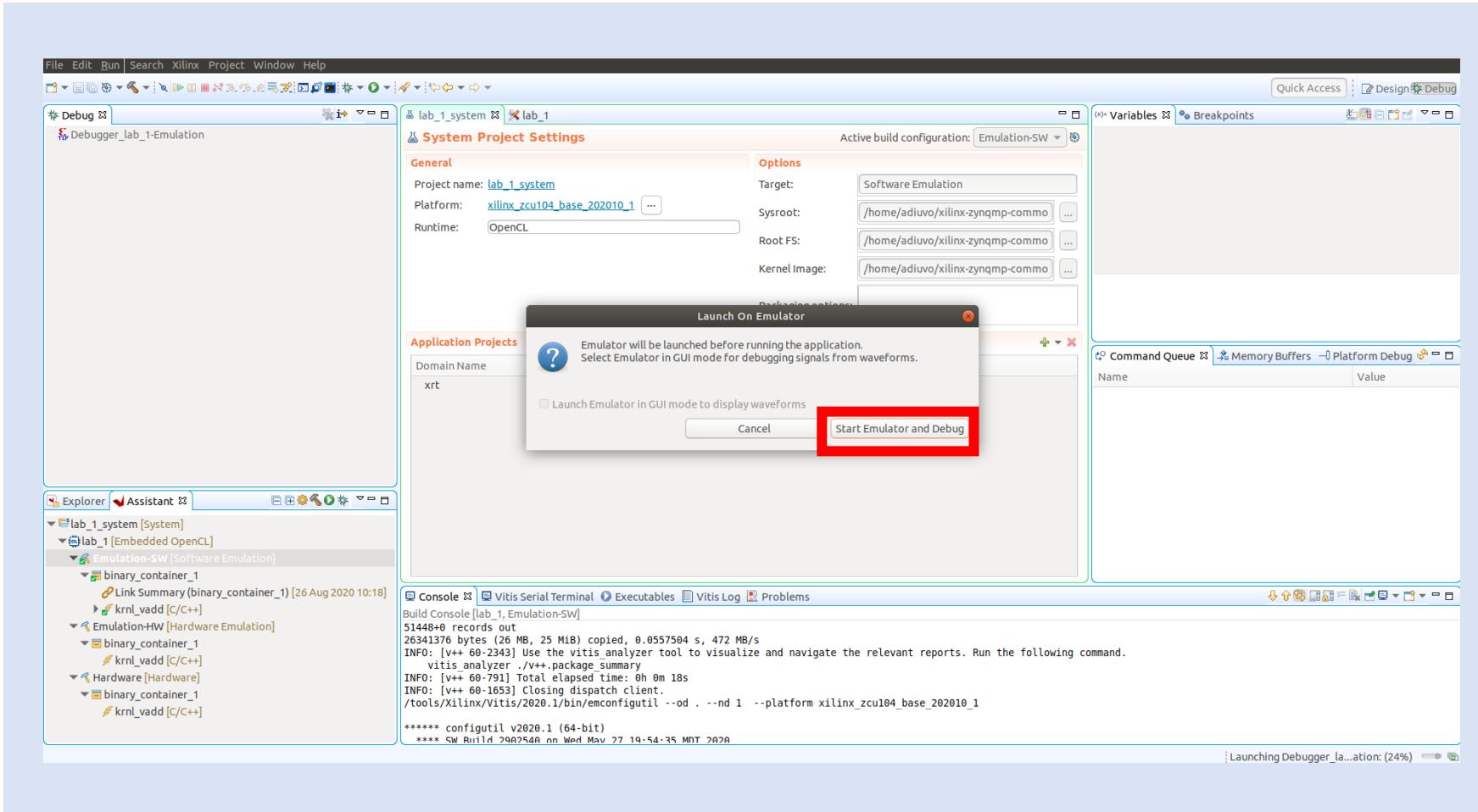
Lab 1: Understanding Vitis Project creation & Flow

Step 15 – Launch the debugger by right clicking on Emulation-SW and Launch on Emulator



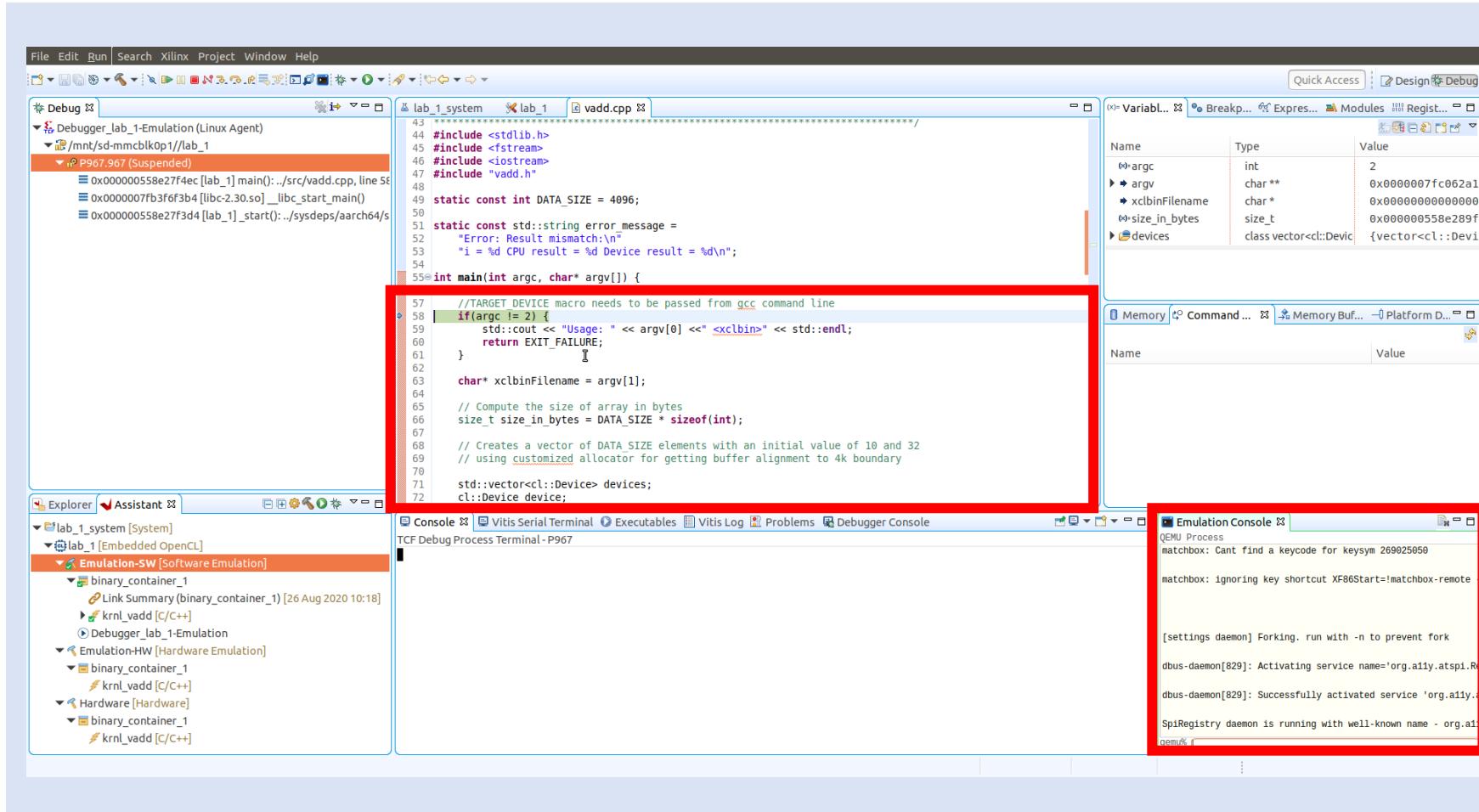
Lab 1: Understanding Vitis Project creation & Flow

Step 16 – This will open the Debug Perspective and click on start Emulator and Debug



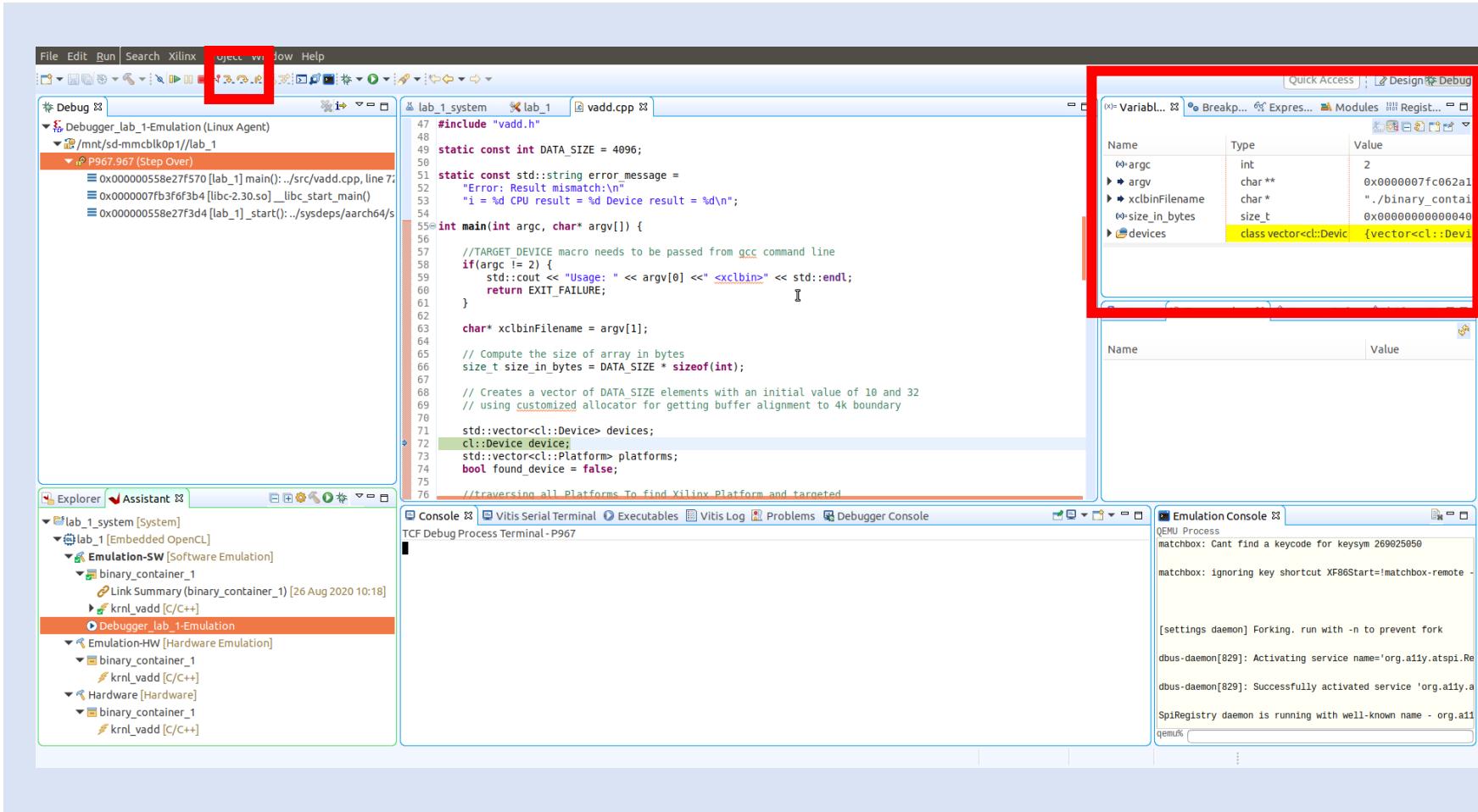
Lab 1: Understanding Vitis Project creation & Flow

Step 17 – Once the Emulator is loaded and the TCF agent connected the Host application will pause awaiting execution.



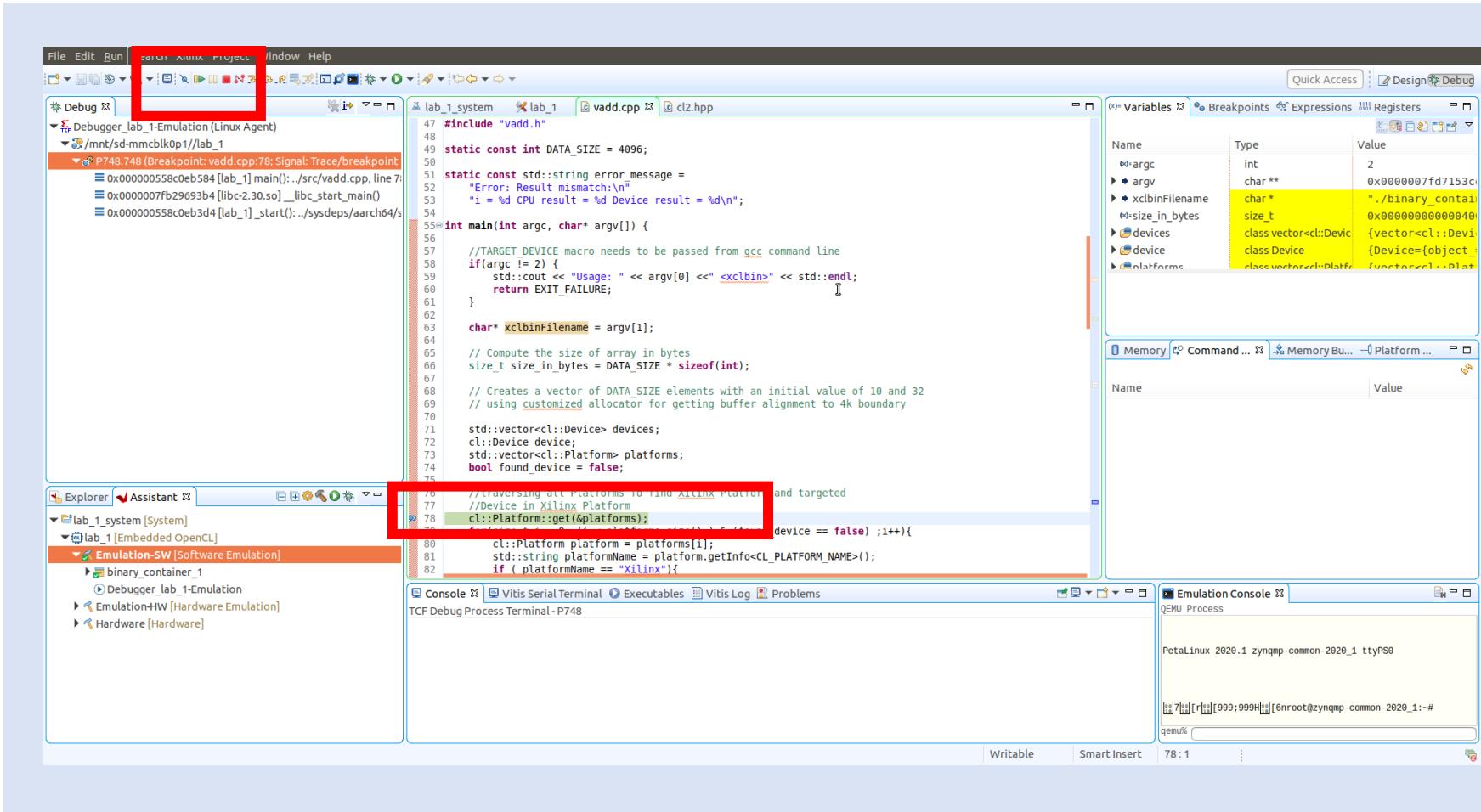
Lab 1: Understanding Vitis Project creation & Flow

Step 18 – Single step through a few instructions and see the variables update



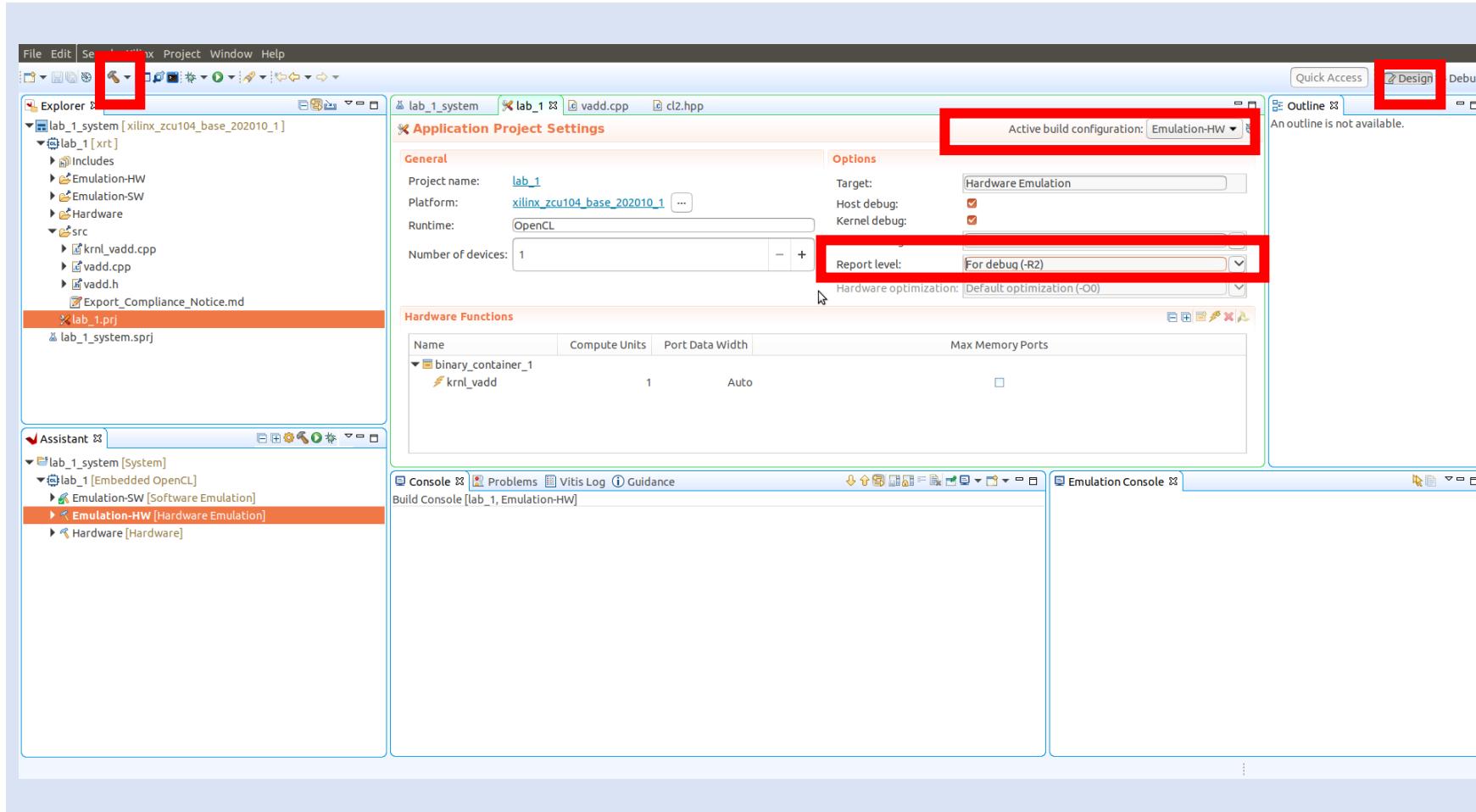
Lab 1: Understanding Vitis Project creation & Flow

Step 19 – Double click in the edge of the source code on line 78 to insert a breakpoint then select run, see the break point get hit and variables update. Click on the red terminate button



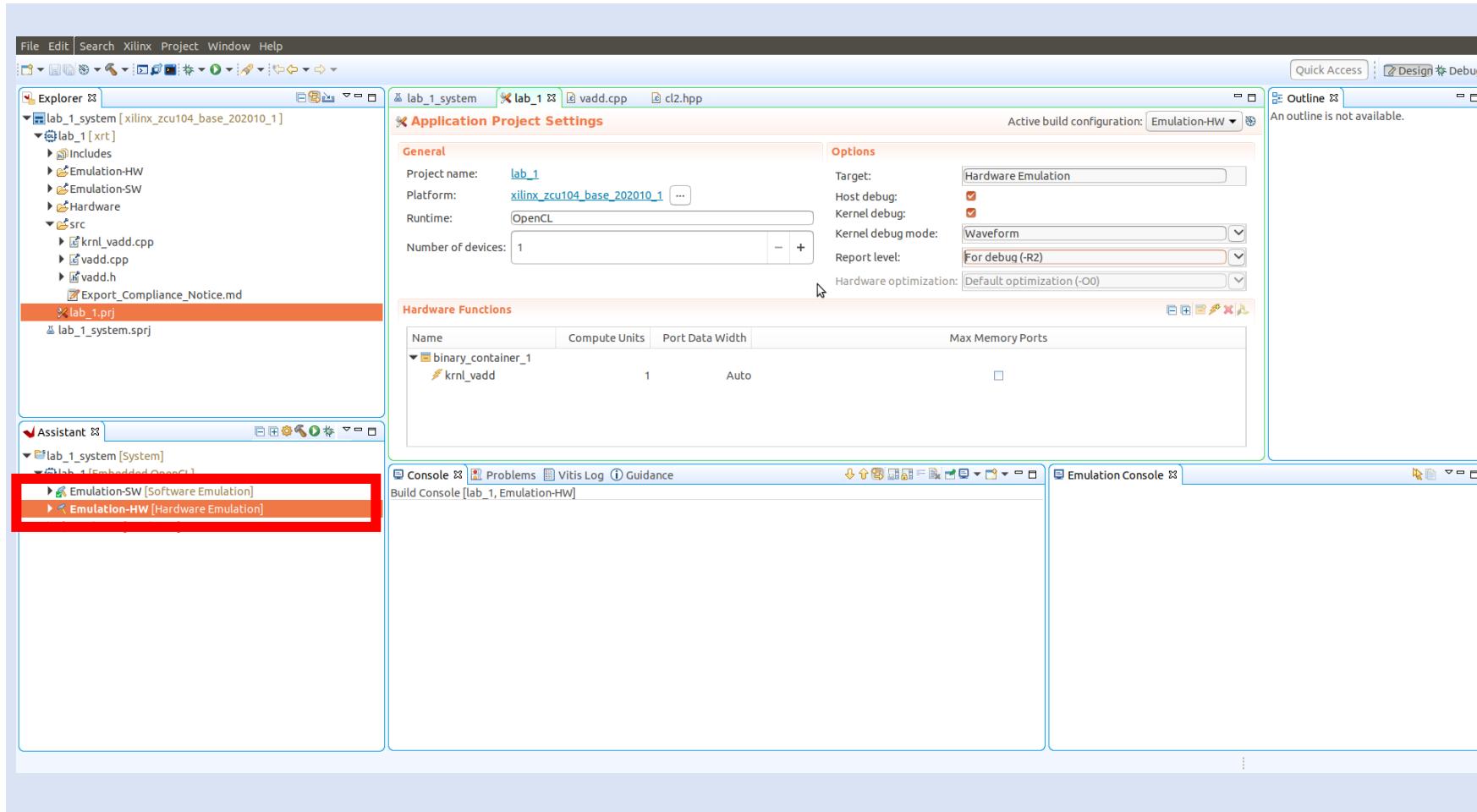
Lab 1: Understanding Vitis Project creation & Flow

Step 20 – Change the perspective back to design, set the active build configuration to Emulation-HW, Report Level to For-Debug and build the design



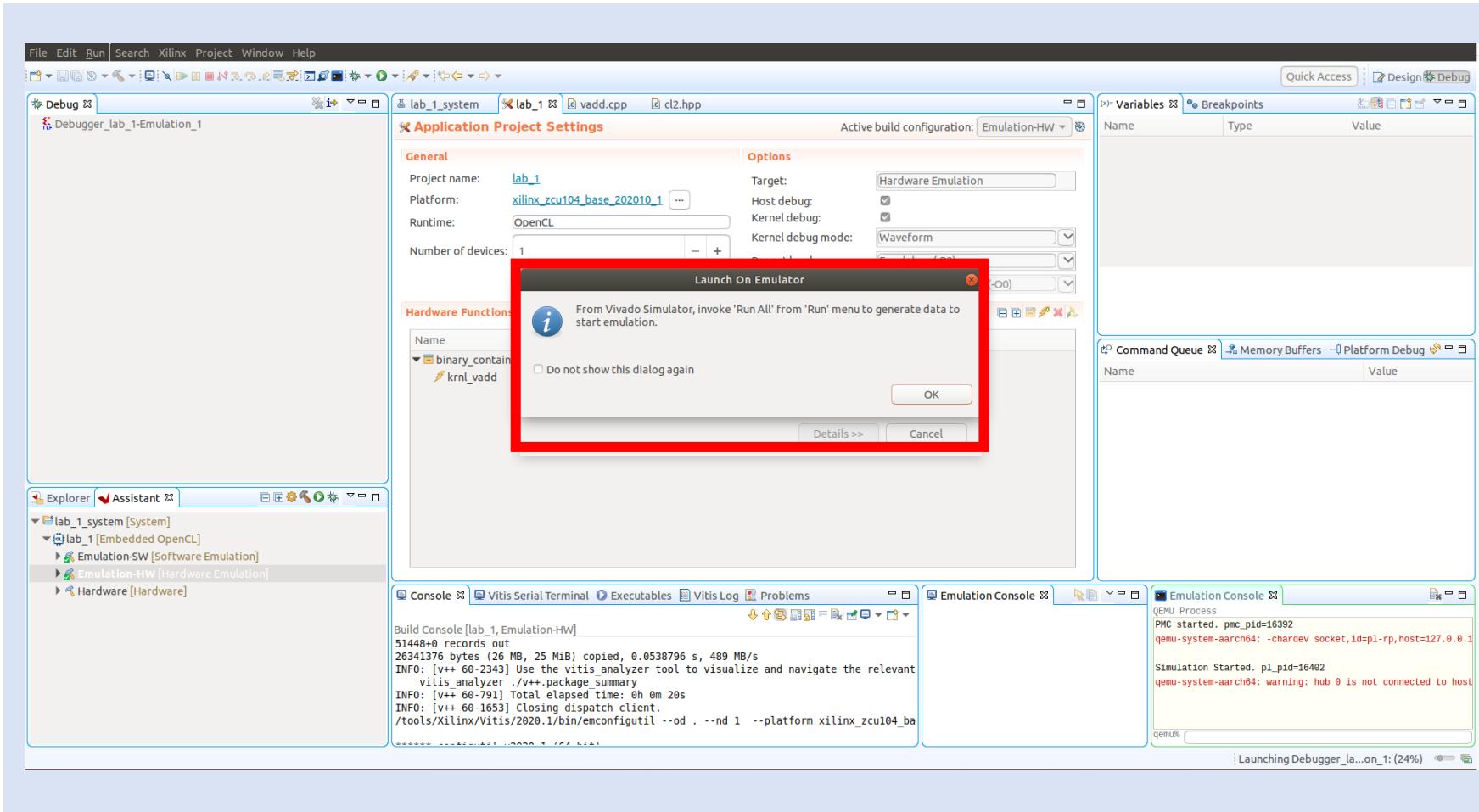
Lab 1: Understanding Vitis Project creation & Flow

Step 21 – Once build is complete, right click on Emulation-HW and launch a emulation debug session



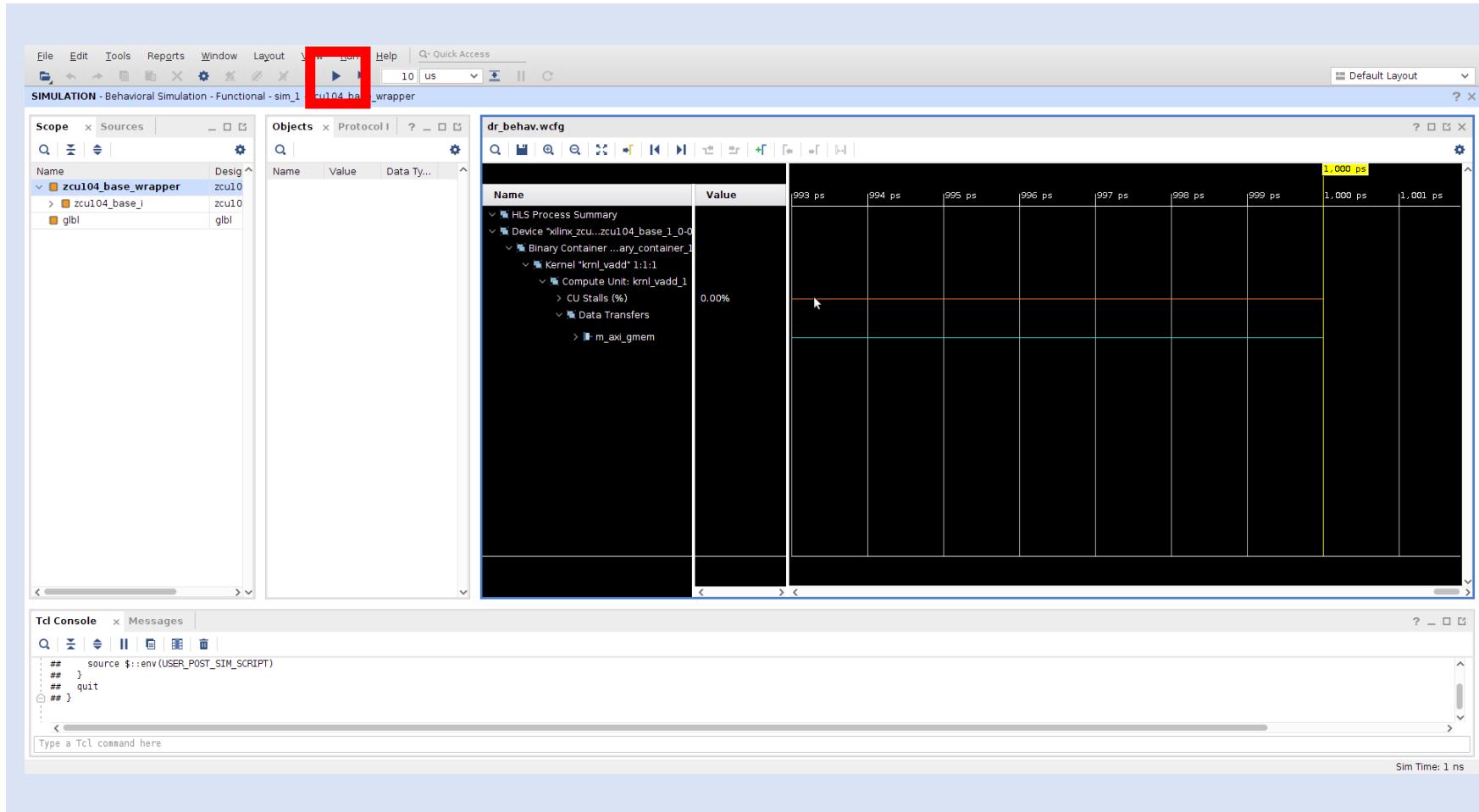
Lab 1: Understanding Vitis Project creation & Flow

Step 22 – This will launch Vivado, change views to Vivado when the dialog below appears



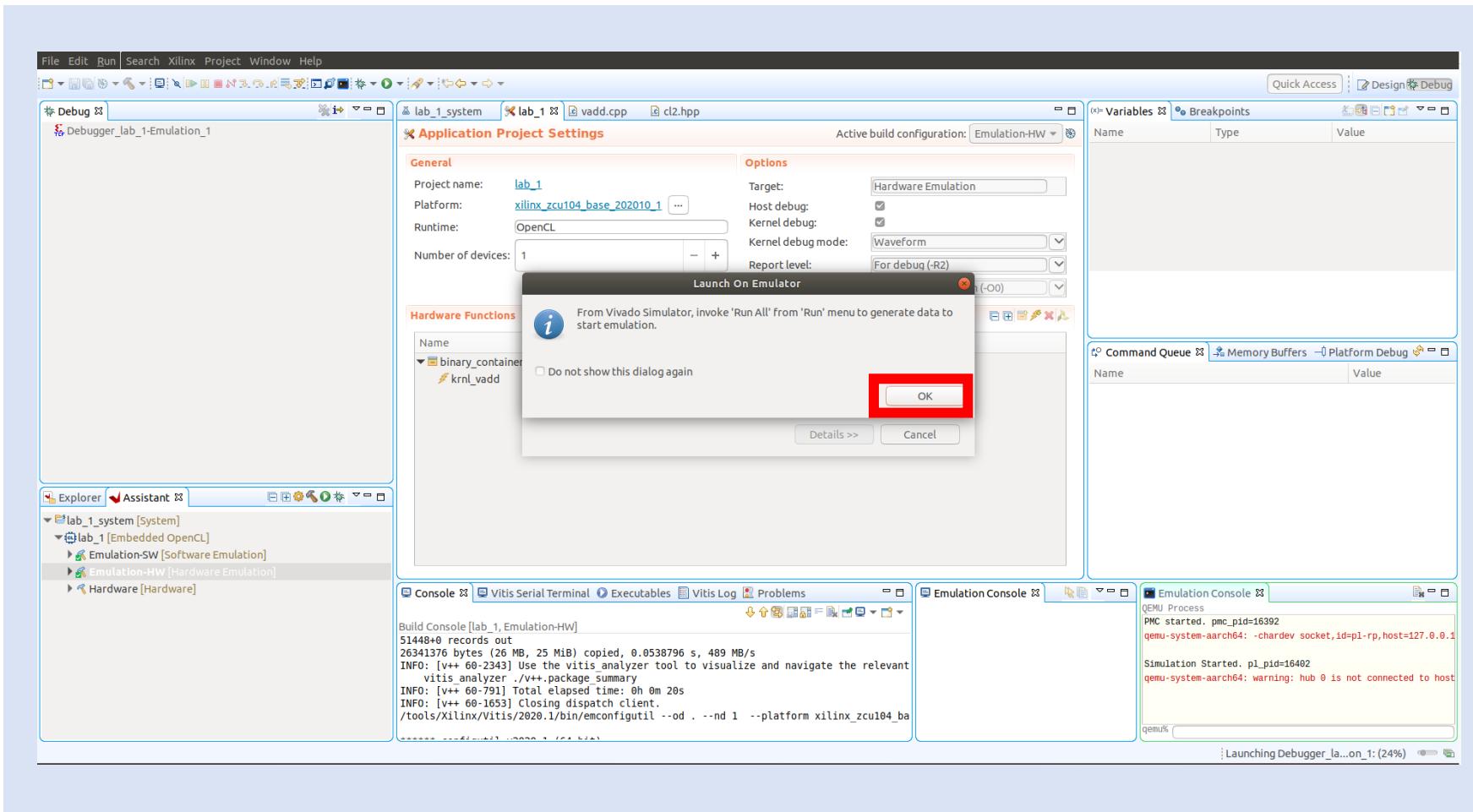
Lab 1: Understanding Vitis Project creation & Flow

Step 23 – Click on the run all button in Vivado and switch back to Vitis



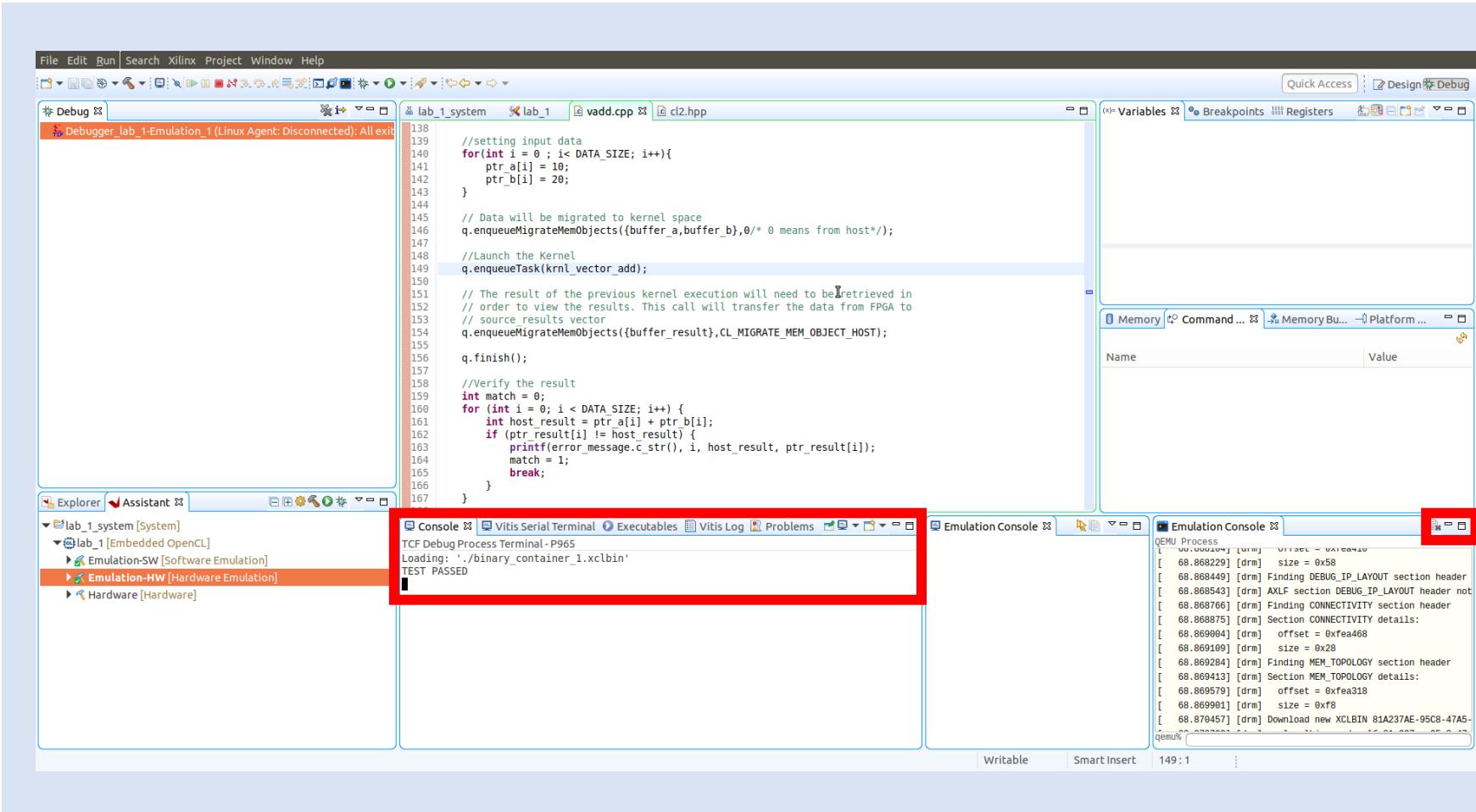
Lab 1: Understanding Vitis Project creation & Flow

Step 24 – Click OK on the dialog



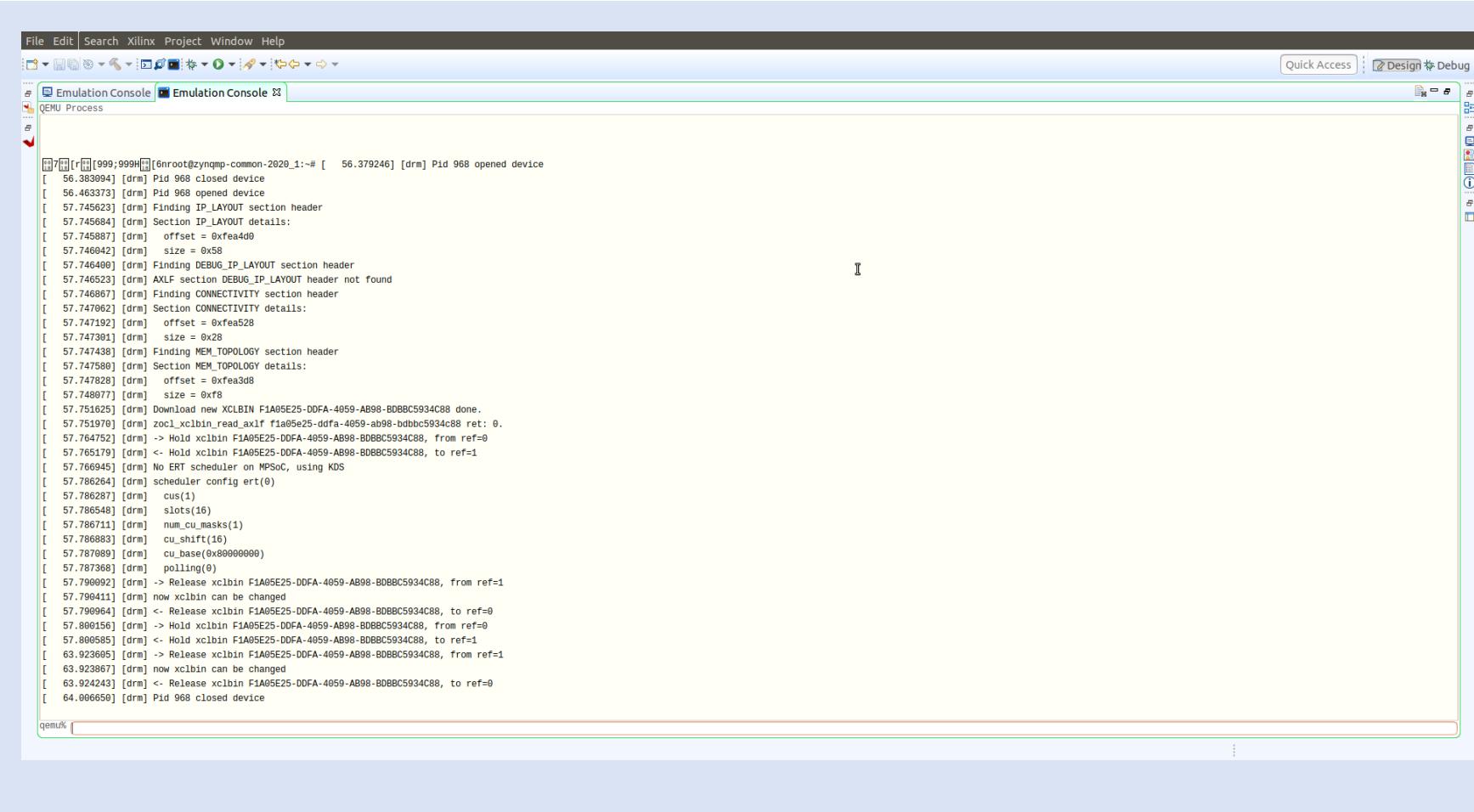
Lab 1: Understanding Vitis Project creation & Flow

Step 25 – When the Debugger loads, click Run and the Application will execute and should show a passed status, click on maximise in the Emulation Console



Lab 1: Understanding Vitis Project creation & Flow

Step 26 – In the Emulation console you will see the XCLBinary being loaded as you will on the real hardware.

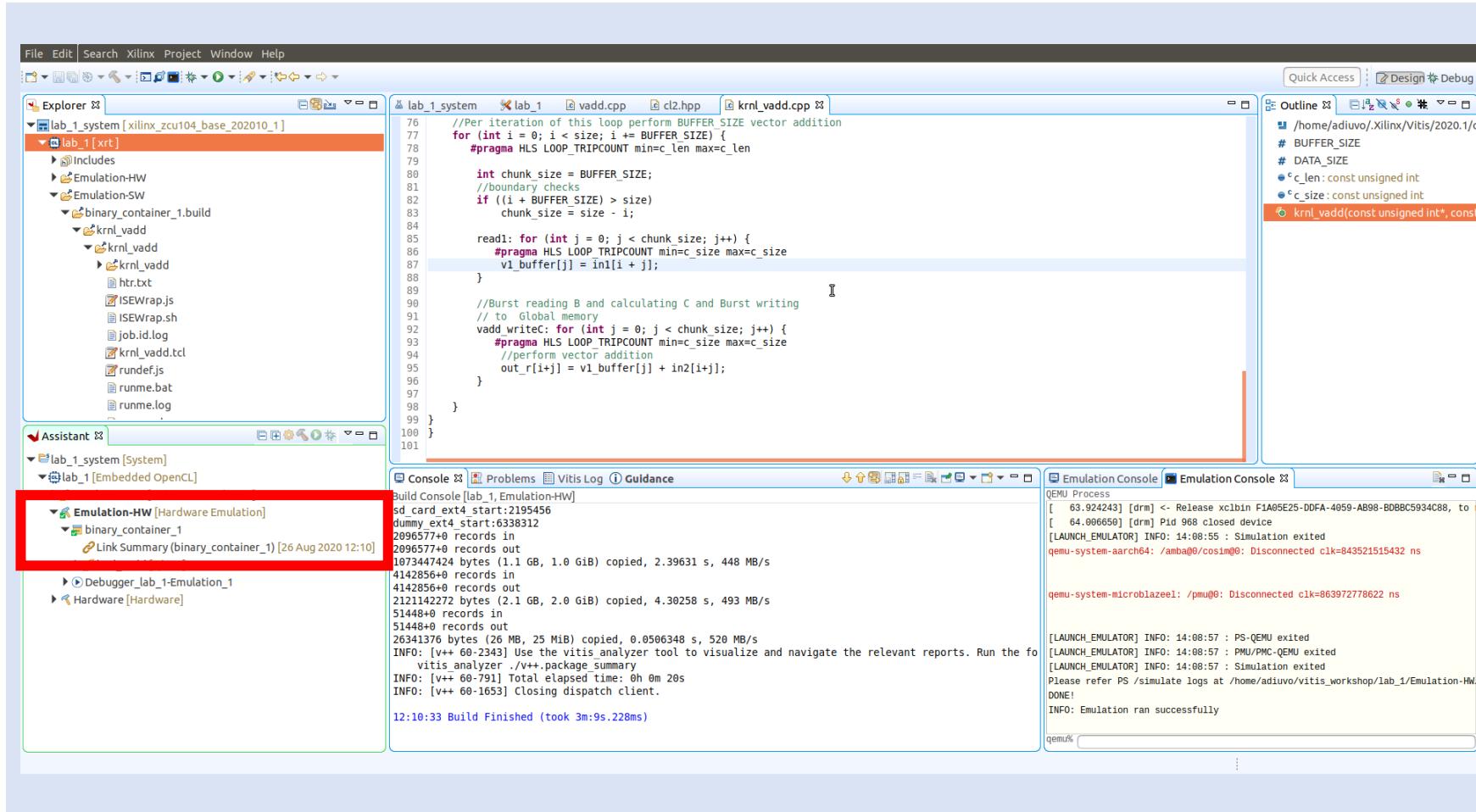


The screenshot shows the Vitis IDE interface with the Emulation Console tab selected. The console window displays a log of system boot and initialization messages. Key logs include:

- [56.383094] [drm] Pid 968 closed device
- [56.463373] [drm] Pid 968 opened device
- [57.745623] [drm] Finding IP_LAYOUT section header
- [57.745684] [drm] Section IP_LAYOUT details:
- [57.745887] [drm] offset = 0xfea4d0
- [57.746042] [drm] size = 0x58
- [57.746408] [drm] Finding DEBUG_IP_LAYOUT section header
- [57.746523] [drm] AXLF section DEBUG_IP_LAYOUT header not found
- [57.746867] [drm] Finding CONNECTIVITY section header
- [57.747062] [drm] Section CONNECTIVITY details:
- [57.747192] [drm] offset = 0xfea528
- [57.747301] [drm] size = 0x28
- [57.747438] [drm] Finding MEM_TOPOLOGY section header
- [57.747580] [drm] Section MEM_TOPOLOGY details:
- [57.747828] [drm] offset = 0xfea3d8
- [57.748077] [drm] size = 0x8f
- [57.751625] [drm] Download new XCLBIN f1a05e25-ddfa-4059-ab98-bdbbc5934c88 done.
- [57.751970] [drm] zocl_xclbin_read_axlf f1a05e25-ddfa-4059-ab98-bdbbc5934c88 ret: 0
- [57.764752] [drm] -> Hold xclbin f1a05e25-ddfa-4059-ab98-bdbbc5934c88, from ref=0
- [57.765179] [drm] <- Hold xclbin f1a05e25-ddfa-4059-ab98-bdbbc5934c88, to ref=1
- [57.766945] [drm] No ERT scheduler or MPSoC, using KDS
- [57.786264] [drm] scheduler config ept(0)
- [57.786287] [drm] cus(1)
- [57.786548] [drm] slots(16)
- [57.786711] [drm] num_cu_masks(1)
- [57.786883] [drm] cu_shift(16)
- [57.787089] [drm] cu_base(0x80000000)
- [57.787368] [drm] polling(0)
- [57.790092] [drm] -> Release xclbin f1a05e25-ddfa-4059-ab98-bdbbc5934c88, from ref=1
- [57.790411] [drm] now xclbin can be changed
- [57.790964] [drm] <- Release xclbin f1a05e25-ddfa-4059-ab98-bdbbc5934c88, to ref=0
- [57.800156] [drm] -> Hold xclbin f1a05e25-ddfa-4059-ab98-bdbbc5934c88, from ref=0
- [57.800585] [drm] <- Hold xclbin f1a05e25-ddfa-4059-ab98-bdbbc5934c88, to ref=1
- [63.923665] [drm] -> Release xclbin f1a05e25-ddfa-4059-ab98-bdbbc5934c88, from ref=1
- [63.923867] [drm] now xclbin can be changed
- [63.924243] [drm] <- Release xclbin f1a05e25-ddfa-4059-ab98-bdbbc5934c88, to ref=0
- [64.006650] [drm] Pid 968 closed device

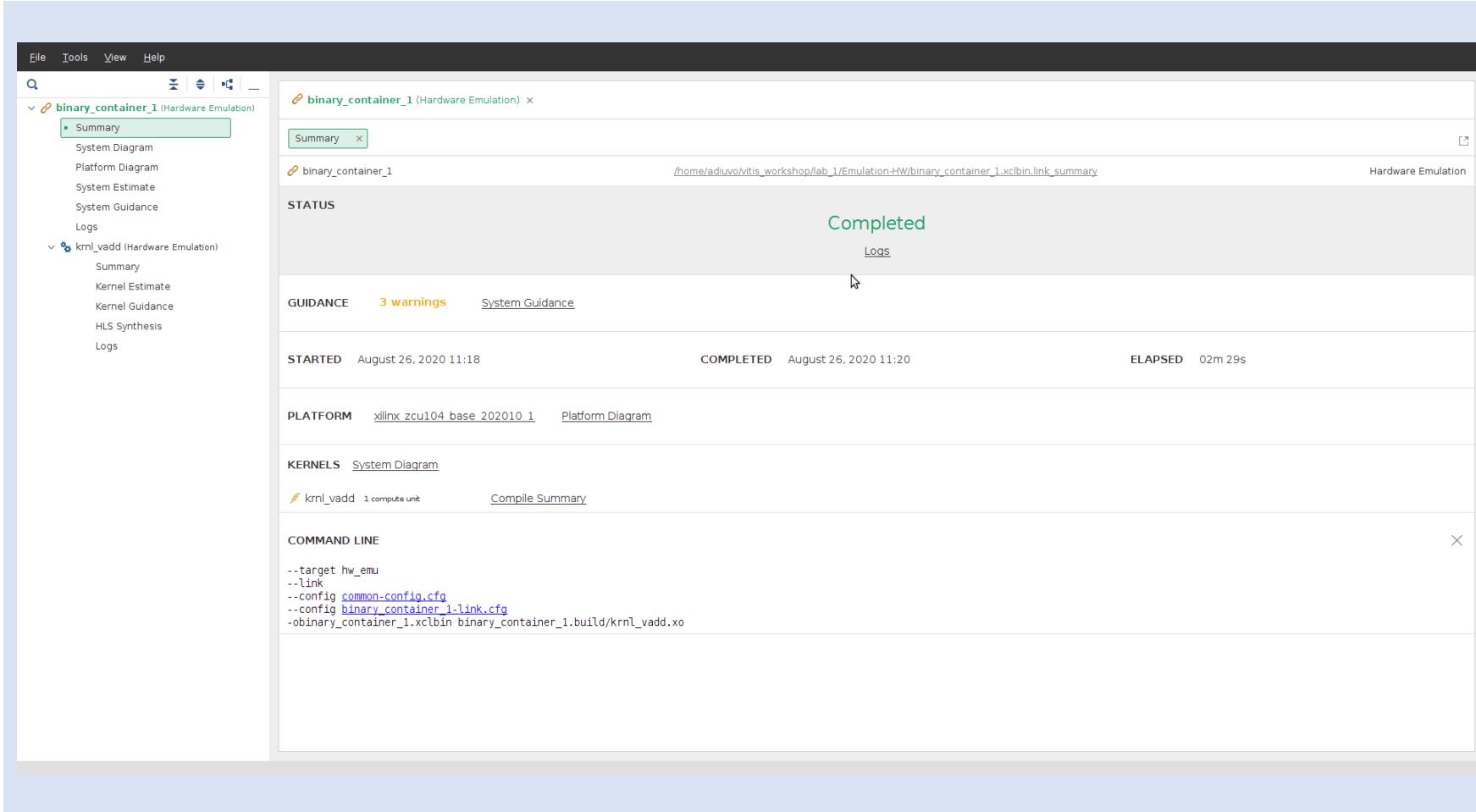
Lab 1: Understanding Vitis Project creation & Flow

Step 24 – Under the assistant view, Emulation hardware select the XCLBin, right click and open the Vitis Analyser.



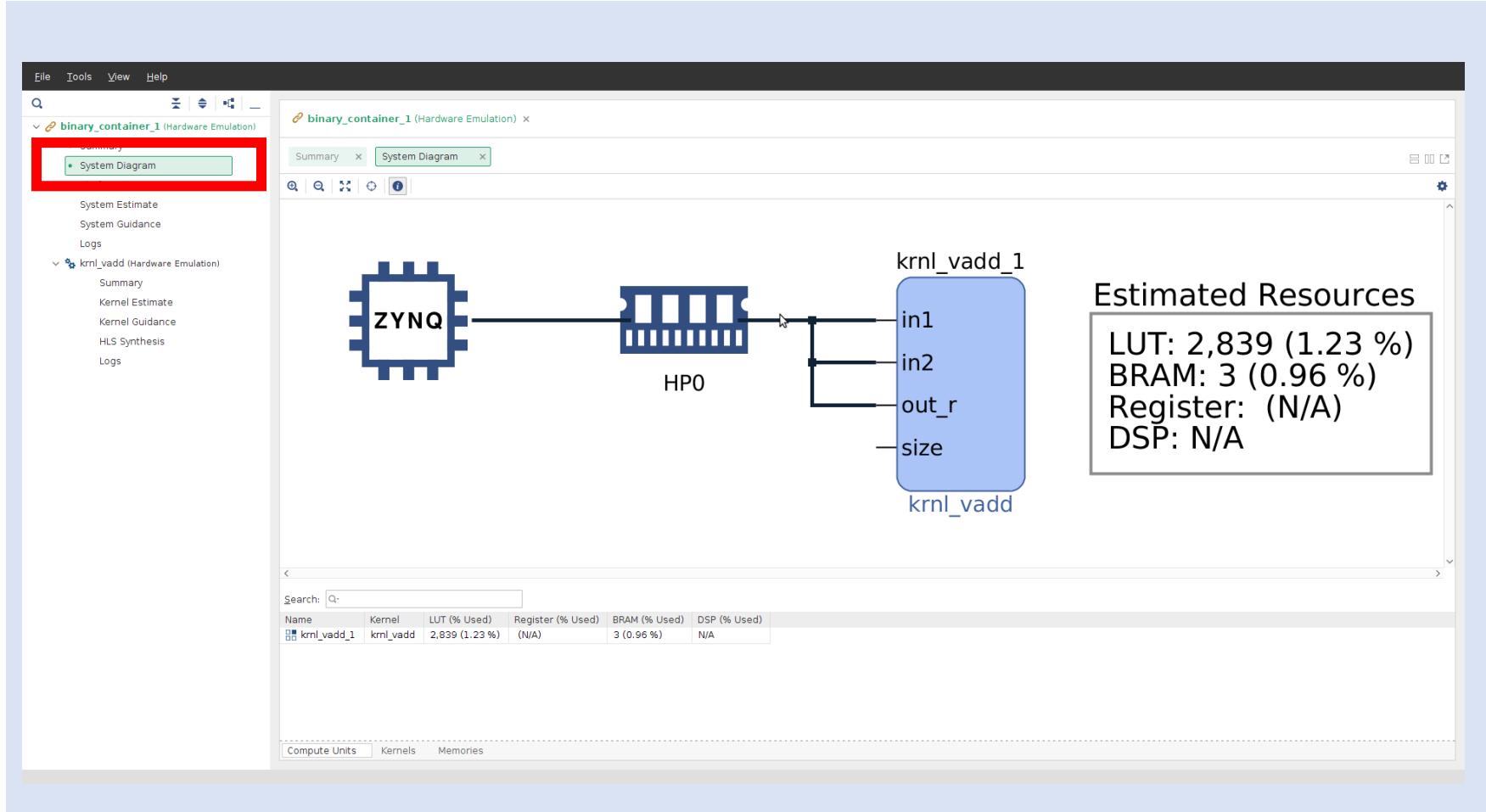
Lab 1: Understanding Vitis Project creation & Flow

Step 24 – The Vitis Analyzer will provide information on the System Performance and Accelerator performance.



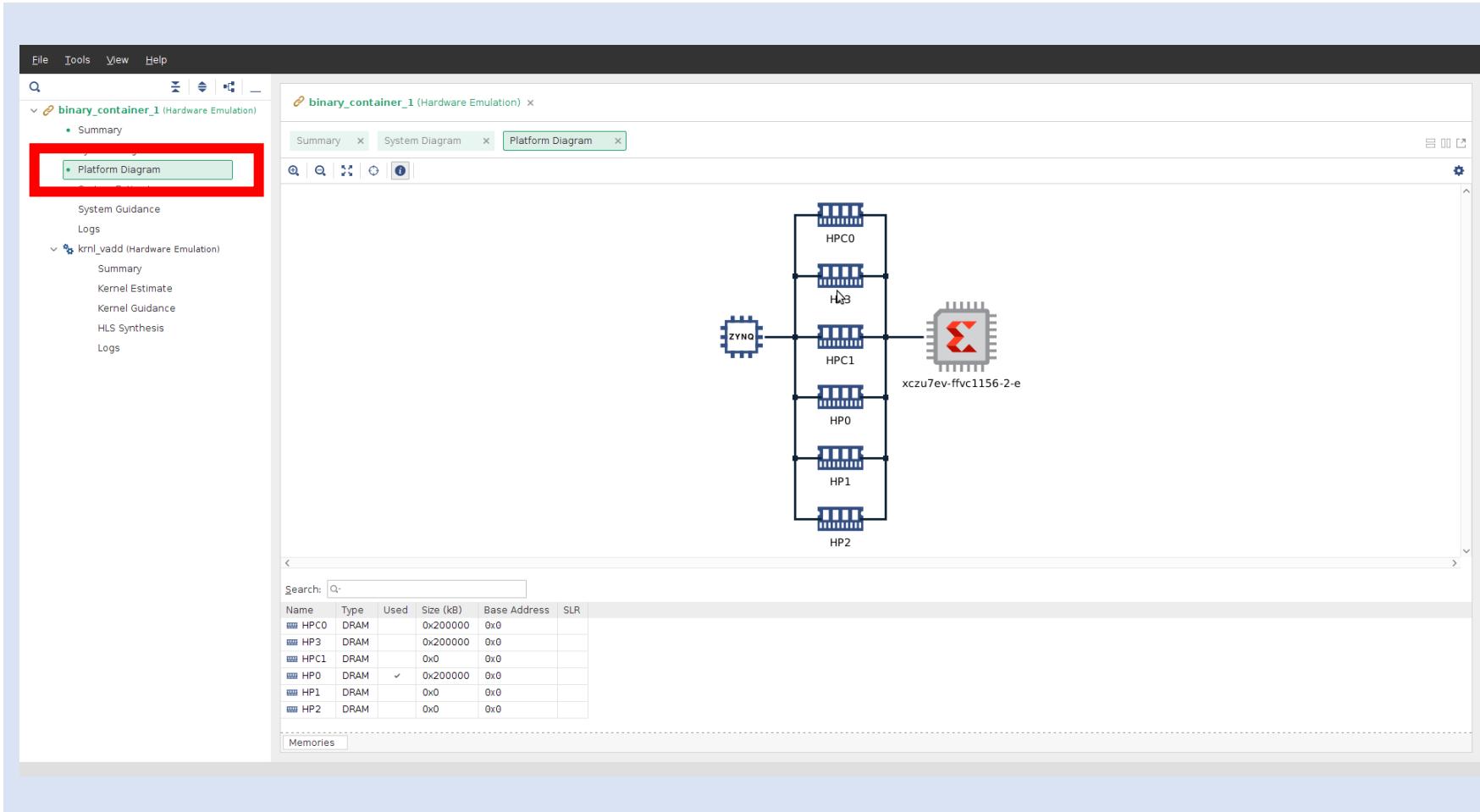
Lab 1: Understanding Vitis Project creation & Flow

Step 24 – Click on the System Design this will show how the accelerator is connected to the Host



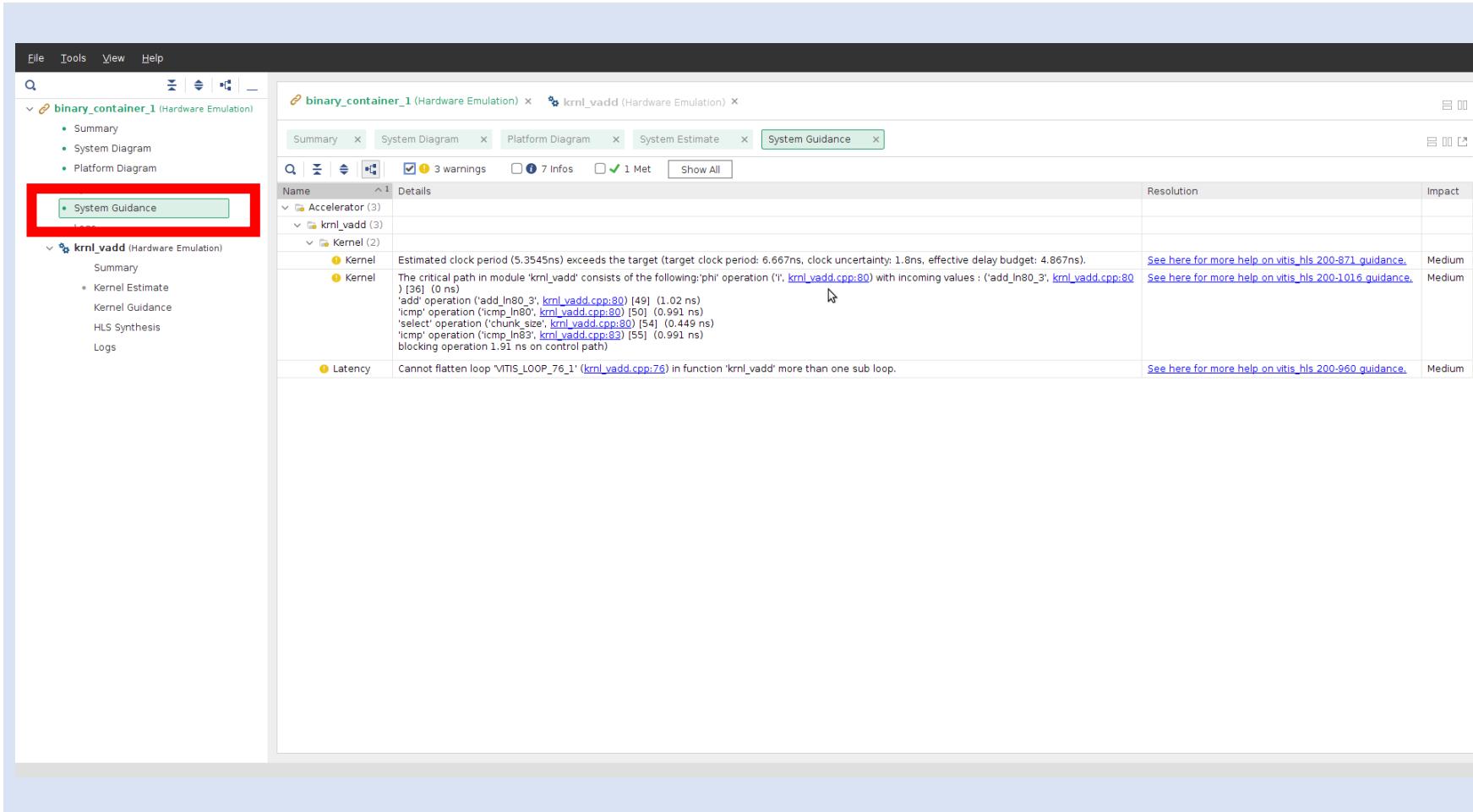
Lab 1: Understanding Vitis Project creation & Flow

Step 24 – Click on the Platform Diagram this will show the connections available in the system



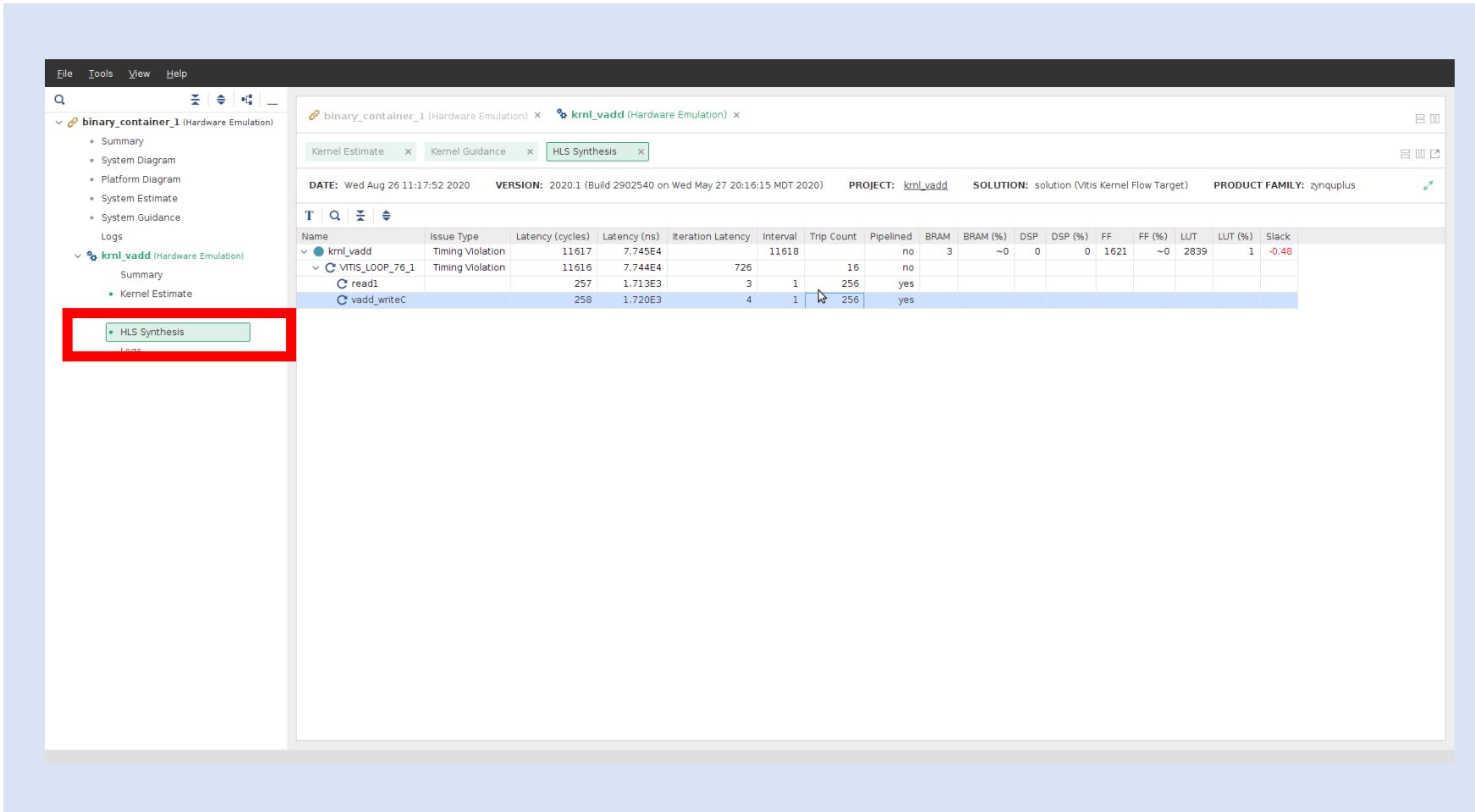
Lab 1: Understanding Vitis Project creation & Flow

Step 24 – Click on the System Guidance, this will report any warnings and resolutions



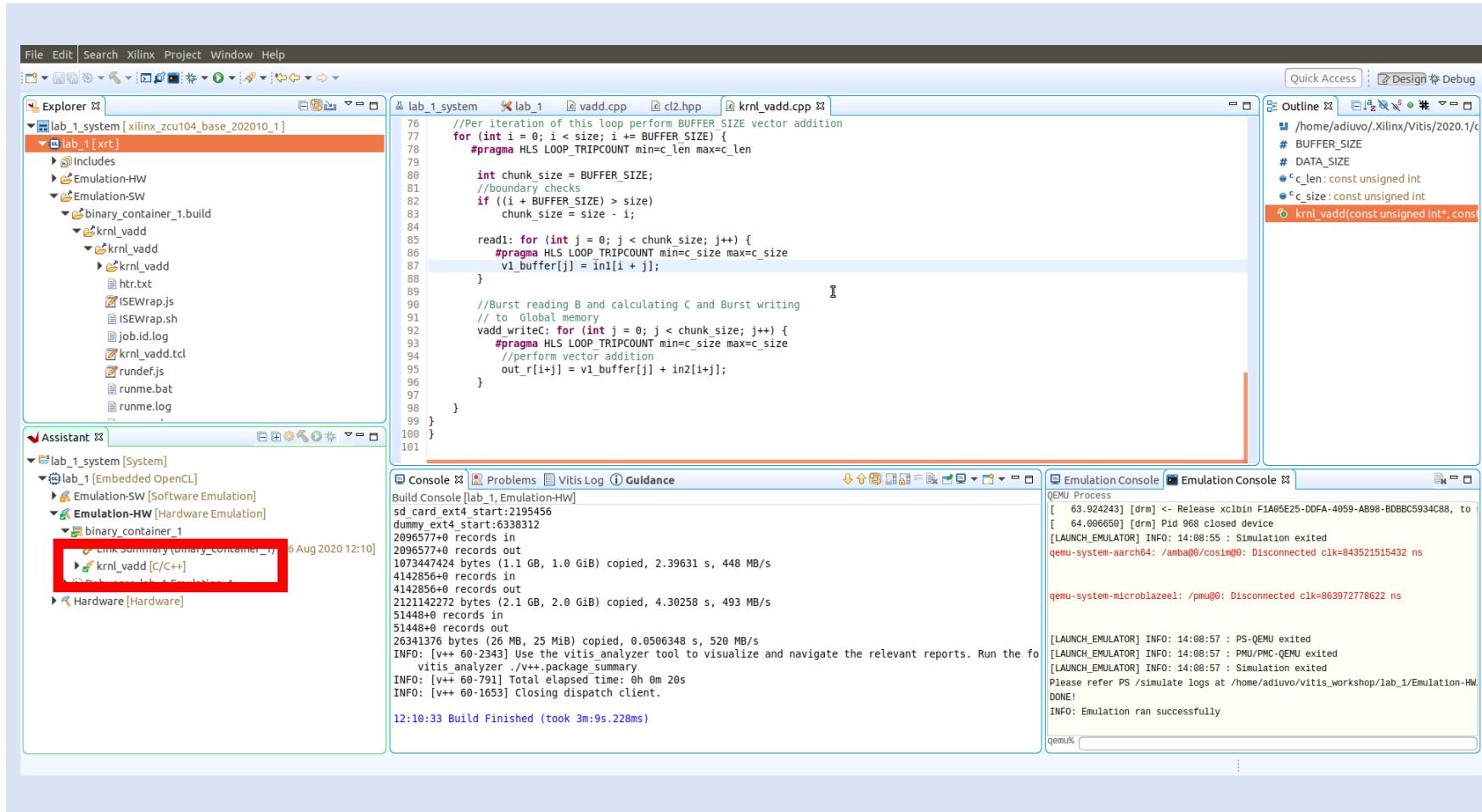
Lab 1: Understanding Vitis Project creation & Flow

Step 24 – Click on HLS Synthesis, this will show the performance of the accelerator, close the Vitis Analyser



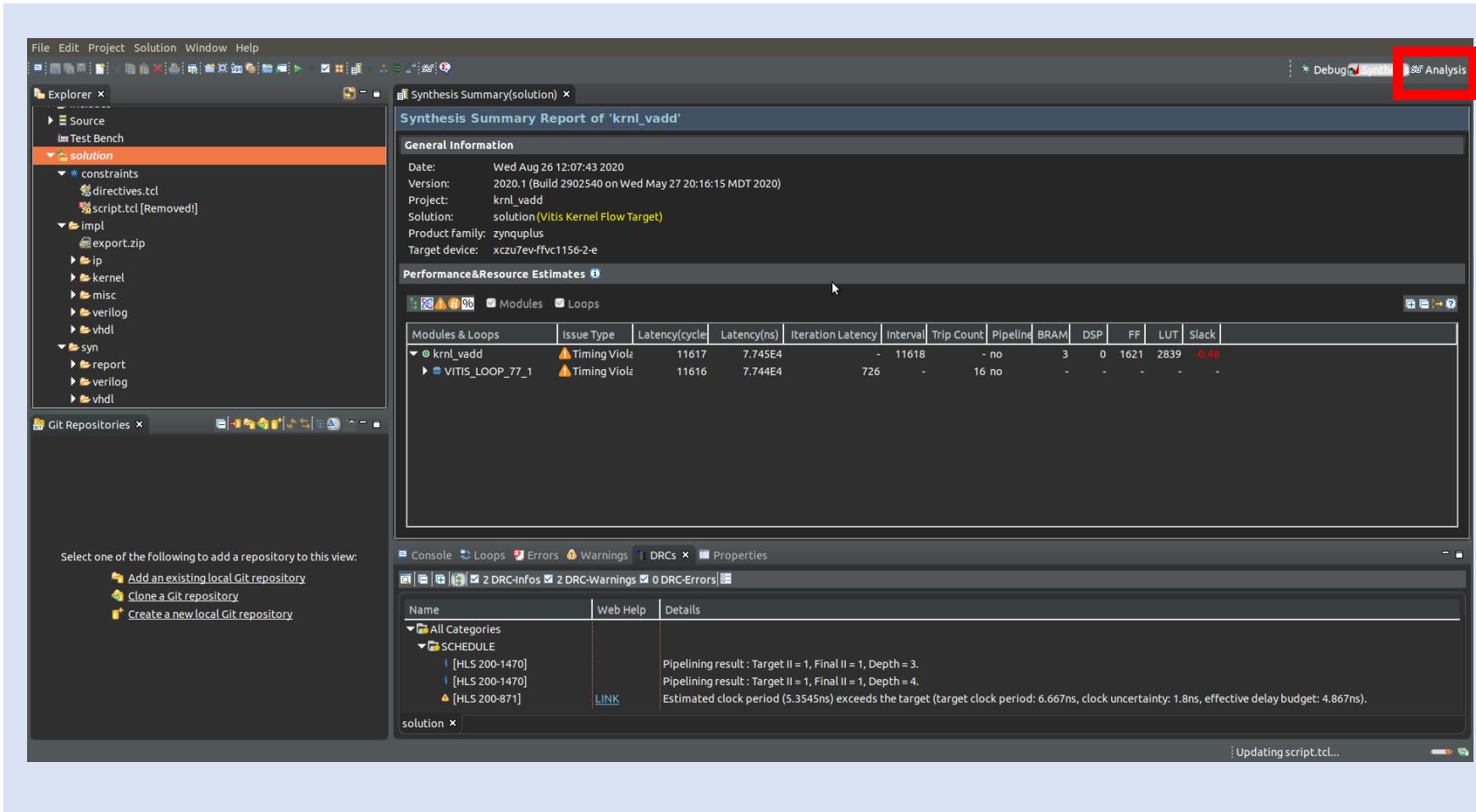
Lab 1: Understanding Vitis Project creation & Flow

Step 24 – Right Click on the krnl_vadd under the Assistant view and launch Vitis HLS.



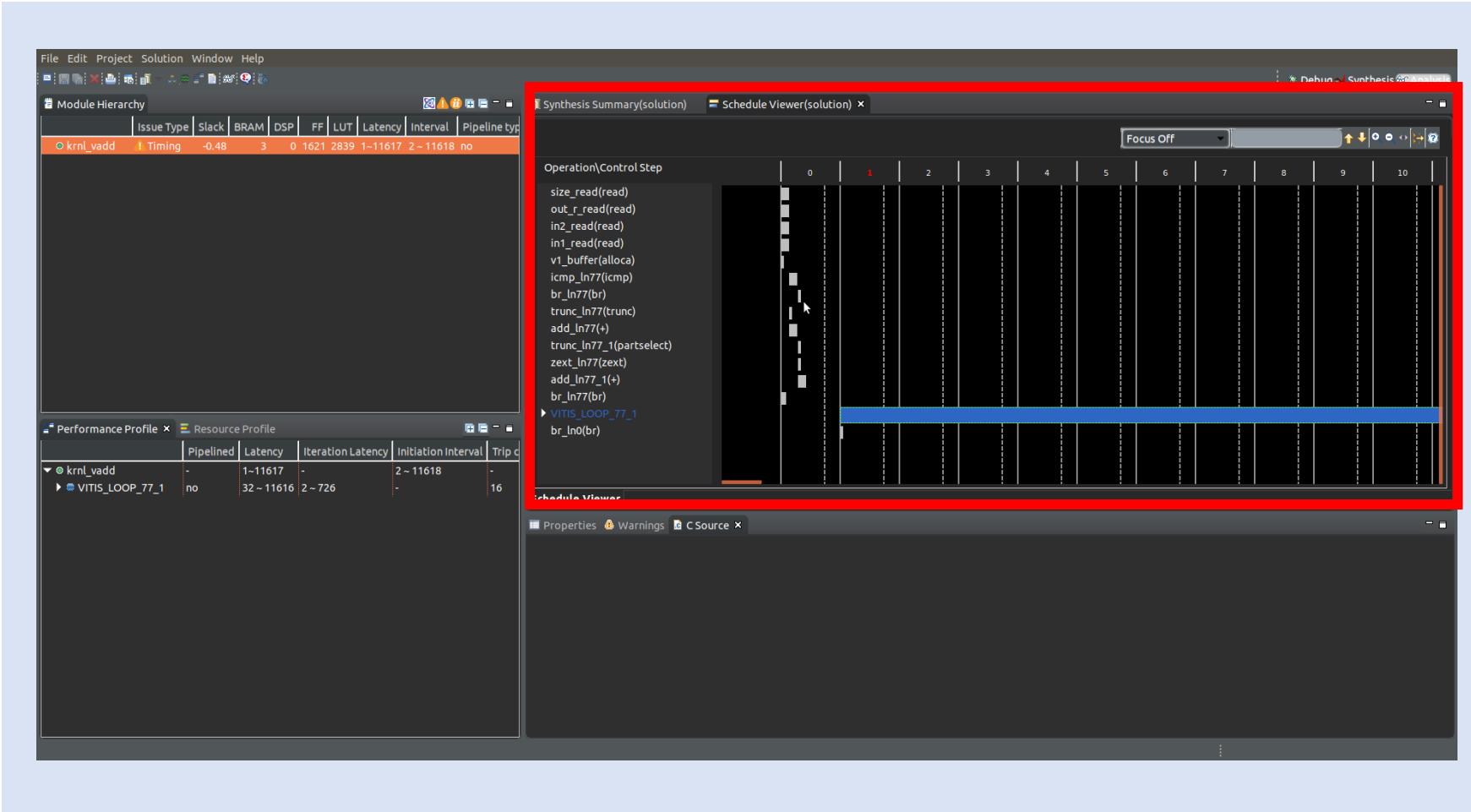
Lab 1: Understanding Vitis Project creation & Flow

Step 24 – This will open Vitis HLS project, click on Analysis View.



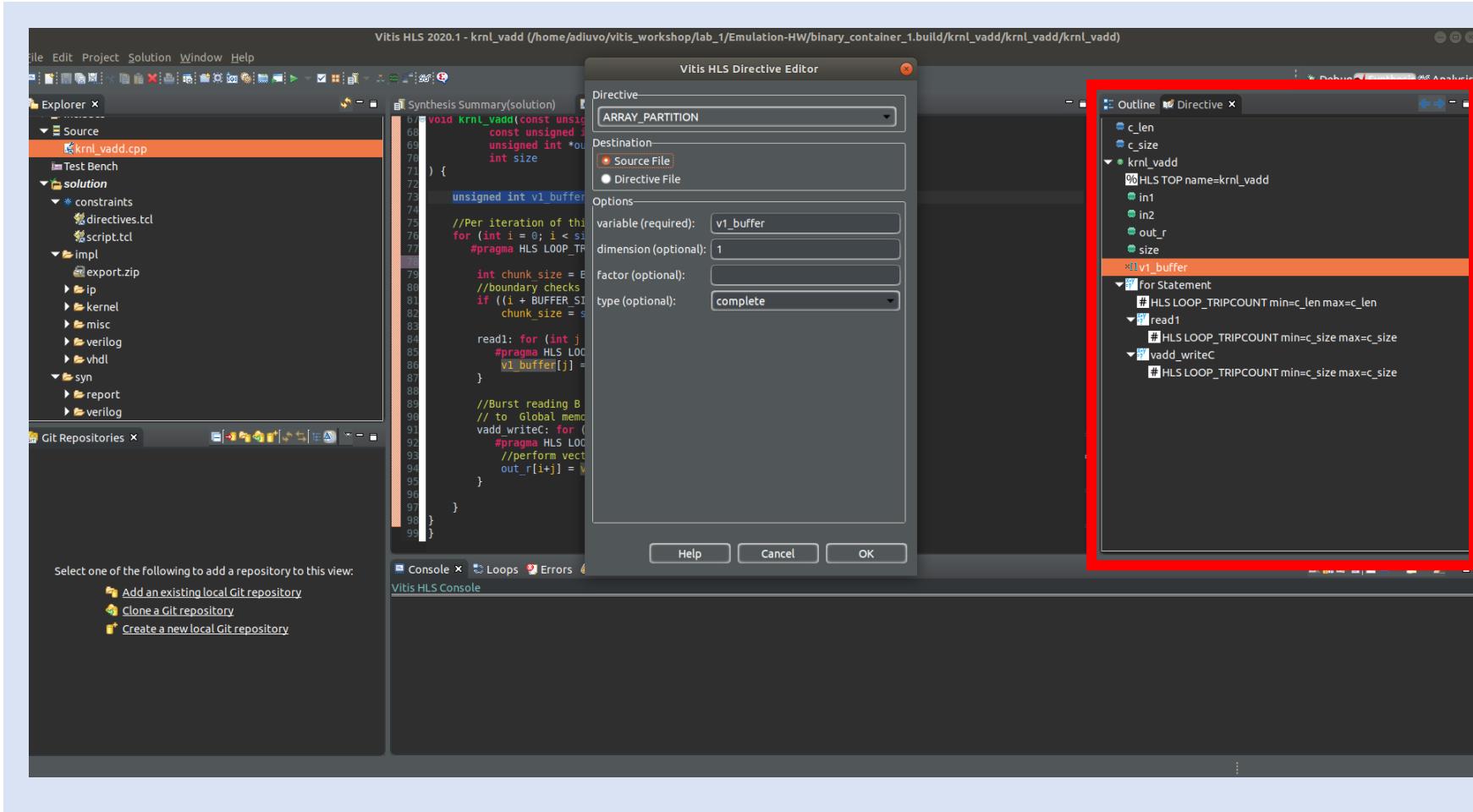
Lab 1: Understanding Vitis Project creation & Flow

Step 24 – This will open the schedule viewer; it is in this view we can cross probe to the C/C++ and determine what the bottle necks if any are. Explore the Analysis view then switch back the Synthesis View



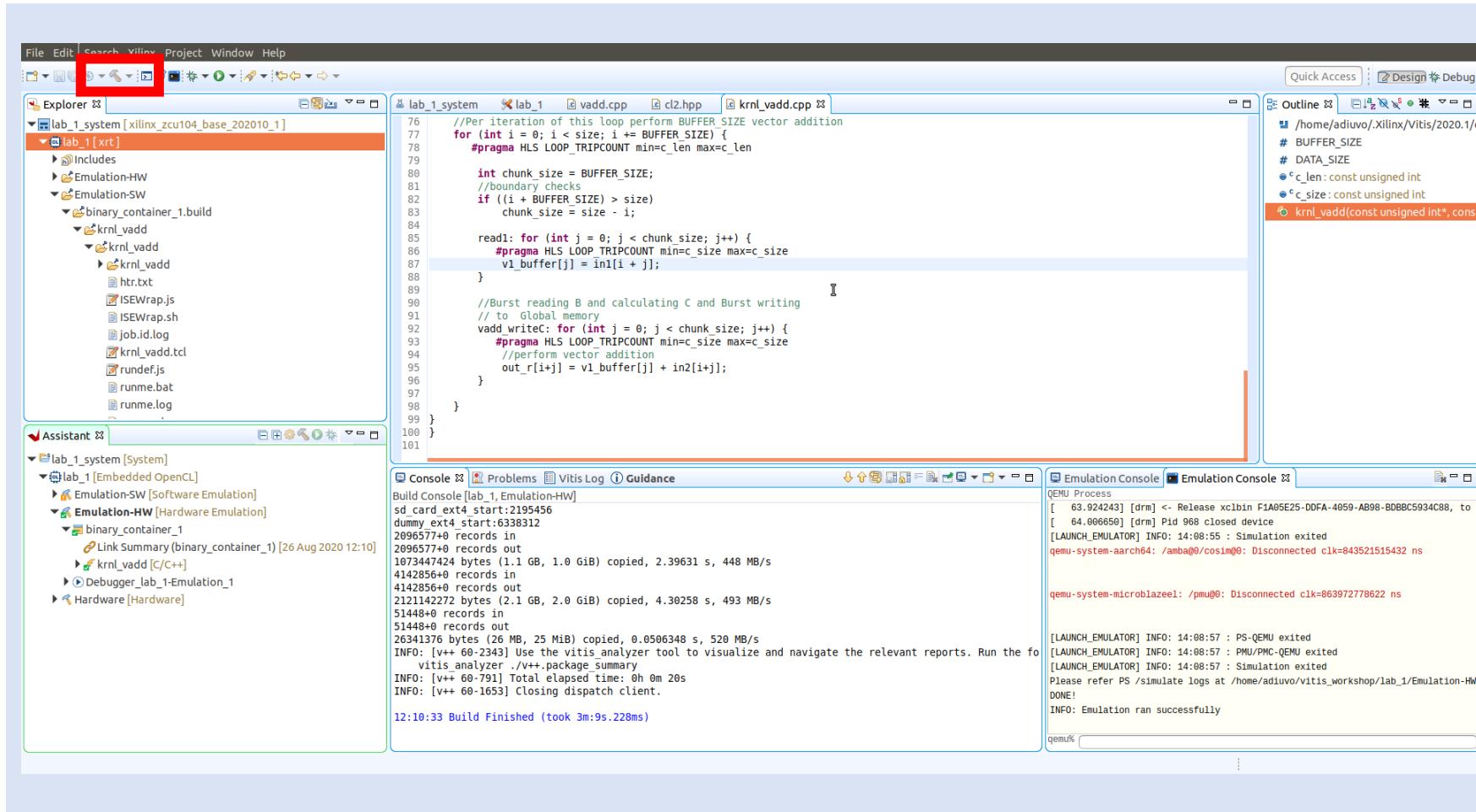
Lab 1: Understanding Vitis Project creation & Flow

Step 24 – If we want to add any optimizations, we can use the directive tab, double click on an element and then use the directive editor to add them to the source code. Explore the optimizations but click cancel and close Vitis HLS



Lab 1: Understanding Vitis Project creation & Flow

Step 24 – Back in Vitis, if we had made any changes in Vitis HLS we would need to rebuild the project.



Lab 1 Summary

The concludes lab 1, throughout this lab we have demonstrated

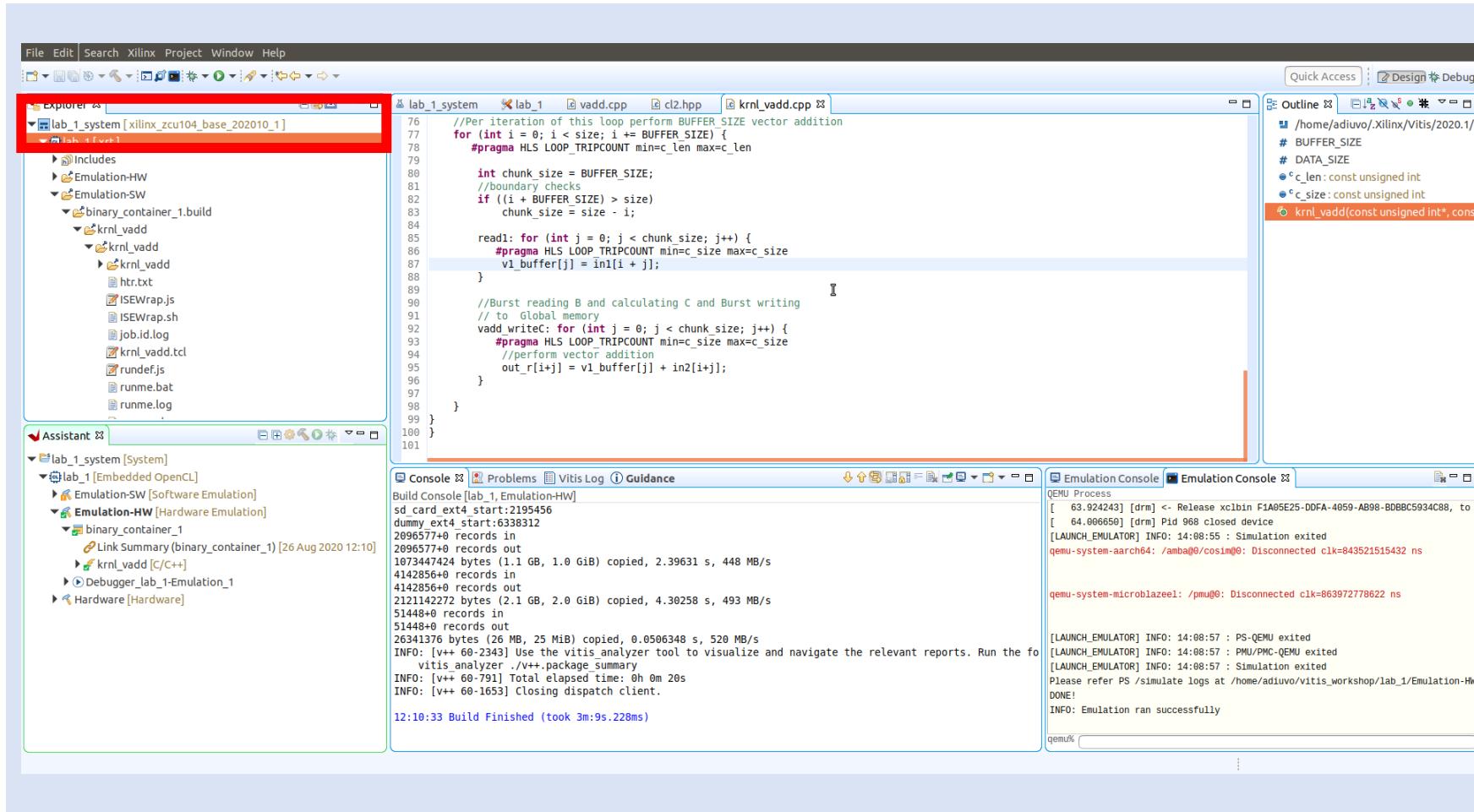
1. How to Open Vitis
2. How to create a project
3. How to Build & Debug a SW Emulation Flow – Including Breakpoints and Single Stepping
4. How to Build & Debug a HW Emulation Flow – Including Waveform
5. How to Examine the Vitis Analysis Report
6. How to work with accelerators kernels in Vitis HLS and Analyze bottle necks and add in pragma for optimizations.

Lab 2

Instantiating Xilinx Deep Learning Processor

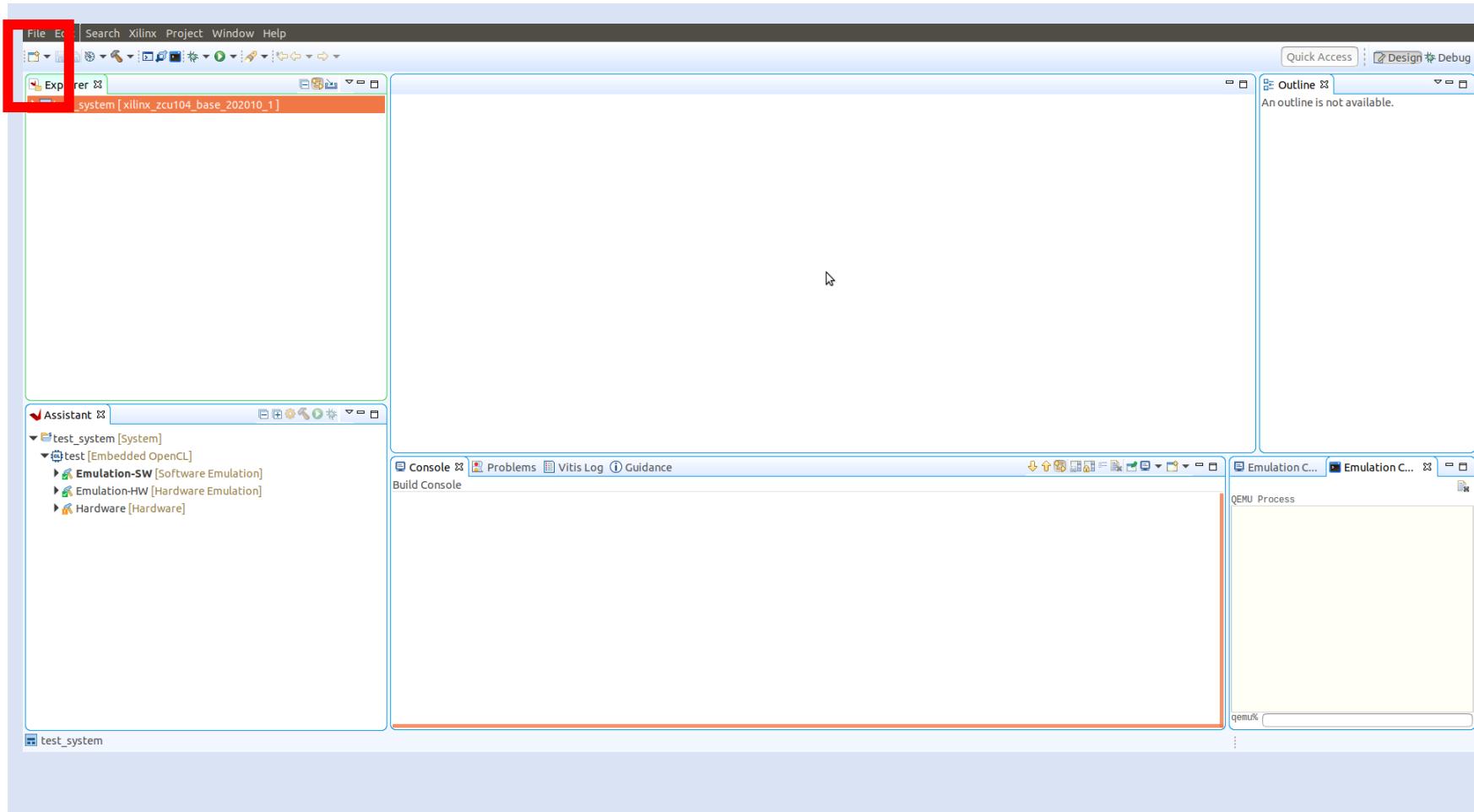
Lab 2: Instantiating Xilinx Deep Learning Processor —

Step 1 – Minimize the Lab_1_system project



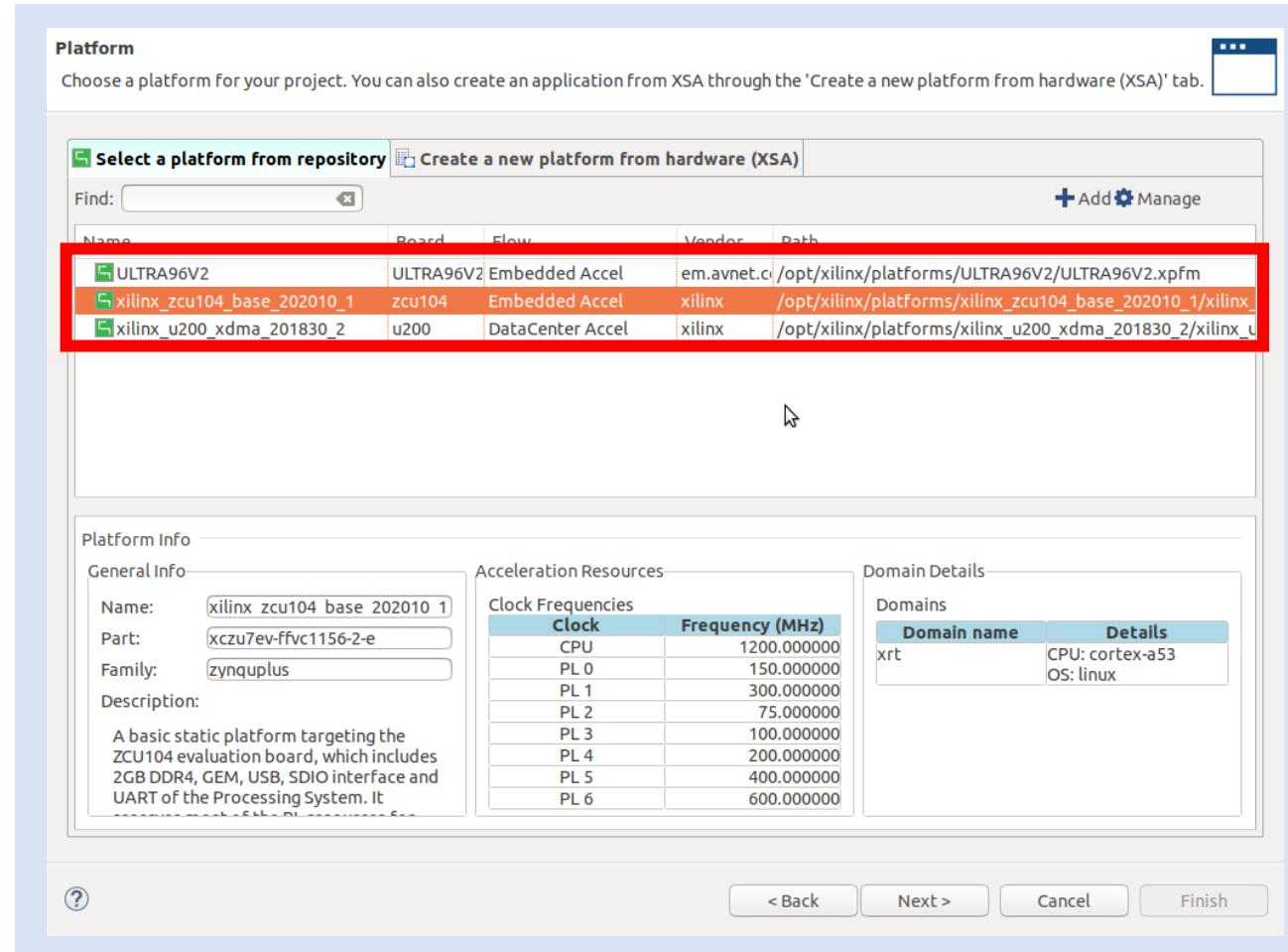
Lab 2: Instantiating Xilinx Deep Learning Processor

Step 2 – Click and create a new application project



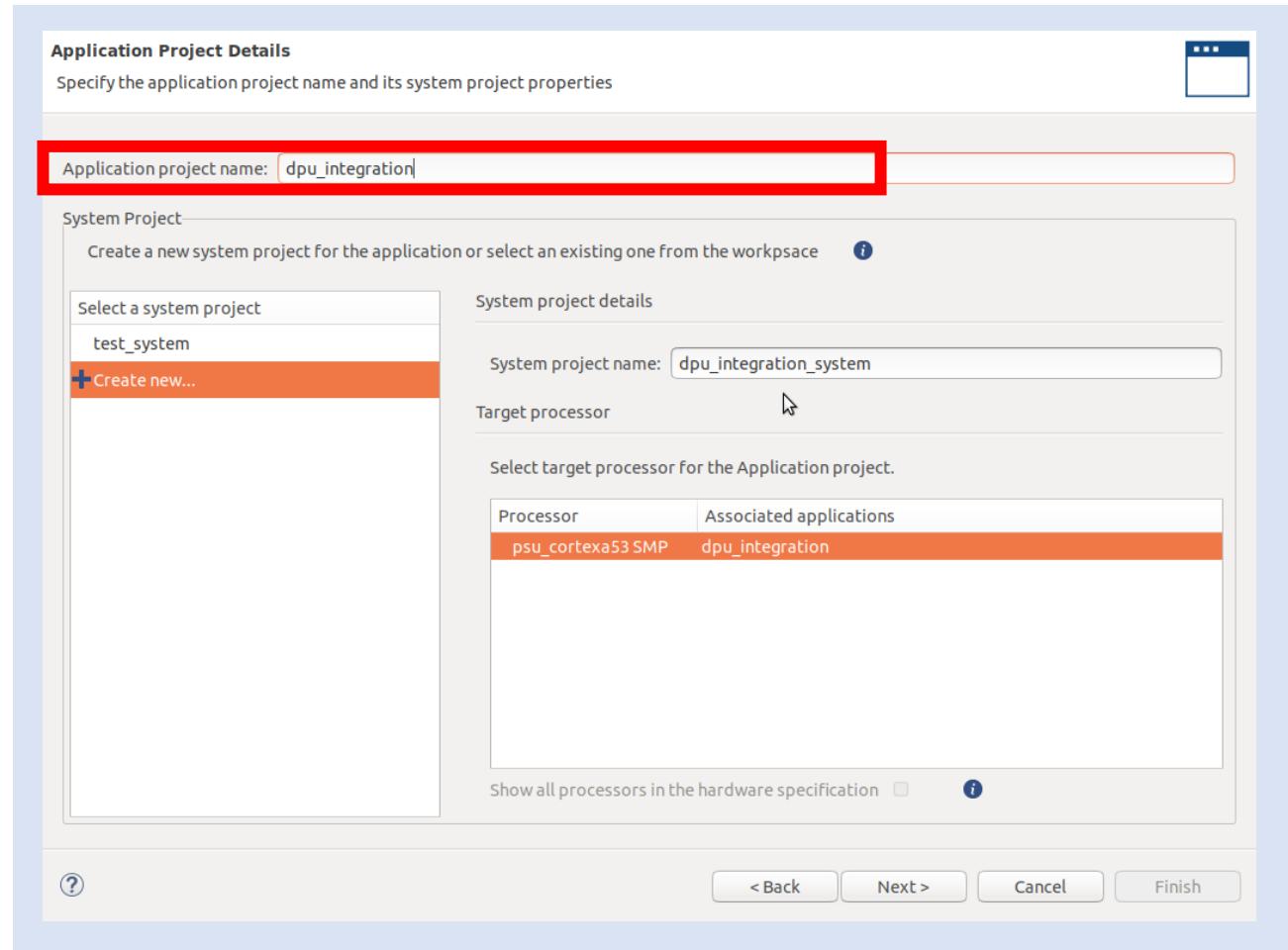
Lab 2: Instantiating Xilinx Deep Learning Processor

Step 3 – Select the platform you desire – for this example ZCU104 and click next



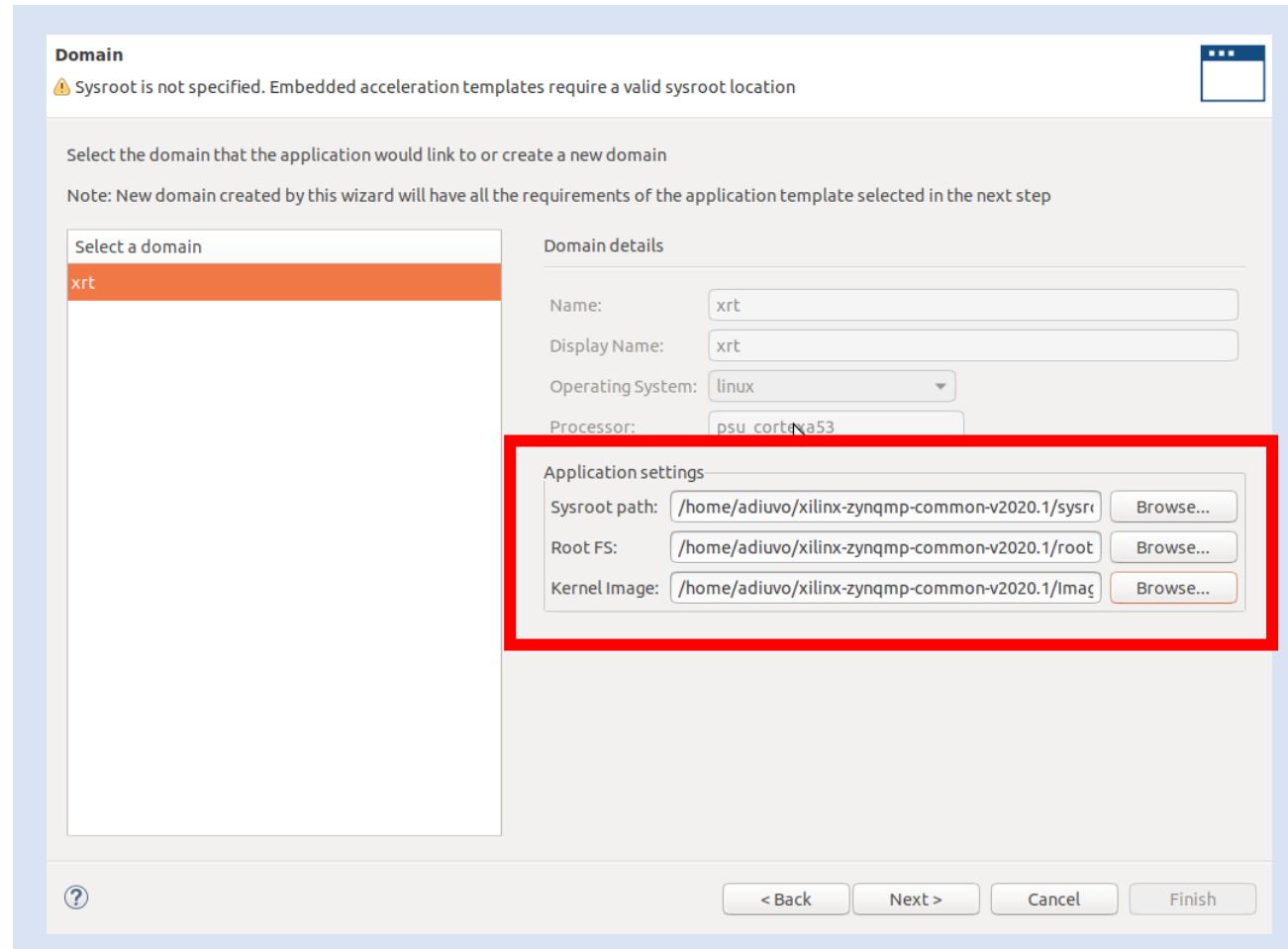
Lab 2: Instantiating Xilinx Deep Learning Processor

Step 4 – Enter a project name and click next



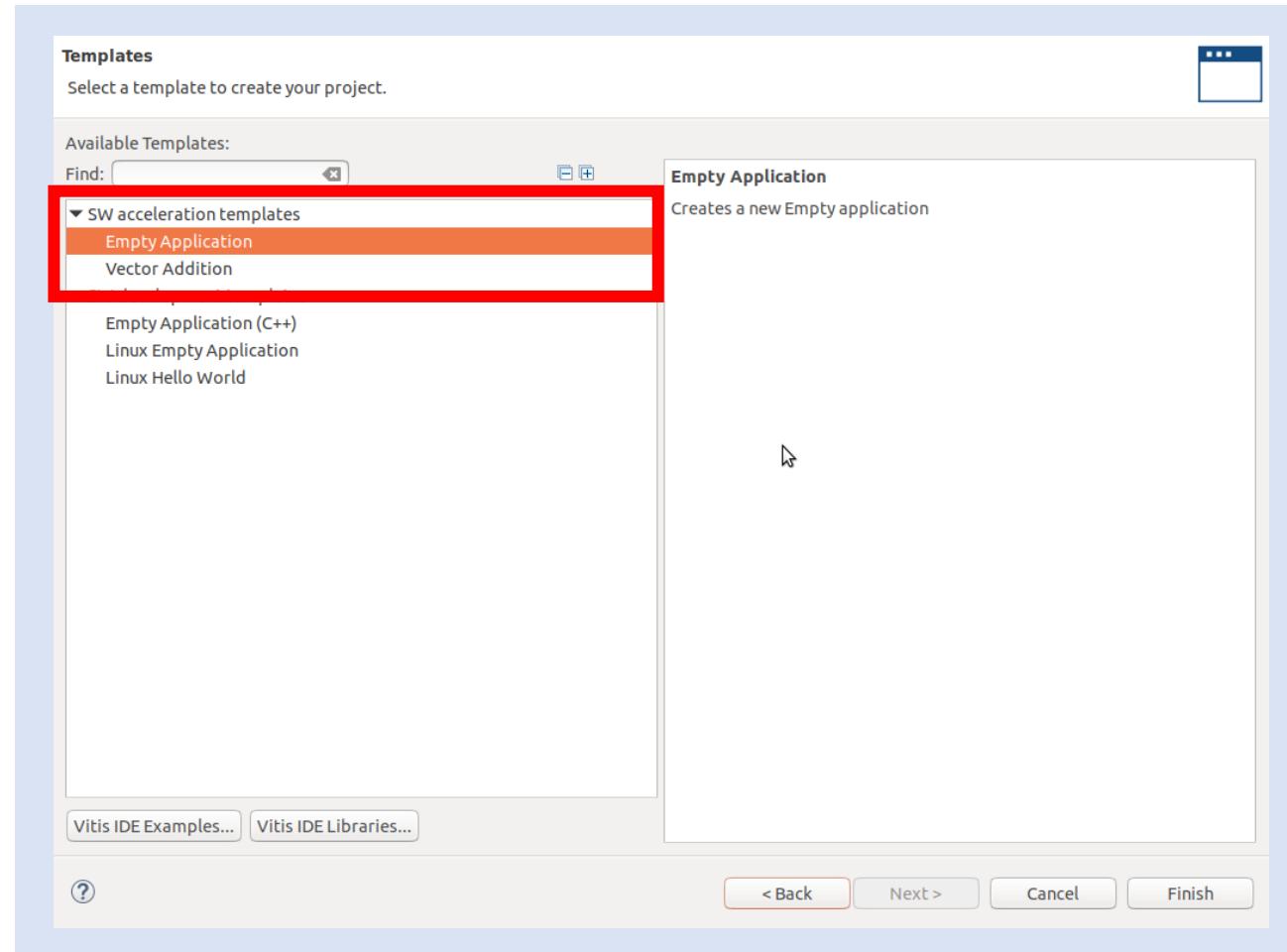
Lab 2: Instantiating Xilinx Deep Learning Processor

Step 5 – Enter the location of the SYSROOT, RootFS and Kernel Image



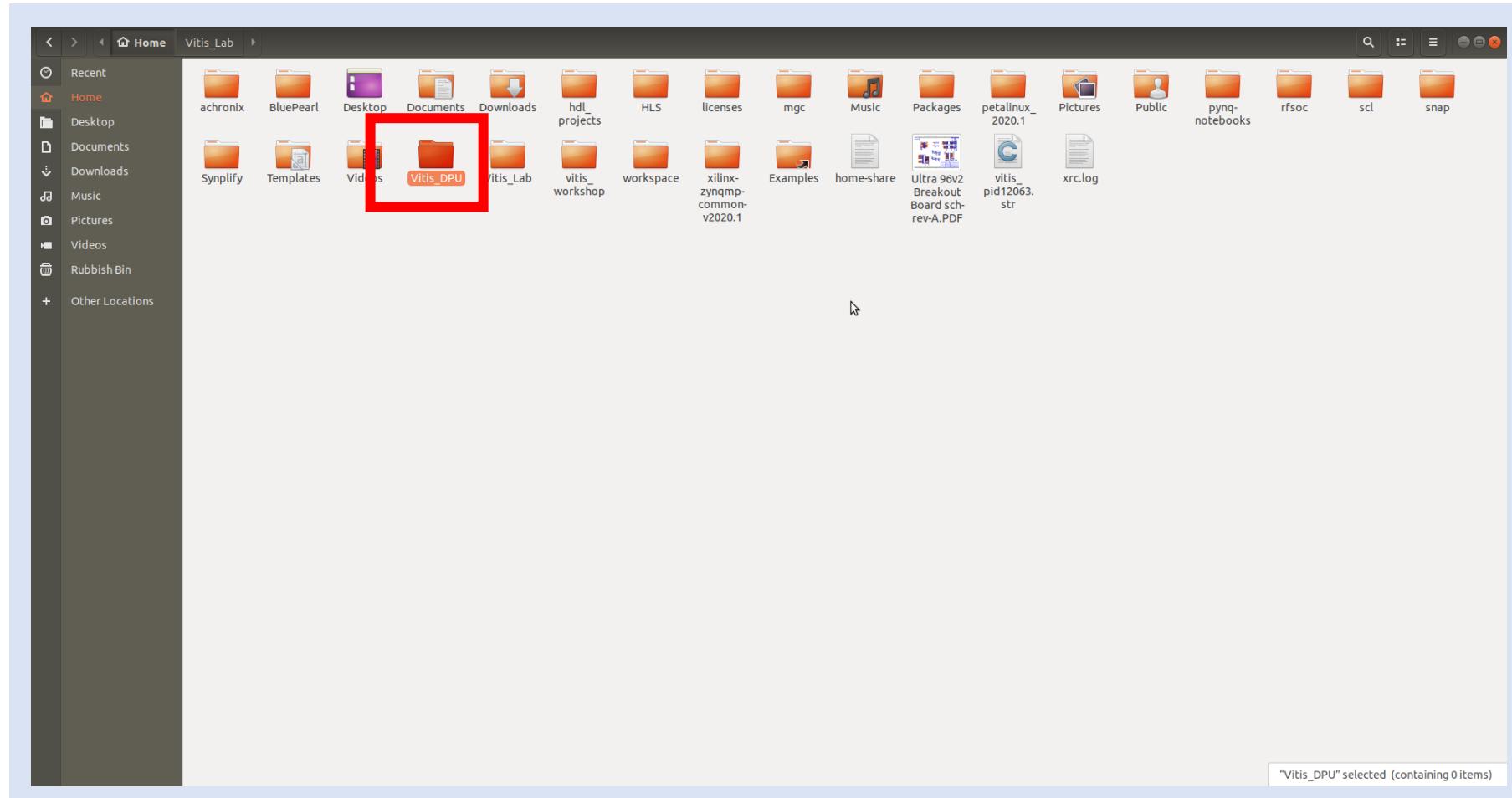
Lab 2: Instantiating Xilinx Deep Learning Processor

Step 6 – Select Empty Application and click on finish



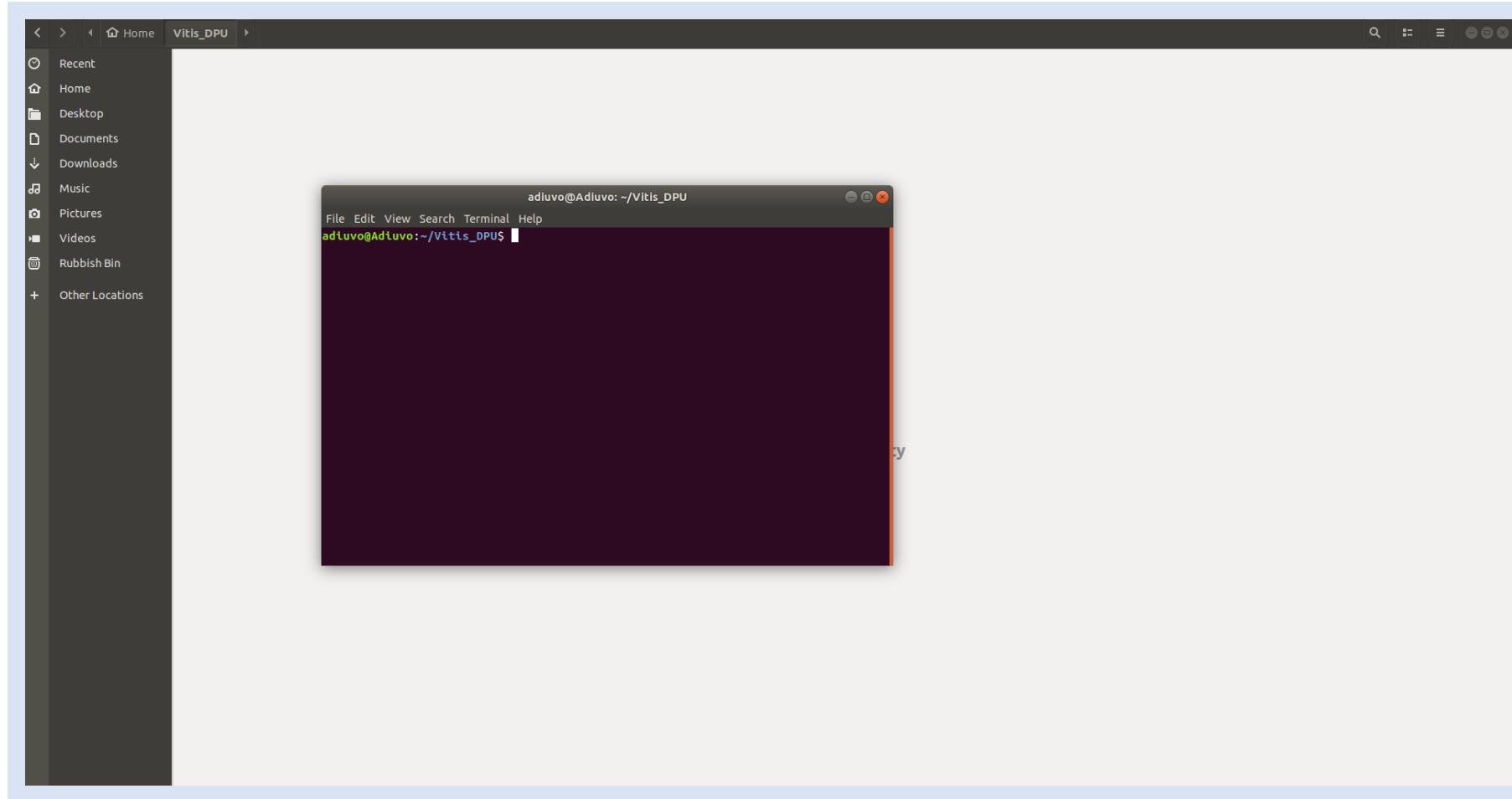
Lab 2: Instantiating Xilinx Deep Learning Processor

Step 7 – Create a new directory in your preferred directory – for example Vitis_DPU



Lab 2: Instantiating Xilinx Deep Learning Processor

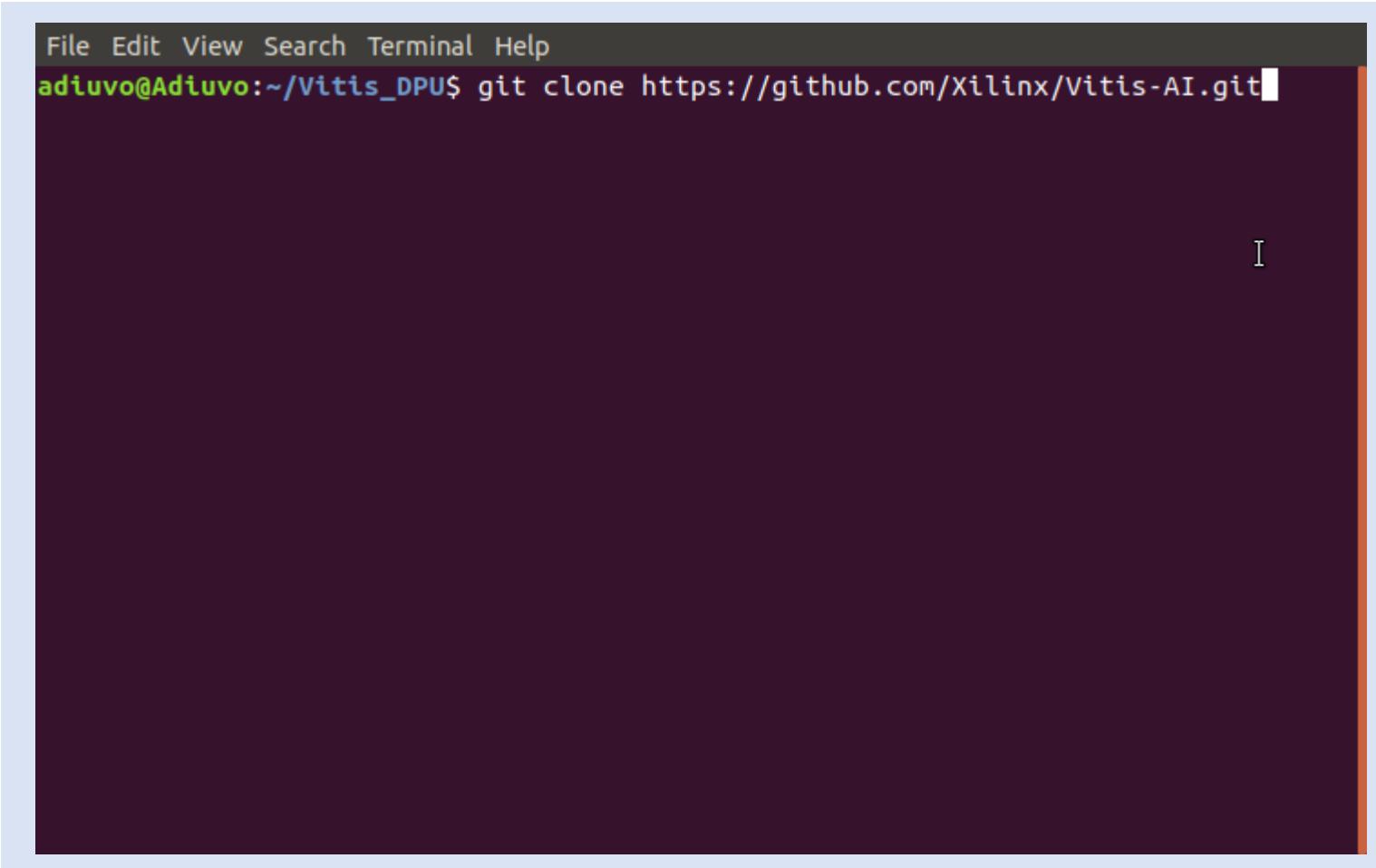
Step 8 – Change directory into the new folder – Open a new terminal in that folder



Lab 2: Instantiating Xilinx Deep Learning Processor

Step 9 – Clone the Vitis-AI github with the command

```
git clone https://github.com/Xilinx/Vitis-AI.git
```

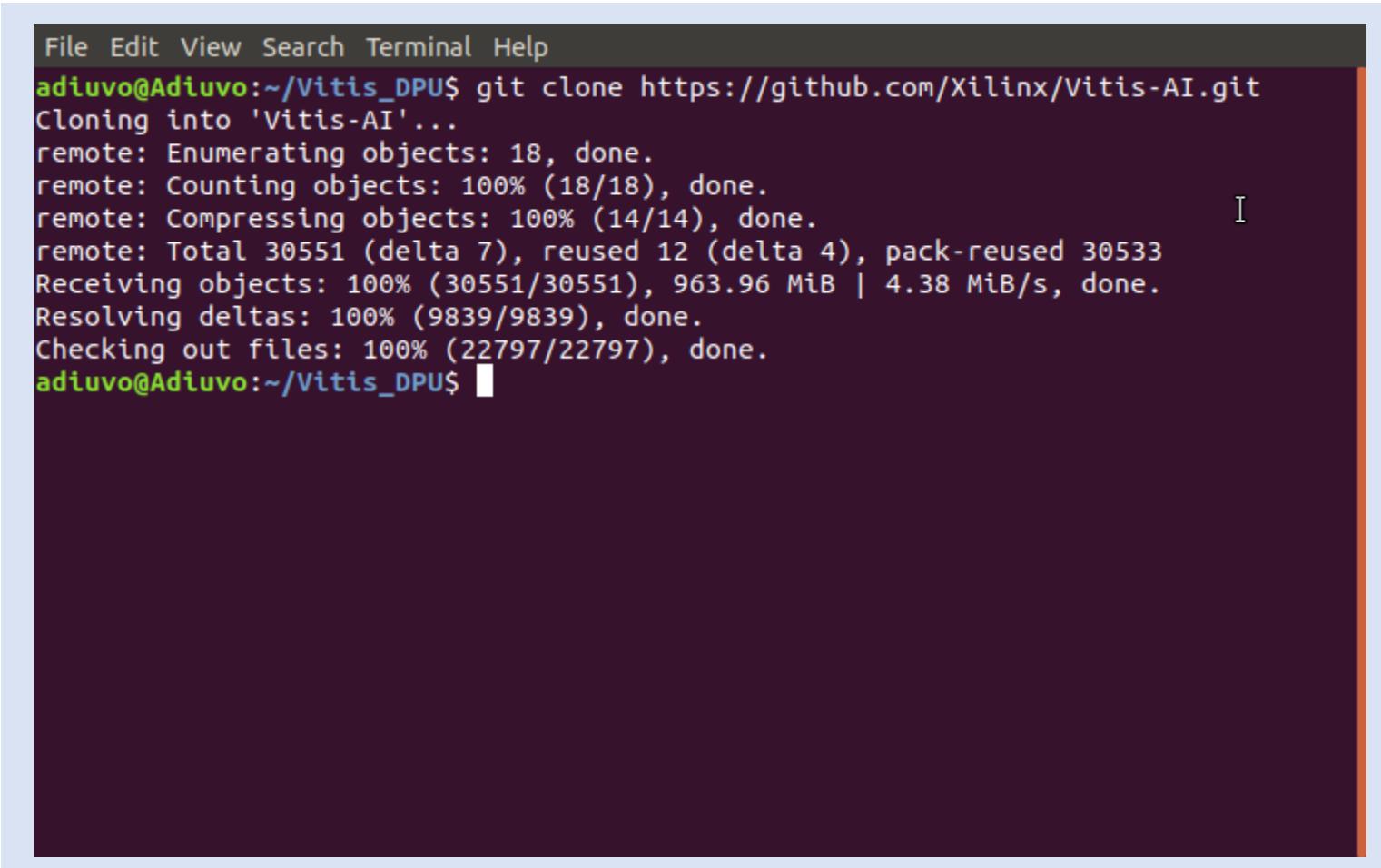


A screenshot of a terminal window with a dark background and light-colored text. The window title bar includes 'File Edit View Search Terminal Help'. The command 'git clone https://github.com/Xilinx/Vitis-AI.git' is typed into the terminal, with the cursor at the end of the URL. The terminal is running on a Linux system named 'adiuvo'.

```
File Edit View Search Terminal Help  
adiuvo@Adiuvo:~/Vitis_DPU$ git clone https://github.com/Xilinx/Vitis-AI.git
```

Lab 2: Instantiating Xilinx Deep Learning Processor

Step 10 – This will clone the Vitis-AI tool

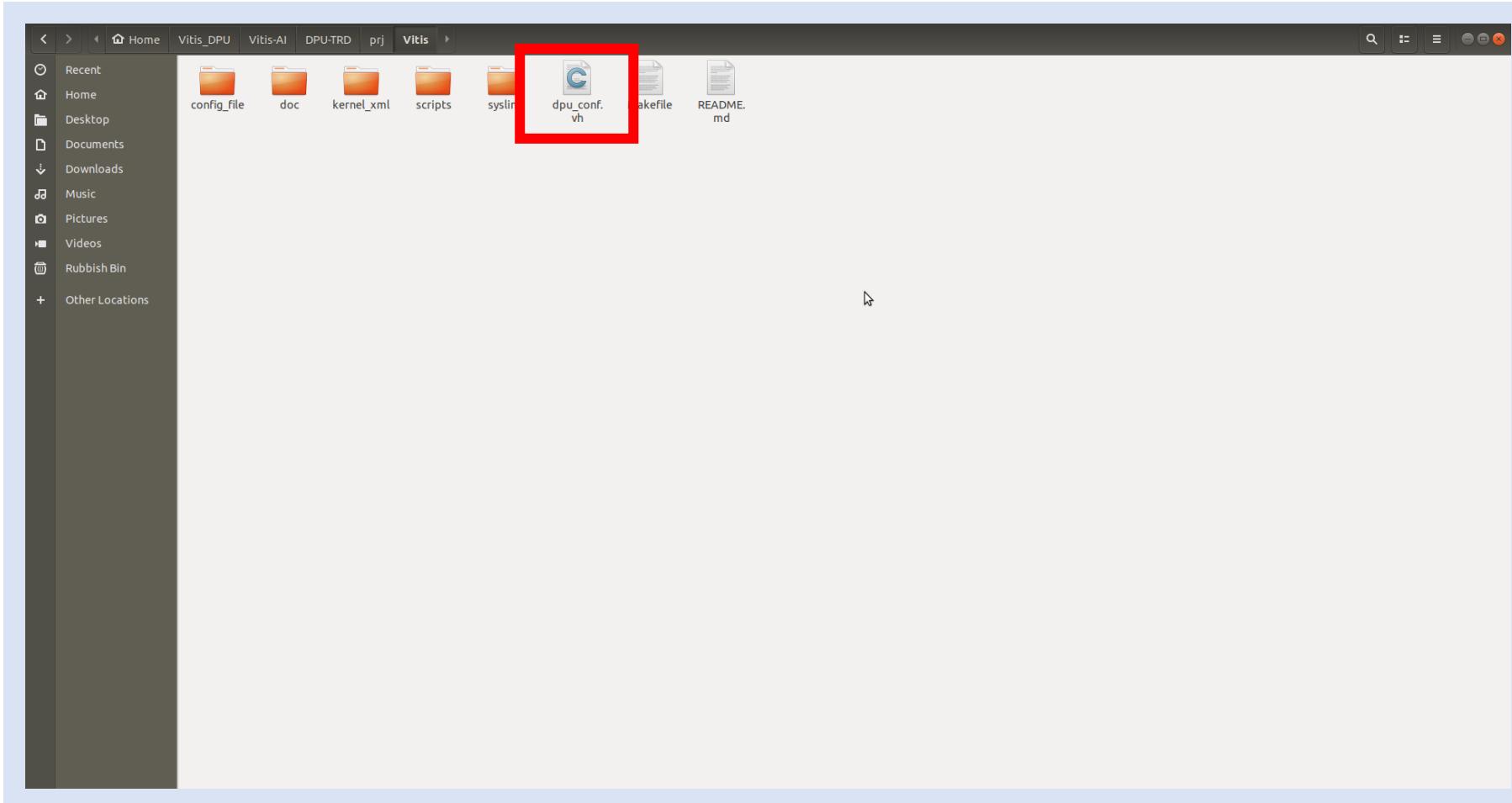


A terminal window showing the output of a `git clone` command. The command is `git clone https://github.com/Xilinx/Vitis-AI.git`. The output shows the progress of cloning, including object enumeration, counting, compressing, and receiving objects from the remote repository. The process is completed successfully.

```
File Edit View Search Terminal Help
adiuvo@Adiubo:~/Vitis_DPU$ git clone https://github.com/Xilinx/Vitis-AI.git
Cloning into 'Vitis-AI'...
remote: Enumerating objects: 18, done.
remote: Counting objects: 100% (18/18), done.
remote: Compressing objects: 100% (14/14), done.
remote: Total 30551 (delta 7), reused 12 (delta 4), pack-reused 30533
Receiving objects: 100% (30551/30551), 963.96 MiB | 4.38 MiB/s, done.
Resolving deltas: 100% (9839/9839), done.
Checking out files: 100% (22797/22797), done.
adiuvo@Adiubo:~/Vitis_DPU$
```

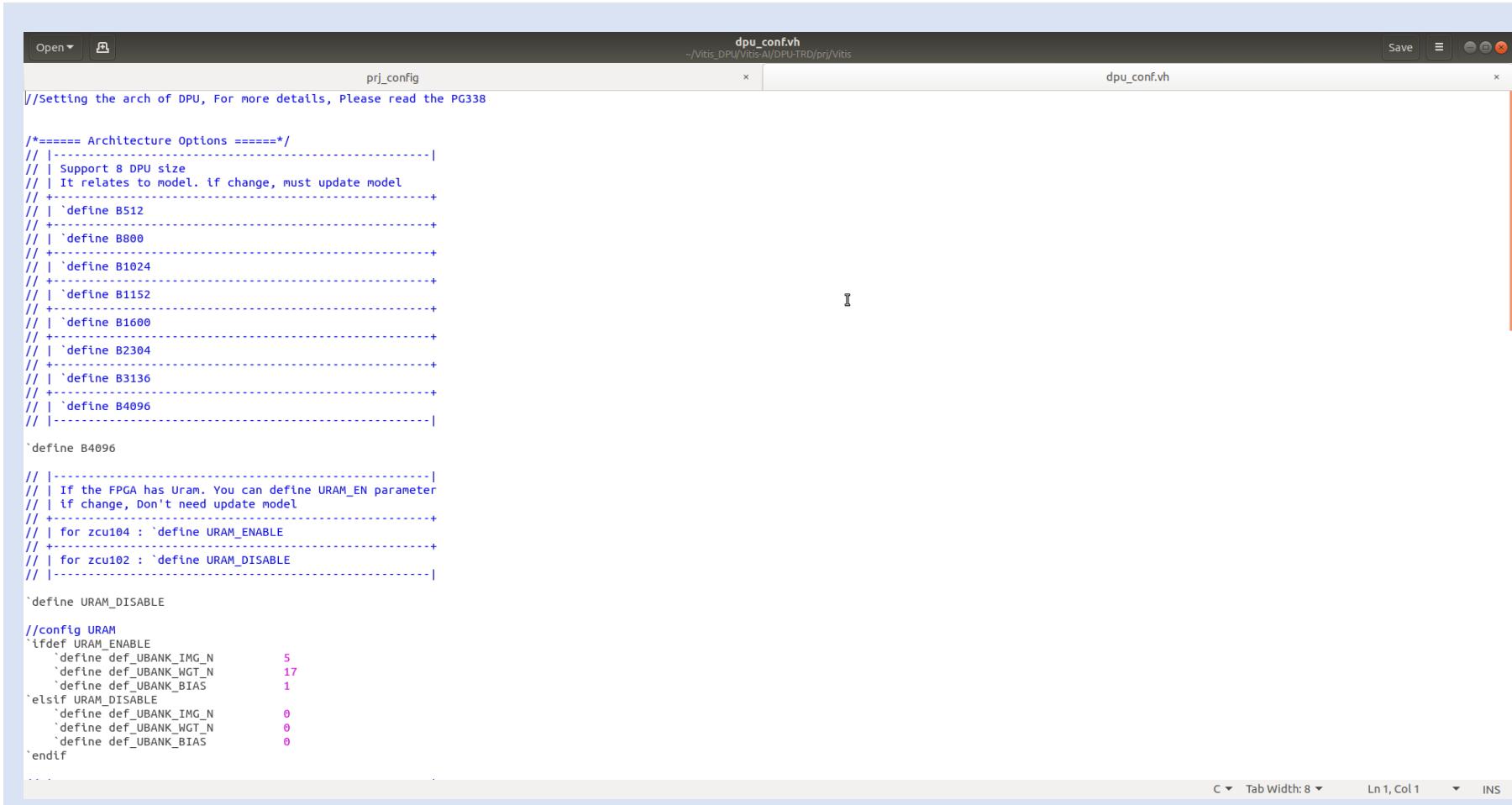
Lab 2: Instantiating Xilinx Deep Learning Processor —

Step 11 – Change directory into the Vitis-AI/DPU-TRD/prj/Vitis and open dpu_conf.vh



Lab 2: Instantiating Xilinx Deep Learning Processor —

Step 12 – to configure the DPU we use dpu_conf.vh – examine the file and close it



```
//Setting the arch of DPU, For more details, Please read the PG338

/*===== Architecture Options =====*/
// |-----|
// | Support 8 DPU size
// | It relates to model. if change, must update model
// +-----+
// | `define B512
// +-----+
// | `define B800
// +-----+
// | `define B1024
// +-----+
// | `define B1152
// +-----+
// | `define B1600
// +-----+
// | `define B2304
// +-----+
// | `define B3136
// +-----+
// | `define B4096
// +-----+
`define B4096

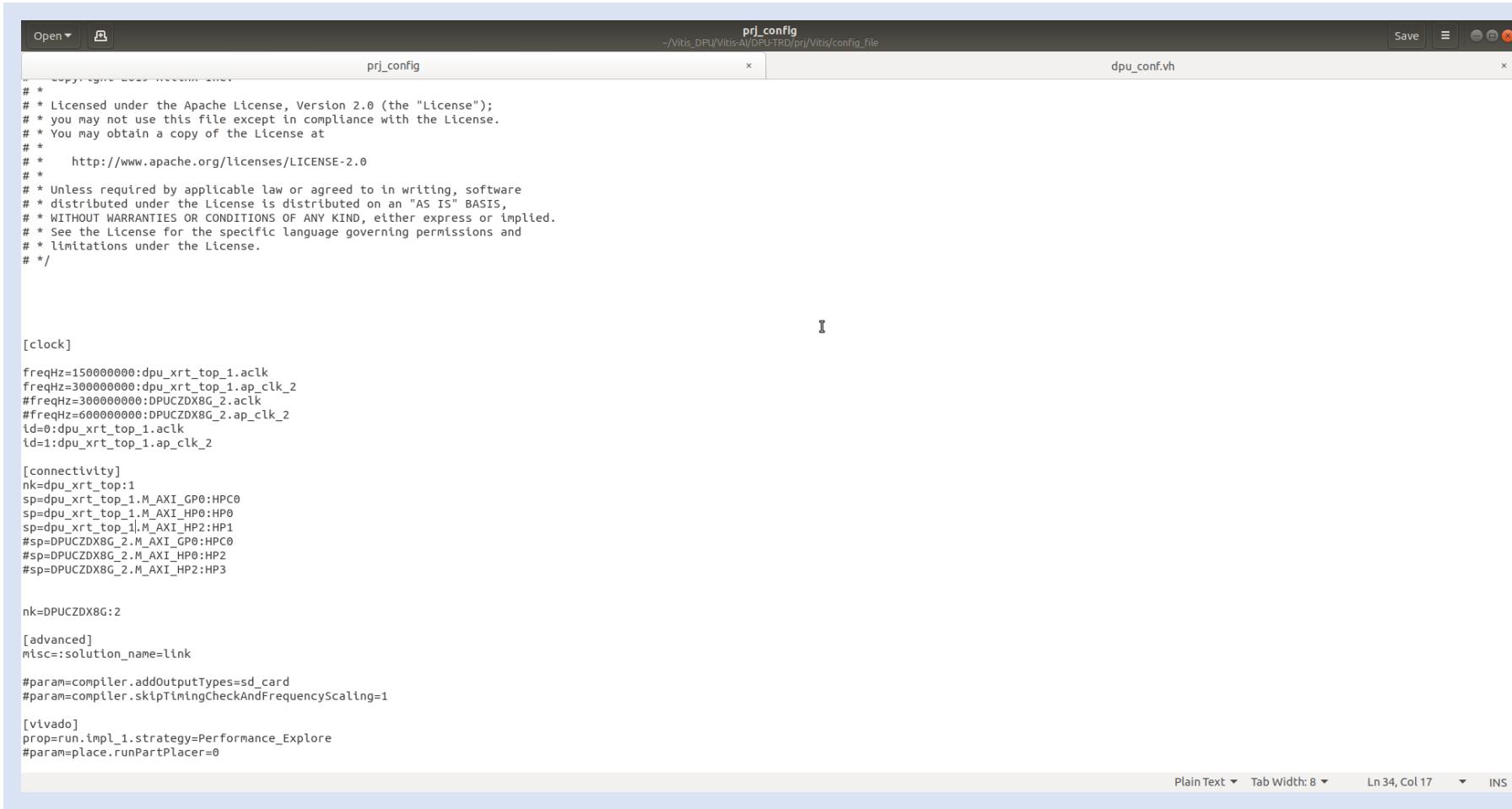
// |-----|
// | If the FPGA has Uram. You can define URAM_EN parameter
// | if change, Don't need update model
// +-----+
// | for zcu104 : `define URAM_ENABLE
// +-----+
// | for zcu102 : `define URAM_DISABLE
// +-----+

`define URAM_DISABLE

//config URAM
`ifdef URAM_ENABLE
    `define def_UBANK_IMG_N      5
    `define def_UBANK_WGT_N     17
    `define def_UBANK_BIAS       1
`elsif URAM_DISABLE
    `define def_UBANK_IMG_N      0
    `define def_UBANK_WGT_N      0
    `define def_UBANK_BIAS       0
`endiff
`endif
```

Lab 2: Instantiating Xilinx Deep Learning Processor

Step 13 – Change directory to the config_file open the file prj_config for editing – update the file to be as shown below



The screenshot shows a text editor window titled "prj_config" with the path "-/Vitis_DPU/Vitis-AI/DPU-TRD/prj/Vitis/config_file". The editor has two tabs: "prj_config" and "dpu_conf.vh". The "prj_config" tab contains configuration parameters for the DPU. The code is as follows:

```
# * Licensed under the Apache License, Version 2.0 (the "License");
# * you may not use this file except in compliance with the License.
# * You may obtain a copy of the License at
# *
# *     http://www.apache.org/licenses/LICENSE-2.0
# *
# * Unless required by applicable law or agreed to in writing, software
# * distributed under the License is distributed on an "AS IS" BASIS,
# * WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
# * See the License for the specific language governing permissions and
# * limitations under the License.
# */

[clock]
freqHz=150000000:dpu_xrt_top_1.aclk
freqHz=300000000:dpu_xrt_top_1.ap_clk_2
#freqHz=300000000:DPUCZDX8G_2.aclk
#freqHz=600000000:DPUCZDX8G_2.ap_clk_2
id=0:dpu_xrt_top_1.aclk
id=1:dpu_xrt_top_1.ap_clk_2

[connectivity]
nk=dpu_xrt_top:1
sp=dpu_xrt_top_1.M_AXI_GPO:HPC0
sp=dpu_xrt_top_1.M_AXI_HPO:HPO
sp=dpu_xrt_top_1.M_AXI_HP2:HP1
#sp=DPUCZDX8G_2.M_AXI_GPO:HPC0
#sp=DPUCZDX8G_2.M_AXI_HPO:HP2
#sp=DPUCZDX8G_2.M_AXI_HP2:HP3

nk=DPUCZDX8G:2

[advanced]
misc=:solution_name=link

#param=compiler.addOutputTypes=sd_card
#param=compiler.skipTimingCheckAndFrequencyScaling=1

[vivado]
prop=run.impl_1.strategy=Performance_Explore
#param=place.RunPartPlacer=0
```

The bottom of the editor shows status bars for "Plain Text", "Tab Width: 8", "Ln 34, Col 17", and "INS".

Lab 2: Instantiating Xilinx Deep Learning Processor

Step 14 – In the terminal window export the platform location and make the XO

export SDX_PLATFORM=<location>

make binary_container_1/dpu.xo DEVICE=zcu104

```

File Edit View Search Terminal Help
adiuvo@Adiuvo:~/Vitis_DPU/Vitis-AI/DPU-TRD/prj/Vitis$ export SDX_PLATFORM=/opt/xilinx/platforms/xilinx_zcu104_base_202010_1/xilinx_zcu104_base_202010_1.xpfm
adiuvo@Adiuvo:~/Vitis_DPU/Vitis-AI/DPU-TRD/prj/Vitis$ echo $SDX_PLATFORM
/opt/xilinx/platforms/xilinx_zcu104_base_202010_1/xilinx_zcu104_base_202010_1.xpfm
adiuvo@Adiuvo:~/Vitis_DPU/Vitis-AI/DPU-TRD/prj/Vitis$ make binary_container_1/dpu.xo DEVICE=zcu104
/tools/Xilinx/Vivado/2020.1/bin/vivado -mode batch -source scripts/gen_dpu_xo.tcl -tclargs binary_container_1/dpu.xo DPUCZDX8G hw zcu104

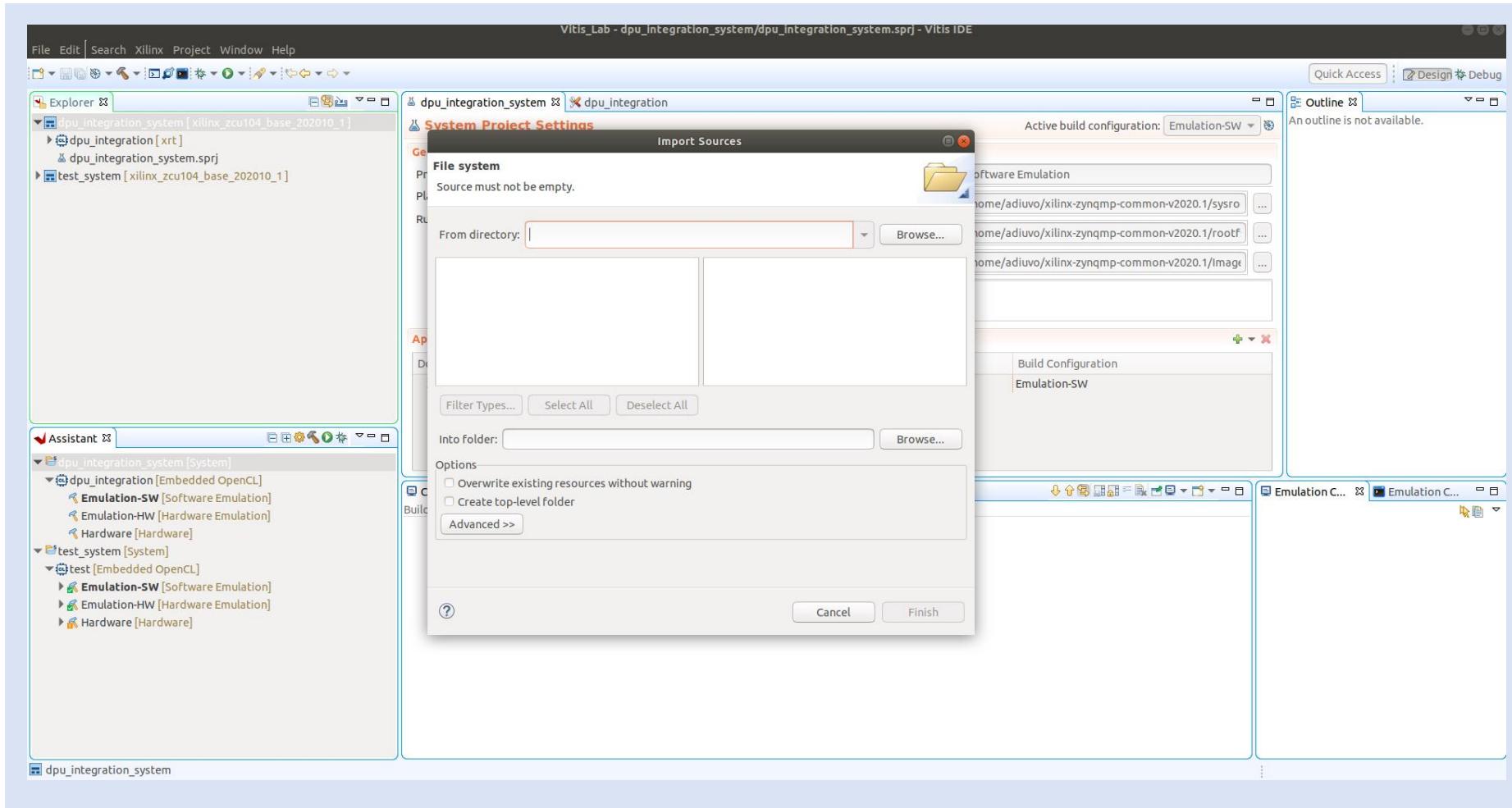
***** Vivado v2020.1 (64-bit)
**** SW Build 2902540 on Wed May 27 19:54:35 MDT 2020
**** IP Build 2902112 on Wed May 27 22:43:36 MDT 2020
** Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.

source scripts/gen_dpu_xo.tcl
# if { $::argc != 4 } {
#   puts "ERROR: Program \"$::argv0\" requires 4 arguments!\n"
#   puts "Usage: $::argv0 <xoname> <krnl_name> <target> <device>\n"
#   exit
# }
# set xoname [lindex $::argv 0]
# set krnl_name [lindex $::argv 1]
# set target [lindex $::argv 2]
# set device [lindex $::argv 3]
# set suffix "${krnl_name}_${target}_${device}"
# source -notrace ./scripts/package_dpu_kernel.tcl
INFO: [IP_Flow 19-5654] Module 'DPUCZDX8G' uses SystemVerilog sources with a Verilog top file. These SystemVerilog files will not be analysed by the packager.
INFO: [IP_Flow 19-1842] HDL Parser: Found include file "src/arch_def.vh" from the top-level HDL file.
INFO: [IP_Flow 19-1842] HDL Parser: Found include file "/home/adiuvo/Vitis_DPU/Vitis-AI/DPU-TRD/prj/Vitis/dpu_conf.vh" from the top-level HDL file.
INFO: [IP_Flow 19-1841] HDL Parser: Add include file "/home/adiuvo/Vitis_DPU/Vitis-AI/DPU-TRD/prj/Vitis/dpu_conf.vh" to file group xilinx_anylanguagesynthesis.
INFO: [IP_Flow 19-1841] HDL Parser: Add include file "/home/adiuvo/Vitis_DPU/Vitis-AI/DPU-TRD/prj/Vitis/dpu_conf.vh" to file group xilinx_anylanguagbehalorsimulation.
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No User IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2020.1/data/ip'.
INFO: [IP_Flow 19-5107] Inferred bus interface 'aclk' of definition 'xilinx.com:signal:clock:1.0' (from X_INTERFACE_INFO parameter from HDL file).
INFO: [IP_Flow 19-5107] Inferred bus interface 'aclk' of definition 'xilinx.com:signal:clock:1.0' (from 'X_INTERFACE_INFO' attribute).
INFO: [IP_Flow 19-5107] Inferred bus interface 'ap_clk_2' of definition 'xilinx.com:signal:clock:1.0' (from X_INTERFACE_INFO parameter from HDL file).
INFO: [IP_Flow 19-5107] Inferred bus interface 'ap_clk_2' of definition 'xilinx.com:signal:clock:1.0' (from 'X_INTERFACE_INFO' attribute).
INFO: [IP_Flow 19-5107] Inferred bus interface 'ap_rst_n_2' of definition 'xilinx.com:signal:reset:1.0' (from X_INTERFACE_INFO parameter from HDL file).
INFO: [IP_Flow 19-5107] Inferred bus interface 'ap_rst_n_2' of definition 'xilinx.com:signal:reset:1.0' (from 'X_INTERFACE_INFO' attribute).
INFO: [IP_Flow 19-5107] Inferred bus interface 'aresetn' of definition 'xilinx.com:signal:reset:1.0' (from X_INTERFACE_INFO parameter from HDL file).
INFO: [IP_Flow 19-5107] Inferred bus interface 'aresetn' of definition 'xilinx.com:signal:reset:1.0' (from 'X_INTERFACE_INFO' attribute).
INFO: [IP_Flow 19-5107] Inferred bus interface 'M_AXI_GPO' of definition 'xilinx.com:interface:aximm:1.0' (from Xilinx Repository).
INFO: [IP_Flow 19-5107] Inferred bus interface 'M_AXI_HP0' of definition 'xilinx.com:interface:aximm:1.0' (from Xilinx Repository).
INFO: [IP_Flow 19-5107] Inferred bus interface 'M_AXI_HP2' of definition 'xilinx.com:interface:aximm:1.0' (from Xilinx Repository).
INFO: [IP_Flow 19-5107] Inferred bus interface 'S_AXI_CONTROL' of definition 'xilinx.com:interface:aximm:1.0' (from Xilinx Repository).
INFO: [IP_Flow 19-5107] Inferred bus interface 'interrupt' of definition 'xilinx.com:signal:interrupt:1.0' (from Xilinx Repository).

```

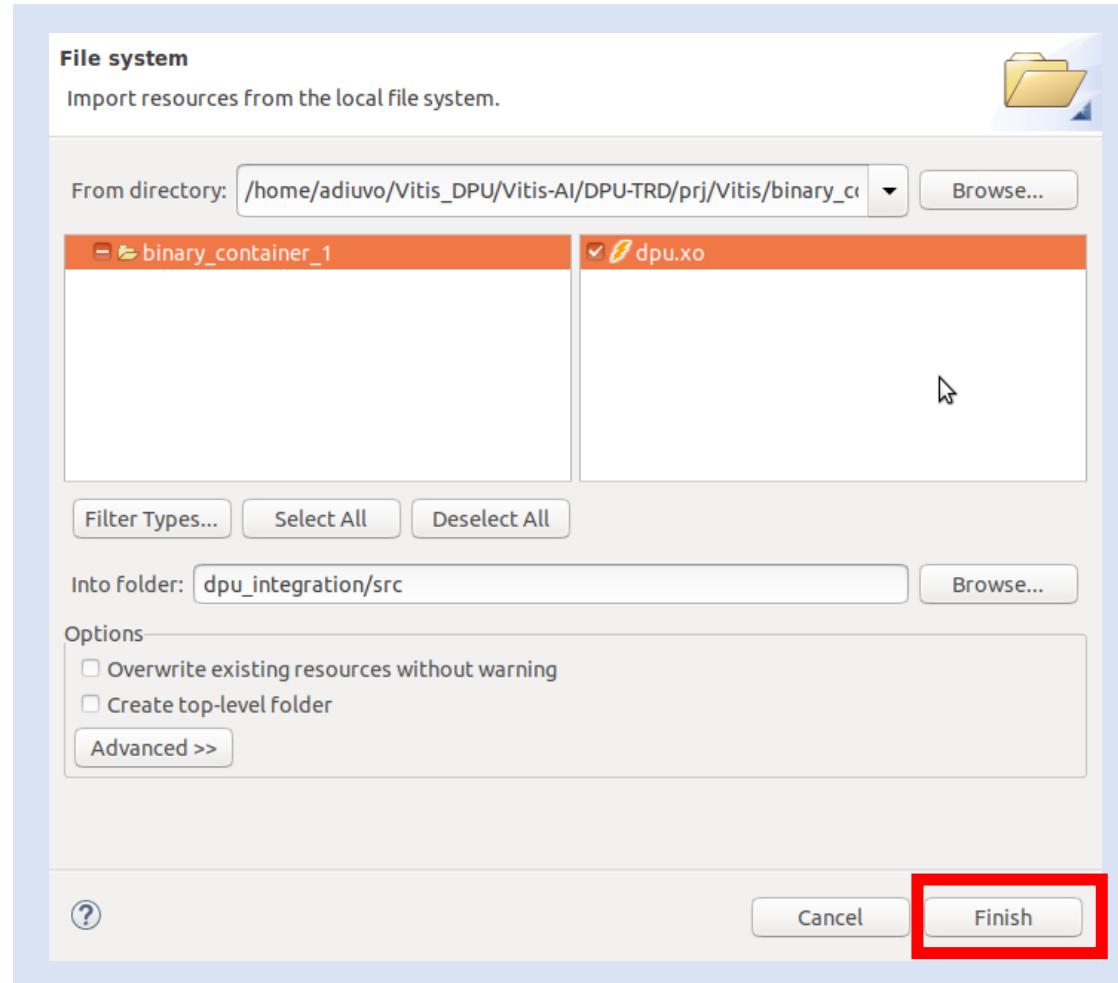
Lab 2: Instantiating Xilinx Deep Learning Processor —

Step 15 – Back in Vitis, click on the src folder in the project, right click and select import sources



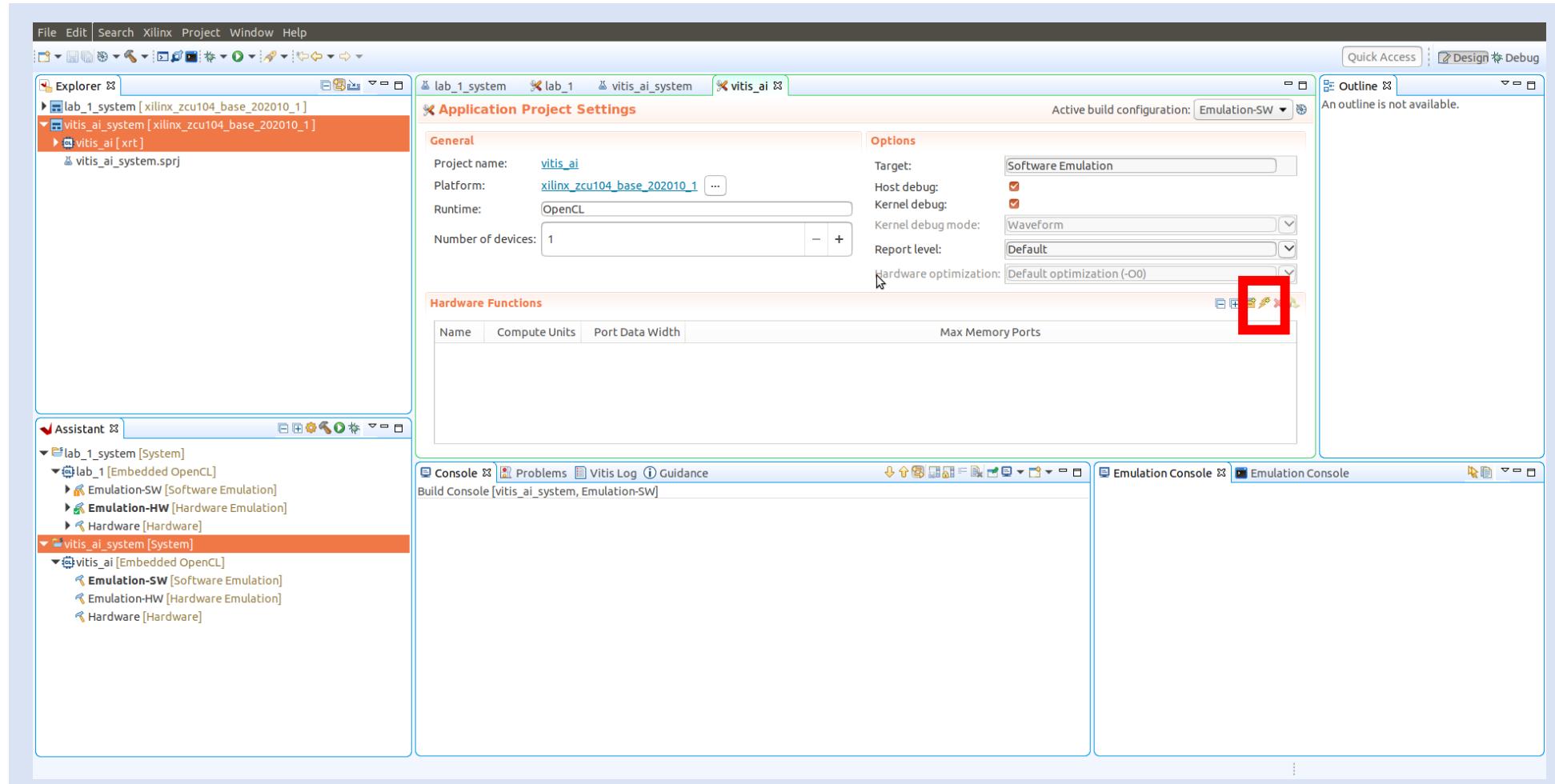
Lab 2: Instantiating Xilinx Deep Learning Processor —

Step 16 – Navigate to the Vitis-AI directory and the binary_container_1 folder. Select the DPU.xo and click finish



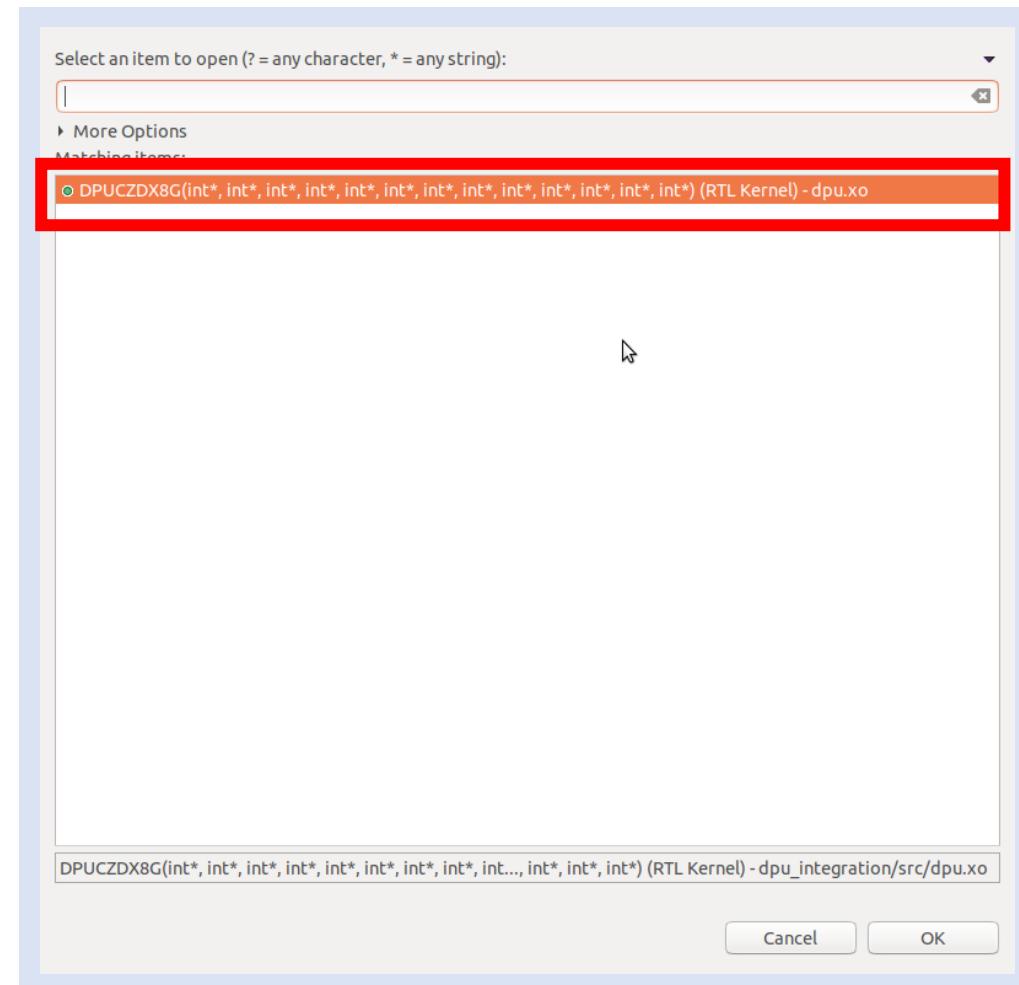
Lab 2: Instantiating Xilinx Deep Learning Processor —

Step 17 – Click on the lightening bolt icon to select the function to accelerate to hardware



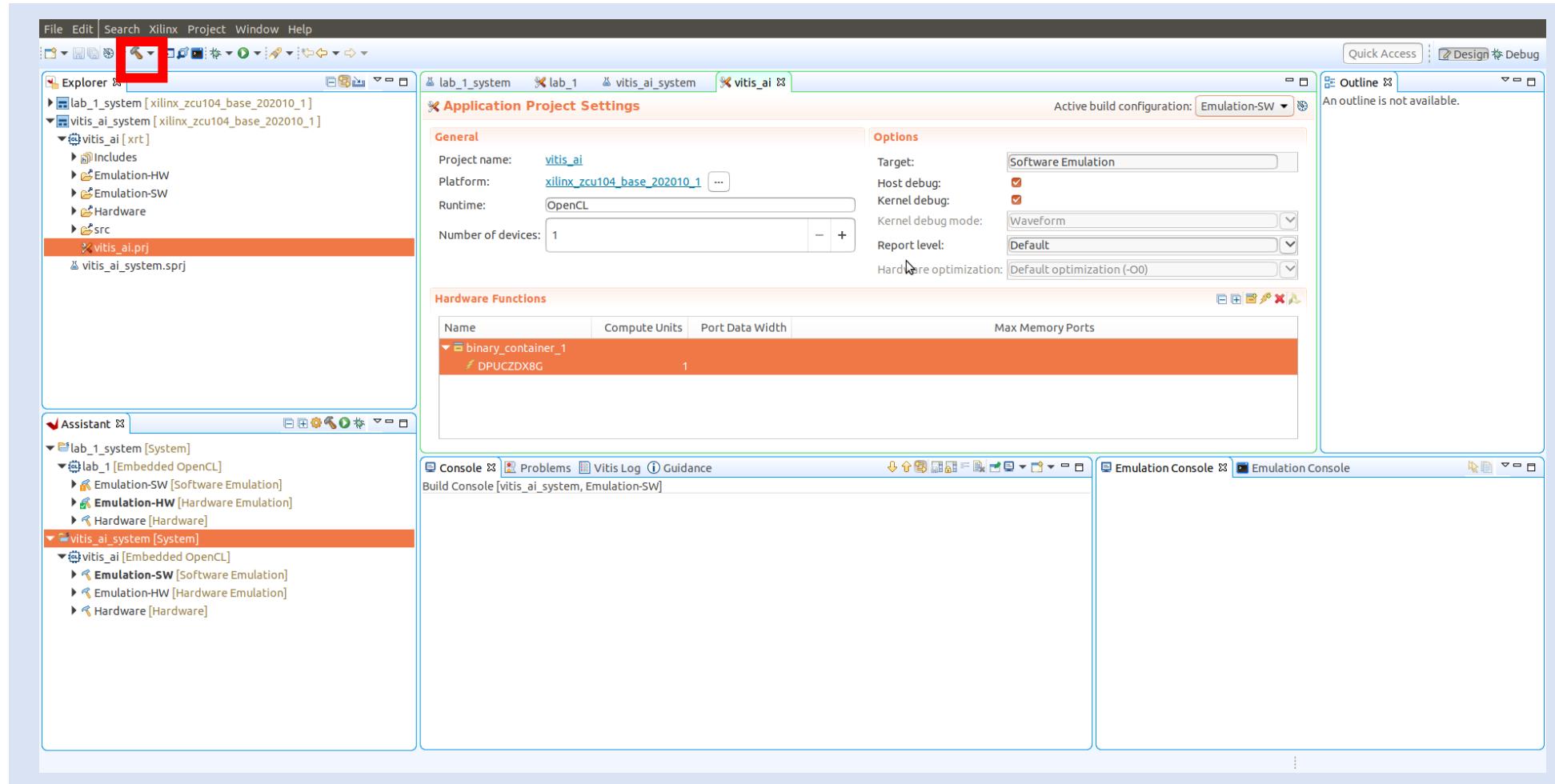
Lab 2: Instantiating Xilinx Deep Learning Processor

Step 18 – Select the DPU function from the list of matching items



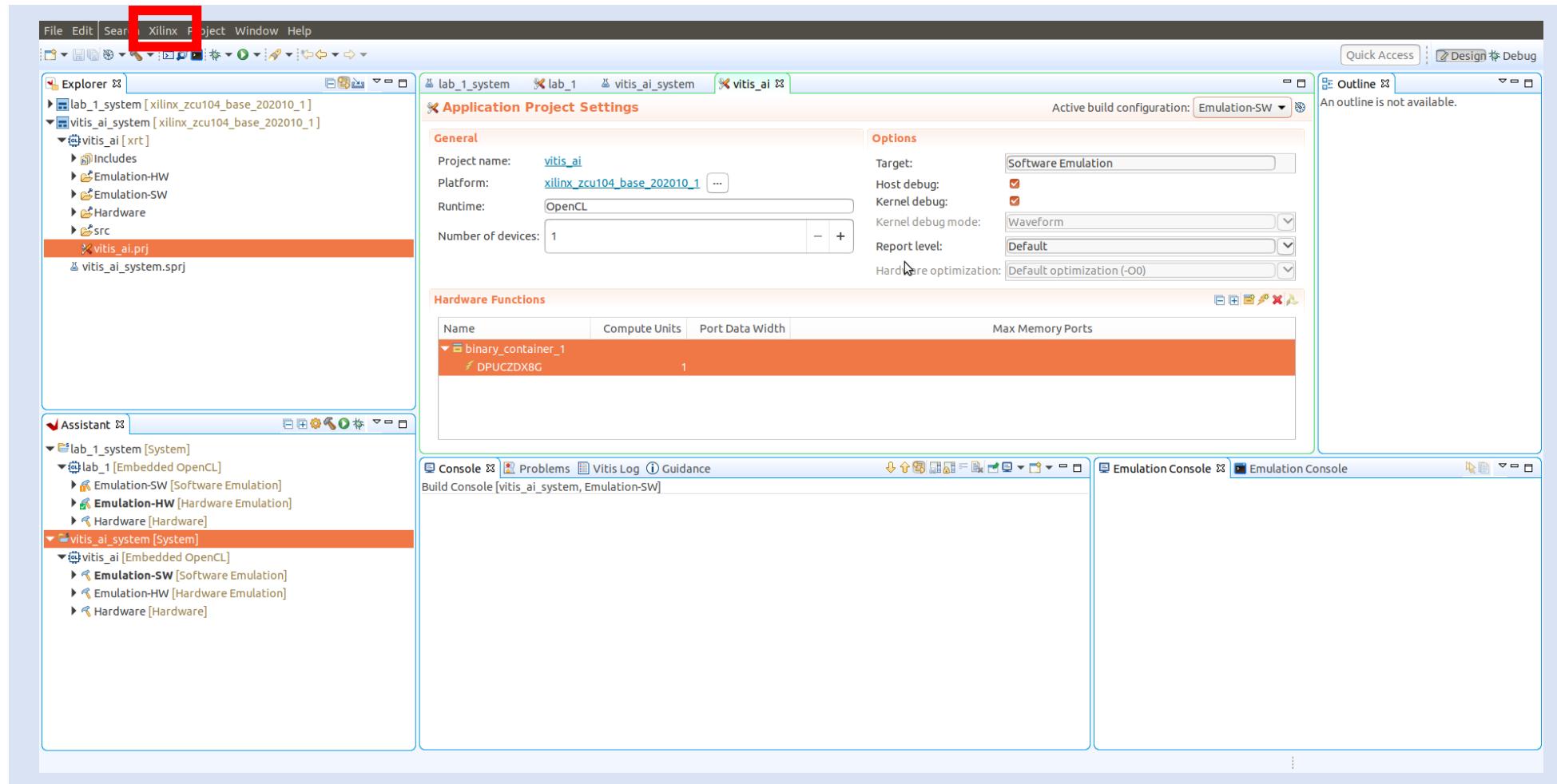
Lab 2: Instantiating Xilinx Deep Learning Processor

Step 19 – Click on build and the design will implement.



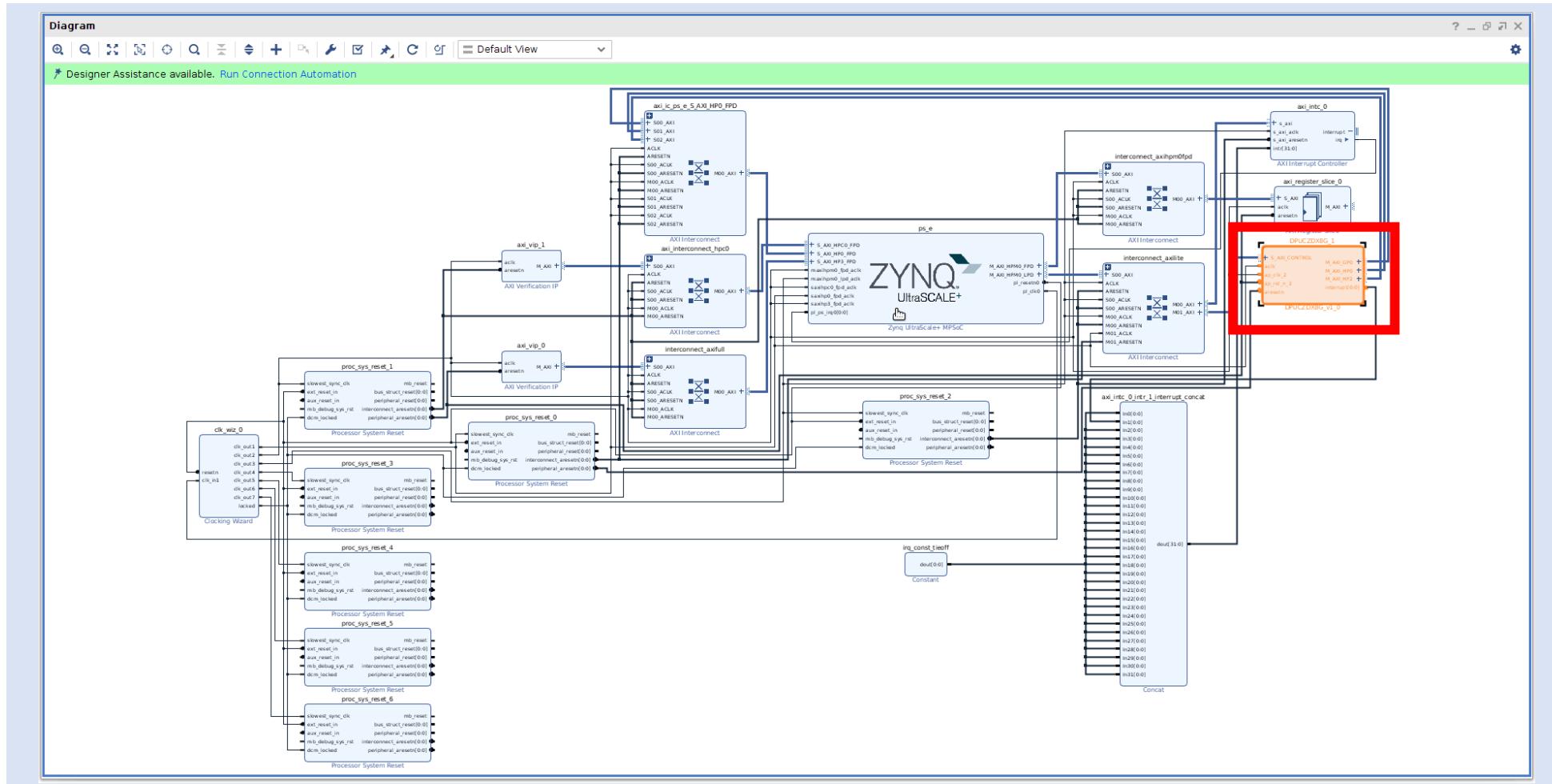
Lab 2: Instantiating Xilinx Deep Learning Processor

Step 20 – Once built, from the Xilinx Menu select Vivado integration and open Vivado project



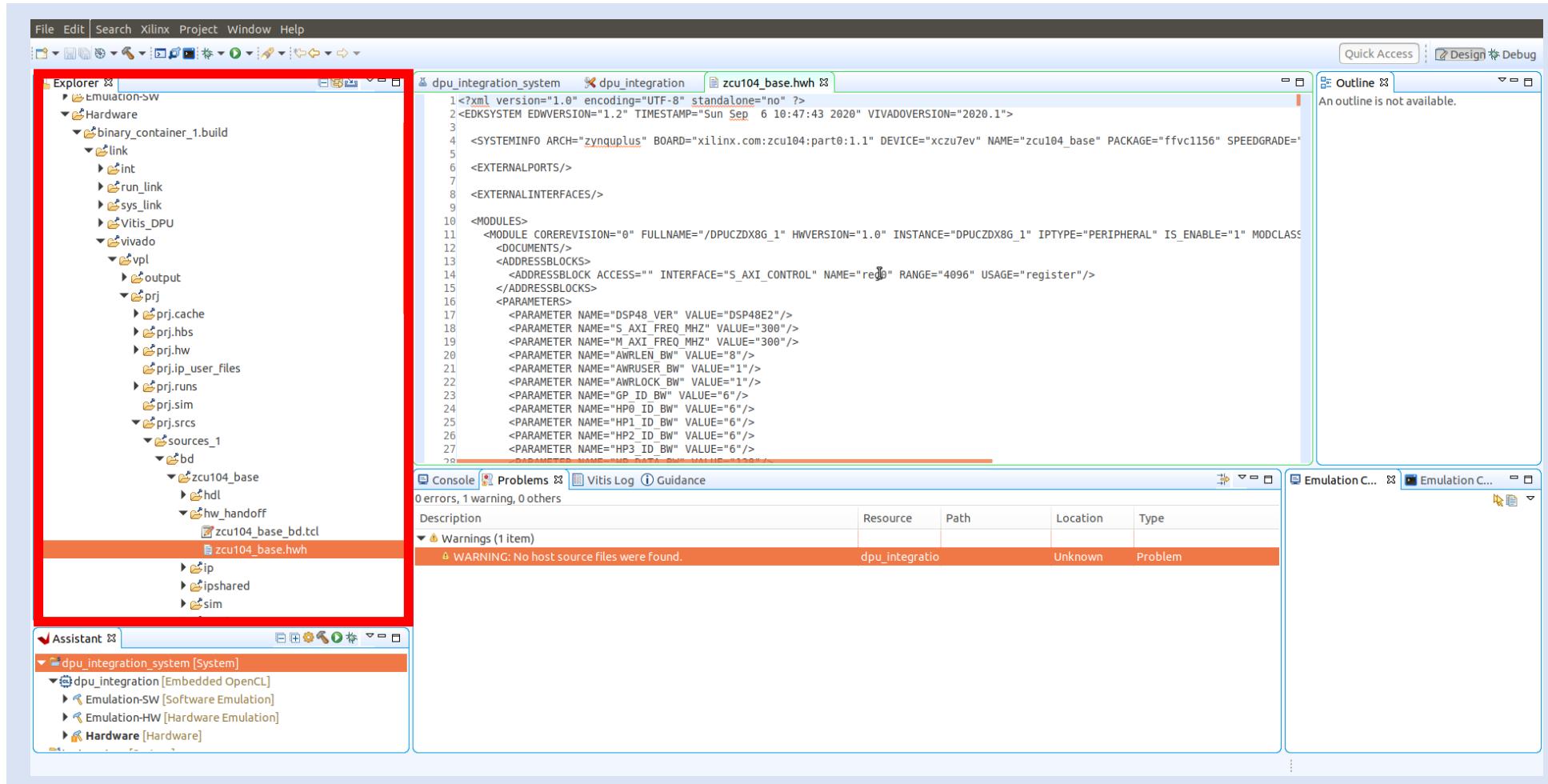
Lab 2: Instantiating Xilinx Deep Learning Processor

Step 21 – Once Vivado opens, open the block diagram and you will see the DPU



Lab 2: Instantiating Xilinx Deep Learning Processor —

Step 21 – With the DPU platform created, the HWH file is now created for use with the remaining Vitis-AI stack



Lab 2 Summary

The concludes lab 2, throughout this lab we have demonstrated

1. How to clone the Vitis-AI tools
2. Modify the DPU configuration
3. Create the DPU.Xo for use in Vitis bottom up flow
4. Import the DPU into Vitis
5. Build the Xclbin and HWH file – required for higher levels Vitis-AI stack
6. Explore the implemented design in Vivado

Further Support

The following resources may be of interest

1. <https://www.adiuvoengineering.com/blog> - Adiuvo engineering blog updated weekly
2. <https://www.adiuvoengineering.com/microzed-chronicles-archive> - Complete Adiuvo engineering blog backlog
3. <https://github.com/Xilinx/Vitis-AI-Tutorials> - Vitis AI Tutorials
4. <https://www.hackster.io/AlbertaBeef/projects> - Good source of Vitis AI Ultra96 projects