

Getting to Know Vivado

Course Workbook

Table of Contents

About this Workbook

[Slide 3](#)

Pre-Lab: Workshop Pre-requisites

[Slide 4](#)

Lab 1: Understanding Vivado

[Slide 7](#)

About this Workbook

This workbook is designed to be used in conjunction with the Getting to Know Vivado course.

The contents of this workbook are created by Adiuvo Engineering & Training, Ltd.

If you have any questions about the contents, or need assistance, please contact Adam Taylor at adam@adiuvoengineering.com.

Pre-Lab

Workshop Pre-requisites

Required Hardware

There is no required hardware for this course.

Downloads and Installations

Step 1 – Download and install the following at least one day prior to the workshop. This may take a significant amount of time and drive space.

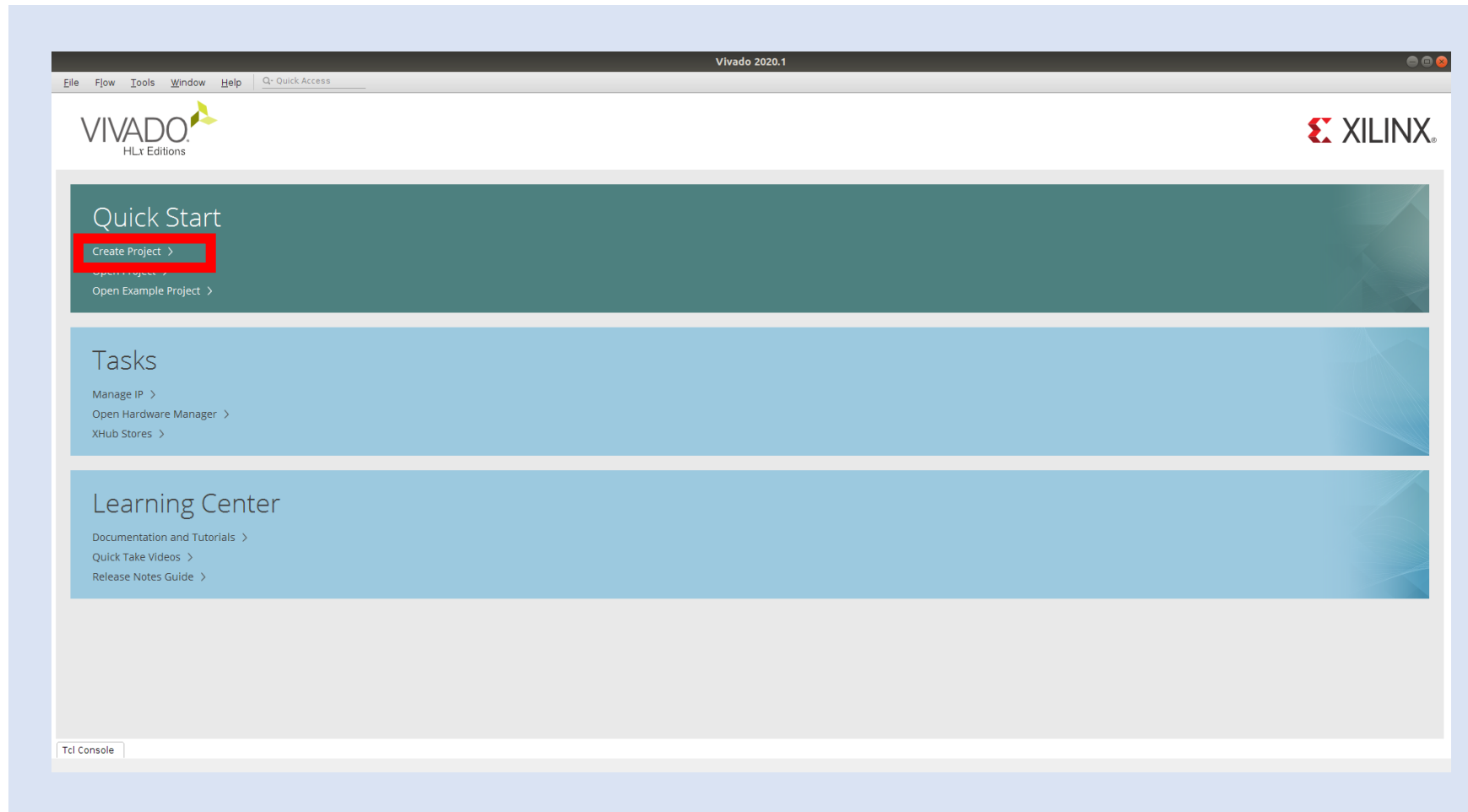
Vivado 2020.1	Download
Source Project Files	Download

Lab 1

Overview and Introduction to Vivado

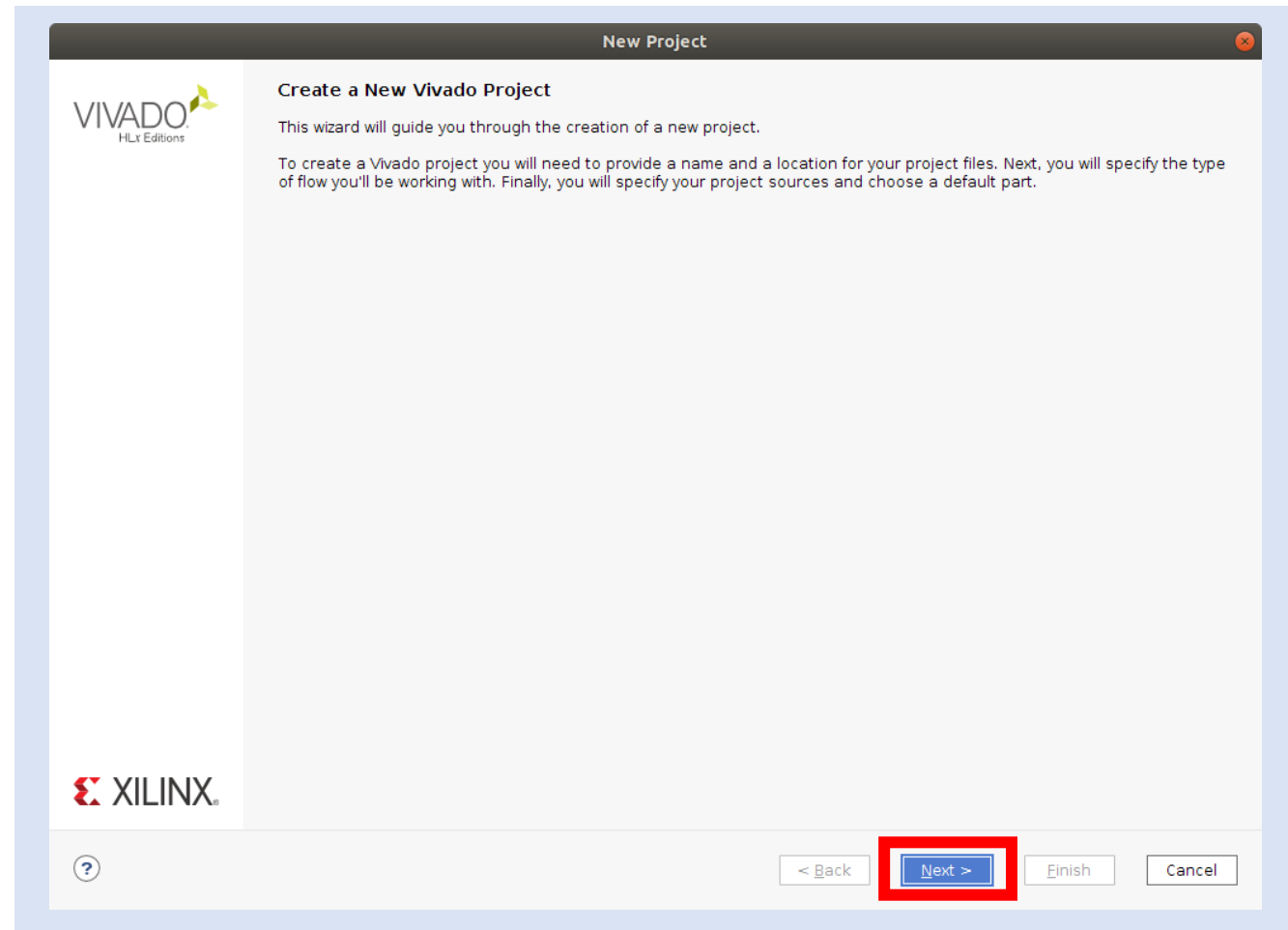
Lab 1: Overview and Introduction to Vivado

Step 1 – Open Vivado 2020.1.



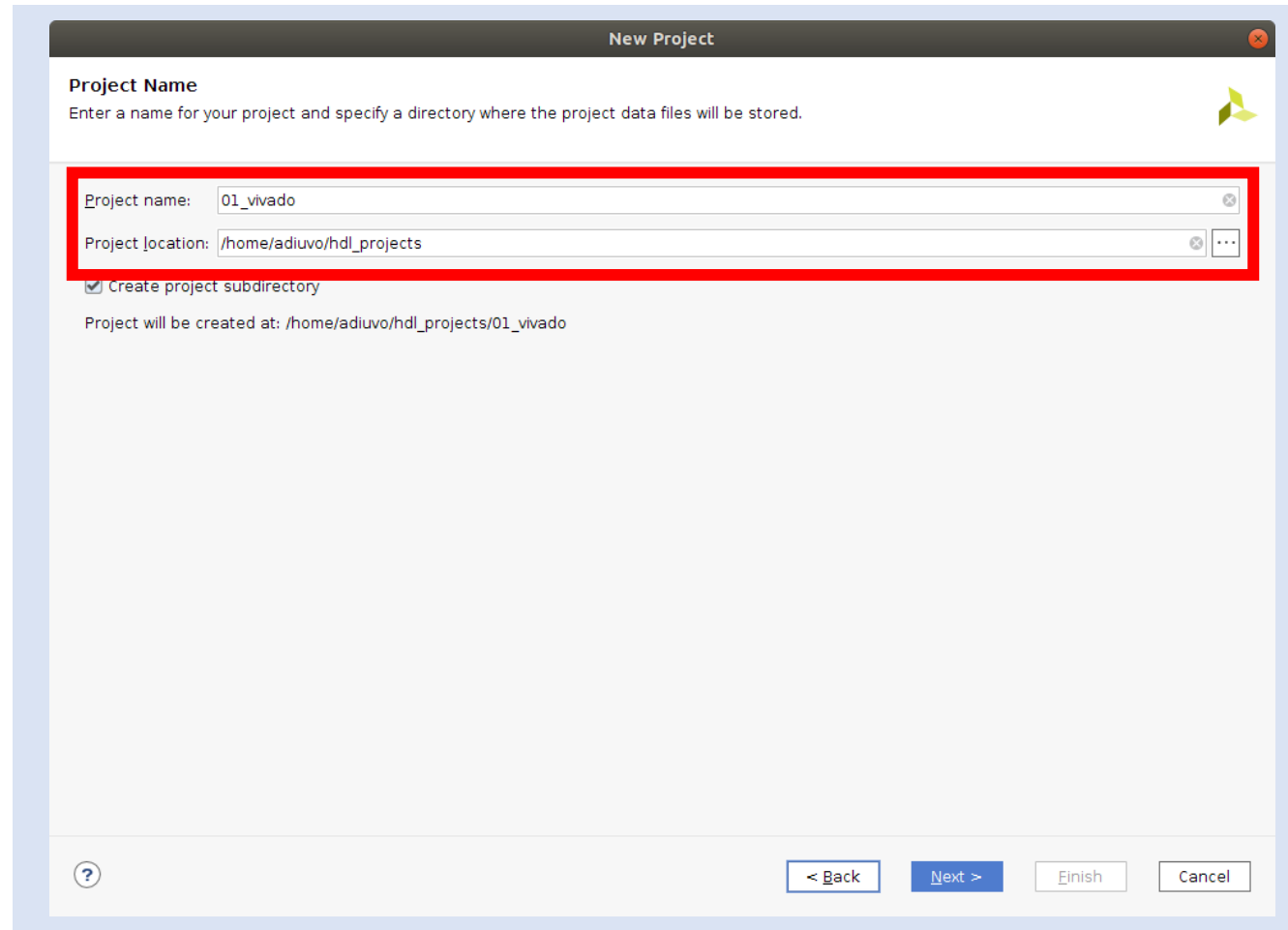
Lab 1: Overview and Introduction to Vivado

Step 2 – Click on **Create Project** – This will open the New Project Wizard – Click **Next**.



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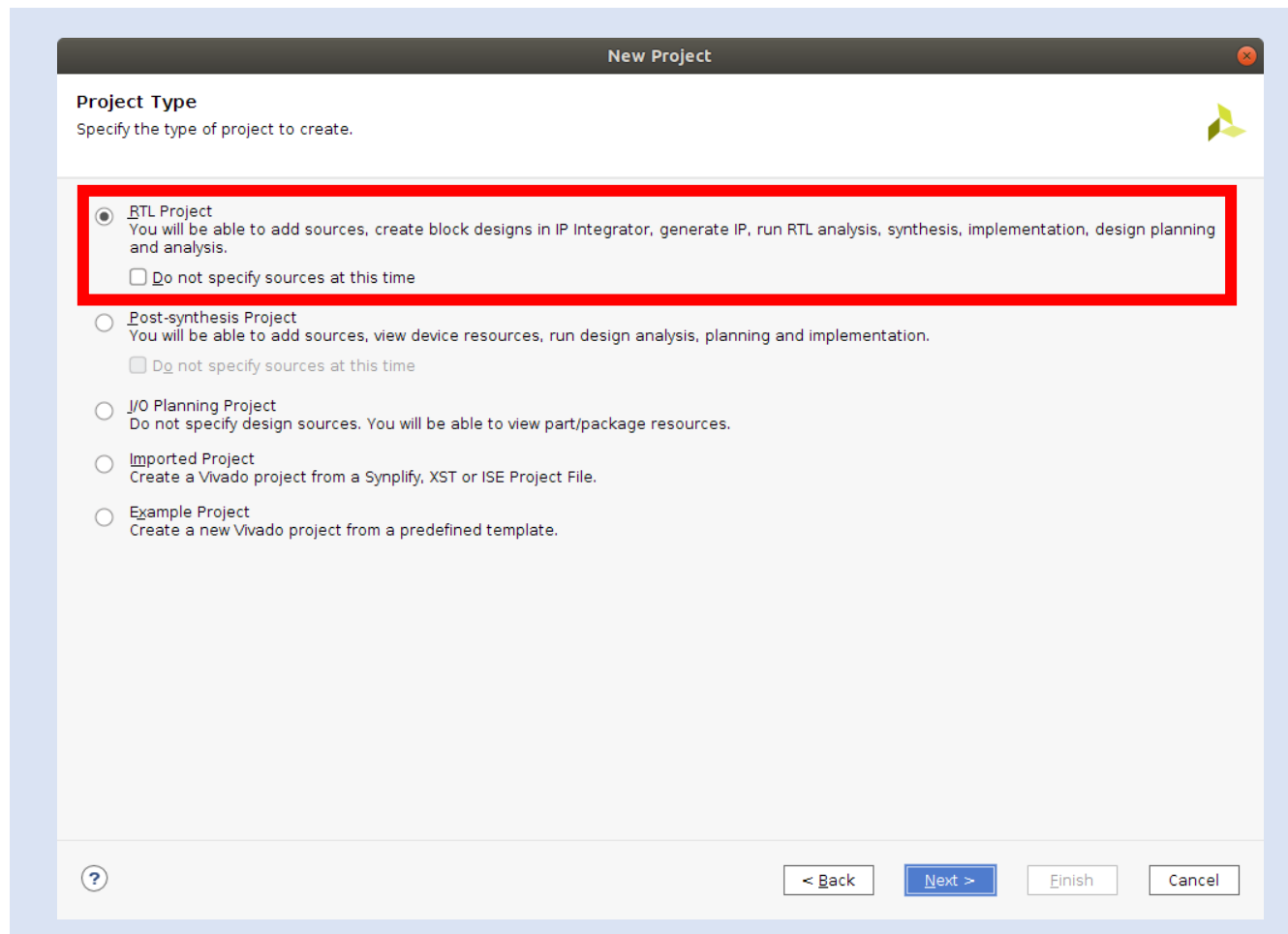
Step 3 – Enter the project name of “**01_Vivado**” and select the location you want to save the project.



The screenshot shows the 'New Project' dialog box in Vivado. The 'Project Name' field is set to '01_vivado' and the 'Project location' is set to '/home/adiuvo/hdl_projects'. The 'Create project subdirectory' checkbox is checked. The project will be created at '/home/adiuvo/hdl_projects/01_vivado'. The 'Next >' button is highlighted.

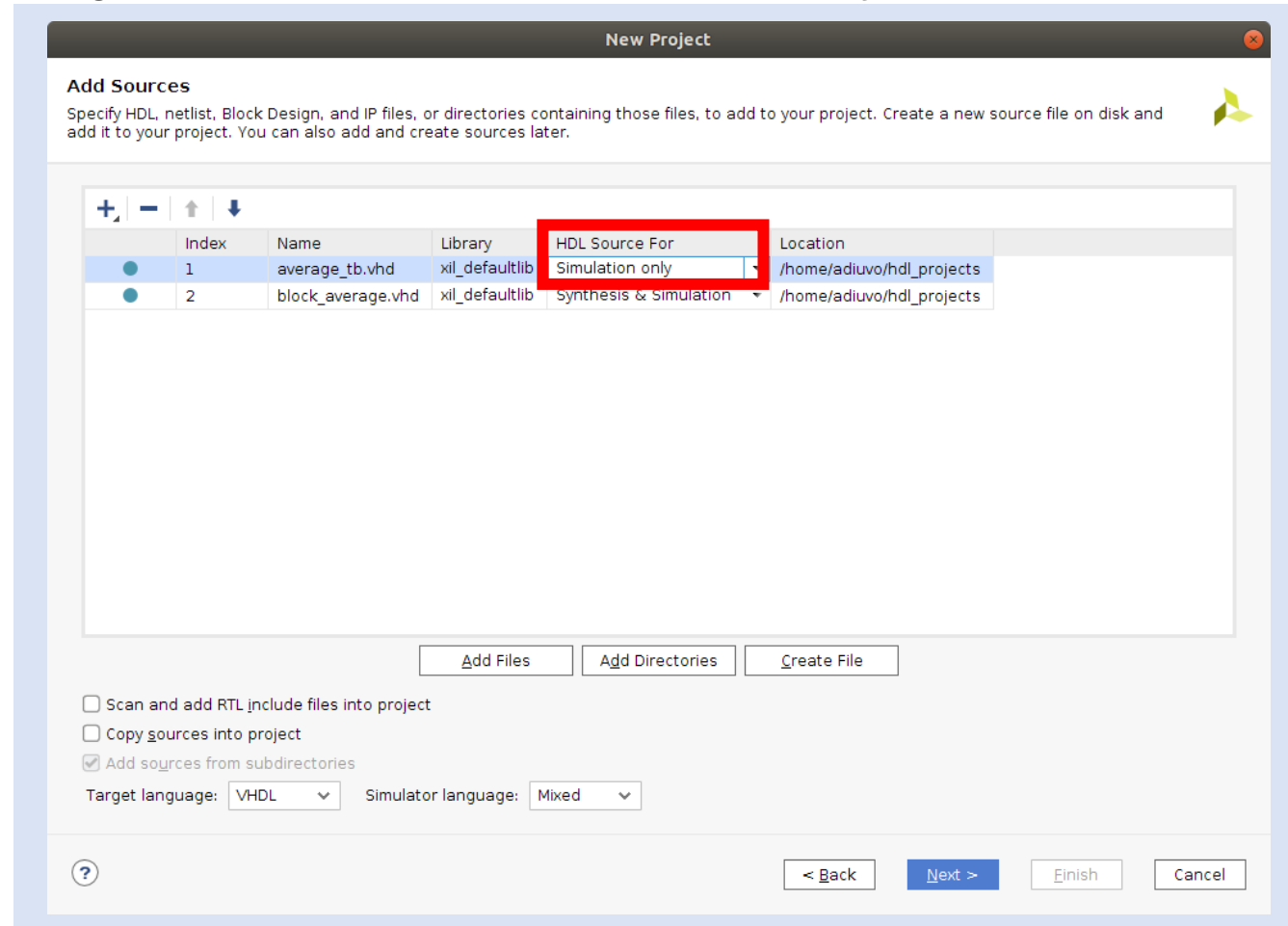
Lab 1: Overview and Introduction to Vivado

Step 4 – Select RTL Project.



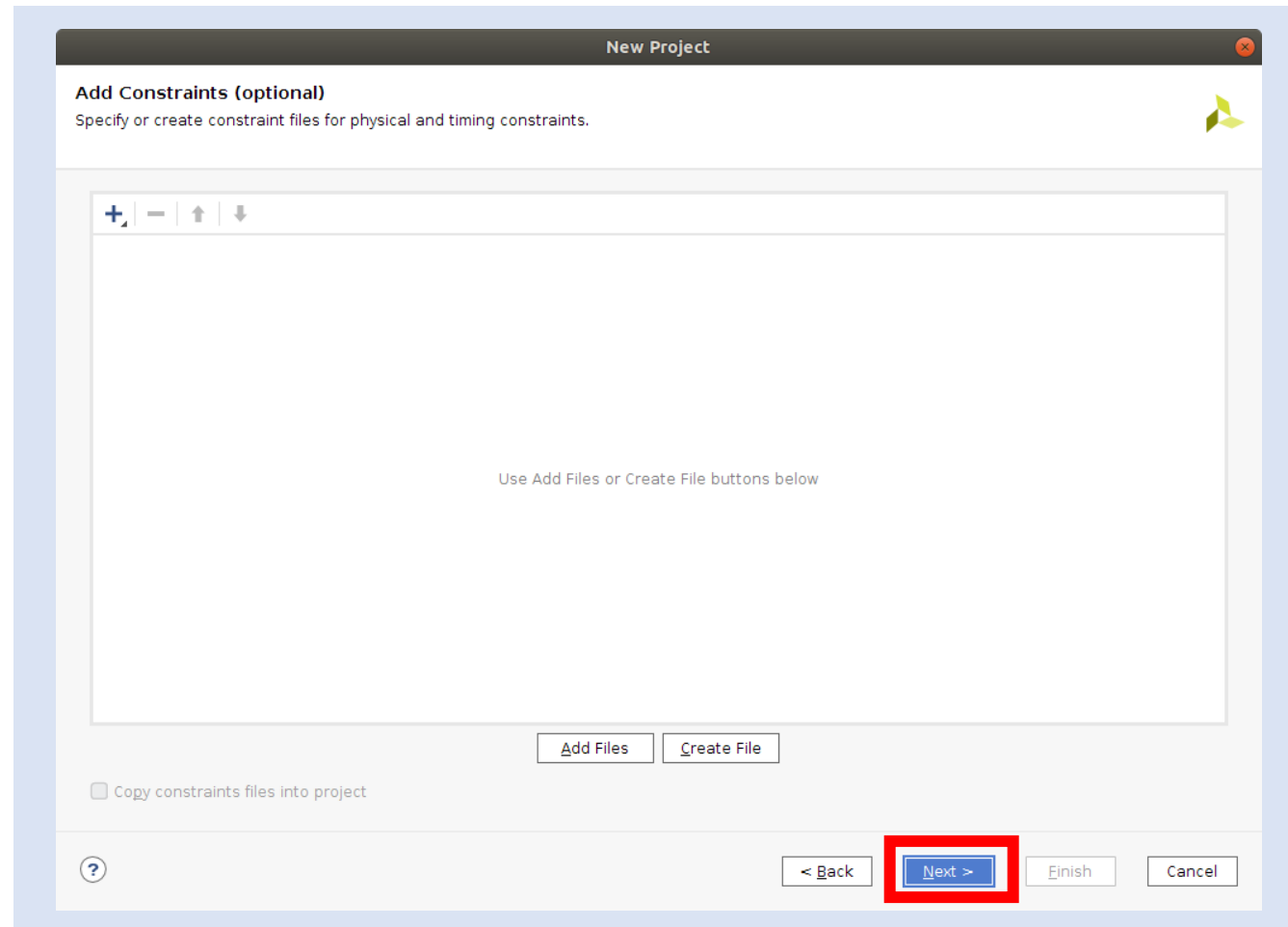
Lab 1: Overview and Introduction to Vivado

Step 5 – Click **ADD FILES** and select the two files downloaded from Github. For the file `average_tb.vhd`, change the HDL source to **Simulation Only**.



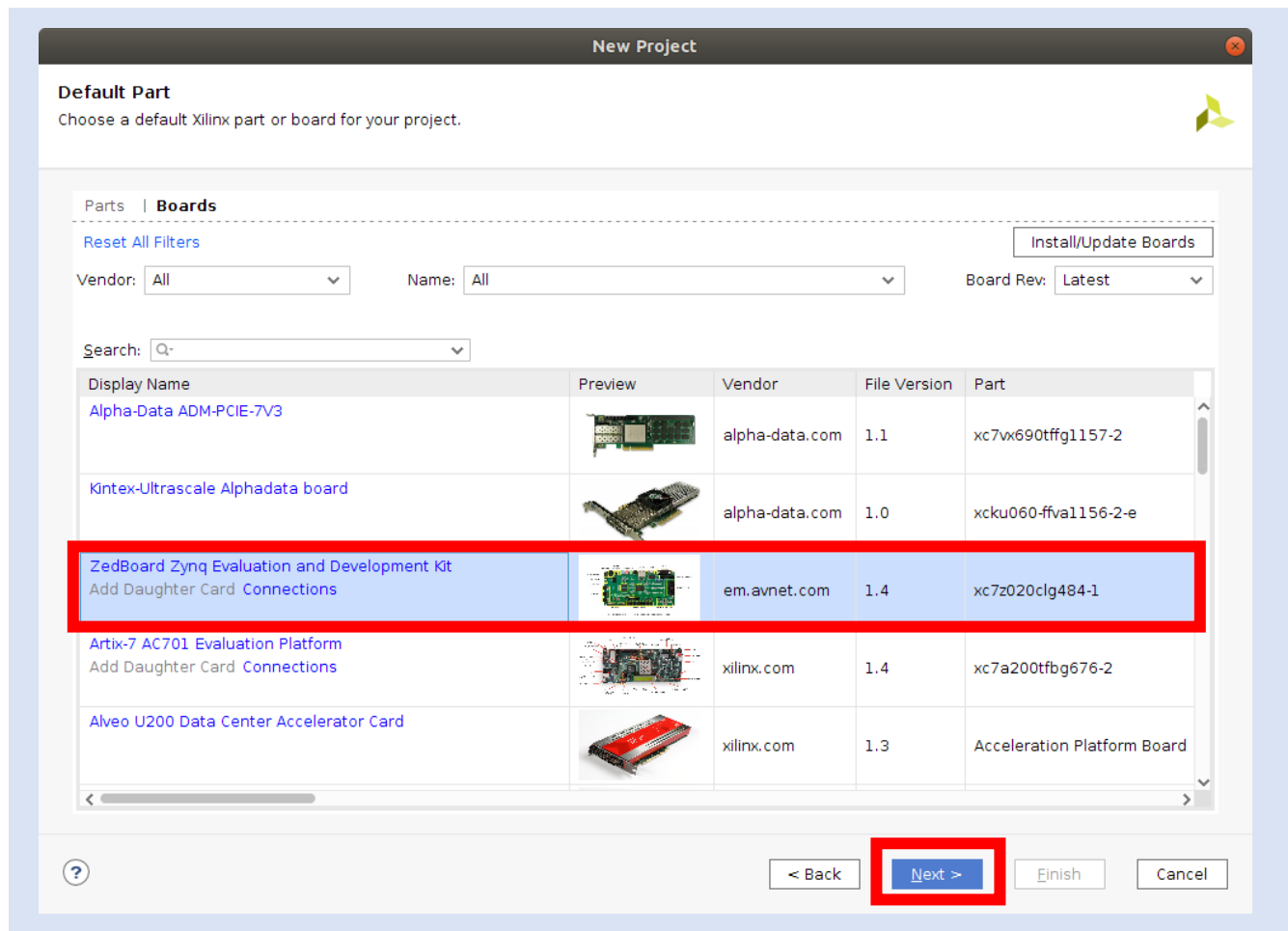
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Step 6 – At this time we do not want to add any constraints files. Click **Next**.



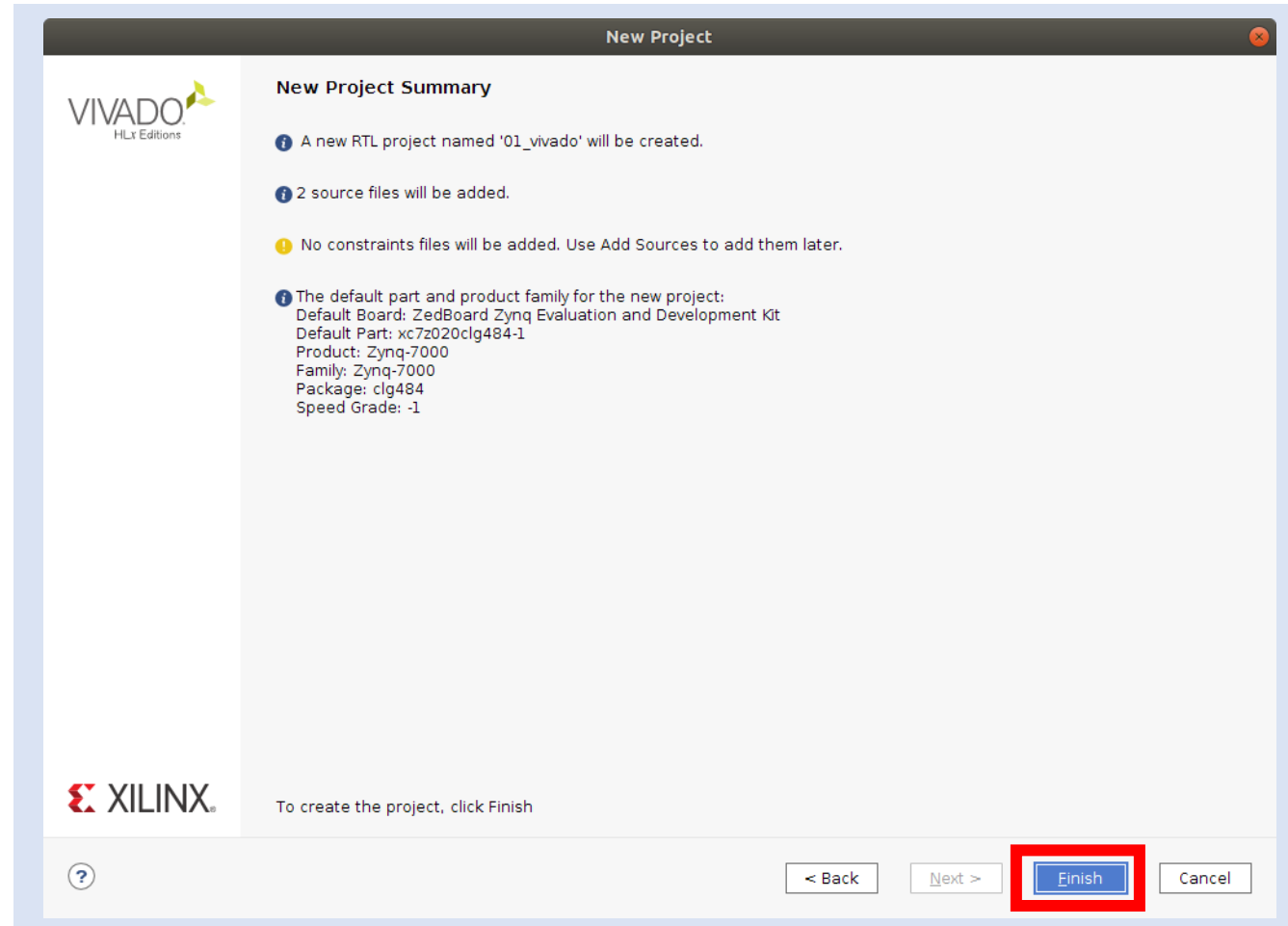
Lab 1: Overview and Introduction to Vivado

Step 7 – Select the ZedBoard and click Next.



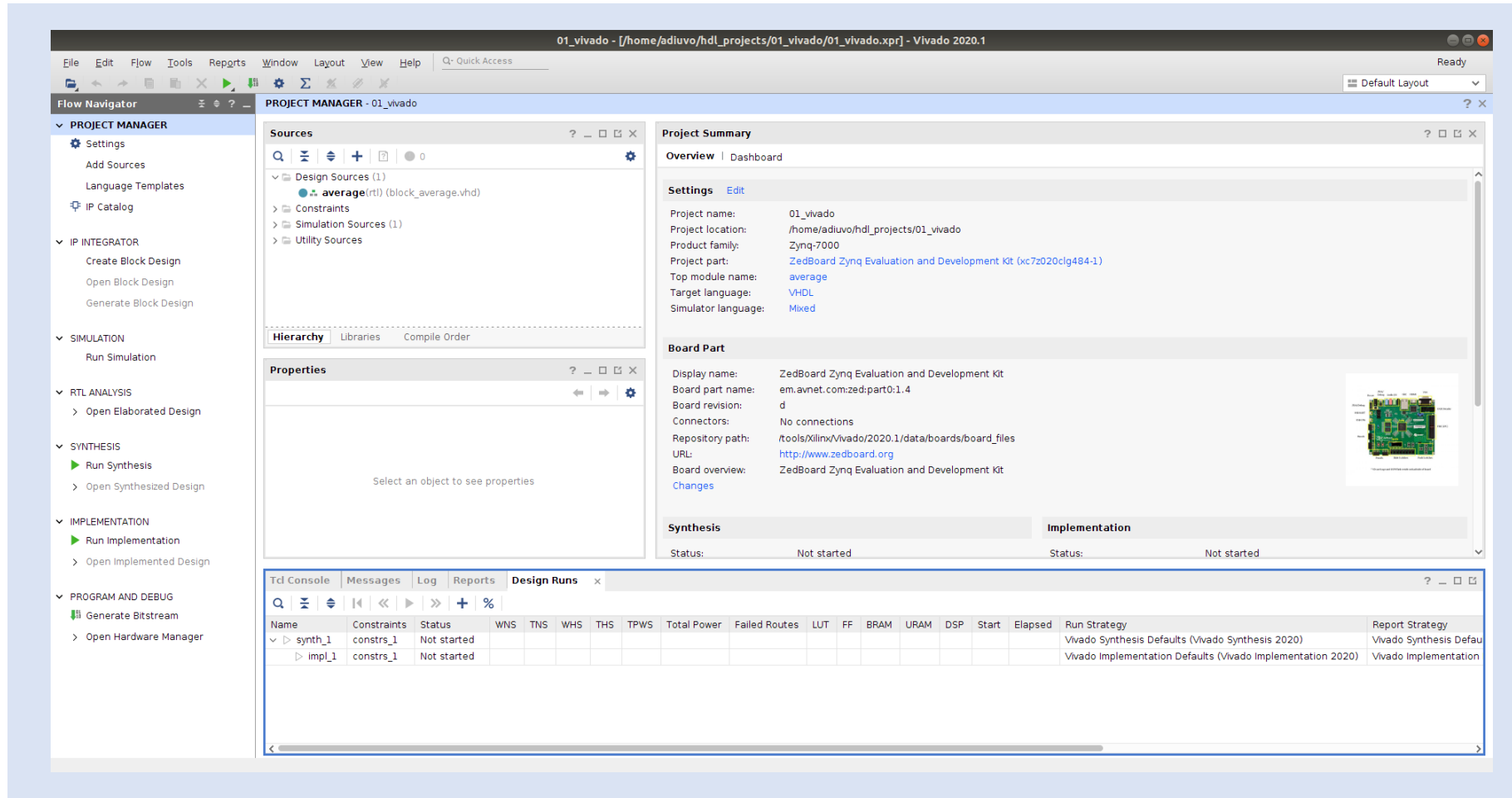
Lab 1: Overview and Introduction to Vivado

Step 8 – On the project summary tab, select **Finish**.



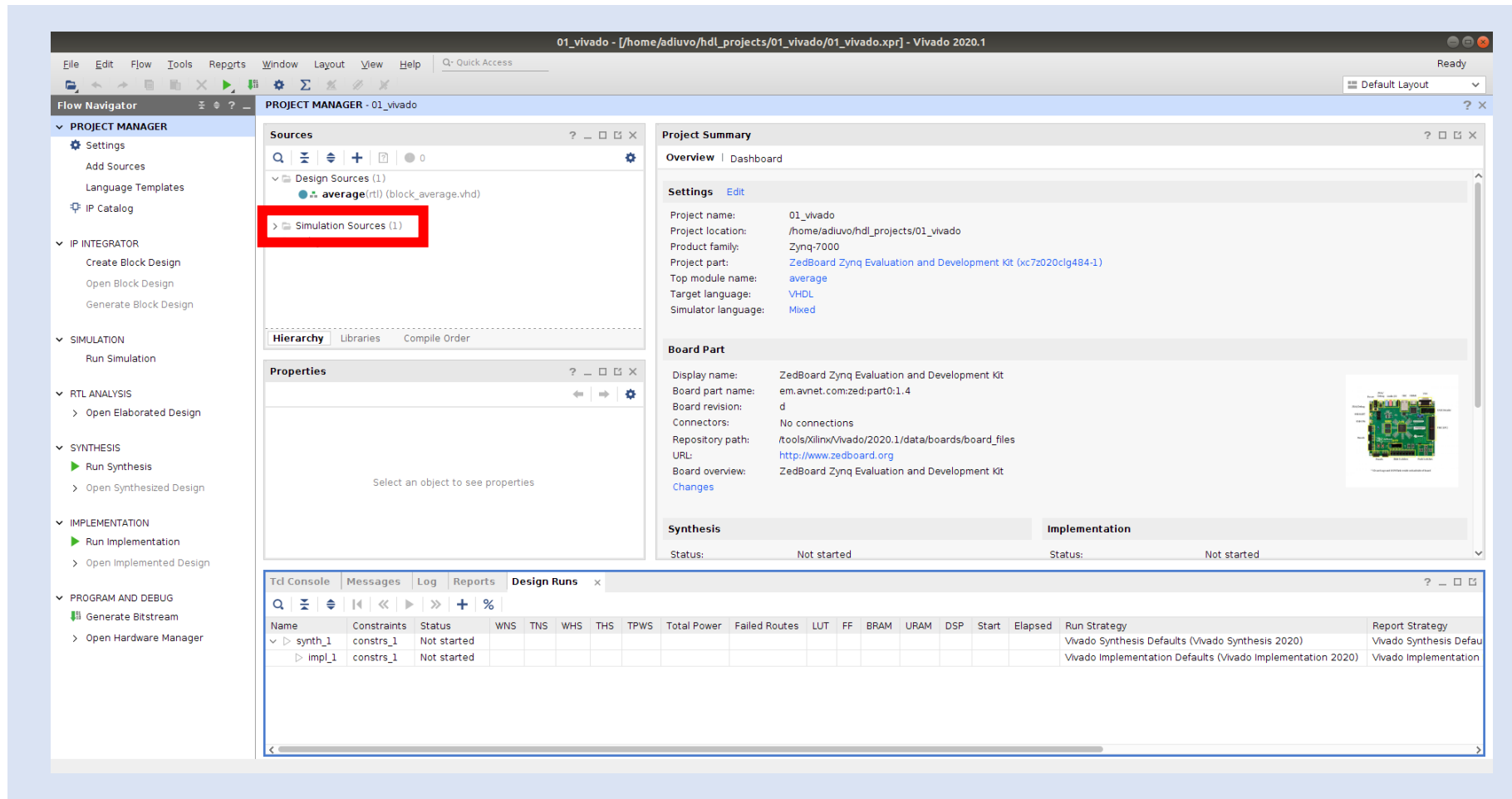
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Step 9 – This will open Vivado in the project manager view.



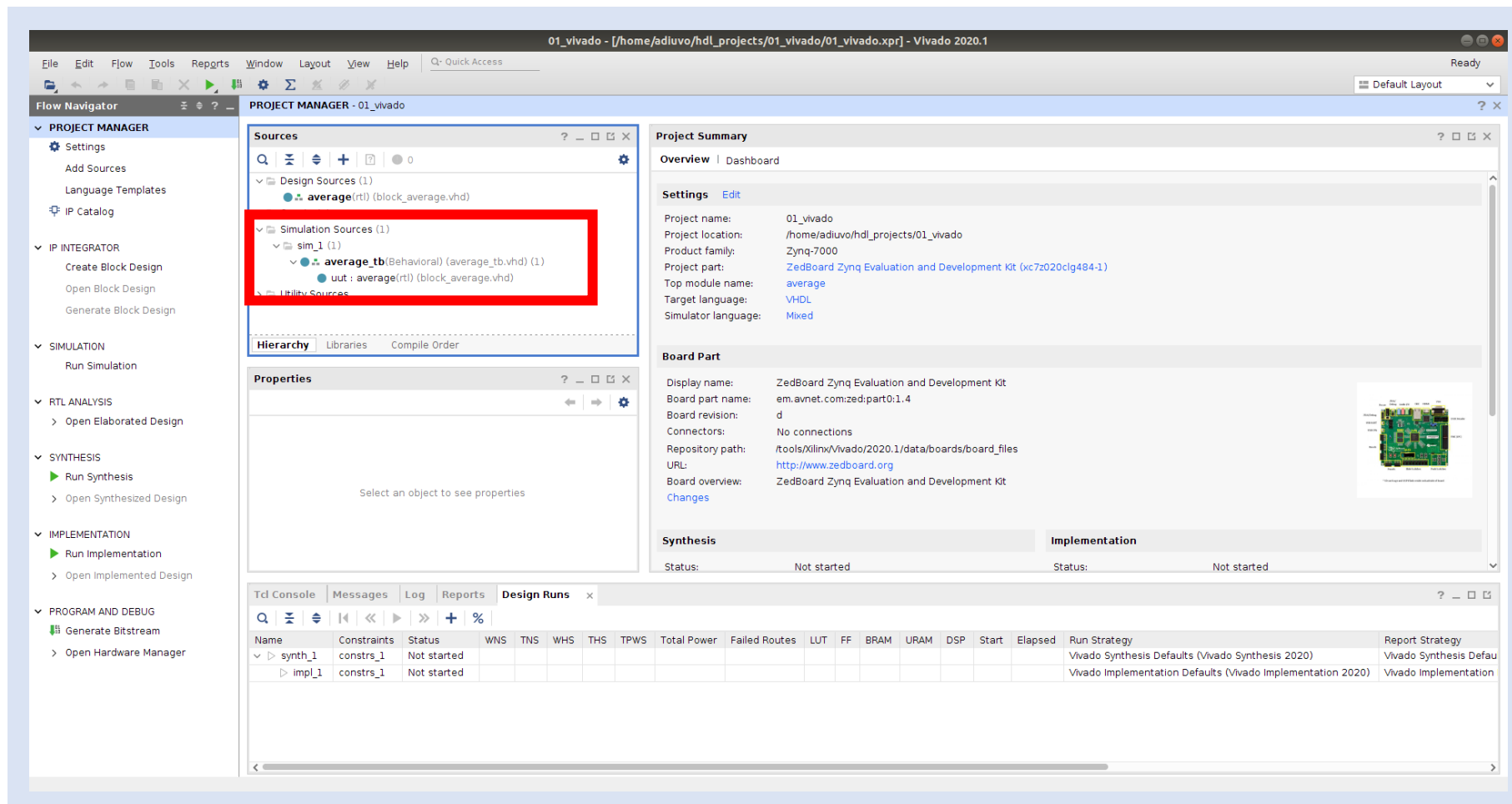
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Step 10 – Expand the Simulation Sources.



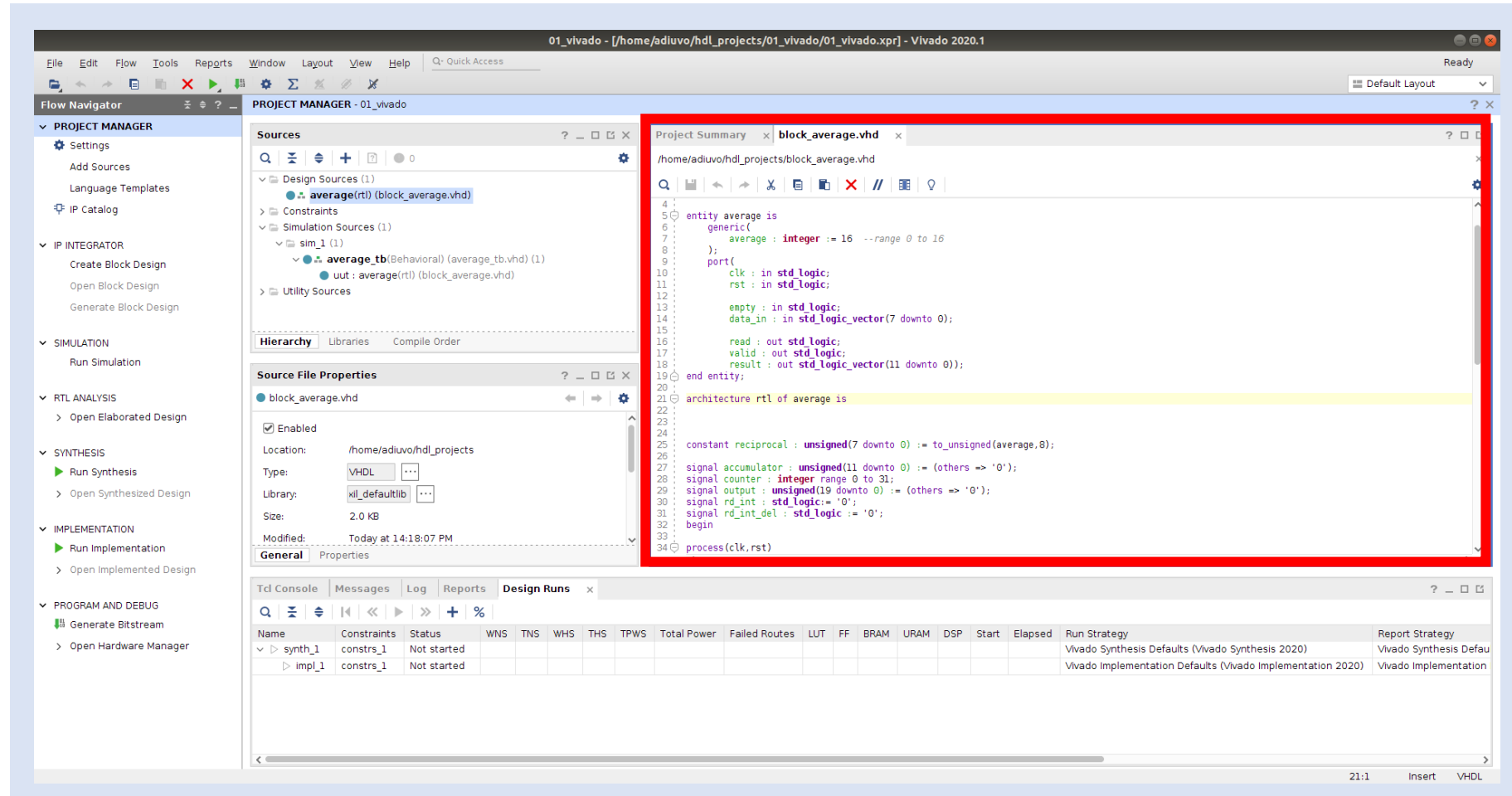
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Step 11 – This will show the test bench and the design source to be simulated.



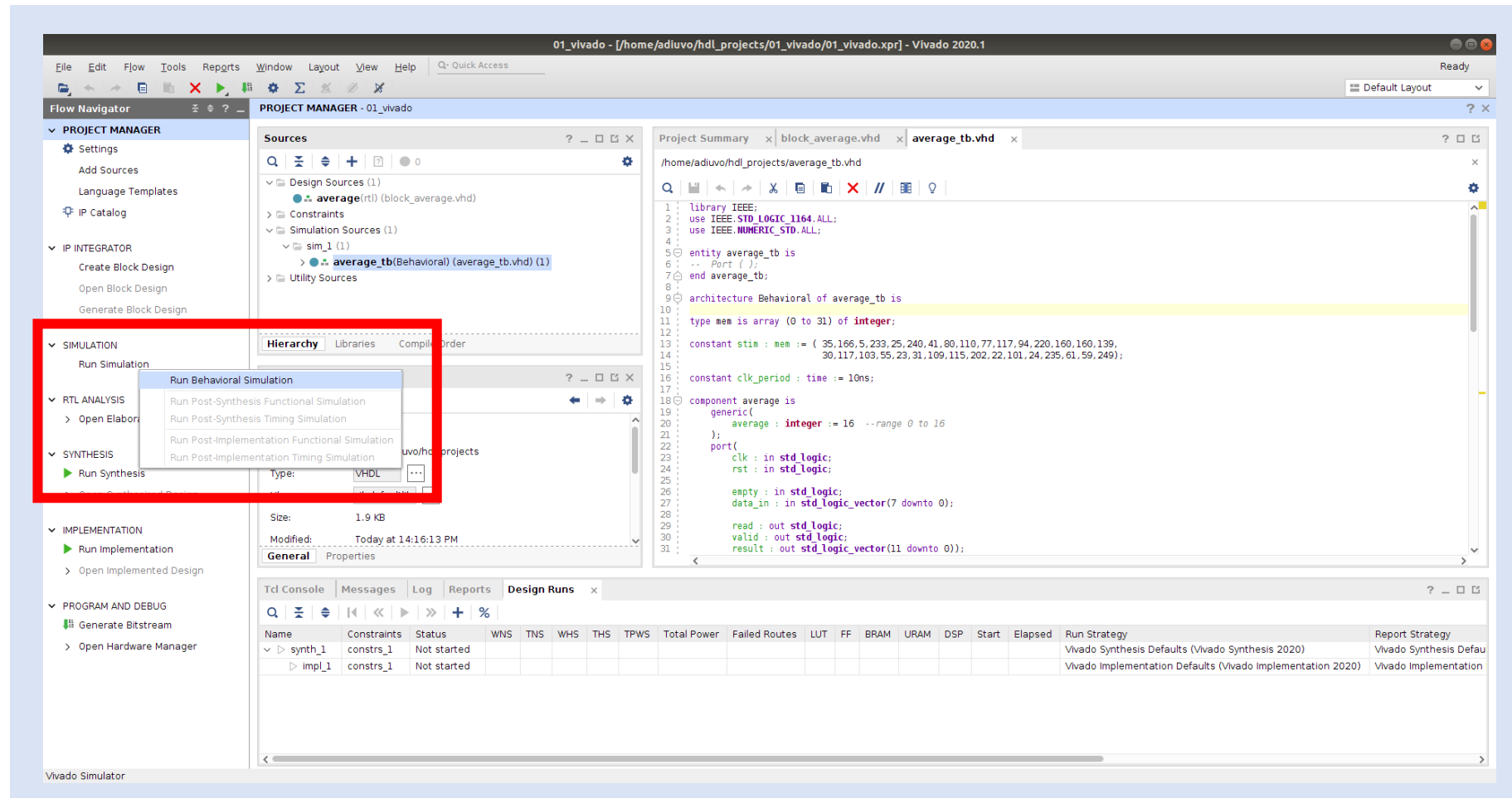
Lab 1: Overview and Introduction to Vivado

Step 12 – Double clicking on the VHDL files will open the source for inspection.



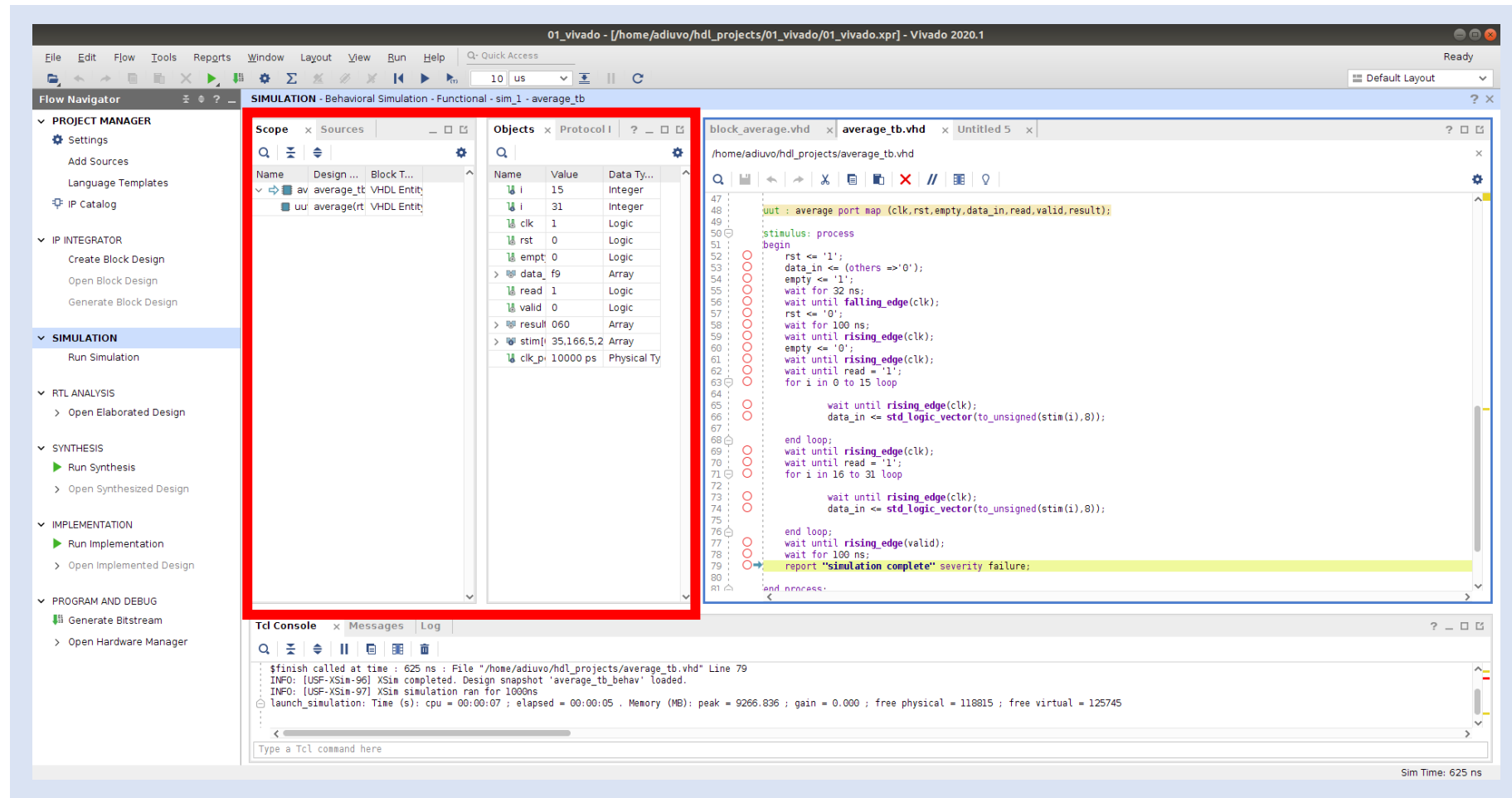
Lab 1: Overview and Introduction to Vivado

Step 13 – To run a simulation, click on Run Simulation and select Run Behavioral Simulation.



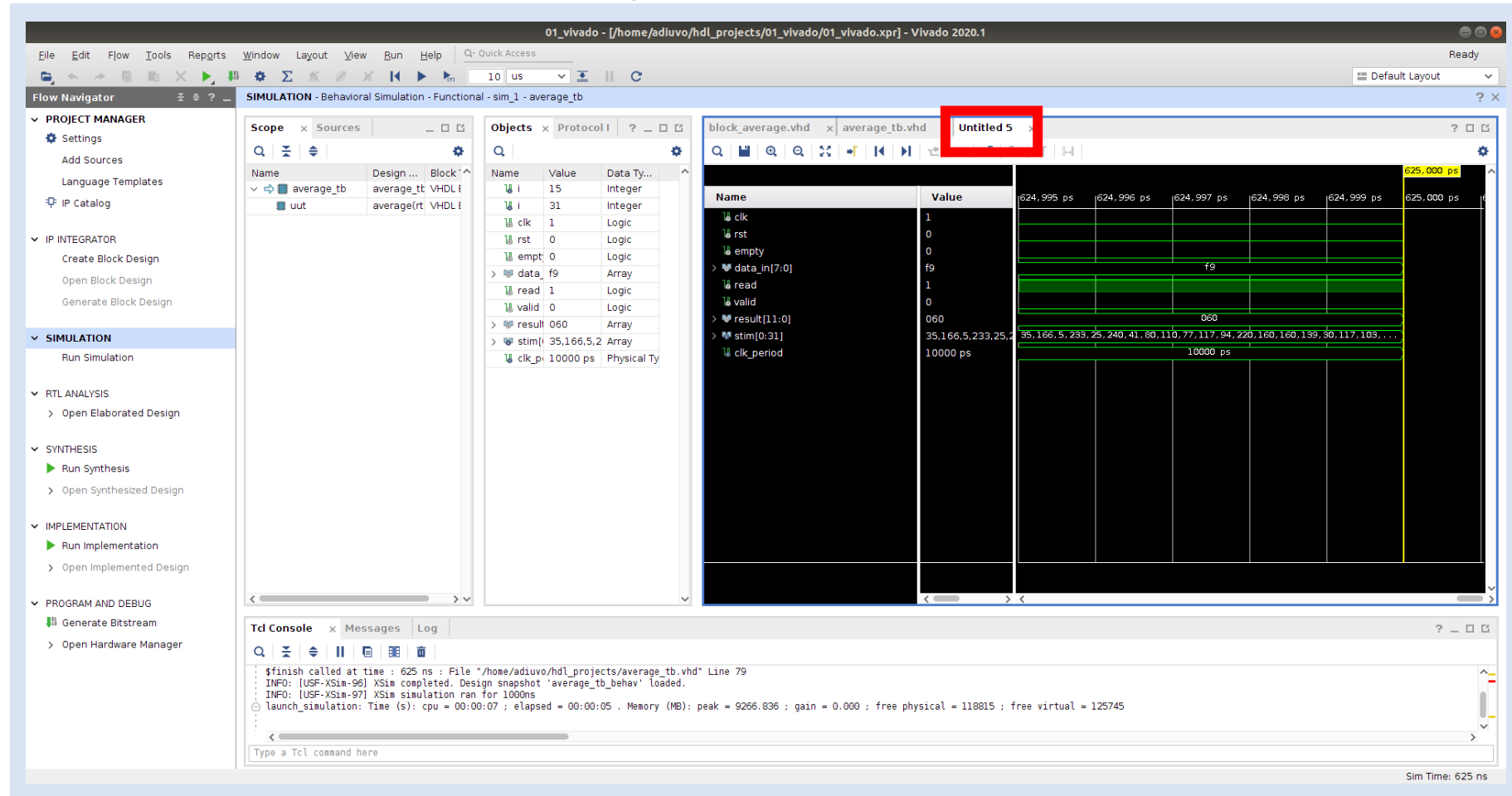
Lab 1: Overview and Introduction to Vivado

Step 14 – This will open the behavioral simulation view. Note the scope and objects.



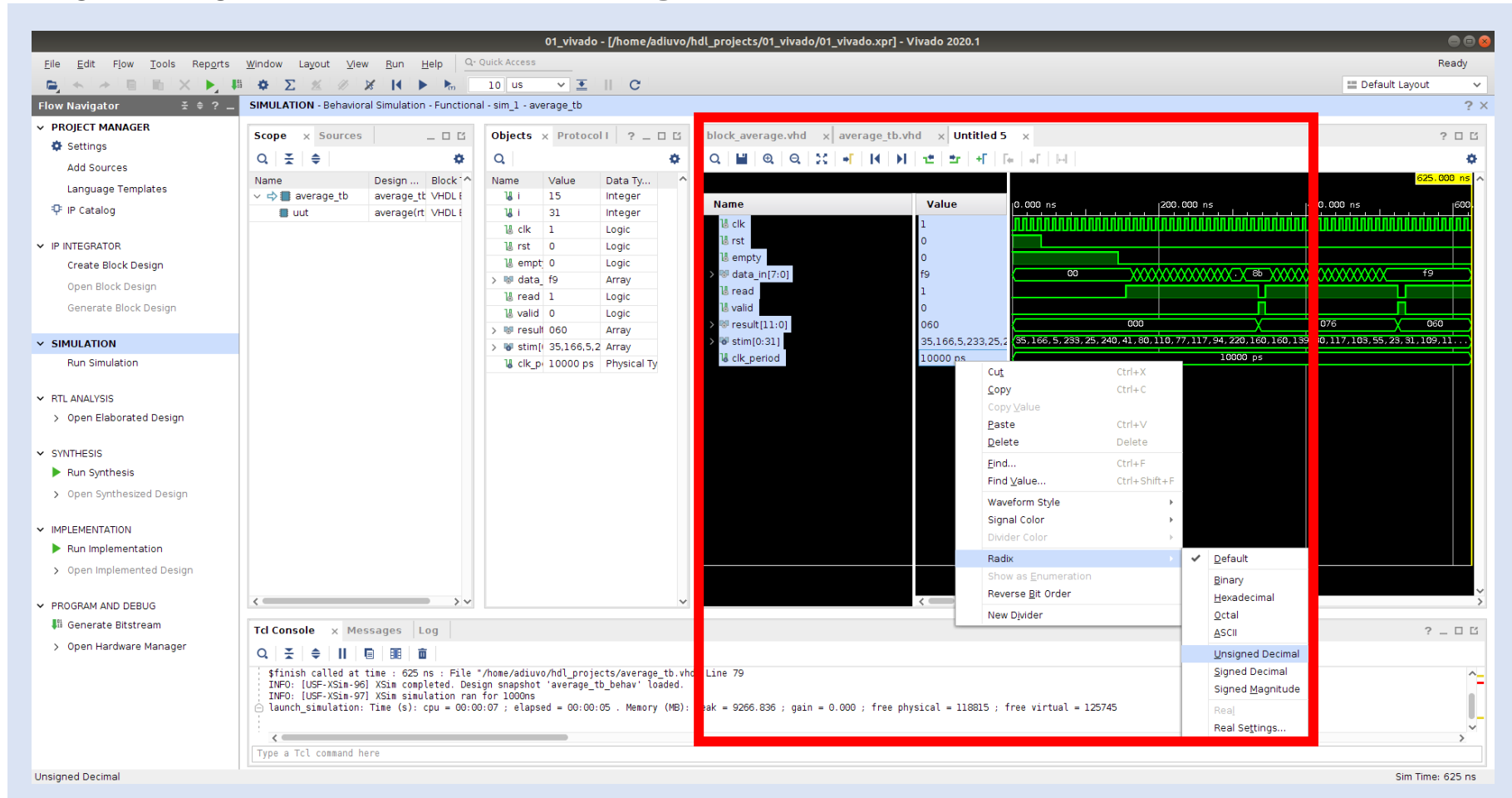
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Step 15 – Click on the **Untitled*** tab to see the waveform of the simulation. Note this view shows the signals defined within the test bench only, not the Unit Under Test.



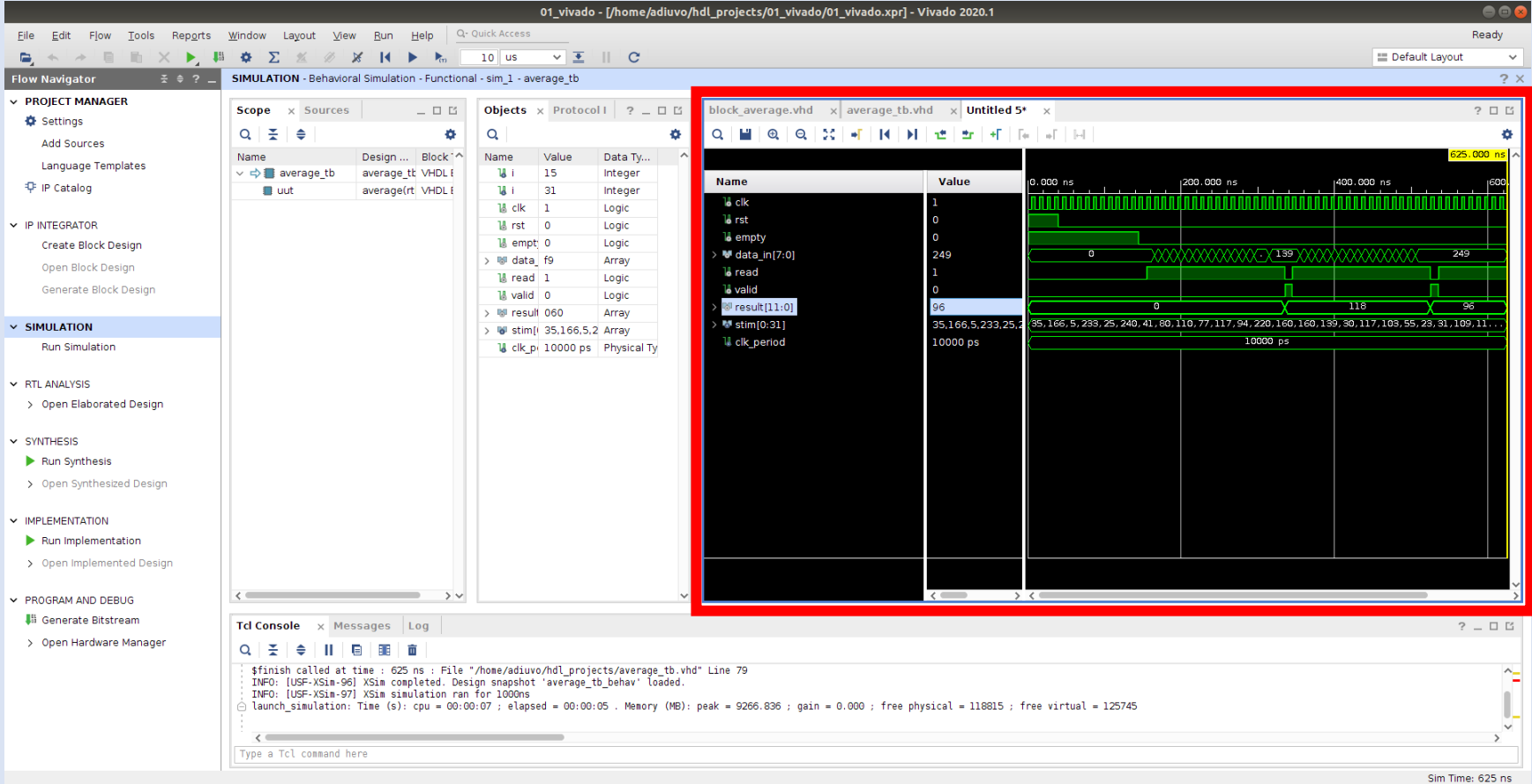
Lab 1: Overview and Introduction to Vivado

Step 16 – At the moment, the results are in hexadecimal but they make more sense in decimal. Select all the signals, right click, and select **unsigned decimal** from the radix.



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Step 17 – This will change the results to decimal. Correct operation has result showing 118 then 96. This is the block average of 16 input values.



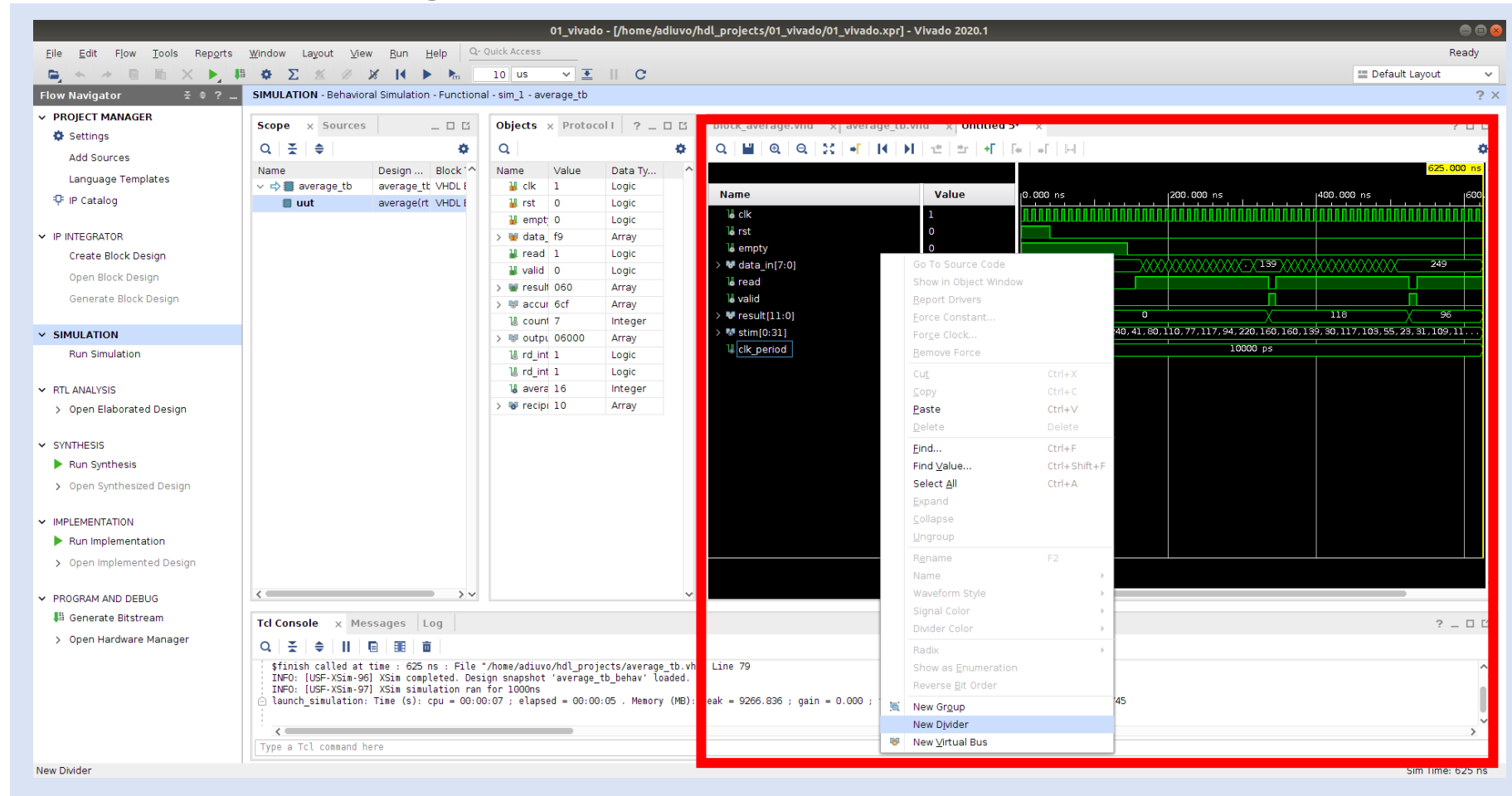
The screenshot displays the Vivado 2020.1 interface during a behavioral simulation. The left sidebar shows the Project Manager with the SIMULATION section selected. The main workspace is divided into several panels:

- Scope:** Shows the 'average_tb' testbench with a 'result' signal.
- Objects:** Lists the simulation objects, including 'result' with a value of 060.
- Timing Diagram:** Displays the waveform for the 'result' signal, showing a value of 118 at 625 ns.
- Tcl Console:** Shows the simulation results, including the message: "INFO: [USF-XSim-96] XSim completed. Design snapshot 'average_tb_behav' loaded."

The 'result' signal is highlighted in the Scope and Objects panels, and its value is shown in the Timing Diagram. The Tcl Console provides detailed simulation information, including the time taken for the simulation and the memory usage.

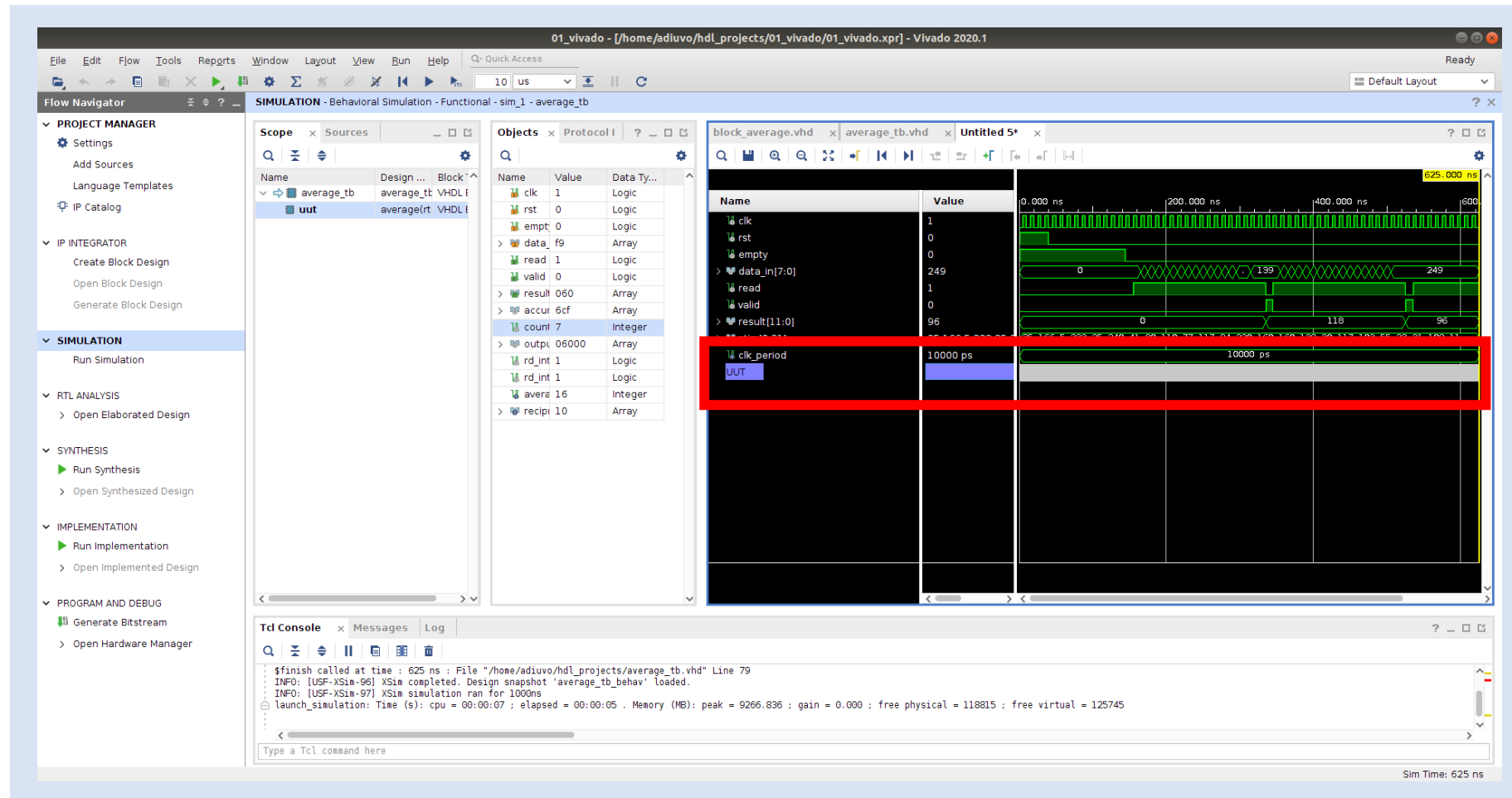
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Step 18 – Often we want to be able to see the signals in the UUT. To do this, first let's insert a divider. Right click on the **bottom signal** and select **New Divider**.



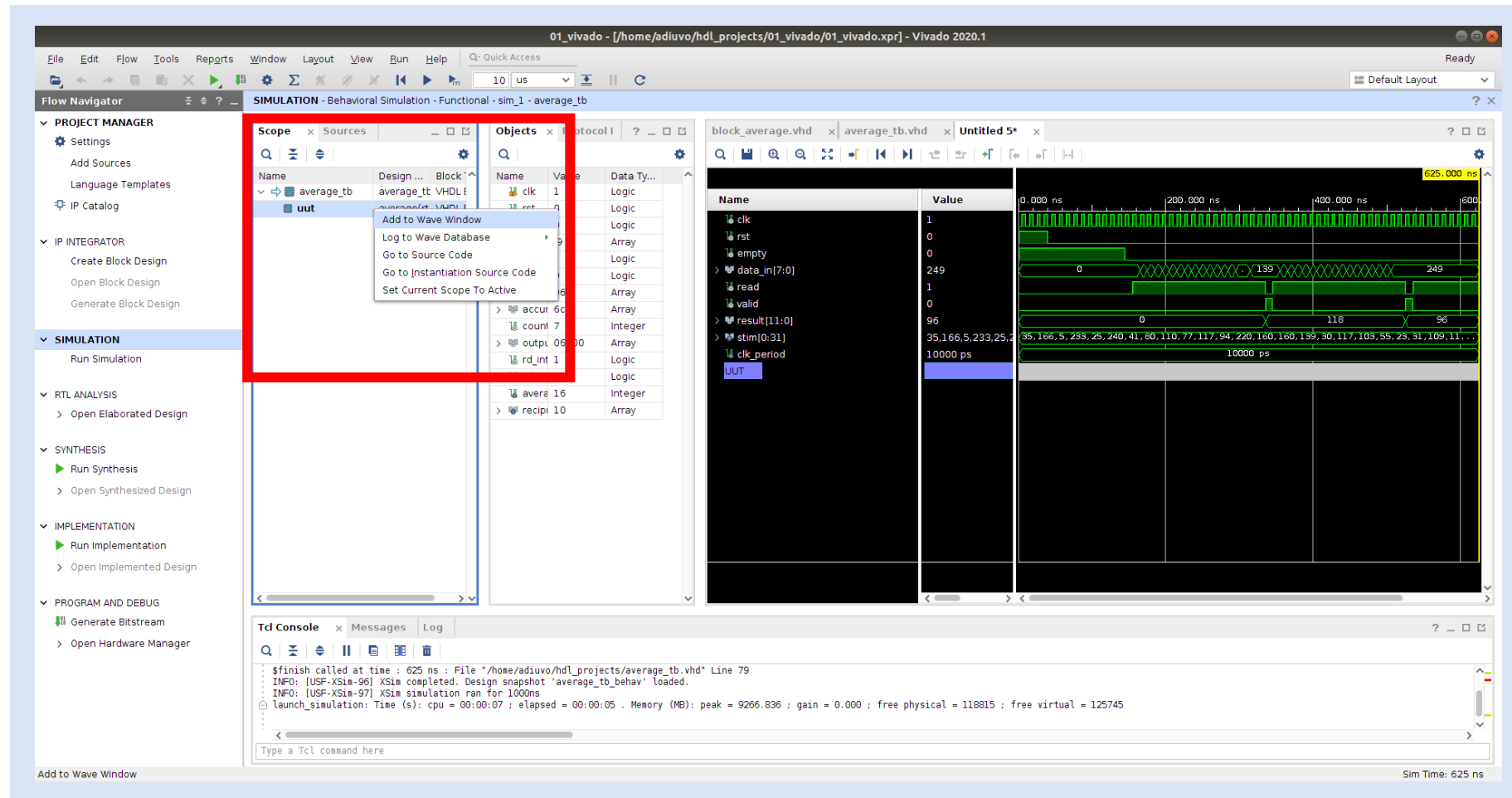
Lab 1: Overview and Introduction to Vivado

Step 19 – When prompted, enter the name **UUT** and you will see the new divider in the waveform.



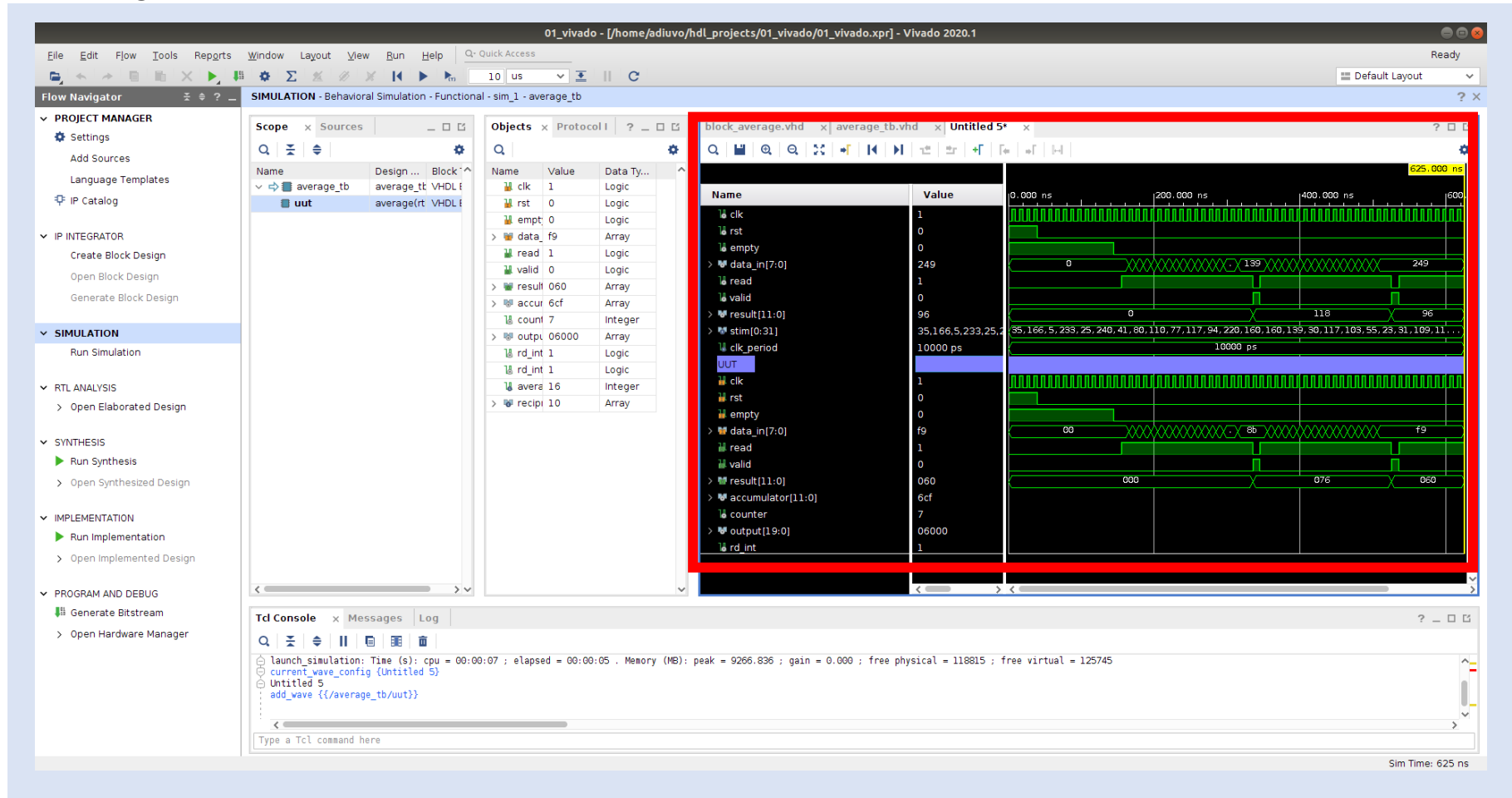
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Step 20 – To add in the UUT, right click on the **UUT** under the scope and select **Add to Wave Window**.



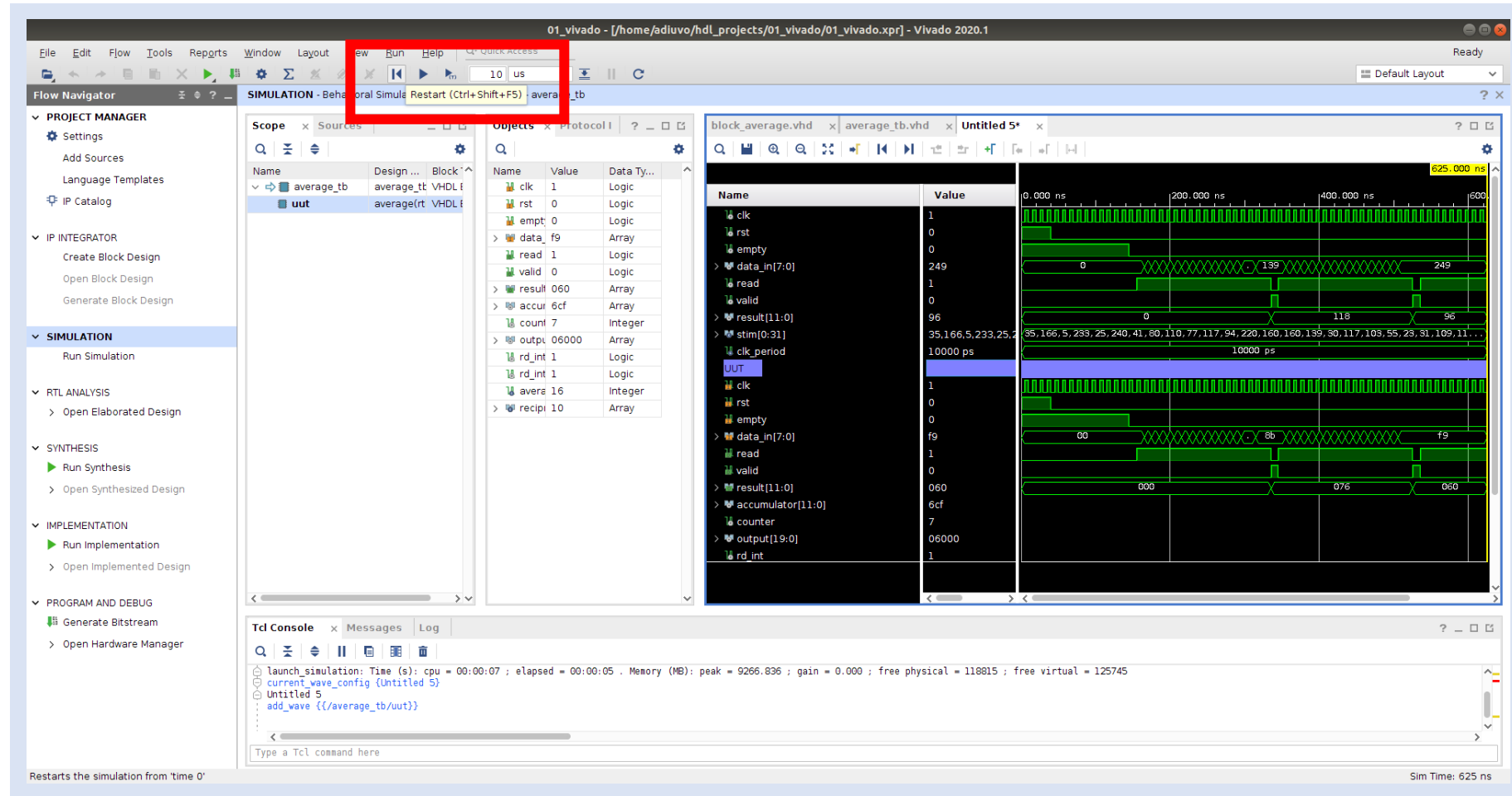
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Step 21 – This will add in the UUT signals, however, some information may be missing as it was not saved during the simulation.



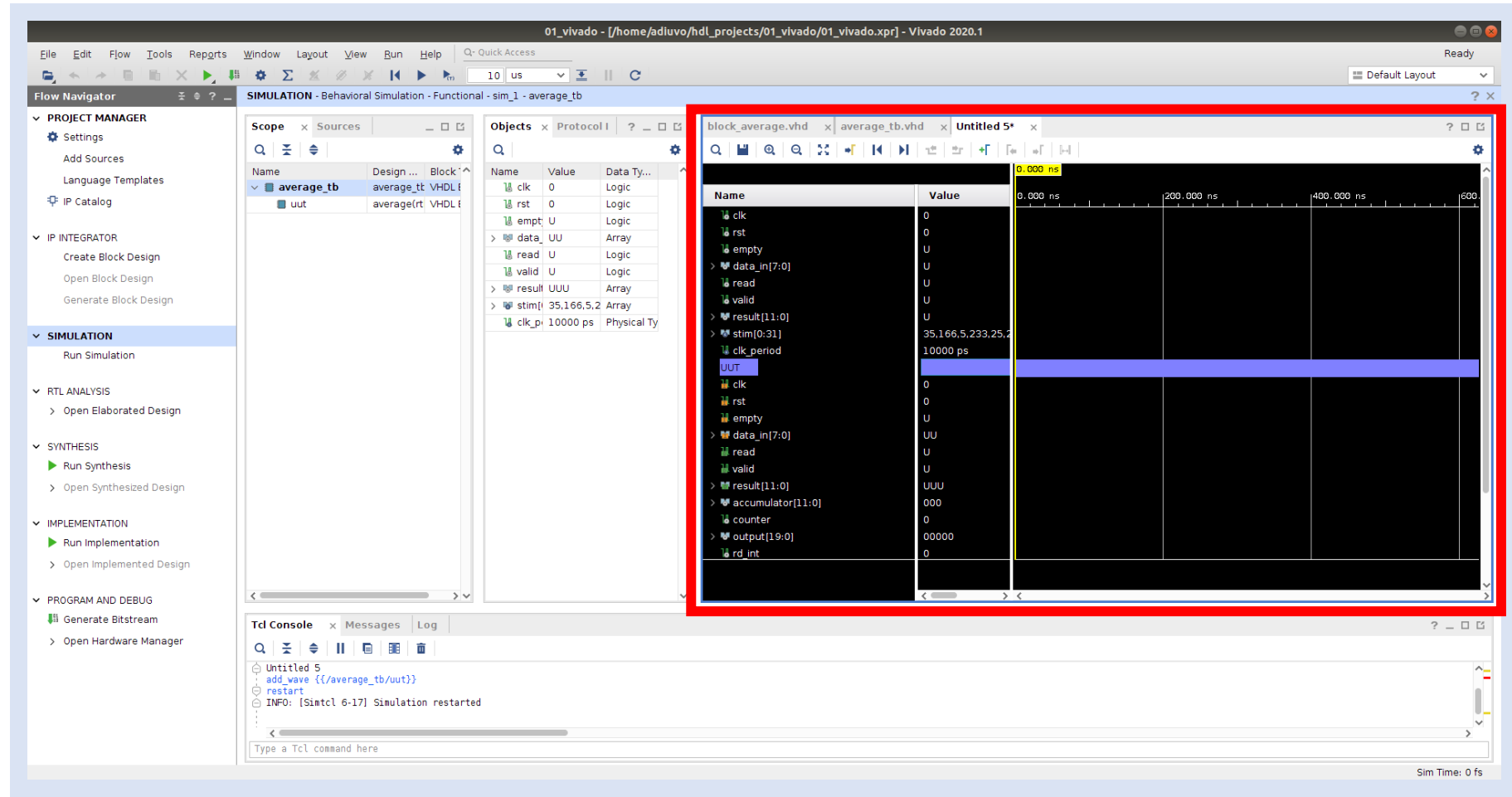
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Step 22 – To add in the missing waveform, we need to restart the simulation. Select **Restart** from menu bar.



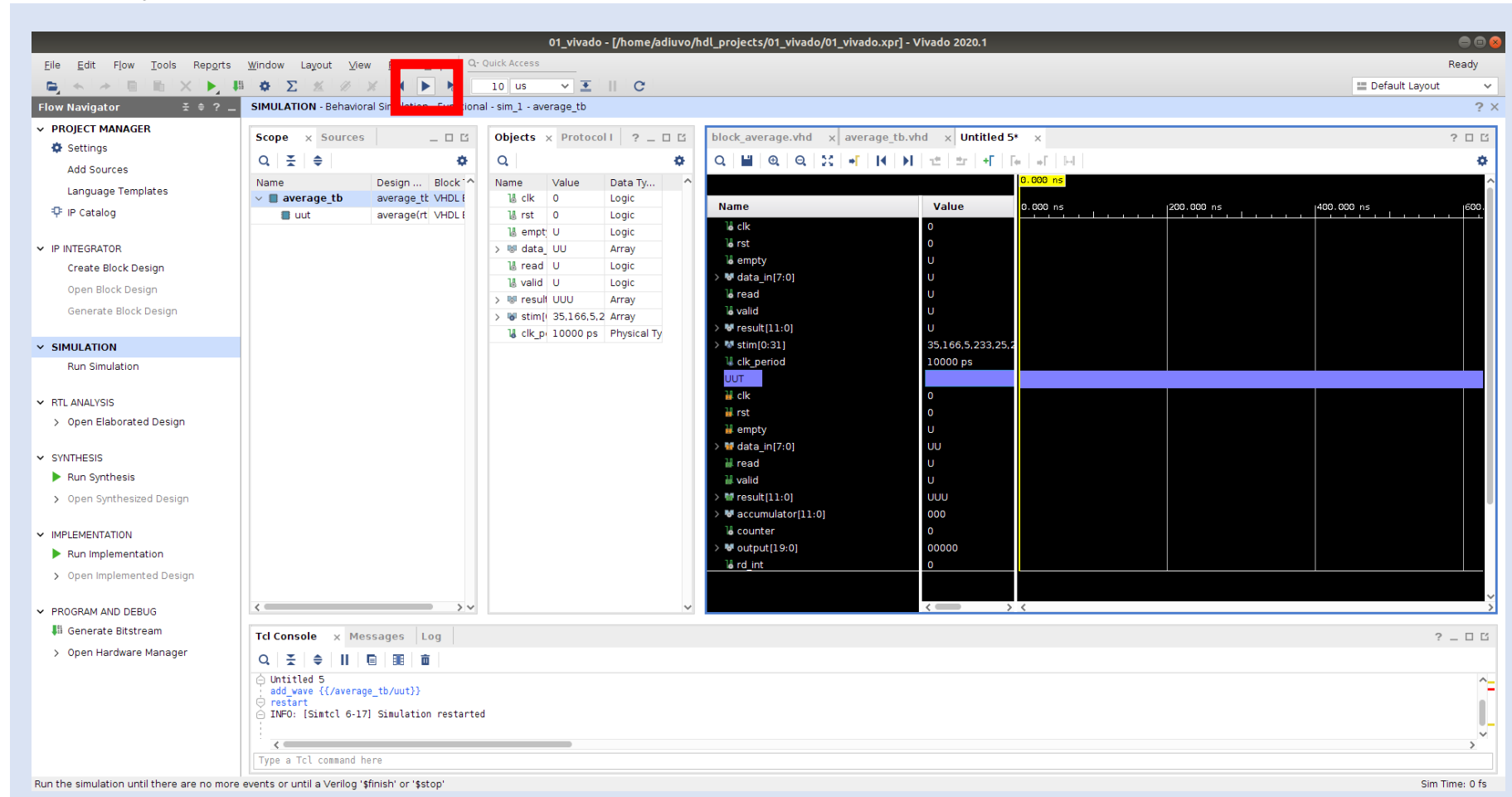
Lab 1: Overview and Introduction to Vivado

Step 23 – This will clear all waveform data and restart the simulation.



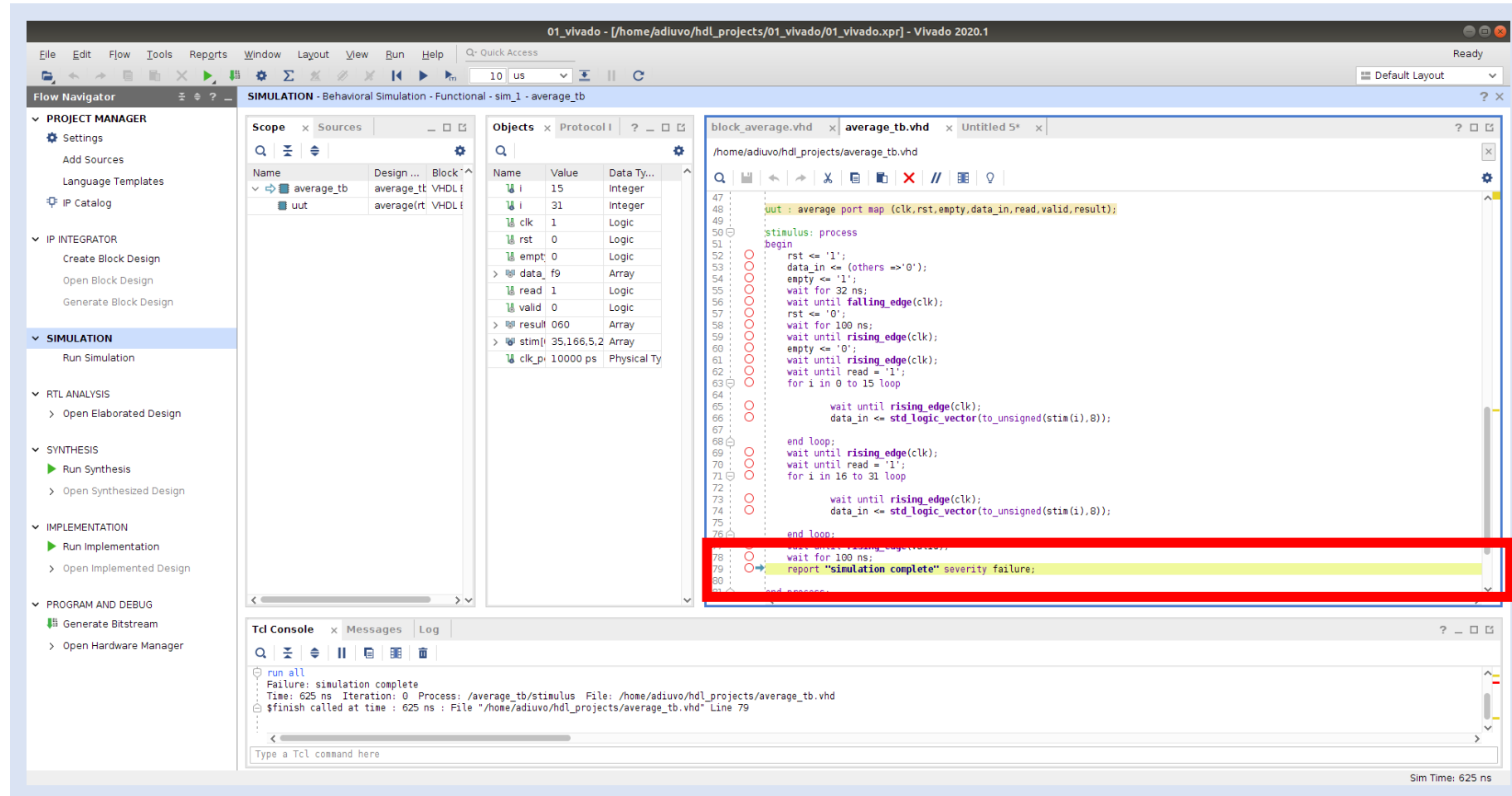
Lab 1: Overview and Introduction to Vivado

Step 24 – To rerun the simulation, select the **Run** button on the menu. The simulation will stop automatically.



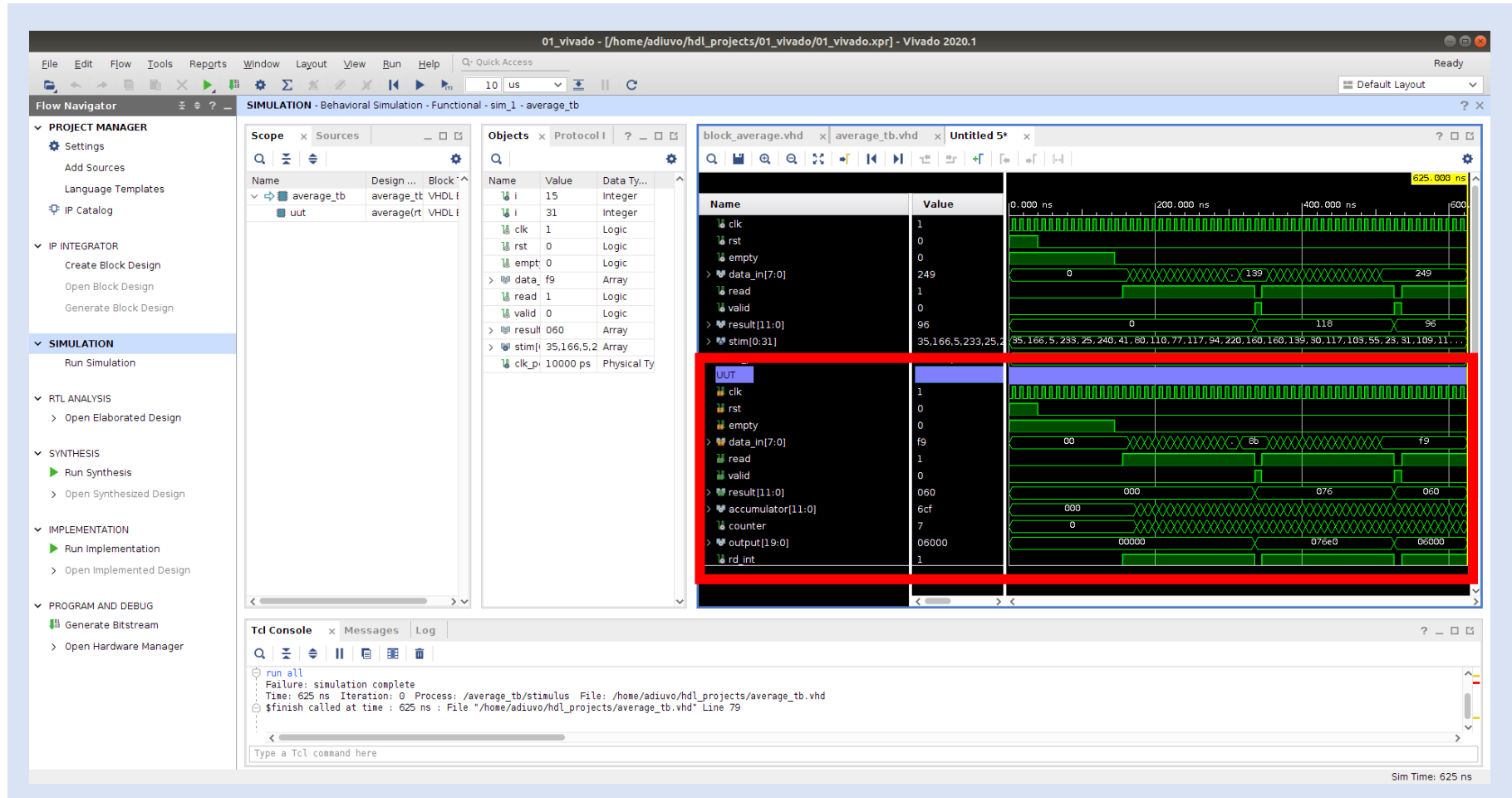
Lab 1: Overview and Introduction to Vivado

Step 25 – When the simulation completes, you will see the highlighted line in the test bench.



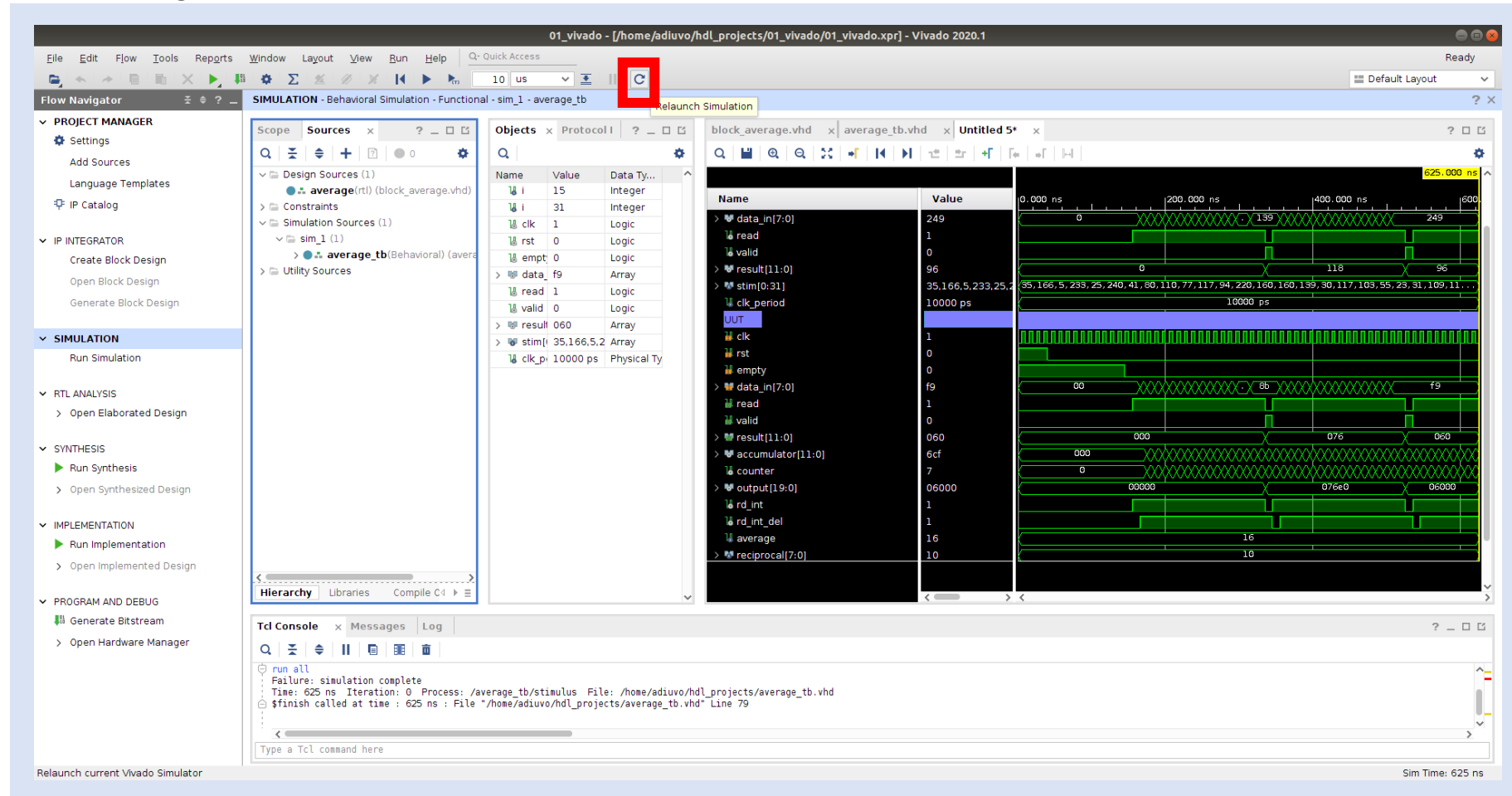
Lab 1: Overview and Introduction to Vivado

Step 26 – Selecting the **waveform tab** again will show all the signals for the UUT.



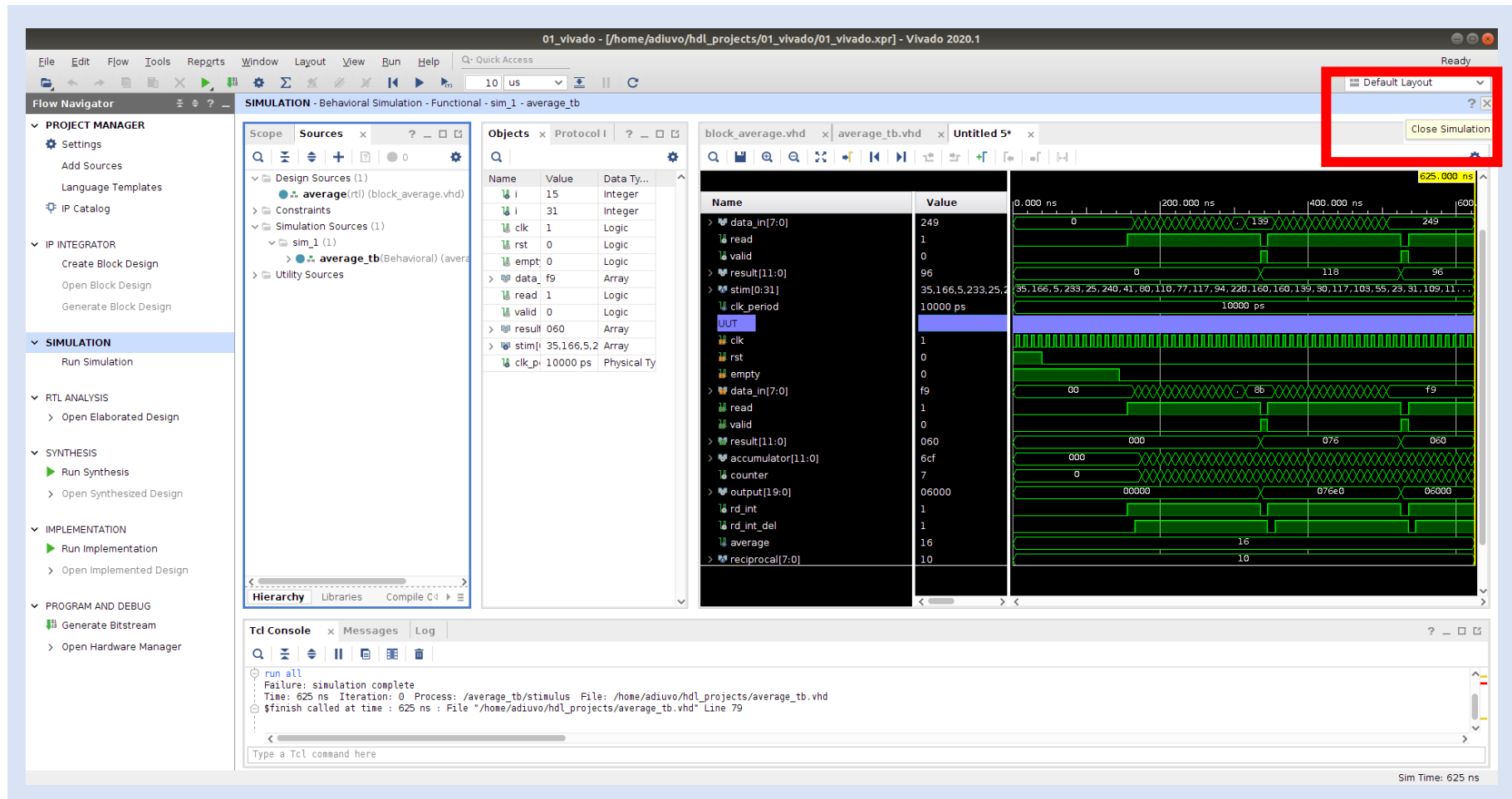
Lab 1: Overview and Introduction to Vivado

Step 27 – If you make changes to the source code, you need to relaunch the simulation. This can be achieved using the relaunch button on the menu.



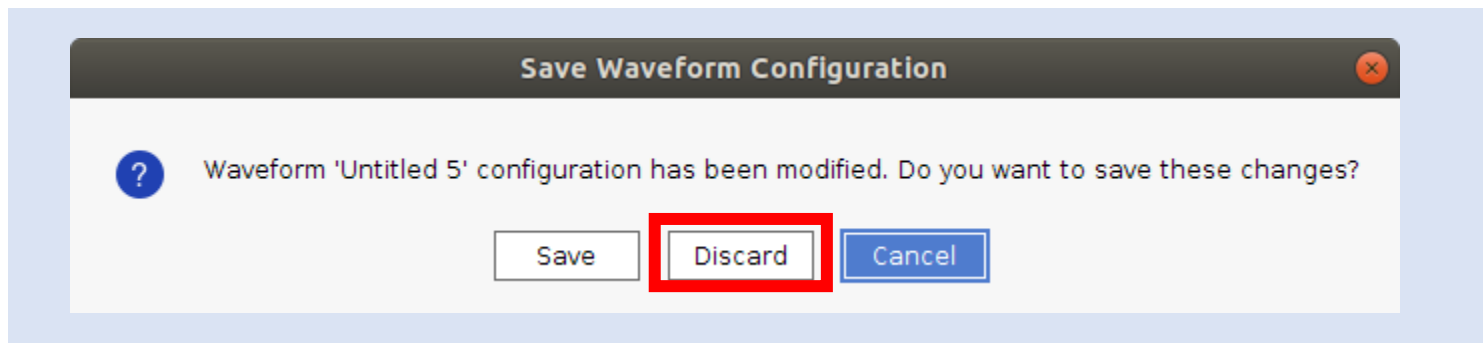
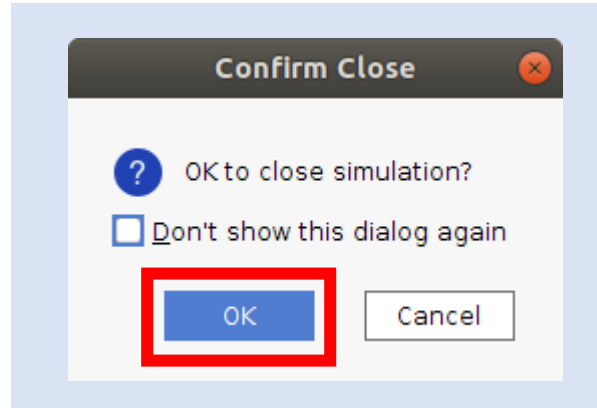
Lab 1: Overview and Introduction to Vivado

Step 28 – With the simulation complete, we are now ready to implement the design. Close the simulation view.



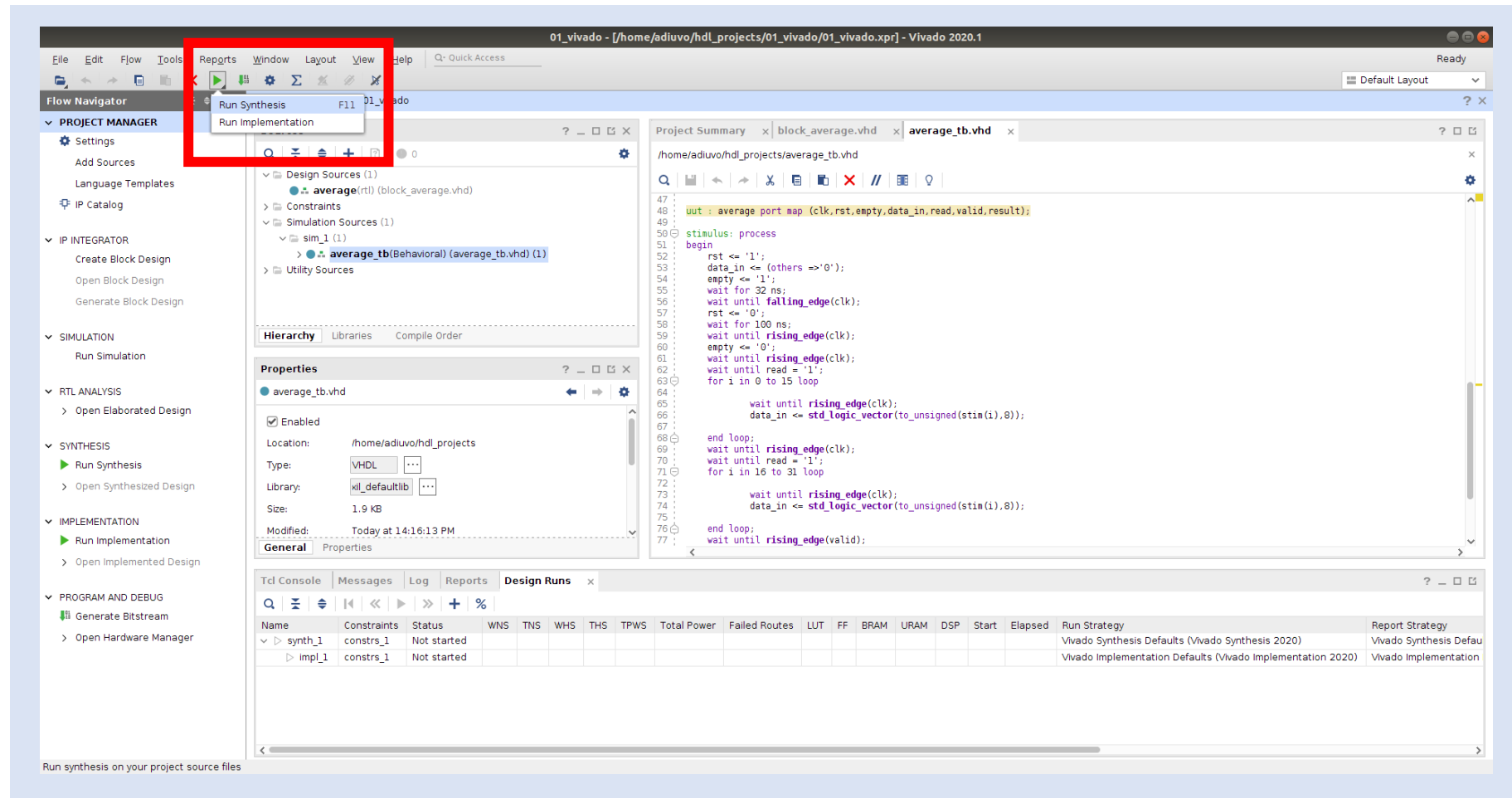
Lab 1: Overview and Introduction to Vivado

Step 29 – When asked to confirm, click **OK**. If a save waveform dialog pops up, select **Discard**.



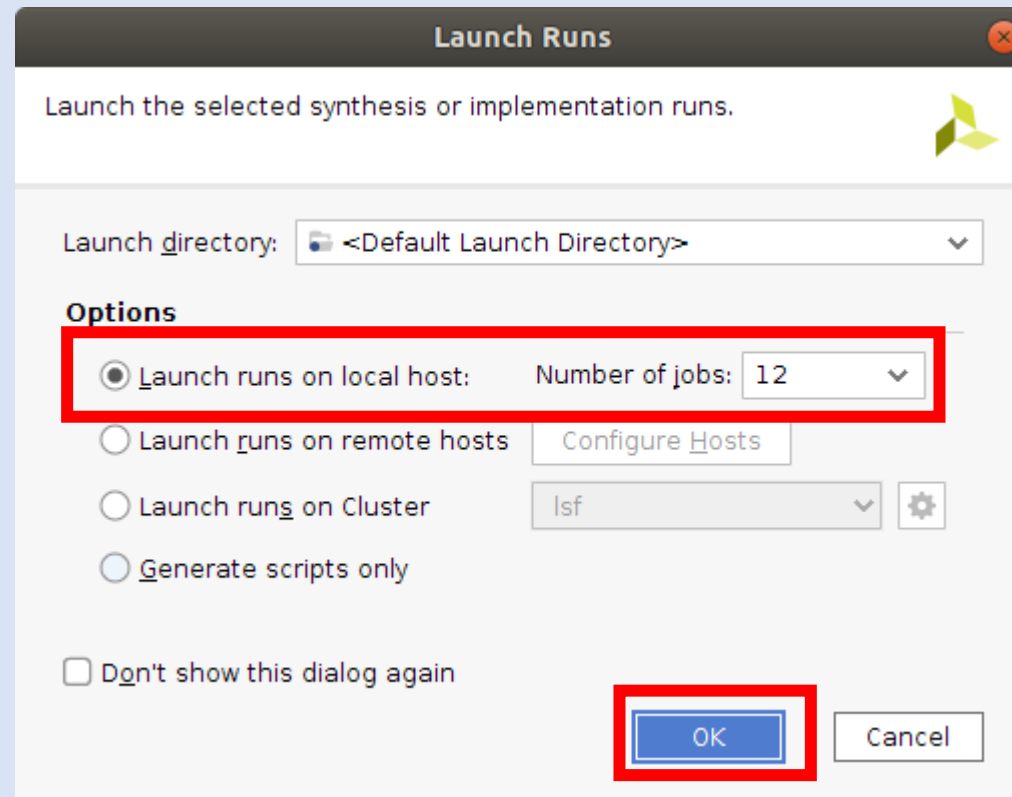
Lab 1: Overview and Introduction to Vivado

Step 30 – To synthesize the design, click the **green run arrow** and select **Run Synthesis**.



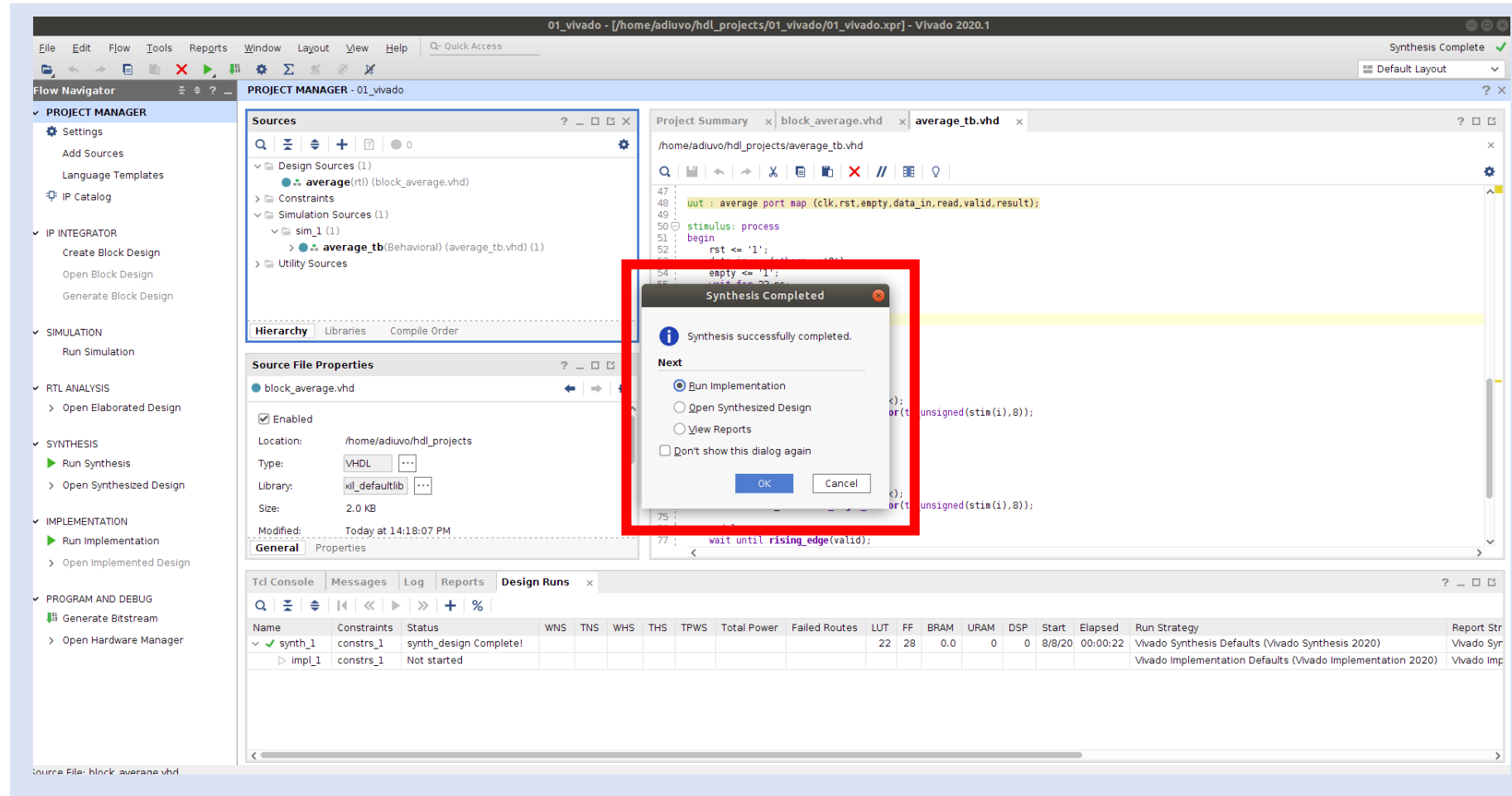
Lab 1: Overview and Introduction to Vivado

Step 31 – On the Launch Runs dialog, select the number of jobs you want to run on your system and click **OK**.



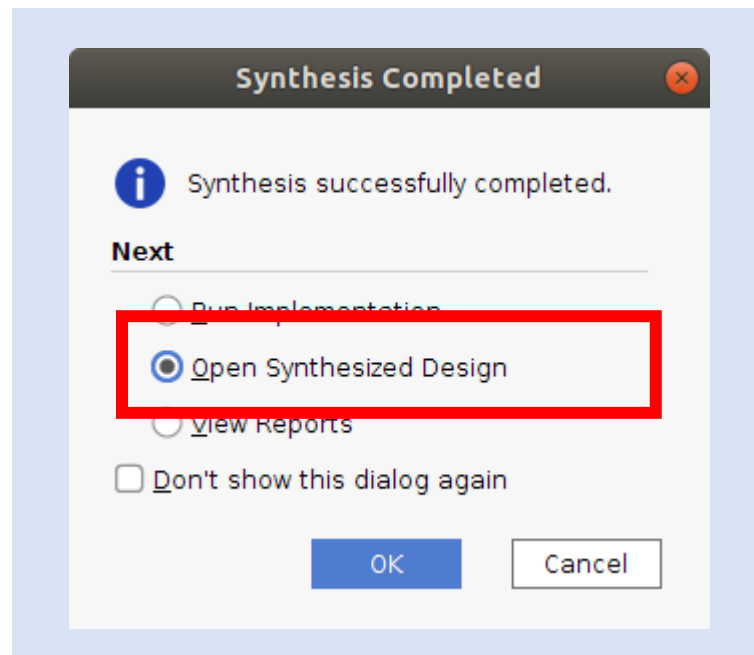
Lab 1: Overview and Introduction to Vivado

Step 32 – When synthesis is complete, you will see a dialog box appear.



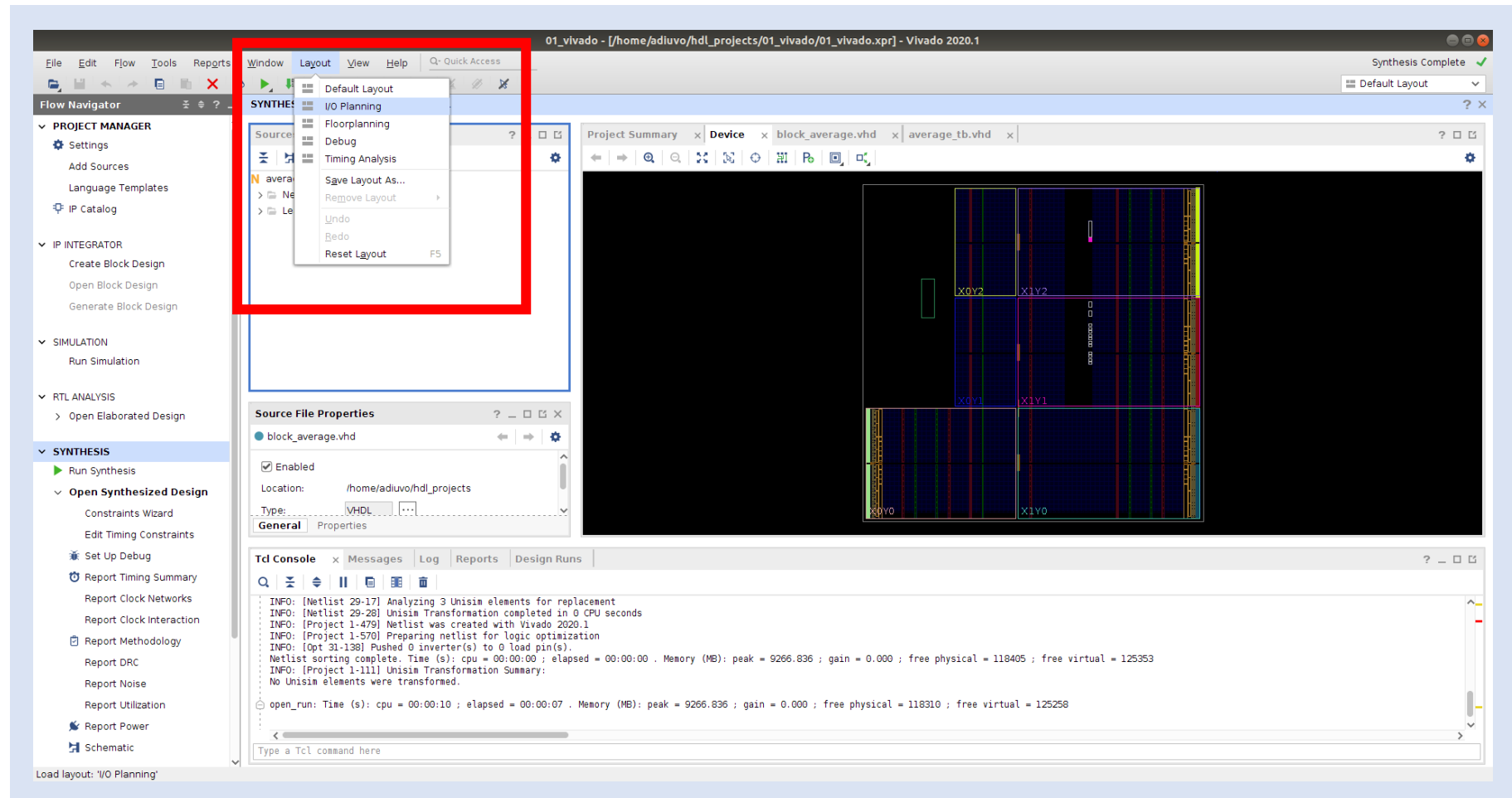
Lab 1: Overview and Introduction to Vivado

Step 33 – Select Open Synthesized Design.



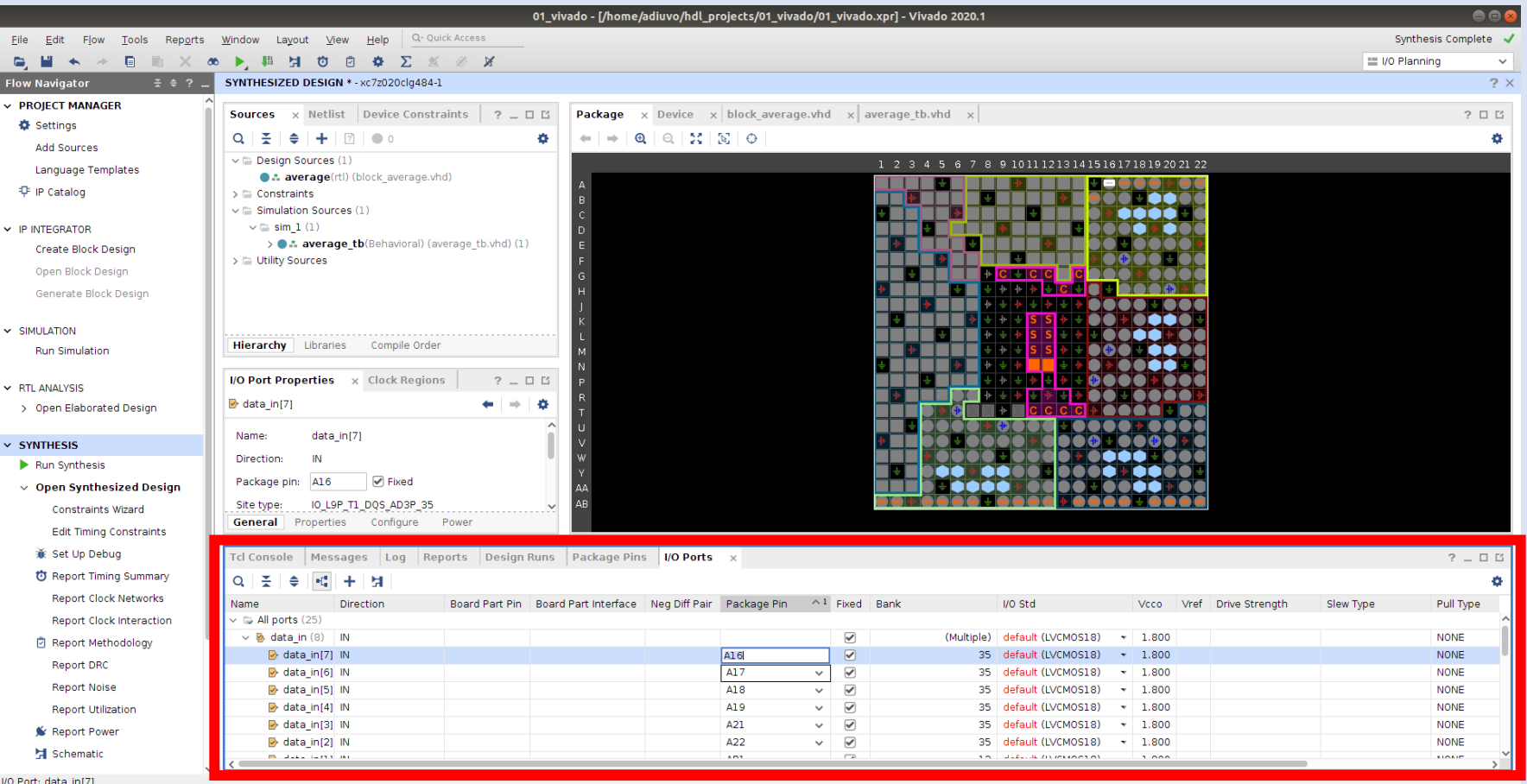
Lab 1: Overview and Introduction to Vivado

Step 34 – This will open the synthesis view. From the menu layout, select **I/O Planning**.



Lab 1: Overview and Introduction to Vivado

Step 35 – Expand the Data_In, Result and Scalar Ports and assign them to pins. All EXCEPT the clock pin can be assigned to any pin.



The screenshot shows the Vivado 2020.1 interface. The left sidebar contains the Project Manager, IP Integrator, Simulation, RTL Analysis, and Synthesis sections. The main window displays the Synthesized Design, showing the Sources, Netlist, and Package tabs. The I/O Port Properties window is open, showing the properties for 'data_in[7]'. The I/O Ports window is also open, showing a table of ports and their assignments to pins.

I/O Port Properties:

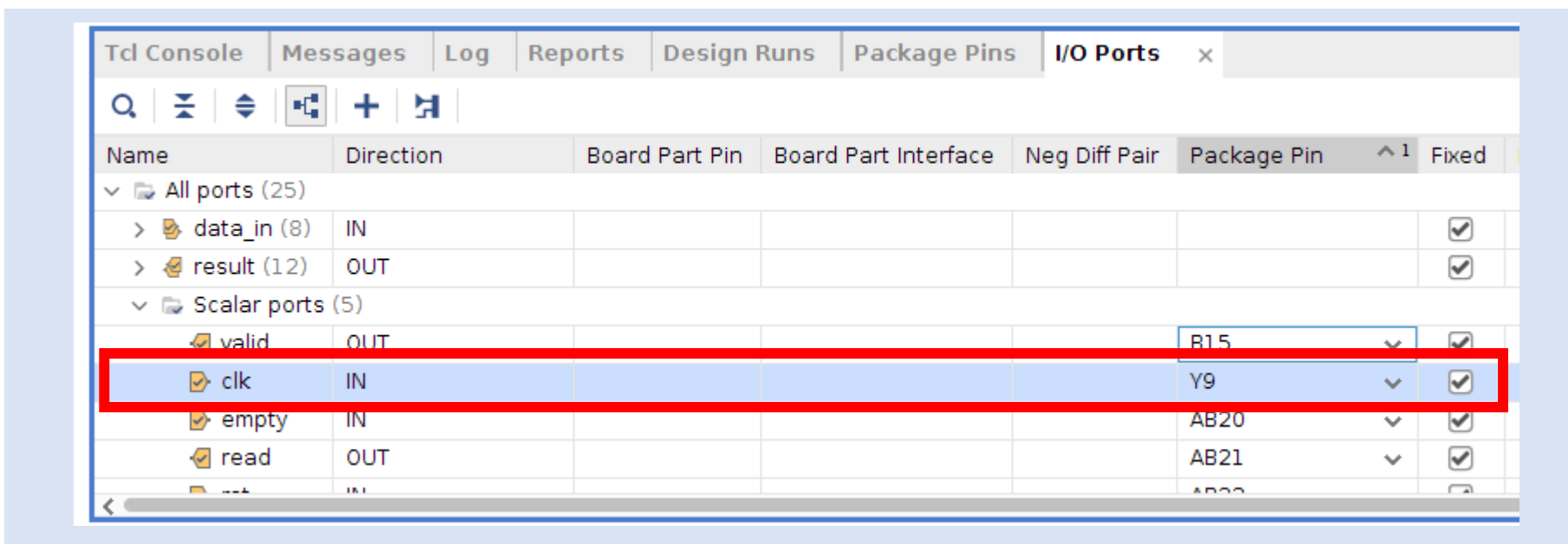
- Name: data_in[7]
- Direction: IN
- Package pin: A16
- Site type: IO_L9P_T1_DQS_AD3P_35

I/O Ports:

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type
data_in[8]	IN							(Multiple)	default (LVCMOS18)	1.800			NONE
data_in[7]	IN				A16			35	default (LVCMOS18)	1.800			NONE
data_in[6]	IN				A17			35	default (LVCMOS18)	1.800			NONE
data_in[5]	IN				A18			35	default (LVCMOS18)	1.800			NONE
data_in[4]	IN				A19			35	default (LVCMOS18)	1.800			NONE
data_in[3]	IN				A21			35	default (LVCMOS18)	1.800			NONE
data_in[2]	IN				A22			35	default (LVCMOS18)	1.800			NONE

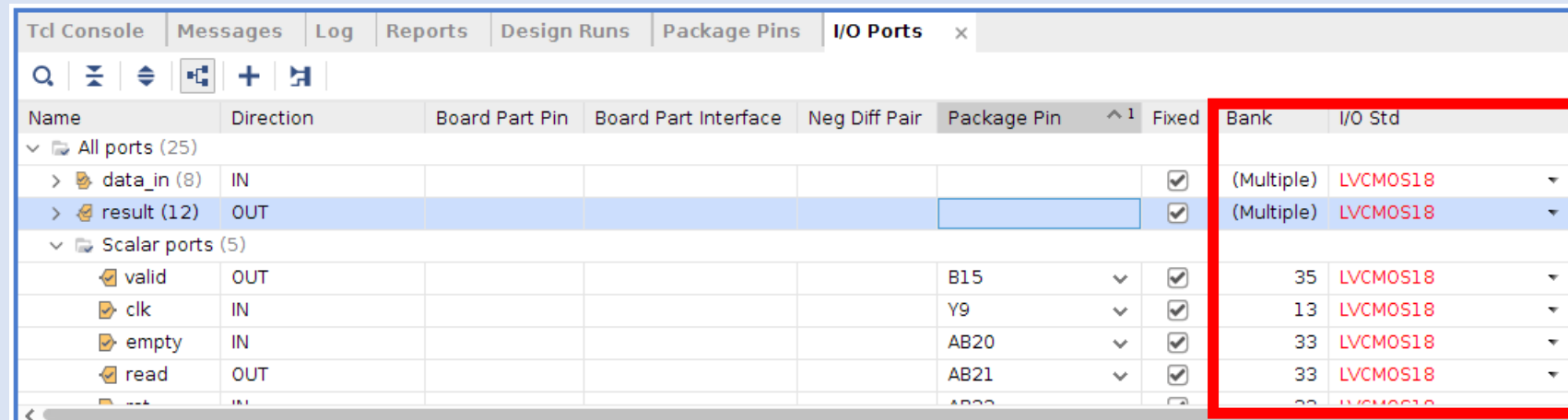
Lab 1: Overview and Introduction to Vivado

Step 36 – Assign the **clock pin to Y9**. Clocks have to be assigned to clock capable pins.



Lab 1: Overview and Introduction to Vivado

Step 37 – Ensure the **IO Standard** is set to **LVC MOS18**. Do not leave it as default because this will lead to a failure to implement and generate a bitstream.

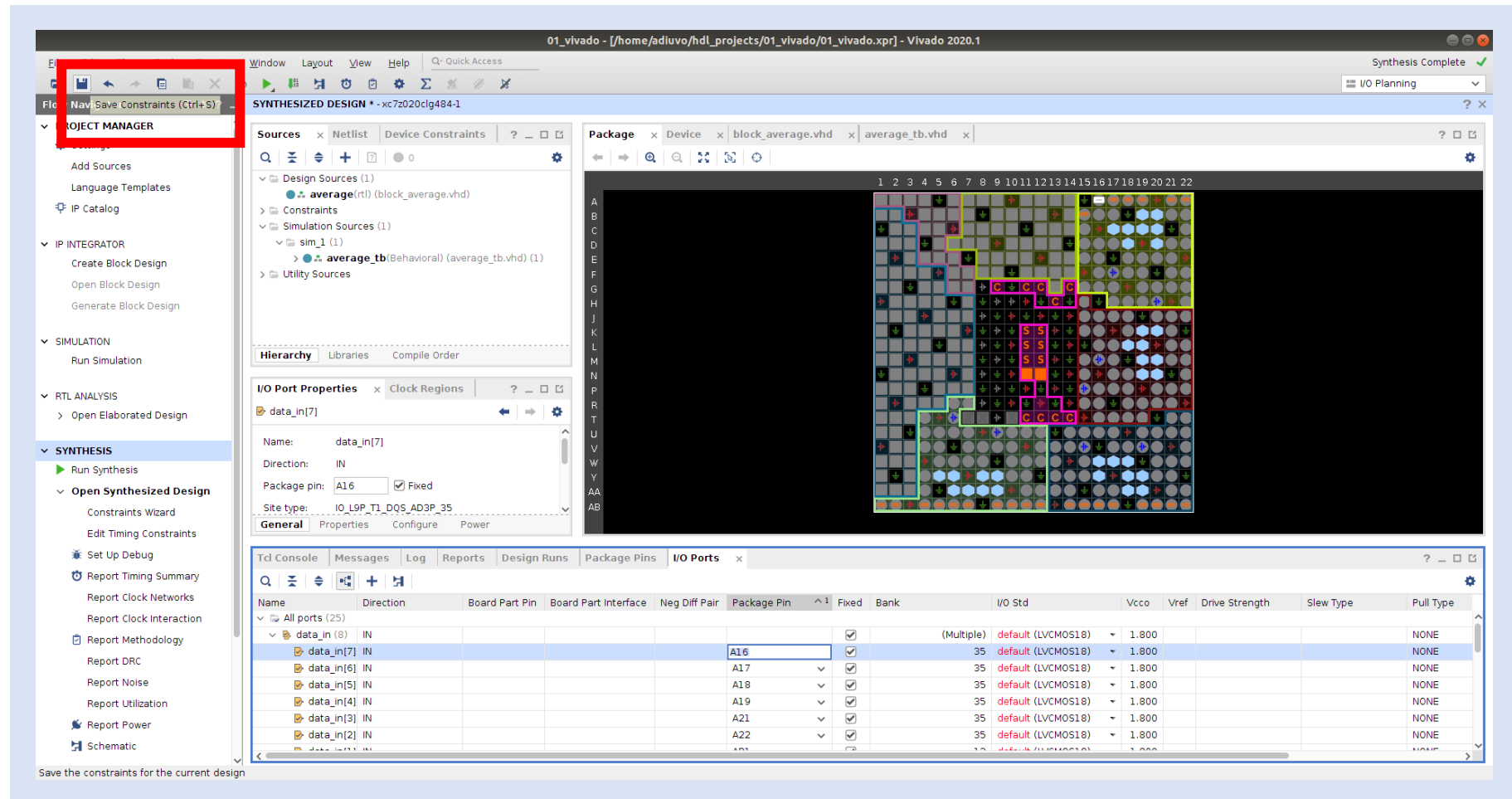


The screenshot shows the 'I/O Ports' window in Vivado. The table lists various ports and their configurations. A red box highlights the 'Bank' and 'I/O Std' columns, showing that all ports are configured with 'LVC MOS18' as the I/O standard.

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std
All ports (25)								
> data_in (8)	IN					<input checked="" type="checkbox"/>	(Multiple)	LVC MOS18
> result (12)	OUT					<input checked="" type="checkbox"/>	(Multiple)	LVC MOS18
Scalar ports (5)								
valid	OUT				B15	<input checked="" type="checkbox"/>	35	LVC MOS18
clk	IN				Y9	<input checked="" type="checkbox"/>	13	LVC MOS18
empty	IN				AB20	<input checked="" type="checkbox"/>	33	LVC MOS18
read	OUT				AB21	<input checked="" type="checkbox"/>	33	LVC MOS18

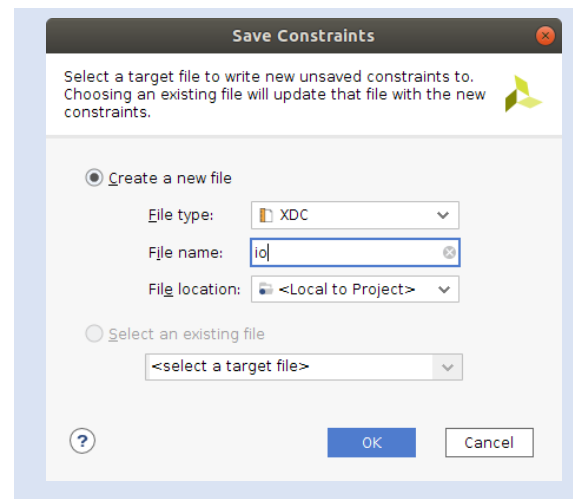
Lab 1: Overview and Introduction to Vivado

Step 38 – Save the Constraints we just edited.



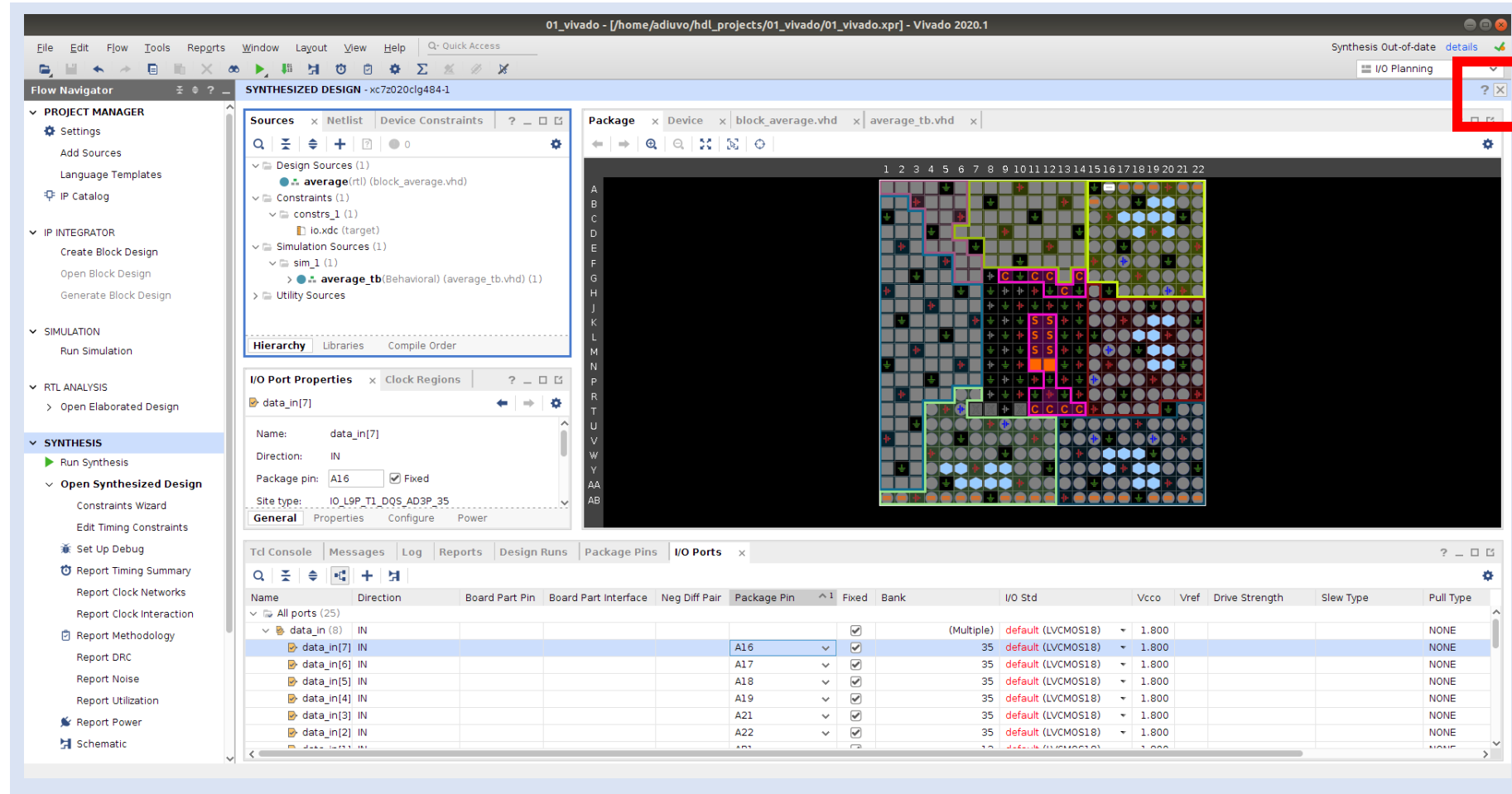
Lab 1: Overview and Introduction to Vivado

Step 39 – This will present two new dialogs. Click **OK** on the first and enter a **file name** for the second.



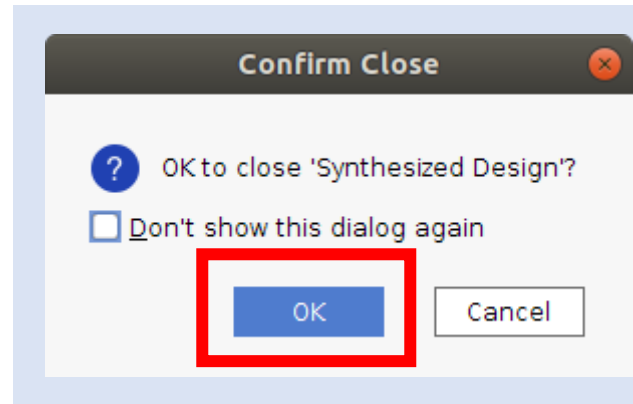
Lab 1: Overview and Introduction to Vivado

Step 40 – Close the Synthesis View.



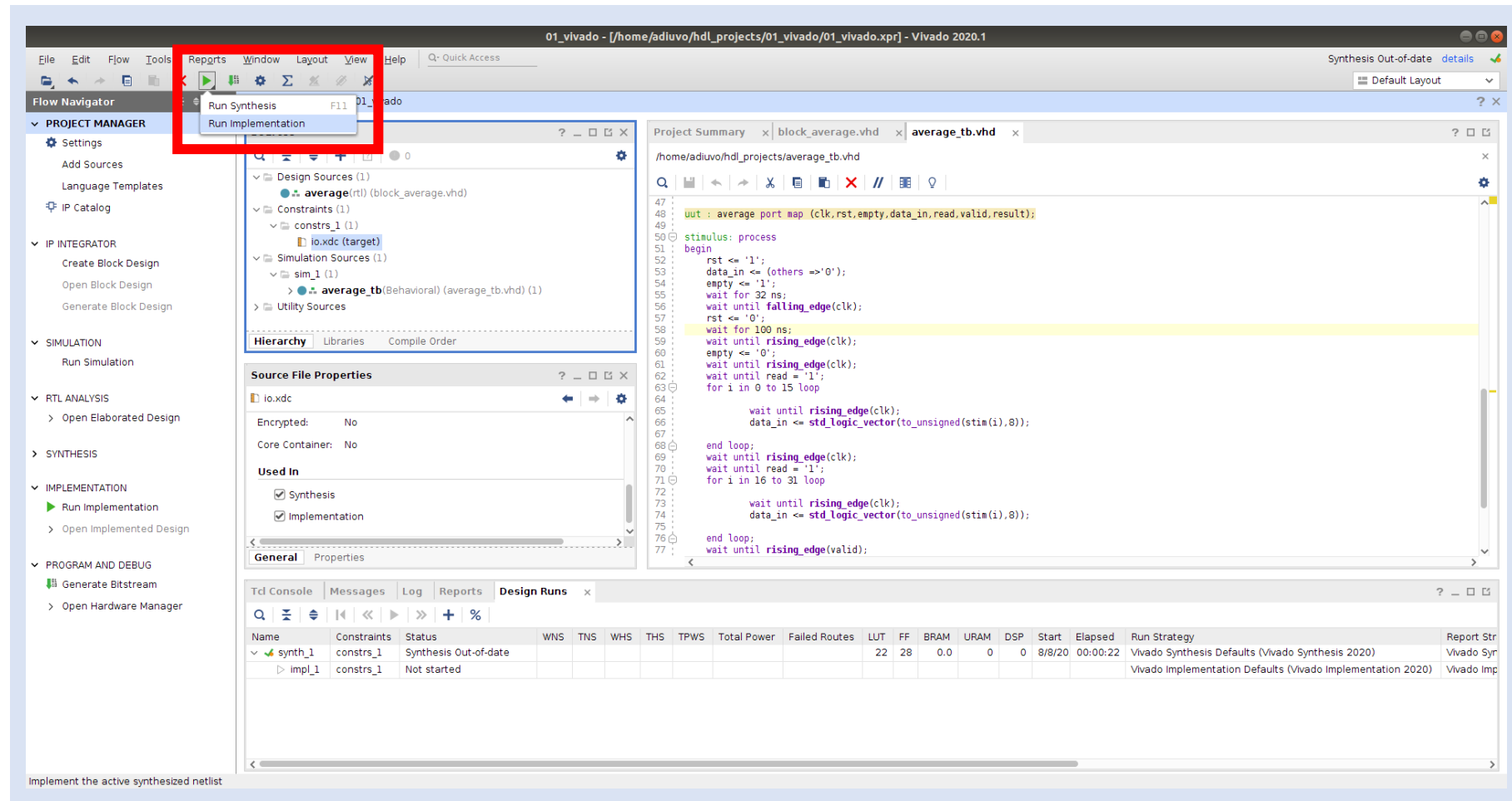
Lab 1: Overview and Introduction to Vivado

Step 41 – Confirm the decision to close by clicking **OK**. This will take us back to the project manager view.



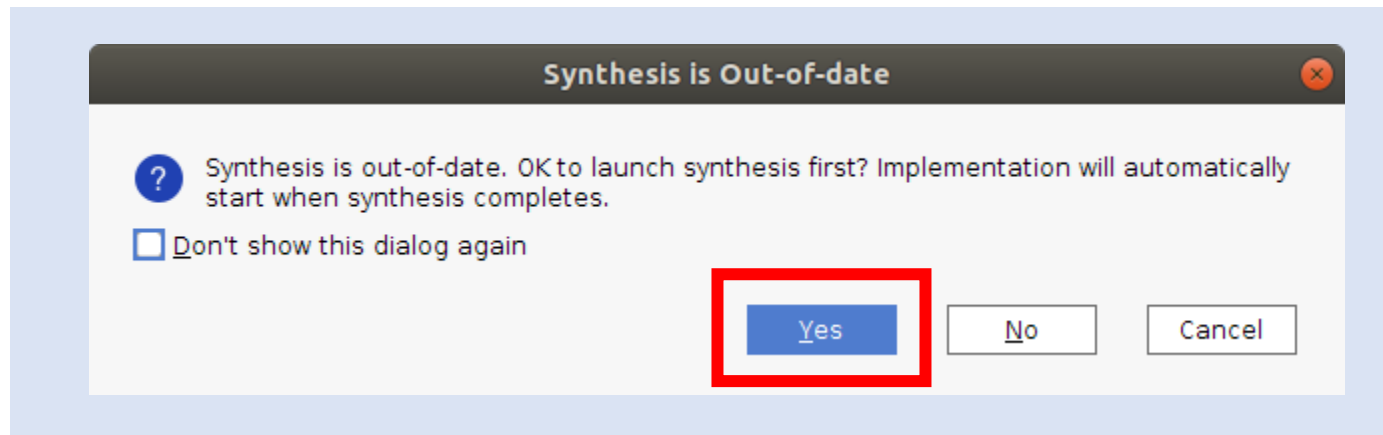
Lab 1: Overview and Introduction to Vivado

Step 42 – We are now ready to Run Implementation.



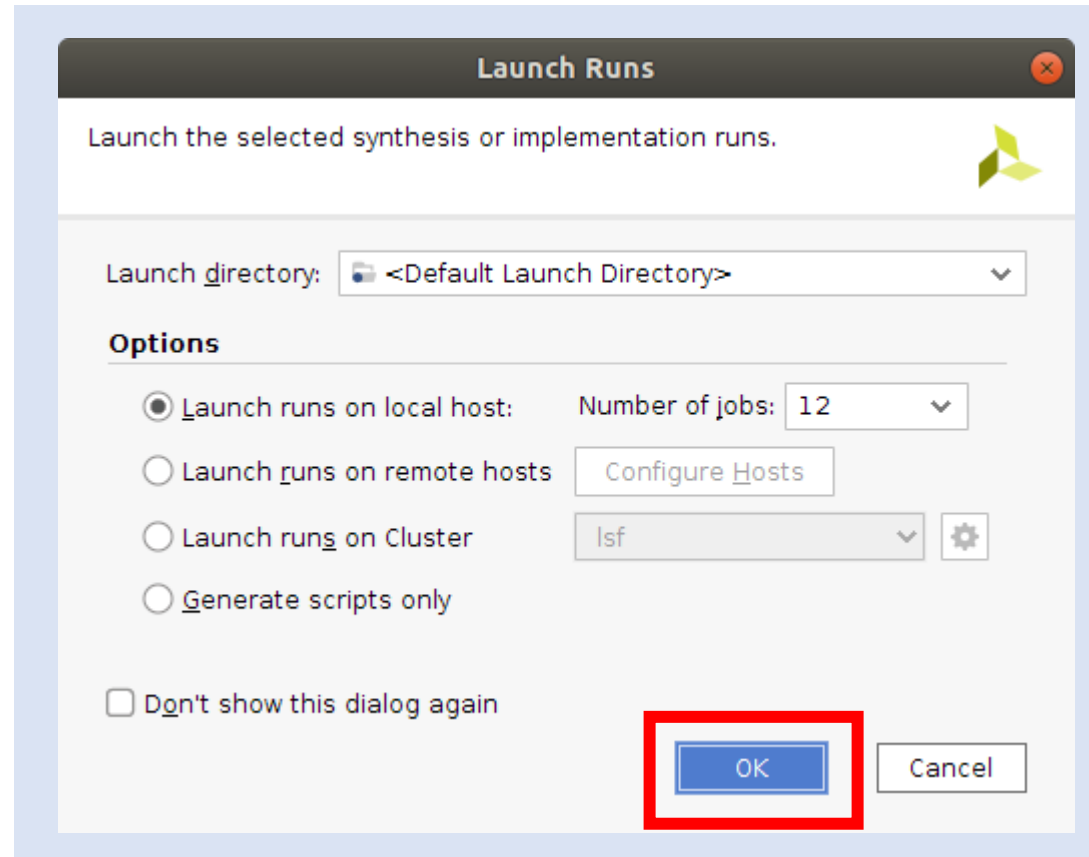
Lab 1: Overview and Introduction to Vivado

Step 43 – Click **Yes** when the Synthesis Out-of-Date dialog pops up.



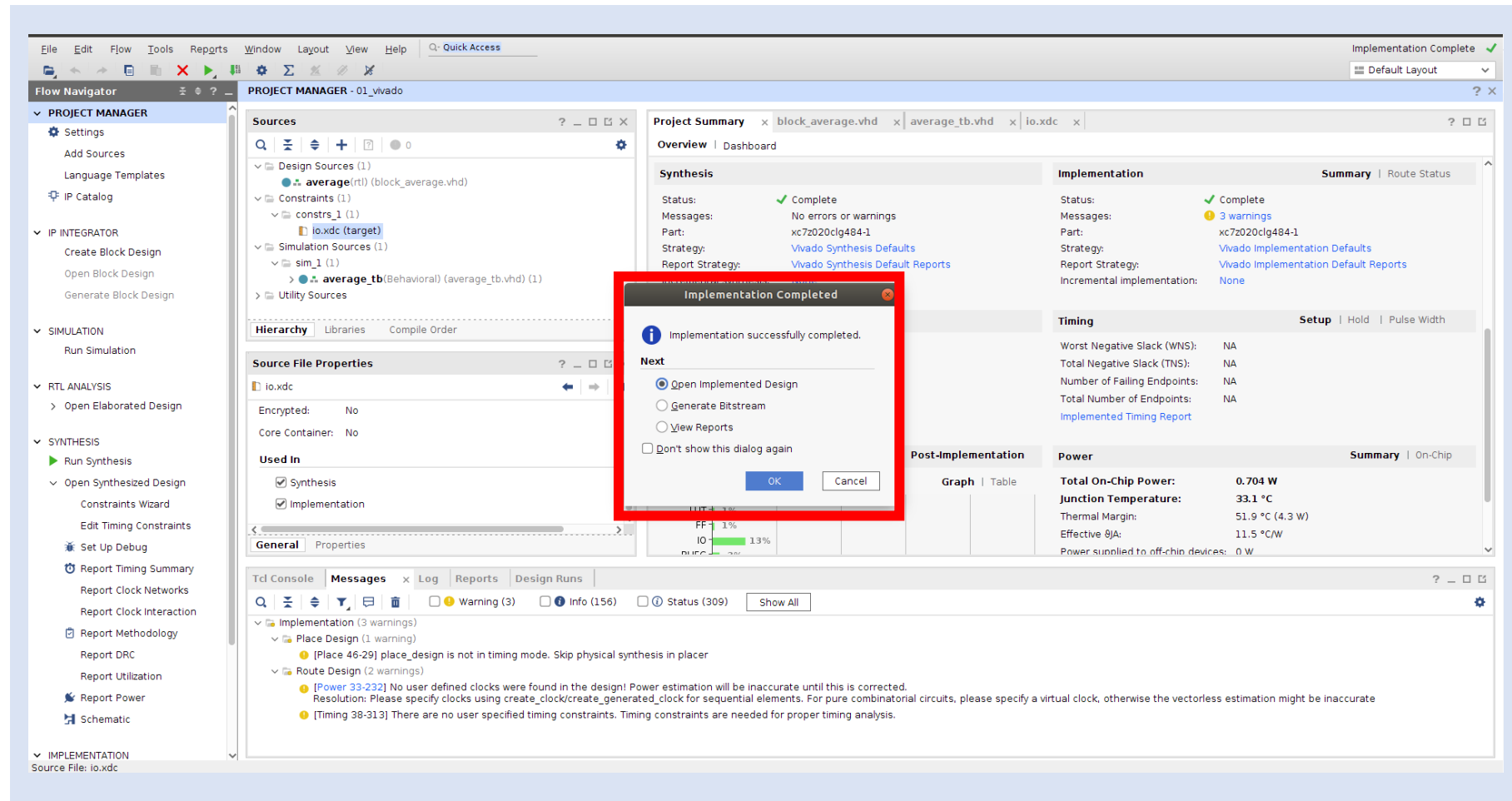
Lab 1: Overview and Introduction to Vivado

Step 44 – Select **OK** on the Launch Runs dialog.



Lab 1: Overview and Introduction to Vivado

Step 45 – When the implementation completes, you will see a dialog appear. Select **Generate Bitstream**.



Lab 1: Overview and Introduction to Vivado

Step 46 – A dialog box will appear when the bitstream generates. Congratulations you have completed your first Vivado FPGA implementation.

