

Getting to Know Vivado

Course Workbook

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About this Workbook

This workbook is designed to be used in conjunction with the Getting to Know Vivado course.

The contents of this workbook are created by Aduvo Engineering & Training, Ltd.

If you have any questions about the contents or need assistance, please contact Adam Taylor at adam@adiuvoengineering.com.

Pre-Lab

Workshop Pre-requisites

Required Hardware

There is no required hardware for this course.

Downloads and Installations

Step 1 – Download and install the following at least one day prior to the workshop. This may take a significant amount of time and drive space.

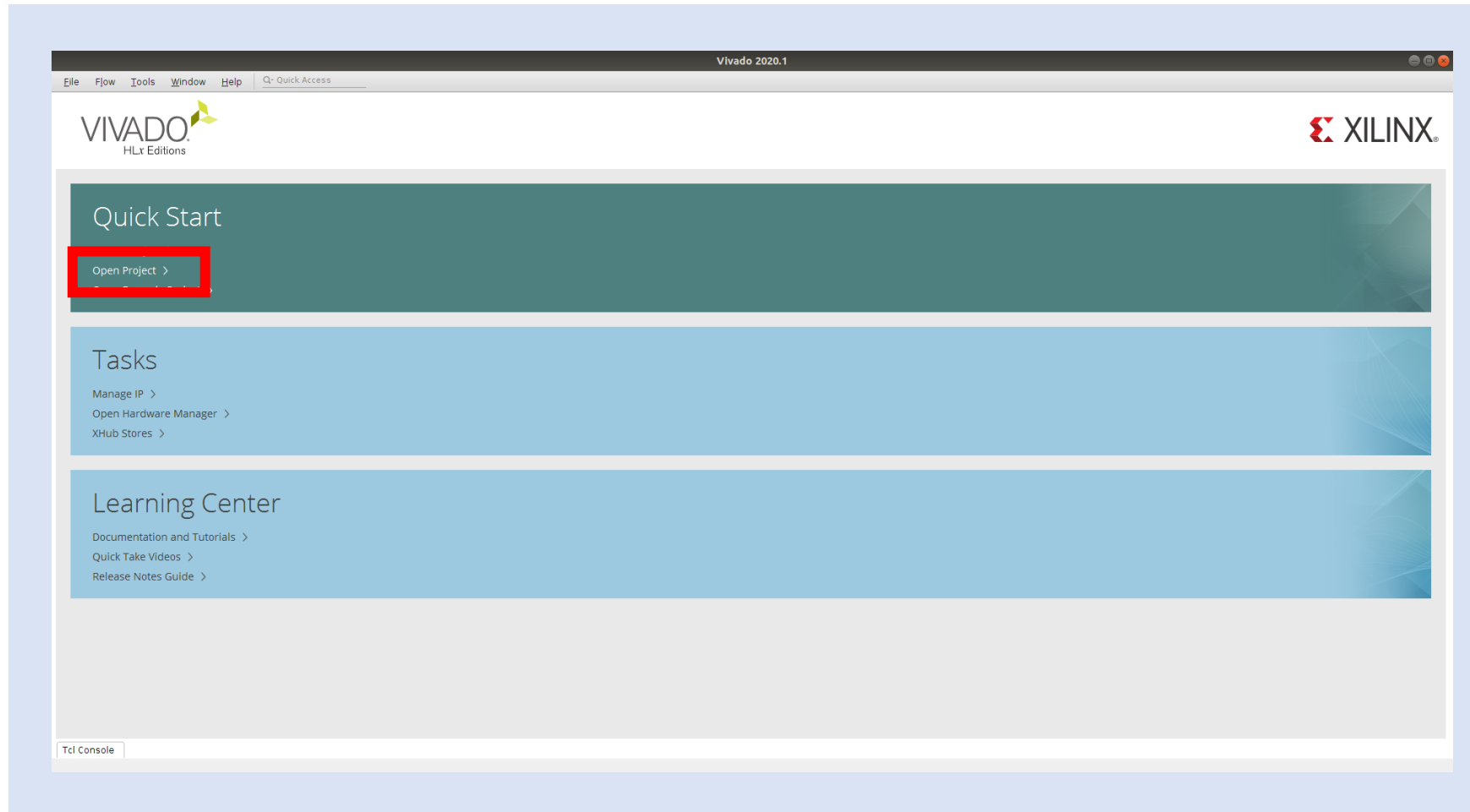
Vivado 2020.1	Download
Source Project Files	Download
Lab 1 must be completed	

Lab 2

Intermediate Vivado

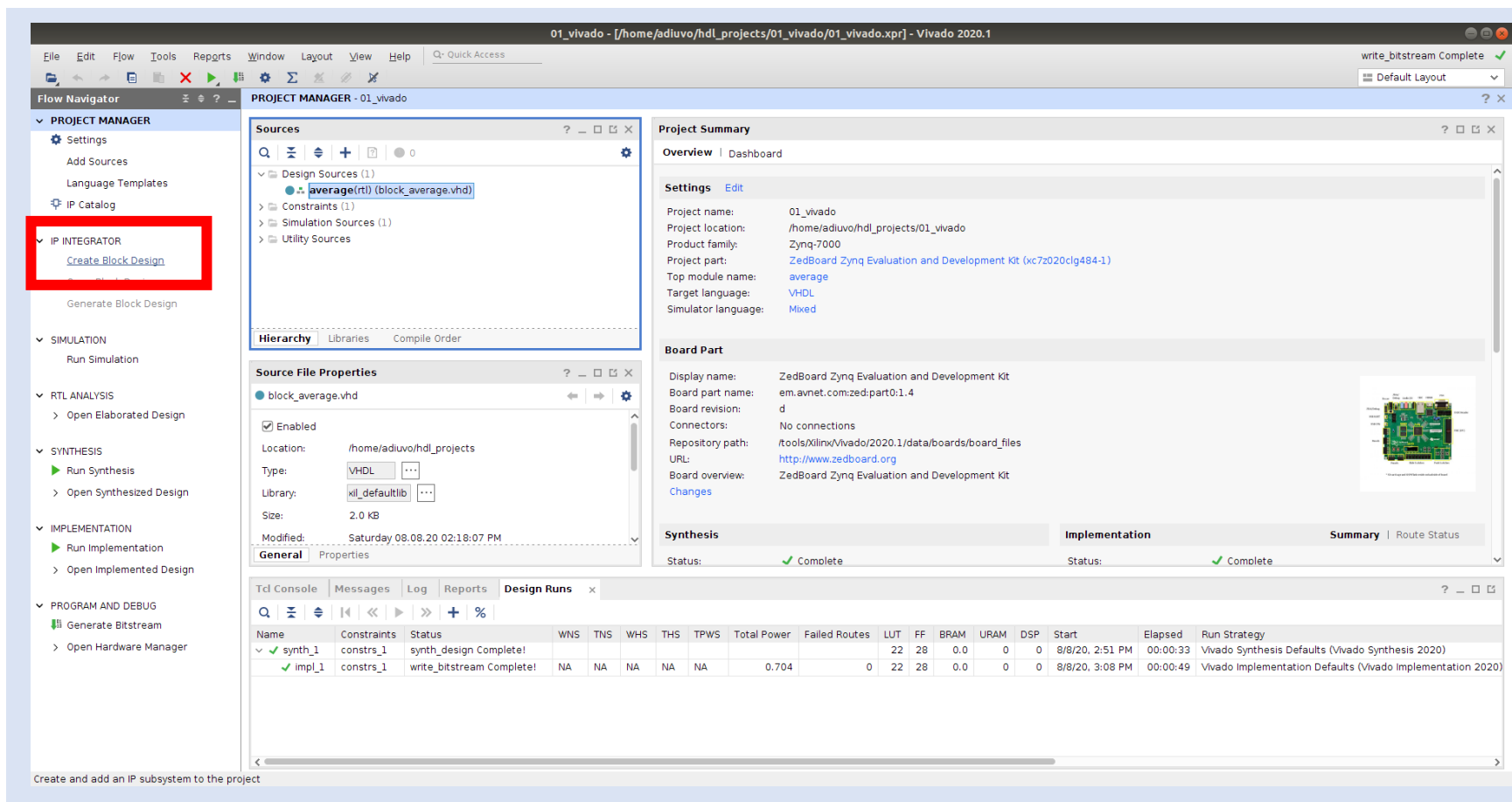
Lab 2: Intermediate Vivado

Step 1 – Open the project created in part one.



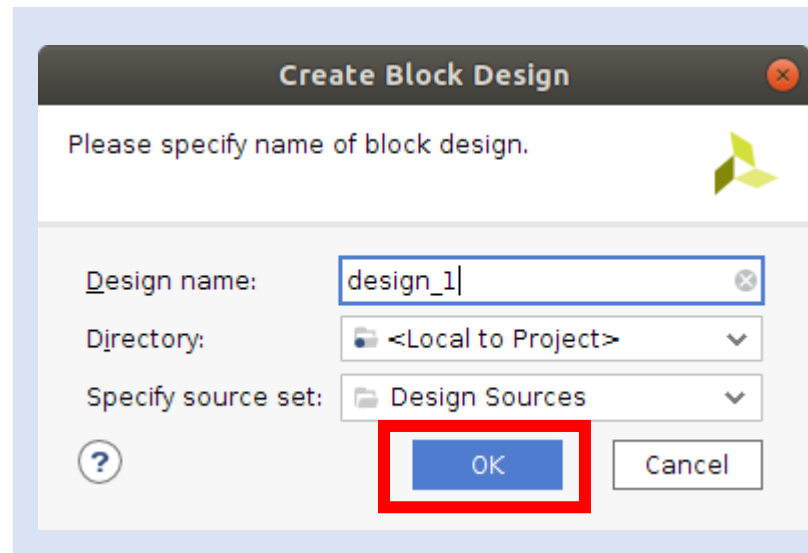
Lab 2: Intermediate Vivado

Step 2 – This will open in project management view. Click on **Create Block Diagram**.



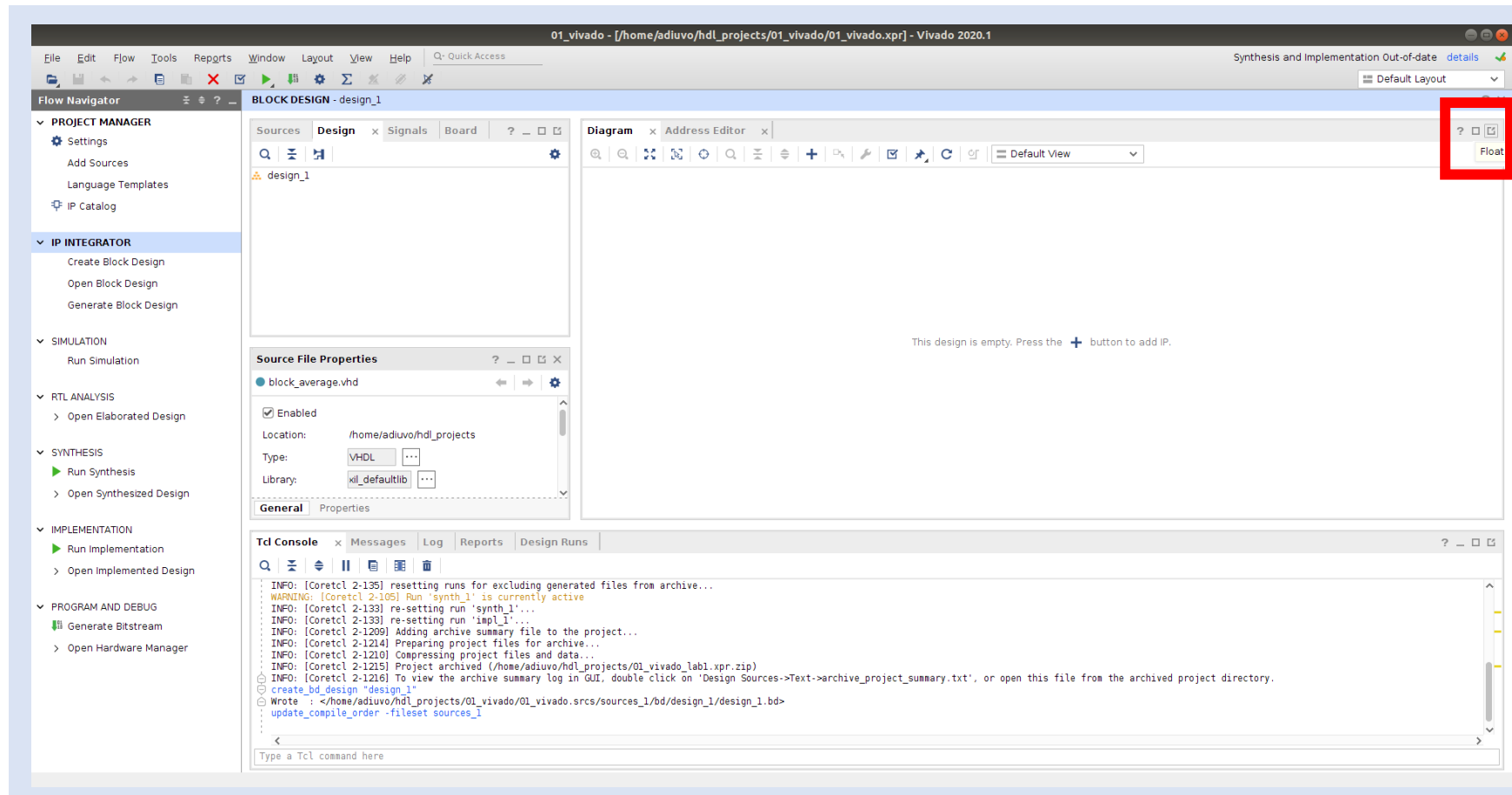
Lab 2: Intermediate Vivado

Step 3 – Leave the predefined name and locations unchanged and click **OK**.



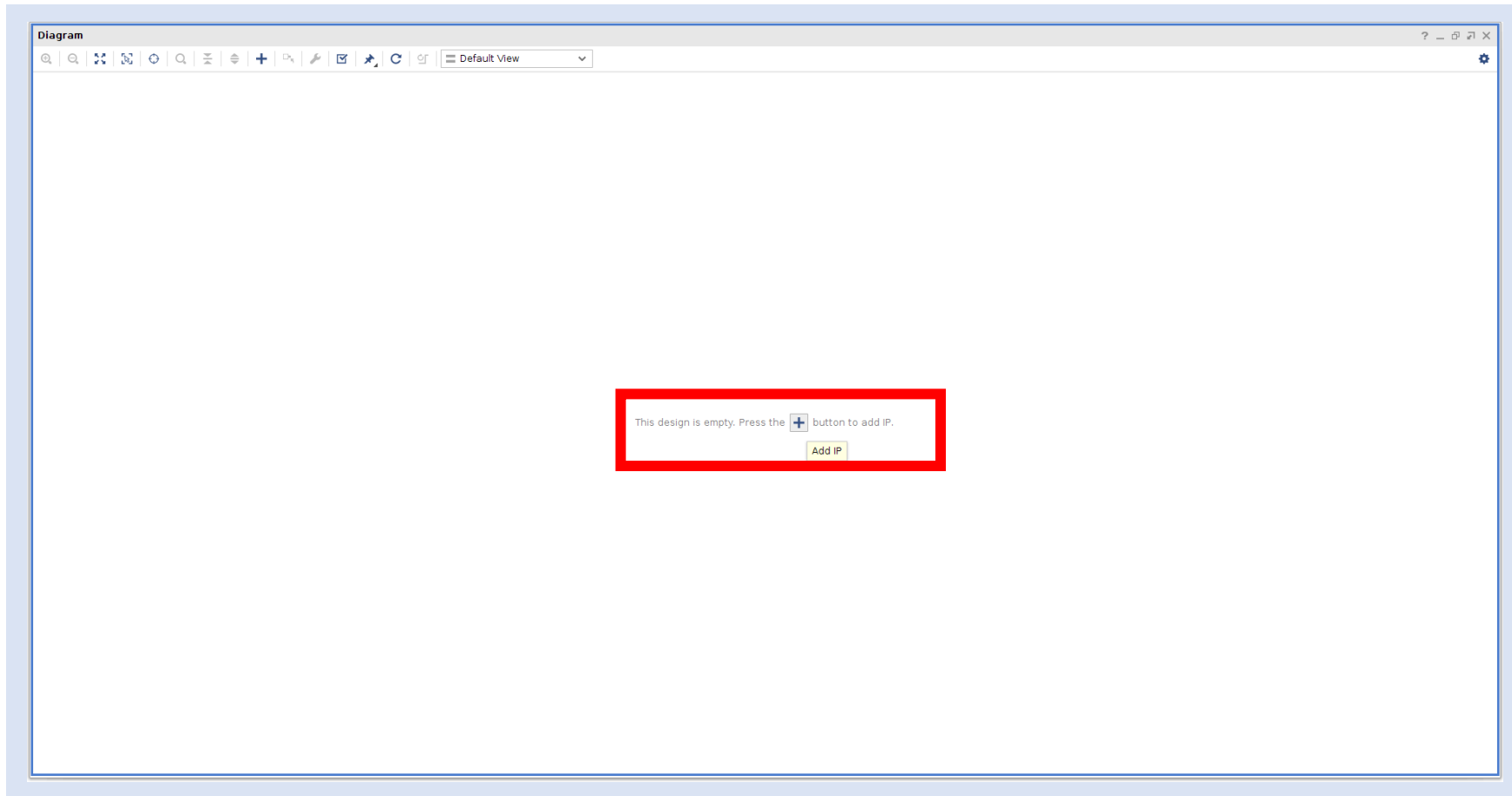
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Step 4 – Undock the block diagram window and maximize it.



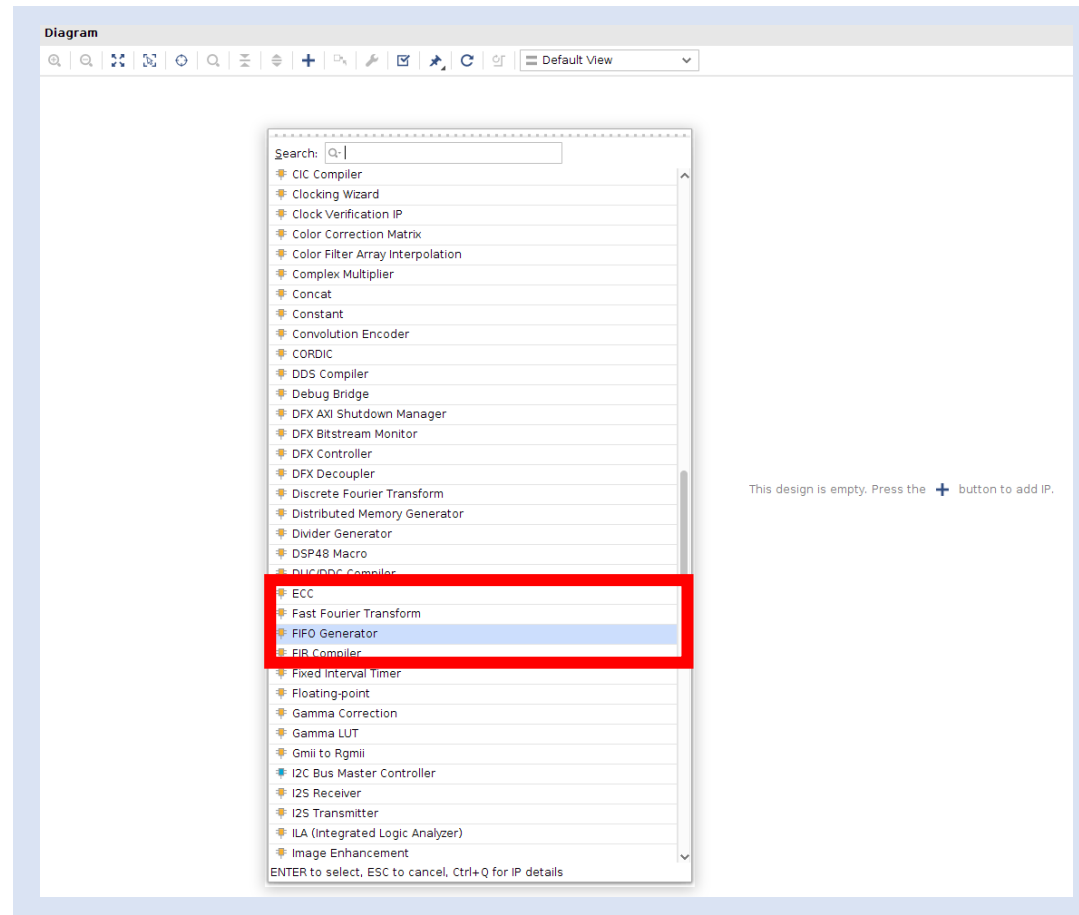
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Step 5 – We are going to add in new IP. Click on the **+** button.



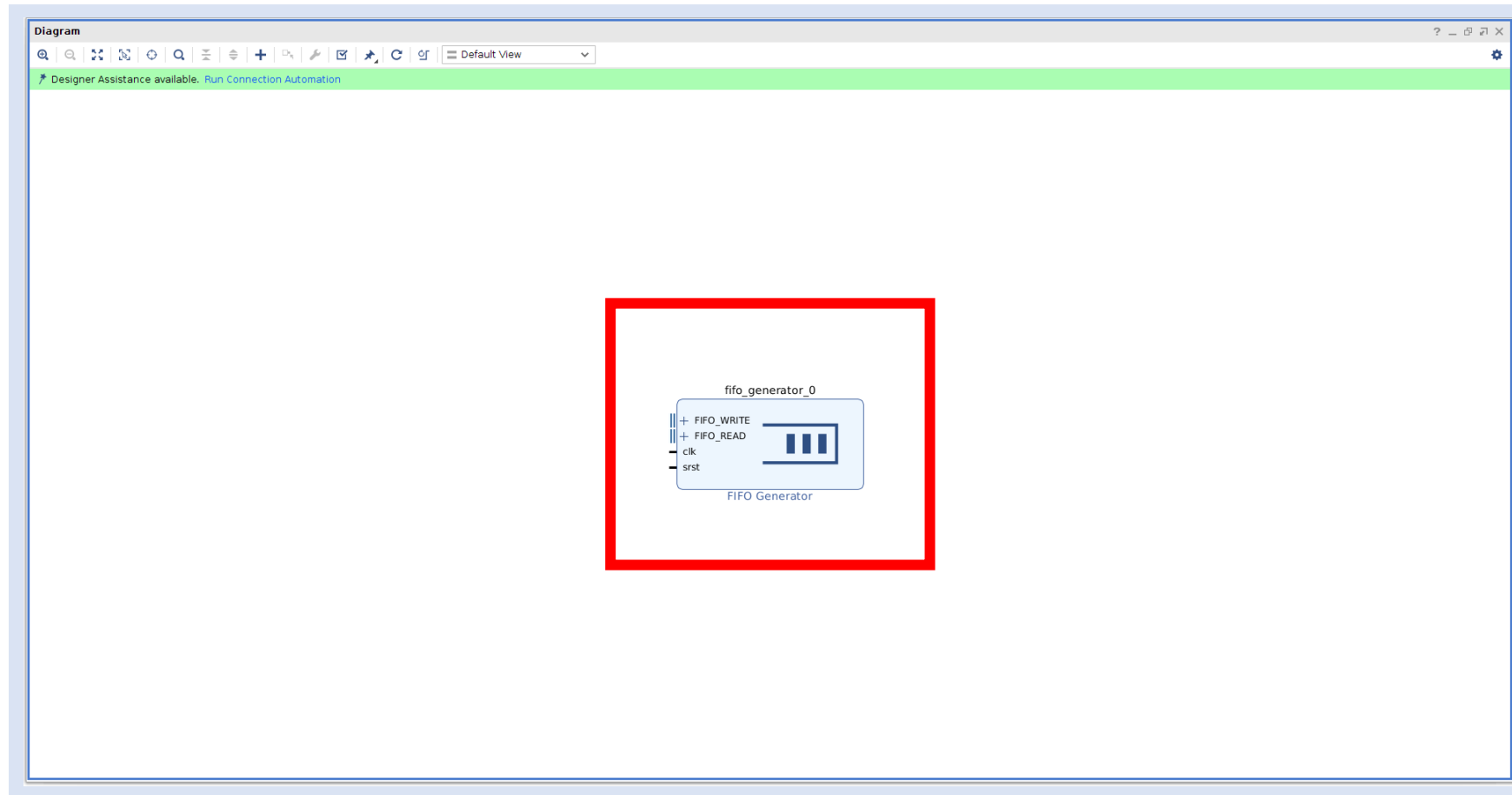
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Step 6 – Select the FIFO Generator. This will add a FIFO to the block diagram.



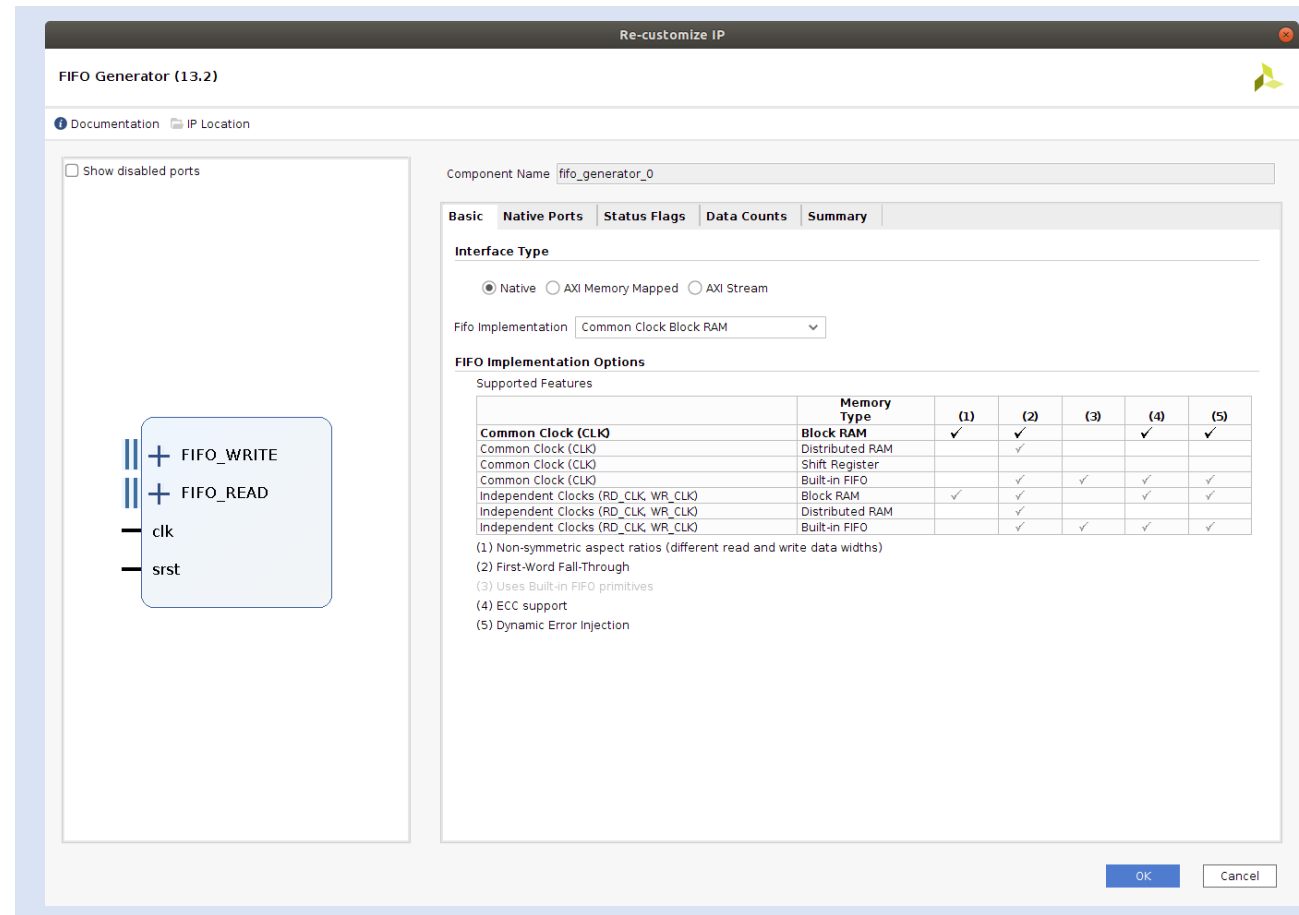
Lab 2: Intermediate Vivado

Step 7 – Double click on the **FIFO Generator** to customize it.



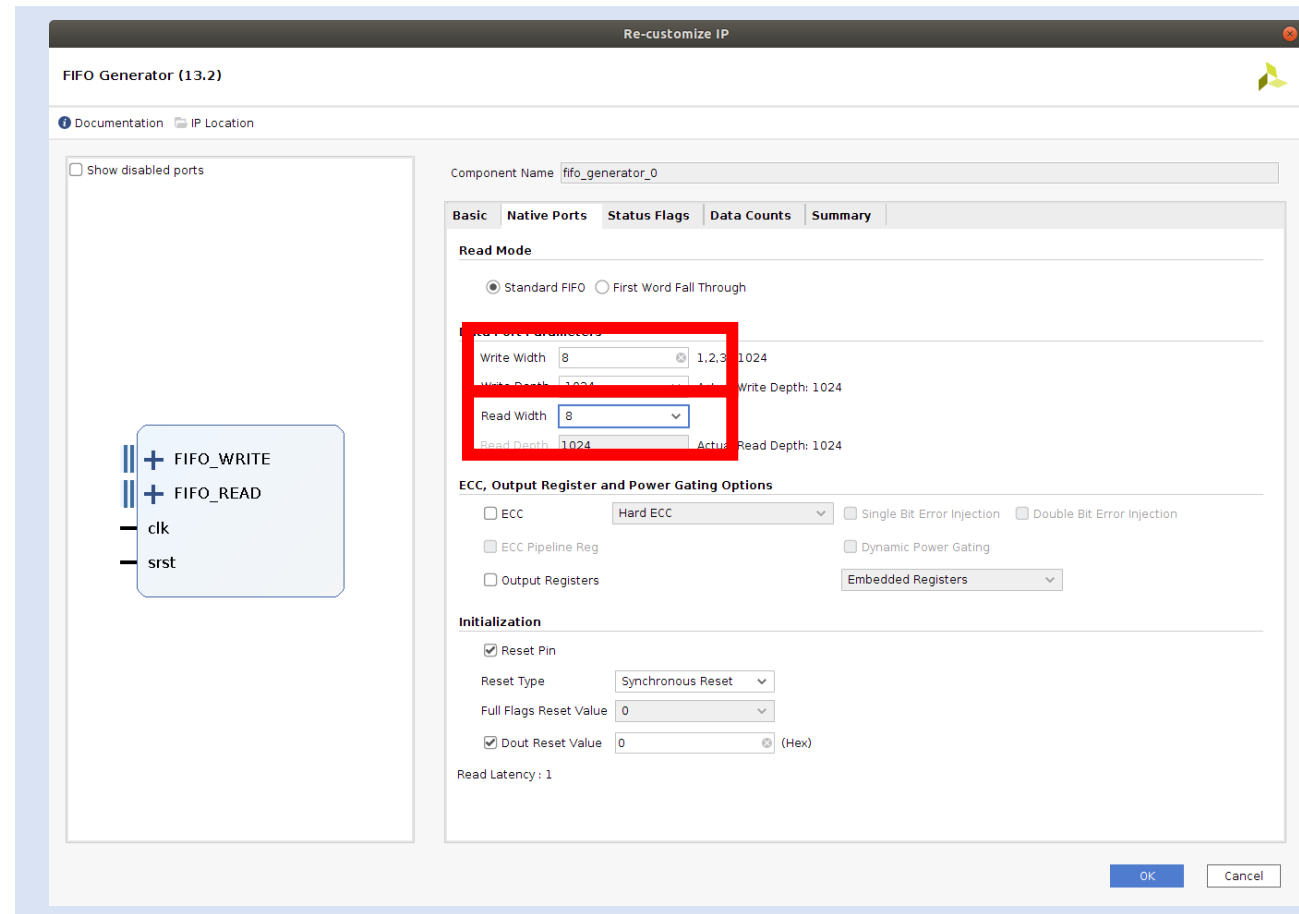
Lab 2: Intermediate Vivado

Step 8 – Leave the first page unchanged.



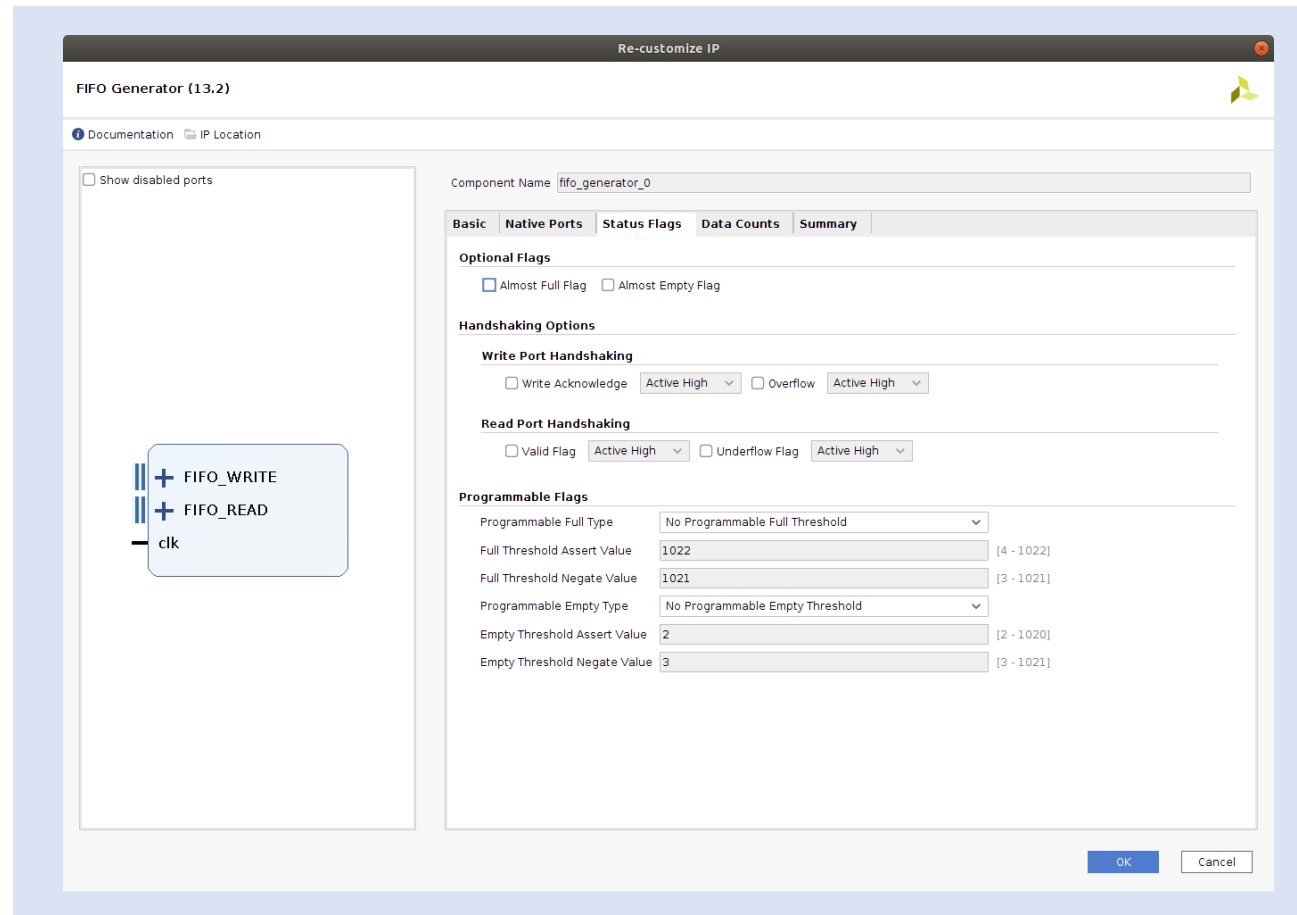
Lab 2: Intermediate Vivado

Step 9 – Change the Write and Read Width to be **8 bits**.



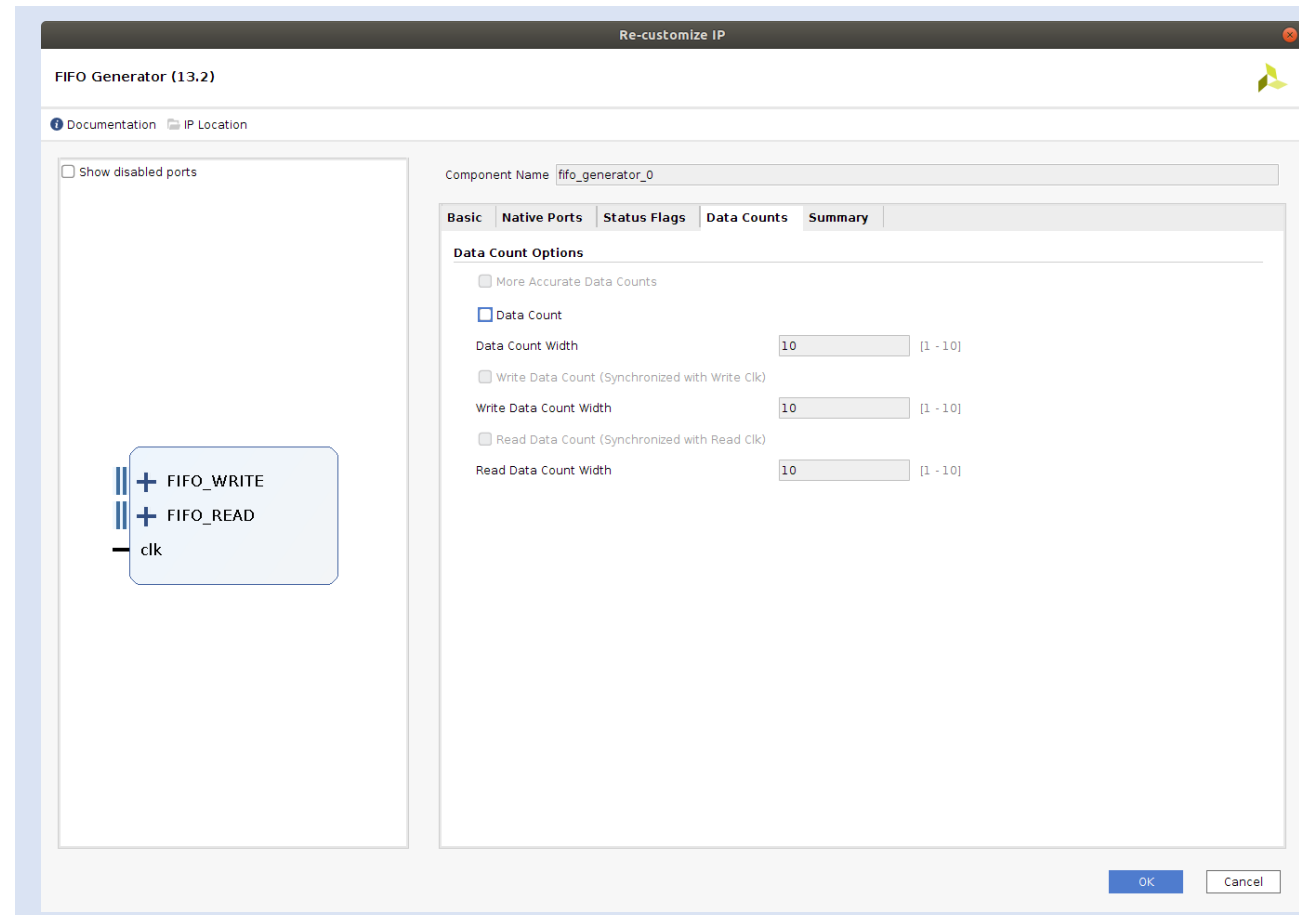
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Step 10 – Leave the third page unchanged.



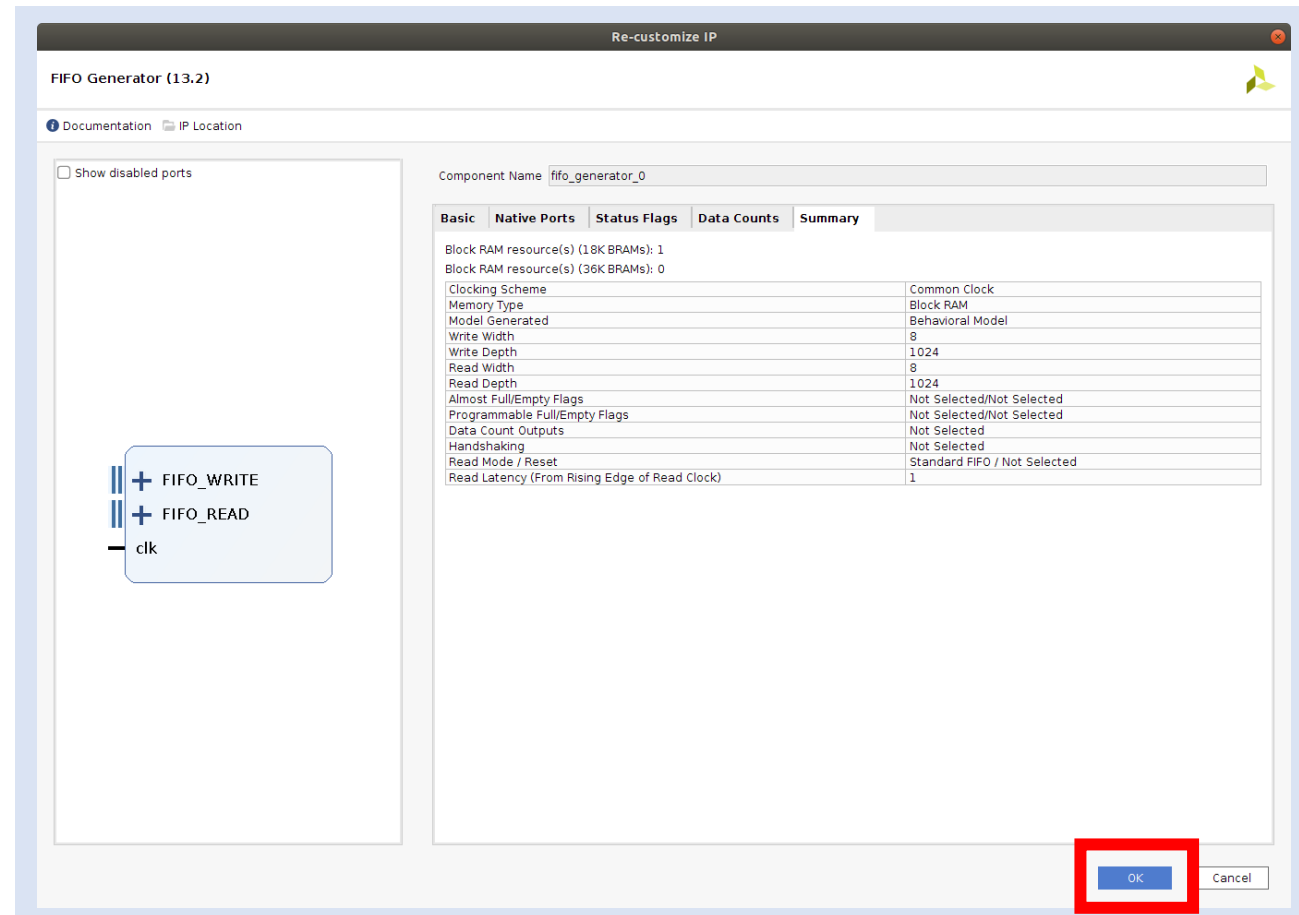
Lab 2: Intermediate Vivado

Step 11 – Leave the fourth page unchanged.



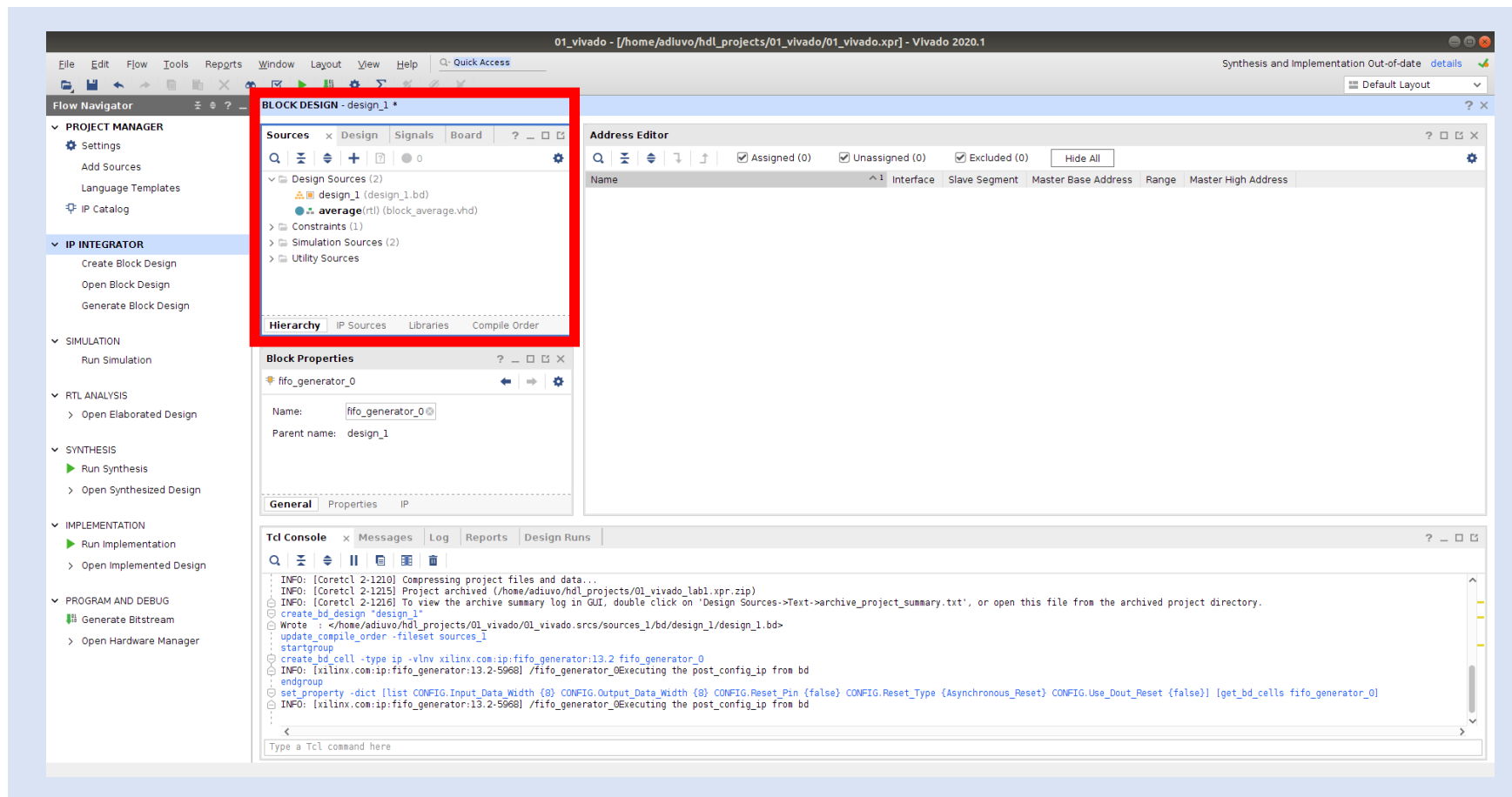
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Step 12 – Leave the final page unchanged. Note that the FIFO OP are unregistered. Click **OK**.



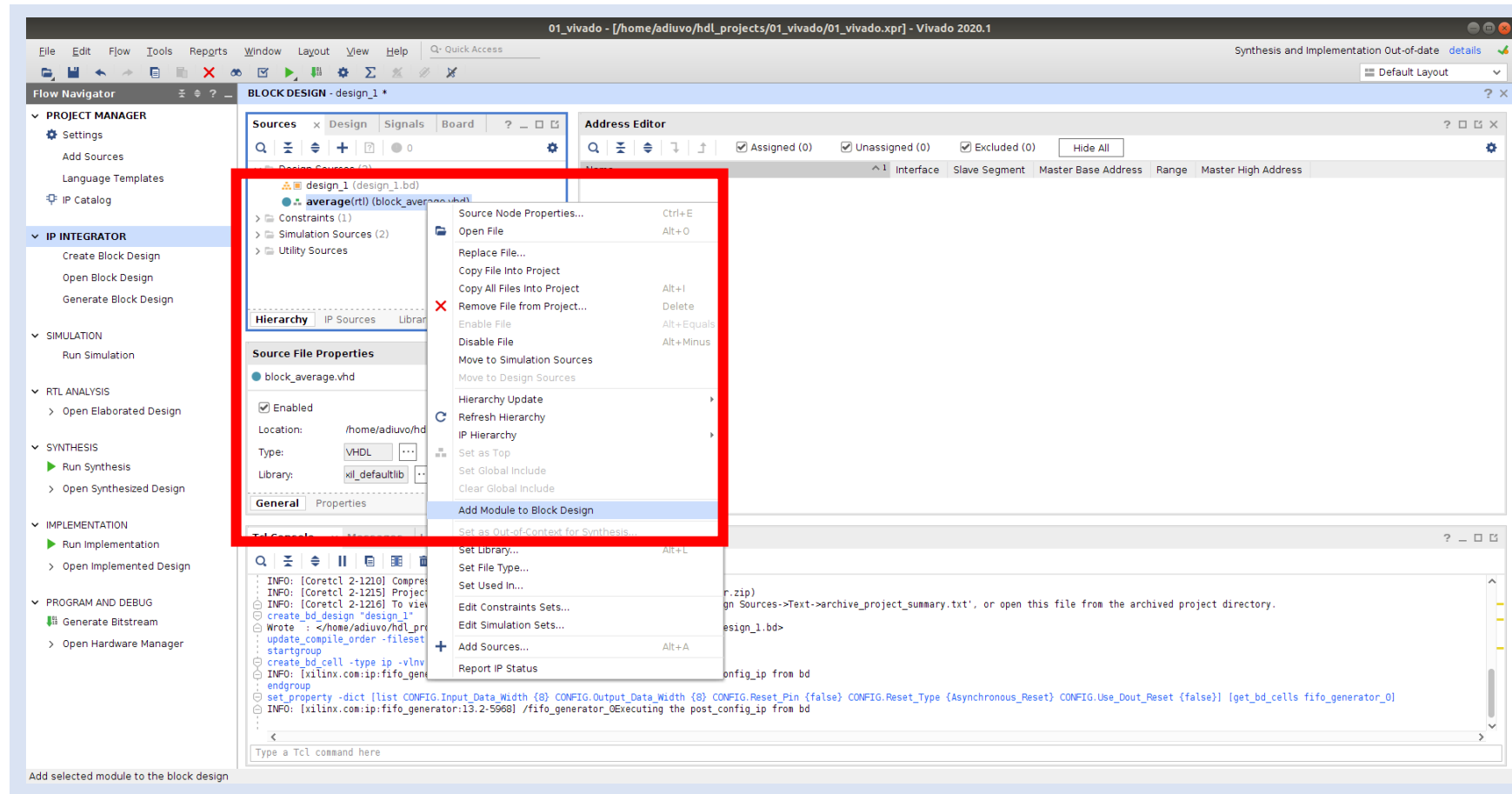
Lab 2: Intermediate Vivado

Step 13 – Click back on the Vivado Project Management view you will see the block diagram under the design sources.



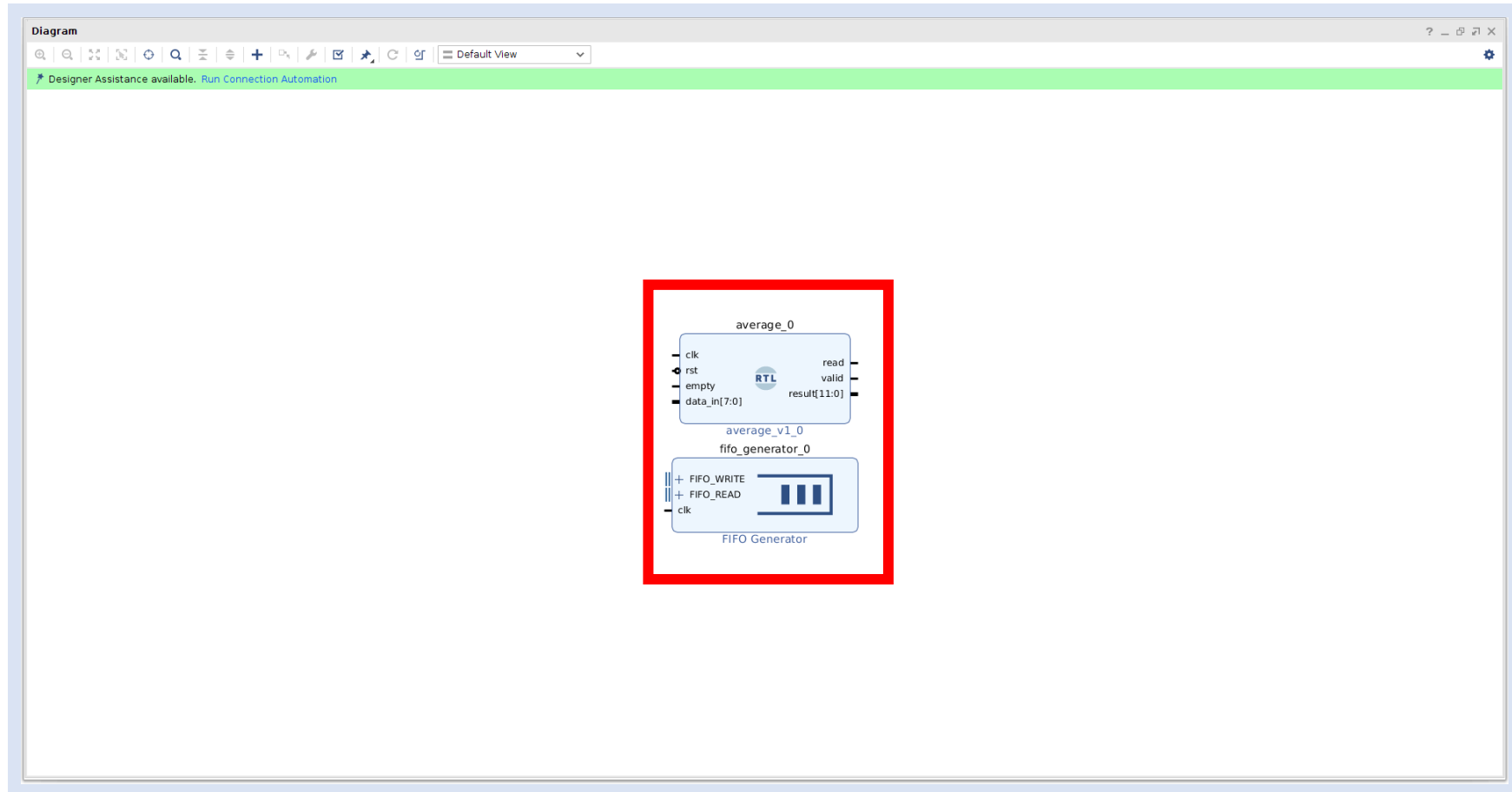
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Step 14 – Right click on the average RTL block and select **Add Module to Block Design.**



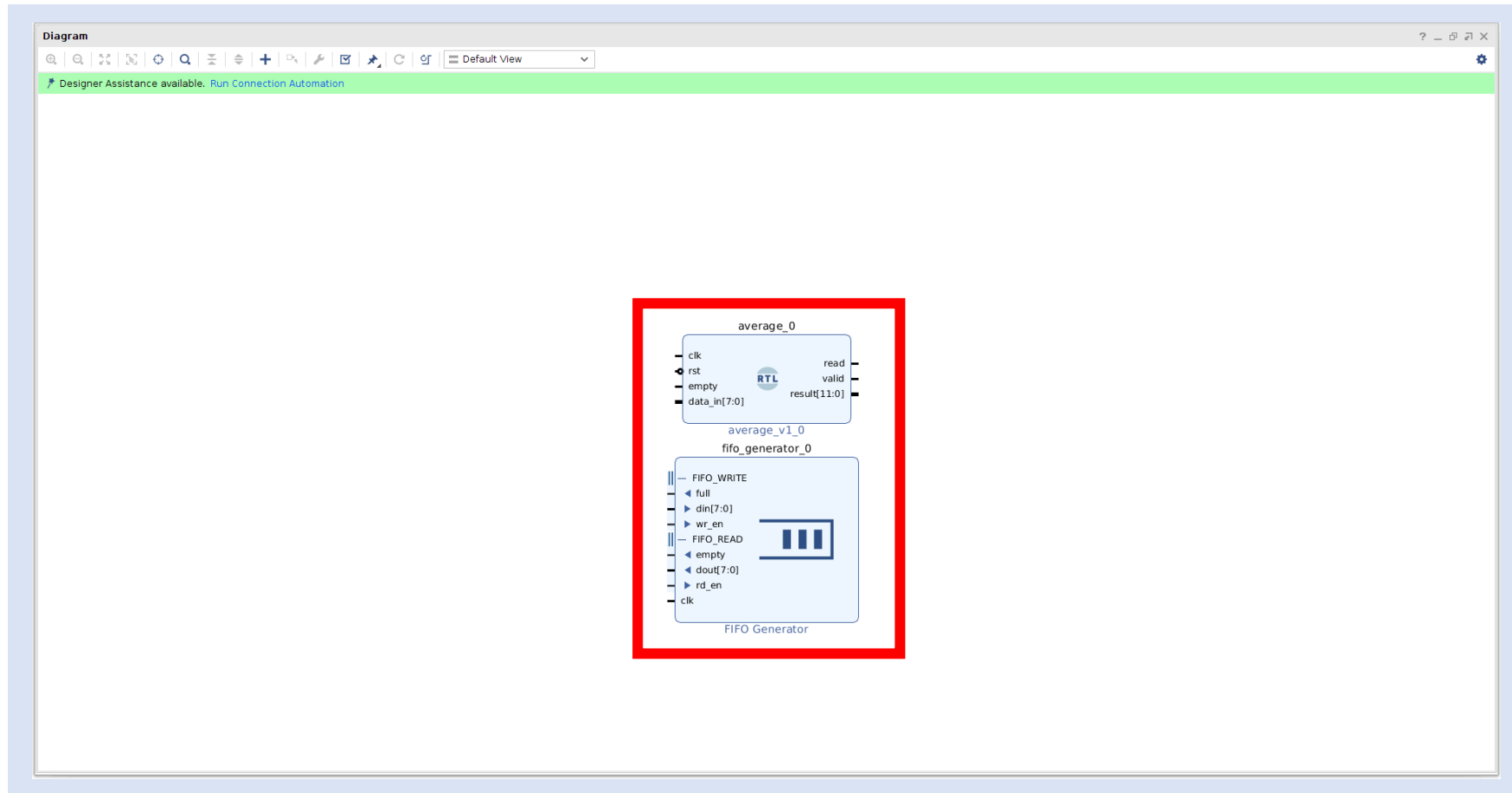
Lab 2: Intermediate Vivado

Step 15 – This will add the average block to the block diagram.



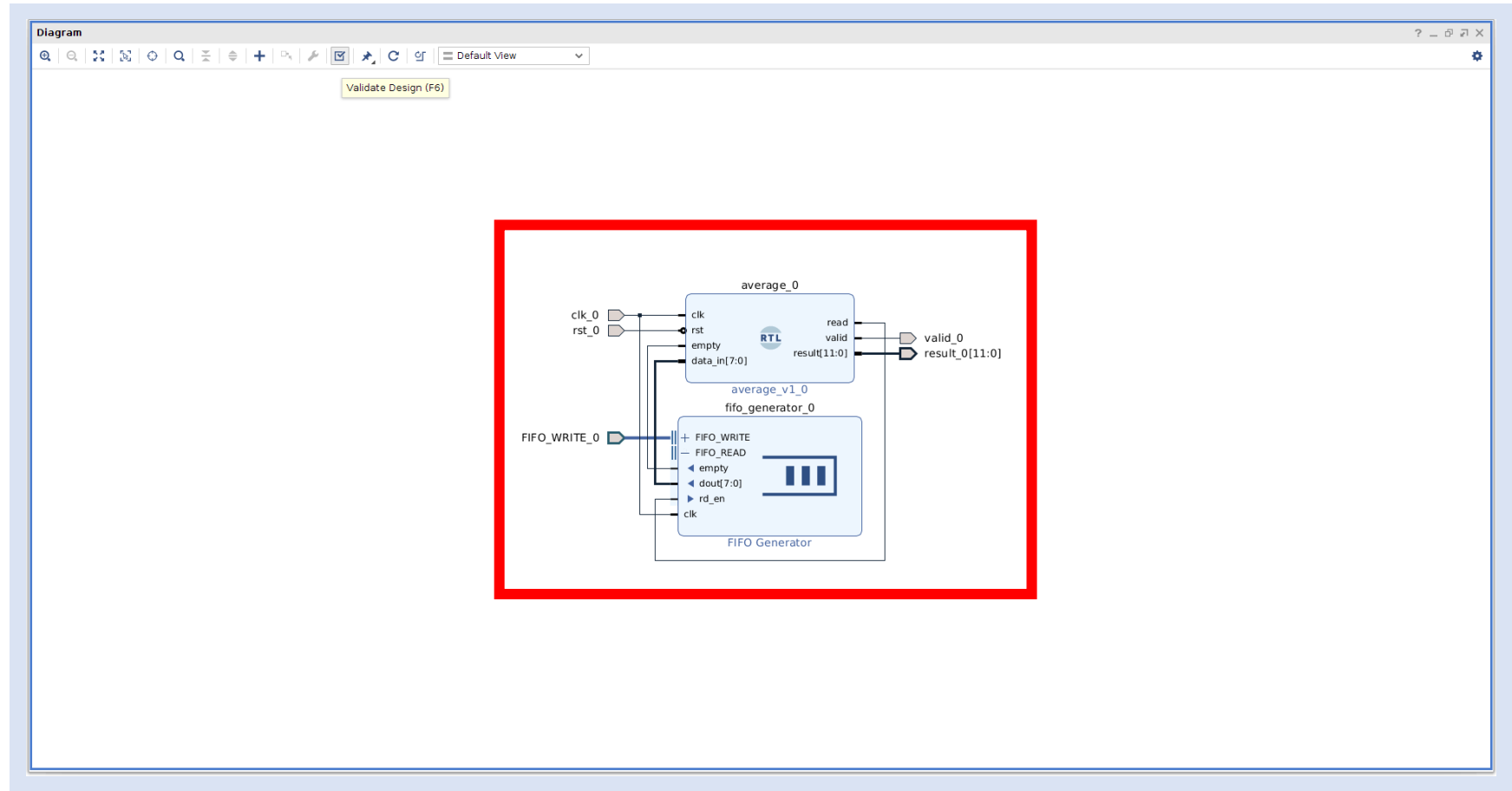
Lab 2: Intermediate Vivado

Step 16 – Expand the FIFO Write and Read Interfaces.



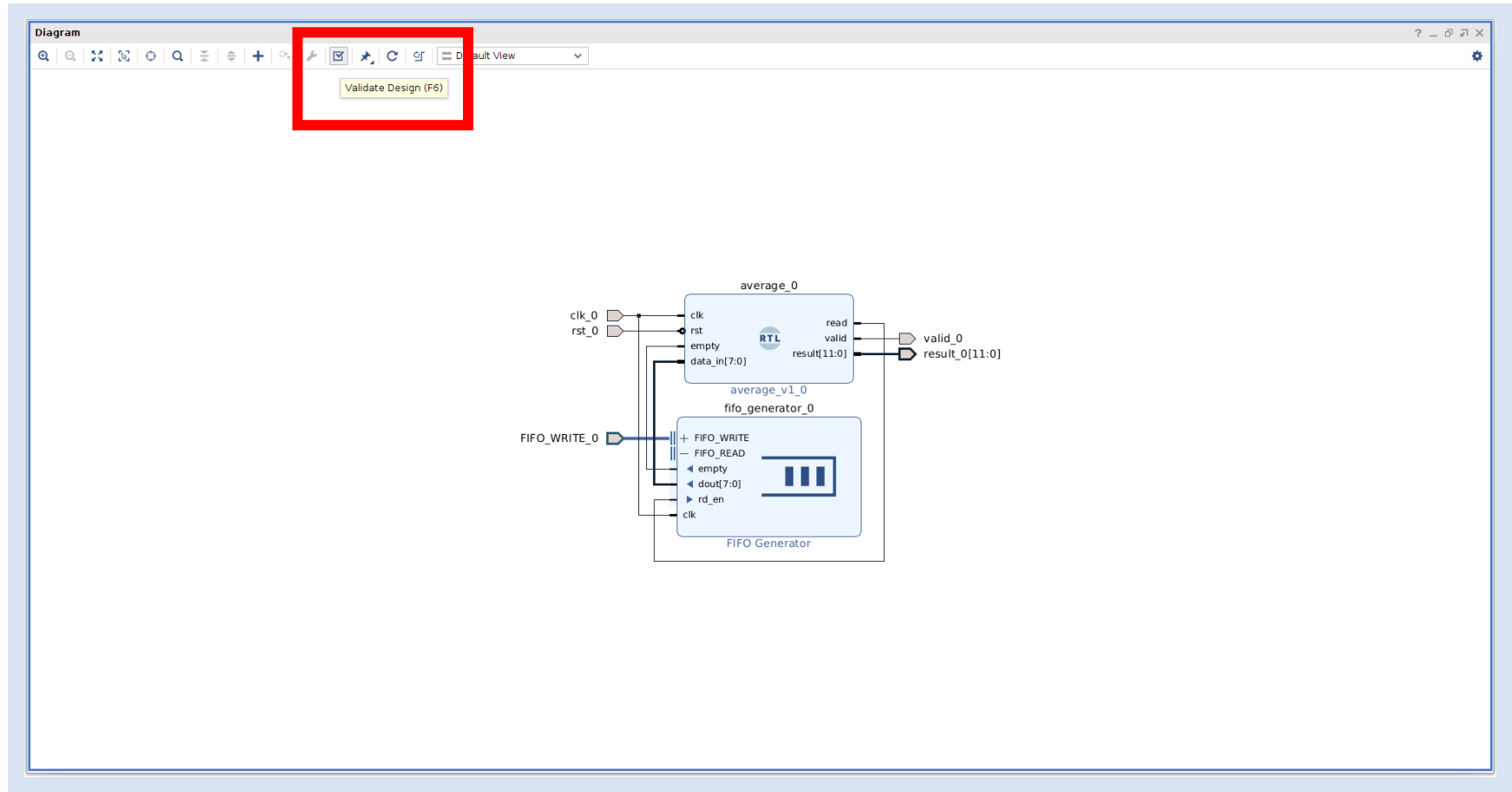
Lab 2: Intermediate Vivado

Step 17 – Make the Clk, Reset, Result, Valid and FIFO Write interfaces external by right-clicking on each pin and selecting **Make External**. Connect the remaining interfaces as below.



Lab 2: Intermediate Vivado

Step 18 – Click on **Validate Design.**



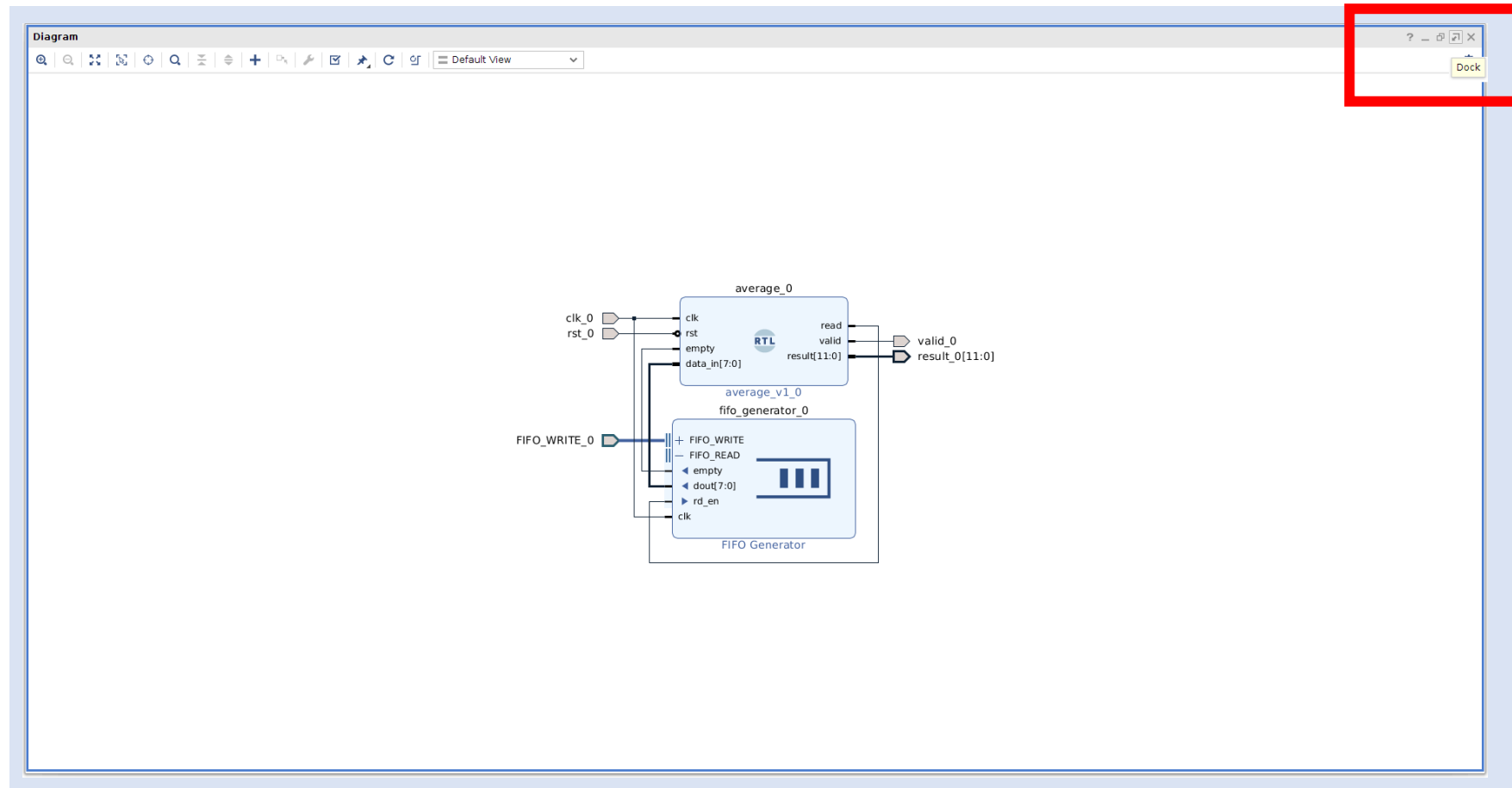
Lab 2: Intermediate Vivado

Step 19 – The validated design should result in no error or critical warnings. Click **OK**.



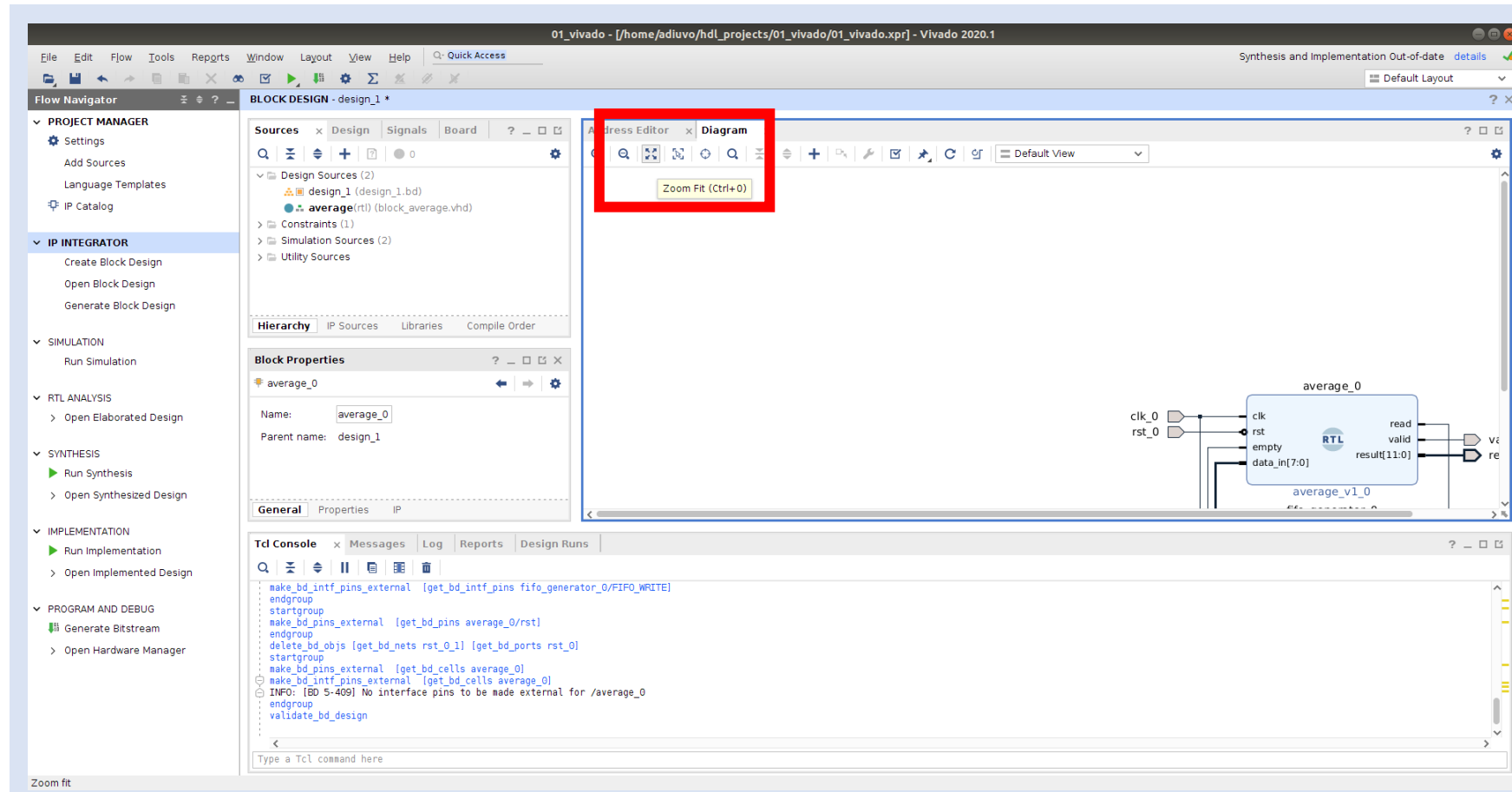
Lab 2: Intermediate Vivado

Step 20 – Re-dock the block diagram window into the Vivado Project Manager.



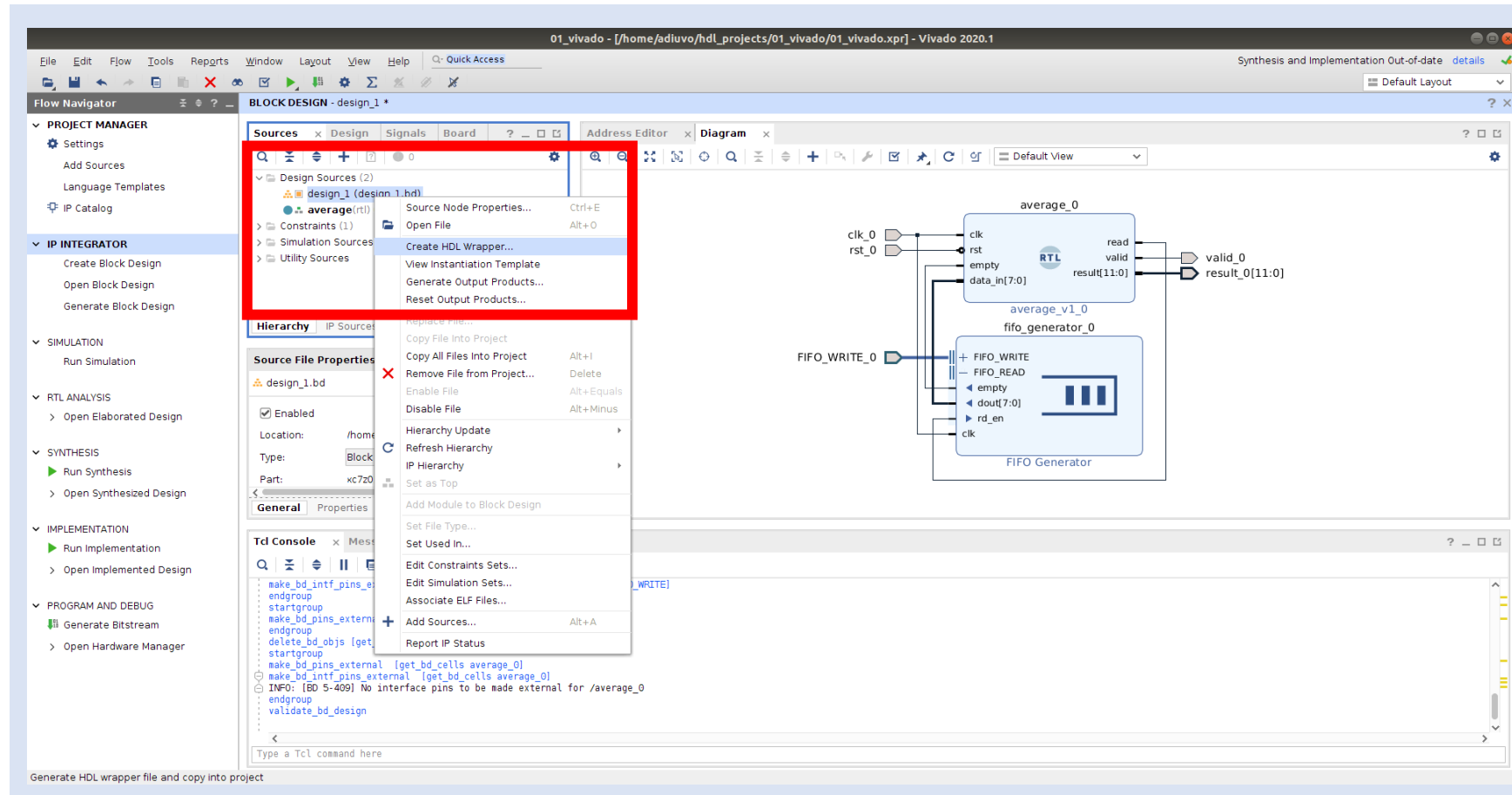
Lab 2: Intermediate Vivado

Step 21 – Click on the **Zoom Fit** button to fit the design to the window.



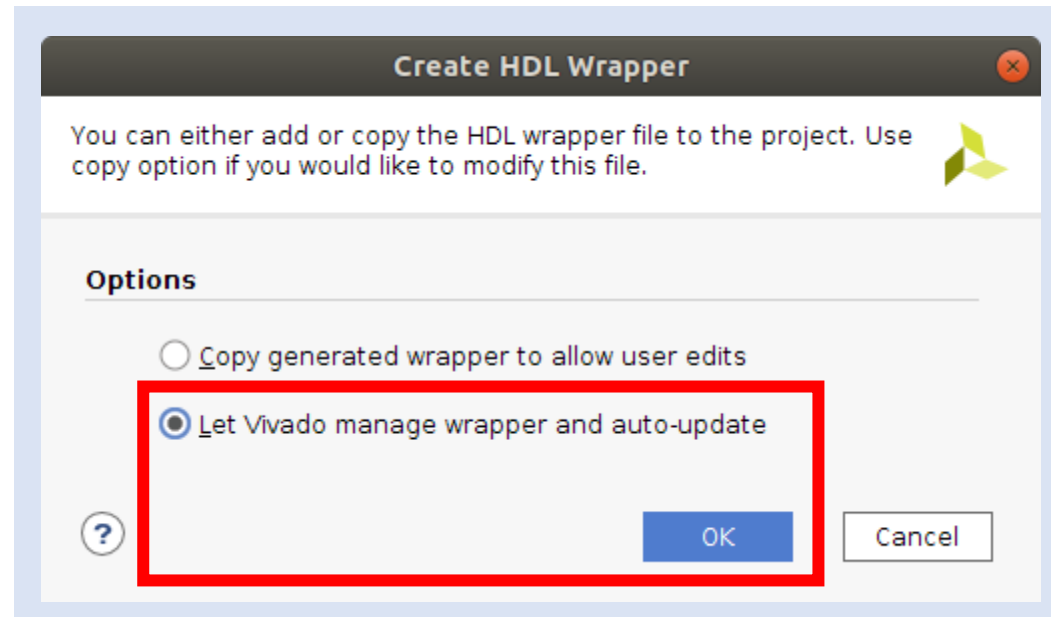
Lab 2: Intermediate Vivado

Step 22 – Right click on the block diagram design under the Design Sources tab and select **Create HDL Wrapper.**



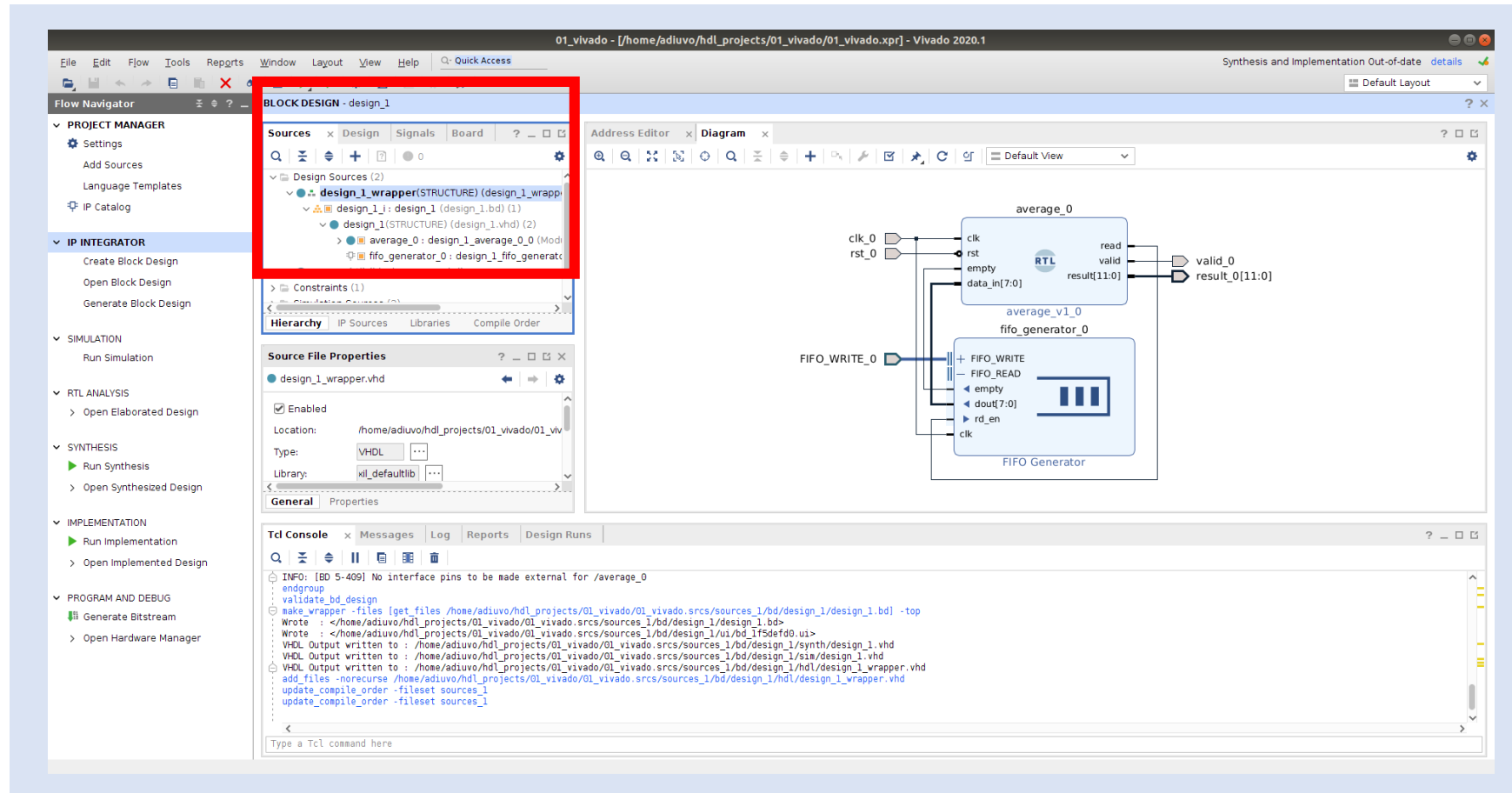
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Step 23 – Allow Vivado to manage the wrapper and click **OK**.



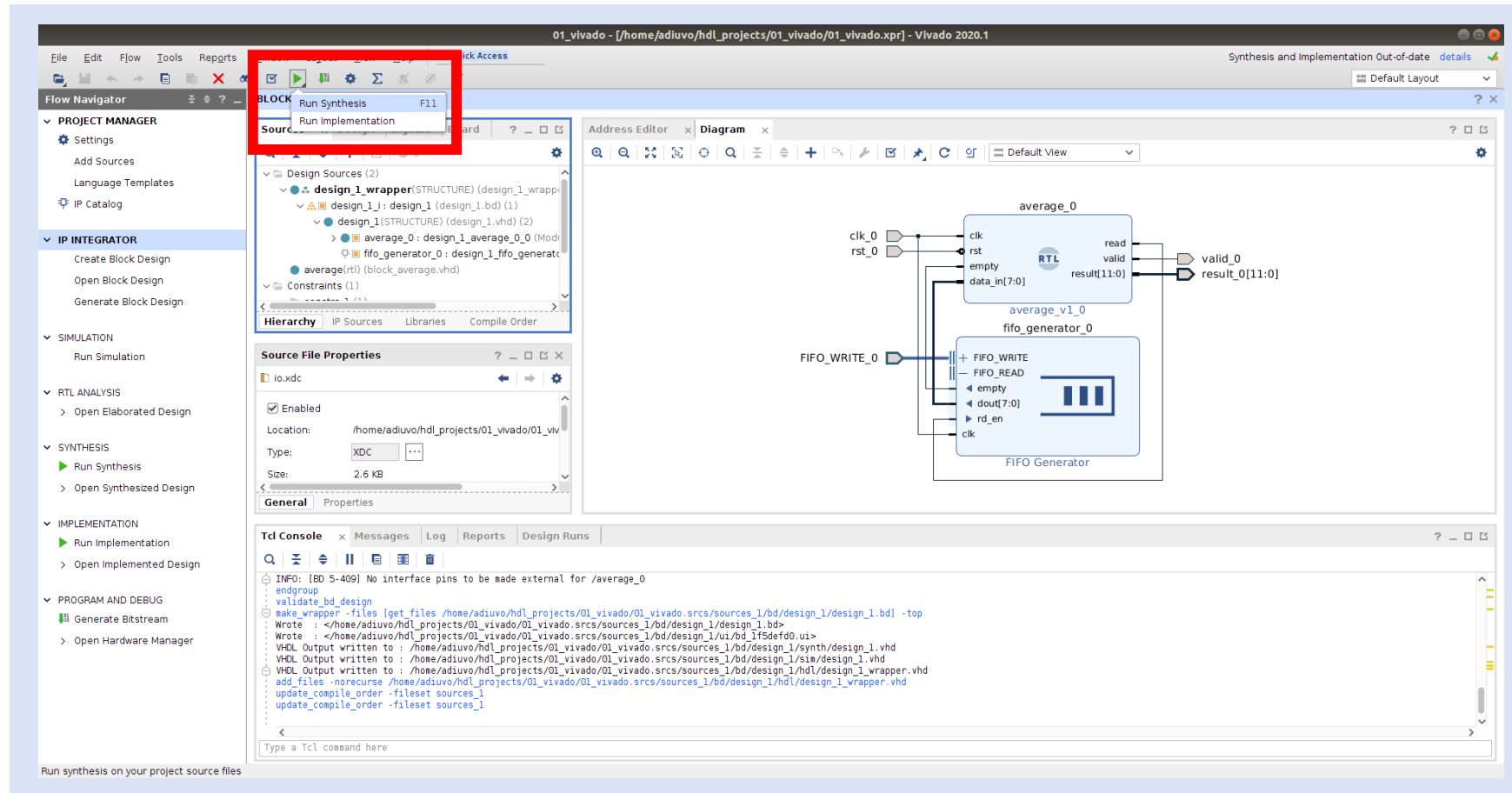
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Step 24 – Expand the newly created wrapper and you will see the entire design.



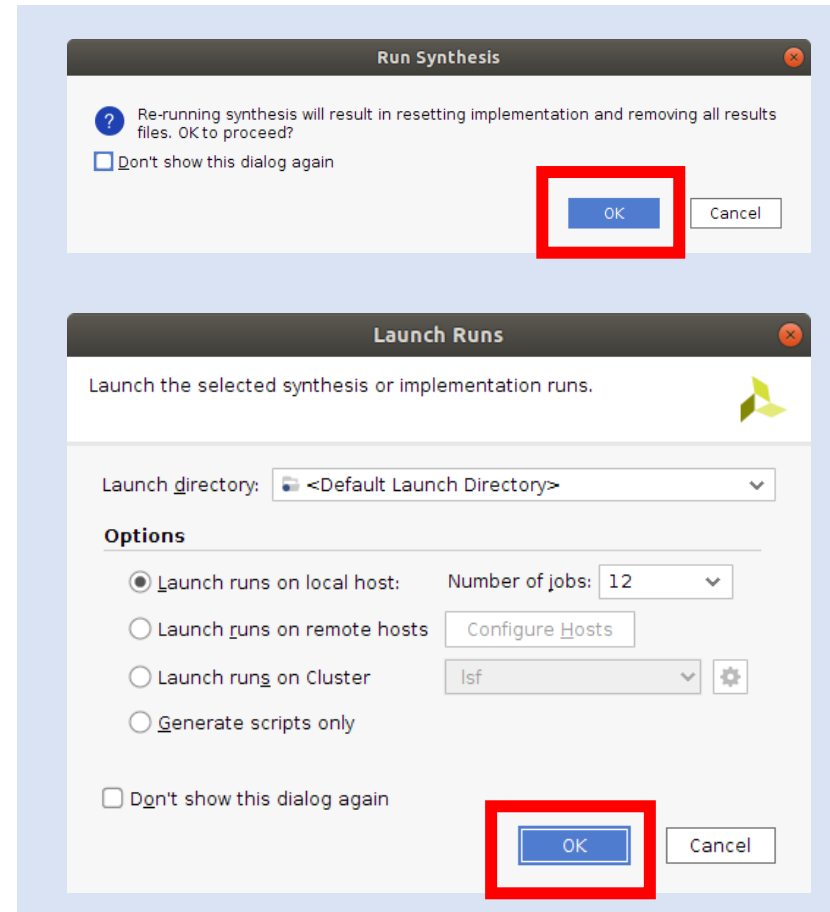
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Step 25 – Run the Synthesis.



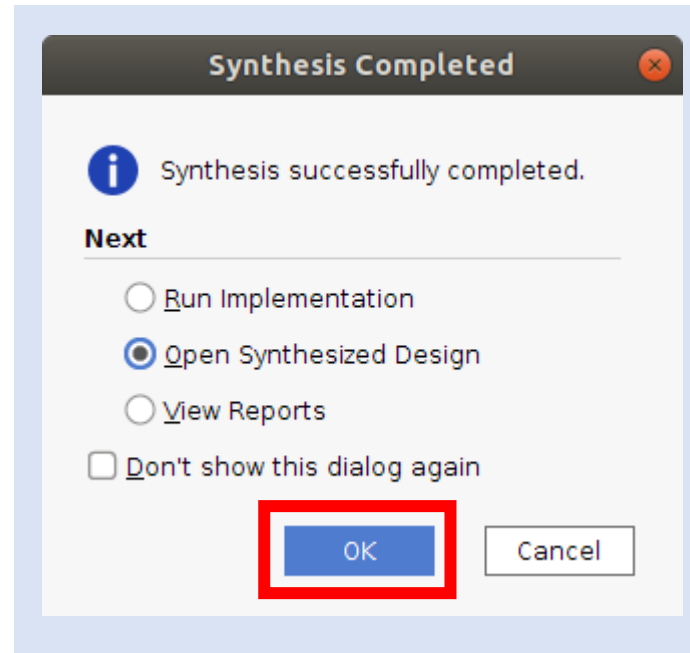
Lab 2: Intermediate Vivado

Step 26 – On both resultant dialogs click **OK** and wait for synthesis to complete.



Lab 2: Intermediate Vivado

Step 27 – When synthesis completes, **Open the Synthesized Design.**



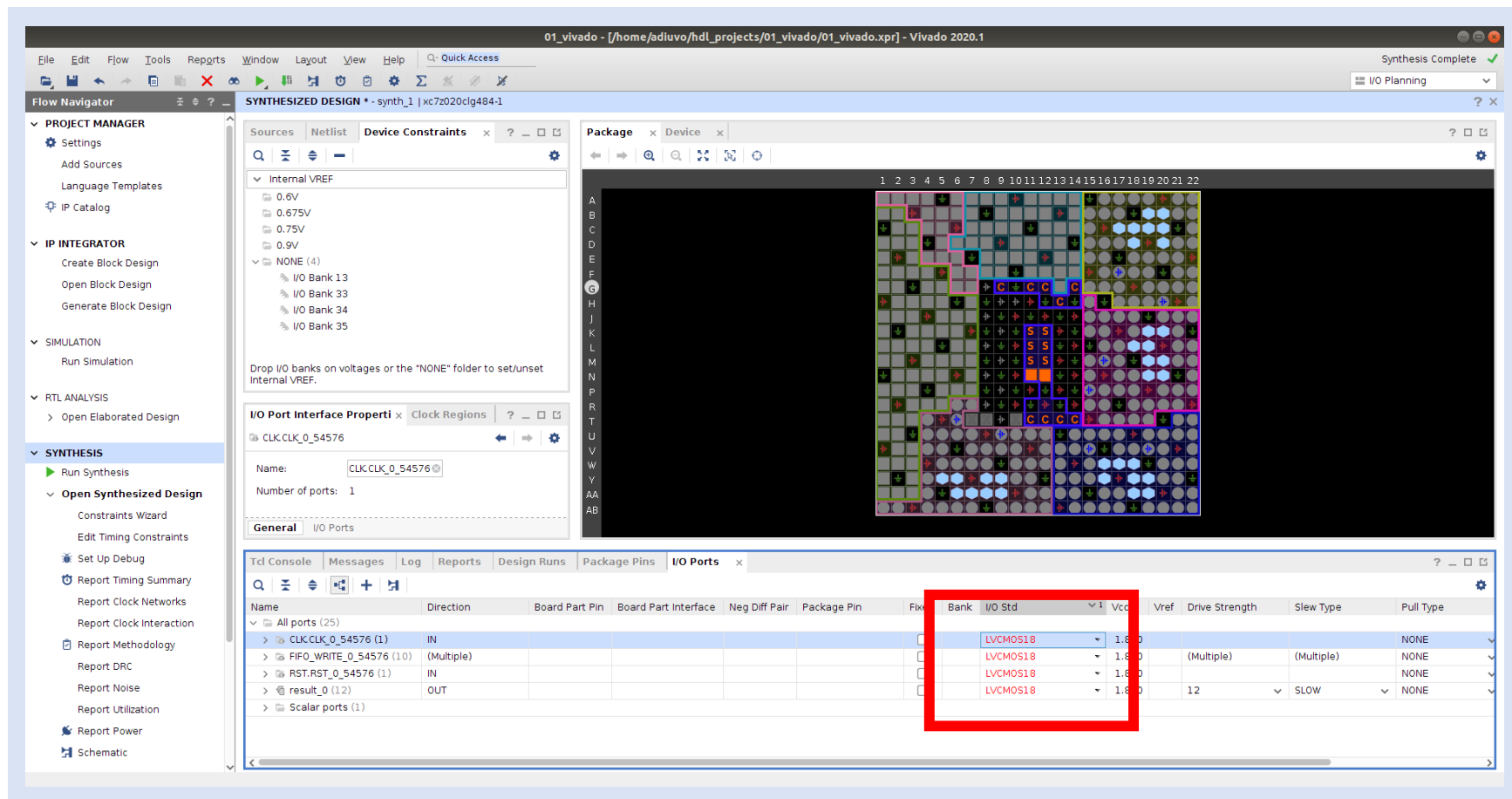
Lab 2: Intermediate Vivado

Step 28 – If any critical warnings pop up, select **OK**. This is due to out of data constraints which we are about to address.



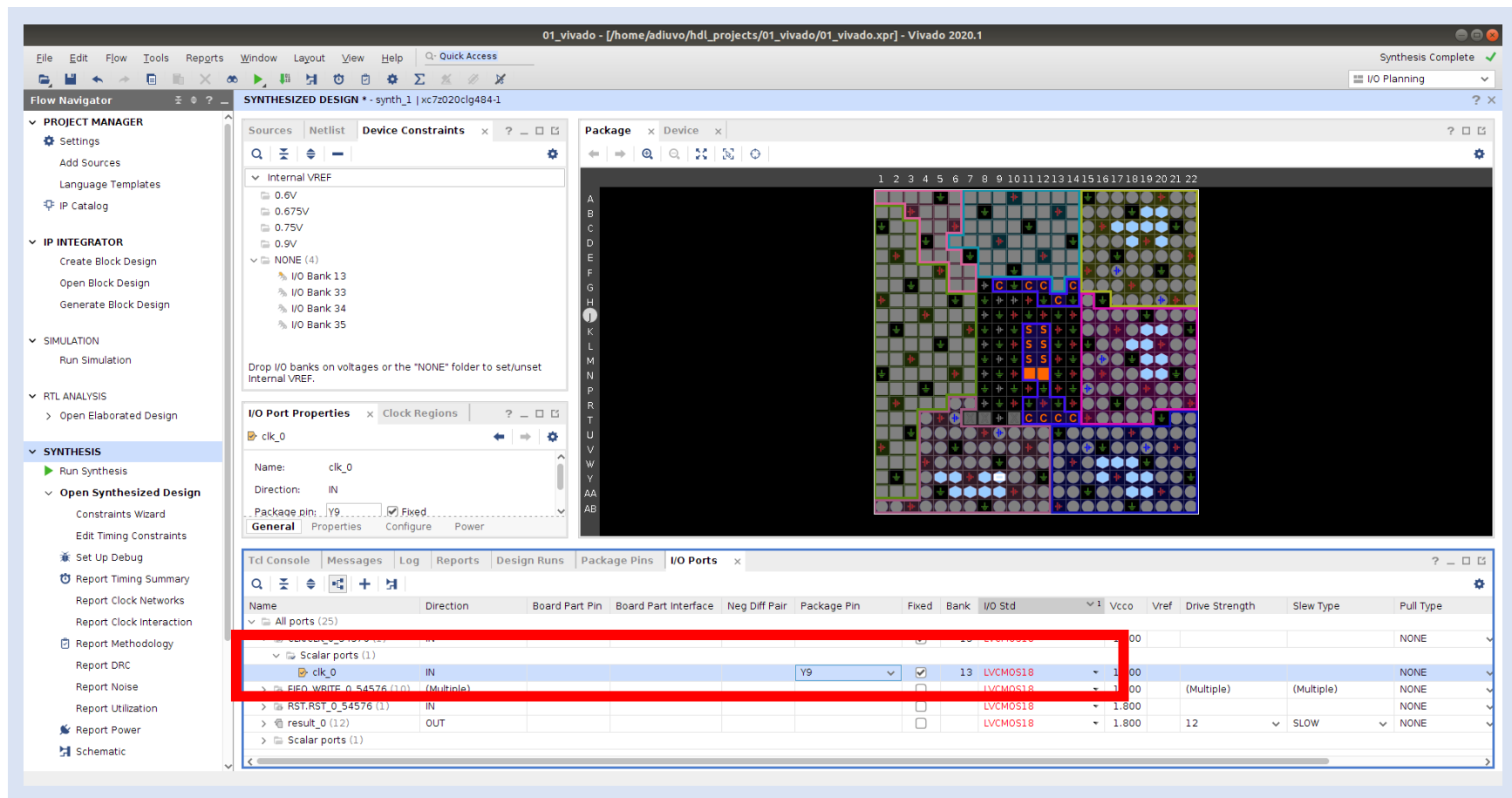
Lab 2: Intermediate Vivado

Step 29 – Change the I/O standard from default to **LVC MOS18**.



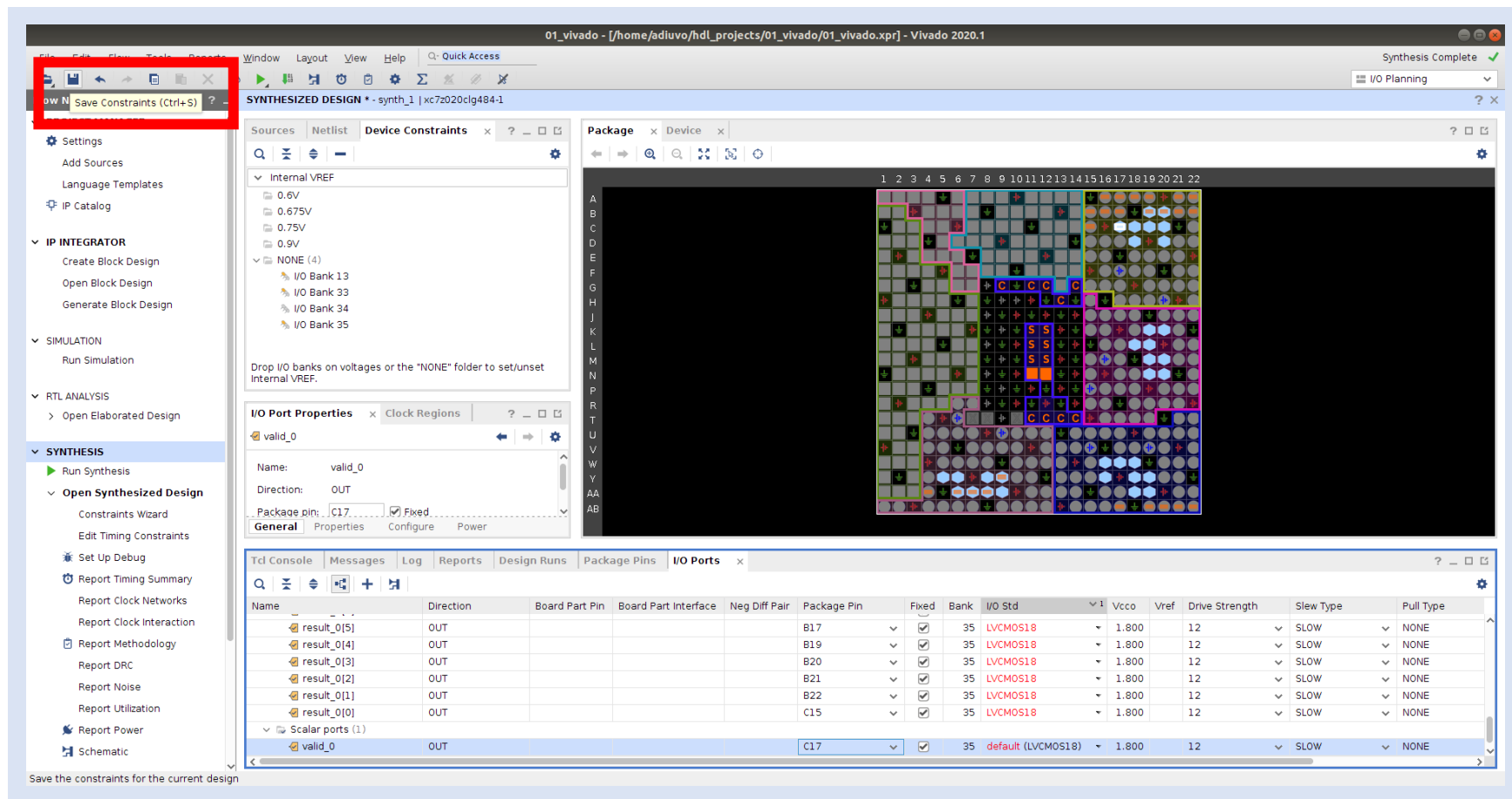
Lab 2: Intermediate Vivado

Step 30 – Assign the clock input to pin **Y9**. Assign all other IO to pins of your choice.



Lab 2: Intermediate Vivado

Step 31 – Click on **Save Constraints**.



Lab 2: Intermediate Vivado

Step 32 – If an out-of-date warning appears, click **OK**.



Lab 2: Intermediate Vivado

Step 33 – From the sources tab, open the **IO constraints**. You will see the old pin out for the previous project and your new project. This is because we have evolved the original project.

The screenshot displays the Vivado IDE interface for a project named '01_vivado'. The left-hand 'Flow Navigator' pane shows the project hierarchy, with the 'SYNTHESIS' tab selected and 'Open Synthesized Design' chosen. The central 'Sources' pane shows the project's source files, including 'design_1_wrapper', 'design_1', 'design_1_vhd', 'average_0', 'fifo_generator_0', 'average', and 'io.xdc'. The 'io.xdc' file is selected, and its content is displayed in the right-hand pane. The content of 'io.xdc' is as follows:

```

1 set_property PACKAGE_PIN A16 [get_ports {data_in[7]}]
2 set_property PACKAGE_PIN A17 [get_ports {data_in[6]}]
3 set_property PACKAGE_PIN A18 [get_ports {data_in[5]}]
4 set_property PACKAGE_PIN A19 [get_ports {data_in[4]}]
5 set_property PACKAGE_PIN A21 [get_ports {data_in[3]}]
6 set_property PACKAGE_PIN A22 [get_ports {data_in[2]}]
7 set_property PACKAGE_PIN AB1 [get_ports {data_in[1]}]
8 set_property PACKAGE_PIN AB2 [get_ports {data_in[0]}]
9 set_property PACKAGE_PIN AB4 [get_ports {result[11]}]
10 set_property PACKAGE_PIN AB5 [get_ports {result[0]}]
11 set_property PACKAGE_PIN AB6 [get_ports {result[1]}]
12 set_property PACKAGE_PIN AB7 [get_ports {result[2]}]
13 set_property PACKAGE_PIN AB9 [get_ports {result[3]}]
14 set_property PACKAGE_PIN AB10 [get_ports {result[4]}]
15 set_property PACKAGE_PIN AB11 [get_ports {result[5]}]
16 set_property PACKAGE_PIN AB12 [get_ports {result[6]}]
17 set_property PACKAGE_PIN AB14 [get_ports {result[7]}]
18 set_property PACKAGE_PIN AB15 [get_ports {result[8]}]
19 set_property PACKAGE_PIN AB16 [get_ports {result[9]}]
20 set_property PACKAGE_PIN AB17 [get_ports {result[10]}]
21 set_property PACKAGE_PIN AB20 [get_ports empty]
22 set_property PACKAGE_PIN AB21 [get_ports read]
23 set_property PACKAGE_PIN AB22 [get_ports rst]
24 set_property PACKAGE_PIN B15 [get_ports valid]
25
26 set_property PACKAGE_PIN Y9 [get_ports clk]
27
28 set_property IOSTANDARD LVCMOS18 [get_ports {data_in[7]}]
29 set_property IOSTANDARD LVCMOS18 [get_ports {data_in[6]}]
30

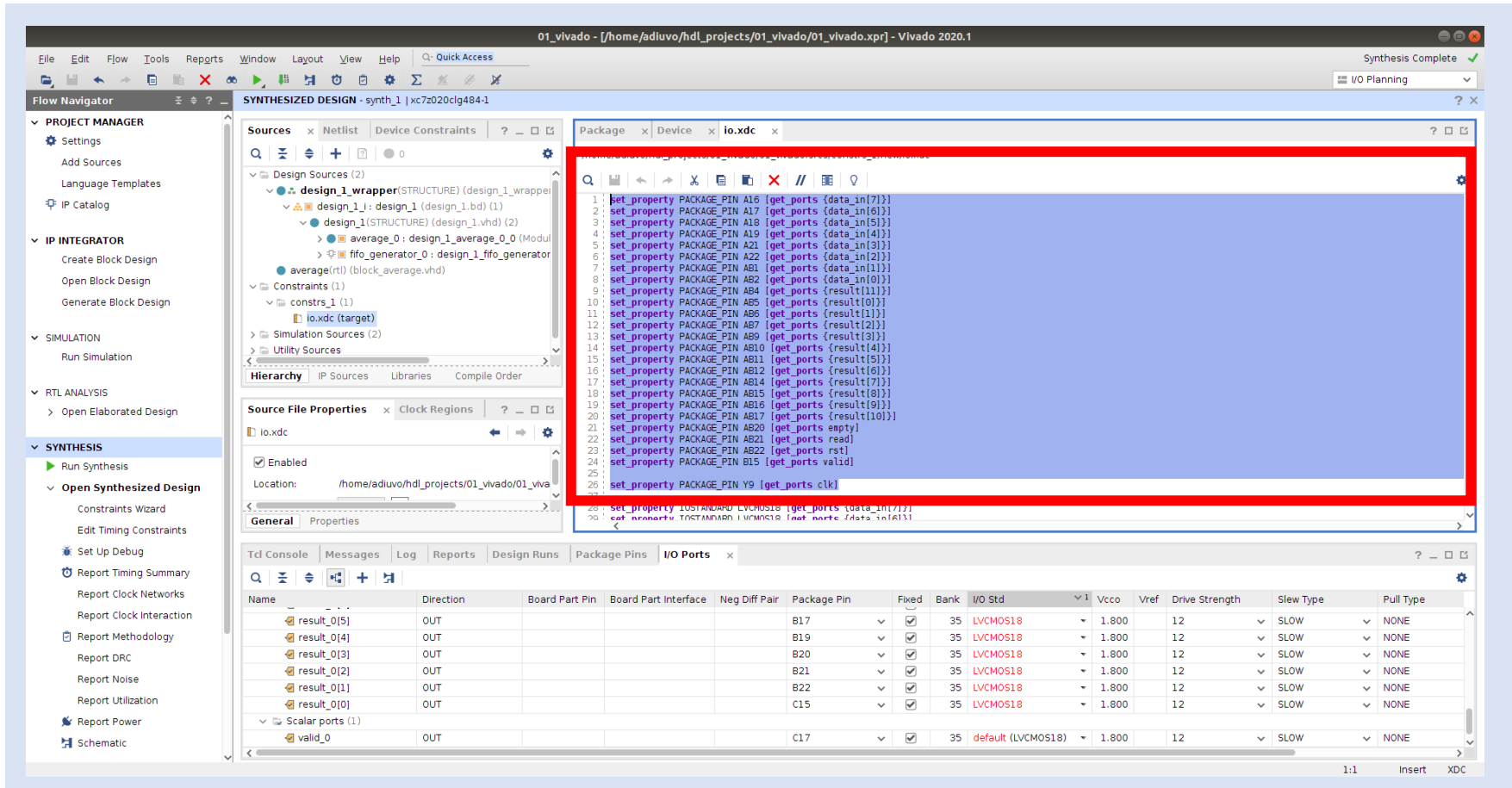
```

The bottom pane shows the 'I/O Ports' table, which lists the package pins and their constraints:

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type
result_0[5]	OUT				B17	✓	35	LVCMOS18	1.800	12	12	SLOW	NONE
result_0[4]	OUT				B19	✓	35	LVCMOS18	1.800	12	12	SLOW	NONE
result_0[3]	OUT				B20	✓	35	LVCMOS18	1.800	12	12	SLOW	NONE
result_0[2]	OUT				B21	✓	35	LVCMOS18	1.800	12	12	SLOW	NONE
result_0[1]	OUT				B22	✓	35	LVCMOS18	1.800	12	12	SLOW	NONE
result_0[0]	OUT				C15	✓	35	LVCMOS18	1.800	12	12	SLOW	NONE
valid_0	OUT				C17	✓	35	default (LVCMOS18)	1.800	12	12	SLOW	NONE

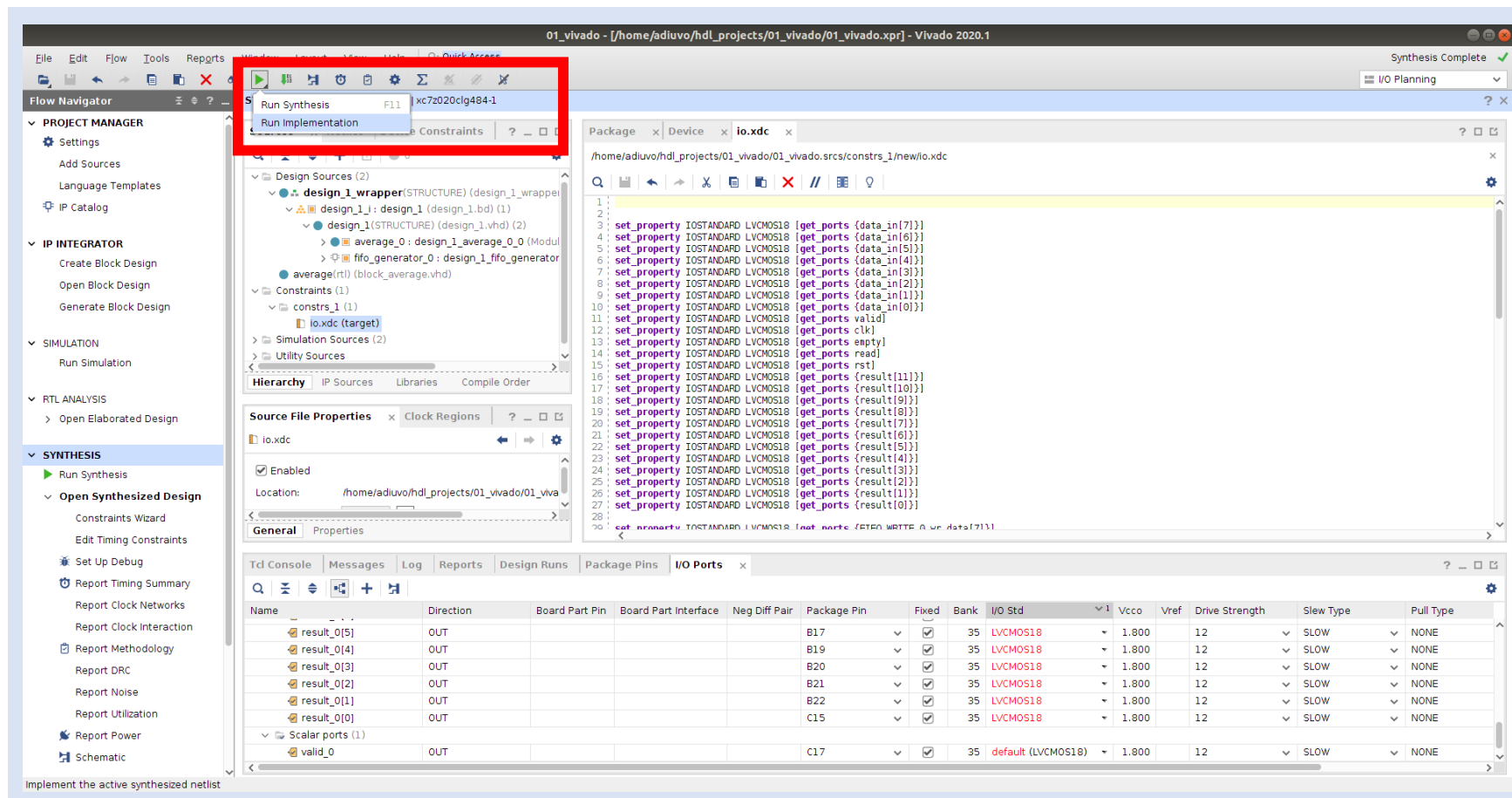
Lab 2: Intermediate Vivado

Step 34 – Select the old constraints (at the top of the file) and delete them. Save the file.



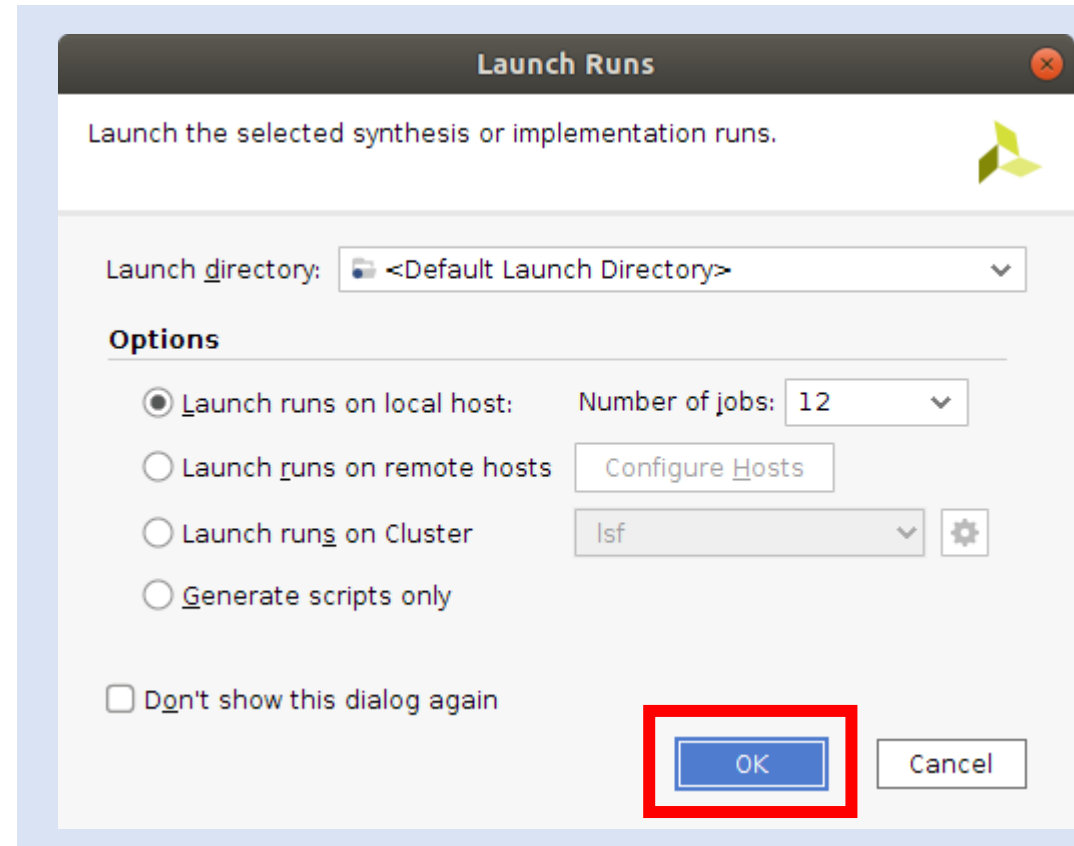
Lab 2: Intermediate Vivado

Step 35 – Run the Implementation.



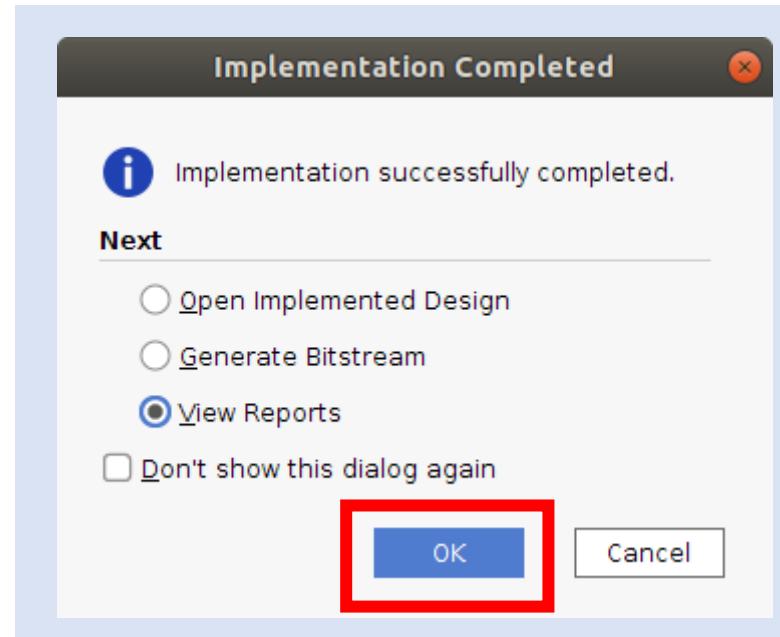
Lab 2: Intermediate Vivado

Step 36 – Click **OK** to run the implementation.



Lab 2: Intermediate Vivado

Step 37 – When the implementation completes, click **View Reports**.



Lab 2: Intermediate Vivado

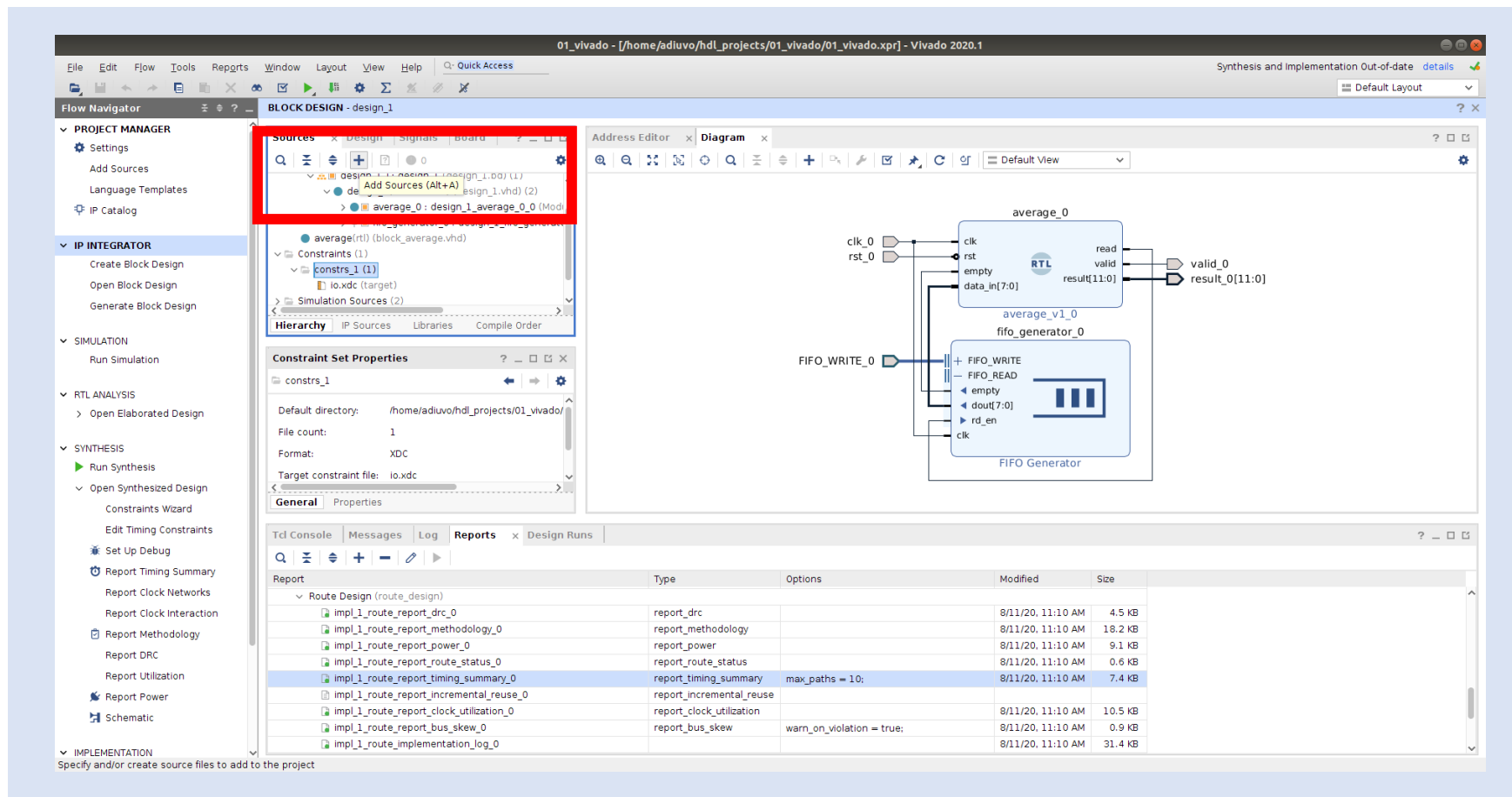
Step 38 – Select Constraints under Design Sources.

The screenshot displays the Vivado 2020.1 IDE interface. The main window is titled '01_vivado - [/home/adiuvo/hdl_projects/01_vivado/01_vivado.xpr] - Vivado 2020.1'. The 'BLOCK DESIGN - design_1' window is open, showing the 'Sources' tab. The 'constrs_1' constraint set is highlighted with a red box. The 'Constraint Set Properties' window is open, showing the 'General' tab with the target constraint file 'io.xdc'. The 'Diagram' tab shows a block diagram of the design, including an 'average_0' block, an 'average_v1_0' block, and a 'fifo_generator_0' block. The 'Reports' window at the bottom shows a list of reports, with 'impl_1_route_report_timing_summary_0' selected.

Report	Type	Options	Modified	Size
impl_1_route_report_drc_0	report_drc		8/11/20, 11:10 AM	4.5 KB
impl_1_route_report_methodology_0	report_methodology		8/11/20, 11:10 AM	18.2 KB
impl_1_route_report_power_0	report_power		8/11/20, 11:10 AM	9.1 KB
impl_1_route_report_route_status_0	report_route_status		8/11/20, 11:10 AM	0.6 KB
impl_1_route_report_timing_summary_0	report_timing_summary	max_paths = 10;	8/11/20, 11:10 AM	7.4 KB
impl_1_route_report_incremental_reuse_0	report_incremental_reuse		8/11/20, 11:10 AM	10.5 KB
impl_1_route_report_clock_utilization_0	report_clock_utilization		8/11/20, 11:10 AM	0.9 KB
impl_1_route_report_bus_skew_0	report_bus_skew	warn_on_violation = true;	8/11/20, 11:10 AM	31.4 KB

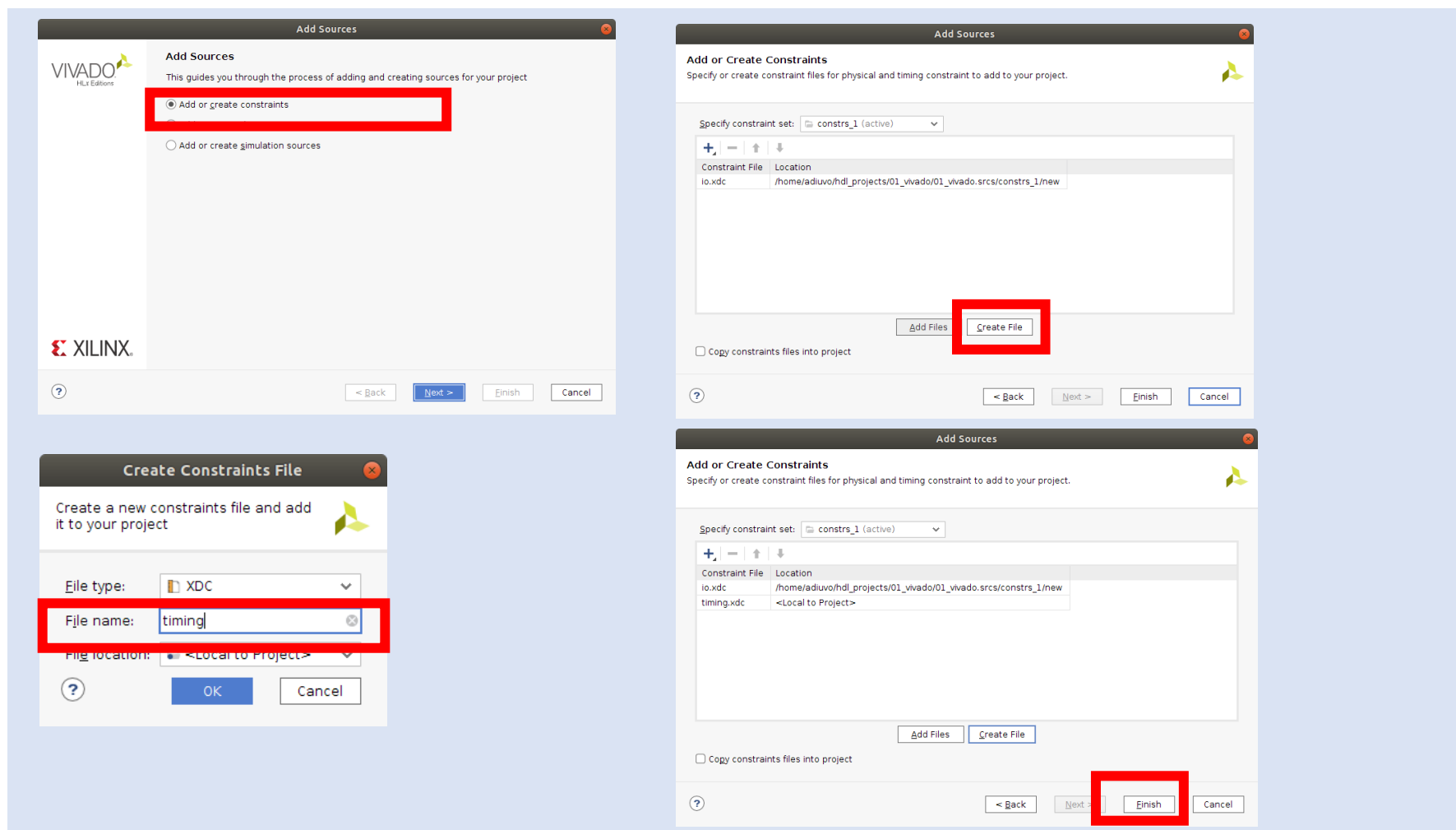
Lab 2: Intermediate Vivado

Step 39 – Click on the Add Source button.



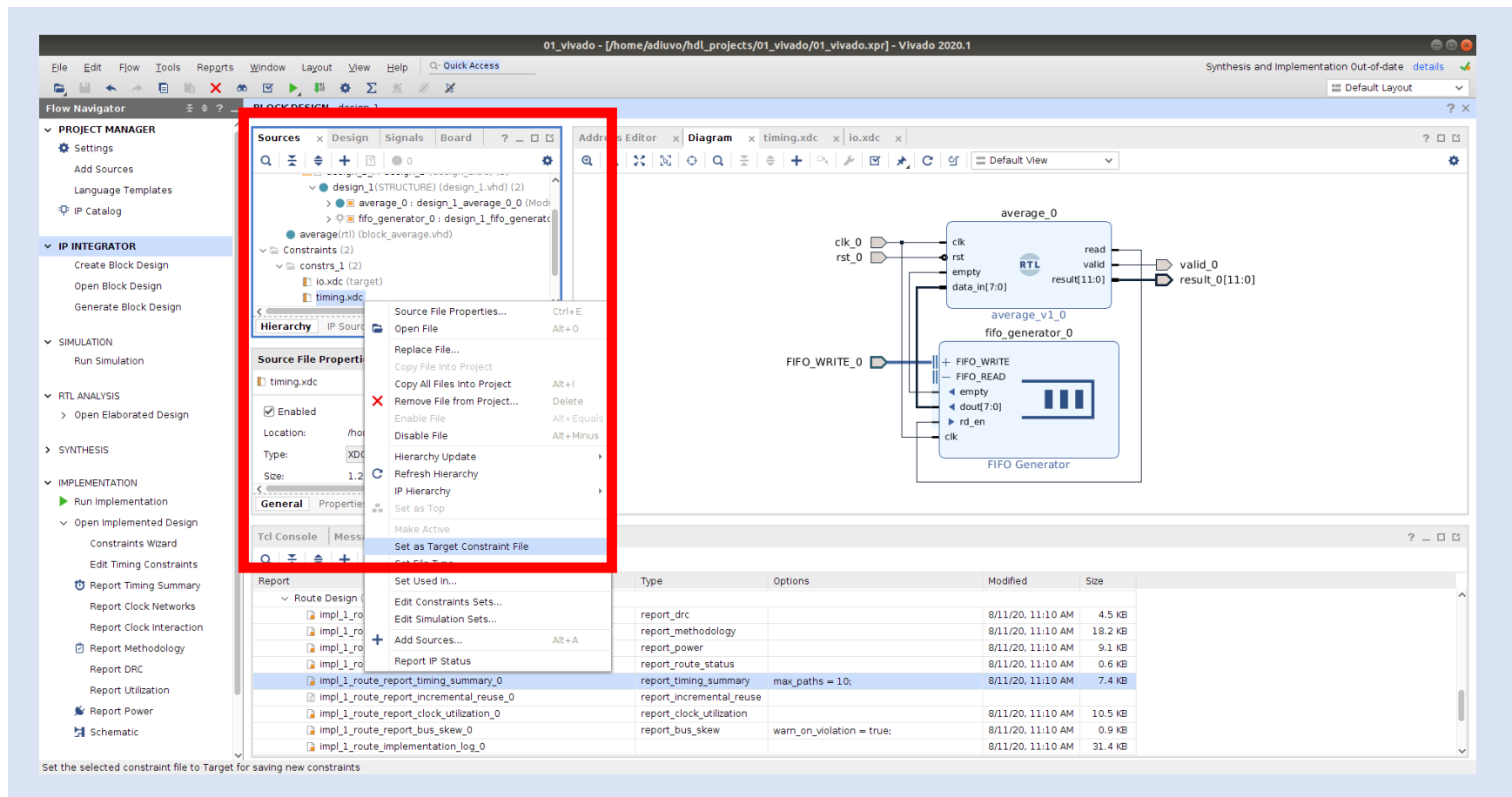
Lab 2: Intermediate Vivado

Step 40 – Select Add or Create Constraints. Then **Create File**, enter the name “**timing**” for the file, and click **Finish**.



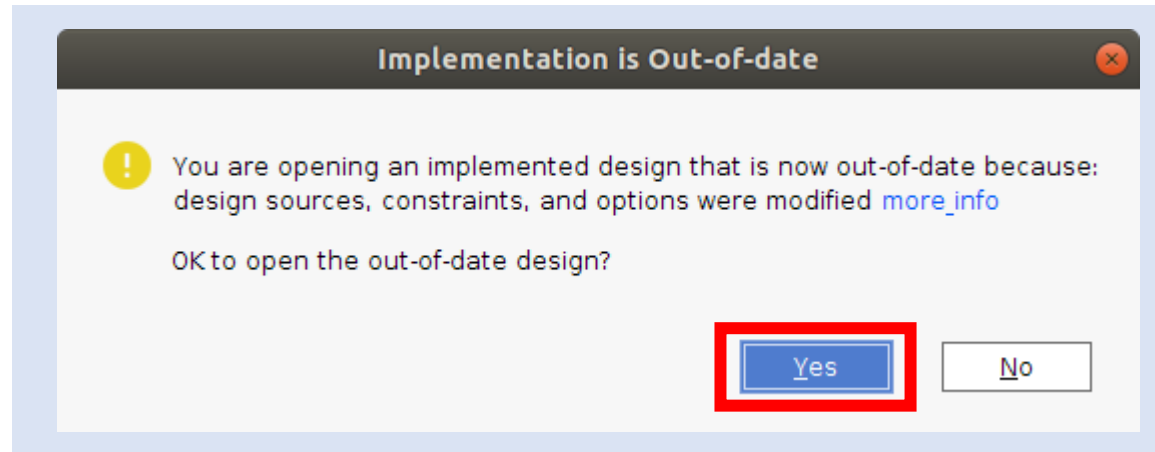
Lab 2: Intermediate Vivado

Step 41 – Right click on the newly created constraint file and select **Set as Target Constraints File**.



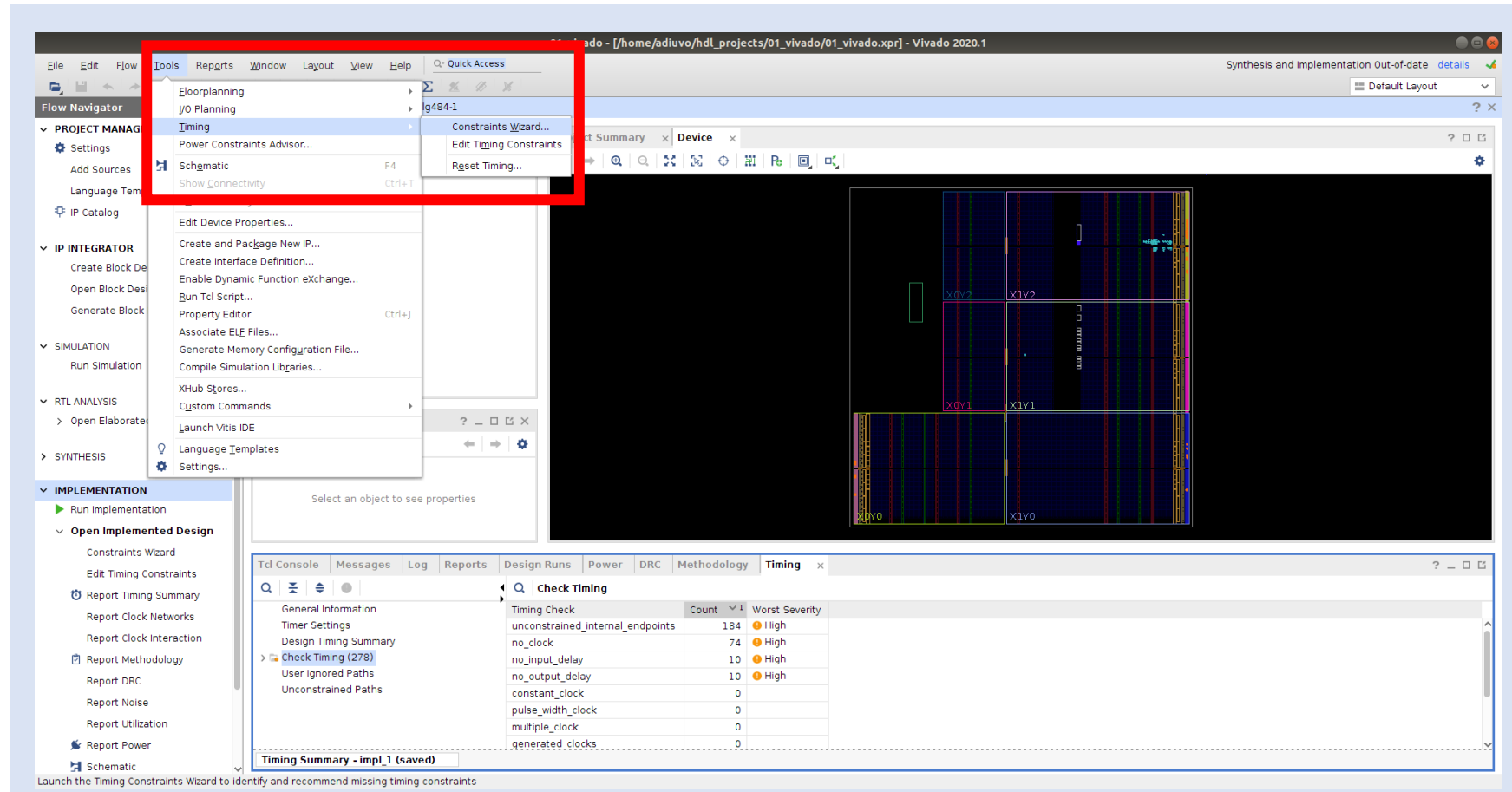
Lab 2: Intermediate Vivado

Step 42 – Open the implemented design. If you see the warning below click **OK**.



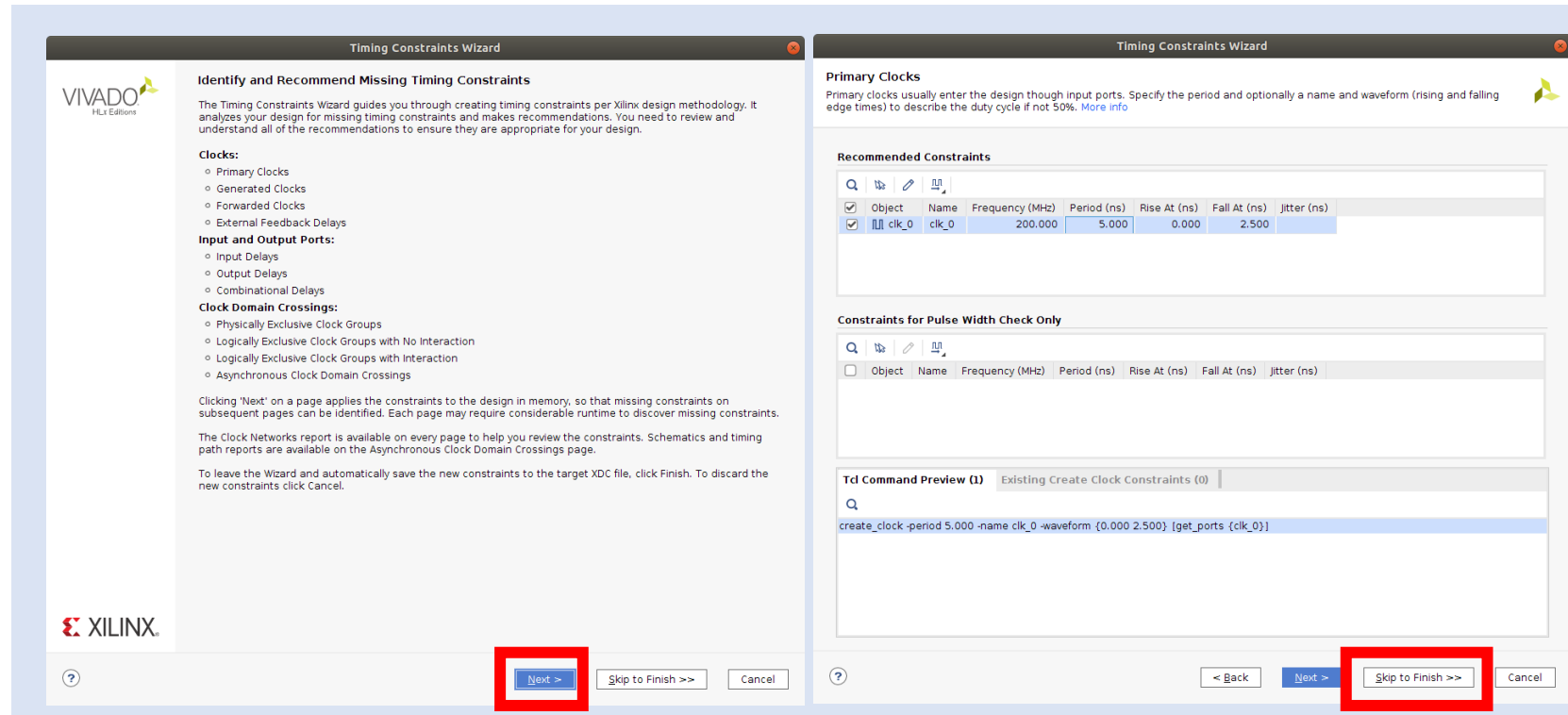
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Step 43 – From the Tools menu, select Timing -> Constraints Wizard.



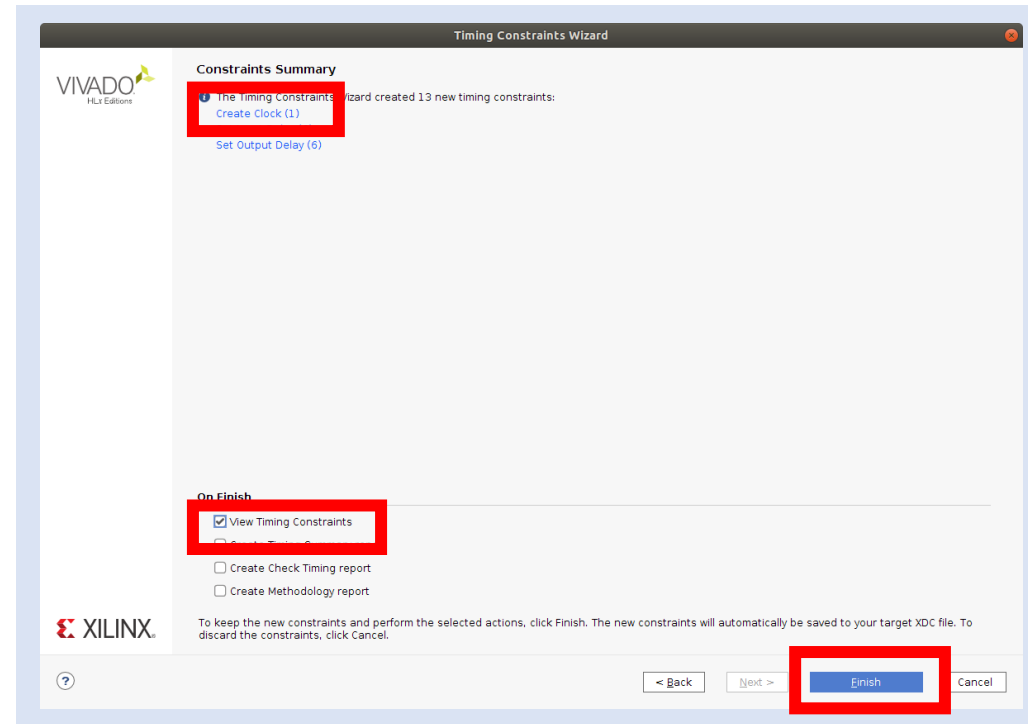
Lab 2: Intermediate Vivado

Step 44 – On the welcome screen, click **Next** and then enter **200 MHz** for the clock frequency. Once done, select **Skip to Finish**.



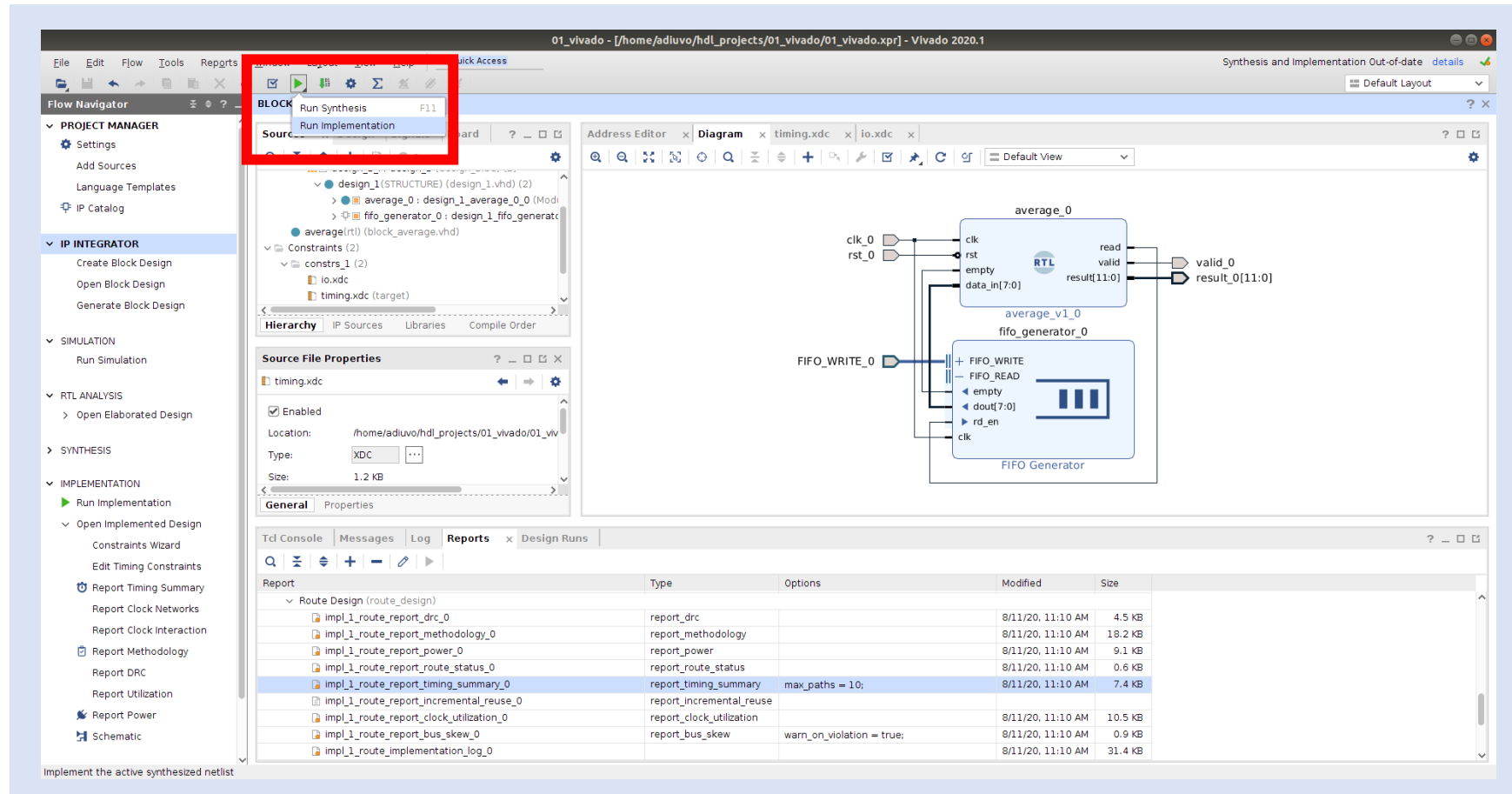
Lab 2: Intermediate Vivado

Step 45 – On the final page, check that only one constraints is being created, check the **View Timing Constraints**, and click **Finish**.



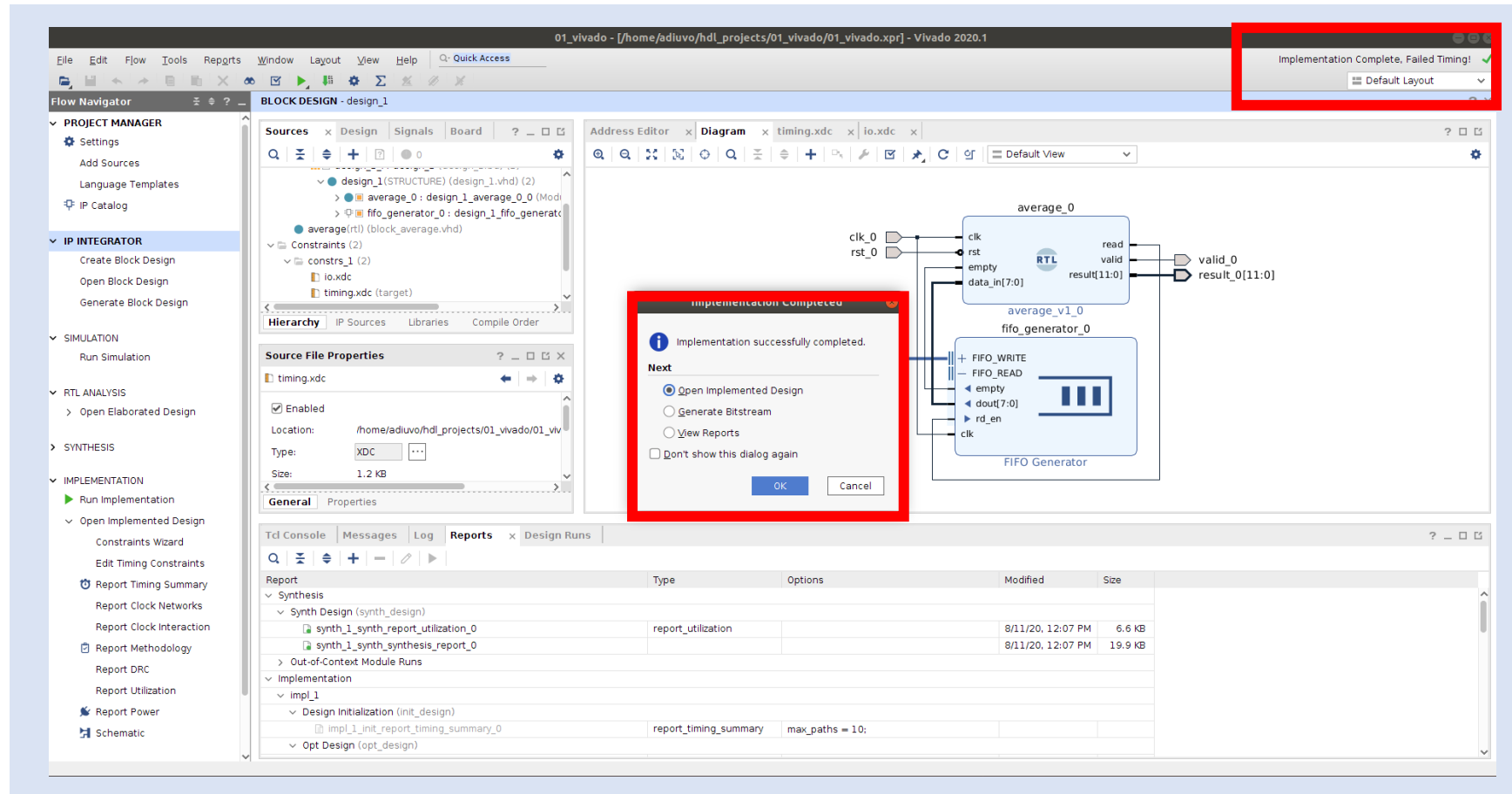
Lab 2: Intermediate Vivado

Step 46 – Close the implementation view and **rerun the implementation**. Click **OK** on any dialogs which pop up prior to implementation starting.



Lab 2: Intermediate Vivado

Step 47 – Once the implementation completes, Timing will fail. Open the **Implemented Design**.



Lab 2: Intermediate Vivado

Step 48 – In the implemented design, select the failing **Intra-Clock Paths**.

The screenshot shows the Vivado IDE interface. The top toolbar indicates 'Implementation Complete, Failed Timing!'. The left sidebar shows the 'Flow Navigator' with the 'IMPLEMENTATION' section expanded. The 'Open Implemented Design' sub-section is active, and the 'Design Timing Summary' report is selected. The main window displays the 'Design Timing Summary' report, which is highlighted with a red box. The report shows the following data:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): -5.081 ns	Worst Hold Slack (WHS): 0.189 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Total Negative Slack (TNS): -57.392 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 25	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 194	Total Number of Endpoints: 194	Total Number of Endpoints: 75

Below the table, it states: **Timing constraints are not met.**

Lab 2: Intermediate Vivado

Step 49 – Select Path 1 and zoom in. You will see that the FIFO output data passes through LUTs before finally being registered. This path is too long for timing at 200 MHz.

The screenshot shows the Vivado 2020.1 interface. The top panel displays the 'Netlist' view with a zoomed-in view of the design showing LUTs and registers. The bottom panel shows the 'Timing' report for 'Intra-Clock Paths - clk_0 - Setup'.

Path Properties:

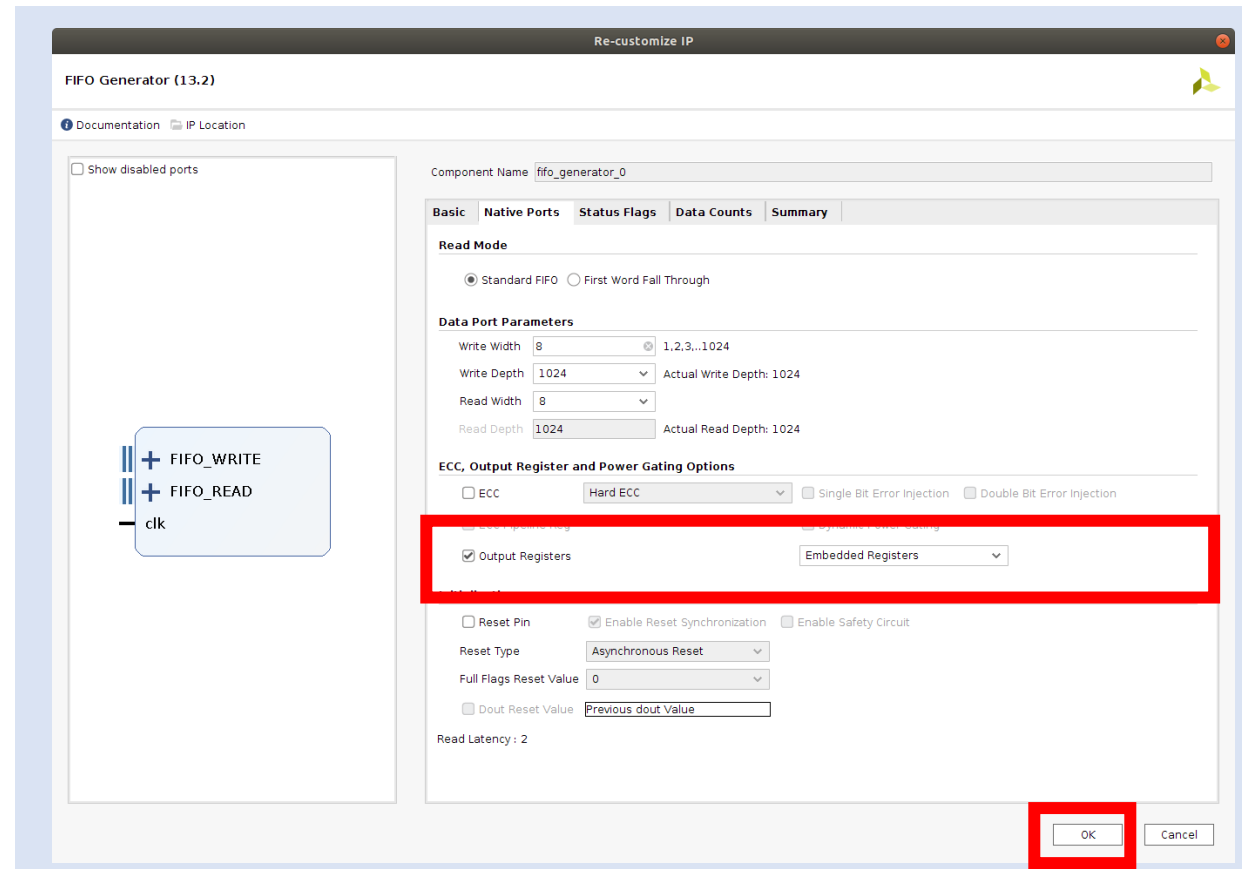
Name	Slack
Path 1	-0.249ns

Timing Summary - impl_1 (saved)

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	-0.249	5	1	design_1_jif...am/CLKBWRCLK	design_1_jif...or_reg[11]/D	5.264	3.887	1.377	5.0	clk_0	clk_0
Path 2	-0.127	4	1	design_1_jif...am/CLKBWRCLK	design_1_jif...ator_reg[7]/D	5.150	3.772	1.377	5.0	clk_0	clk_0
Path 3	-0.118	5	1	design_1_jif...am/CLKBWRCLK	design_1_jif...ator_reg[8]/D	5.090	3.763	1.327	5.0	clk_0	clk_0
Path 4	-0.108	5	1	design_1_jif...am/CLKBWRCLK	design_1_jif...or_reg[10]/D	5.077	3.783	1.294	5.0	clk_0	clk_0
Path 5	-0.024	5	1	design_1_jif...am/CLKBWRCLK	design_1_jif...ator_reg[9]/D	5.040	3.875	1.165	5.0	clk_0	clk_0
Path 6	-0.005	4	1	design_1_jif...am/CLKBWRCLK	design_1_jif...ator_reg[4]/D	4.976	3.649	1.327	5.0	clk_0	clk_0
Path 7	0.004	4	1	design_1_jif...am/CLKBWRCLK	design_1_jif...ator_reg[6]/D	4.963	3.669	1.294	5.0	clk_0	clk_0

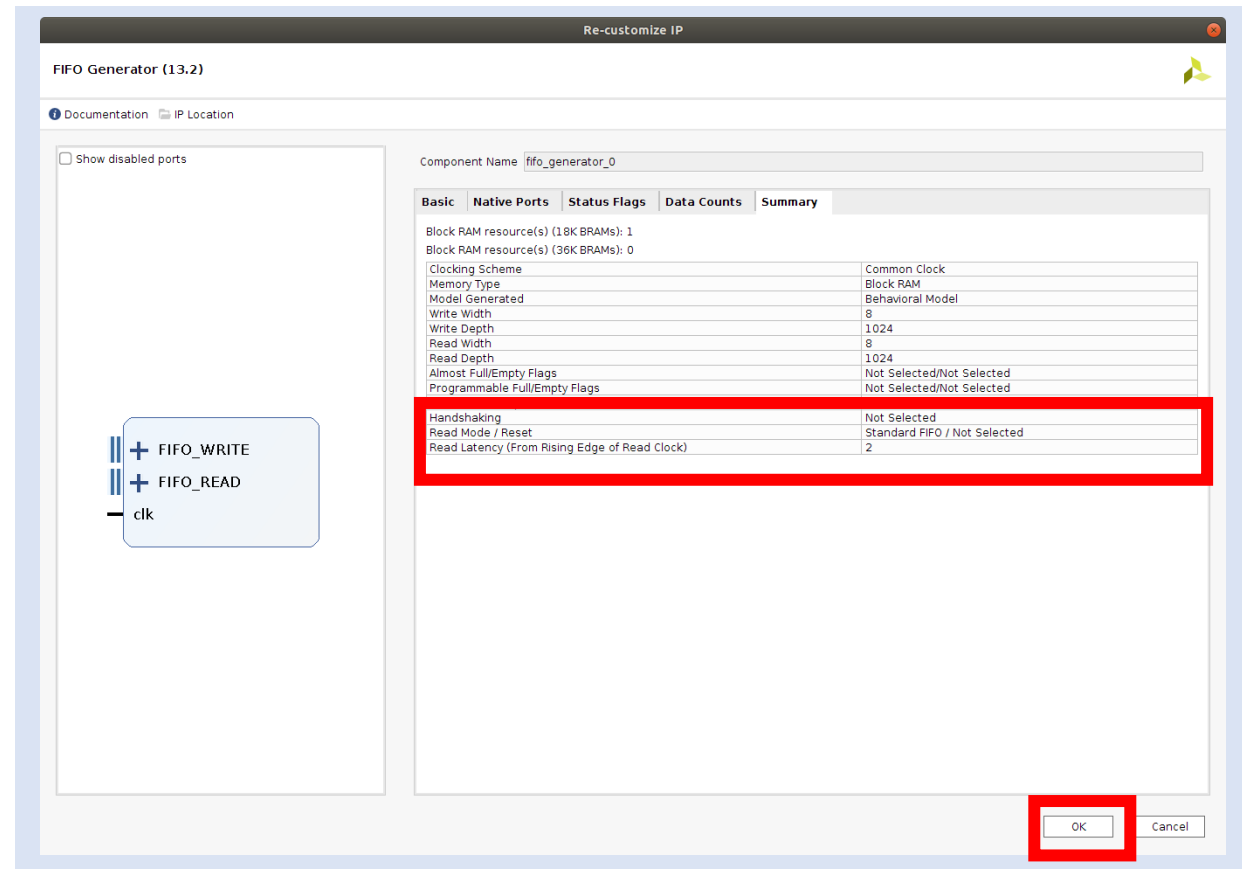
Lab 2: Intermediate Vivado

Step 50 – To fix this, we need to register the output of the FIFO. Close the implementation view and reopen the block diagram. Double click on the **FIFO** to customize.



Lab 2: Intermediate Vivado

Step 51 – Note the latency has changed from 1 to 2 clocks. We would need to correct for this in the average block, however, we proceed assuming that we have.



Lab 2: Intermediate Vivado

Step 52 – Reimplement the design. When the timing is completed, you should see that the implementation is correct and the timing is met.

The screenshot shows the Vivado 2020.1 interface. The top status bar indicates "Implementation Complete" with a green checkmark. The left sidebar shows the "Flow Navigator" with the "SYNTHESIS" section expanded, highlighting "Run Synthesis". The main workspace displays the "Netlist" view, showing the design hierarchy: "design_1_wrapper" containing "Nets (51)", "Leaf Cells (26)", and "design_1_i (design_1)". The "Block Properties" panel is empty. The bottom panel shows the "Design Timing Summary" report, which includes the following data:

Setup			Hold			Pulse Width		
Worst Negative Slack (WNS):	0.172 ns		Worst Hold Slack (WHS):	0.185 ns		Worst Pulse Width Slack (WPWS):	2.000 ns	
Total Negative Slack (TNS):	0.000 ns		Total Hold Slack (THS):	0.000 ns		Total Pulse Width Negative Slack (TPWS):	0.000 ns	
Number of Failing Endpoints:	0		Number of Failing Endpoints:	0		Number of Failing Endpoints:	0	
Total Number of Endpoints:	151		Total Number of Endpoints:	151		Total Number of Endpoints:	76	

All user specified timing constraints are met.