

Getting to Know Vivado

Course Workbook

Table of Contents

About this Workbook	<u>Page 3</u>
Pre-Lab: Workshop Pre-requisites	<u>Page 4</u>
Lab 3: Advanced Vivado	<u>Page 7</u>

About this Workbook

This workbook is designed to be used in conjunction with the Getting to Know Vivado course.

The contents of this workbook are created by Aduvo Engineering & Training, Ltd.

If you have any questions about the contents or need assistance, please contact Adam Taylor at adam@adiuvoengineering.com.

Pre-Lab

Workshop Pre-requisites

Required Hardware

There is no required hardware for this course.

Downloads and Installations

Step 1 – Download and install the following at least one day prior to the workshop. This may take a significant amount of time and drive space.

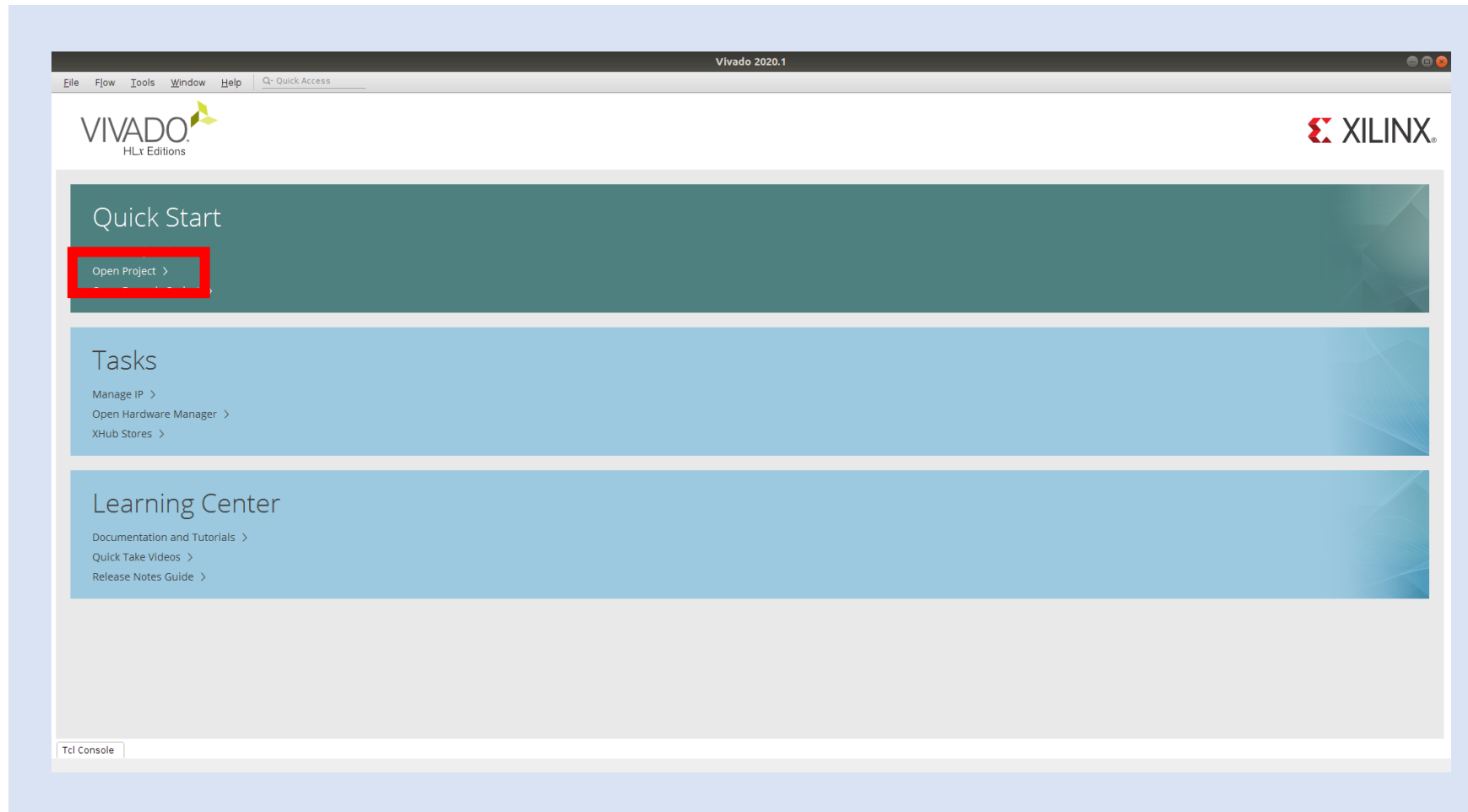
Vivado 2020.1	Download
Source Project Files	Download
Lab 2 must be completed	

Lab 3

Advanced Vivado

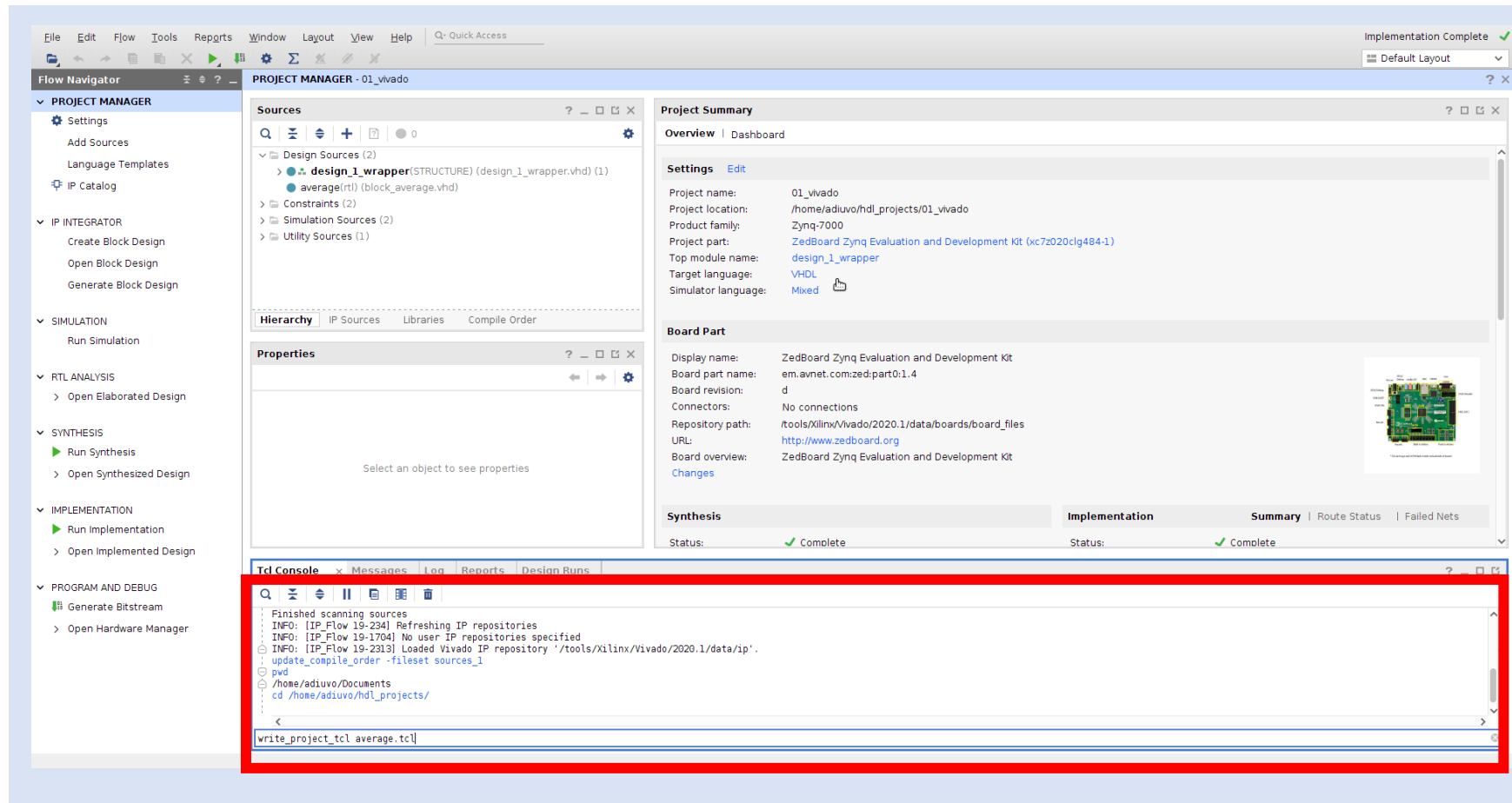
Lab 3: Advanced Vivado

Step 1 – Open the project created in part two.



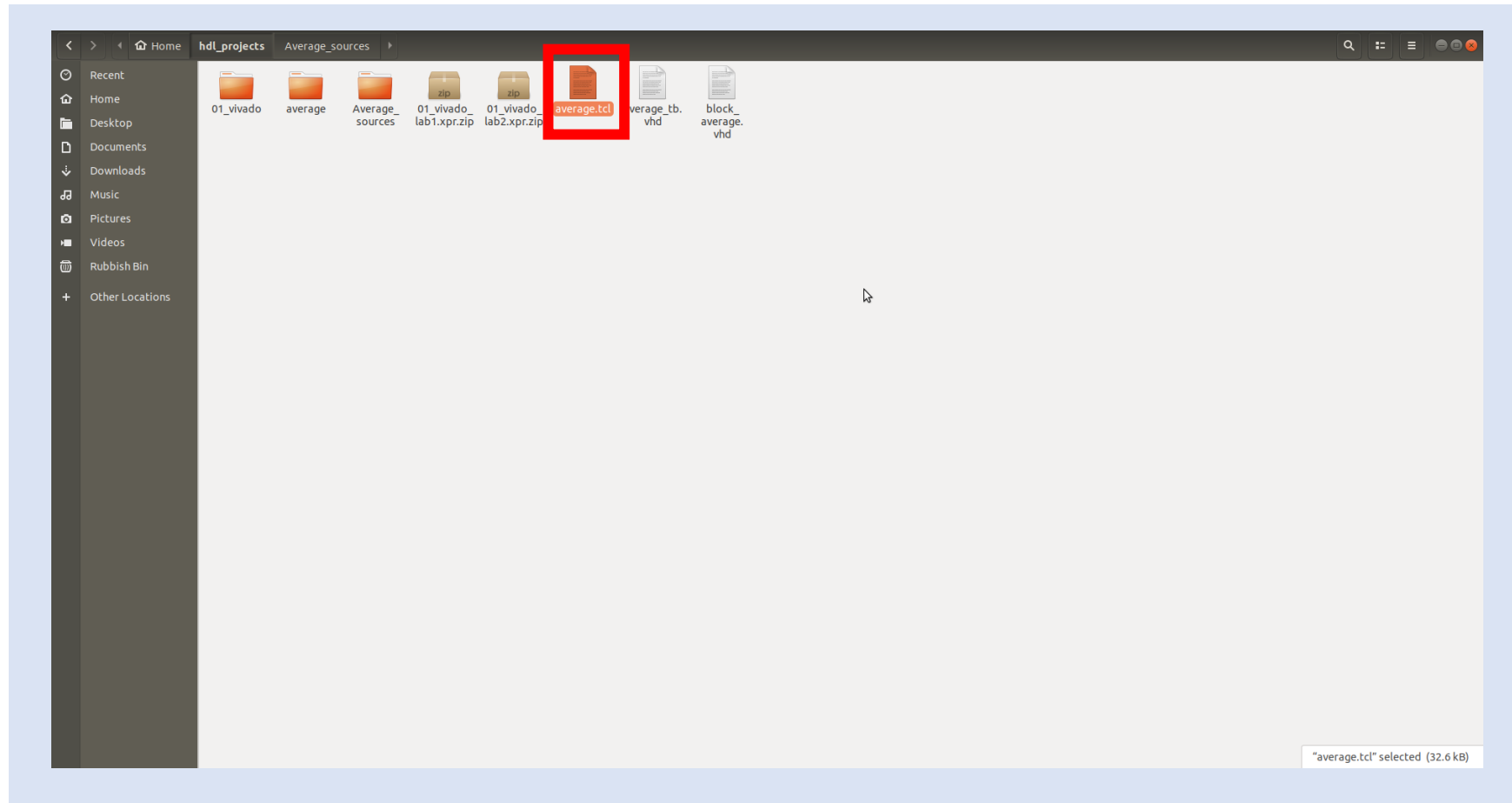
Lab 3: Advanced Vivado

Step 2 – In the TCL window, check the PWD and change directory to the location containing your project. Then enter the command `write_project_tcl average.tcl`.



Lab 3: Advanced Vivado

Step 3 – This will write a project description in TCL to the project directory.



Lab 3: Advanced Vivado

Step 4 – Open the TCL file and change the project name from 01_Vivado to 01_Vivado_rebuild.

```

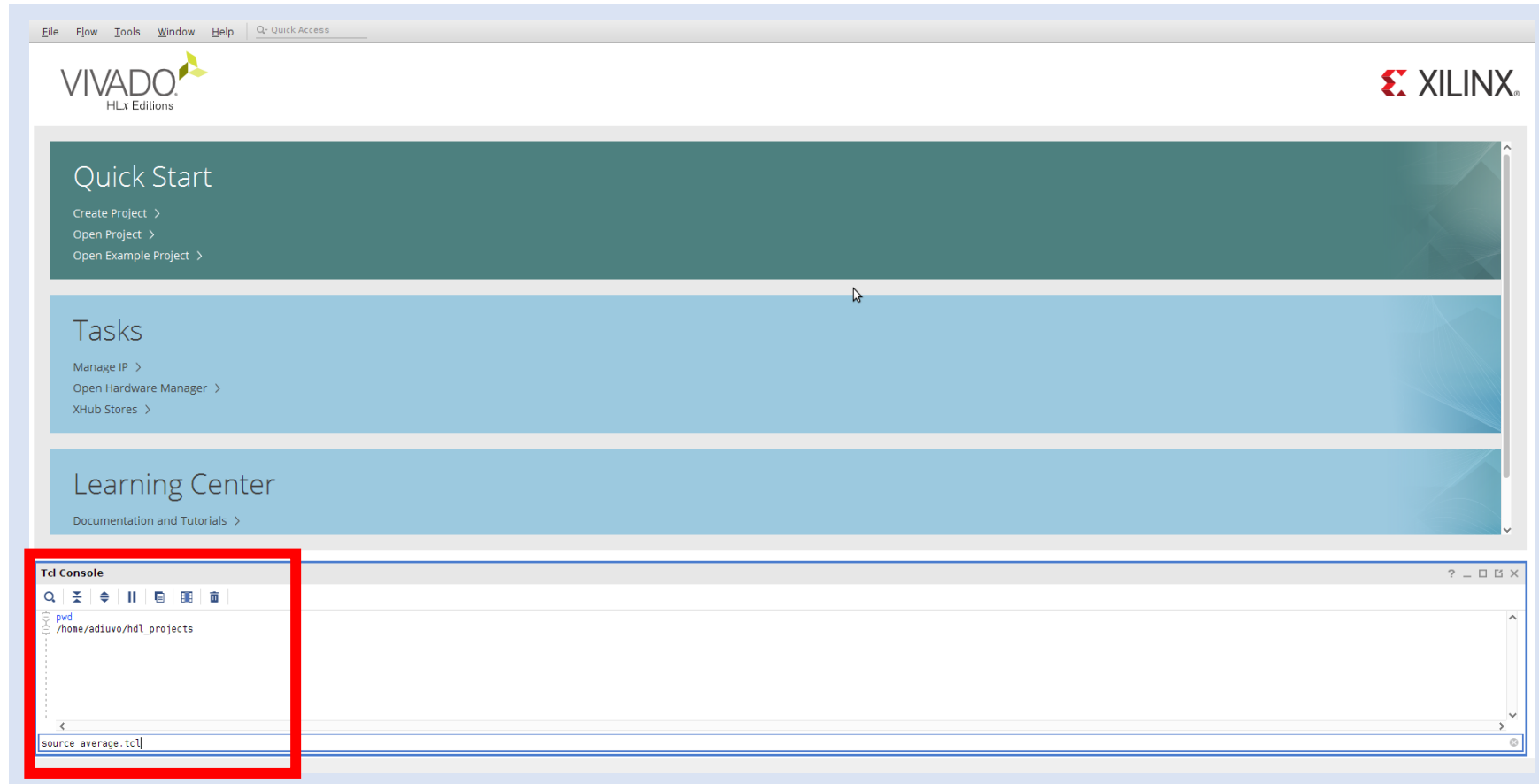
Open ▾  average.tcl
~/hdl_projects

#*****
# Vivado (TM) v2020.1 (64-bit)
#
# average.tcl: Tcl script for re-creating project '01_vivado'
#
# Generated by Vivado on Wed Aug 12 14:33:43 BST 2020
# IP Build 2902112 on Wed May 27 22:43:36 MDT 2020
#
# This file contains the Vivado Tcl commands for re-creating the project to the state*
# when this script was generated. In order to re-create the project, please source this
# file in the Vivado Tcl Shell.
#
# * Note that the runs in the created project will be configured the same way as the
# original project, however they will not be launched automatically. To regenerate the
# run results please launch the synthesis/implementation runs as needed.
#
#*****
# NOTE: In order to use this script for source control purposes, please make sure that the
#       following files are added to the source control system:-
#
# 1. This project restoration tcl script (average.tcl) that was generated.
#
# 2. The following source(s) files that were local or imported into the original project.
#    (Please see the 'Sorig_proj_dir' and 'Sorigin_dir' variable setting below at the start of the script)
#
#    "/home/adiuvo/hdl_projects/01_vivado/01_vivado.srcs/sources_1/bd/design_1/hdl/design_1_wrapper.vhd"
#    "/home/adiuvo/hdl_projects/01_vivado/01_vivado.srcs/constrs_1/new/io.xdc"
#    "/home/adiuvo/hdl_projects/01_vivado/01_vivado.srcs/constrs_1/new/timing.xdc"
#    "/home/adiuvo/hdl_projects/01_vivado/01_vivado.runs/impl_1/rqs_report.rqs"
#
# 3. The following remote source files that were added to the original project:-
#
#    "/home/adiuvo/hdl_projects/block_average.vhd"
#    "/home/adiuvo/hdl_projects/average_tb.vhd"
#
#*****
# Set the reference directory for source file relative paths (by default the value is script directory path)
set origin_dir "."
# Use origin directory path location variable, if specified in the tcl shell
if { [info exists ::origin_dir_loc] } {
    set origin_dir "${origin_dir_loc}/${origin_dir}"
}
# Set the project name
set _xil_proj_name_ "01_vivado_rebuild"
# ***** Vivado Tcl Shell *****
if { [info exists ::user_project_name] } {
    set _xil_proj_name_ ${::user_project_name}
}

```

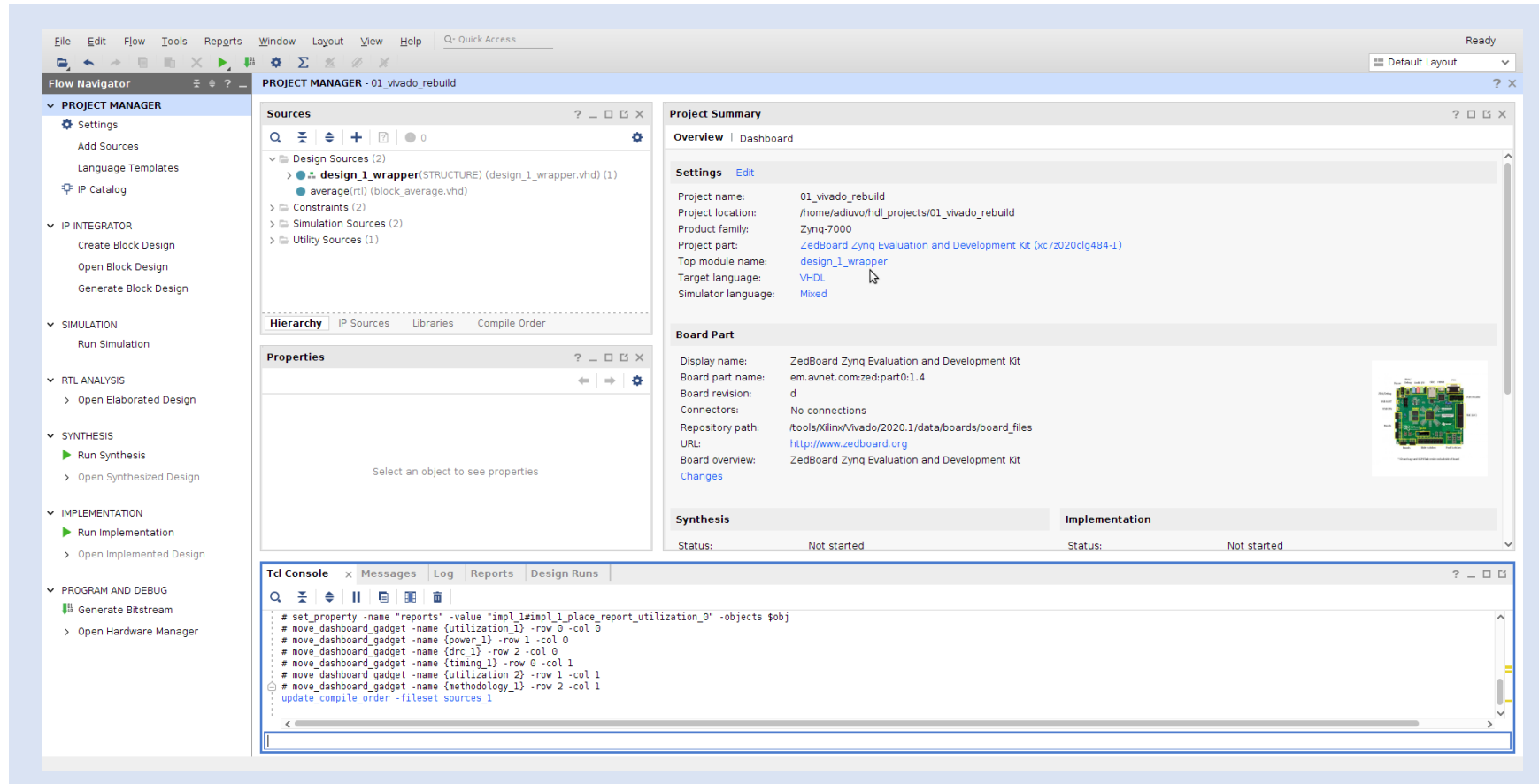
Lab 3: Advanced Vivado

Step 5 – Close the current project and type `source average.tcl` in the TCL window.



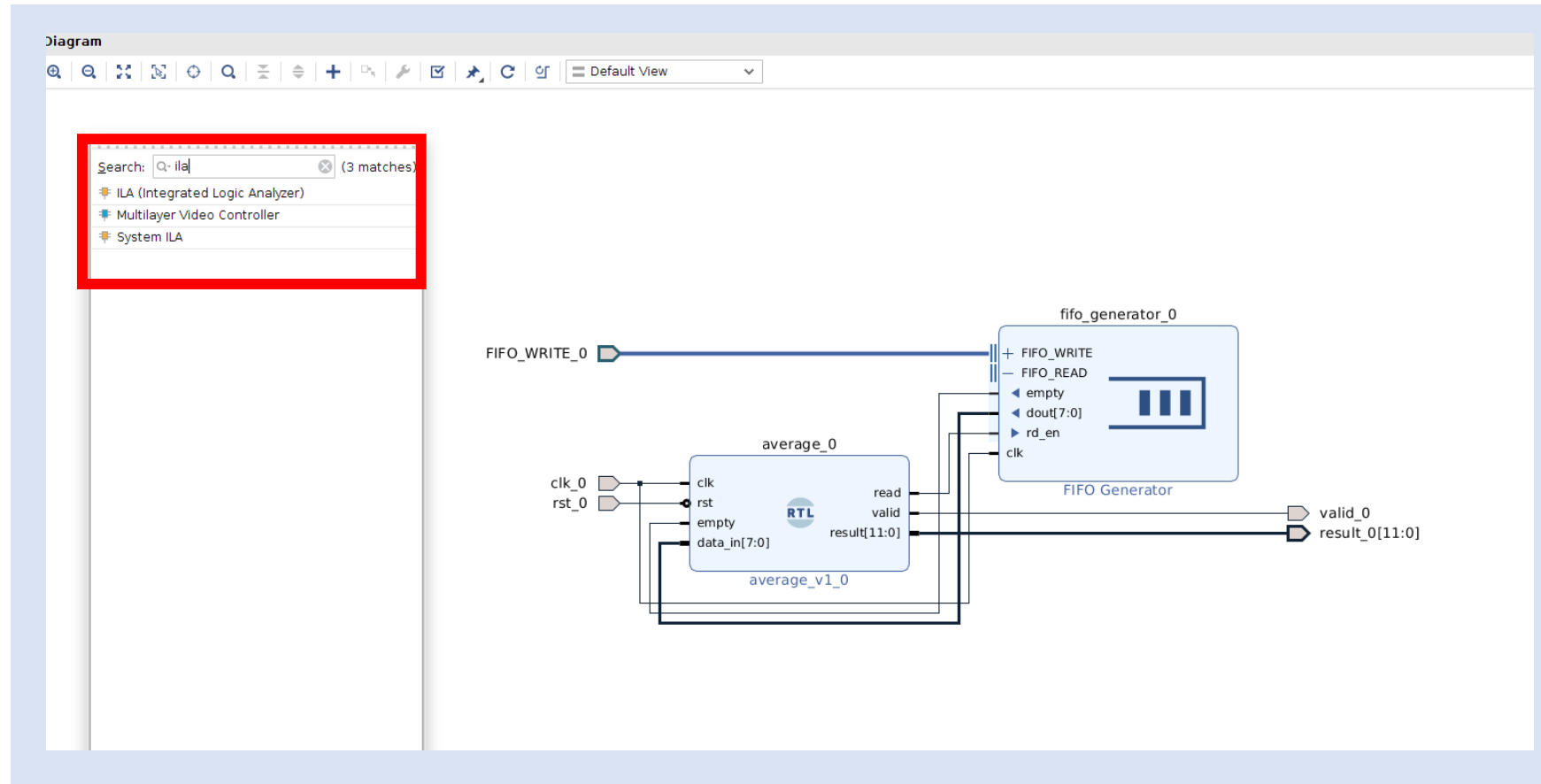
Lab 3: Advanced Vivado

Step 6 – This will rebuild the project exactly as before from the TCL file.



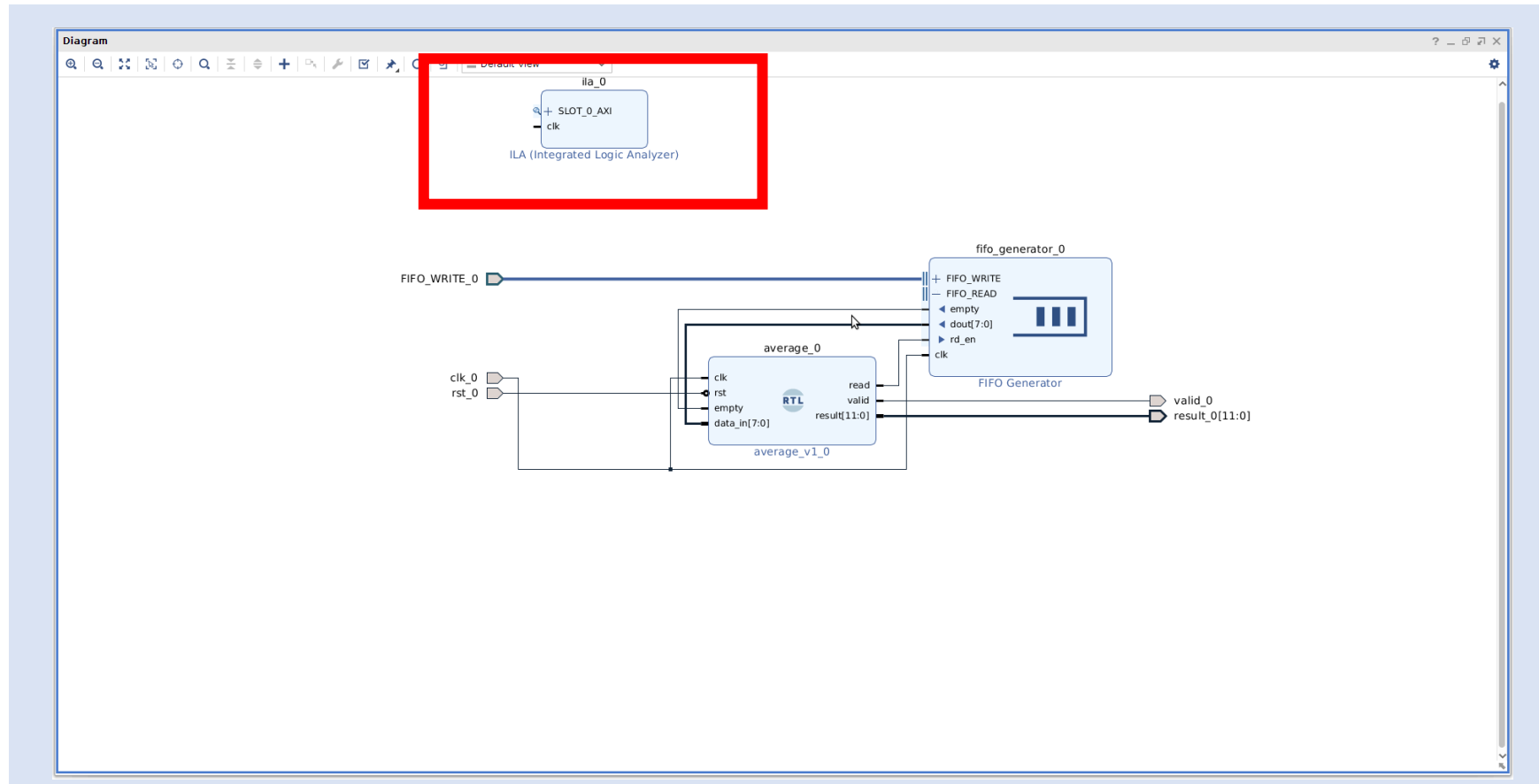
Lab 3: Advanced Vivado

Step 7 – Open the block design and click on the **+** symbol to add in IP. In the search bar, enter **ILA** and then double click on the **ILA (Integrated Logic Analyzer)** to add in the IP core.



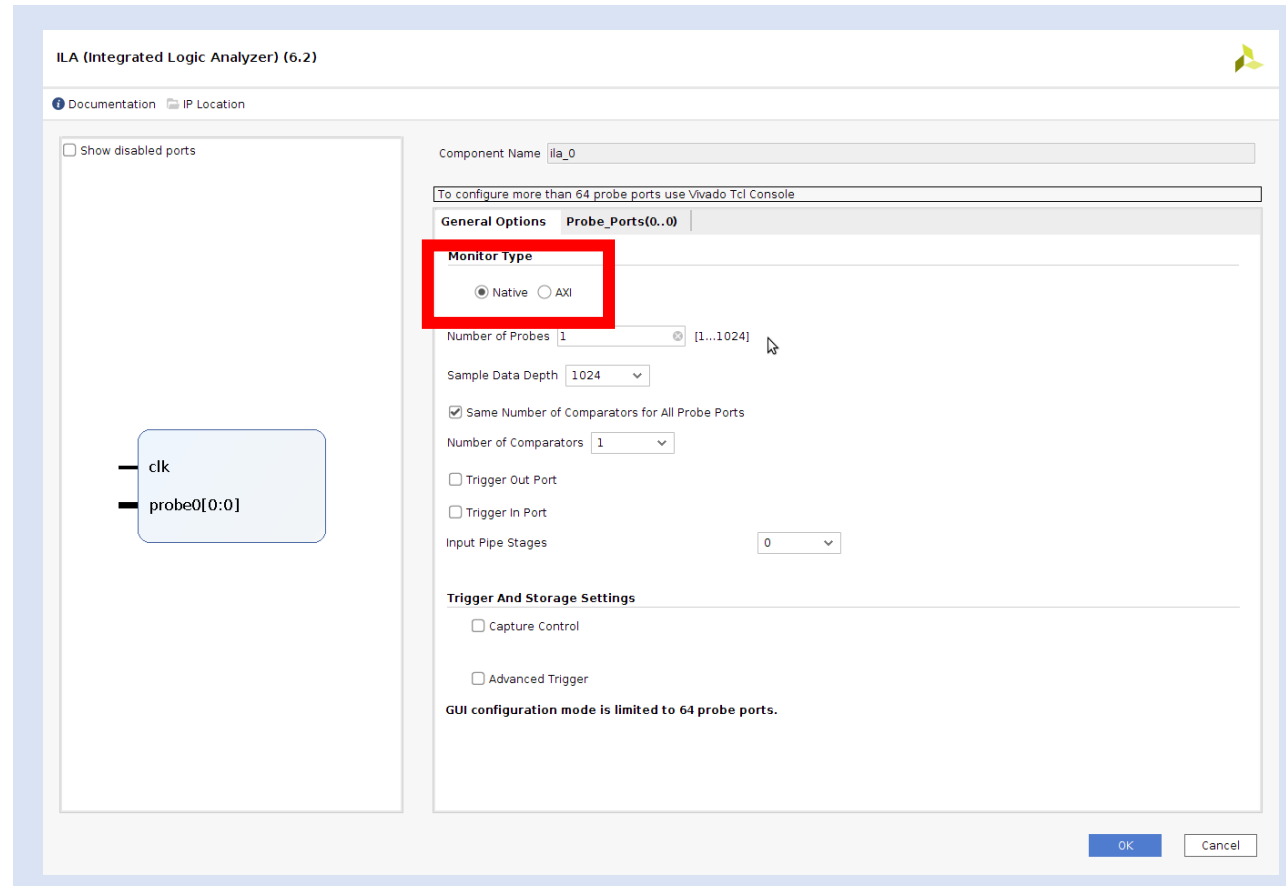
Lab 3: Advanced Vivado

Step 8 – Double click on the **ILA** to customize it.



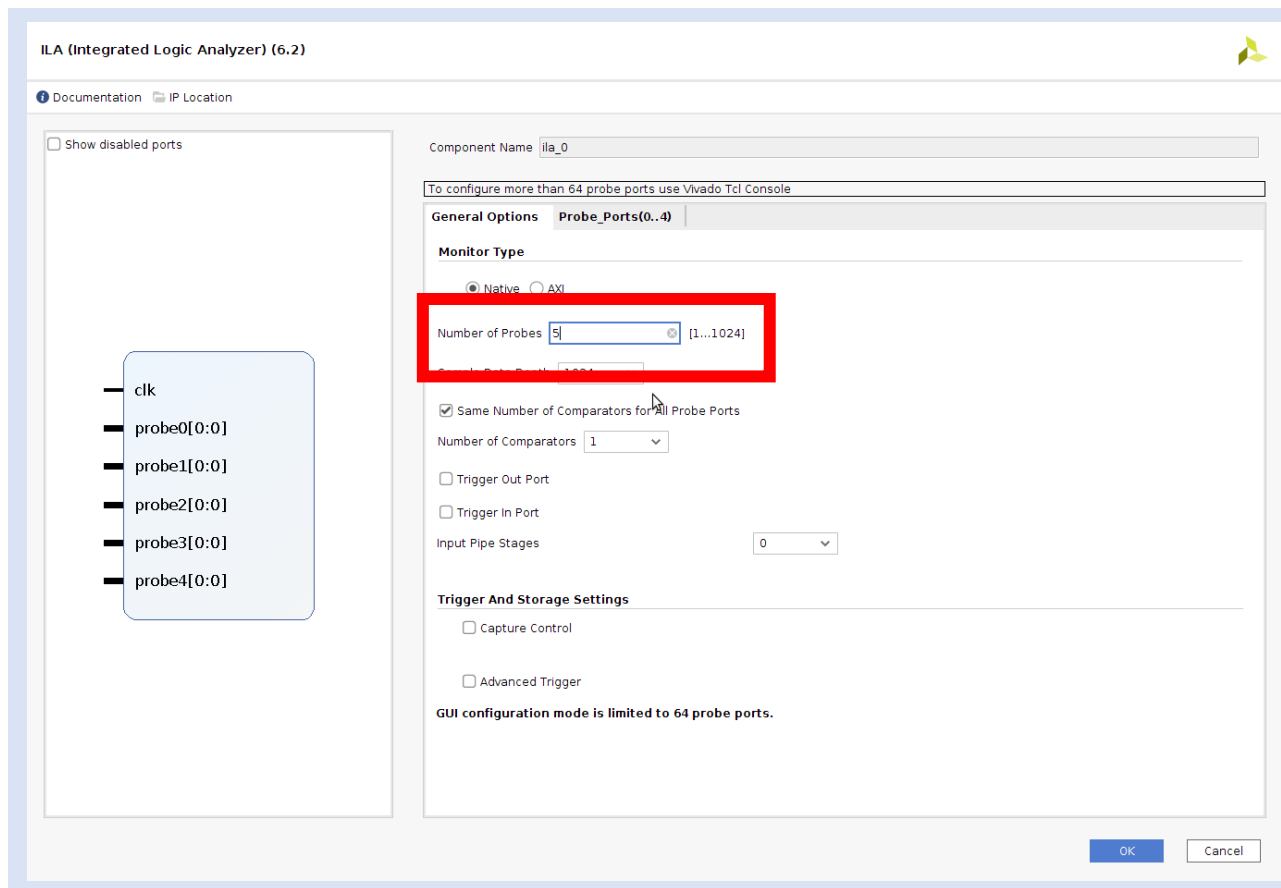
Lab 3: Advanced Vivado

Step 9 – Change the monitor type to **Native**.



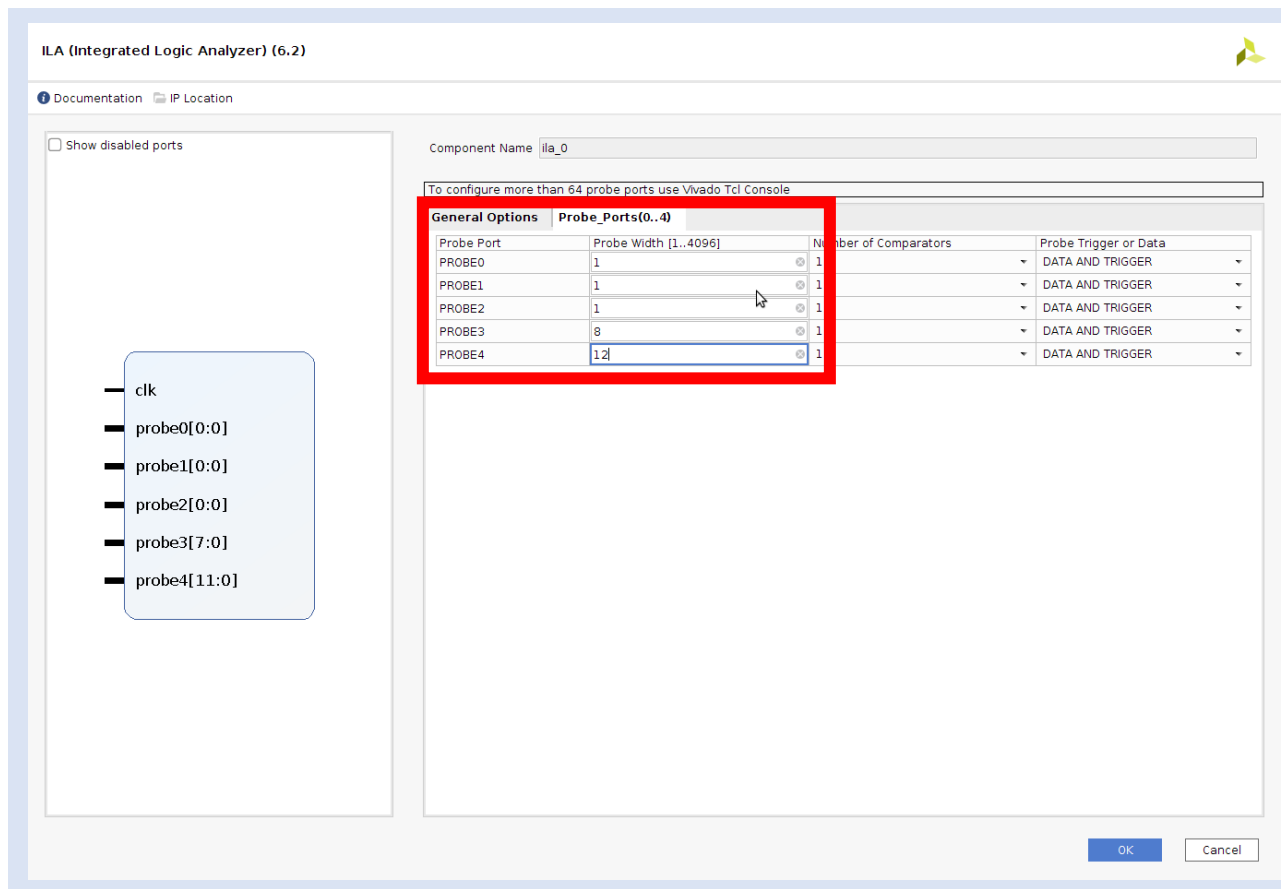
Lab 3: Advanced Vivado

Step 10 – Set the number of probes to 5.



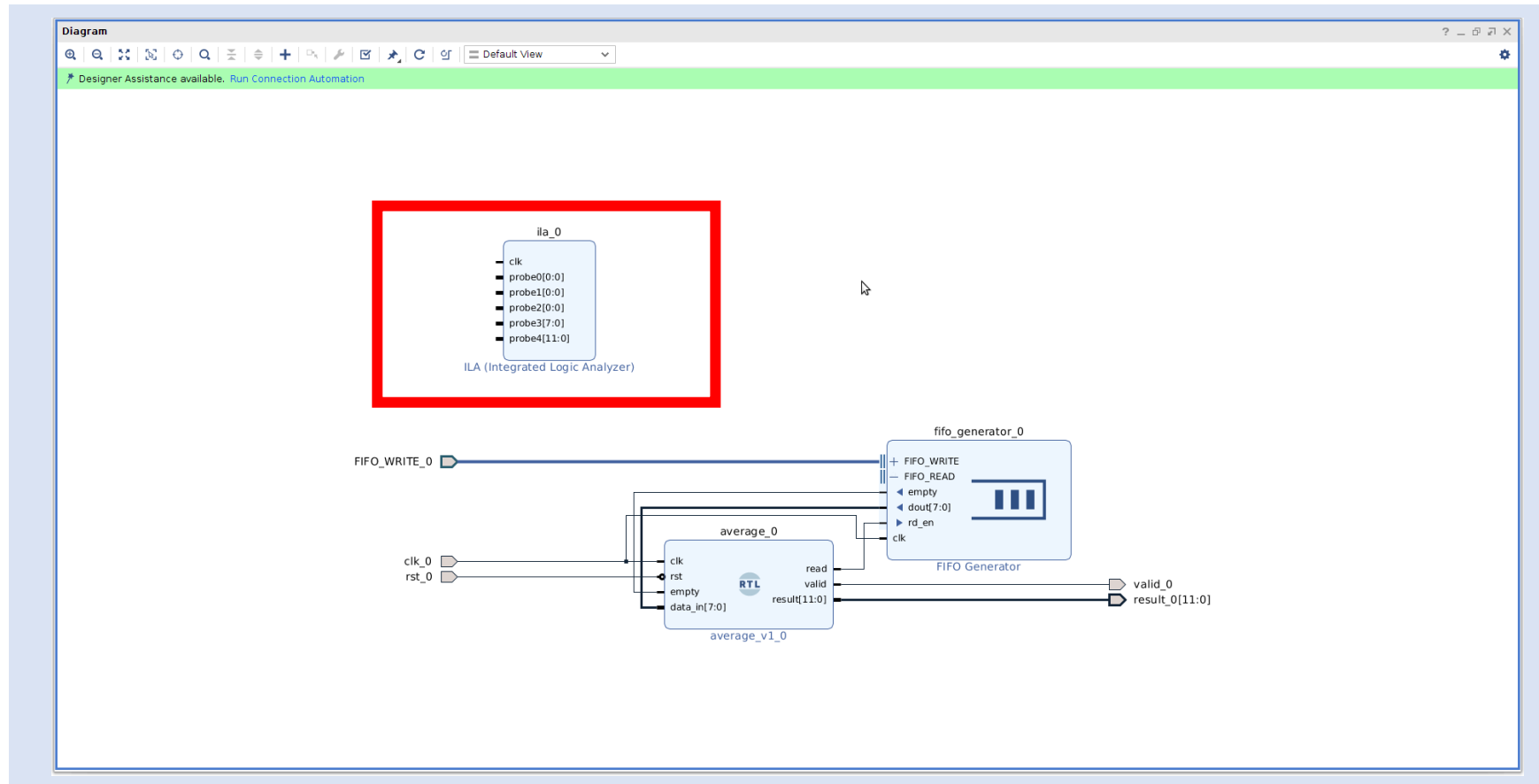
Lab 3: Advanced Vivado

Step 11 – Click on the **Probe Ports Tab** and set the widths of **PROBE3 to 8** and **PROBE4 to 12**, click **OK**.



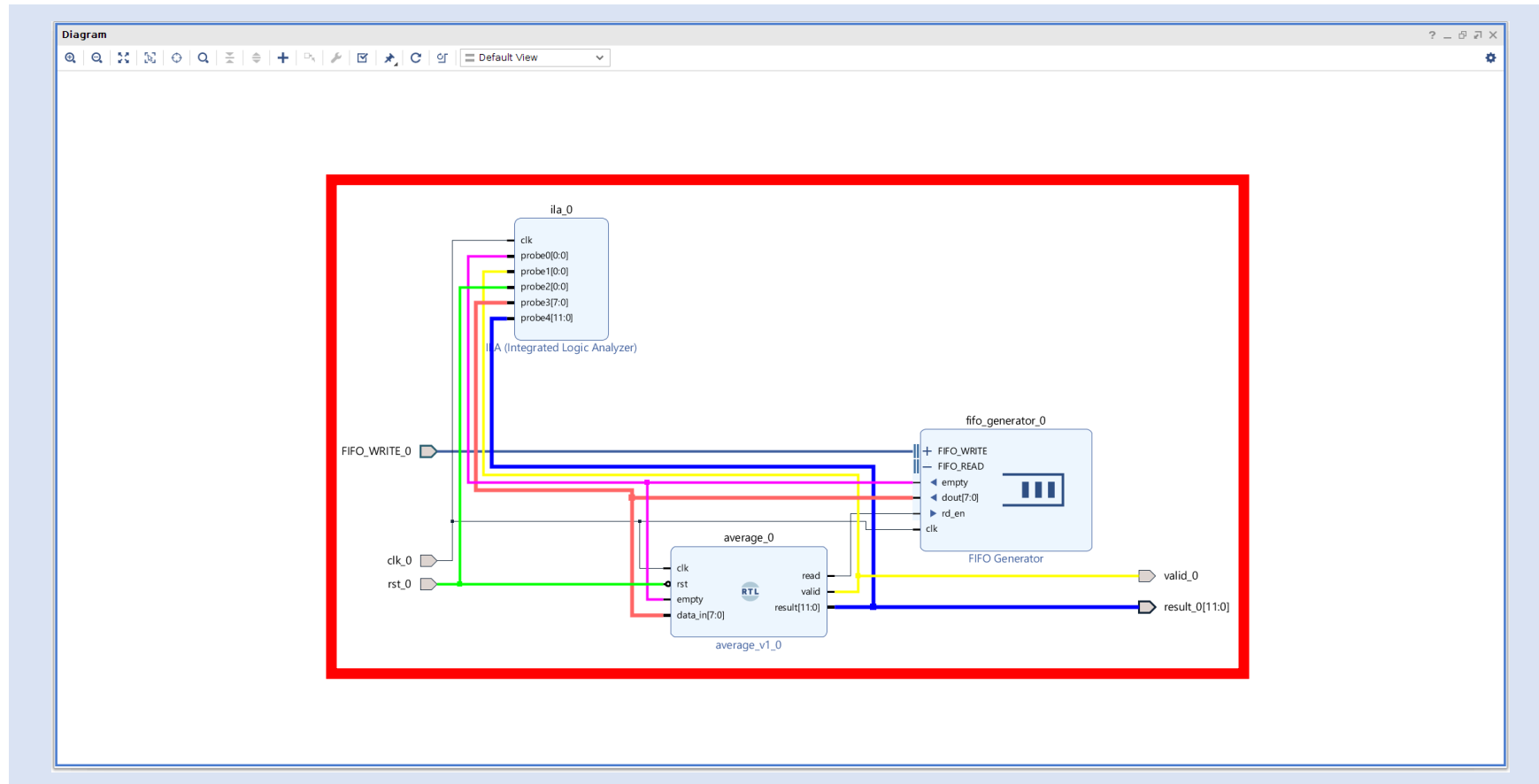
Lab 3: Advanced Vivado

Step 12 – The block diagram should now show the ILA with five ports and a clock input.



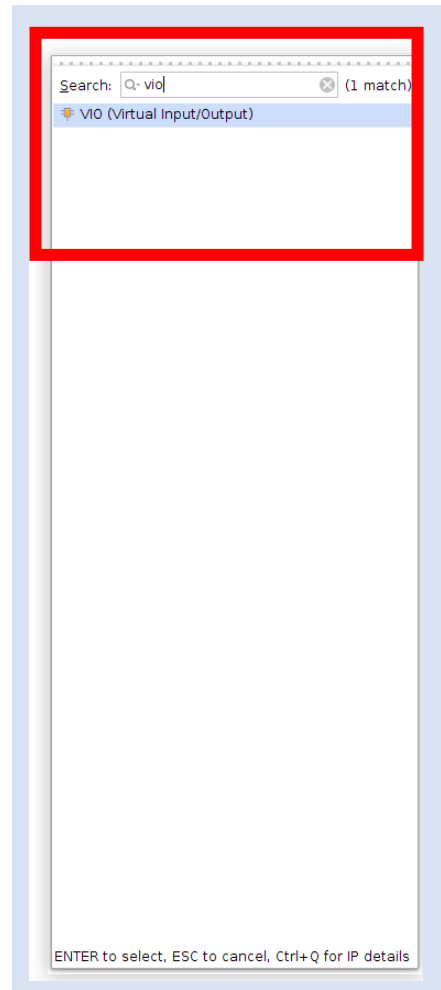
Lab 3: Advanced Vivado

Step 13 – Connect up the ILA as shown below. This will provide us visibility of all input and output of the average block.



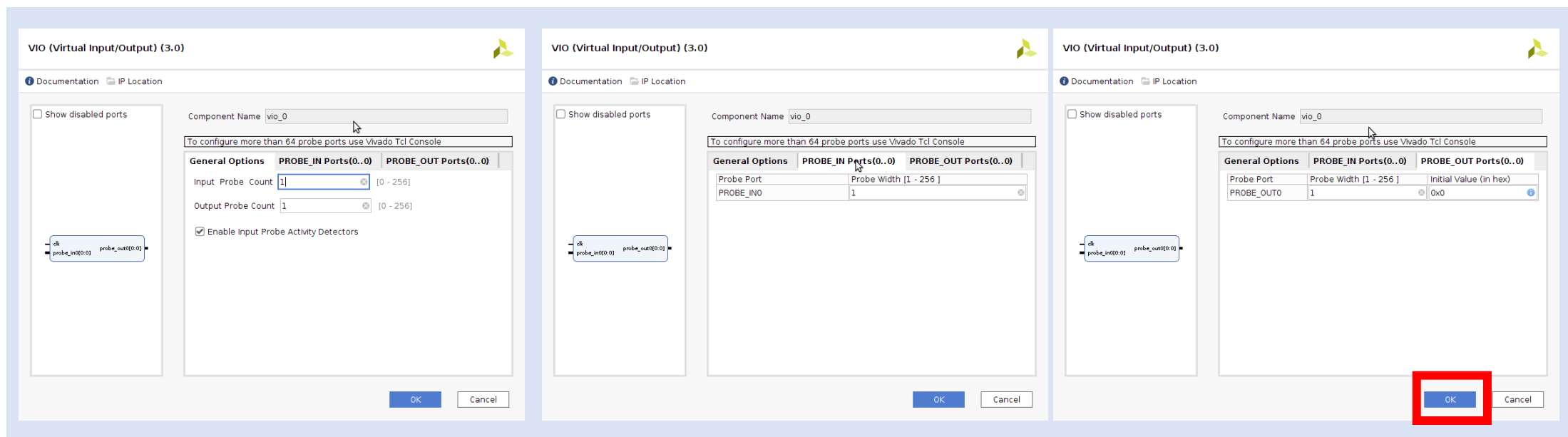
Lab 3: Advanced Vivado

Step 14 – Click on the **+** symbol to add in IP and type **VIO** in the search box. Double click on the **VIO** symbol.



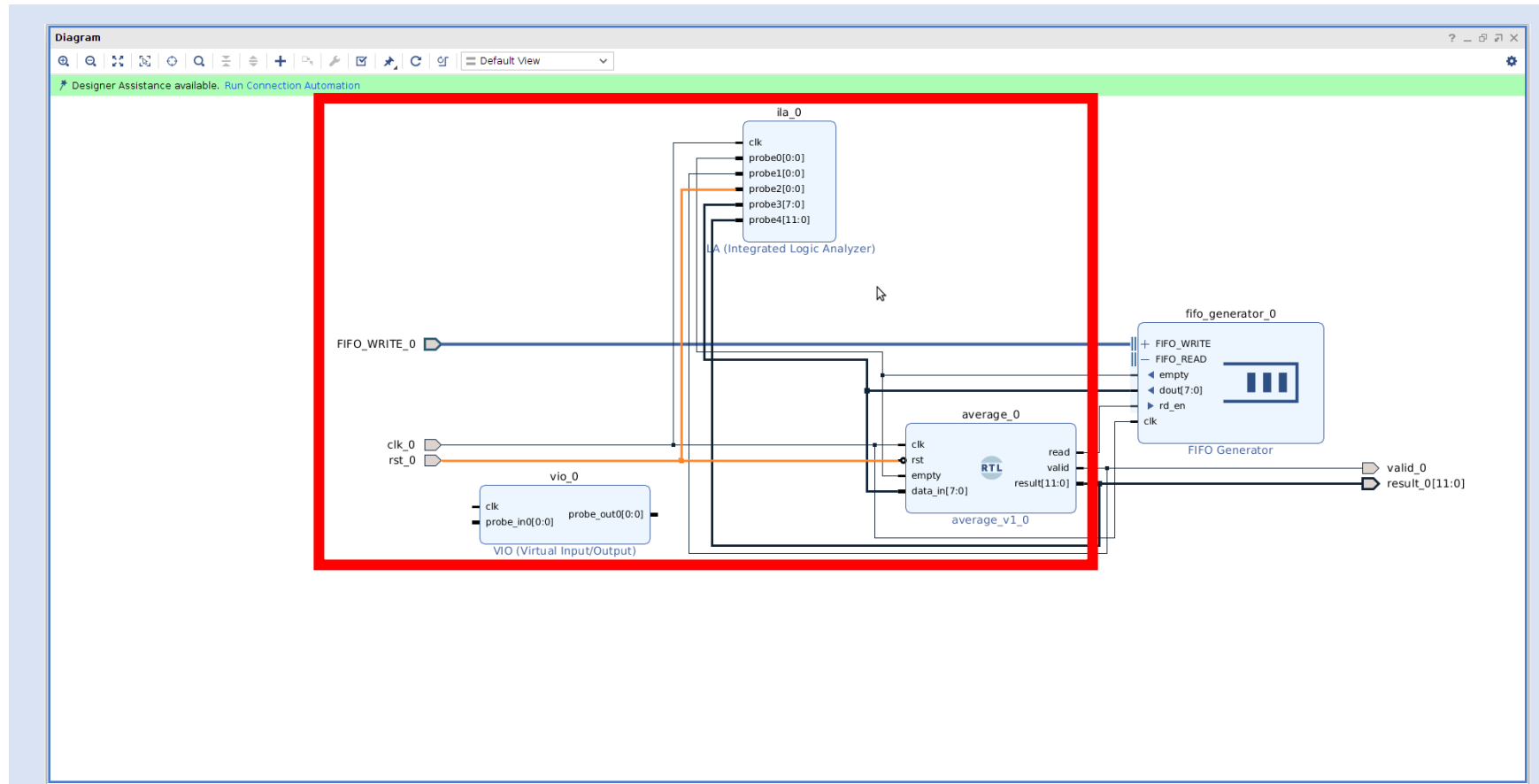
Lab 3: Advanced Vivado

Step 15 – When the VIO is added onto the block diagram, double click it to customize and explore the three tabs. Leave it all unchanged and click **OK**.



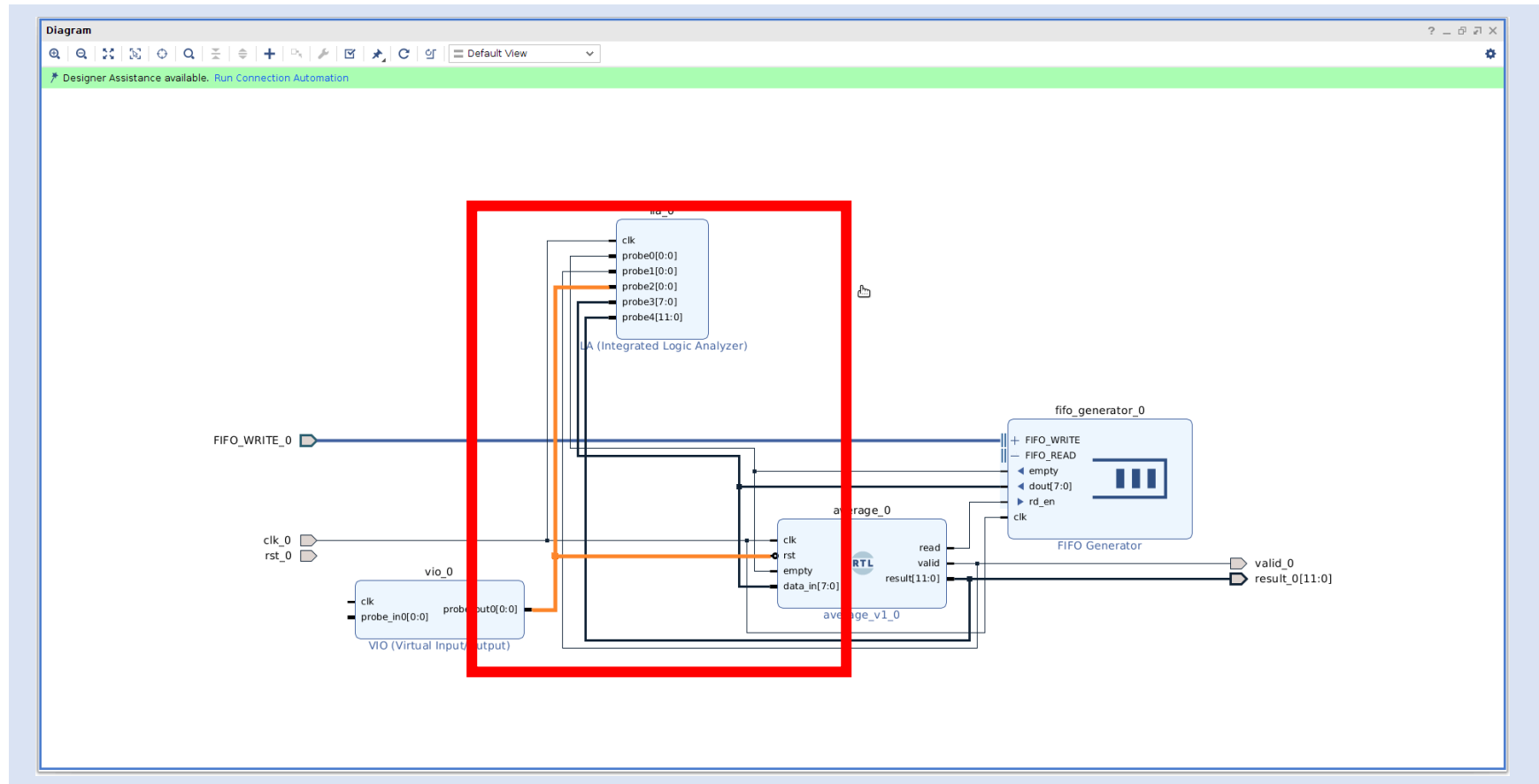
Lab 3: Advanced Vivado

Step 16 – Select the RST_0 line and delete it.



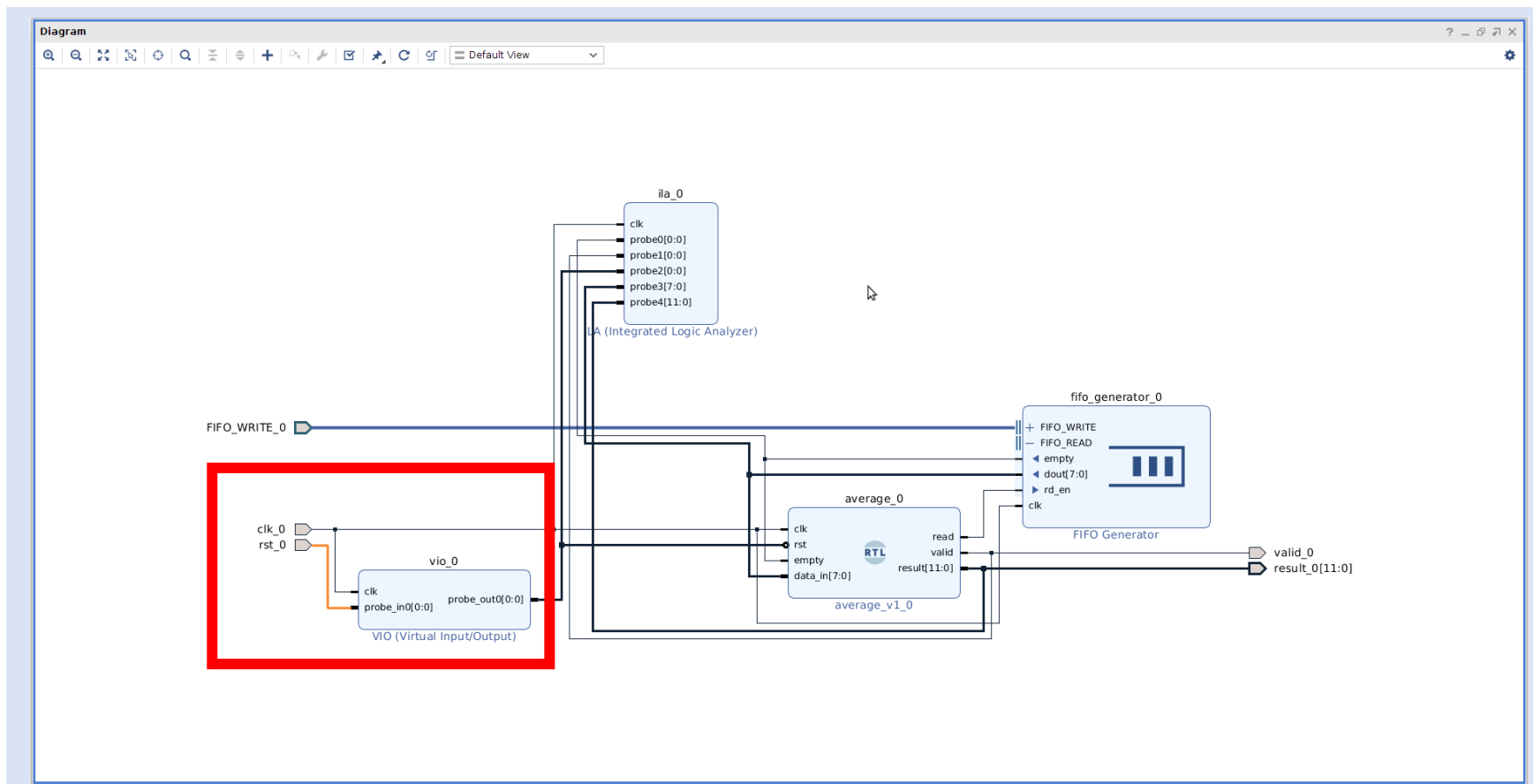
Lab 3: Advanced Vivado

Step 17 – Connect the VIO probe output to the RST and ILA.



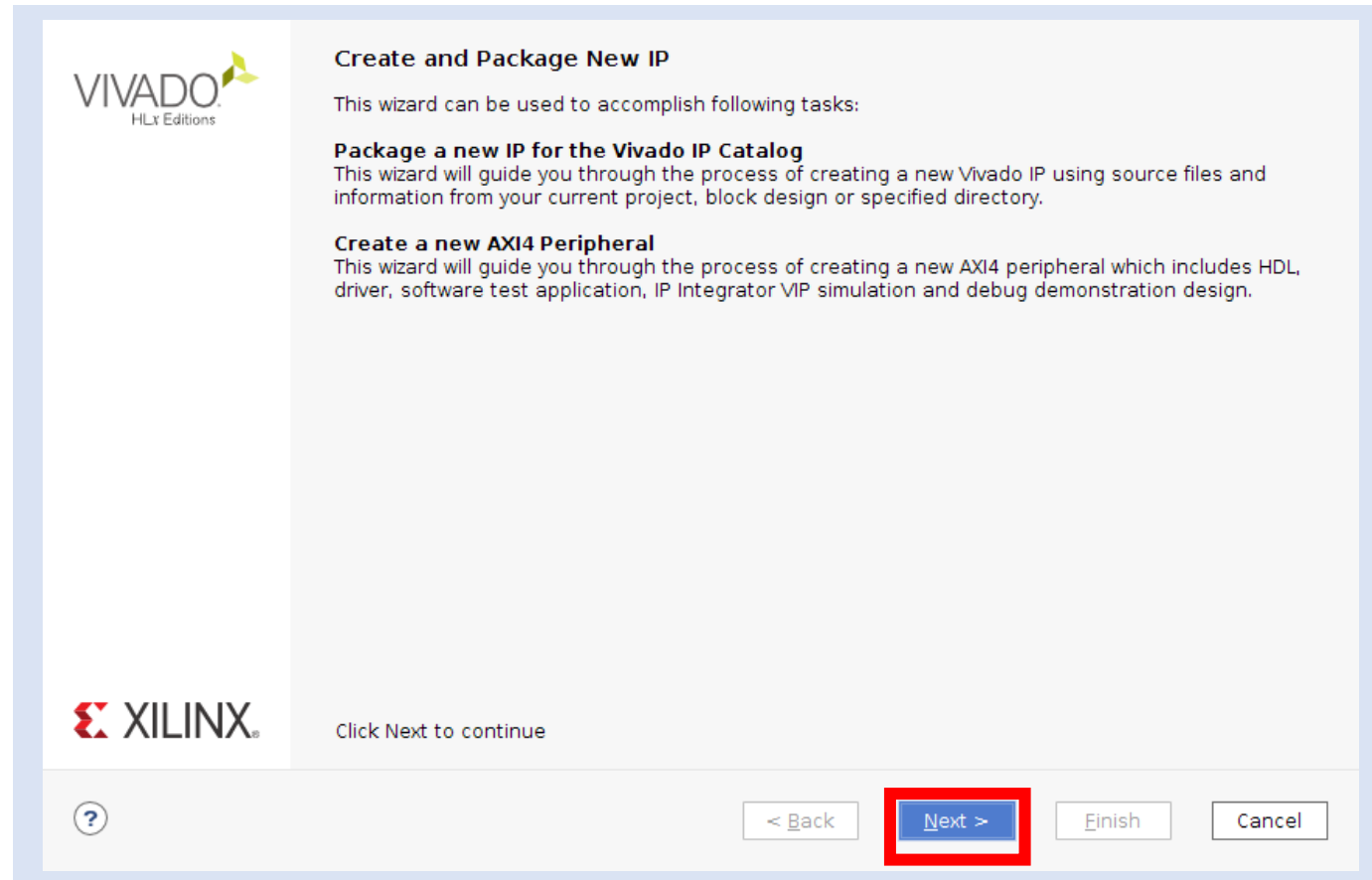
Lab 3: Advanced Vivado

Step 18 – Connect the RST_0 input to the VIO Probe in.



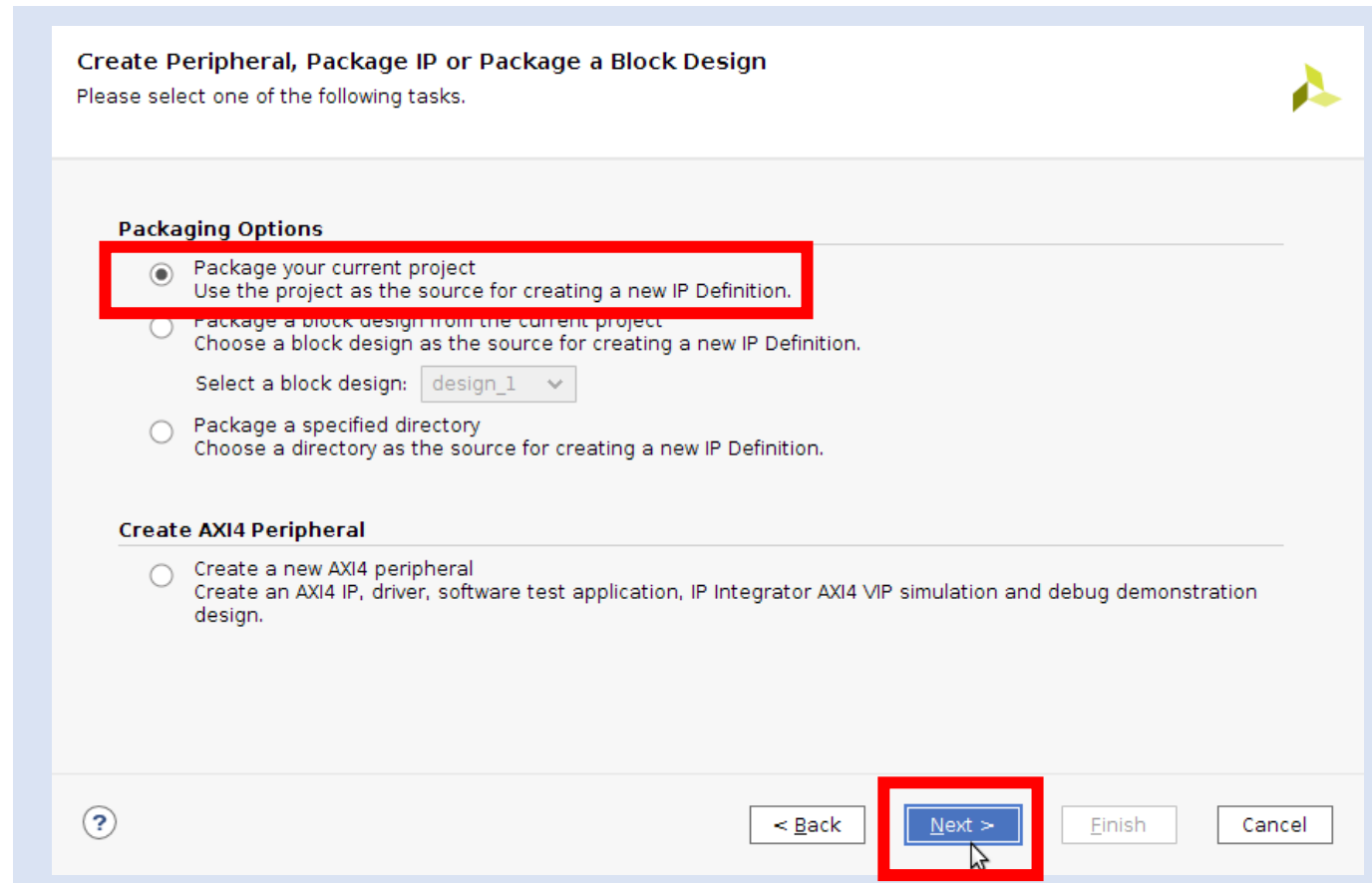
Lab 3: Advanced Vivado

Step 19 – From the Menu bar, select **Tools** → **Create and Package IP**. Select **Next** when the dialog opens.



Lab 3: Advanced Vivado

Step 20 – Select **Package your current project and then **Next**.**



Create Peripheral, Package IP or Package a Block Design
Please select one of the following tasks.

Packaging Options

- ☒ Package your current project
Use the project as the source for creating a new IP Definition.
- ☐ Package a block design from the current project
Choose a block design as the source for creating a new IP Definition.
Select a block design: design_1 ▾
- ☐ Package a specified directory
Choose a directory as the source for creating a new IP Definition.

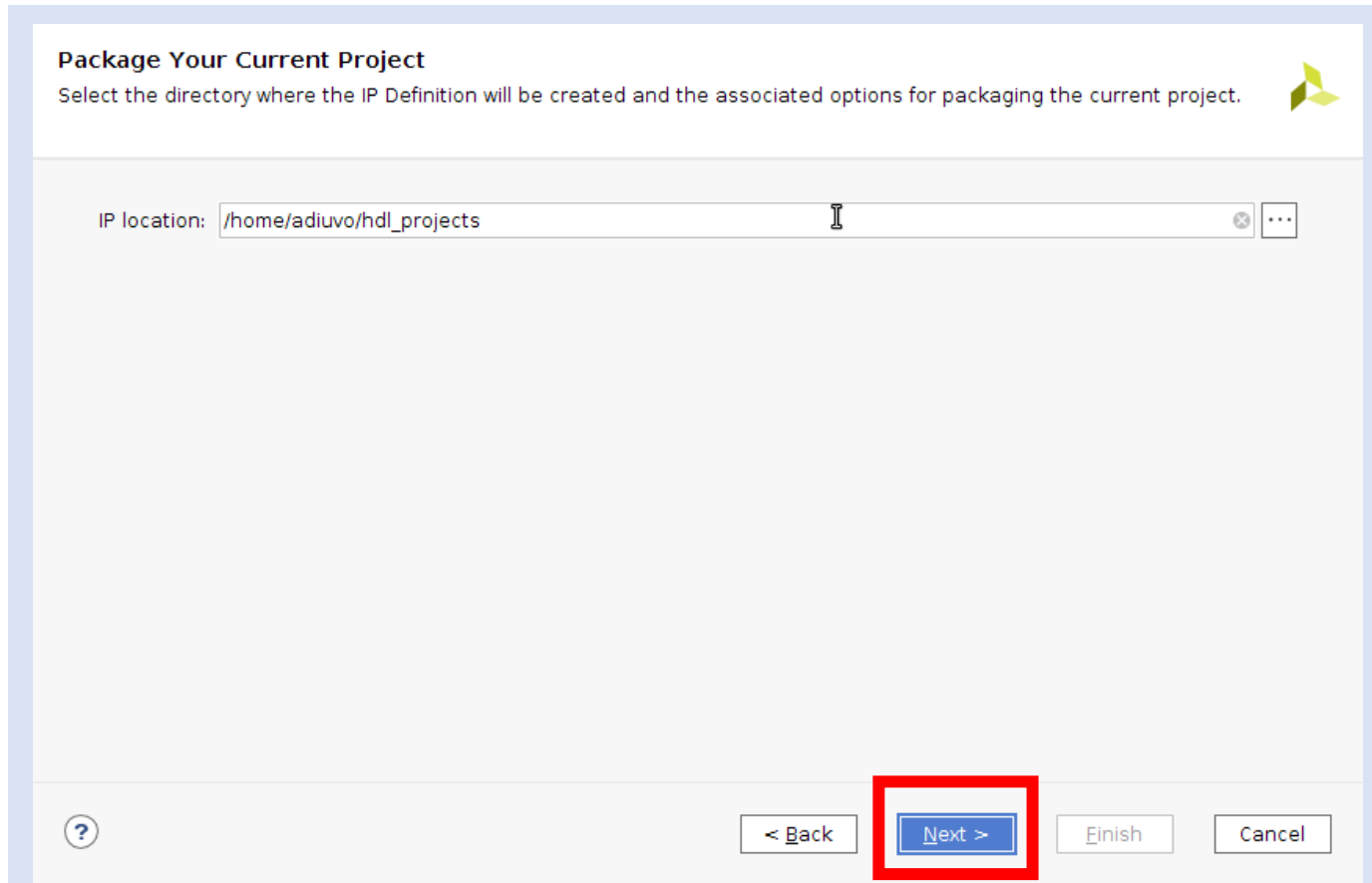
Create AXI4 Peripheral

- ☐ Create a new AXI4 peripheral
Create an AXI4 IP, driver, software test application, IP Integrator AXI4 VIP simulation and debug demonstration design.

? < Back Next > Finish Cancel

Lab 3: Advanced Vivado

Step 21 – Select the location the IP should be saved in and click **Next**.



The image shows the 'Package Your Current Project' dialog box in Vivado. The title bar is light blue. The main area has a light gray background. At the top, the title 'Package Your Current Project' is in bold, followed by the instruction 'Select the directory where the IP Definition will be created and the associated options for packaging the current project.' and the Vivado logo. Below this is a text field labeled 'IP location:' containing the path '/home/adiuvo/hdl_projects'. To the right of the text field are a close button (X) and a browse button (three dots). At the bottom, there is a row of buttons: a help button (question mark in a circle), a '< Back' button, a 'Next >' button (highlighted with a red rectangle), an 'Finish' button, and a 'Cancel' button.

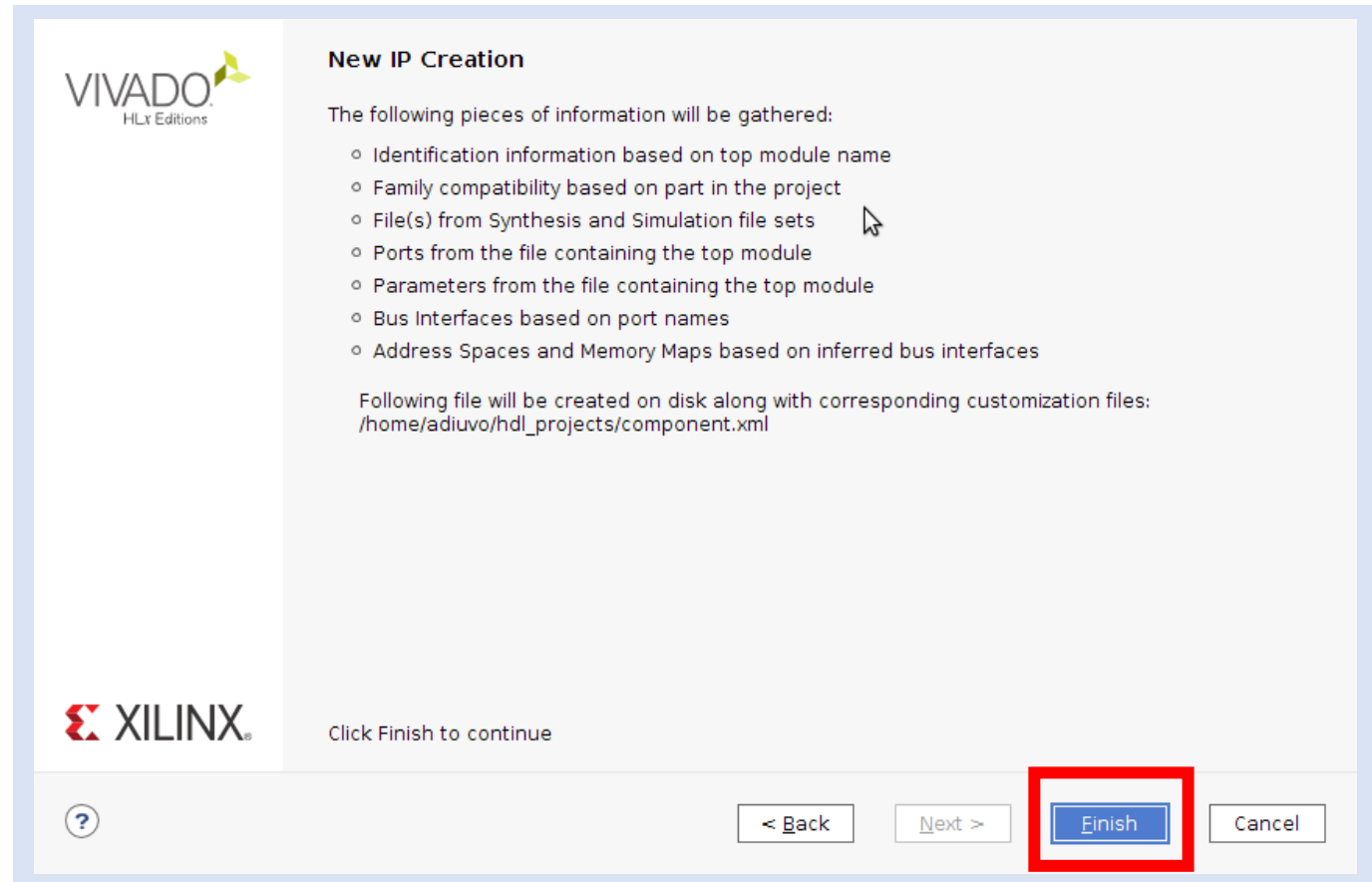
Package Your Current Project
Select the directory where the IP Definition will be created and the associated options for packaging the current project.

IP location: /home/adiuvo/hdl_projects

? < Back Next > Finish Cancel

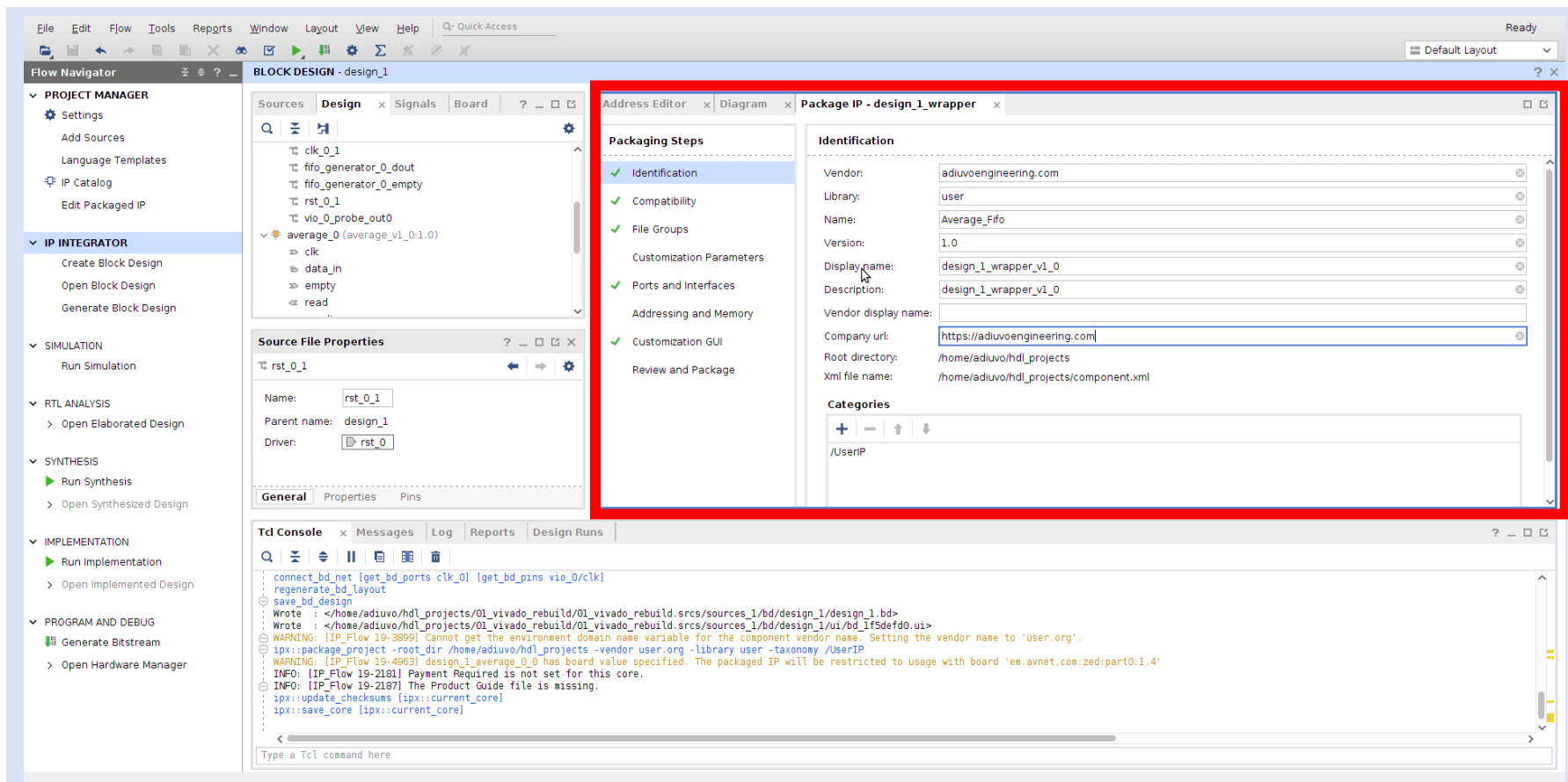
Lab 3: Advanced Vivado

Step 22 – Click on Finish.



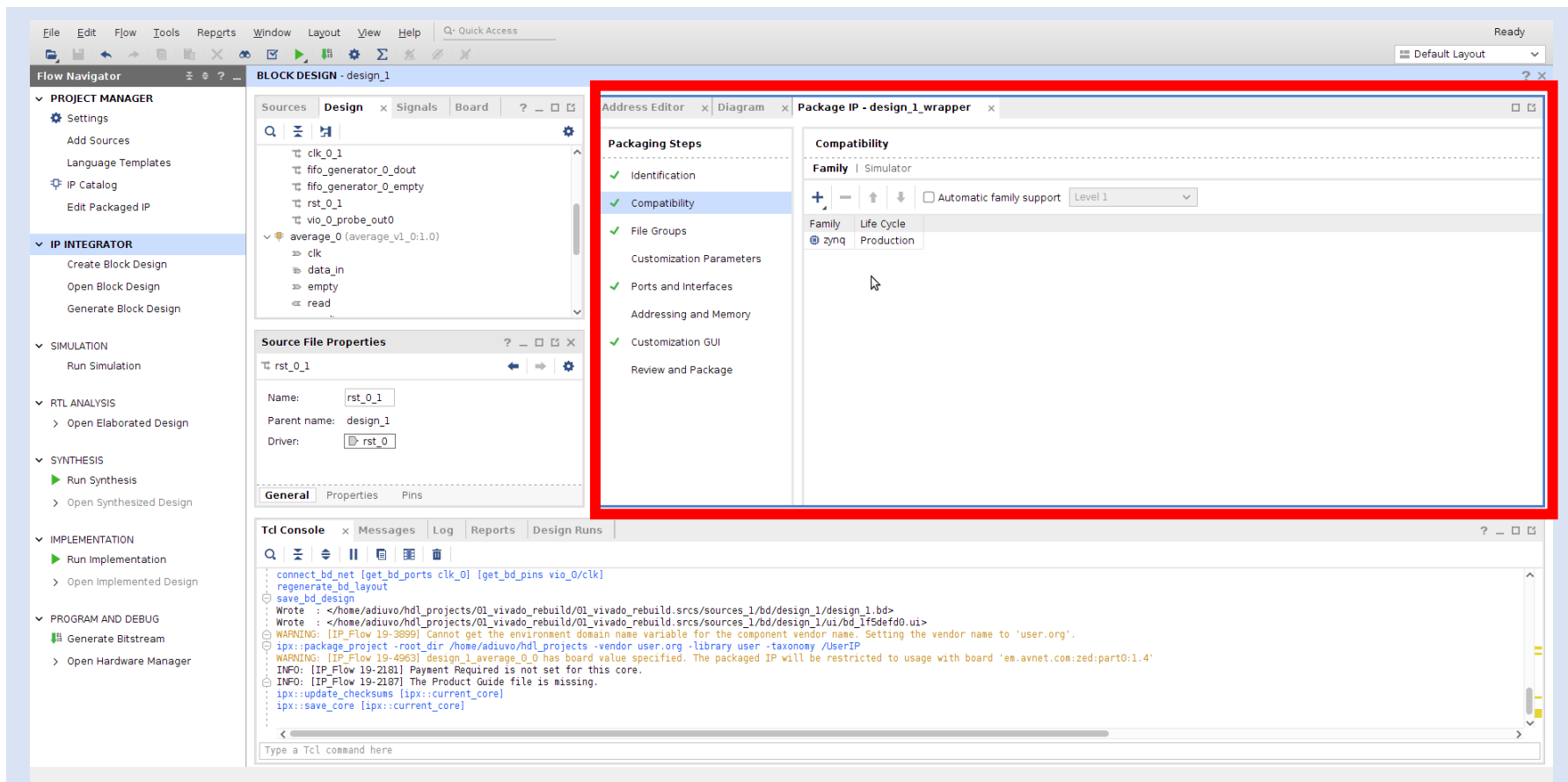
Lab 3: Advanced Vivado

Step 23 – This will open a package view in the project. Enter **Name**, **Version** and **Company URL**.



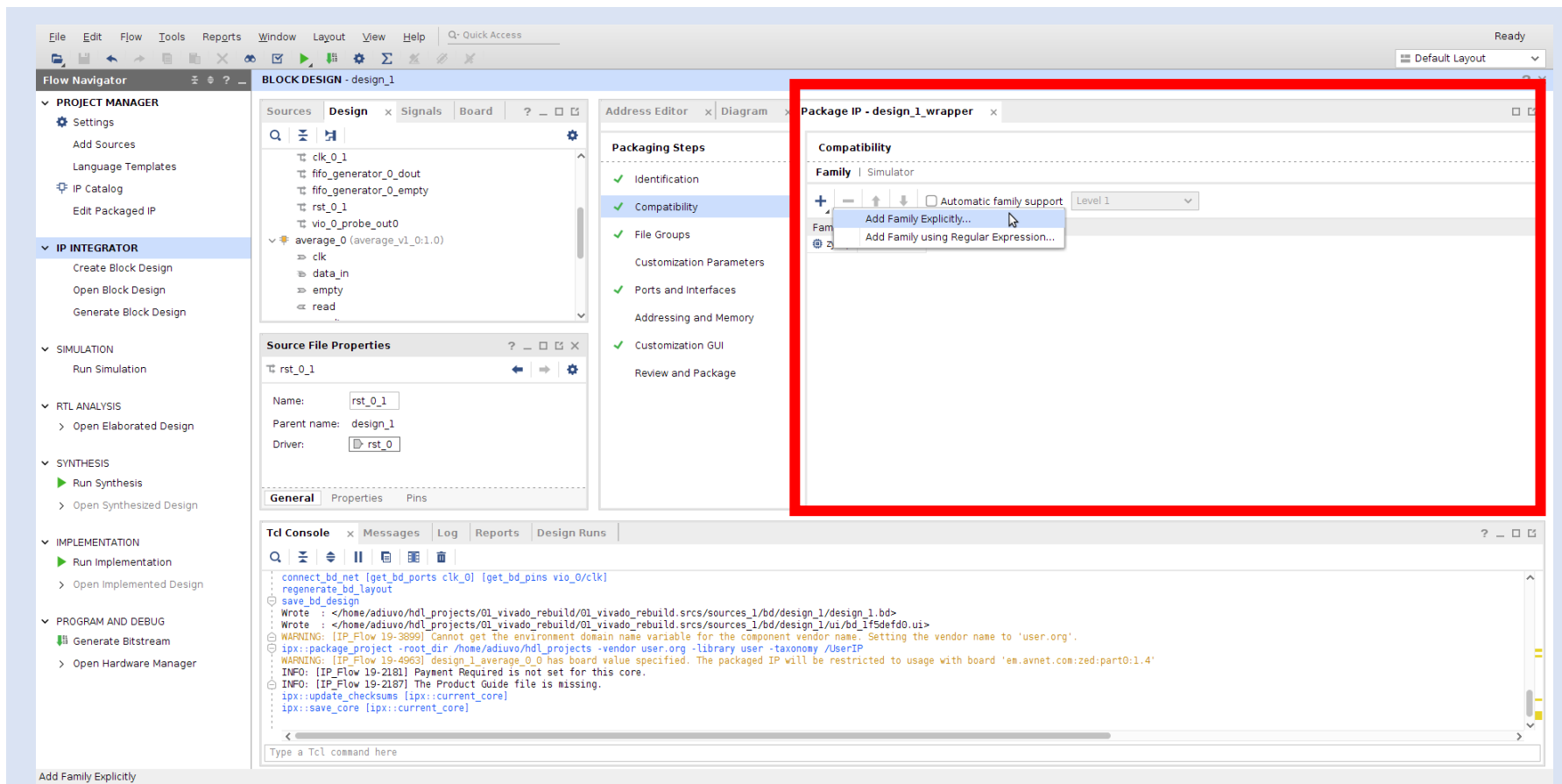
Lab 3: Advanced Vivado

Step 24 – Click on the **Compatibility** tab. This defines what FPGA / SoC the core will work with.



Lab 3: Advanced Vivado

Step 25 – Click on + and select Add Family Explicitly.



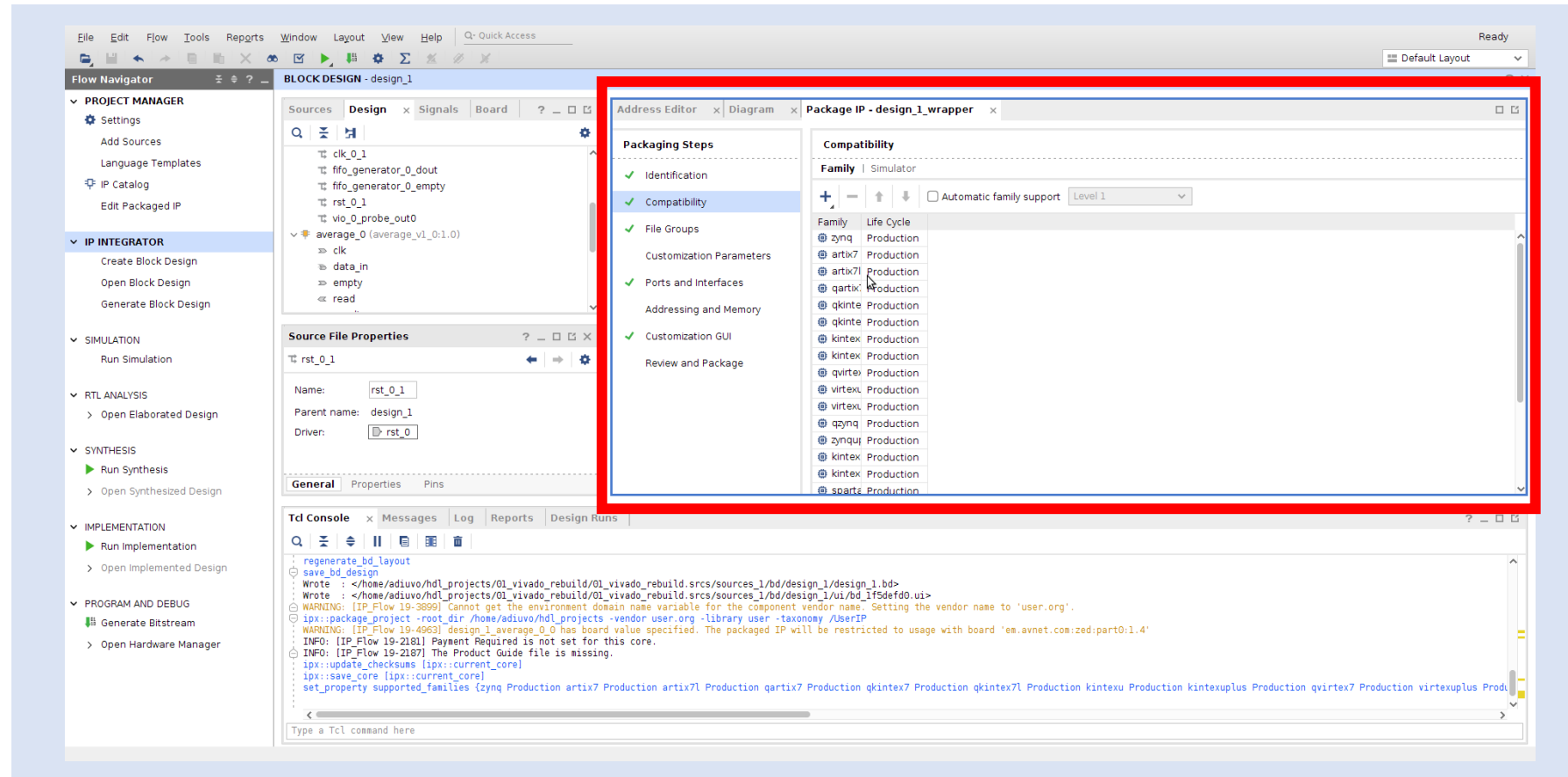
Lab 3: Advanced Vivado

Step 26 – In the resultant dialog, select **All Families** and **Parts** and **Production** from the Life-cycle.



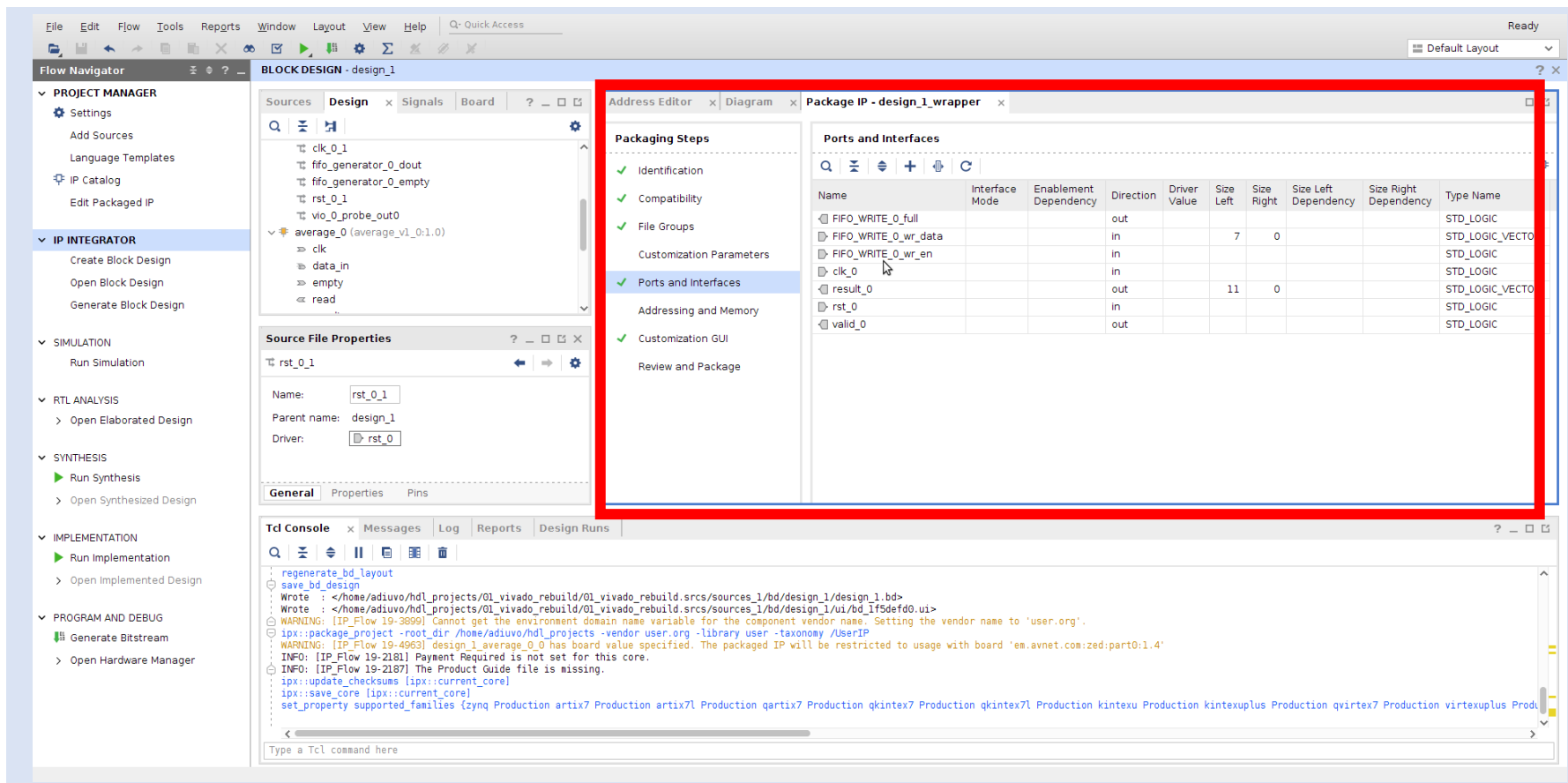
Lab 3: Advanced Vivado

Step 27 – This will make the IP core available to all families and devices.



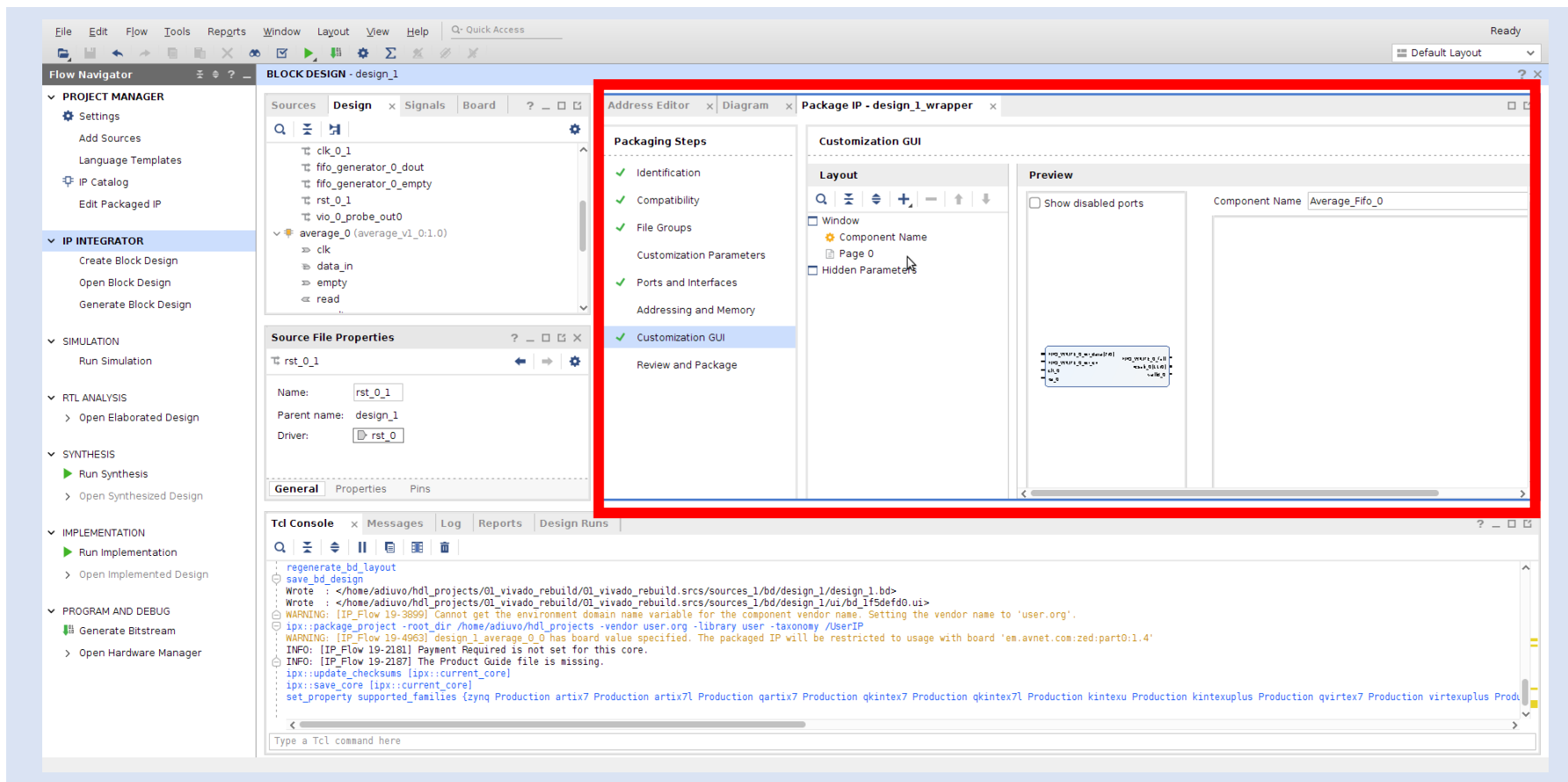
Lab 3: Advanced Vivado

Step 28 – Click on Ports and Interfaces. This should show all the blocks' inputs and outputs.



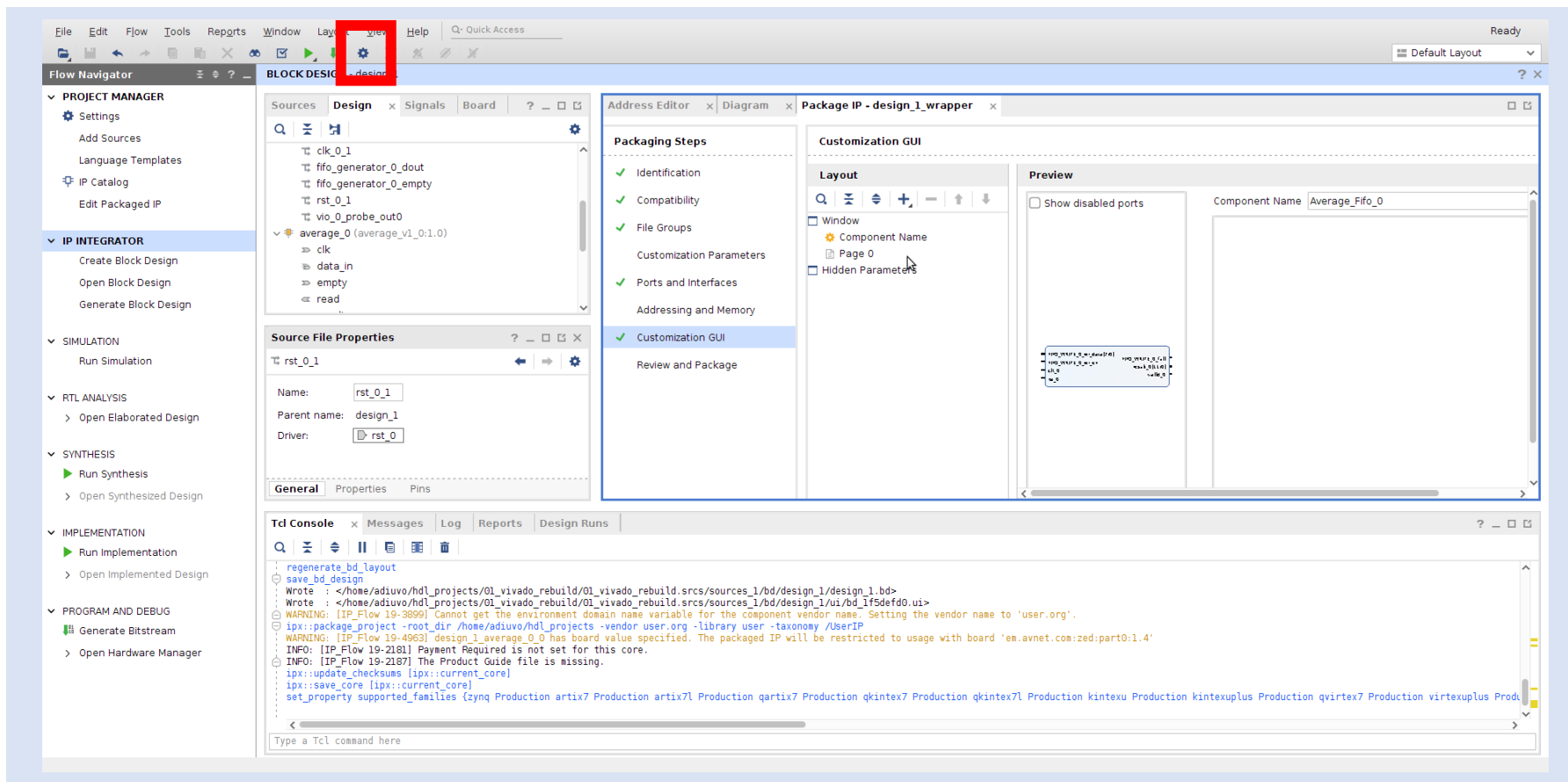
Lab 3: Advanced Vivado

Step 29 – Click on **Customization**. This shows the symbol.



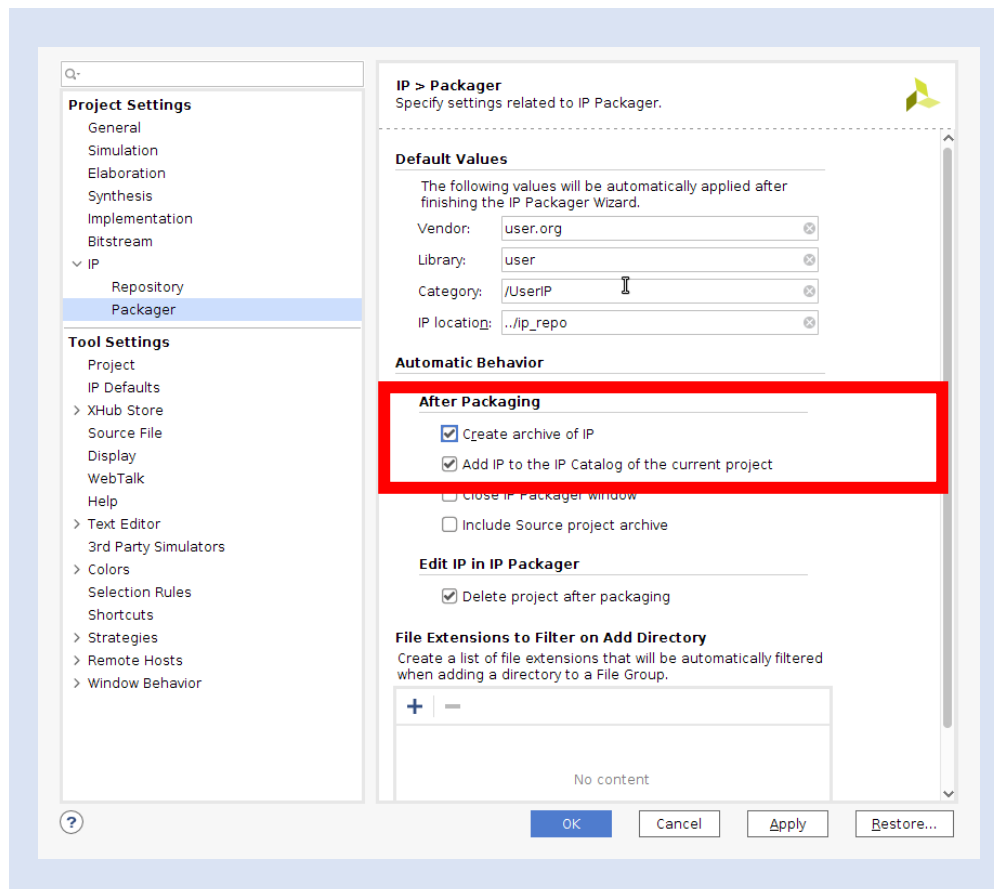
Lab 3: Advanced Vivado

Step 30 – Click on Settings.



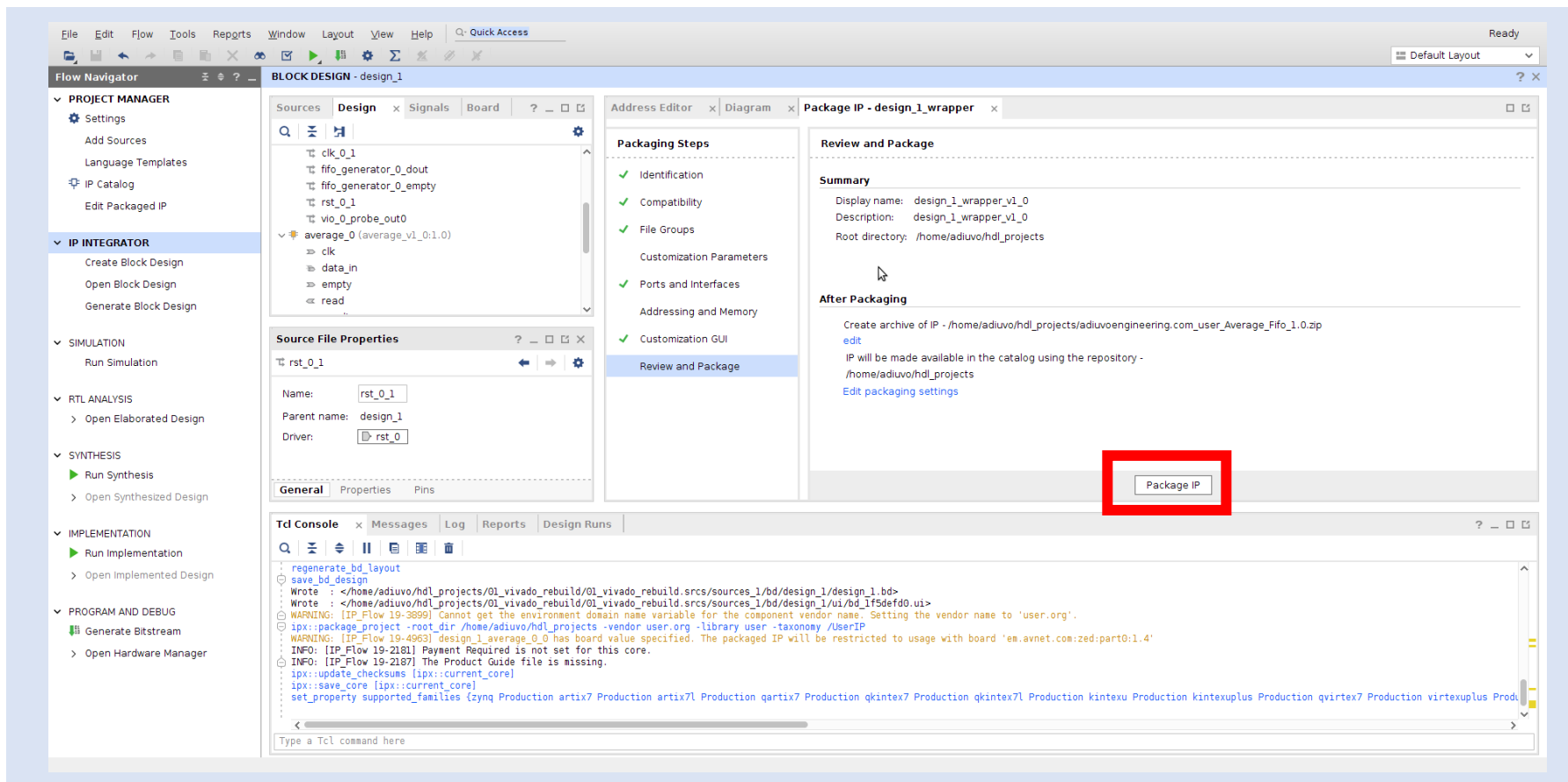
Lab 3: Advanced Vivado

Step 31 – Select Create archive of IP and click OK.



Lab 3: Advanced Vivado

Step 32 – Click on Review and Package and then Package IP.



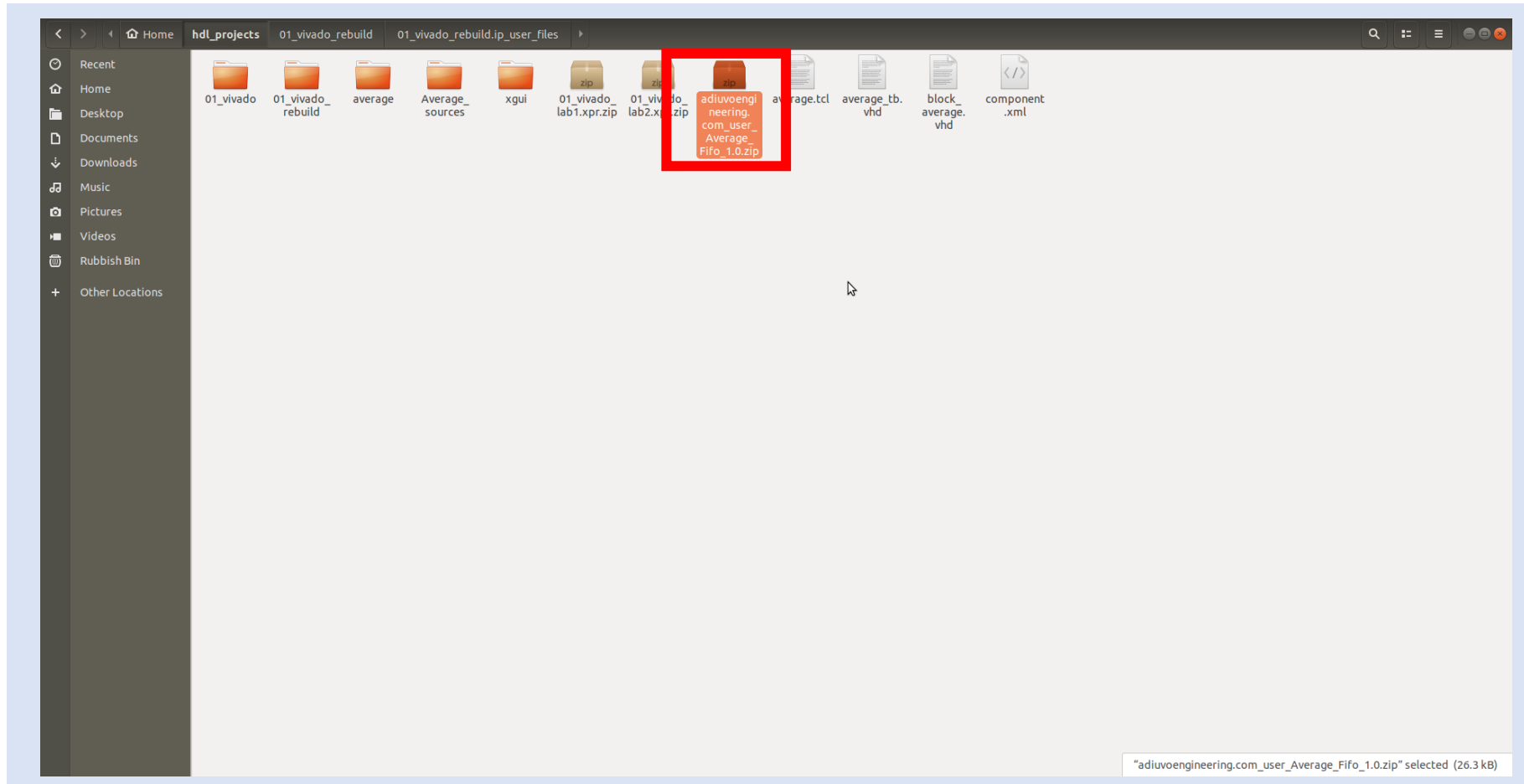
Lab 3: Advanced Vivado

Step 33 – This should show the message below. Click **OK**.



Lab 3: Advanced Vivado

Step 34 – You will see a ZIP file of the component in the directory you identified to save the IP in.



Lab 3: Advanced Vivado

Step 35 – Close the project and create a new Vivado project. In the wizard, click **Next**, then enter the **name and location** and click **Next** again.

Create a New Vivado Project

This wizard will guide you through the creation of a new project.

To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

☒ Create project subdirectory

< Back **Next >** Finish Cancel

Lab 3: Advanced Vivado

Step 36 – Select RTL Project and Next, followed by Next again.

Project Type
Specify the type of project to create.

- ☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☐ Do not specify sources at this time
- ☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time
- ☐ **J/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.
- ☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.
- ☐ **Example Project**
Create a new Vivado project from a predefined template.

Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Use Add Files, Add Directories or Create File buttons below

☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories

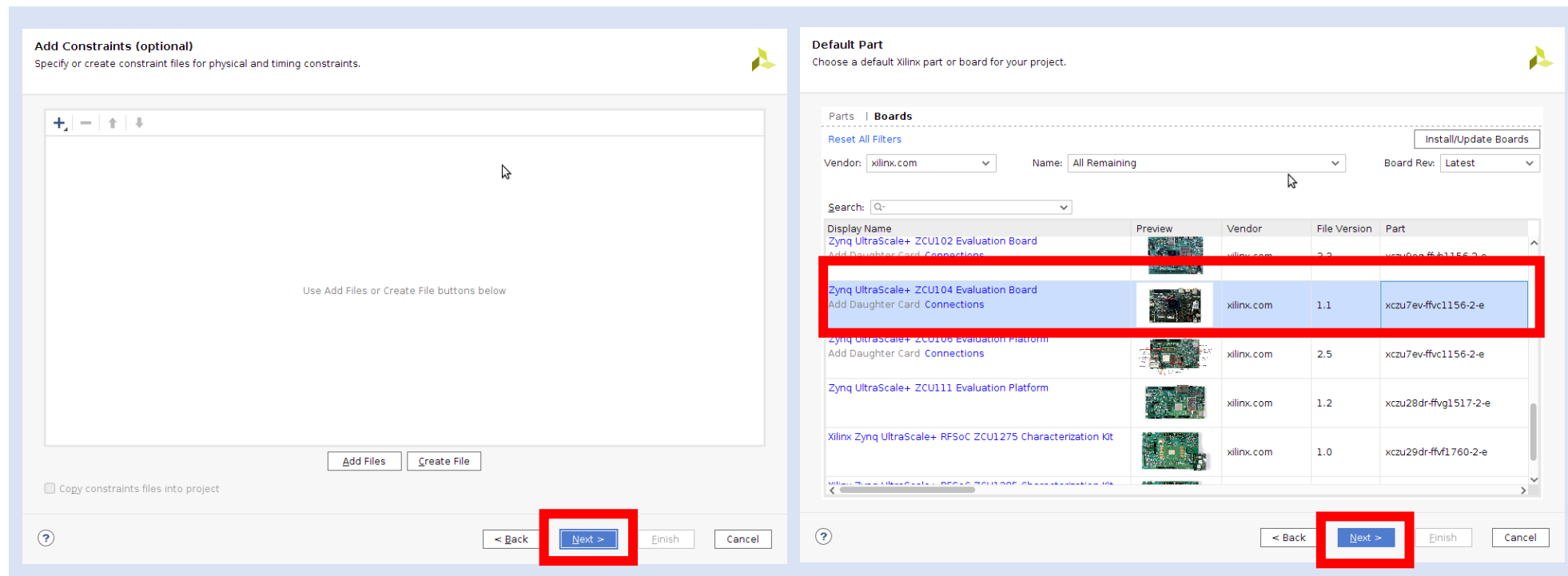
Target language: VHDL Simulator language: Mixed

Project Type Tab Navigation: ? < Back **Next >** Finish Cancel

Add Sources Tab Navigation: ? < Back **Next >** Finish Cancel

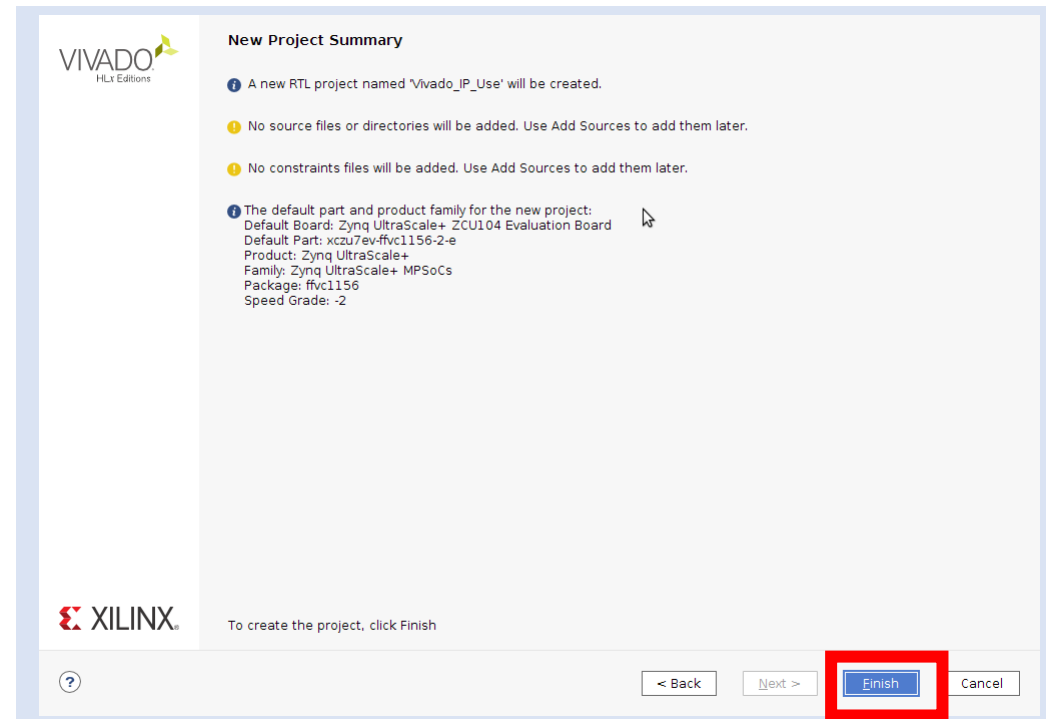
Lab 3: Advanced Vivado

Step 37 – Click **Next** on the Constraints tab. On the Default Part, select the **ZCU104 board** and click **Next**.



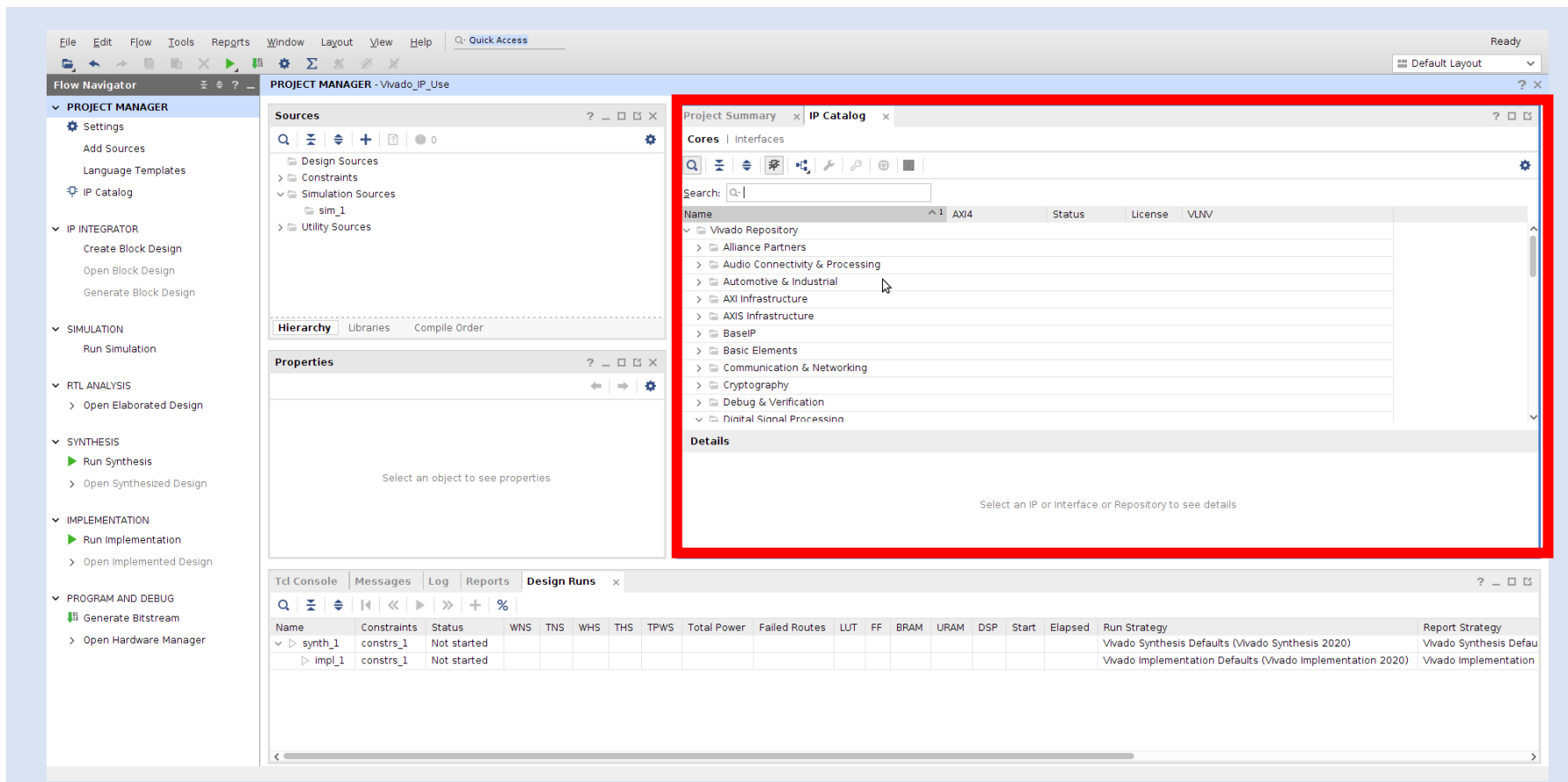
Lab 3: Advanced Vivado

Step 38 – On the final page of the Project Summary, click **OK**.



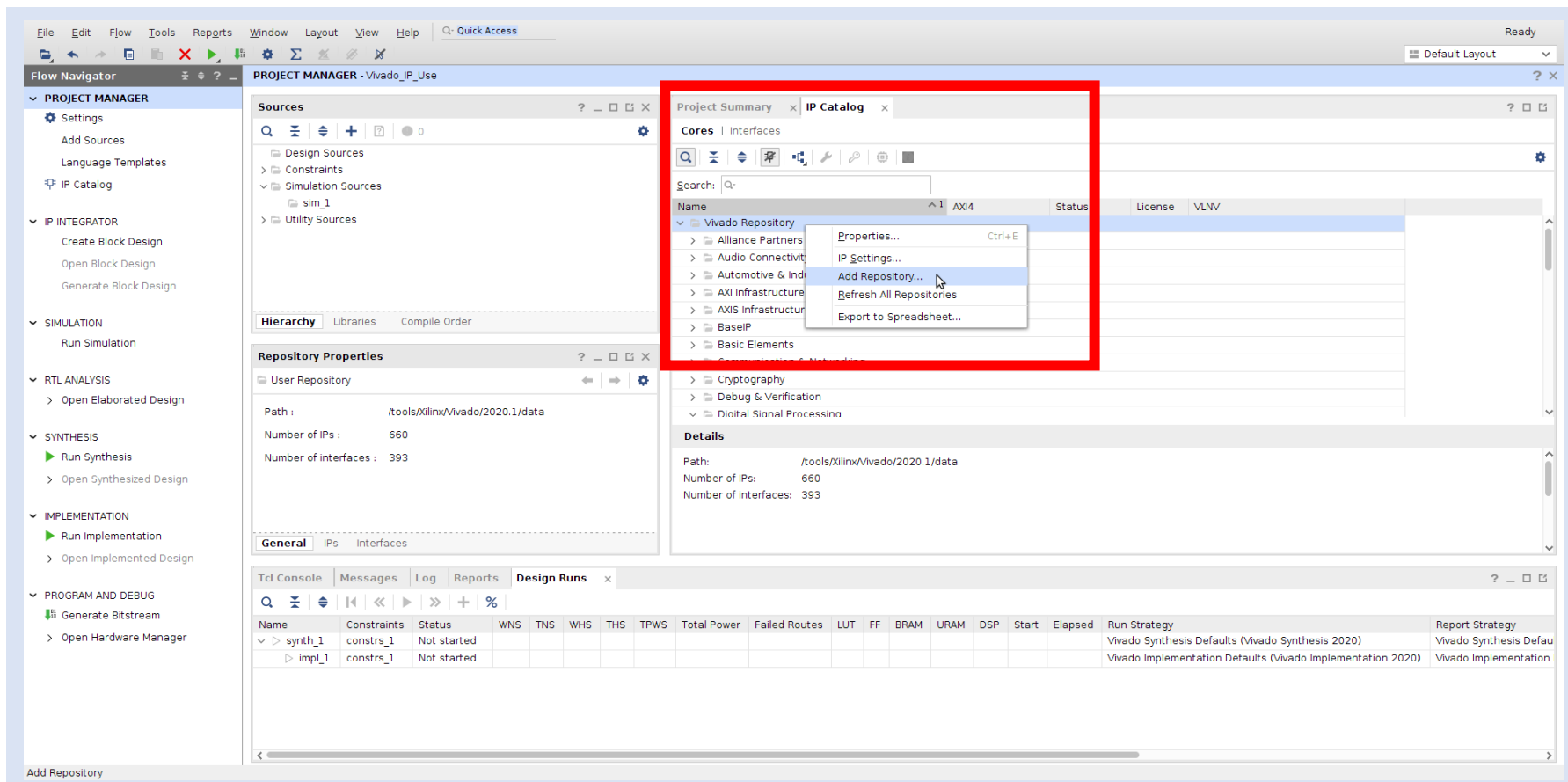
Lab 3: Advanced Vivado

Step 39 – From the menu bar, select **Window** → **IP Catalog**.



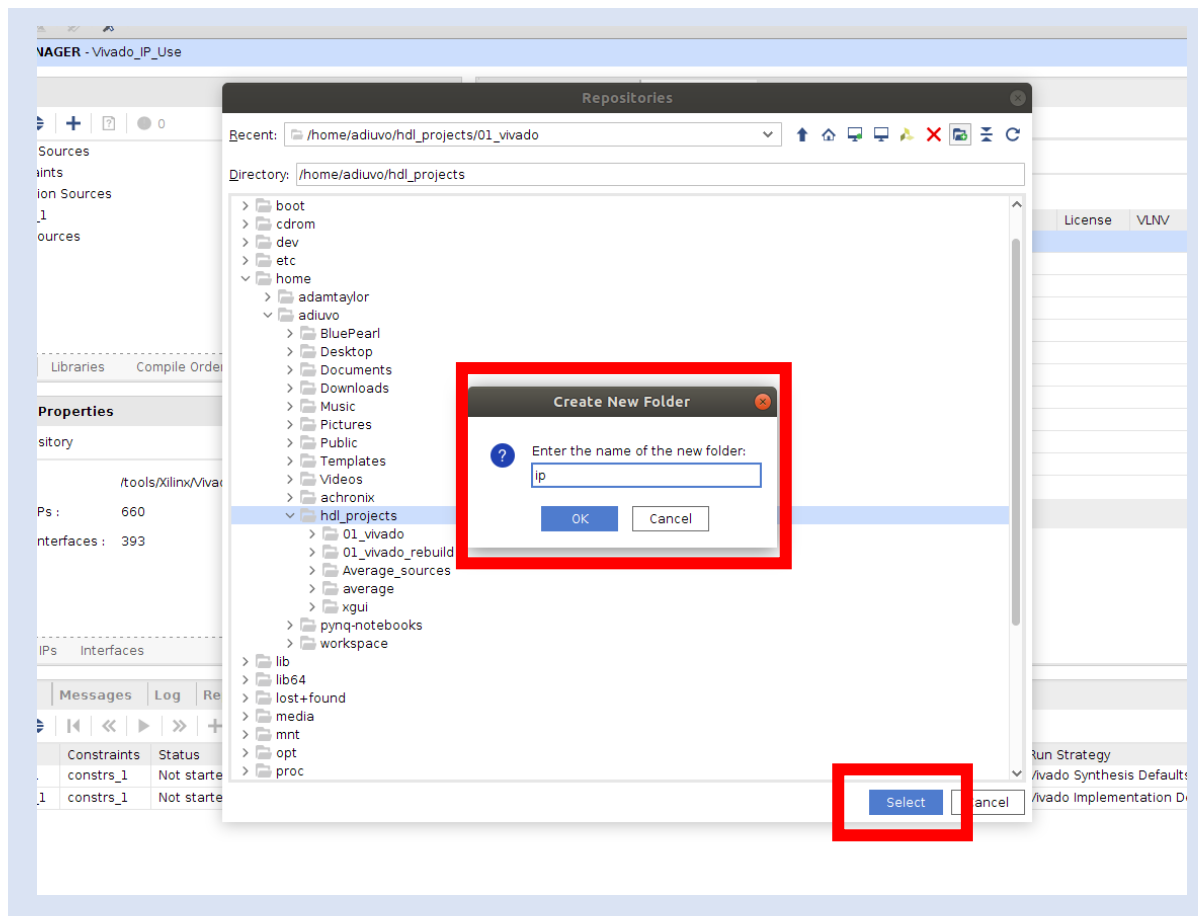
Lab 3: Advanced Vivado

Step 40 – Right click on the Vivado Repository and select Add Repository.



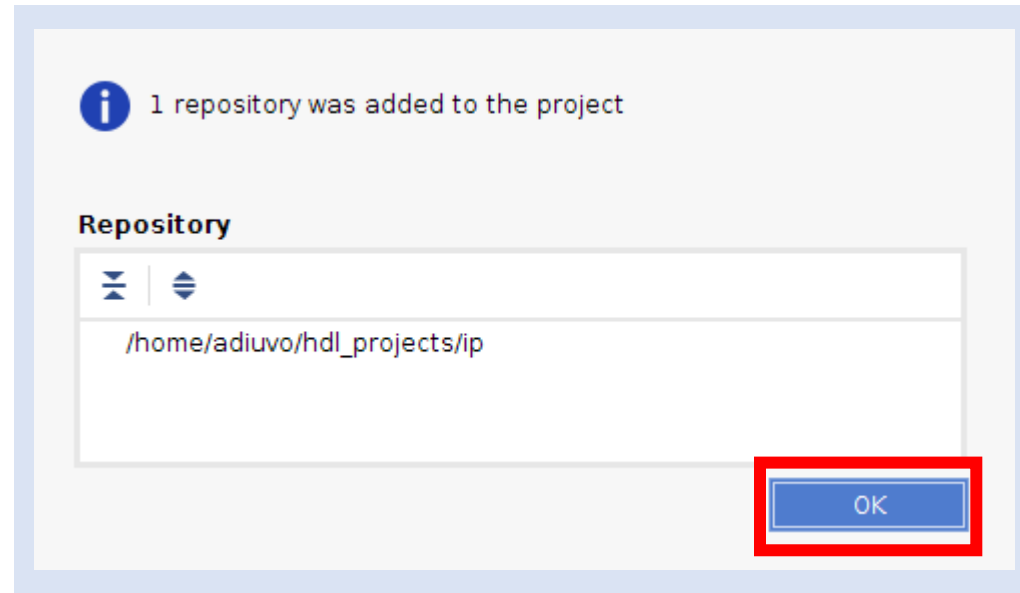
Lab 3: Advanced Vivado

Step 41 – In the open dialog, select **Create New Folder** and name it **IP** and click **Select**.



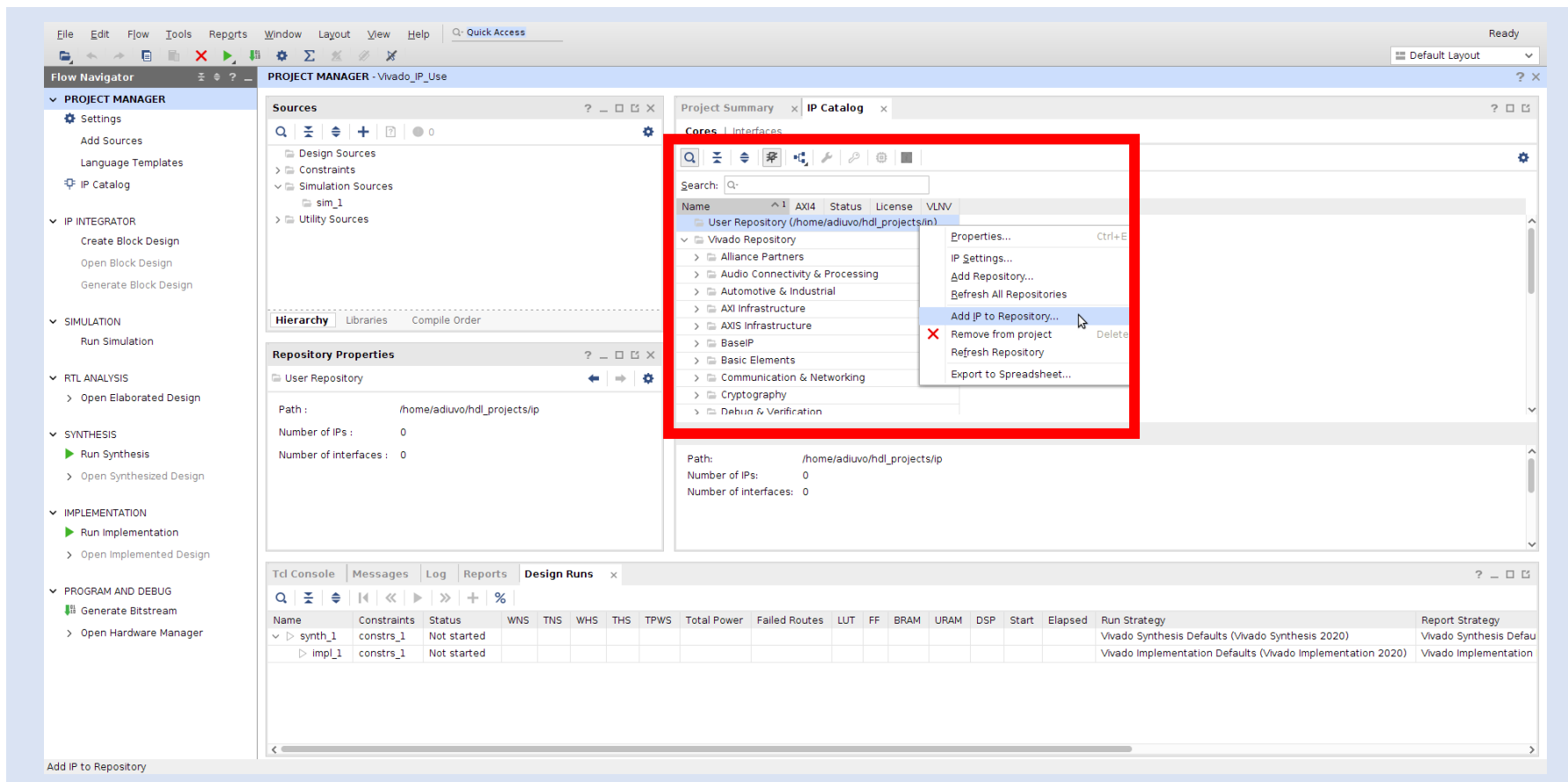
Lab 3: Advanced Vivado

Step 42 – This will show a dialog indicating that one repository was added.



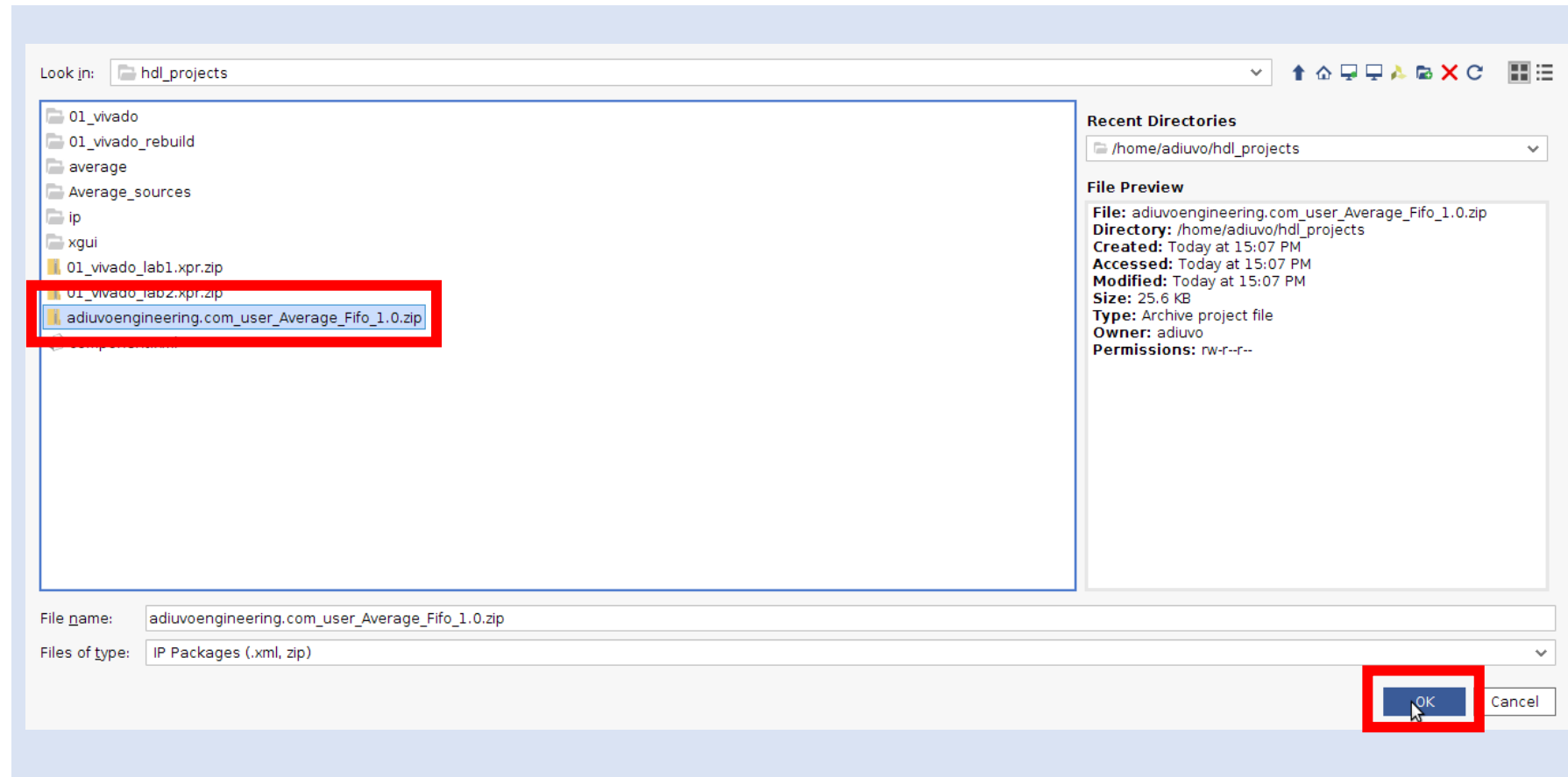
Lab 3: Advanced Vivado

Step 43 – This will add in the repository. Right click on it and select **Add IP to Repository**.



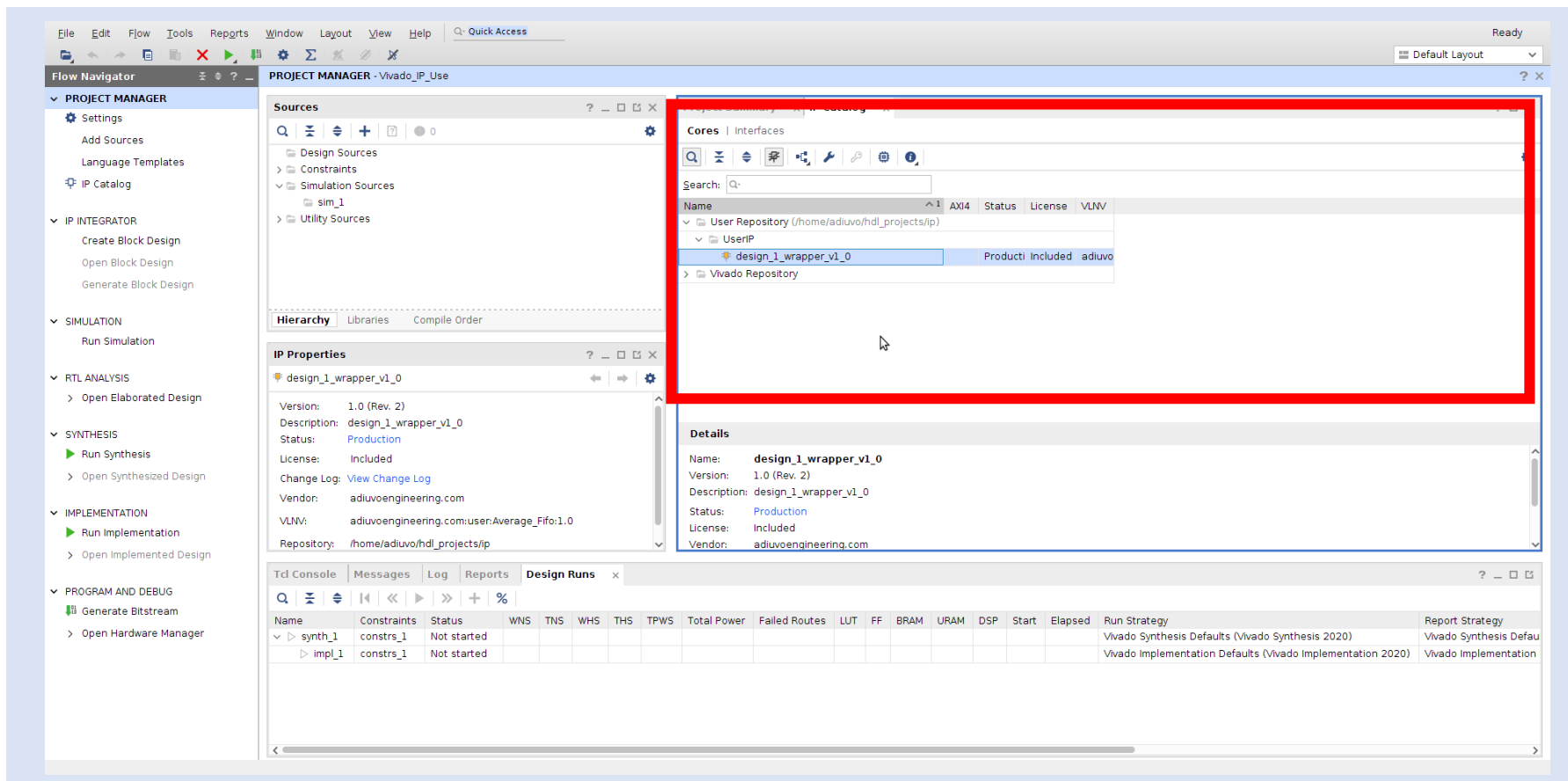
Lab 3: Advanced Vivado

Step 44 – Select the **component ZIP file** in the file dialog and click **OK**.



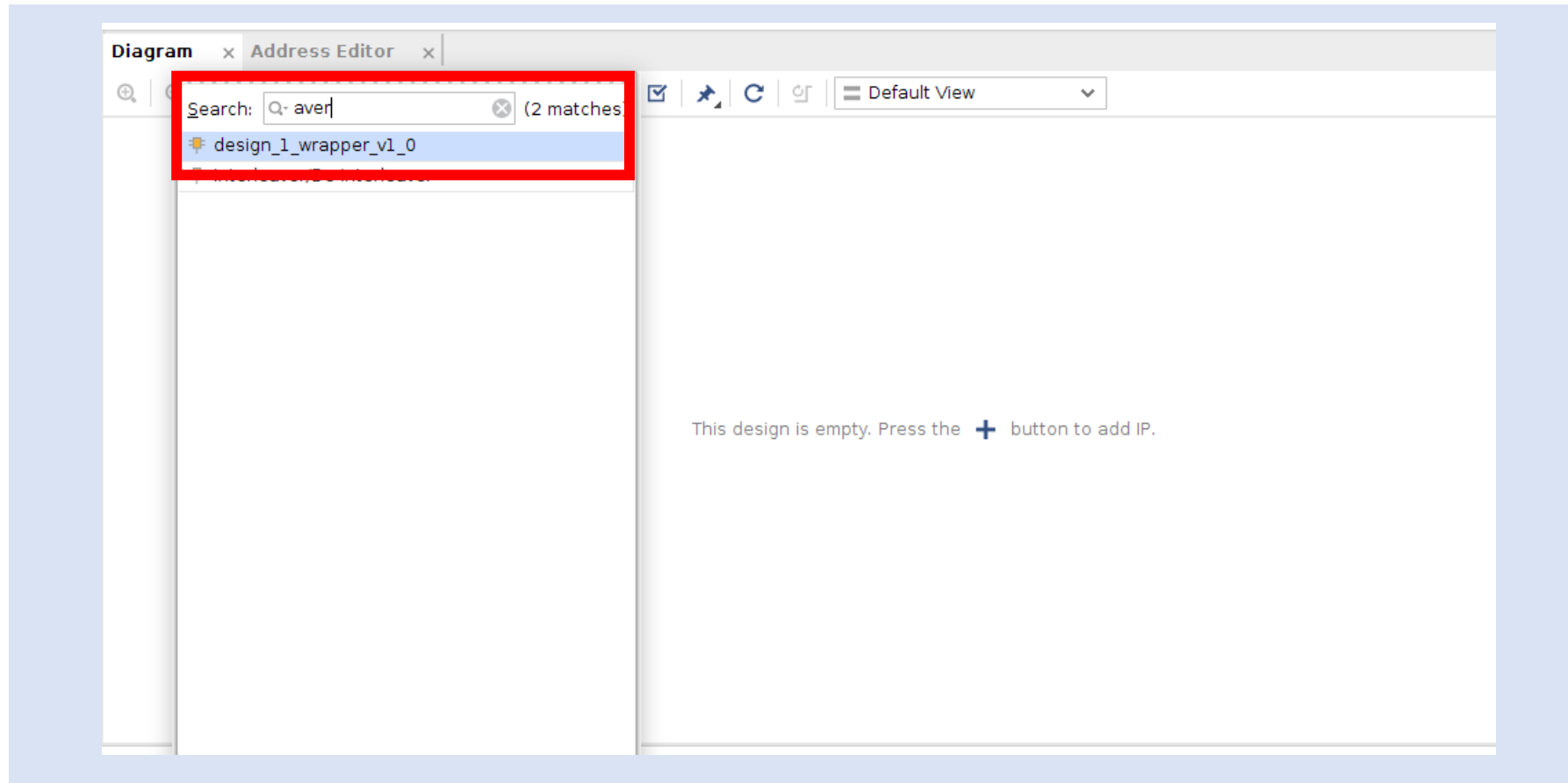
Lab 3: Advanced Vivado

Step 45 – You should now see the IP core in the library ready to go in our new design.



Lab 3: Advanced Vivado

Step 46 – Create a block design and type in the search bar average. Double click on the **design_1_wrapper_V1_0** which comes up.



Lab 3: Advanced Vivado

Step 47 – This will add in the Average block we have created and we are ready to go reusing it in our new developments.

