Getting to Know Vivado

Course Workbook

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About this Workbook

This workbook is designed to be used in conjunction with the Getting to Know Vivado course.

The contents of this workbook are created by Adiuvo Engineering & Training, Ltd.

If you have any questions about the contents or need assistance, please contact Adam Taylor at adam@adiuvoengineering.com.

Pre-Lab

Workshop Pre-requisites

Required Hardware

There is no required hardware for this course.

Downloads and Installations

Step 1 – Download and install the following at least one day prior to the workshop. This may take a significant amount of time and drive space.

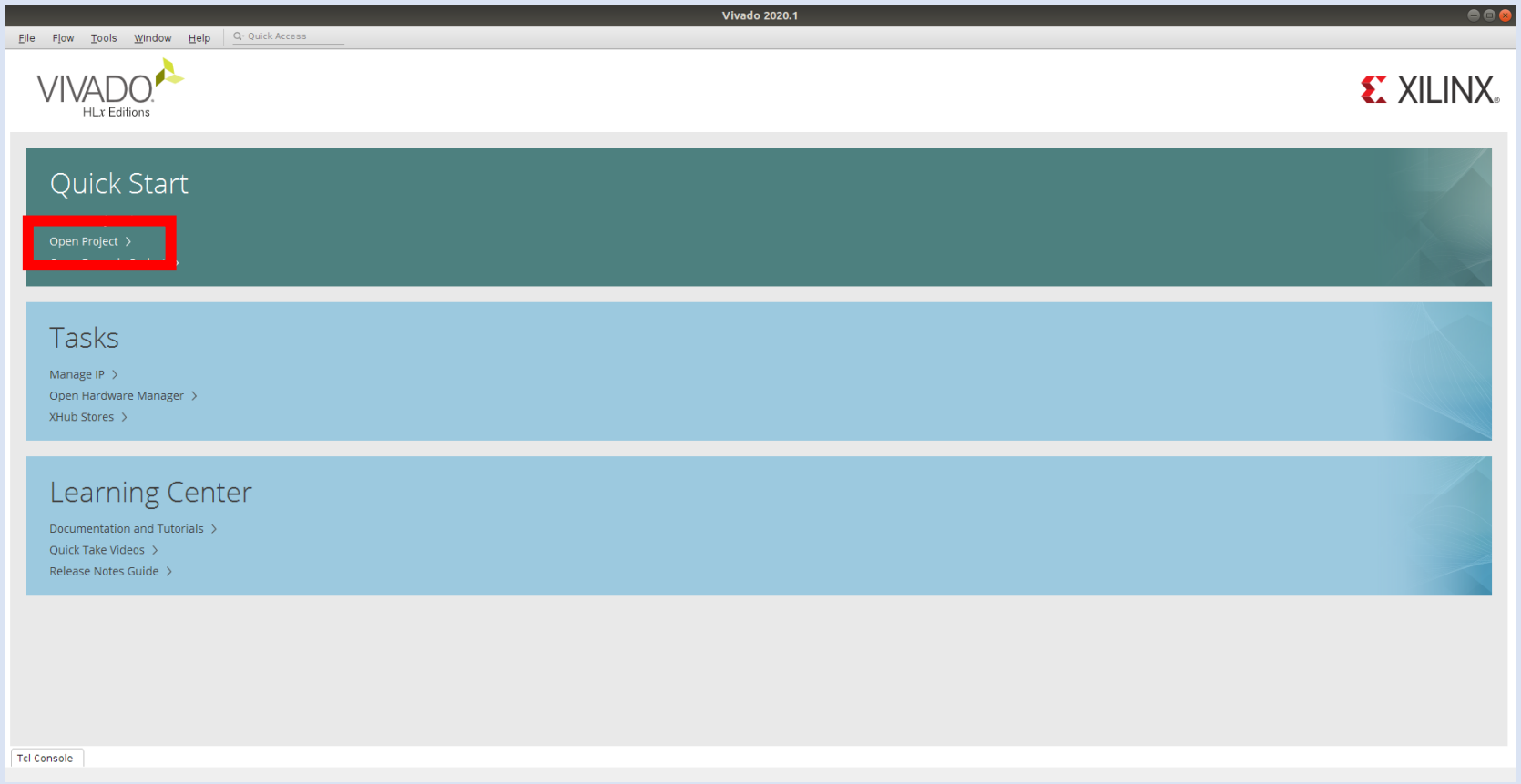
Vivado 2020.1	Download
Source Project Files	Download
Lab 1 must be completed	

Lab 2

Intermediate Vivado

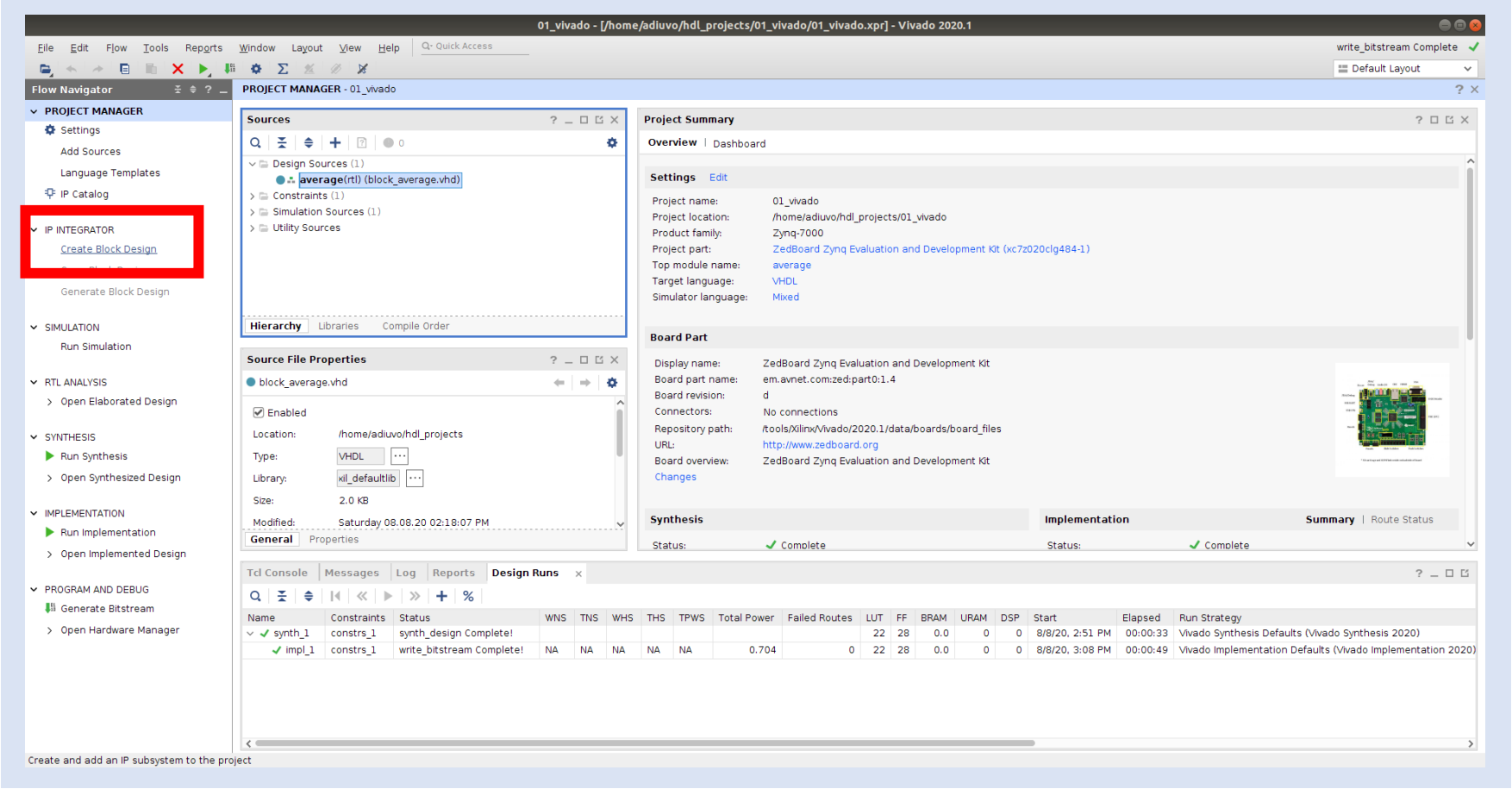
Lab 2: Intermediate Vivado

Step 1 – Open the project created in part one.



Lab 2: Intermediate Vivado

Step 2 – This will open in project management view. Click on **Create Block Diagram**.



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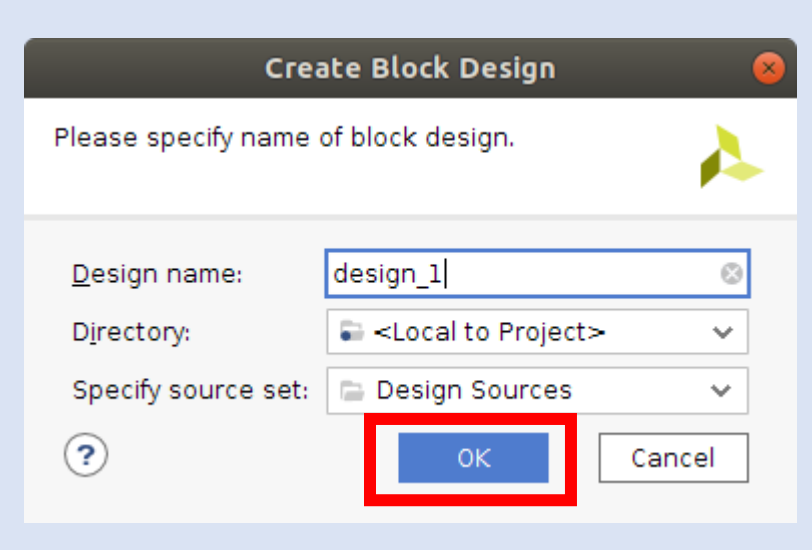
Step 3 – Leave the predefined name and locations unchanged and click **OK**.



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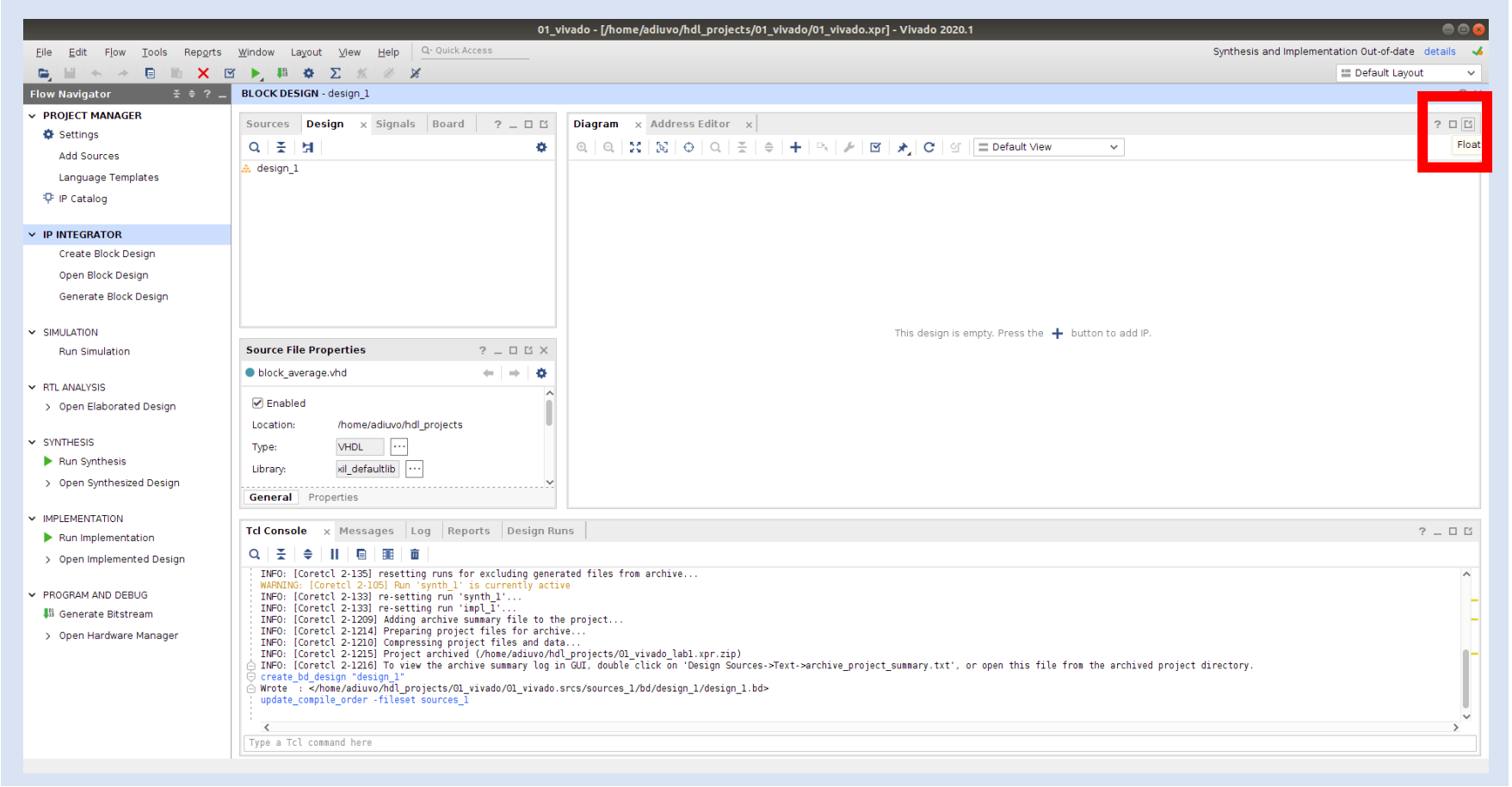
Step 4 – Undock the block diagram window and maximize it.



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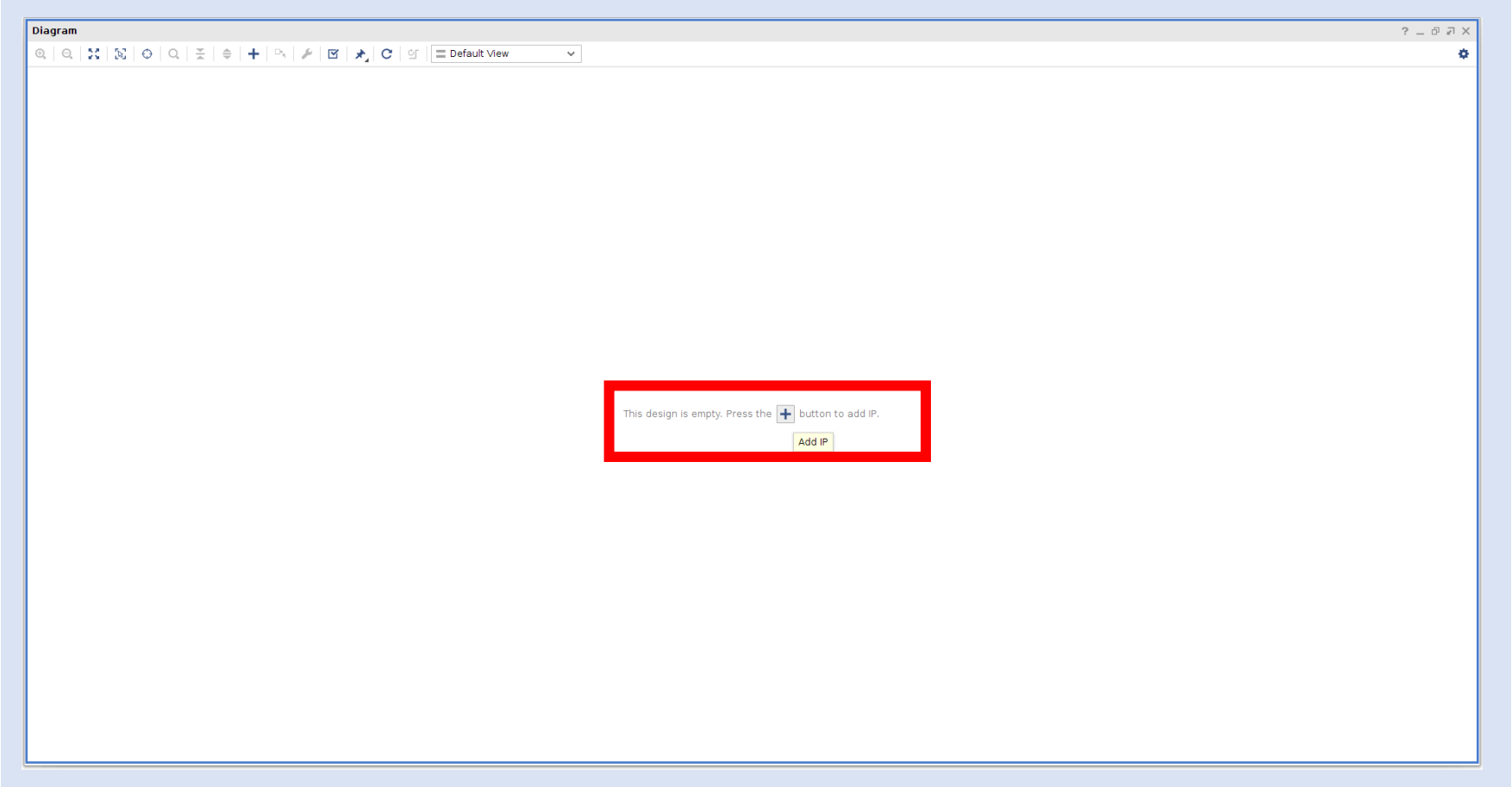
Step 5 – We are going to add in new IP. Click on the **+ button**.



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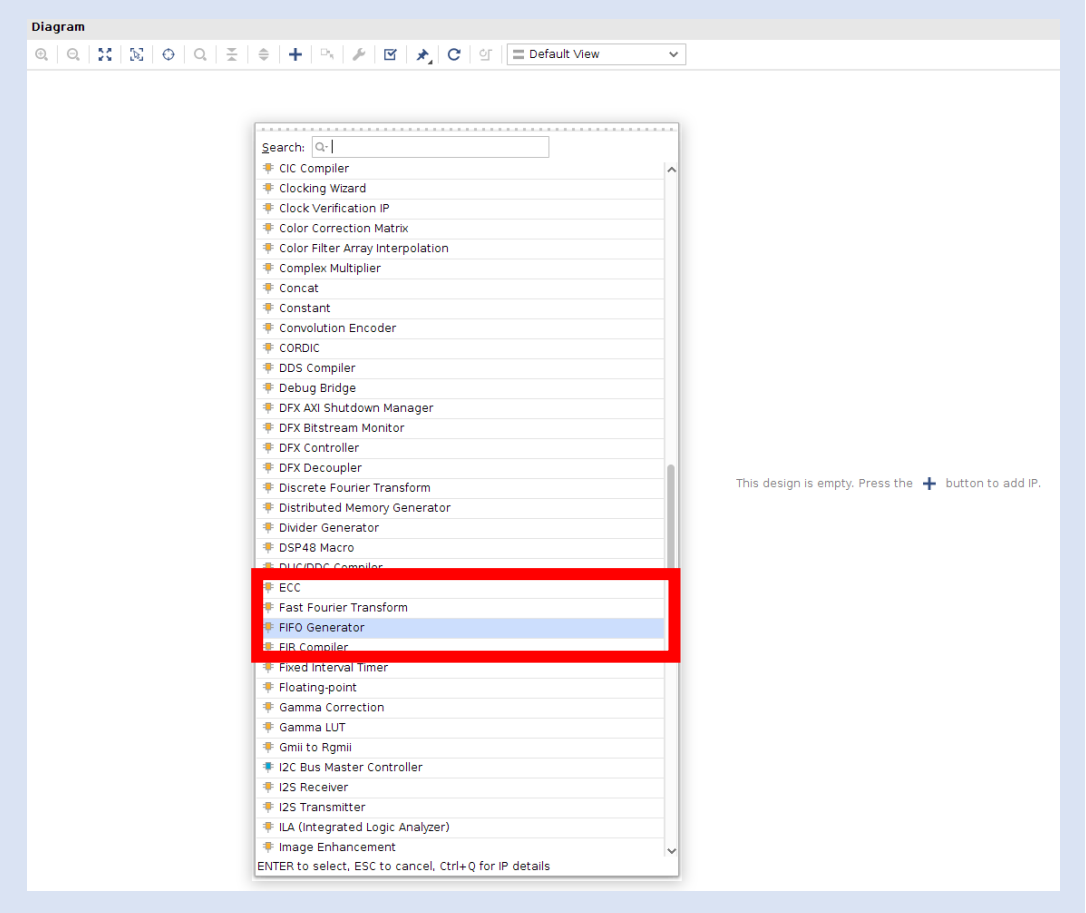
Step 6 – Select the **FIFO Generator**. This will add a FIFO to the block diagram.



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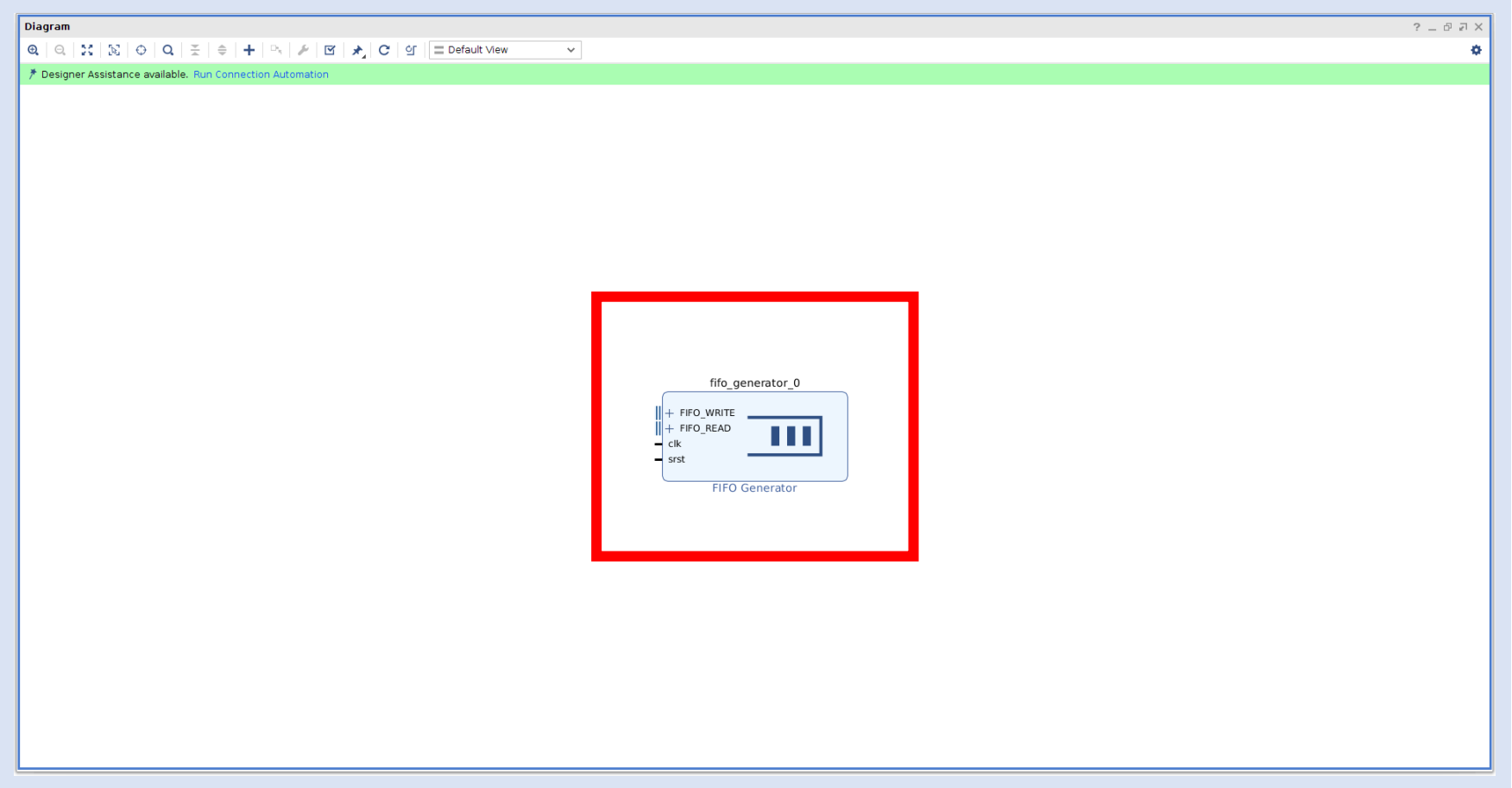
Step 7 – Double click on the **FIFO Generator** to customize it.



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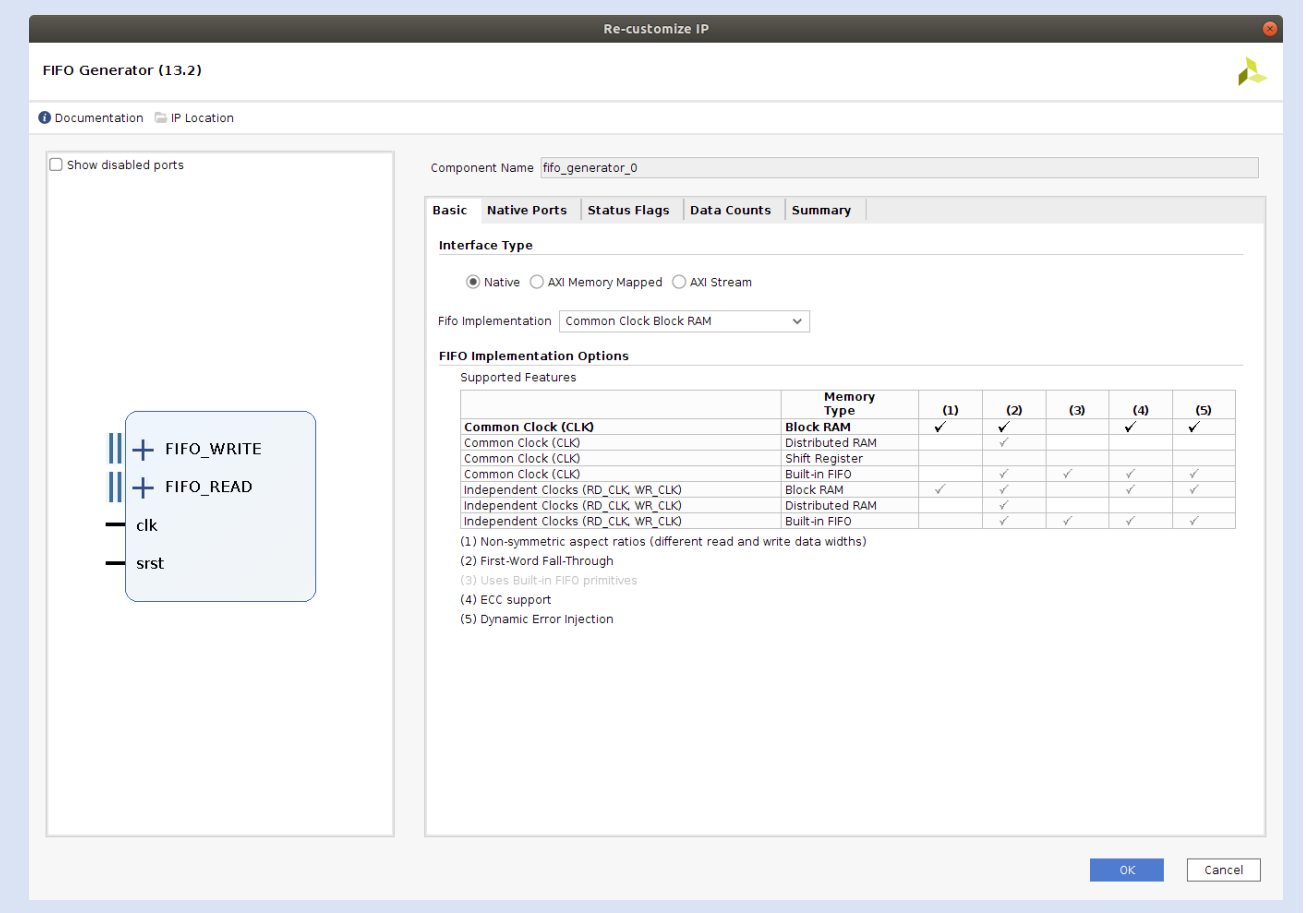
Step 8 – Leave the first page unchanged.



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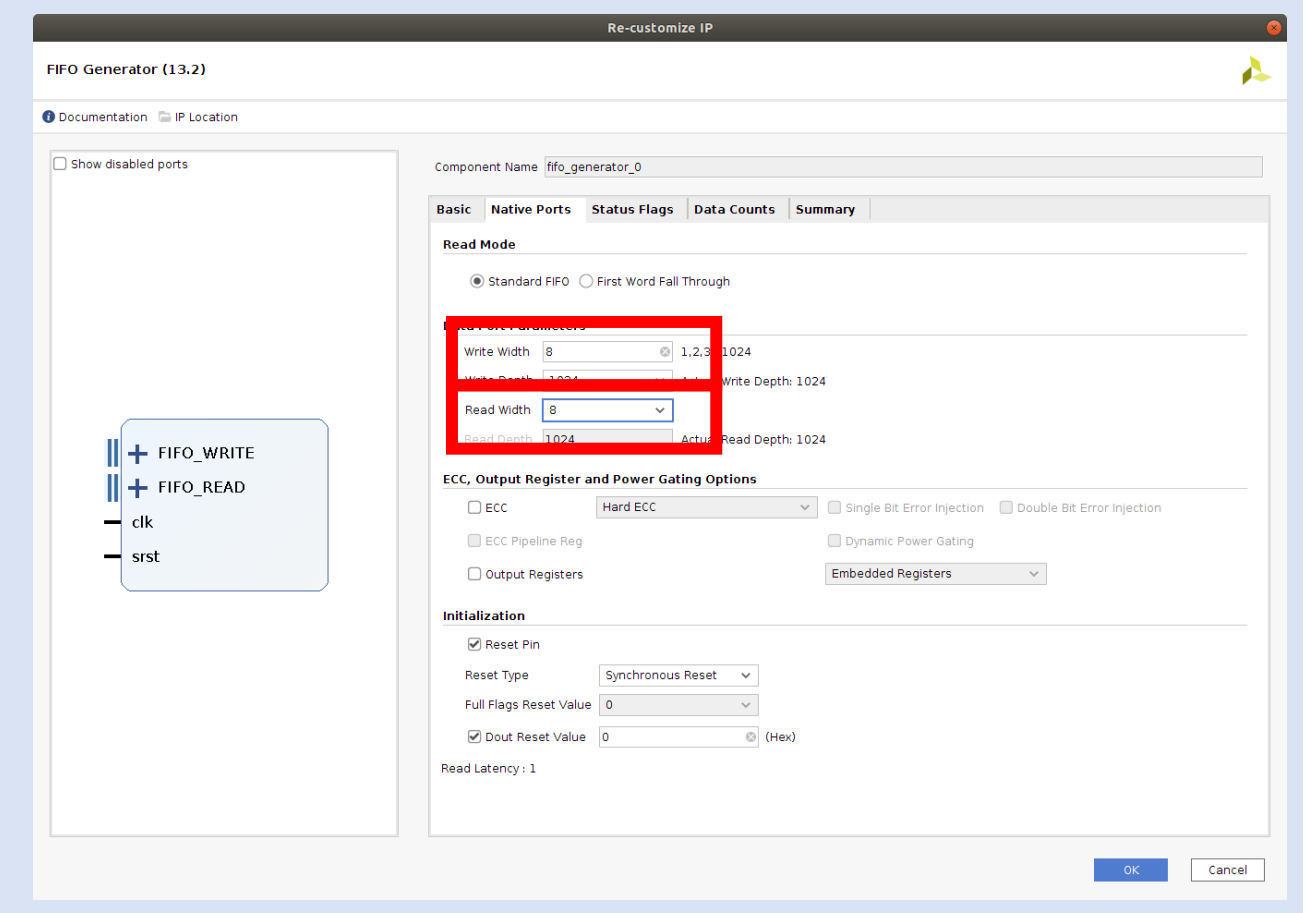
Step 9 – Change the Write and Read Width to be **8 bits**.



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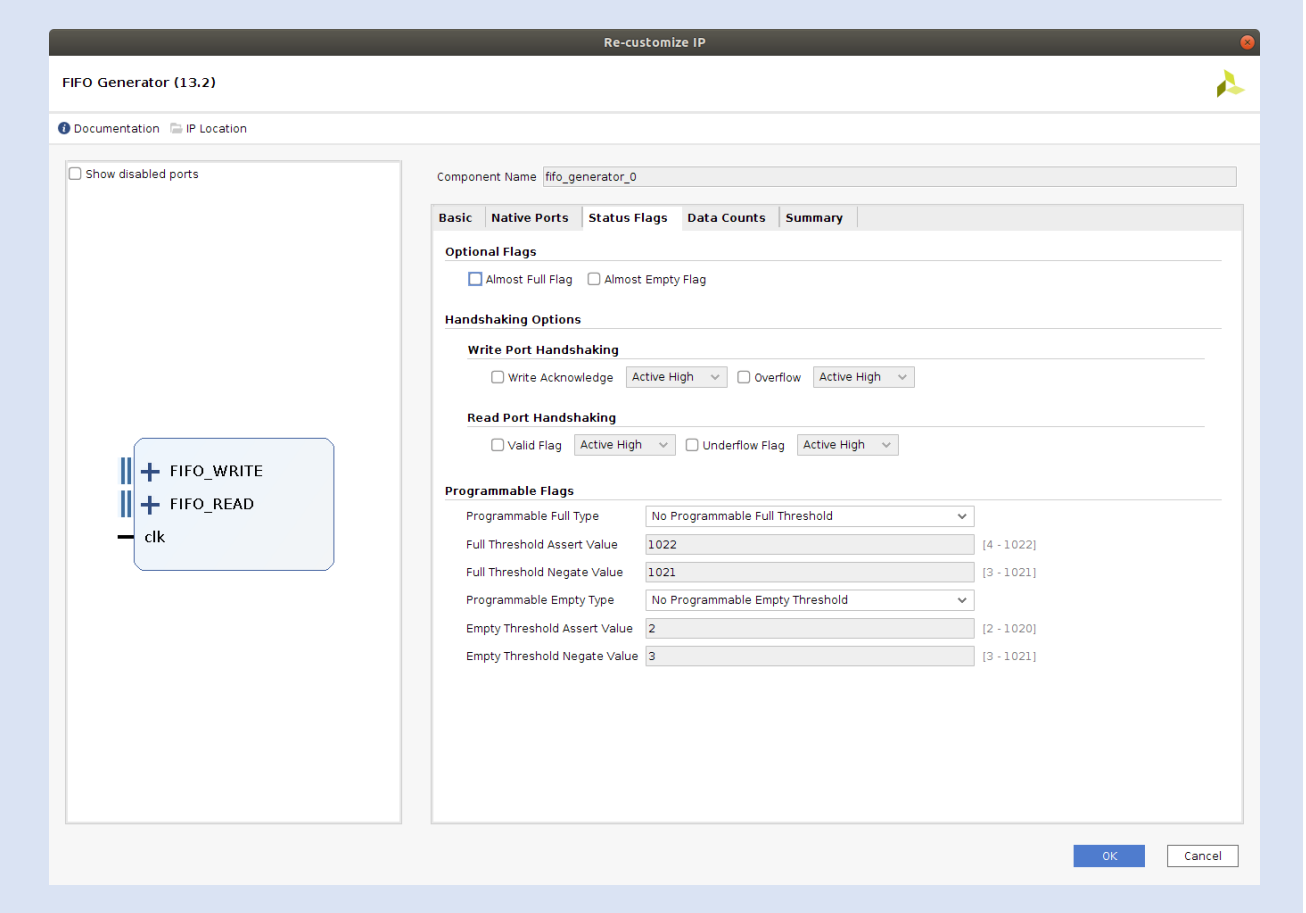
Step 10 – Leave the third page unchanged.



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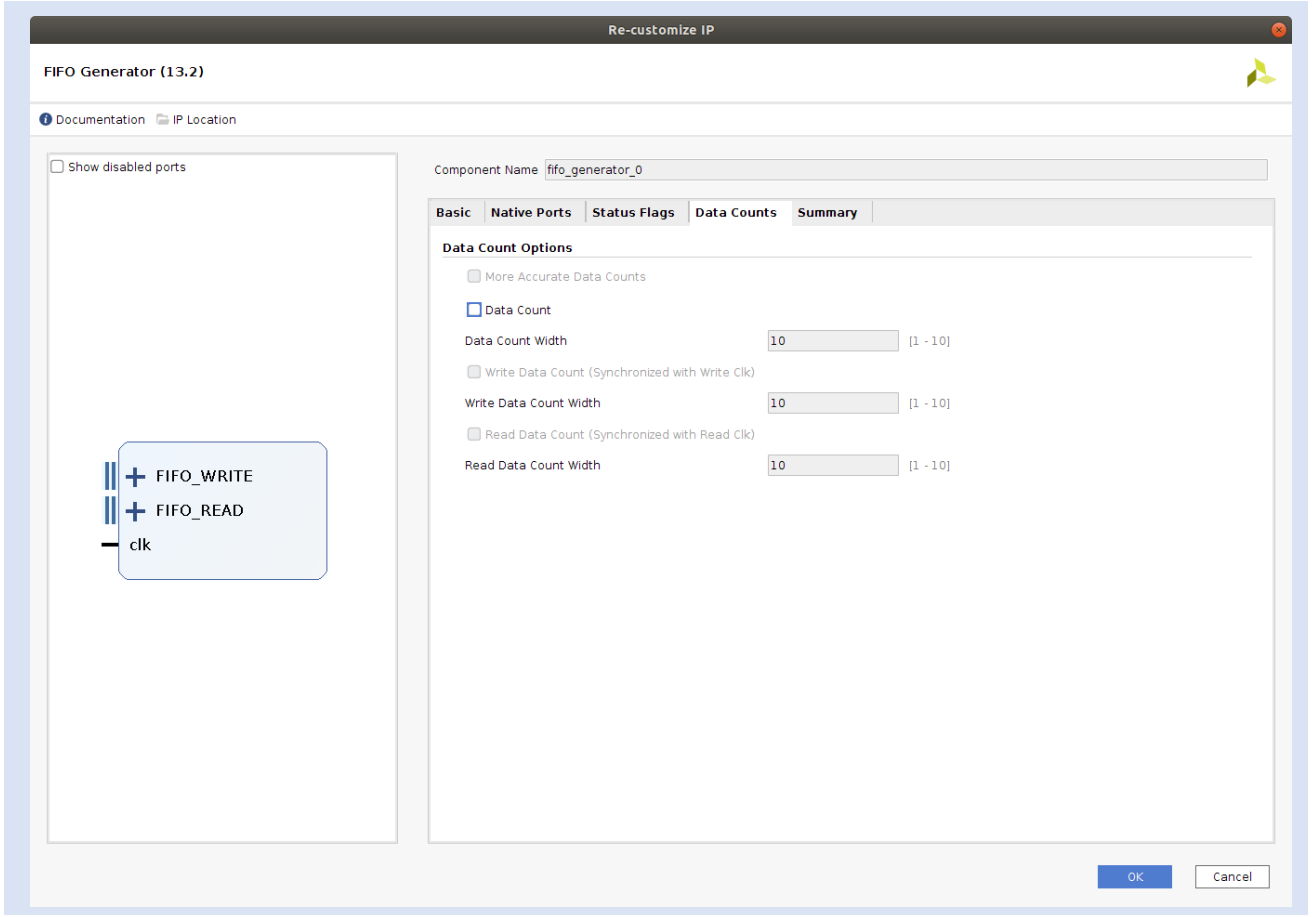
Step 11 – Leave the fourth page unchanged.



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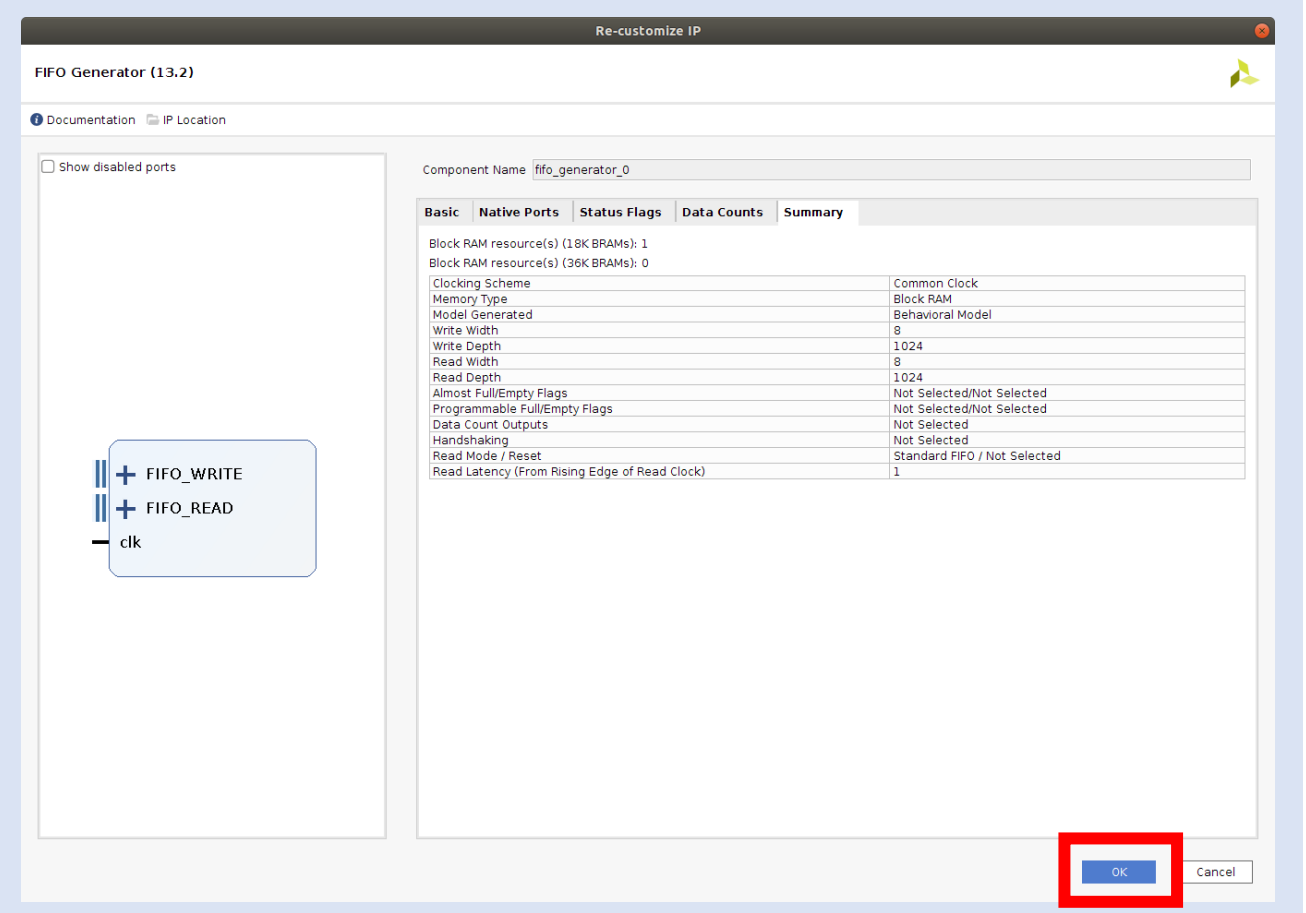
Step 12 – Leave the final page unchanged. Note that the FIFO OP are unregistered. Click **OK**.



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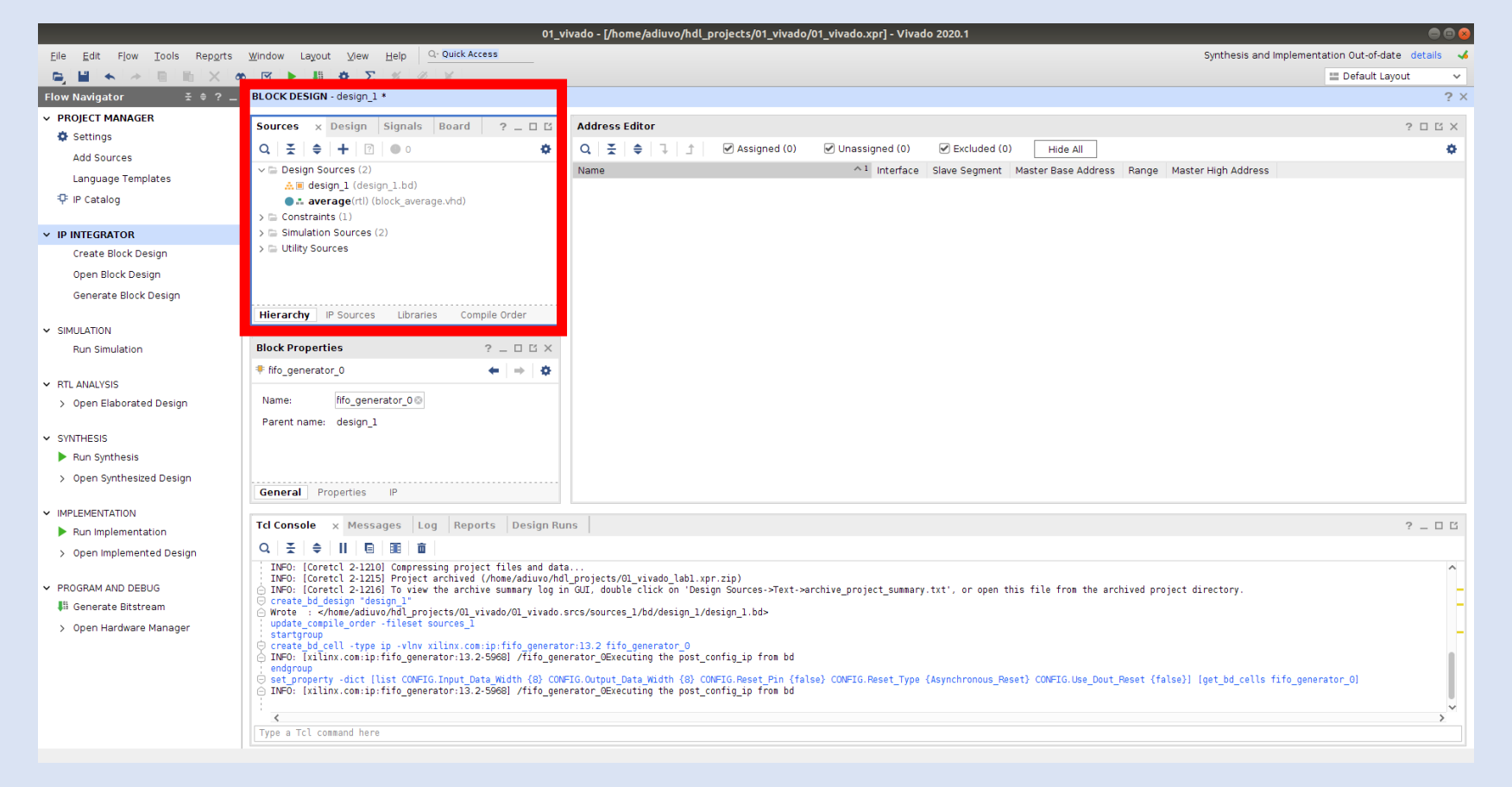
Step 13 – Click back on the Vivado Project Management view you will see the block diagram under the design sources.



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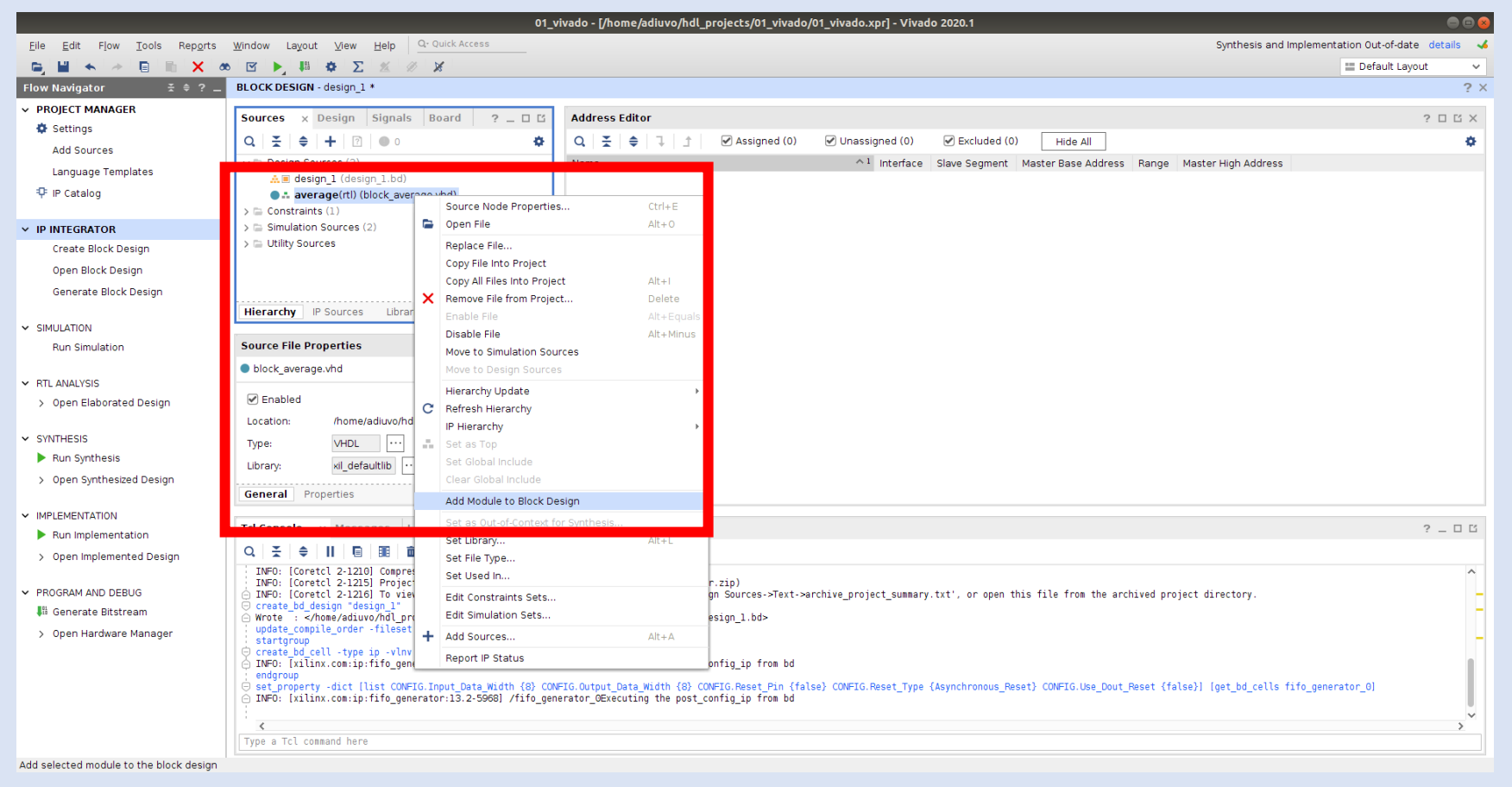
Step 14 – Right click on the average RTL block and select **Add Module to Block Design**.



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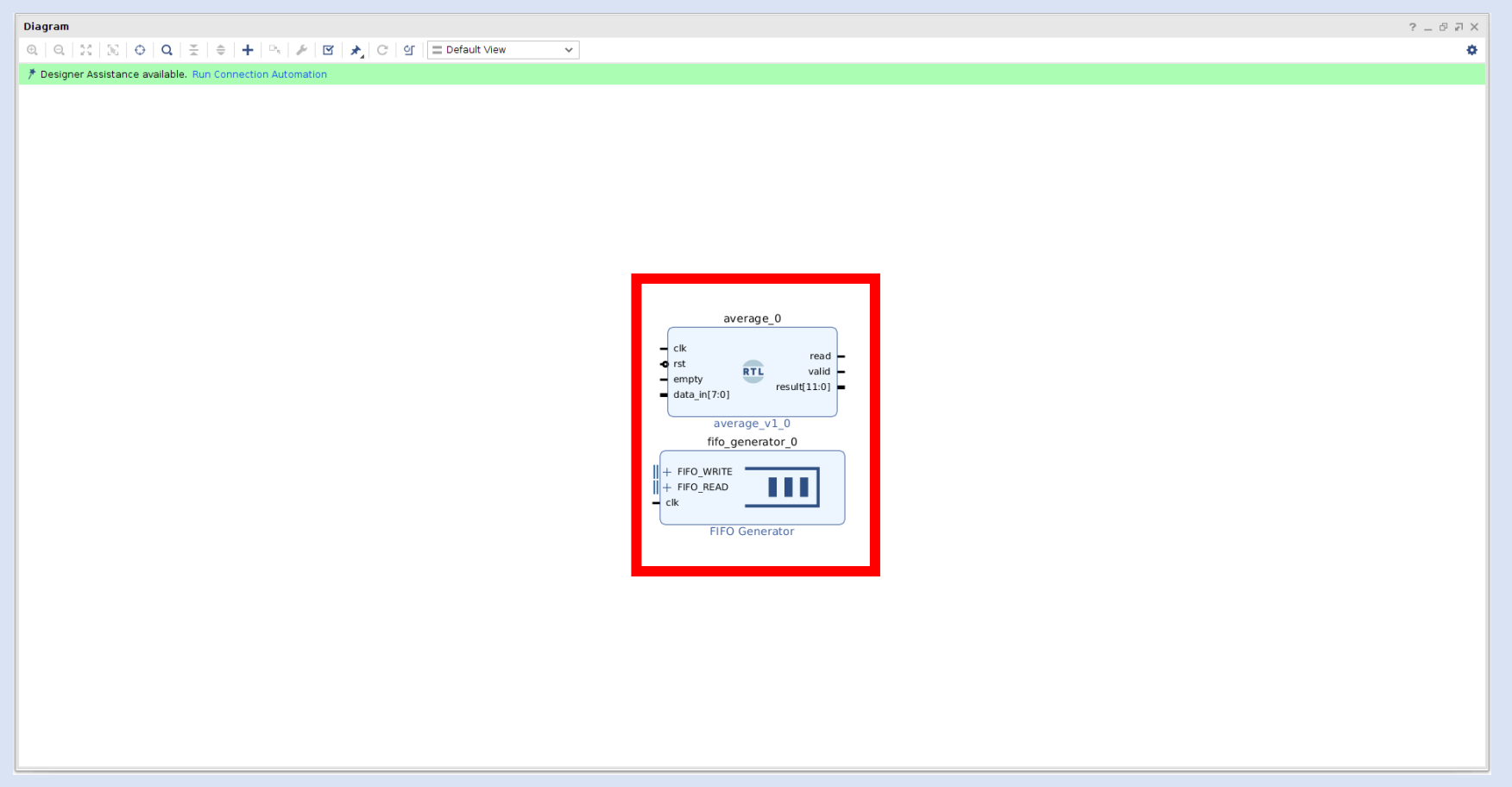
Step 15 – This will add the average block to the block diagram.



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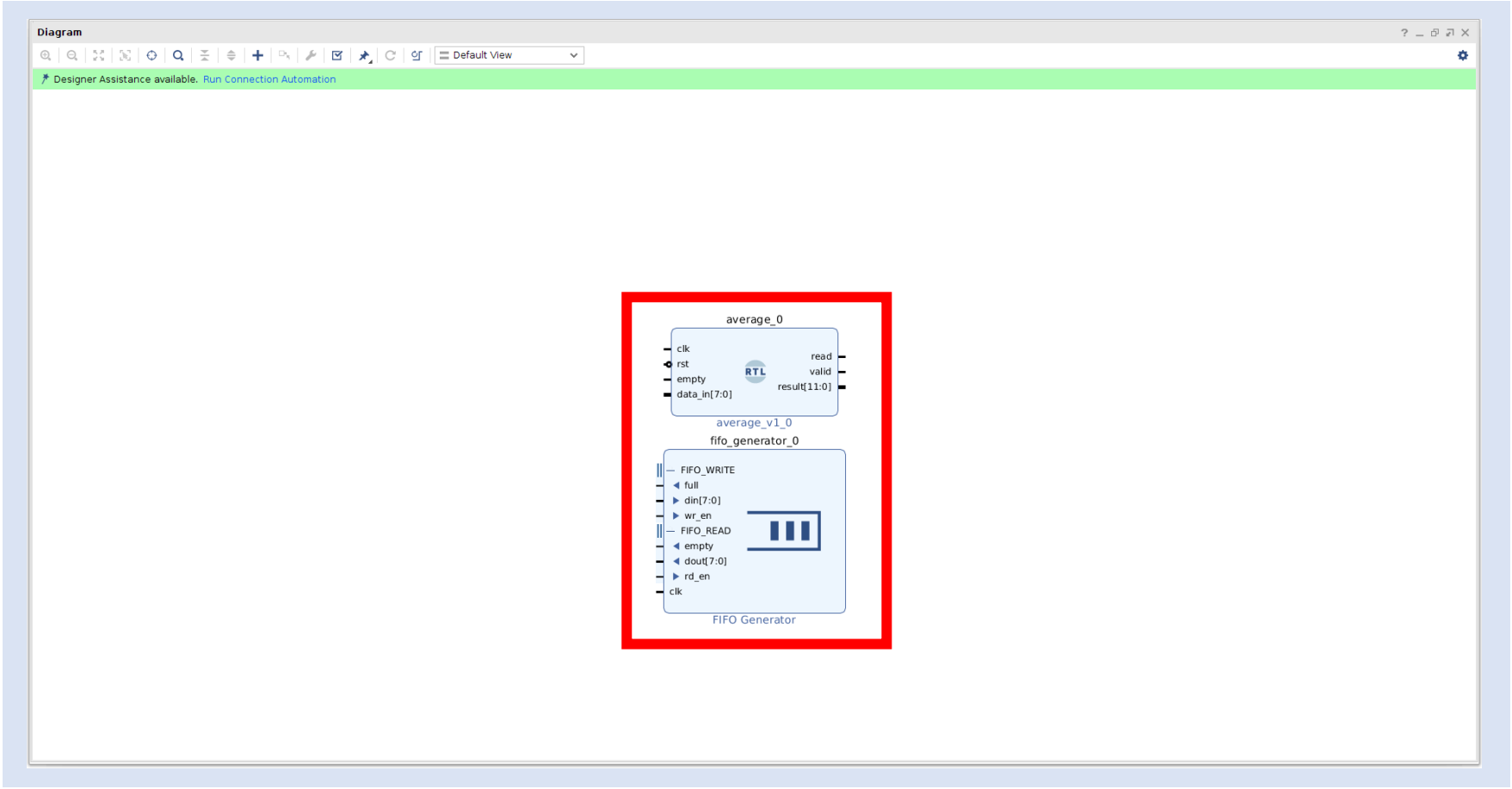
Step 16 – Expand the FIFO Write and Read Interfaces.



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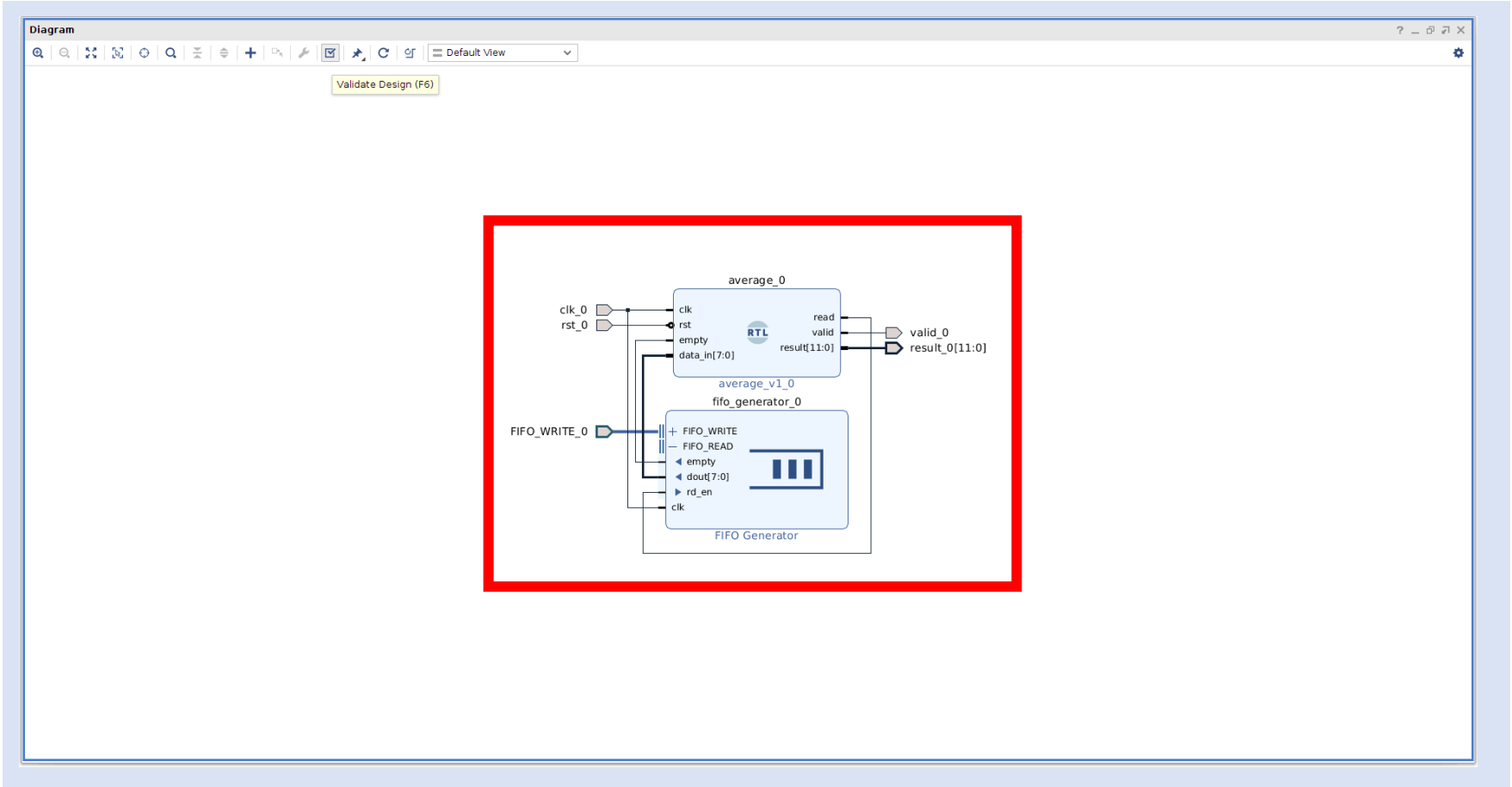
Step 17 – Make the Clk, Reset, Result, Valid and FIFO Write interfaces external by right-clicking on each pin and selecting **Make External**. Connect the remaining interfaces as below.



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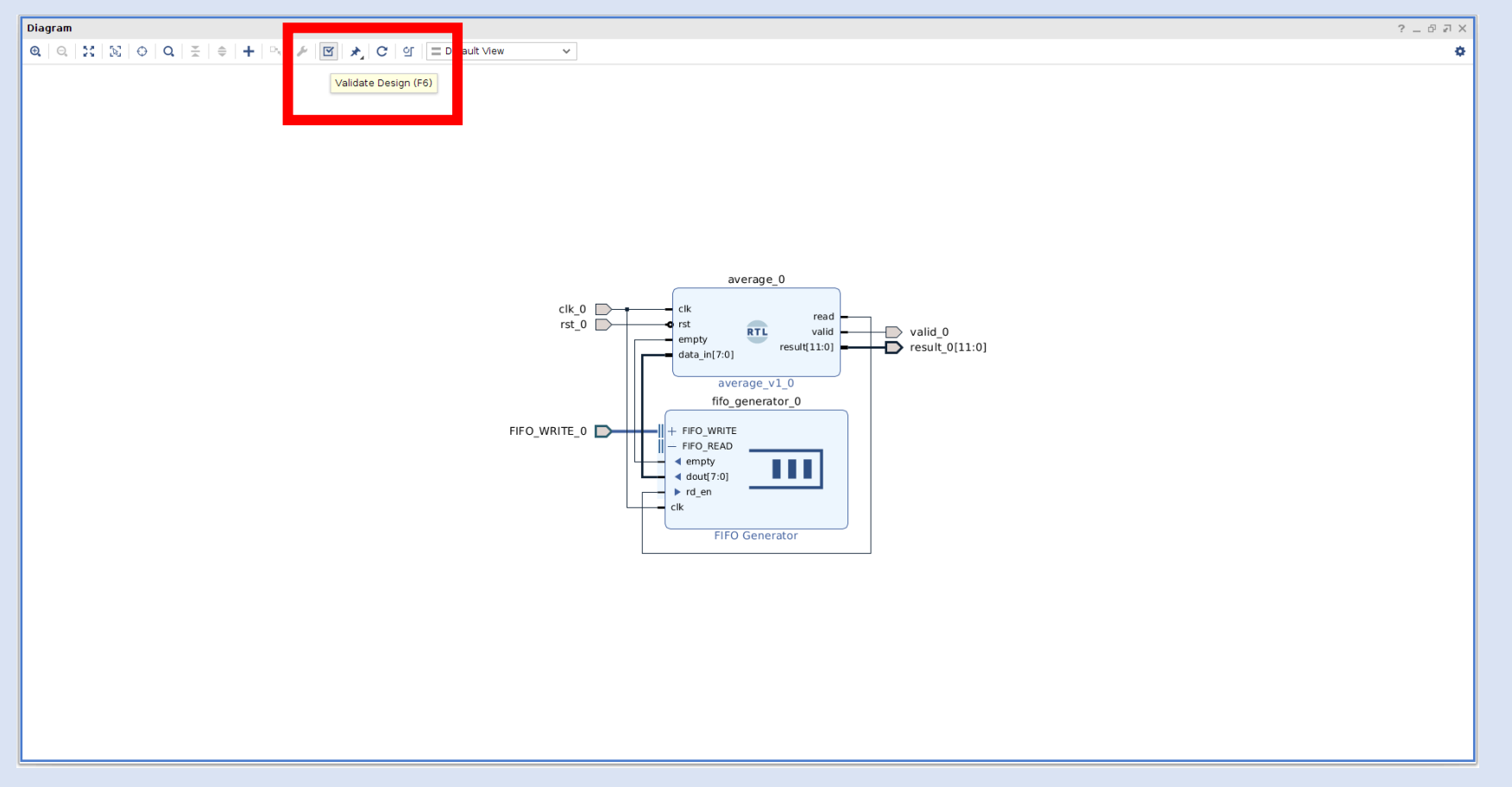
Step 18 – Click on **Validate Design**.



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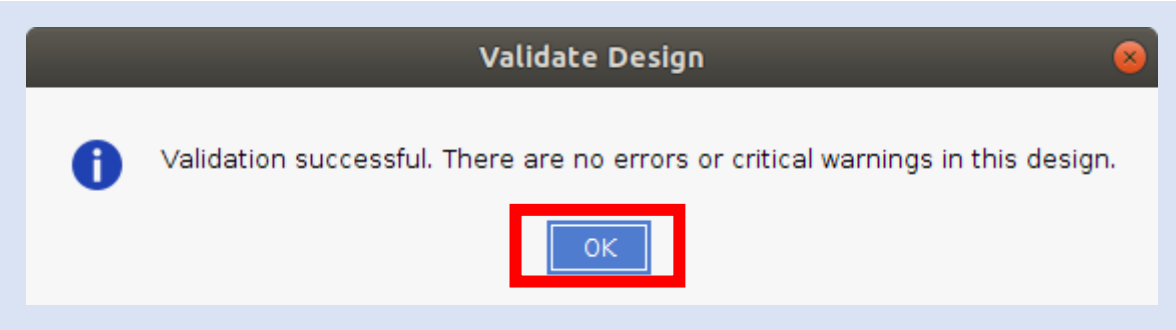
Step 19 – The validated design should result in no error or critical warnings. Click **OK**.



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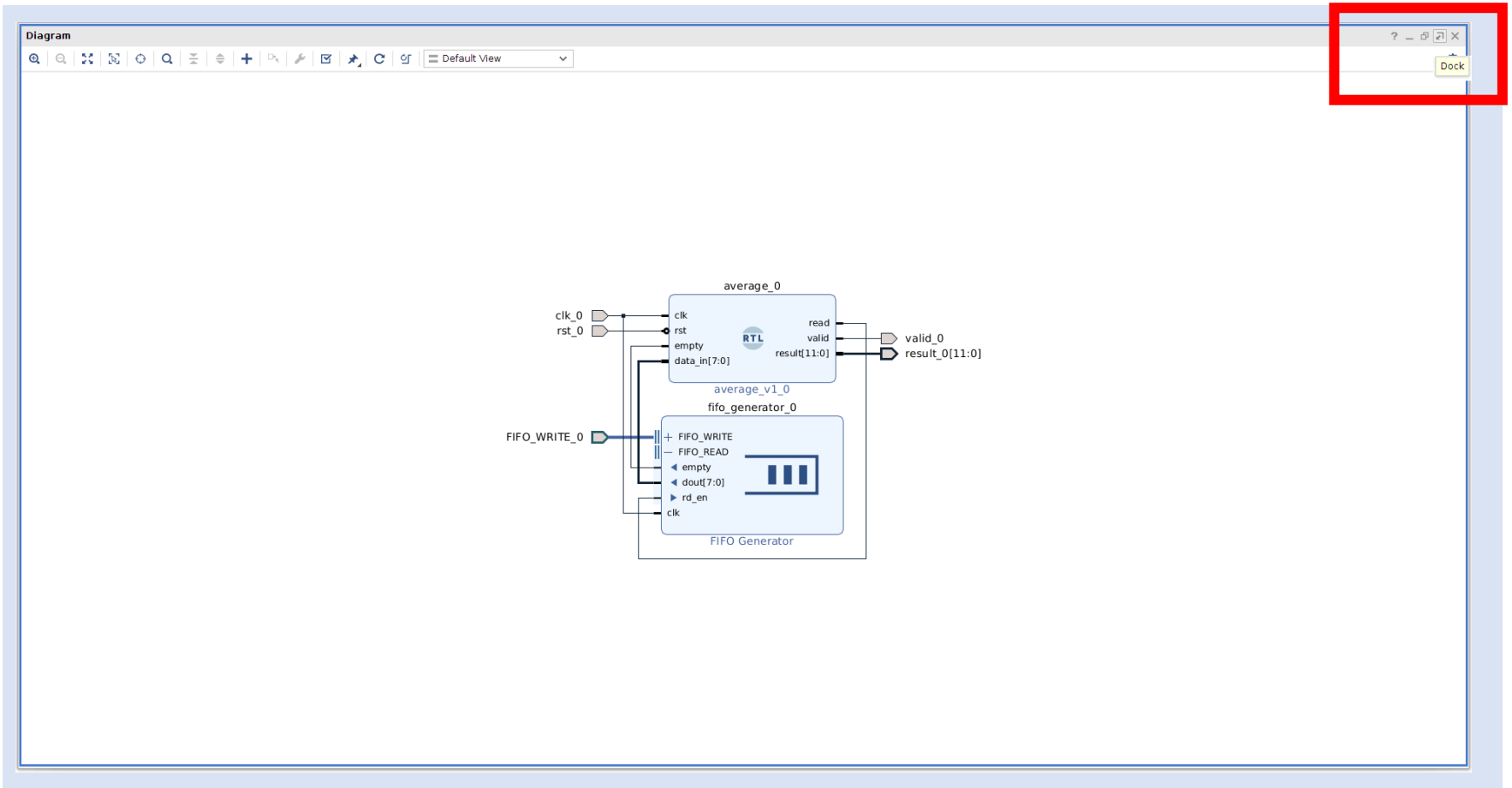
Step 20 – Re-dock the block diagram window into the Vivado Project Manager.



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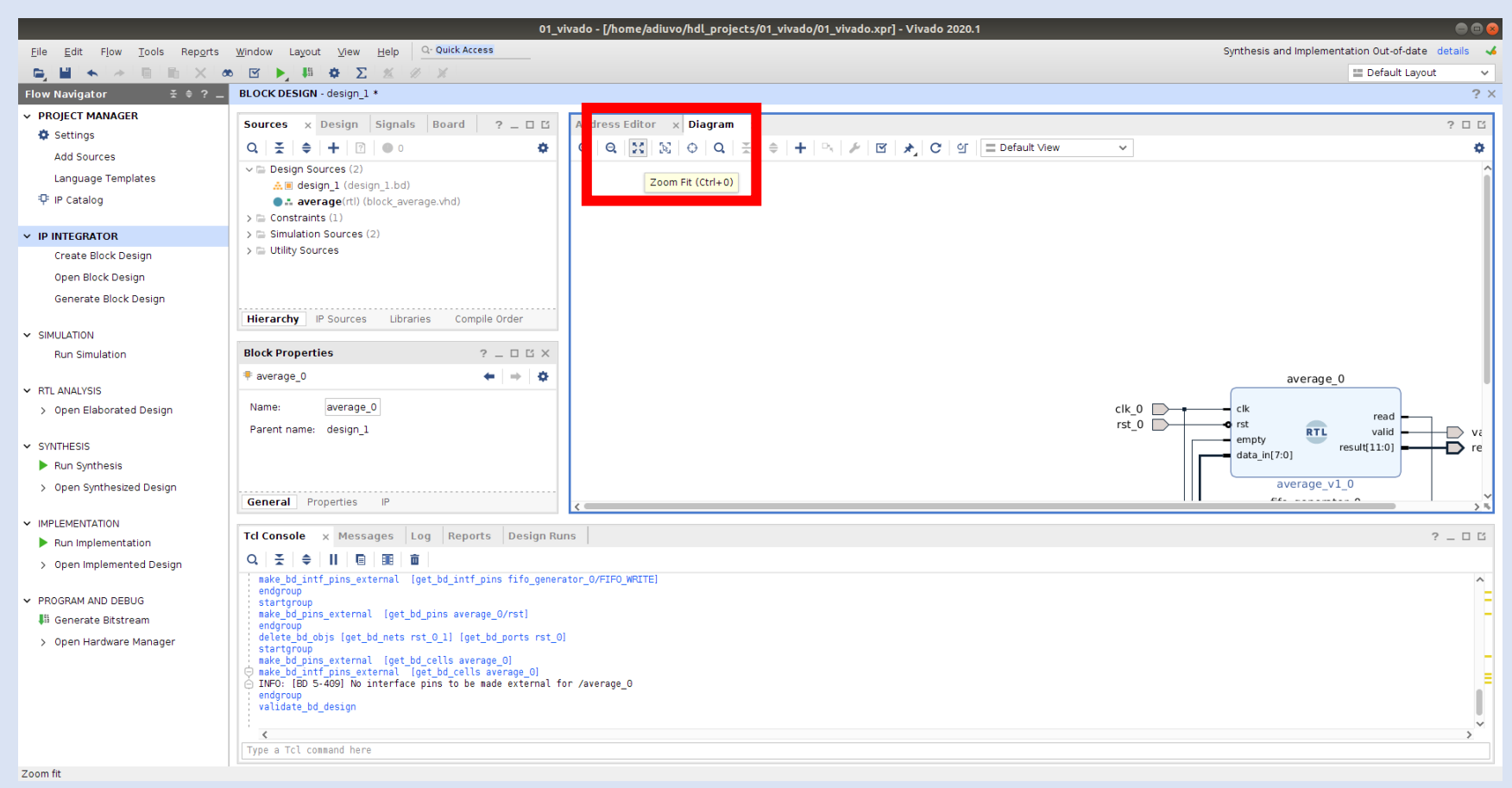
Step 21 – Click on the **Zoom Fit** button to fit the design to the window.



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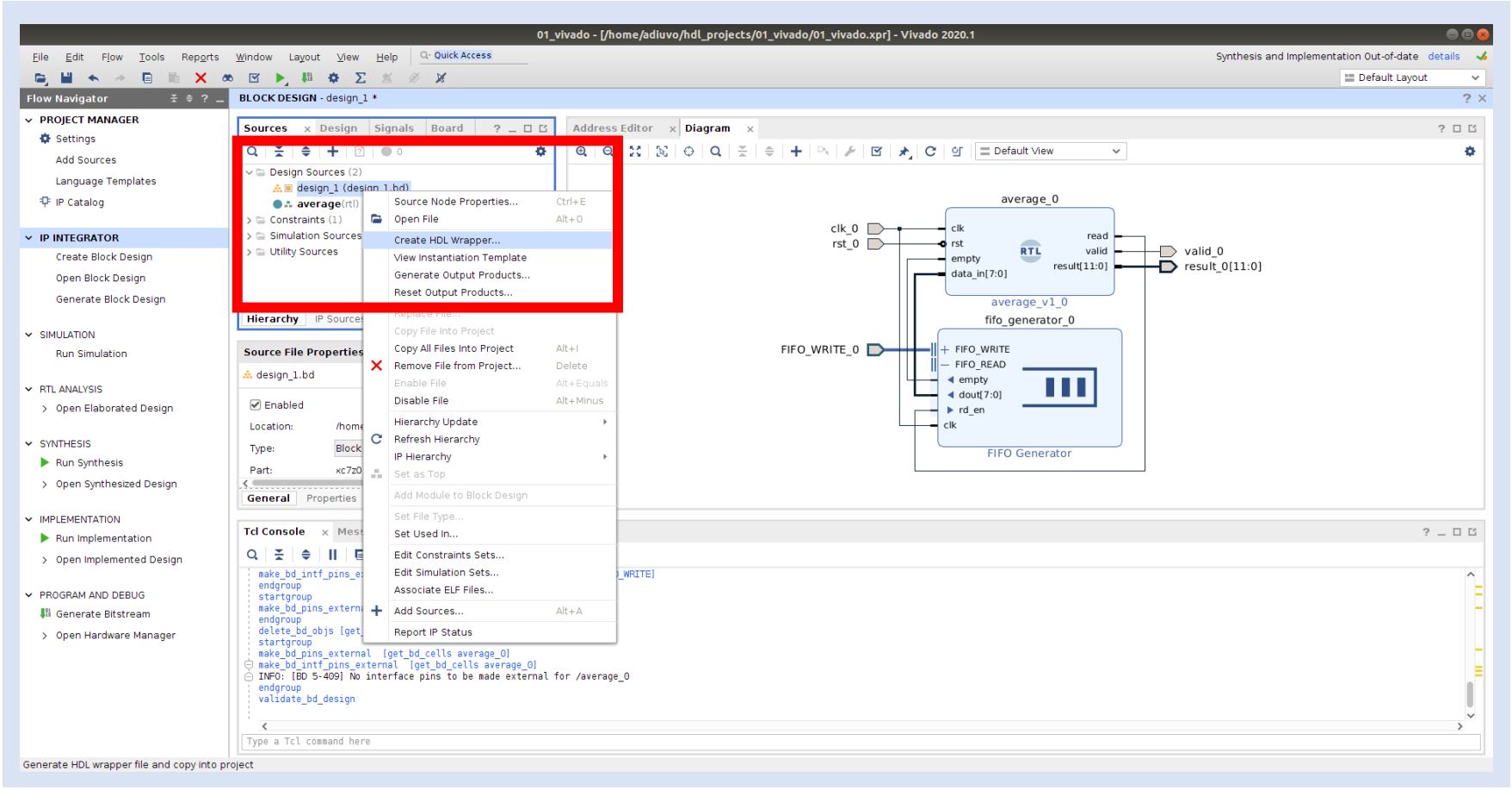
Step 22 – Right click on the block diagram design under the Design Sources tab and select **Create HDL Wrapper**.



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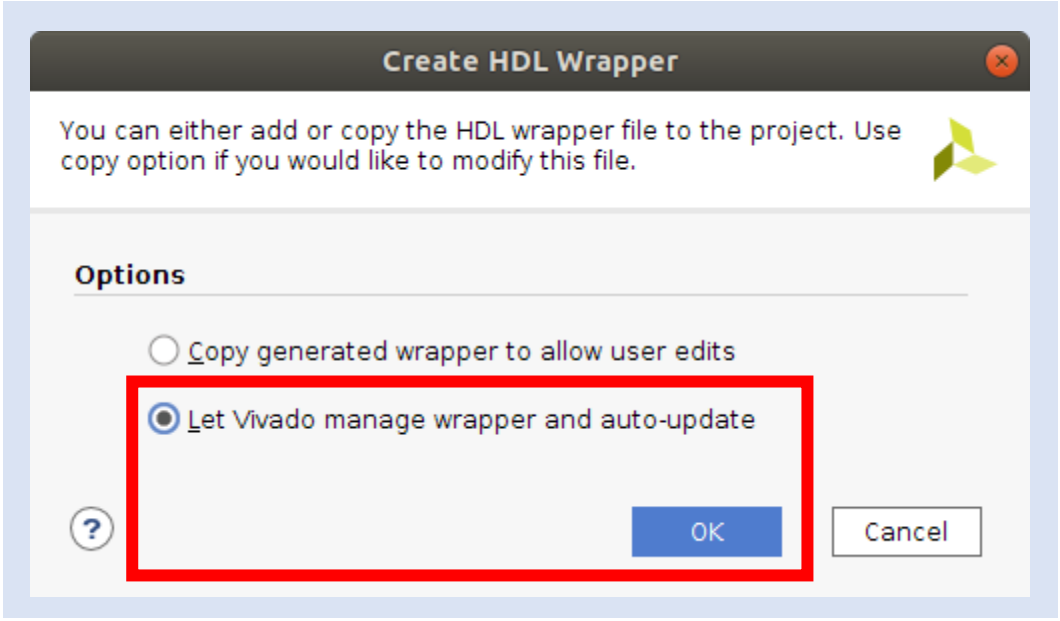
Step 23 – Allow Vivado to manage the wrapper and click **OK**.



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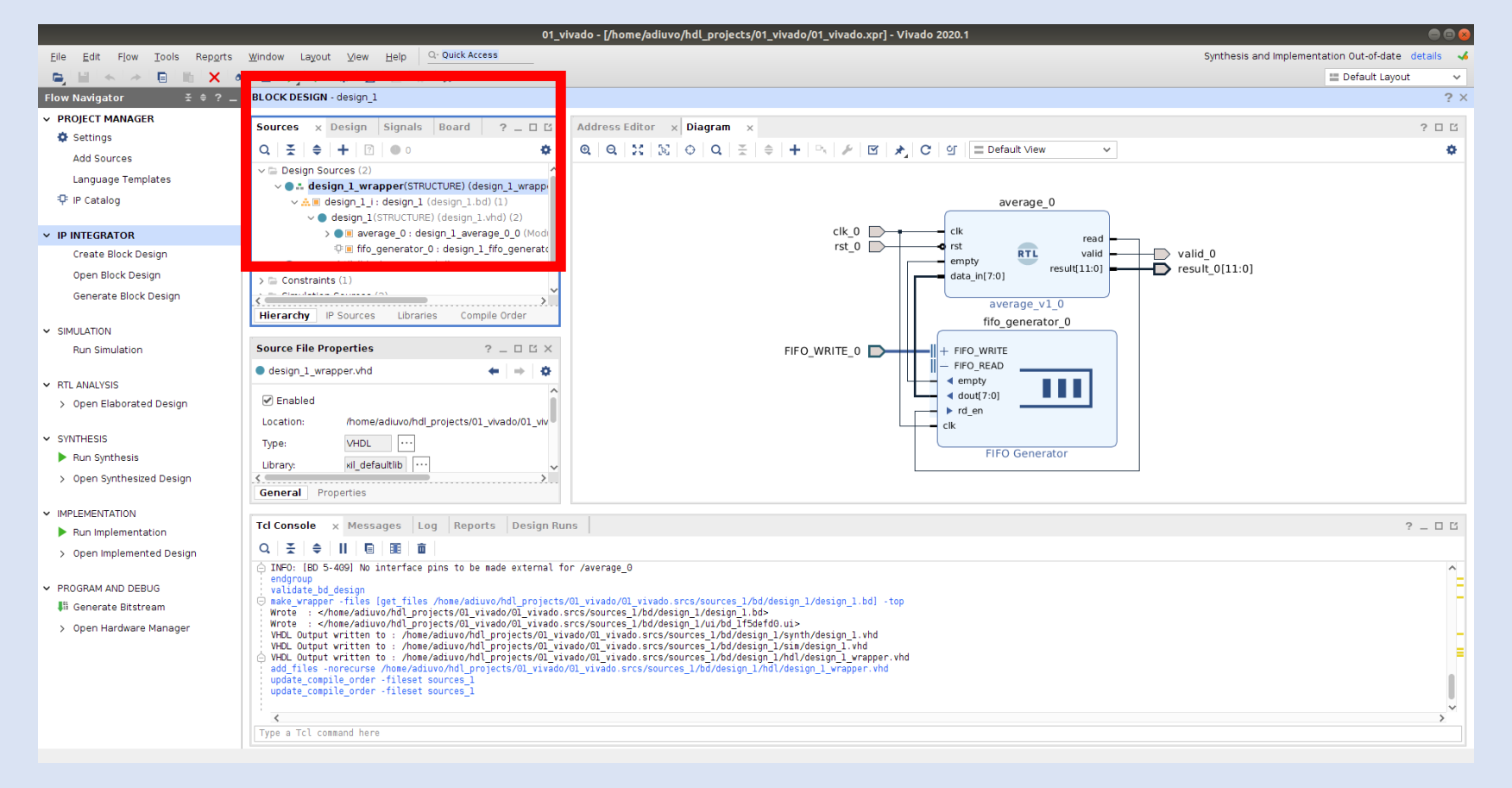
Step 24 – Expand the newly created wrapper and you will see the entire design.



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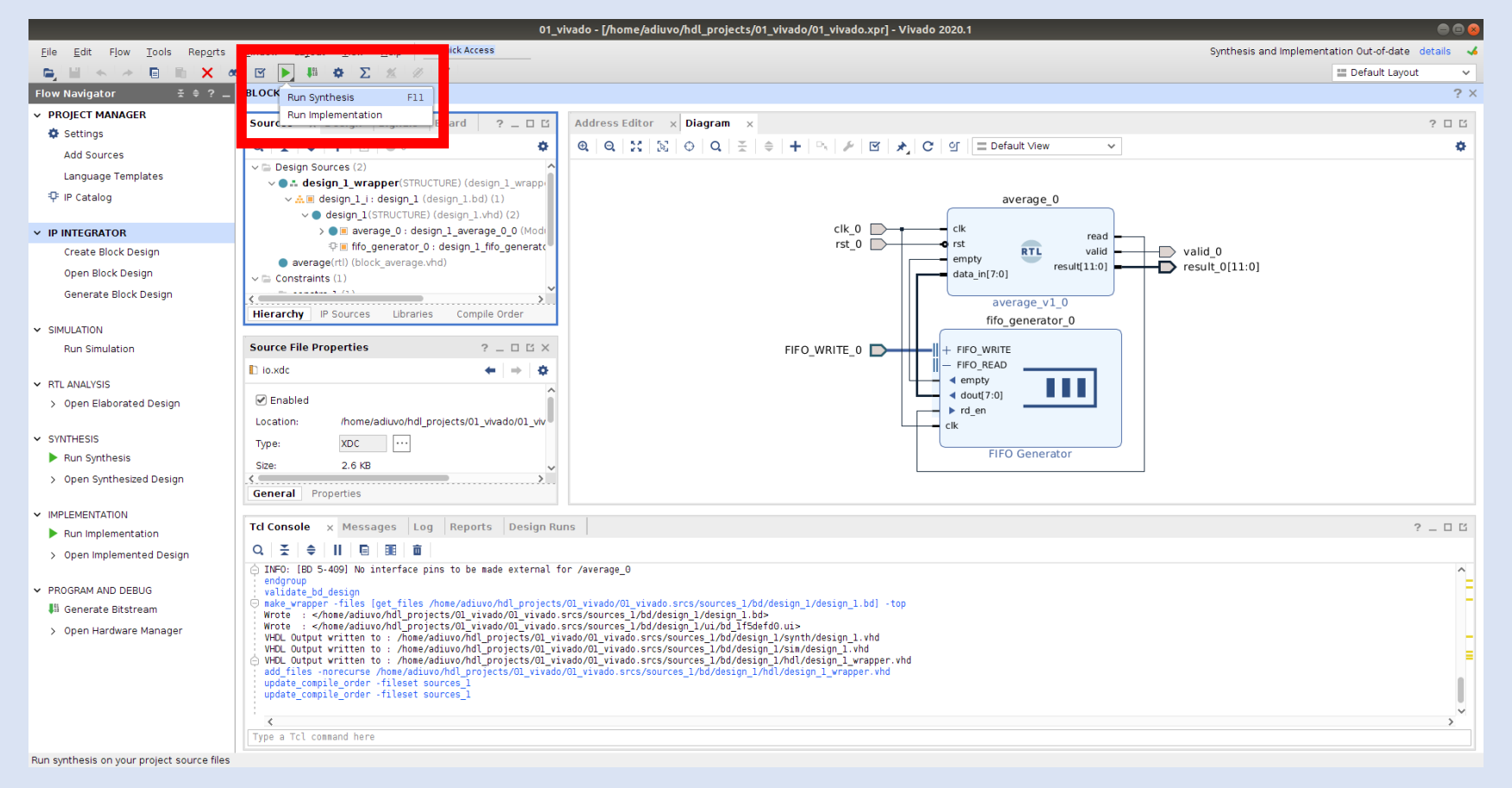
Step 25 – Run the Synthesis.



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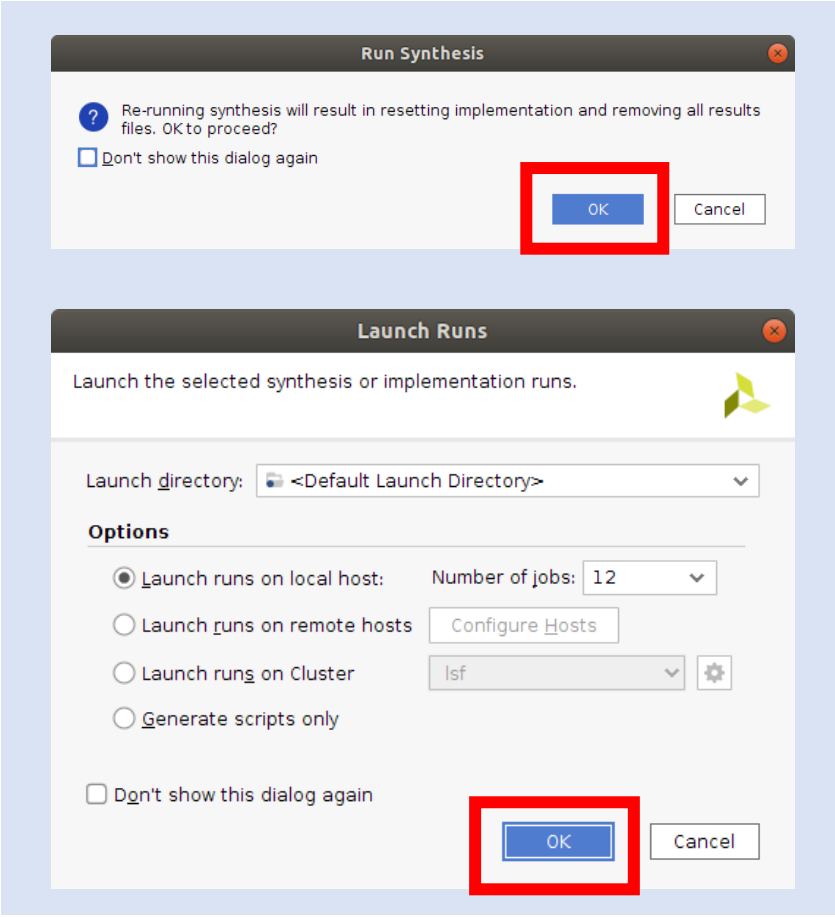
Step 26 – On both resultant dialogs click **OK** and wait for synthesis to complete.



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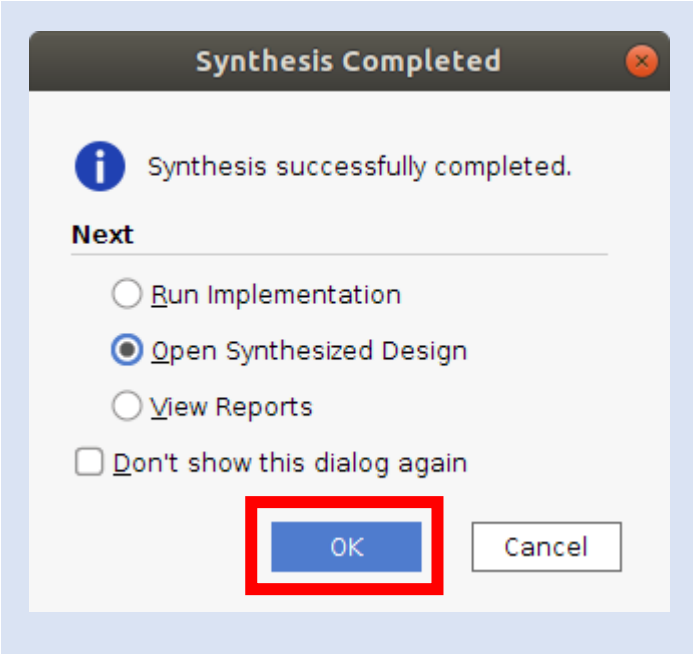
Step 27 – When synthesis completes, **Open the Synthesized Design.**



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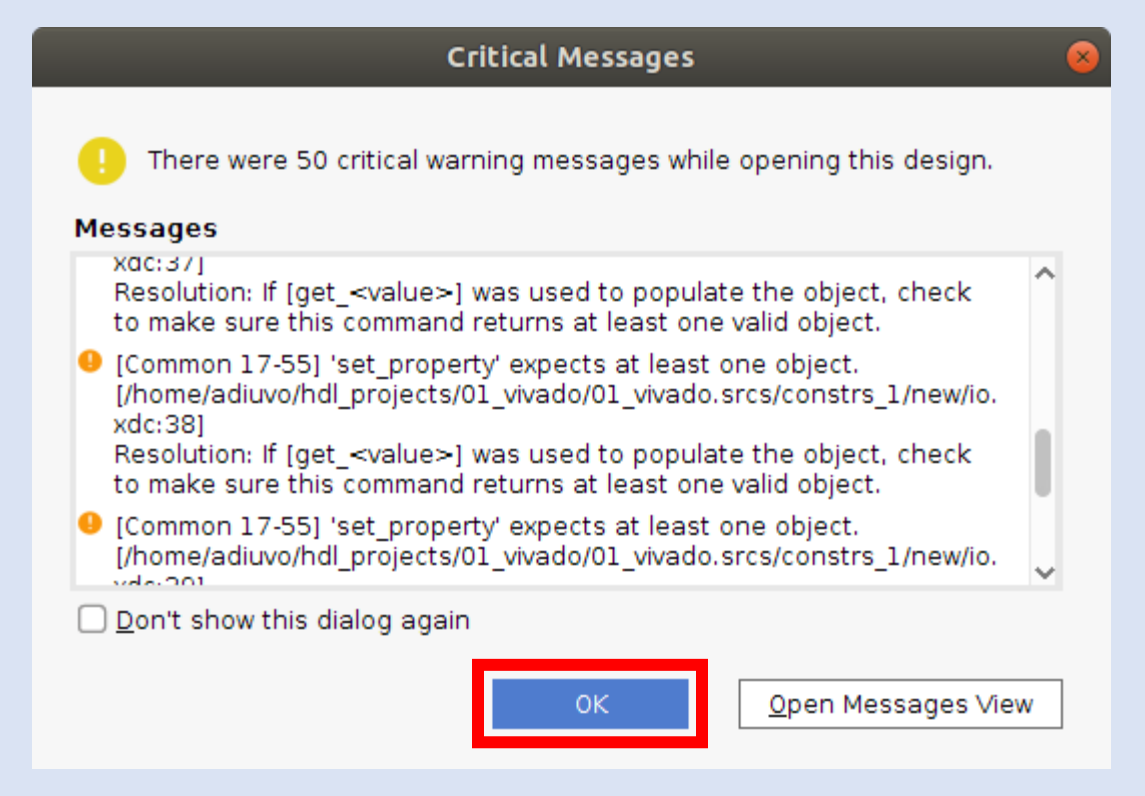
Step 28 – If any critical warnings pop up, select **OK.** This is due to out of data constraints which we are about to address.



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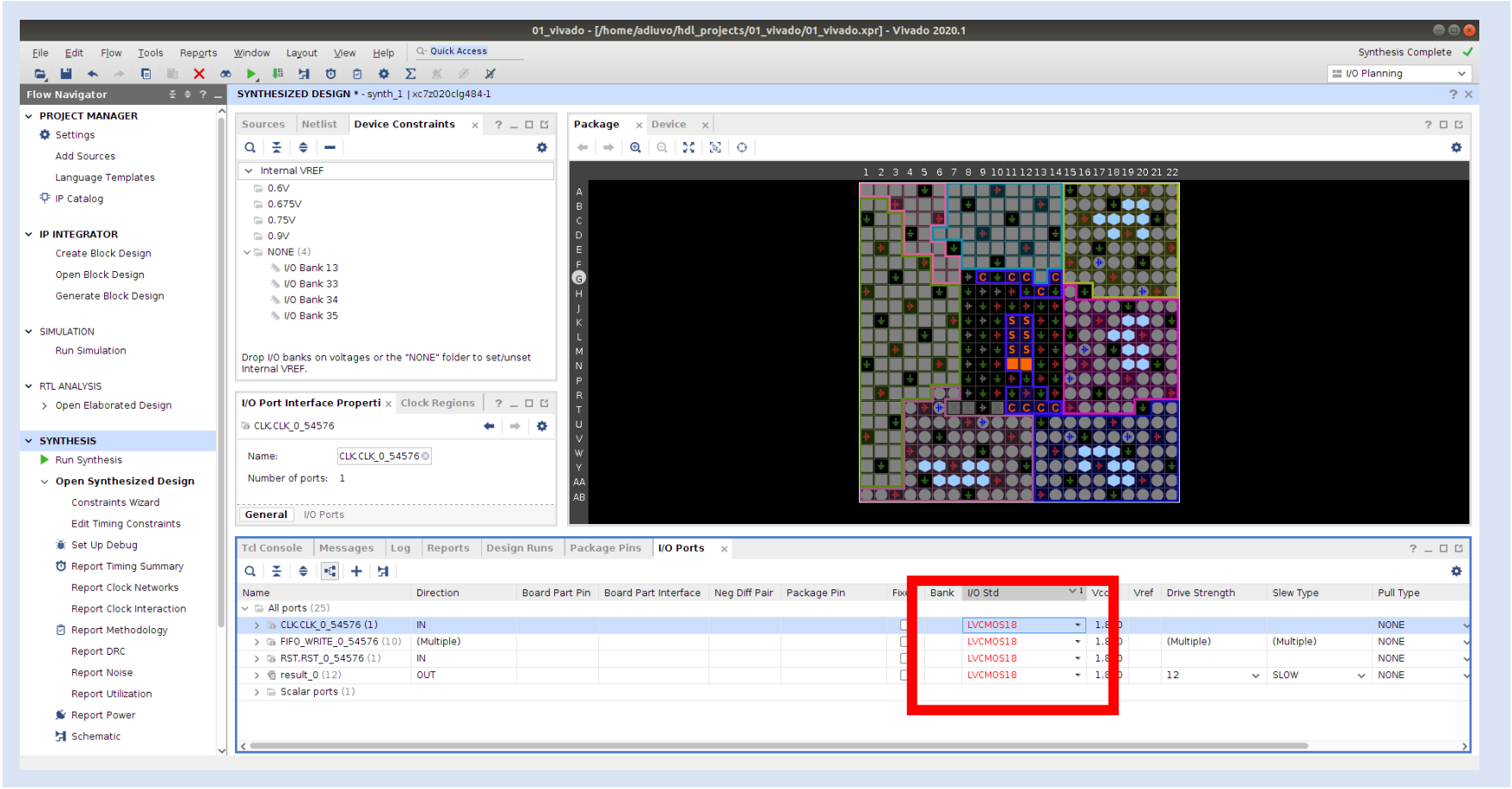
Step 29 – Change the I/O standard from default to **LVCMOS18**.



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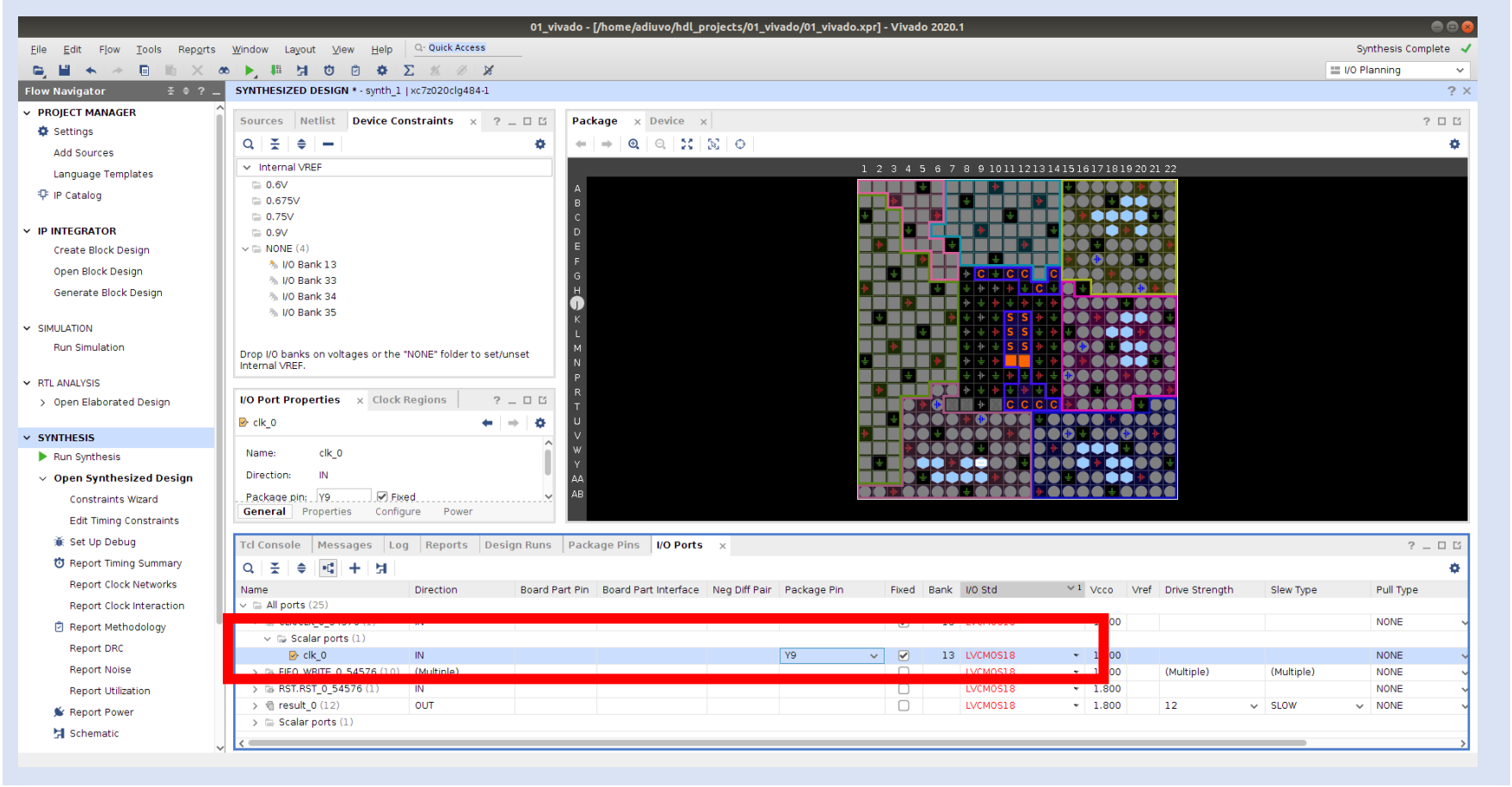
Step 30 – Assign the clock input to pin **Y9.** Assign all other IO to pins of your choice.



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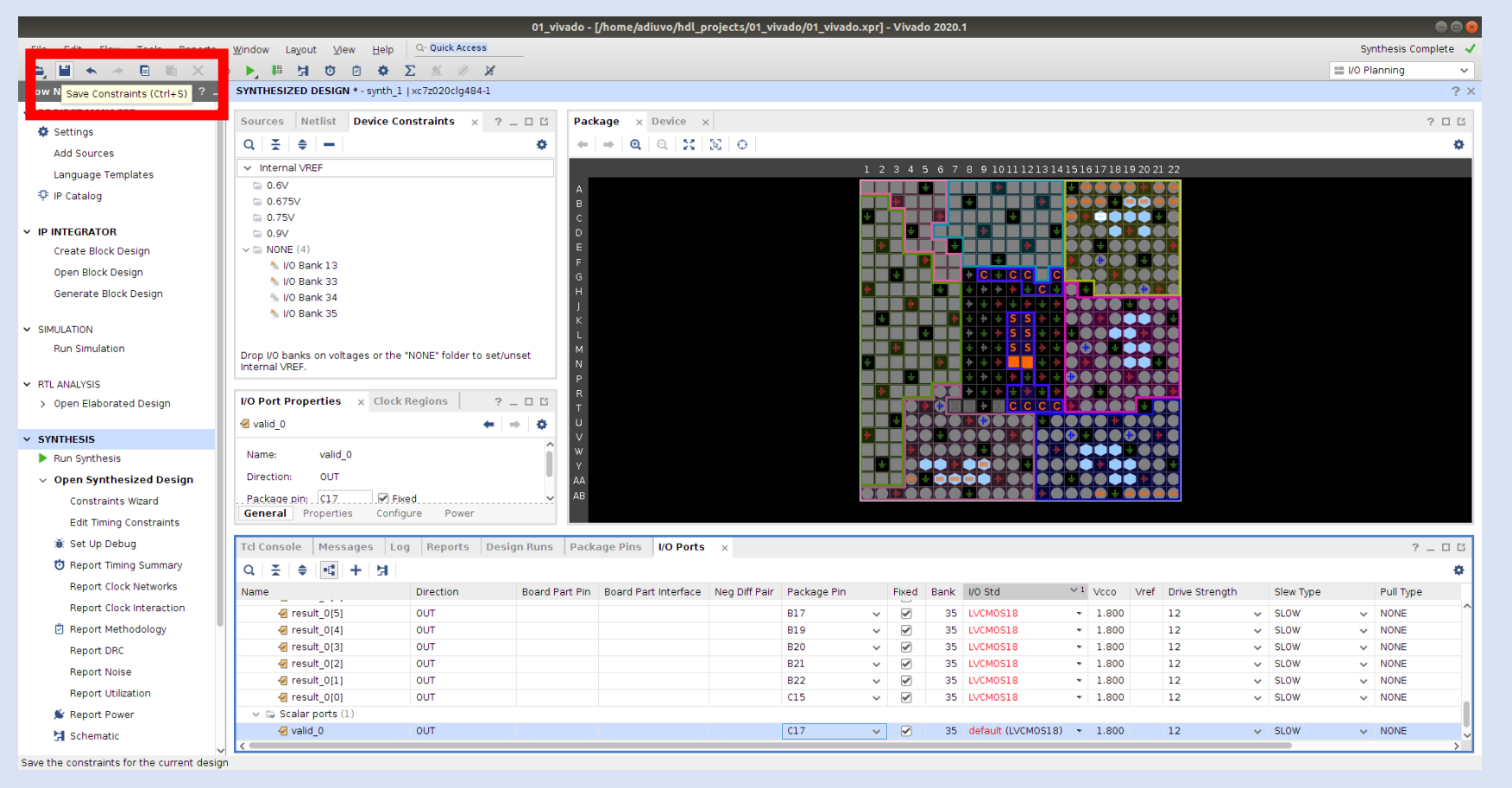
Step 31 – Click on **Save Constraints**.



Lab 2: Intermediate Vivado

Step 32 – If an out-of-date warning appears, click **OK**.

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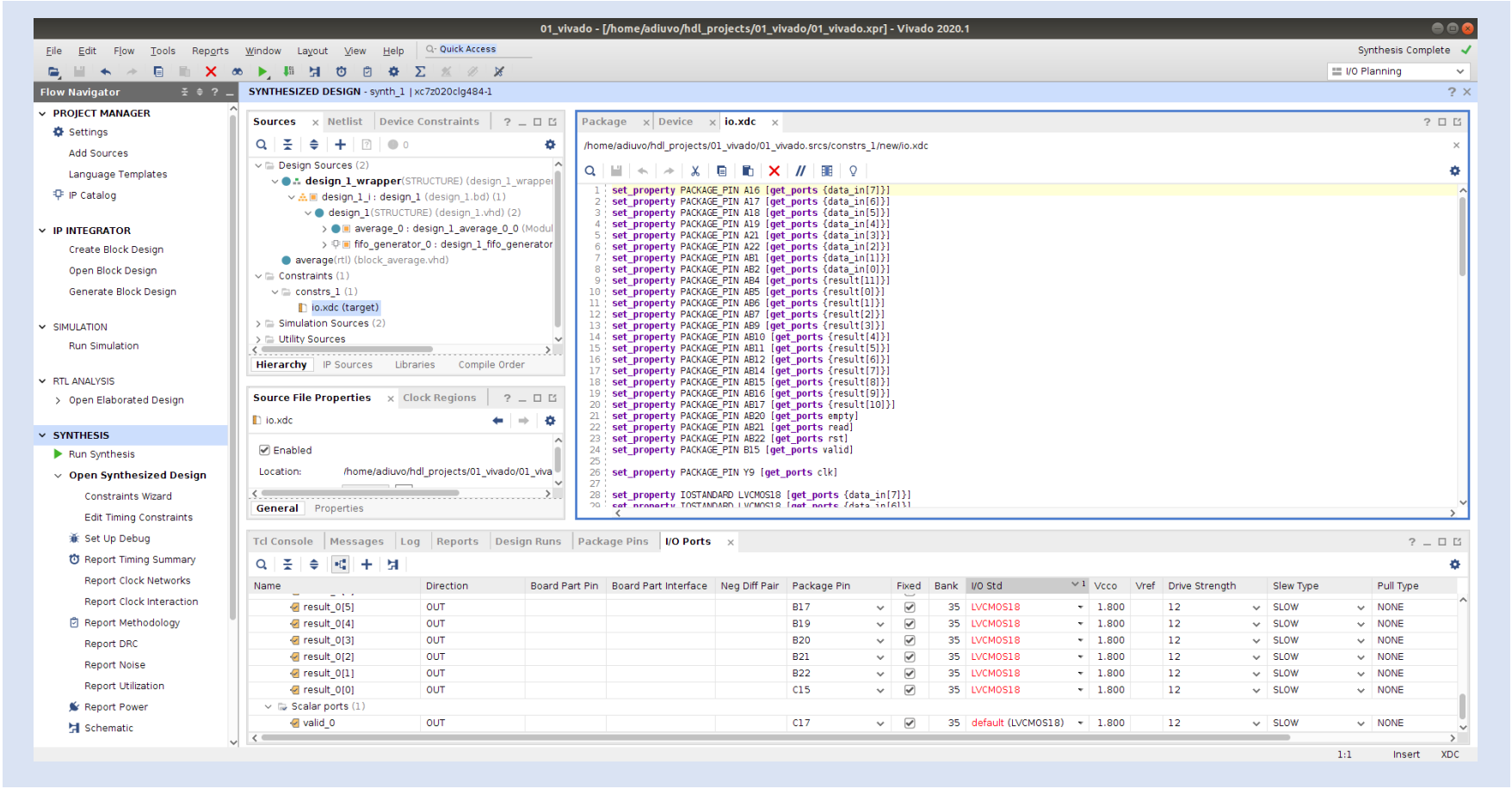
Step 33 – From the sources tab, open the **IO constraints.** You will see the old pin out for the previous project and your new project. This is because we have evolved the original project.



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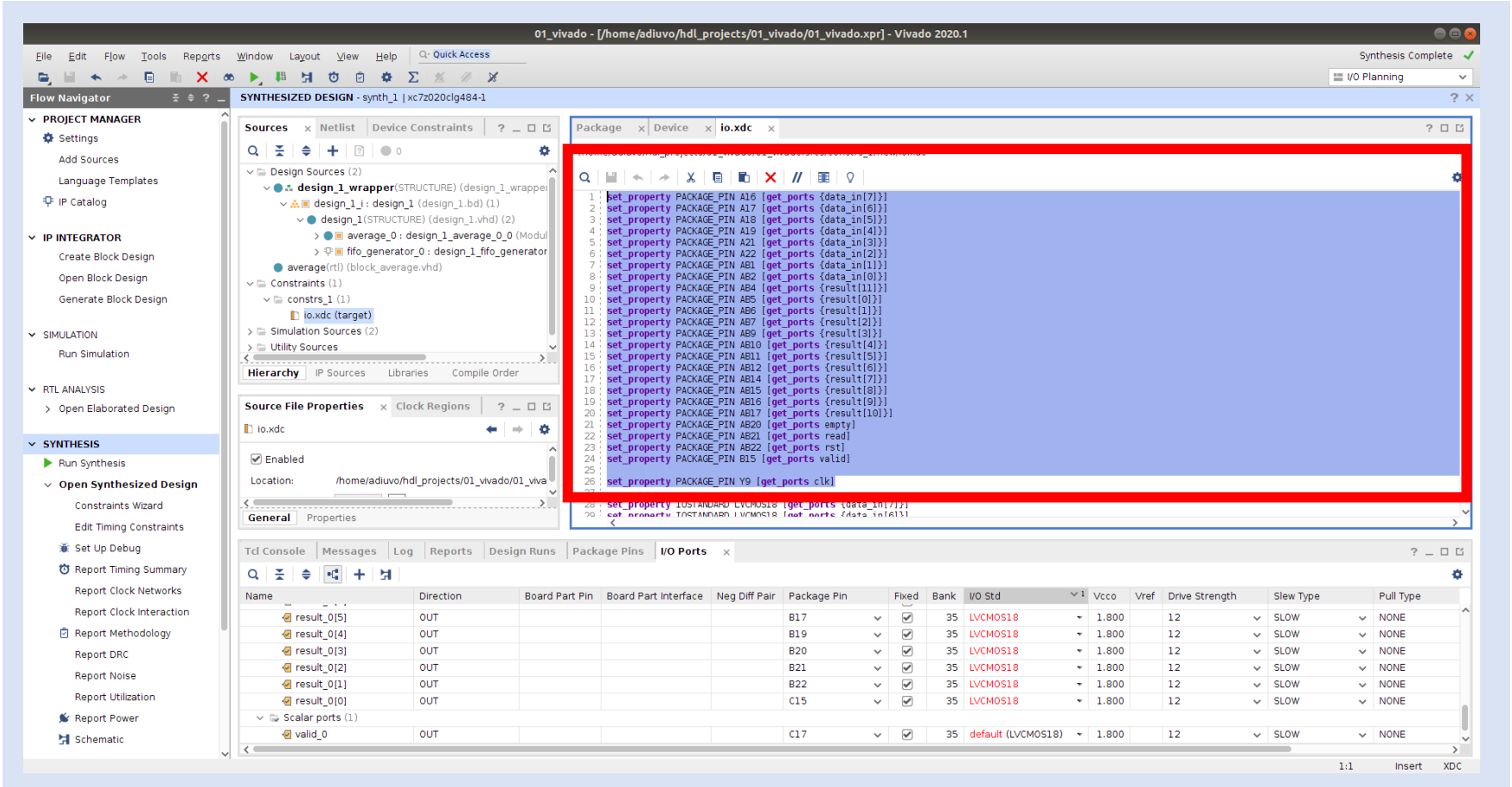
Step 34 – Select the old constraints (at the top of the file) and delete them. Save the file.



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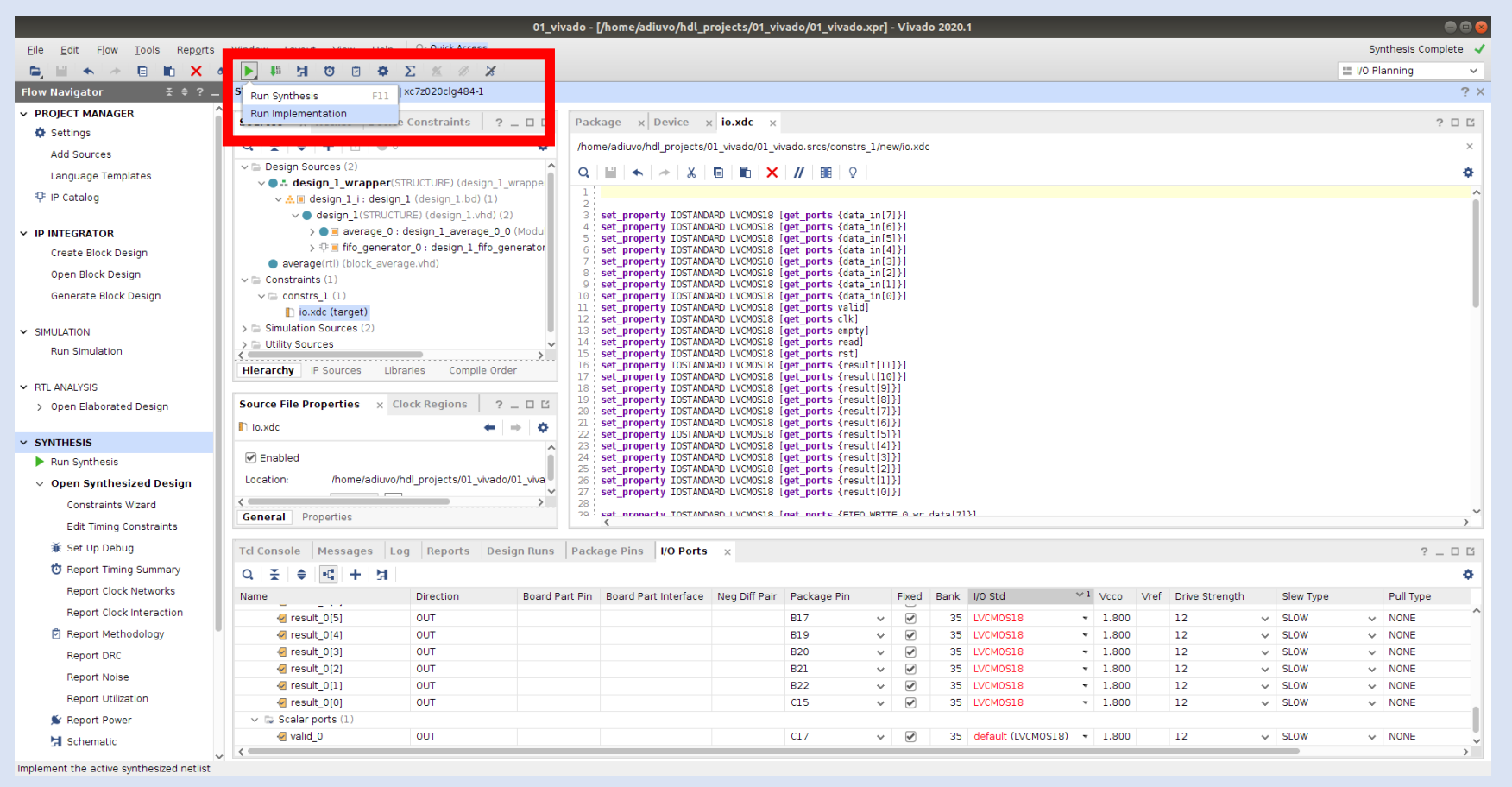
Step 35 – Run the Implementation.



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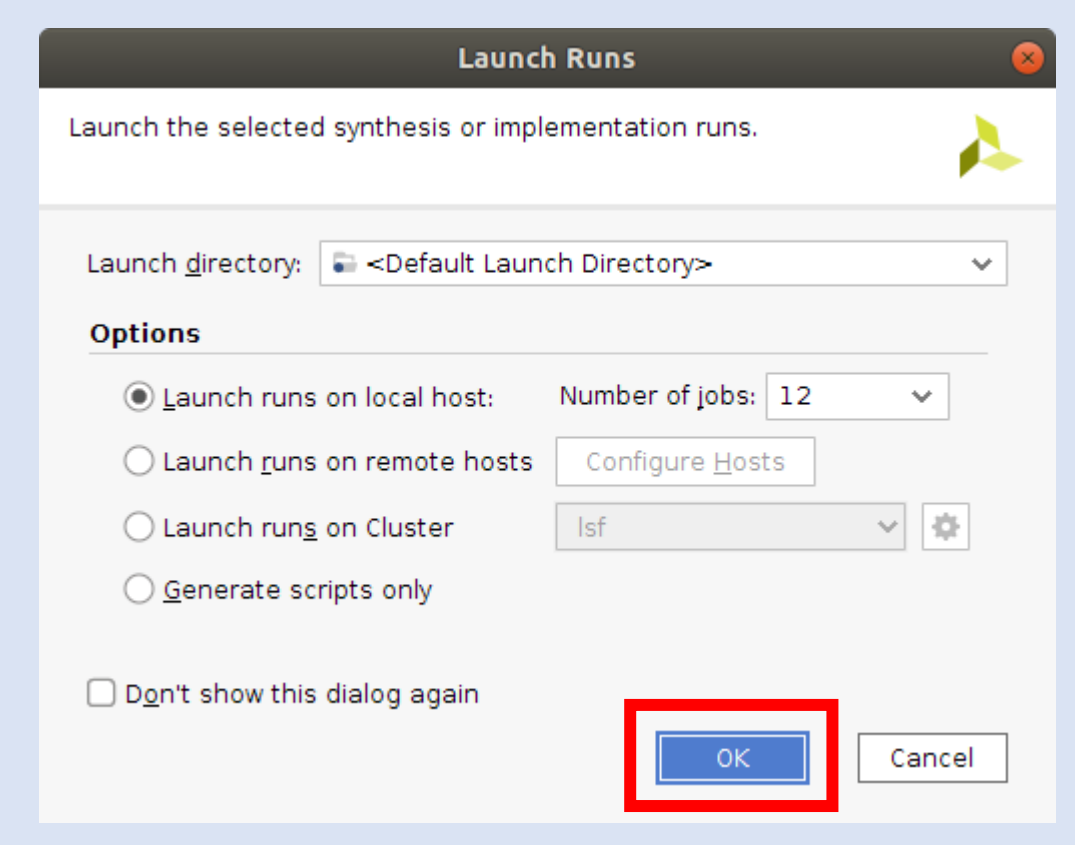
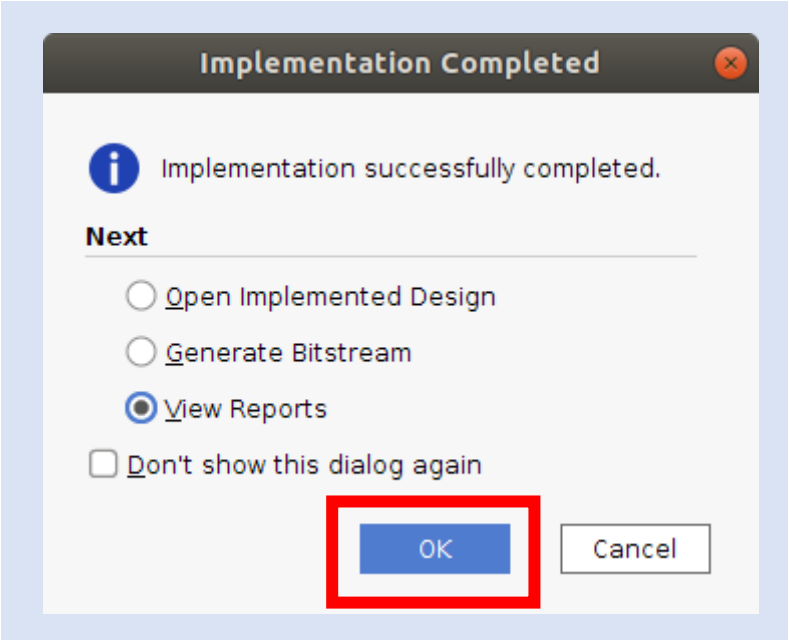
Step 36 – Click **OK** to run the implementation.



Lab 2: Intermediate Vivado

Step 37 – When the implementation completes, click **View Reports**.



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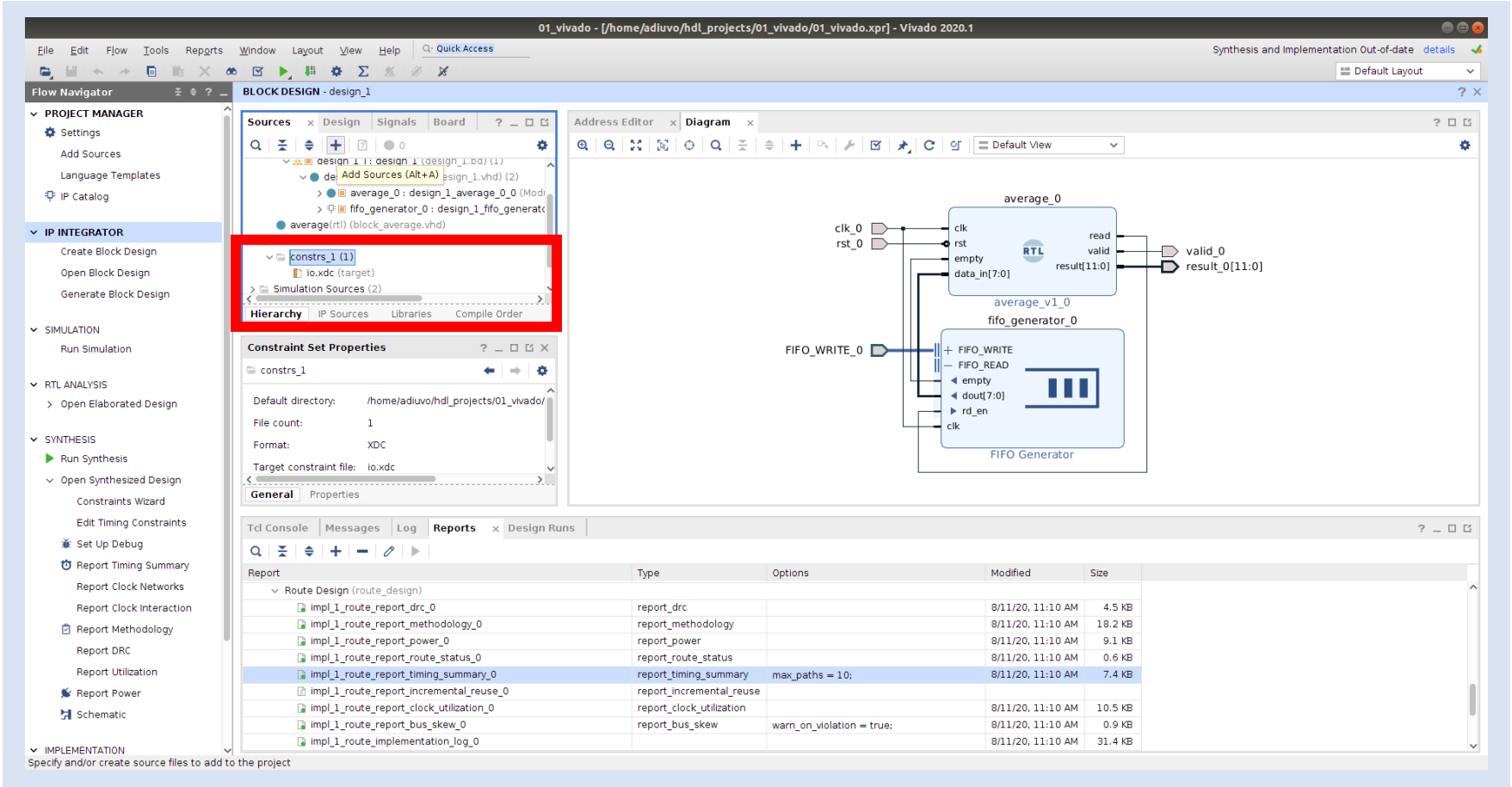
Step 38 – Select **Constraints** under Design Sources.



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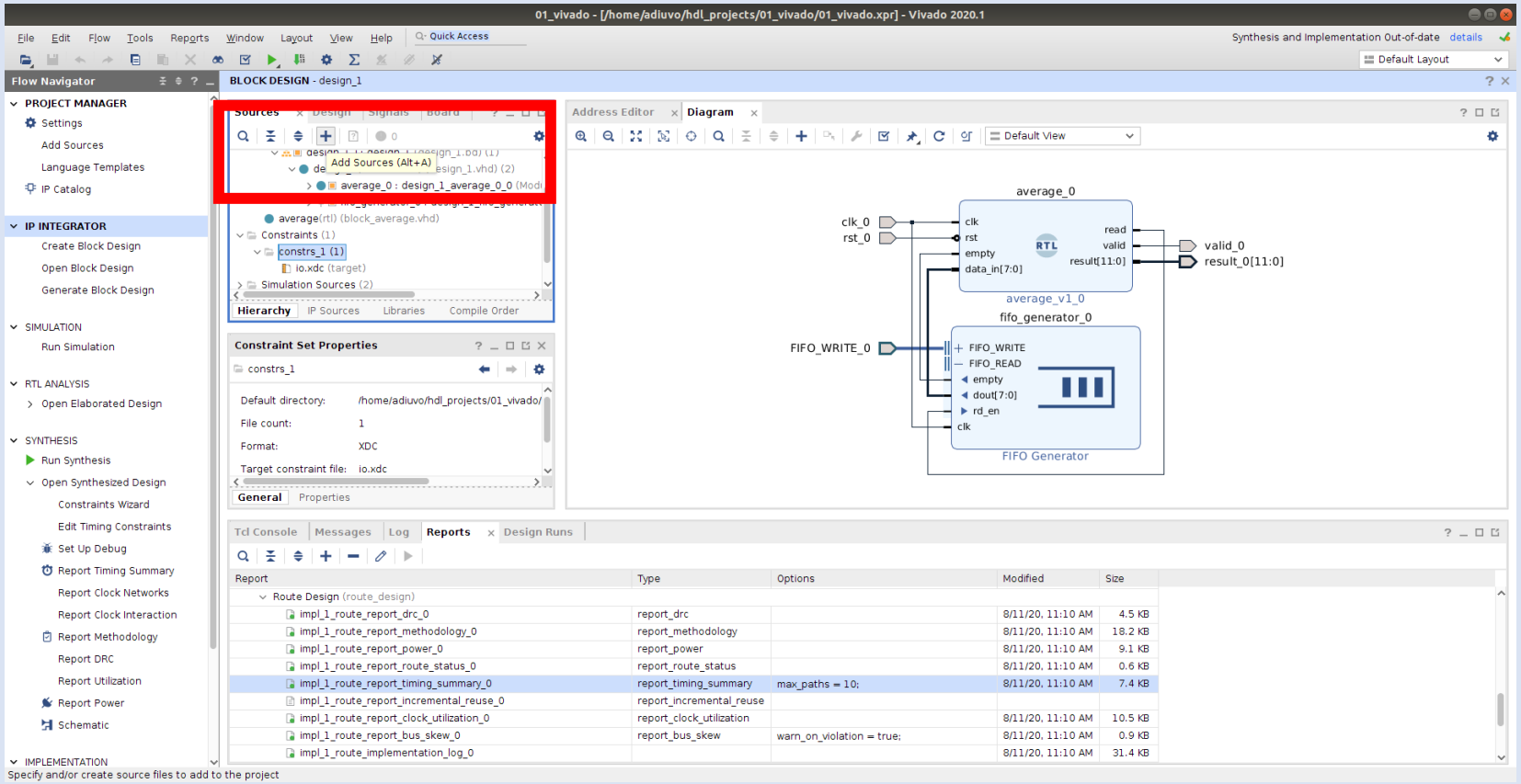
Step 39 – Click on the **Add Source** button.



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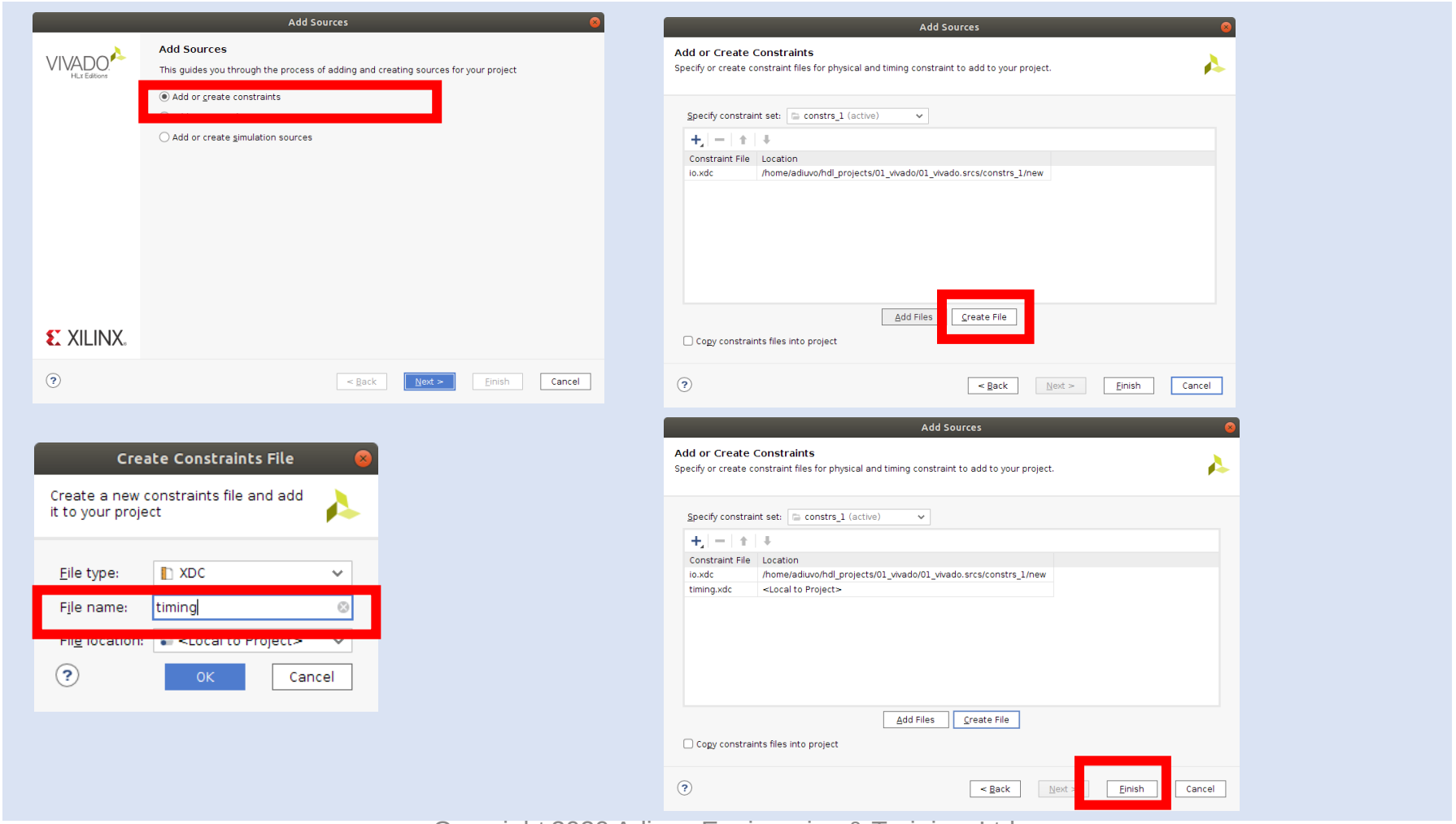
Step 40 – Select **Add or Create Constraints.** Then **Create File**, enter the name **“timing”** for the file, and click **Finish**.



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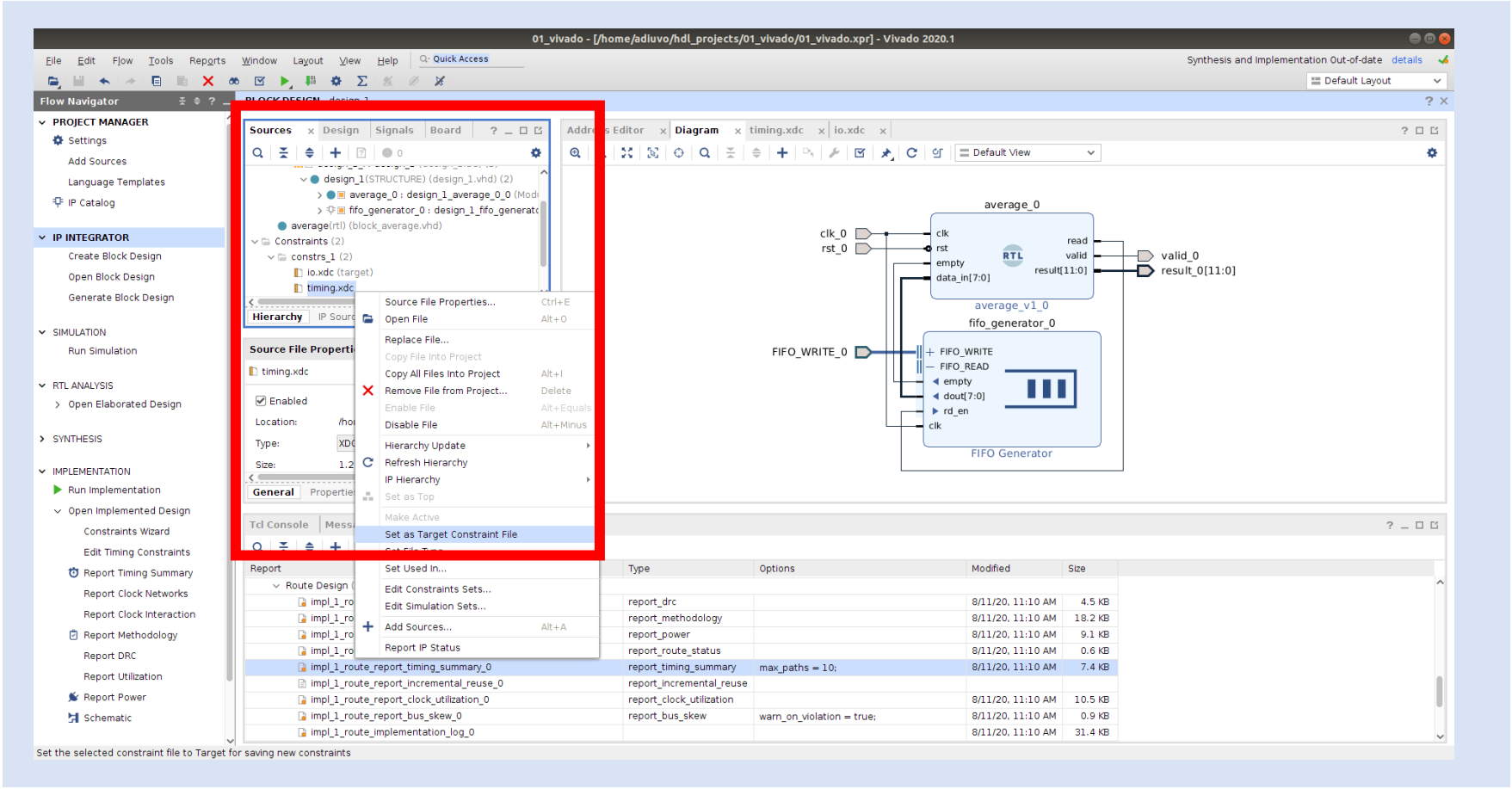
Step 41 – Right click on the newly created constraint file and select **Set as Target Constraints File**.



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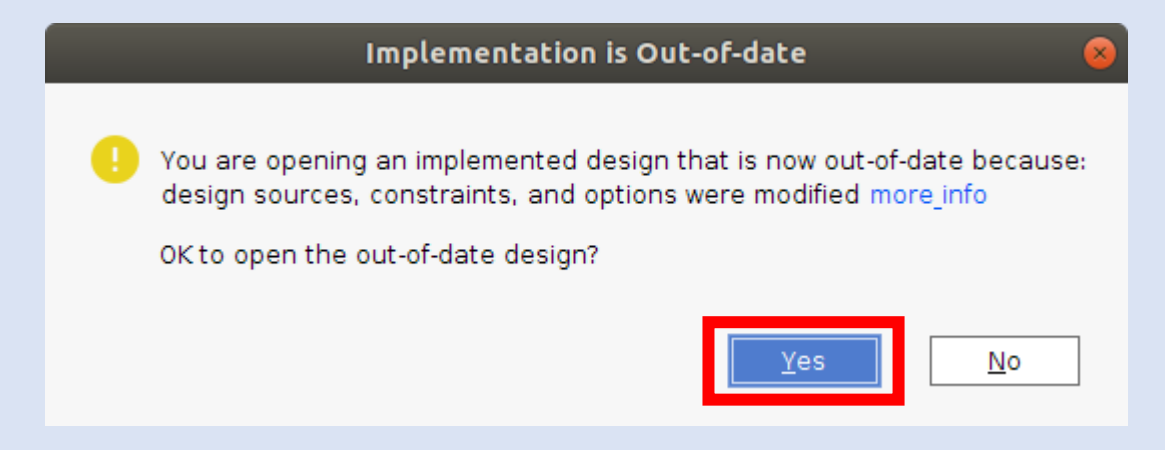
Step 42 – Open the implemented design. If you see the warning below click **OK**.



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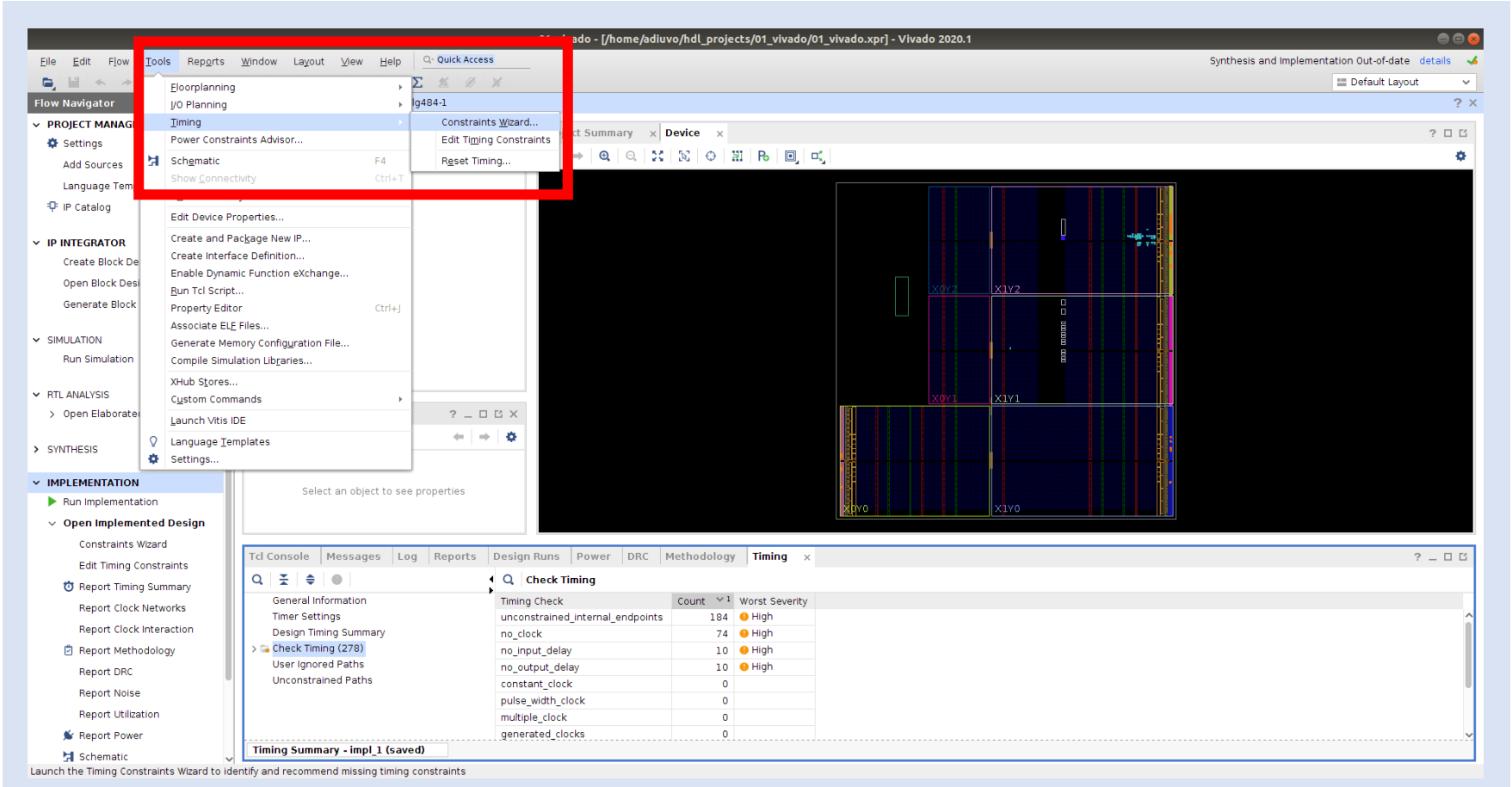
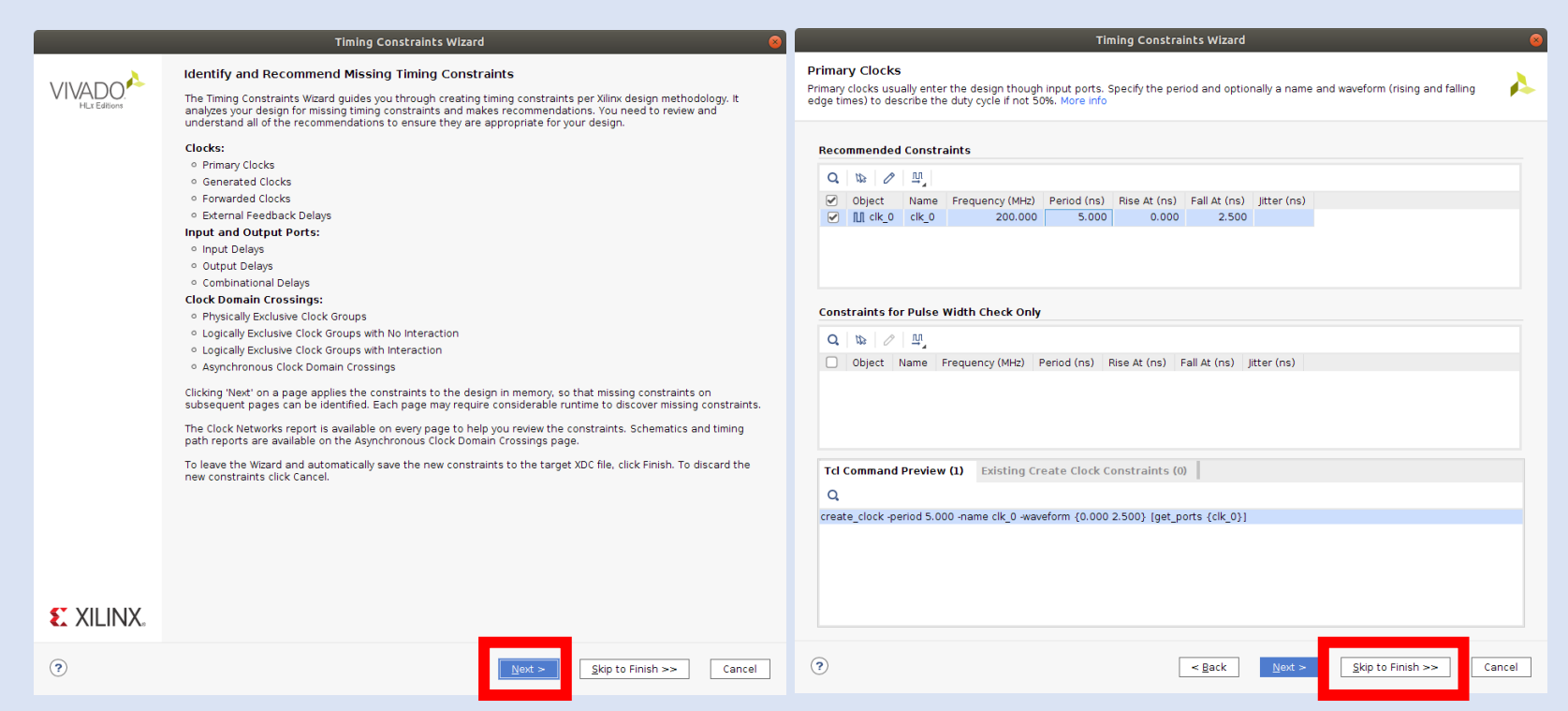
Step 43 – From the Tools menu, select **Timing** -> **Constraints Wizard**.



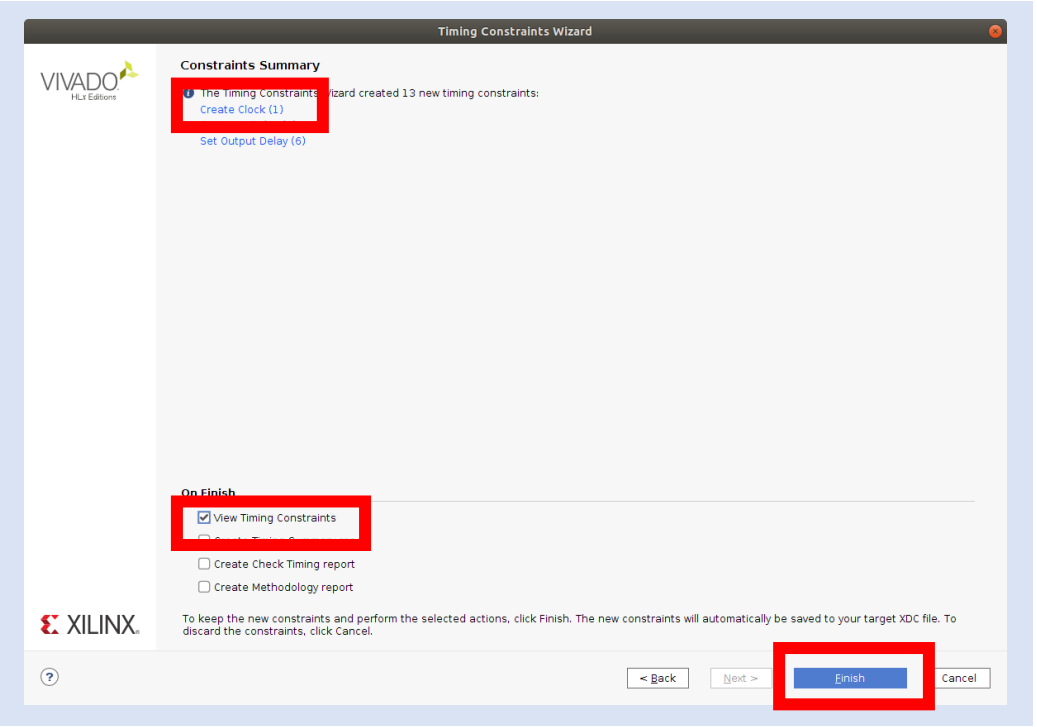
Lab 2: Intermediate Vivado

Step 44 – On the welcome screen, click **Next** and then enter **200 MHz** for the clock frequency. Once done, select **Skip to Finish**.



Lab 2: Intermediate Vivado

Step 45 – On the final page, check that only one constraints is being created, check the **View Timing Constraints,** and click **Finish**.



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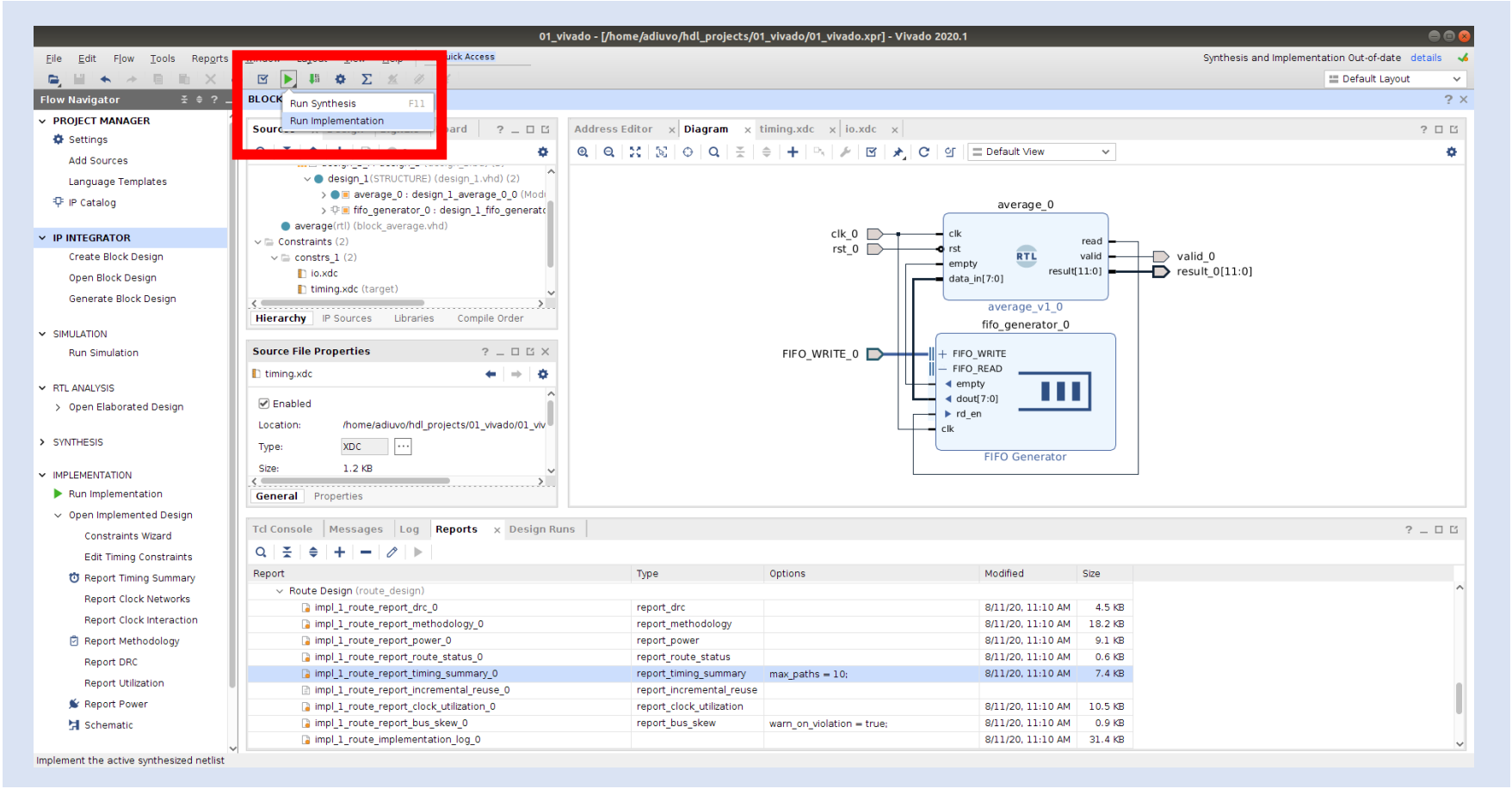
Step 46 – Close the implementation view and **rerun the implementation**. Click **OK** on any dialogs which pop up prior to implementation starting.



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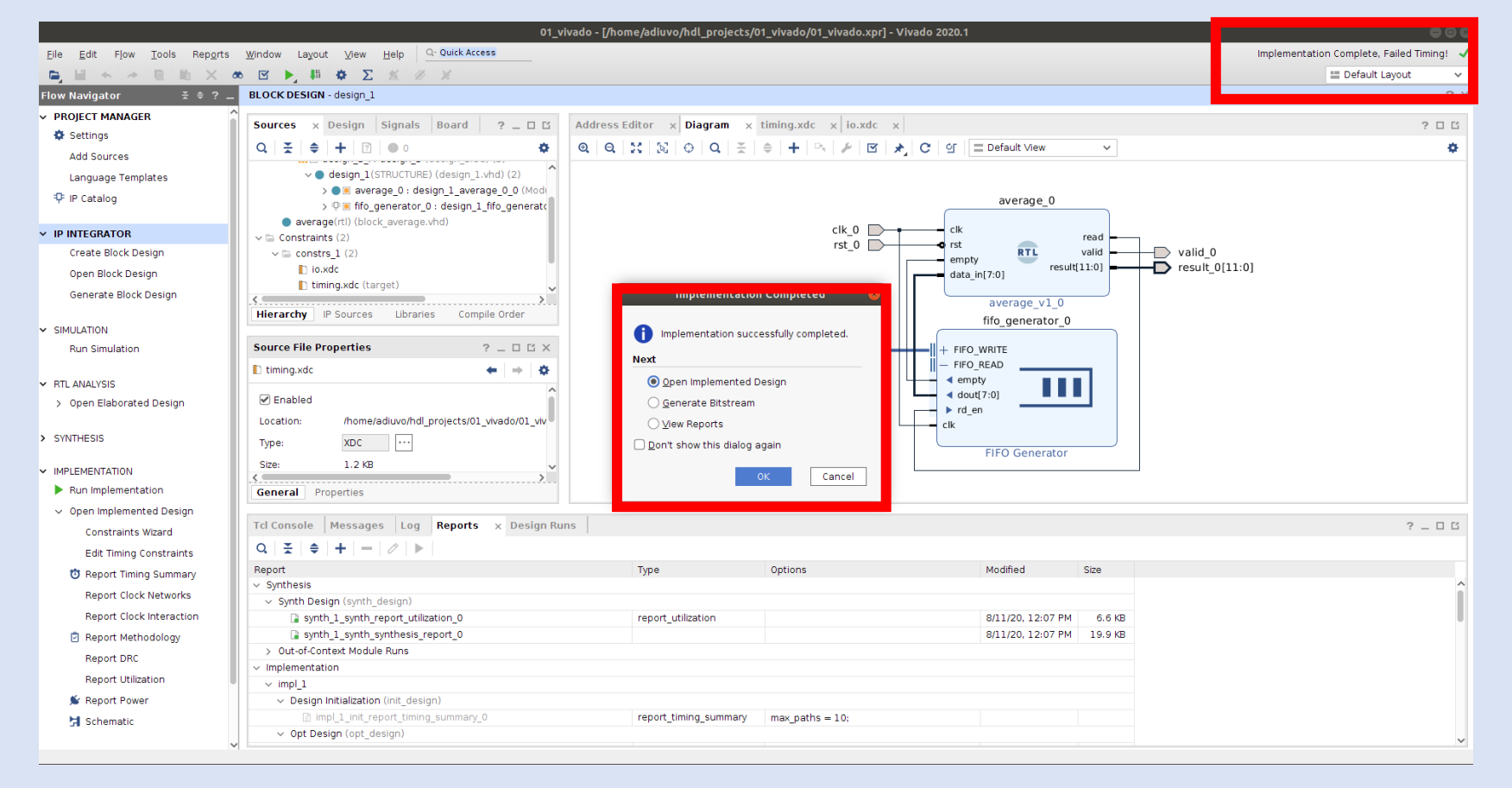
Step 47 – Once the implementation completes, Timing will fail. Open the **Implemented Design**.



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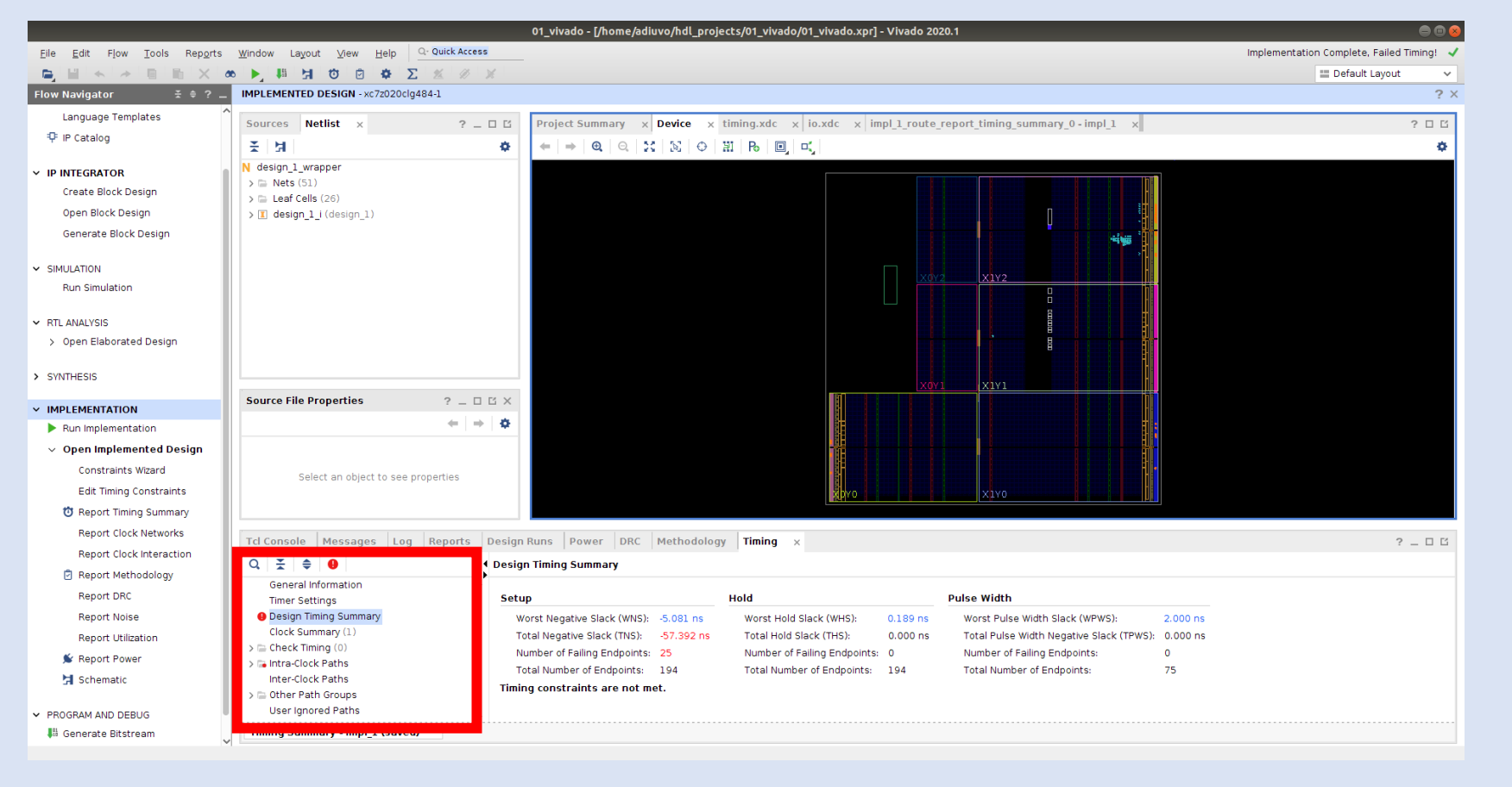
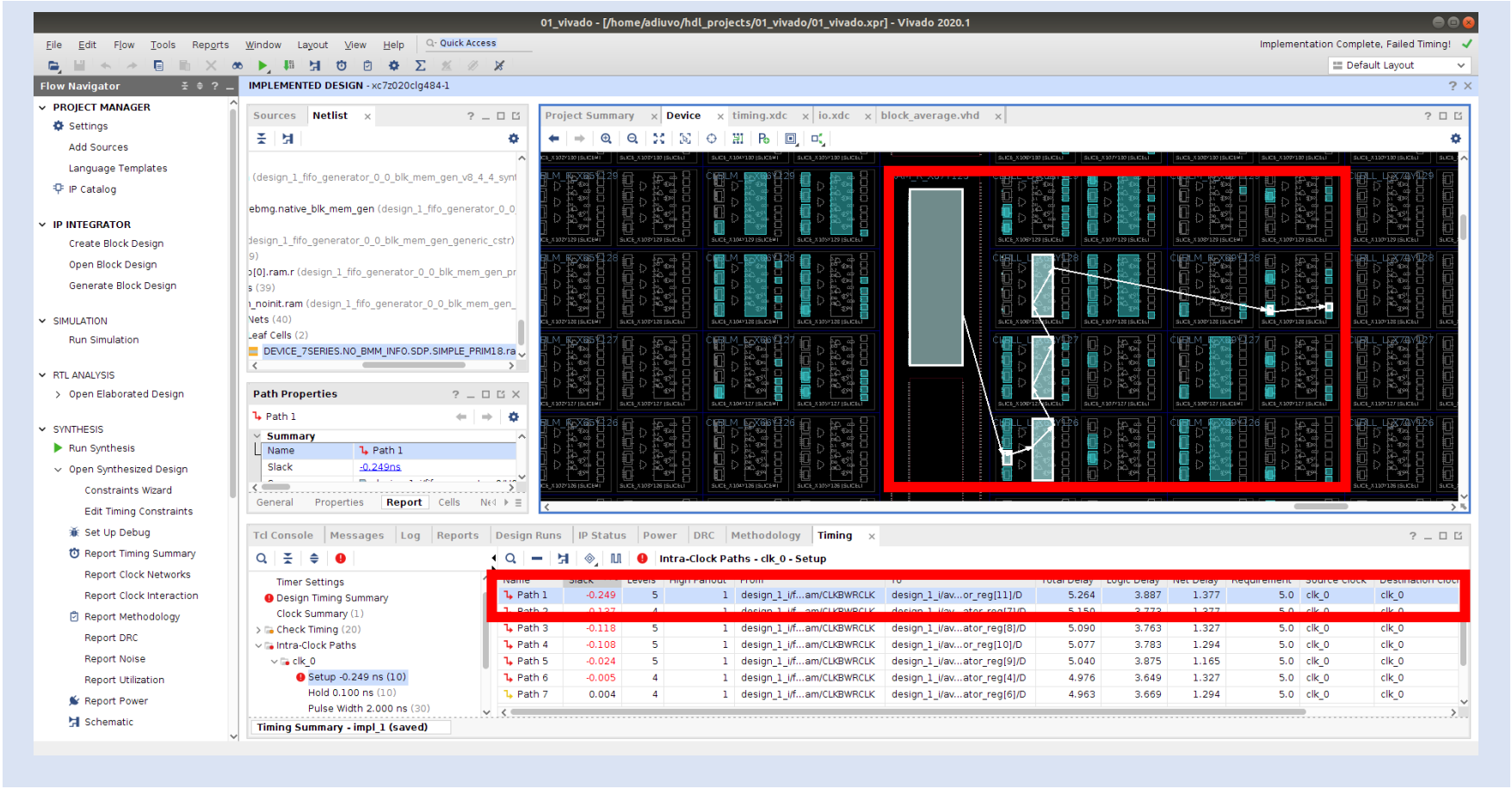
Step 48 – In the implemented design, select the failing **Intra-Clock Paths**.



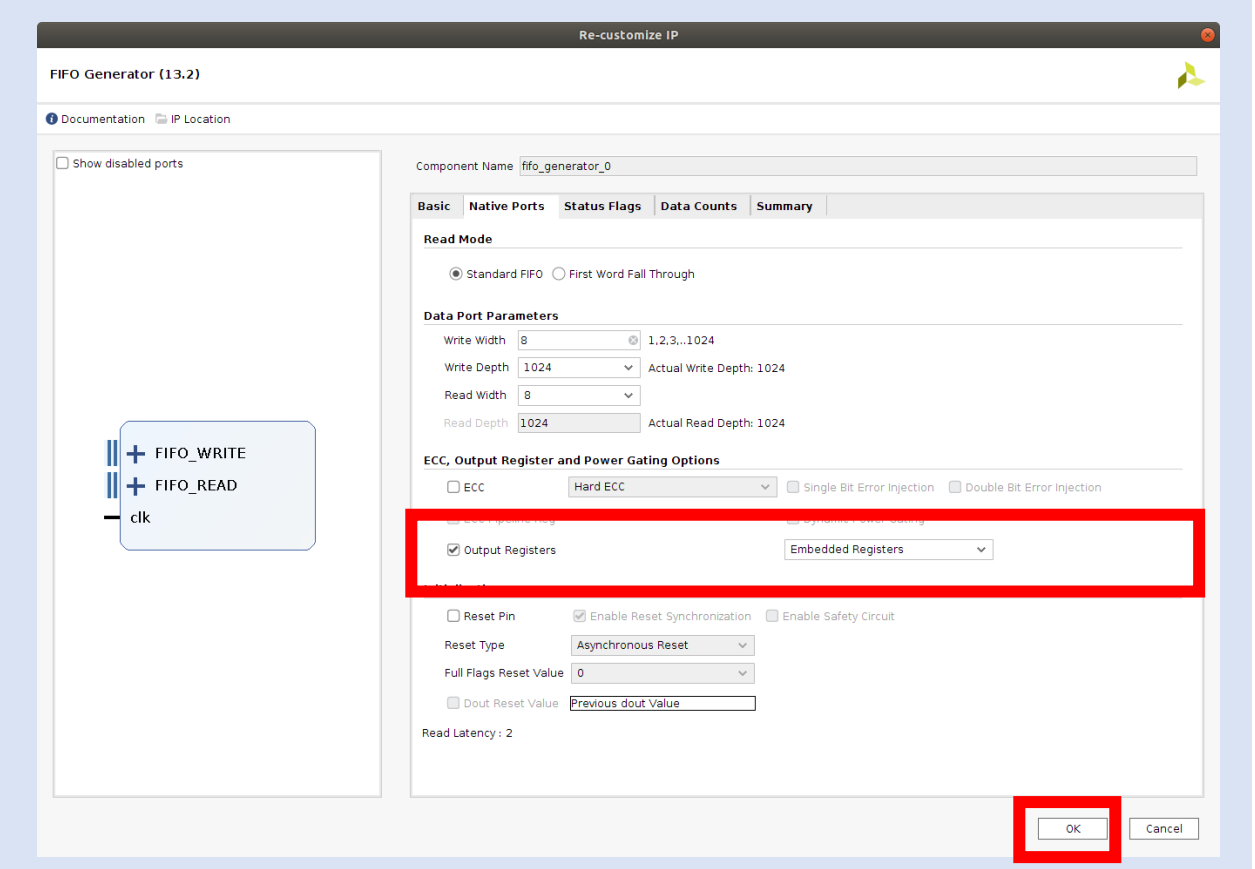
Lab 2: Intermediate Vivado

Step 49 – Select **Path 1** and zoom in. You will see that the FIFO output data passes through LUTs before finally being registered. This path is too long for timing at 200 MHz.



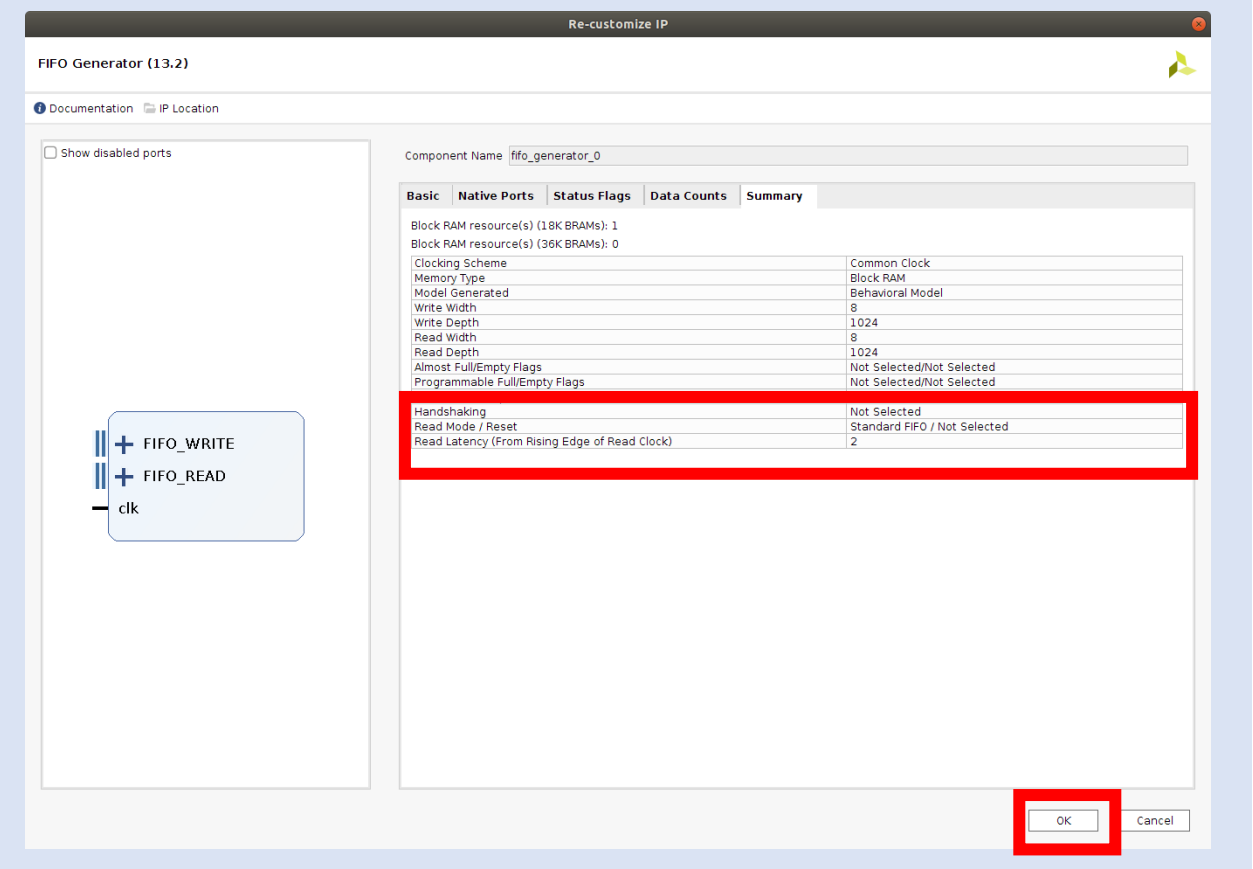
Lab 2: Intermediate Vivado

Step 50 – To fix this, we need to register the output of the FIFO. Close the implementation view and reopen the block diagram. Double click on the **FIFO** to customize.



Lab 2: Intermediate Vivado

Step 51 – Note the latency has changed from 1 to 2 clocks. We would need to correct for this in the average block, however, we proceed assuming that we have.



Lab 2: Intermediate Vivado

Step 52 – Reimplement the design. When the timing is completed, you should see that the implementation is correct and the timing is met.