Getting to Know Vivado

Course Workbook

Table of Contents

About this Workbook

This workbook is designed to be used in conjunction with the Getting to Know Vivado course.

The contents of this workbook are created by Adiuvo Engineering & Training, Ltd.

If you have any questions about the contents or need assistance, please contact Adam Taylor at adam@adiuvoengineering.com.

Pre-Lab

Workshop Pre-requisites

Required Hardware

There is no required hardware for this course.

Downloads and Installations

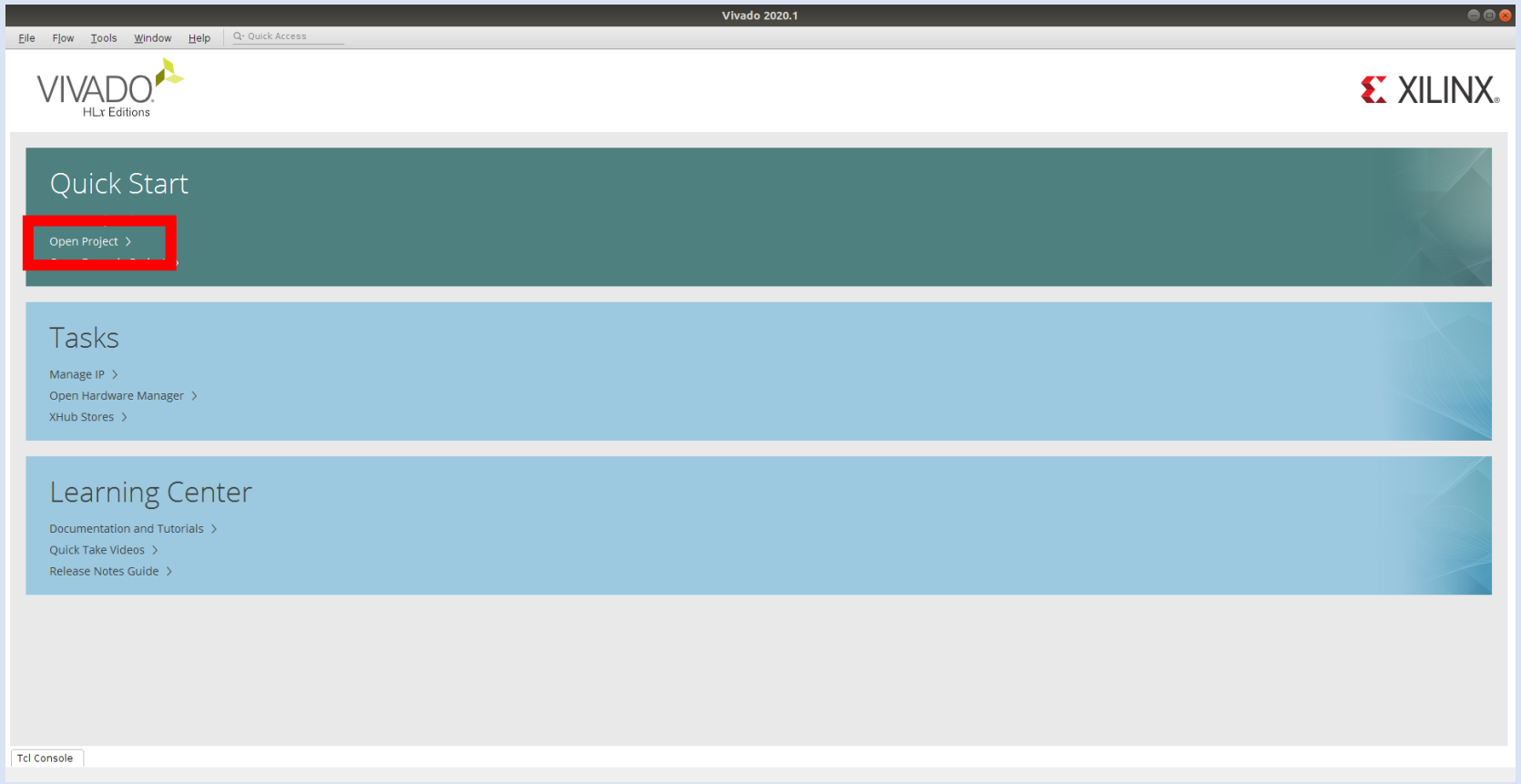
Step 1 – Download and install the following at least one day prior to the workshop. This may take a significant amount of time and drive space.

Vivado 2020.1	Download
Source Project Files	Download
Lab 2 must be completed	

Lab 3
Advanced Vivado

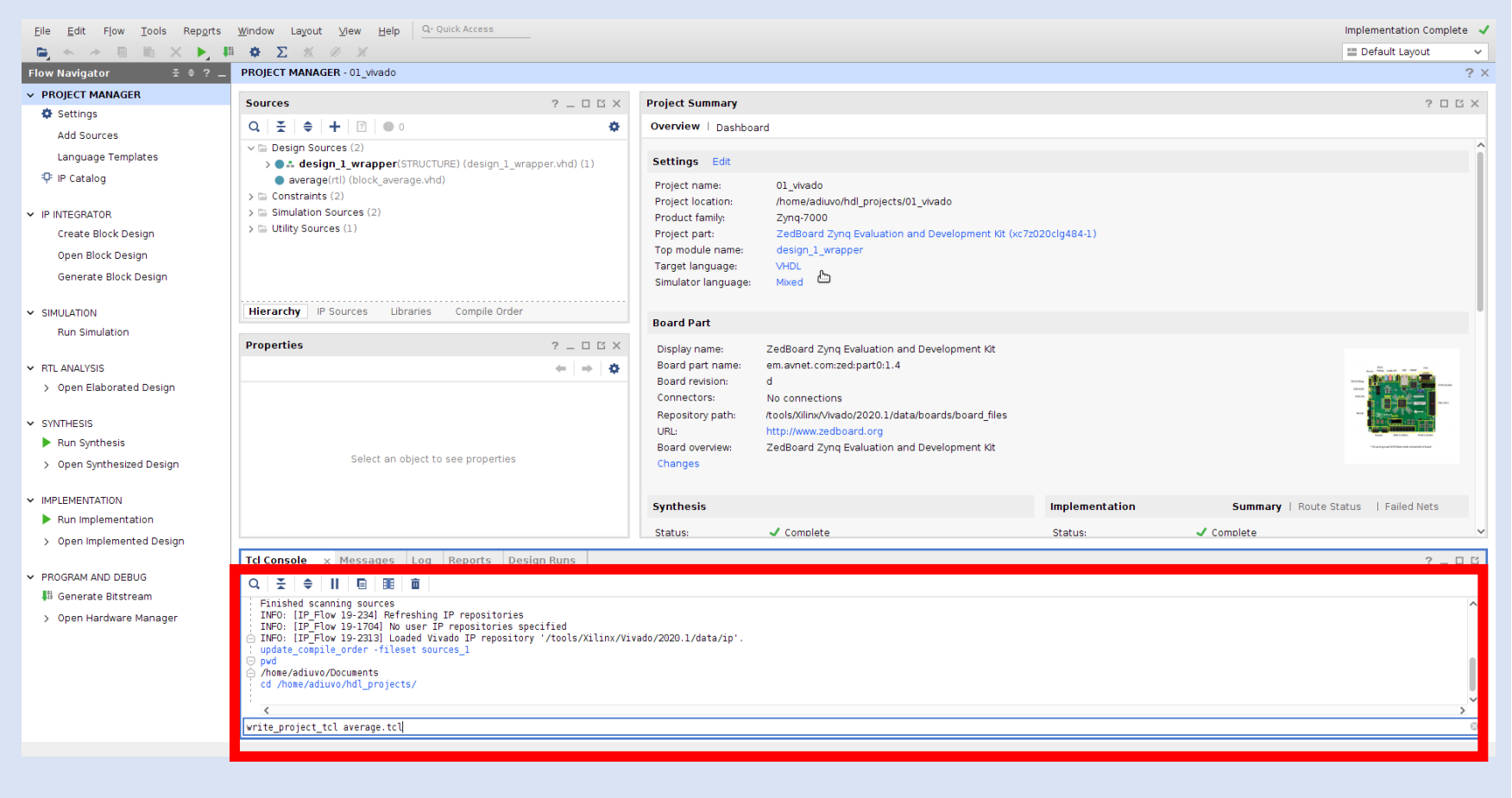
Lab 3: Advanced Vivado

Step 1 – Open the project created in part two.



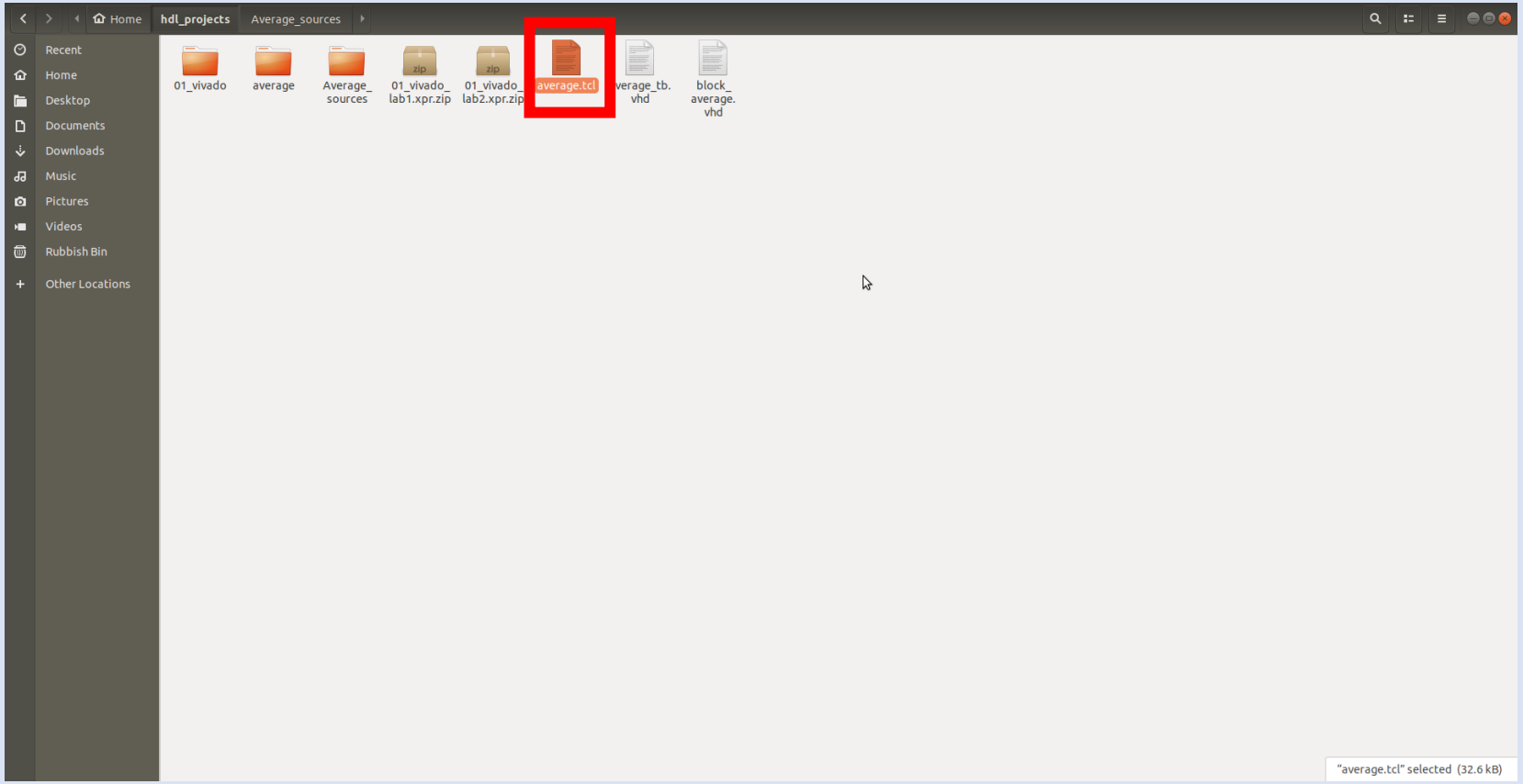
Lab 3: Advanced Vivado

Step 2 – In the TCL window, check the PWD and change directory to the location containing your project. Then enter the command `write_project_tcl average.tcl`.



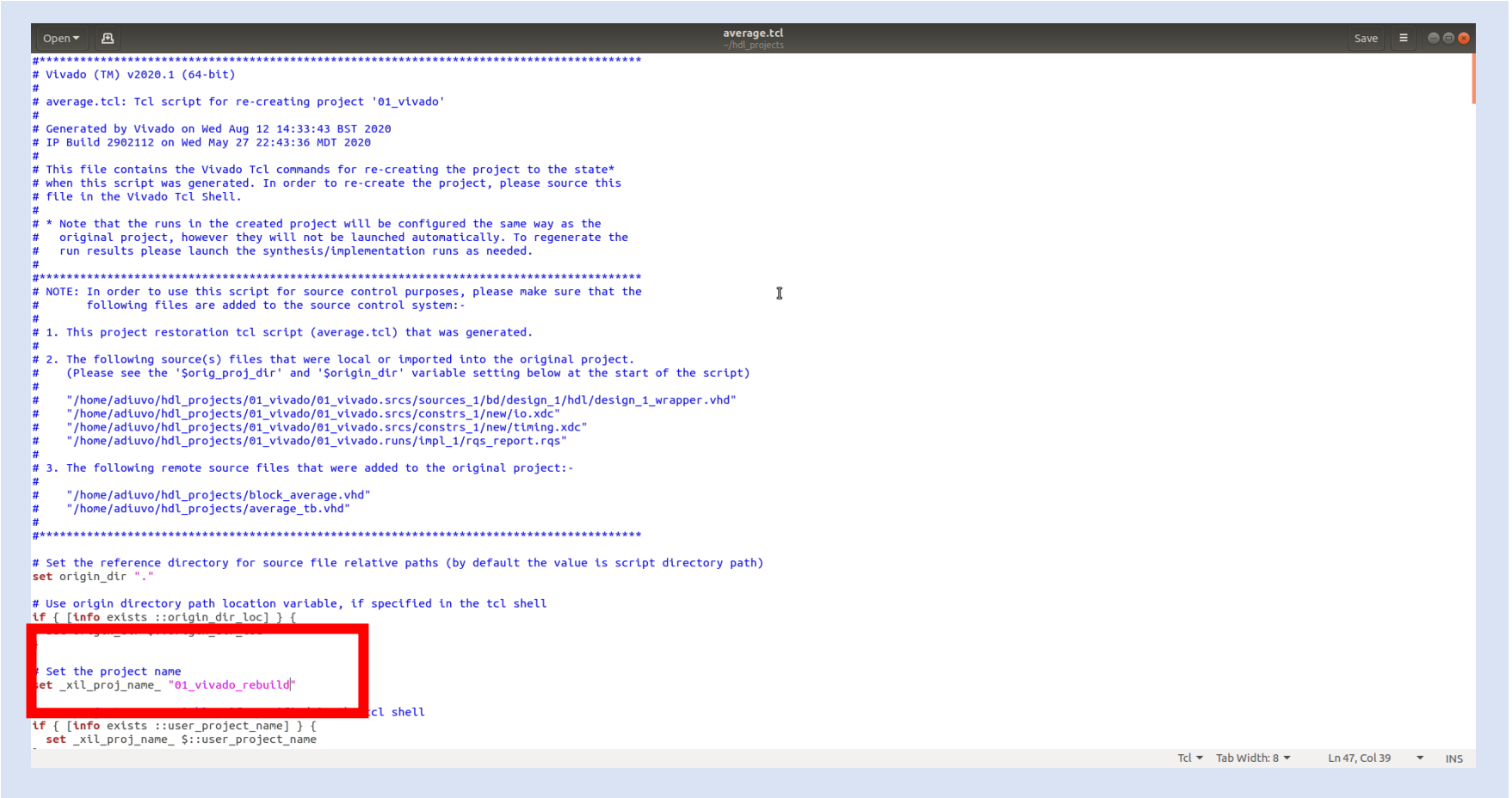
Lab 3: Advanced Vivado

Step 3 – This will write a project description in TCL to the project directory.



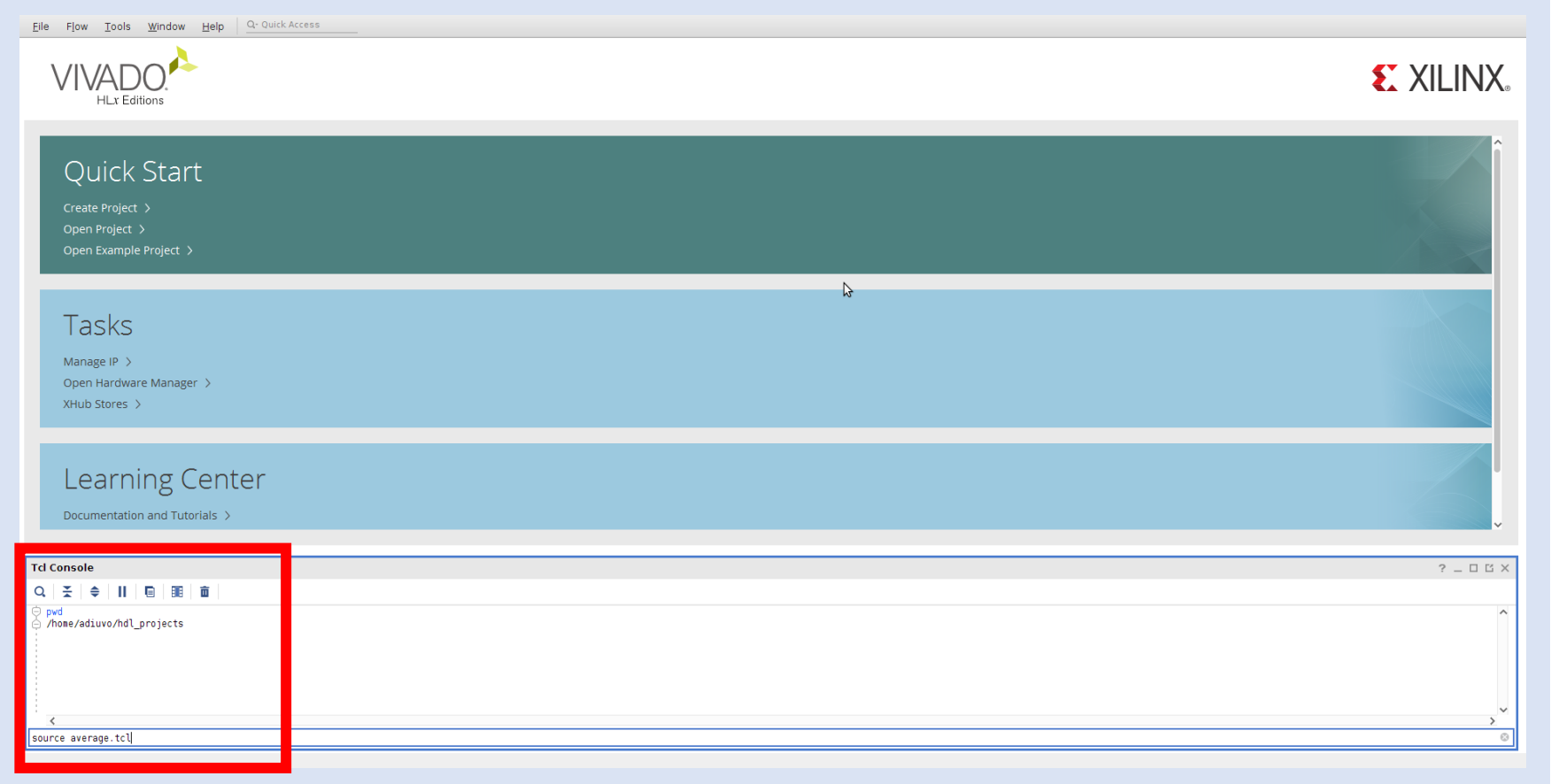
Lab 3: Advanced Vivado

Step 4 – Open the TCL file and change the project name from **01_Vivado** to **01_Vivado_rebuild**.



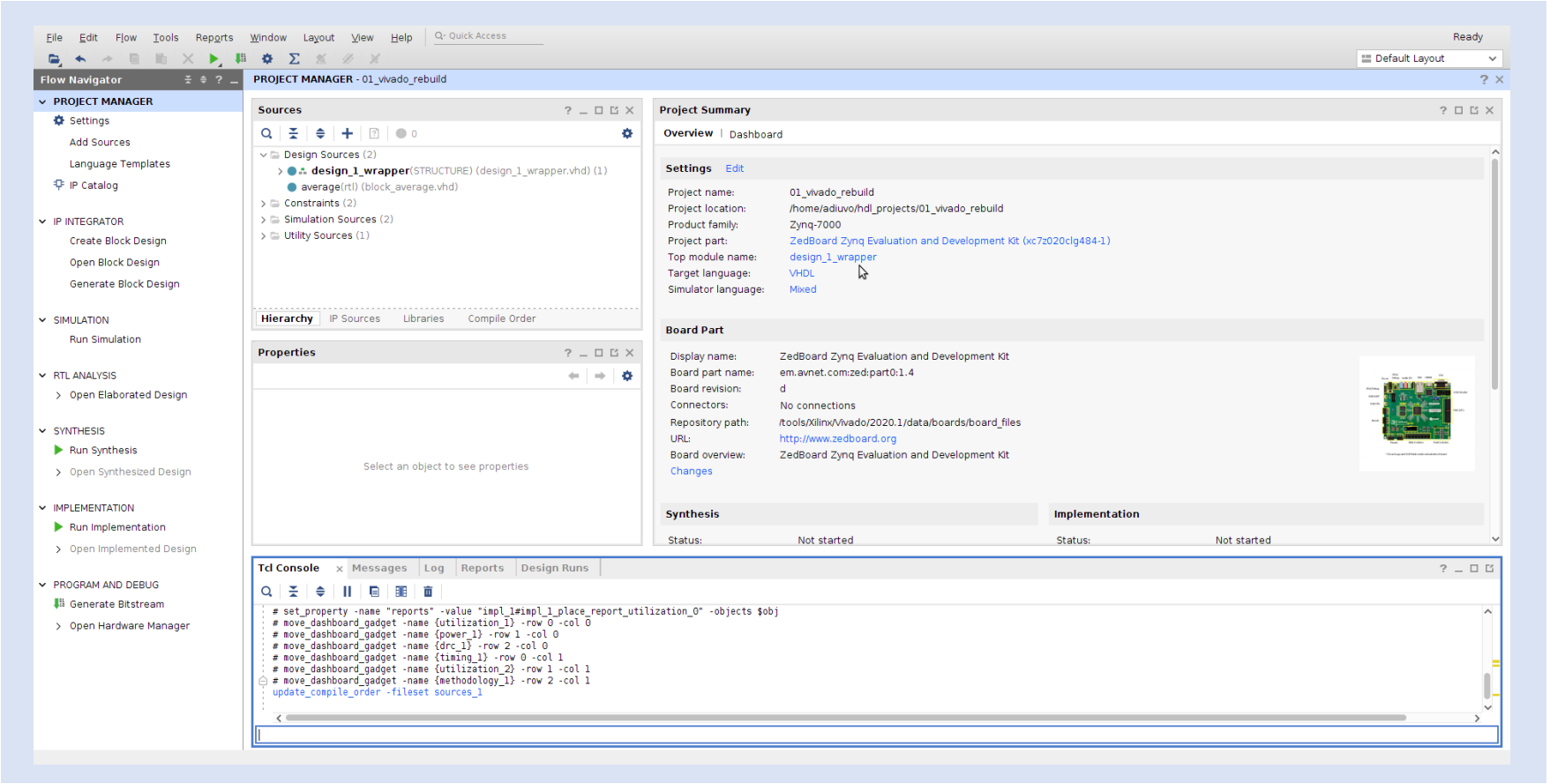
Lab 3: Advanced Vivado

Step 5 – Close the current project and type `source average.tcl`. in the TCL window.



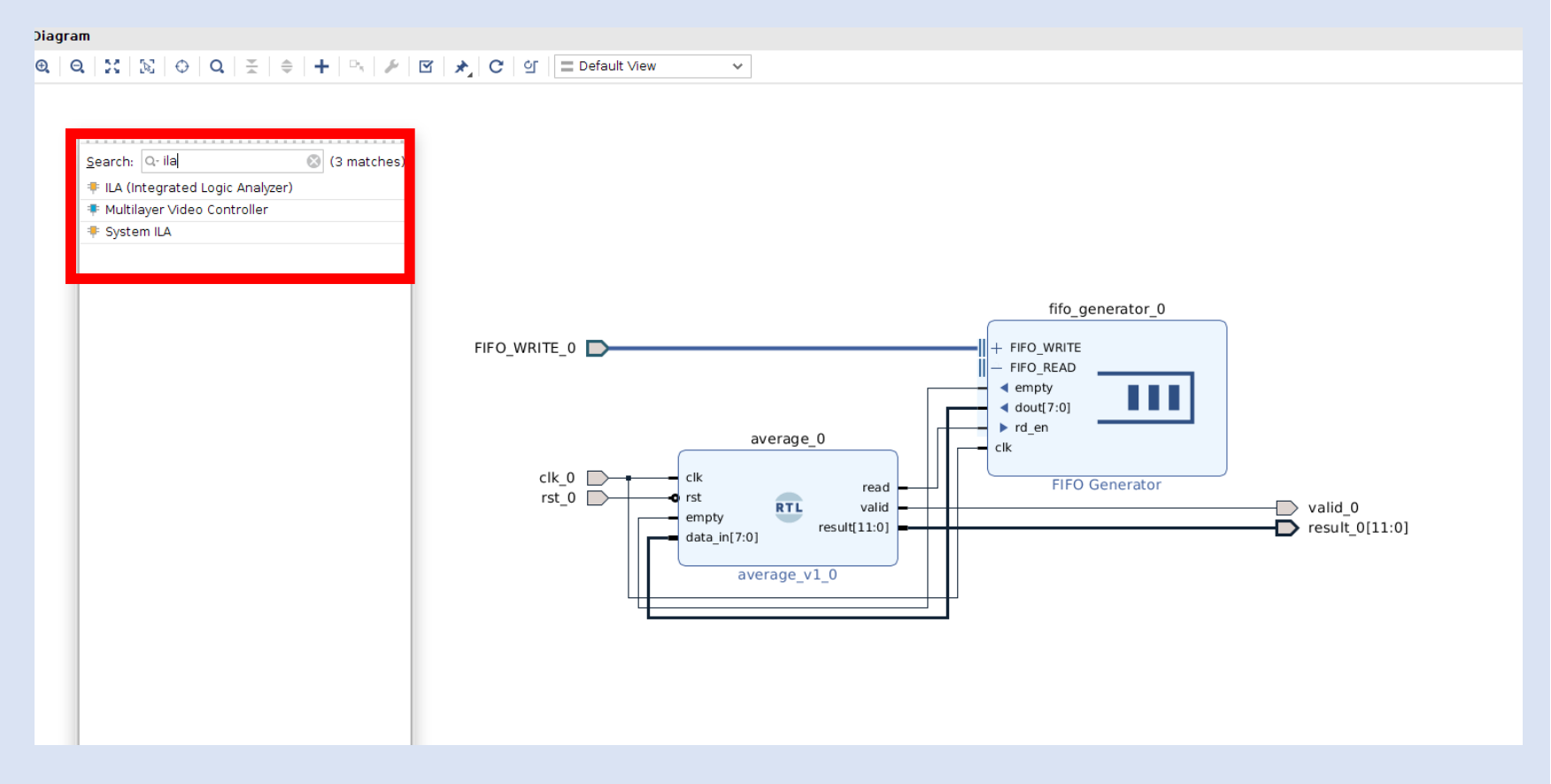
Lab 3: Advanced Vivado

Step 6 – This will rebuild the project exactly as before from the TCL file.



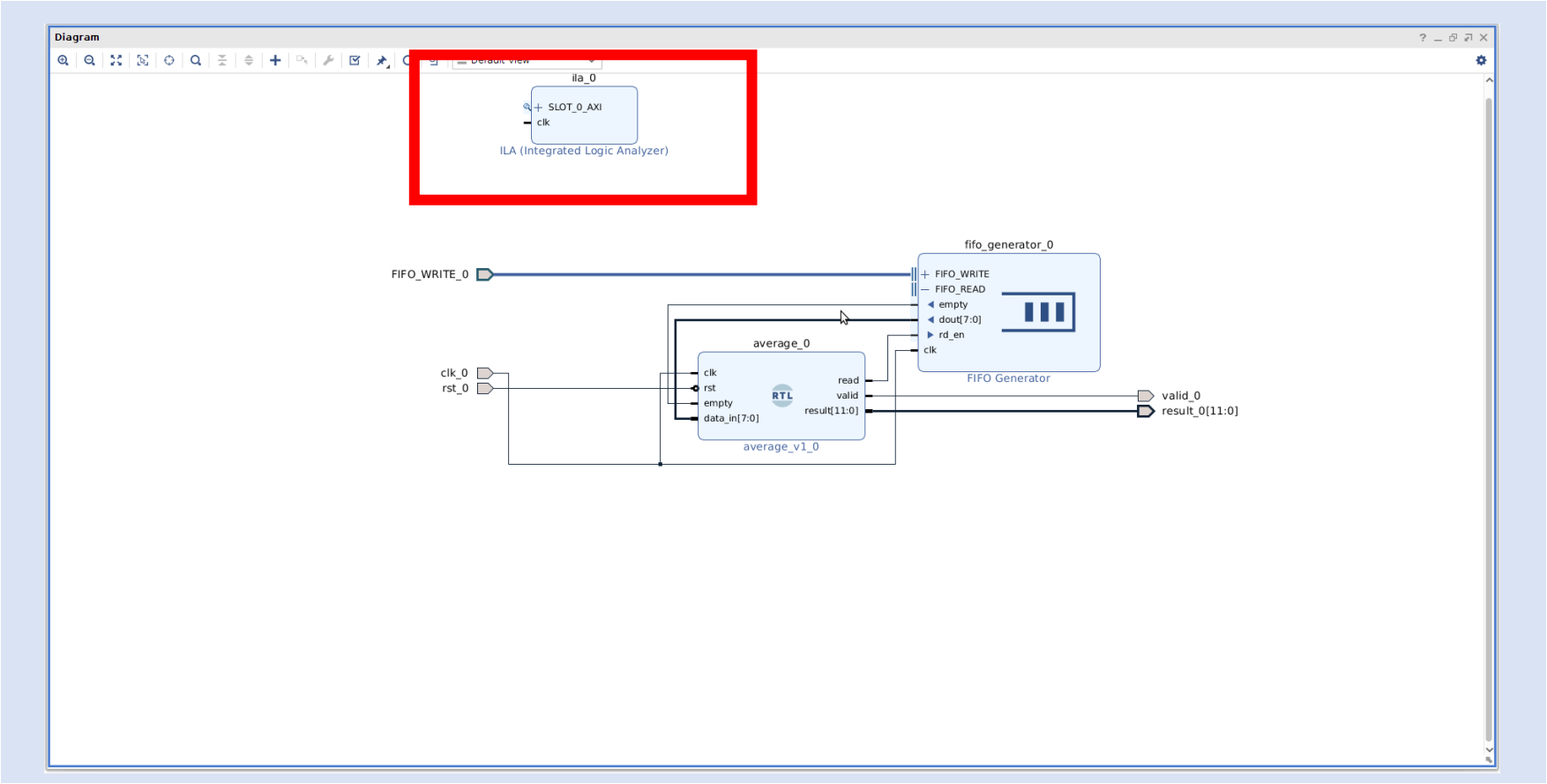
Lab 3: Advanced Vivado

Step 7 – Open the block design and click on the **+ symbol** to add in IP. In the search bar, enter **ILA** and then double click on the **ILA (Integrated Logic Analyzer)** to add in the IP core.



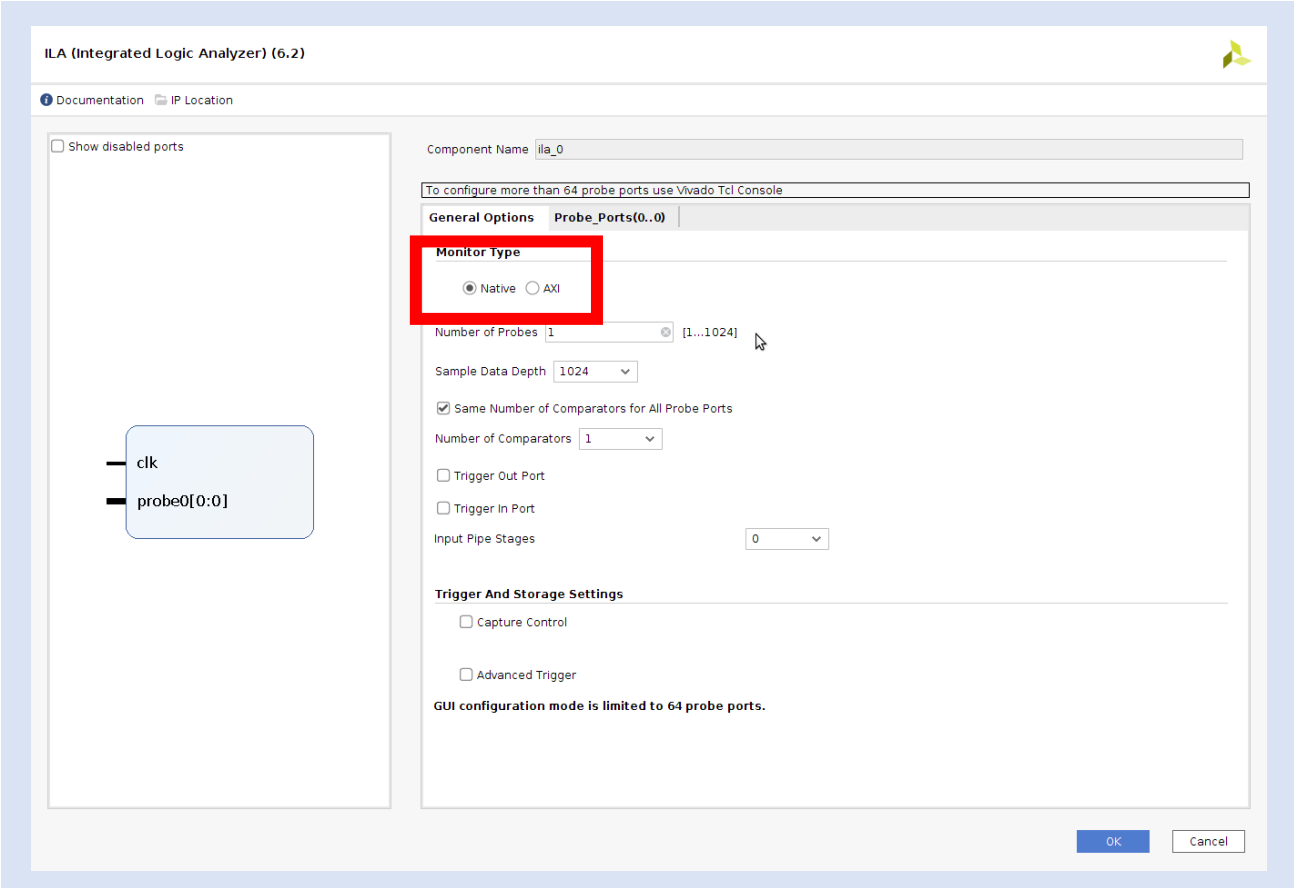
Lab 3: Advanced Vivado

Step 8 – Double click on the **ILA** to customize it.



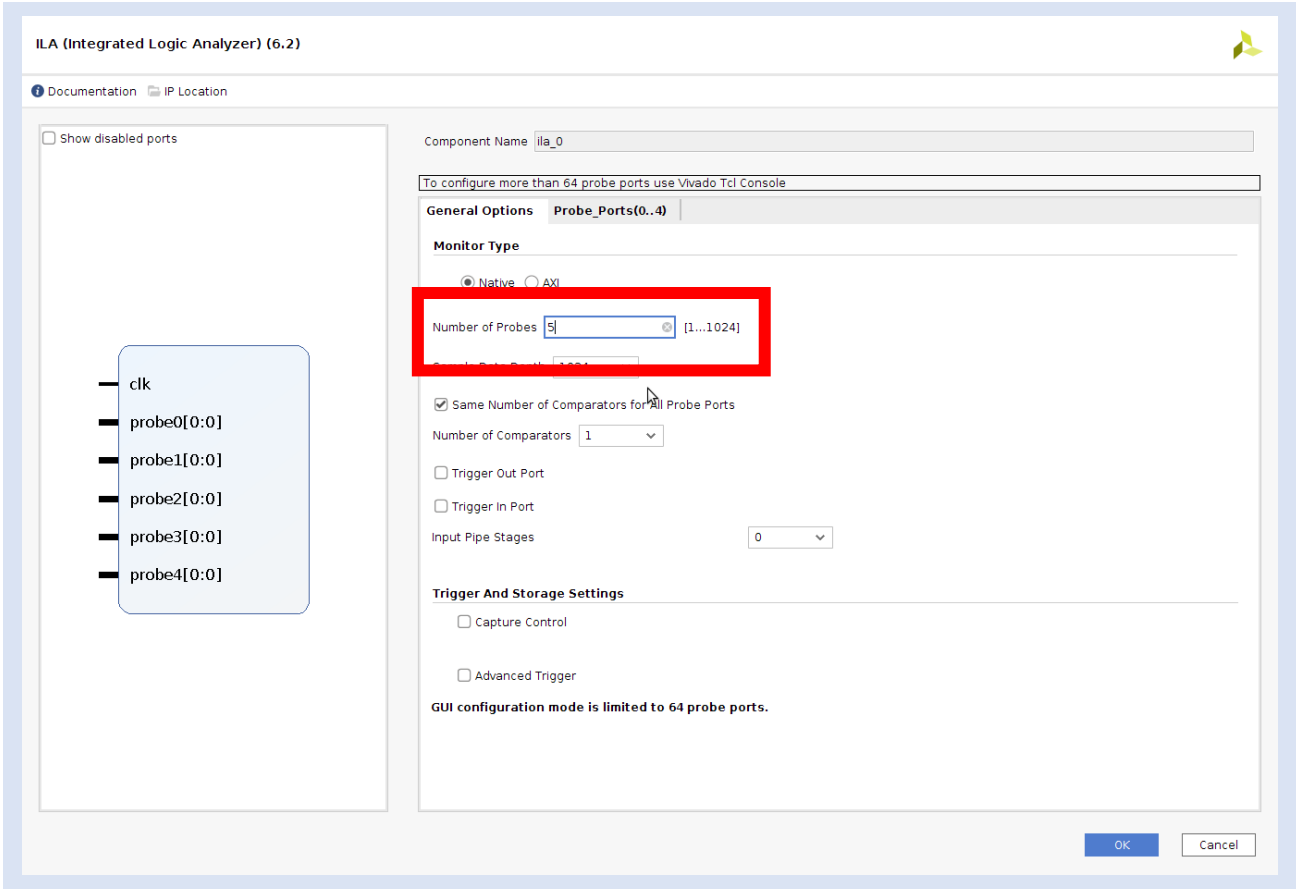
Lab 3: Advanced Vivado

Step 9 – Change the monitor type to **Native**.



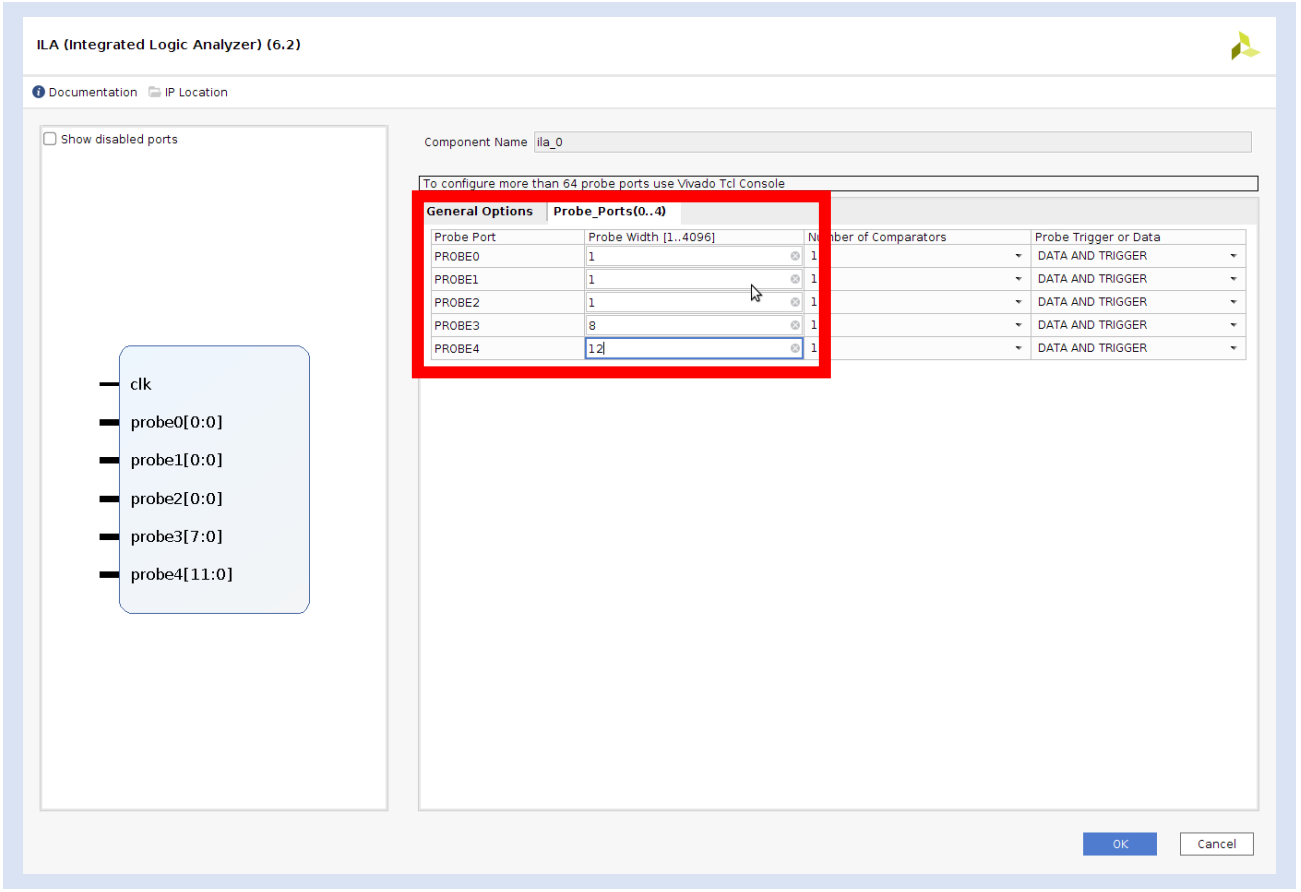
Lab 3: Advanced Vivado

Step 10 – Set the number of probes to **5**.



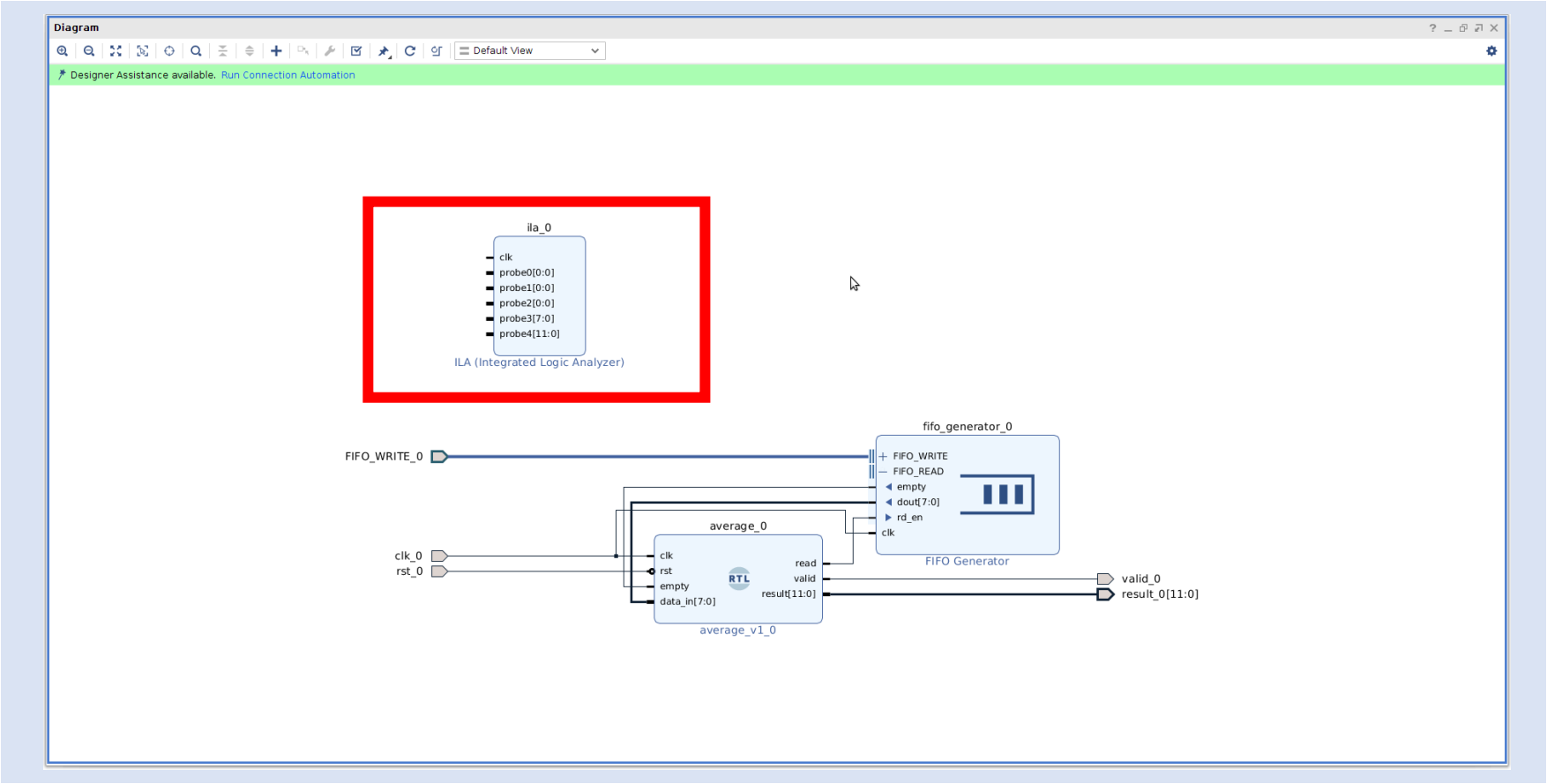
Lab 3: Advanced Vivado

Step 11 – Click on the **Probe Ports Tab** and set the widths of **PROBE3 to 8** and **PROBE4 to 12**, click **OK**.



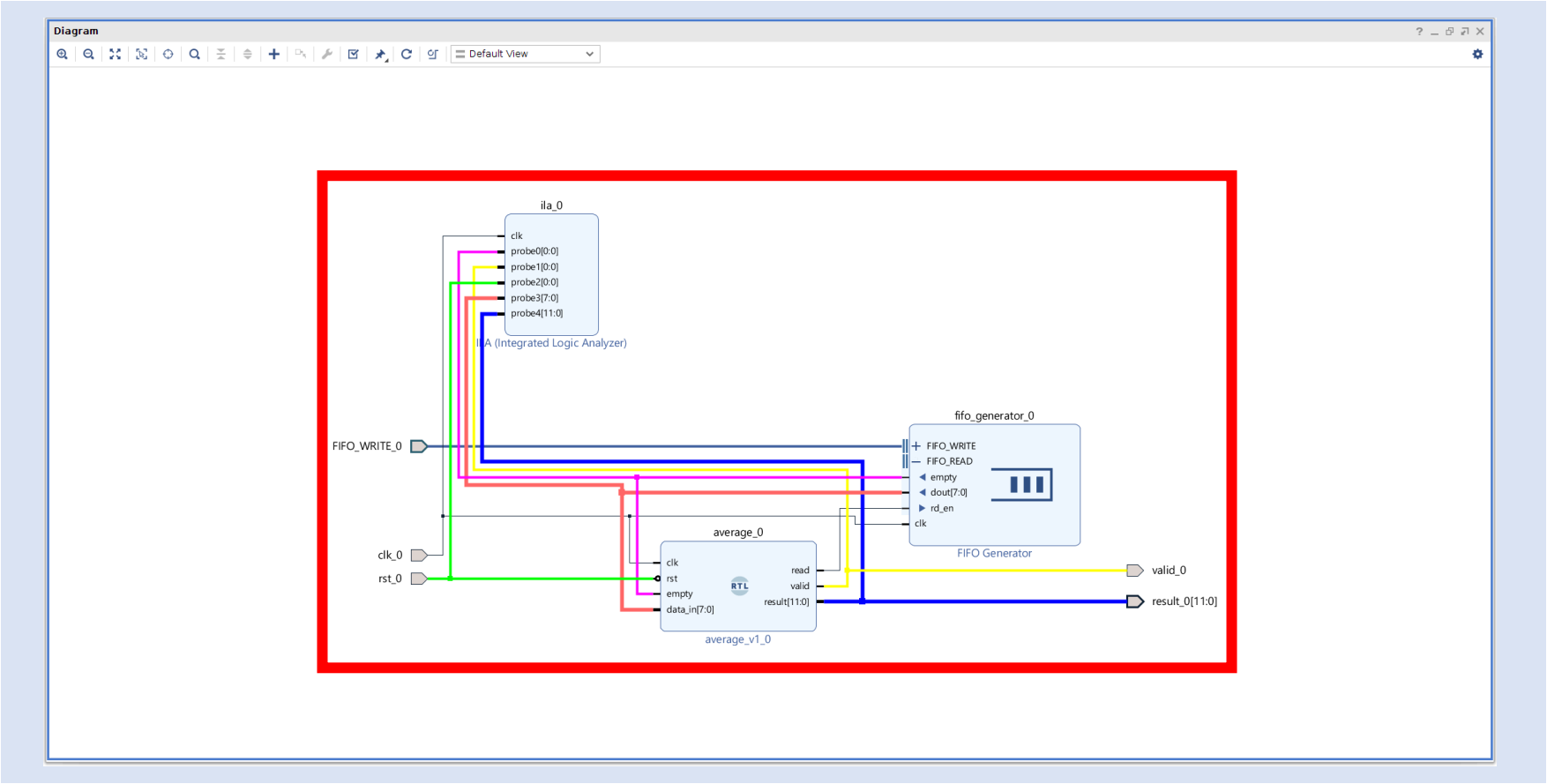
Lab 3: Advanced Vivado

Step 12 – The block diagram should now show the ILA with five ports and a clock input.



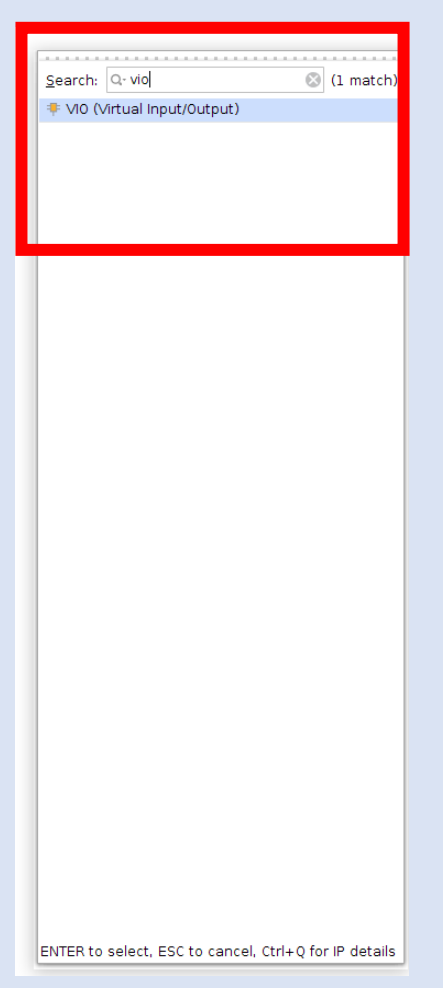
Lab 3: Advanced Vivado

Step 13 – Connect up the ILA as shown below. This will provide us visibility of all input and output of the average block.



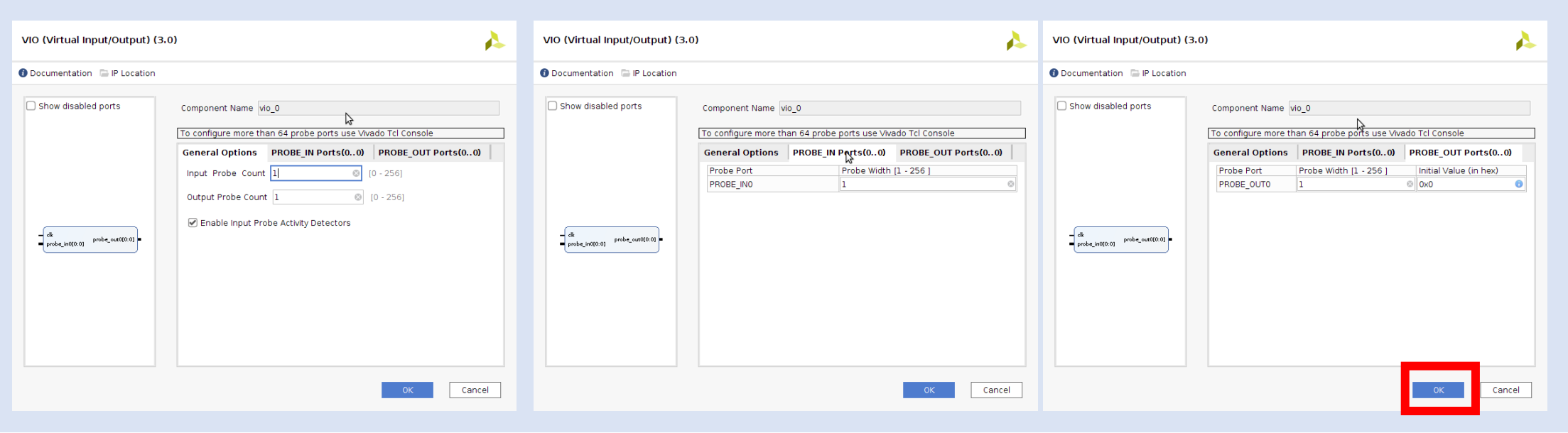
Lab 3: Advanced Vivado

Step 14 – Click on the **+ symbol** to add in IP and type **VIO** in the search box. Double click on the **VIO symbol**.



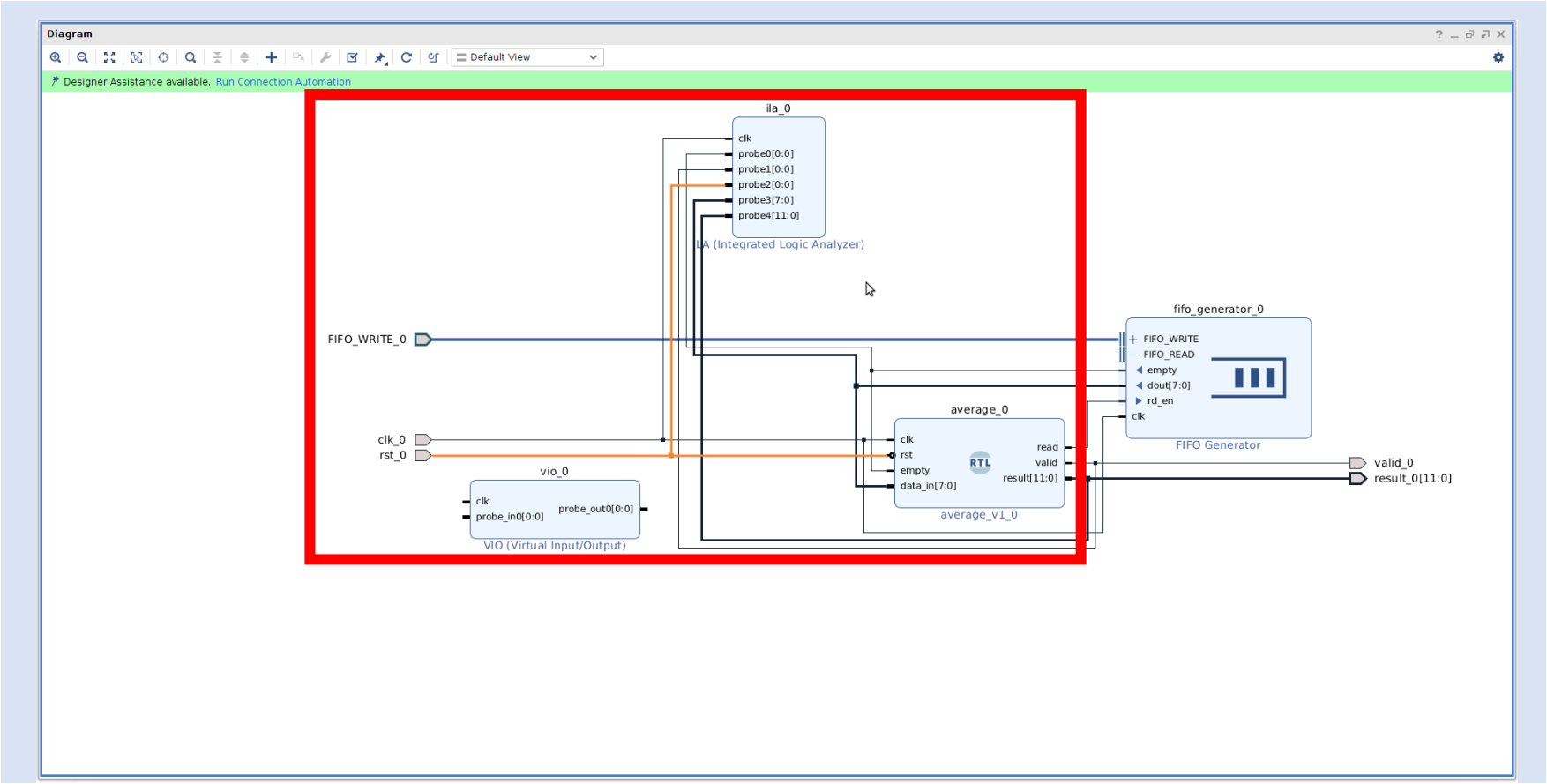
Lab 3: Advanced Vivado

Step 15 – When the VIO is added onto the block diagram, double click it to customize and explore the three tabs. Leave it all unchanged and click **OK**.



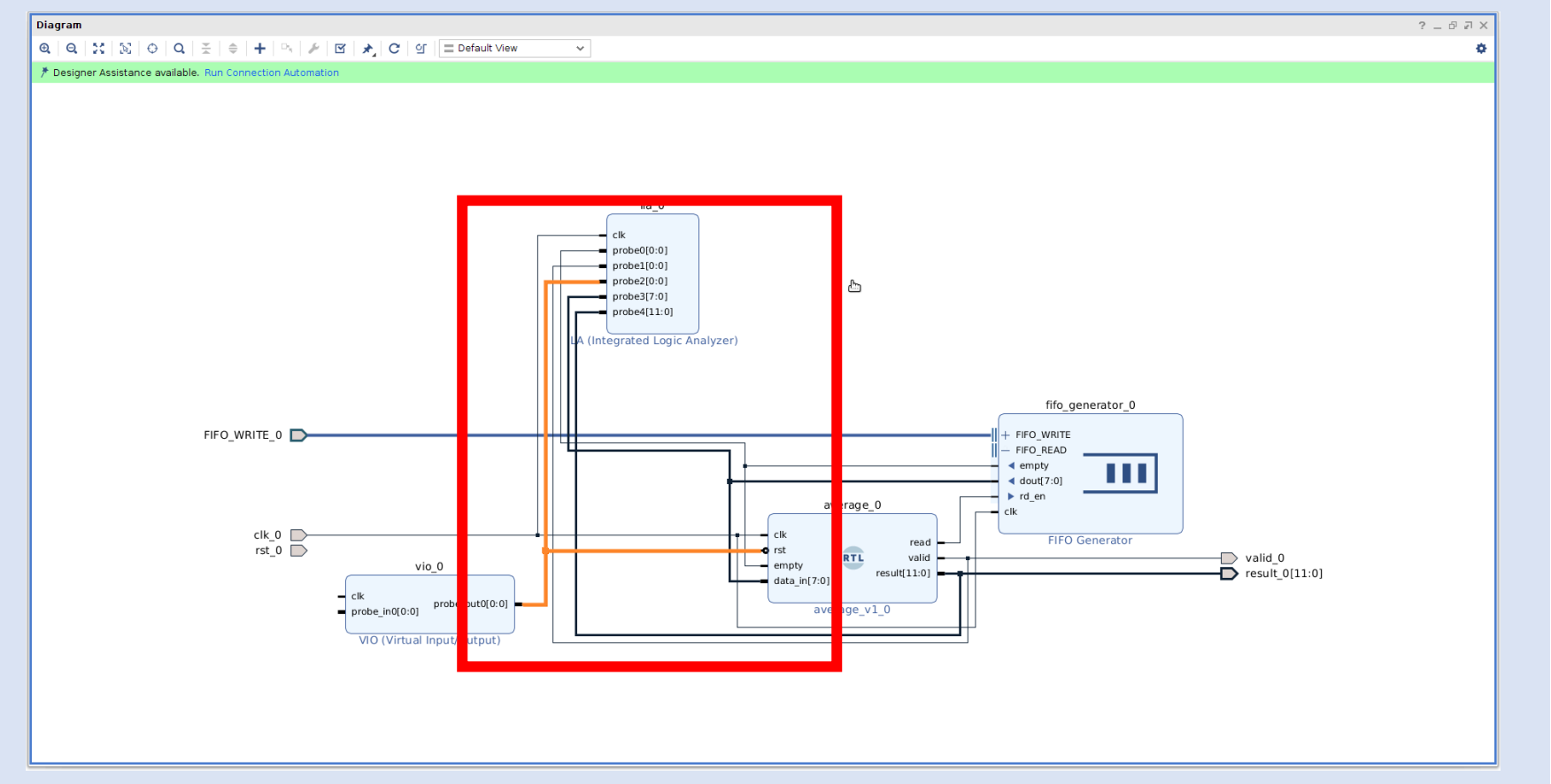
Lab 3: Advanced Vivado

Step 16 – Select the **RST_0 line** and delete it.



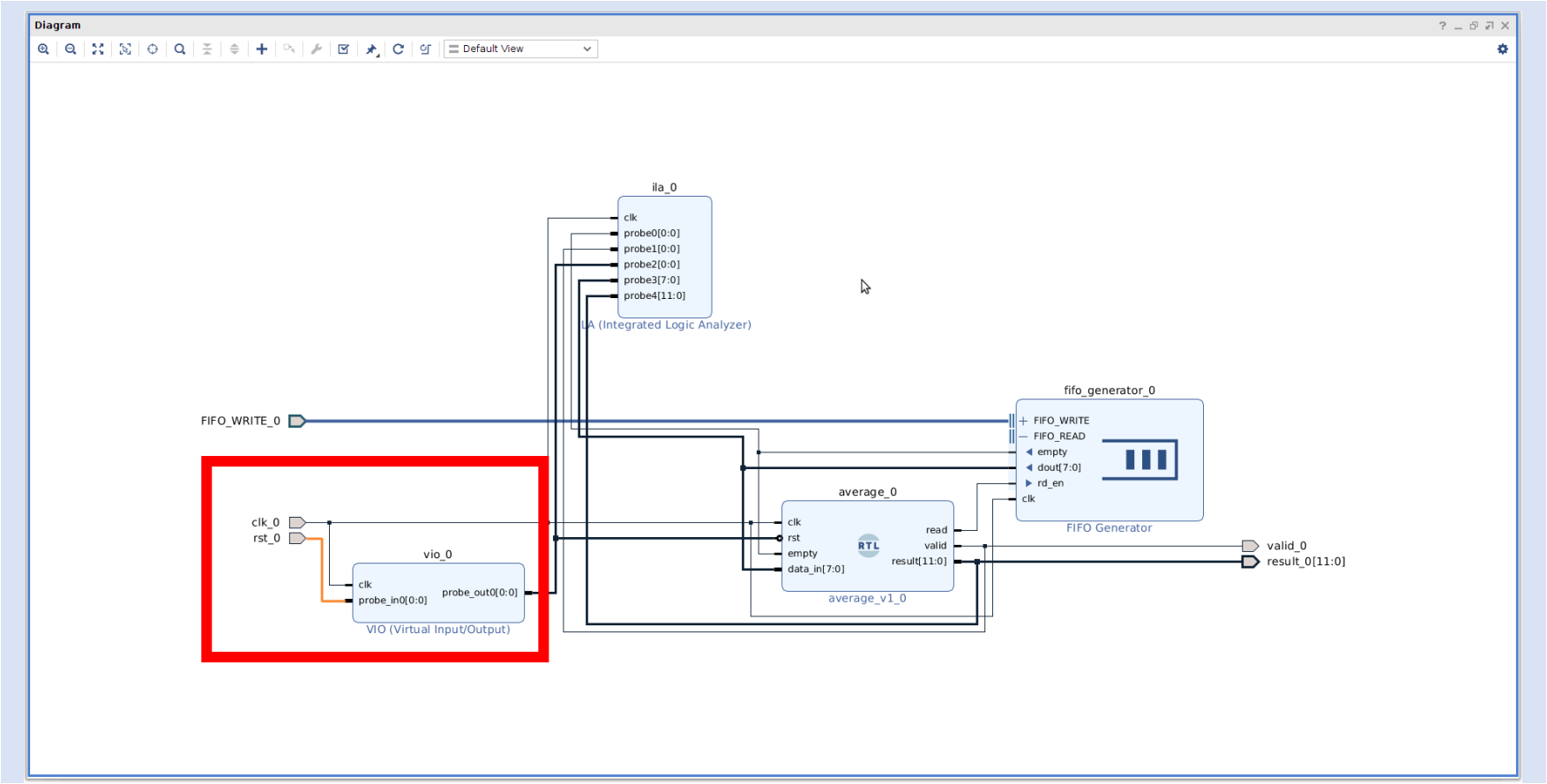
Lab 3: Advanced Vivado

Step 17 – Connect the **VIO probe output** to the **RST** and **ILA**.



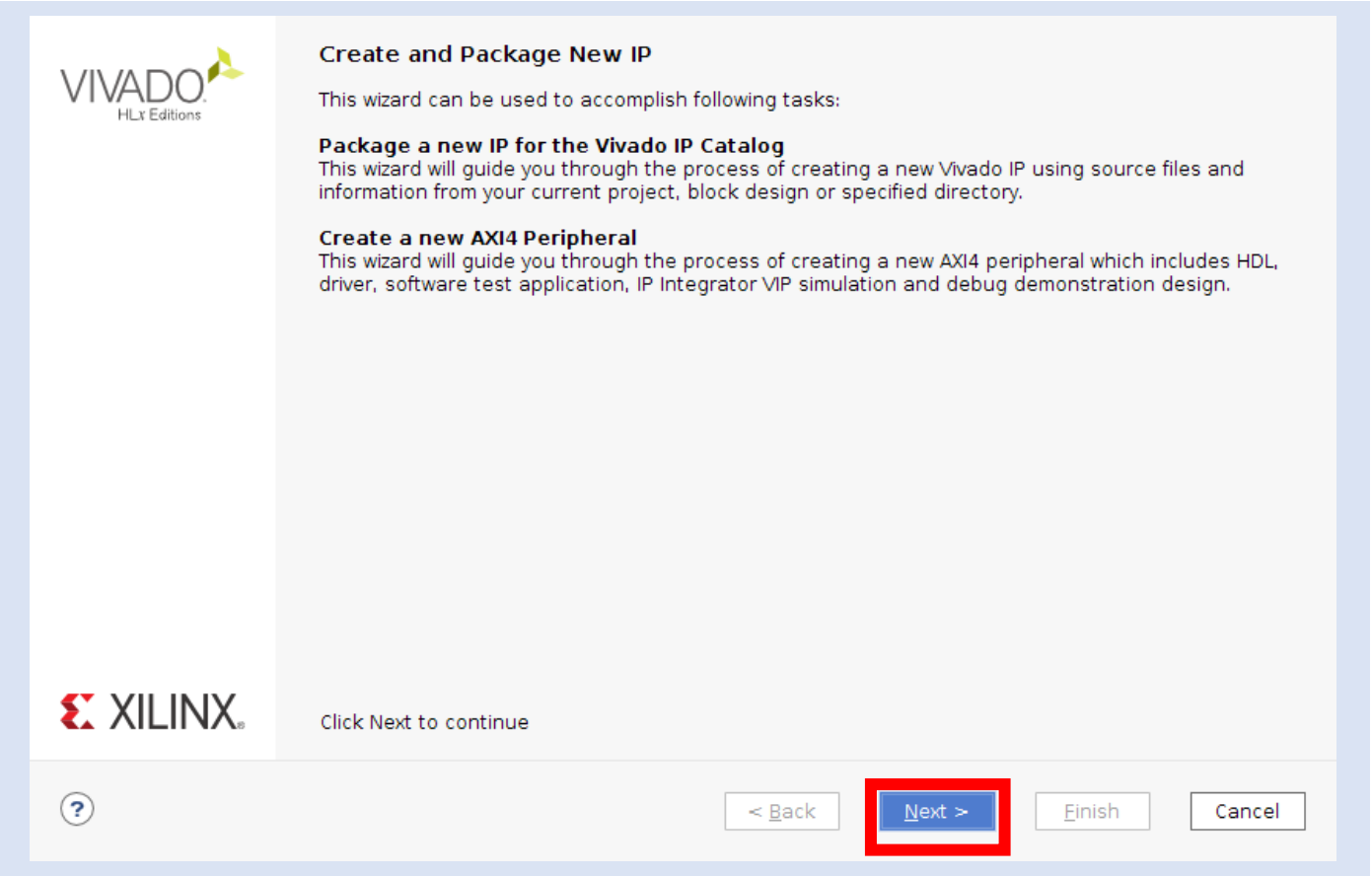
Lab 3: Advanced Vivado

Step 18 – Connect the **RST_0 input** to the VIO Probe in.



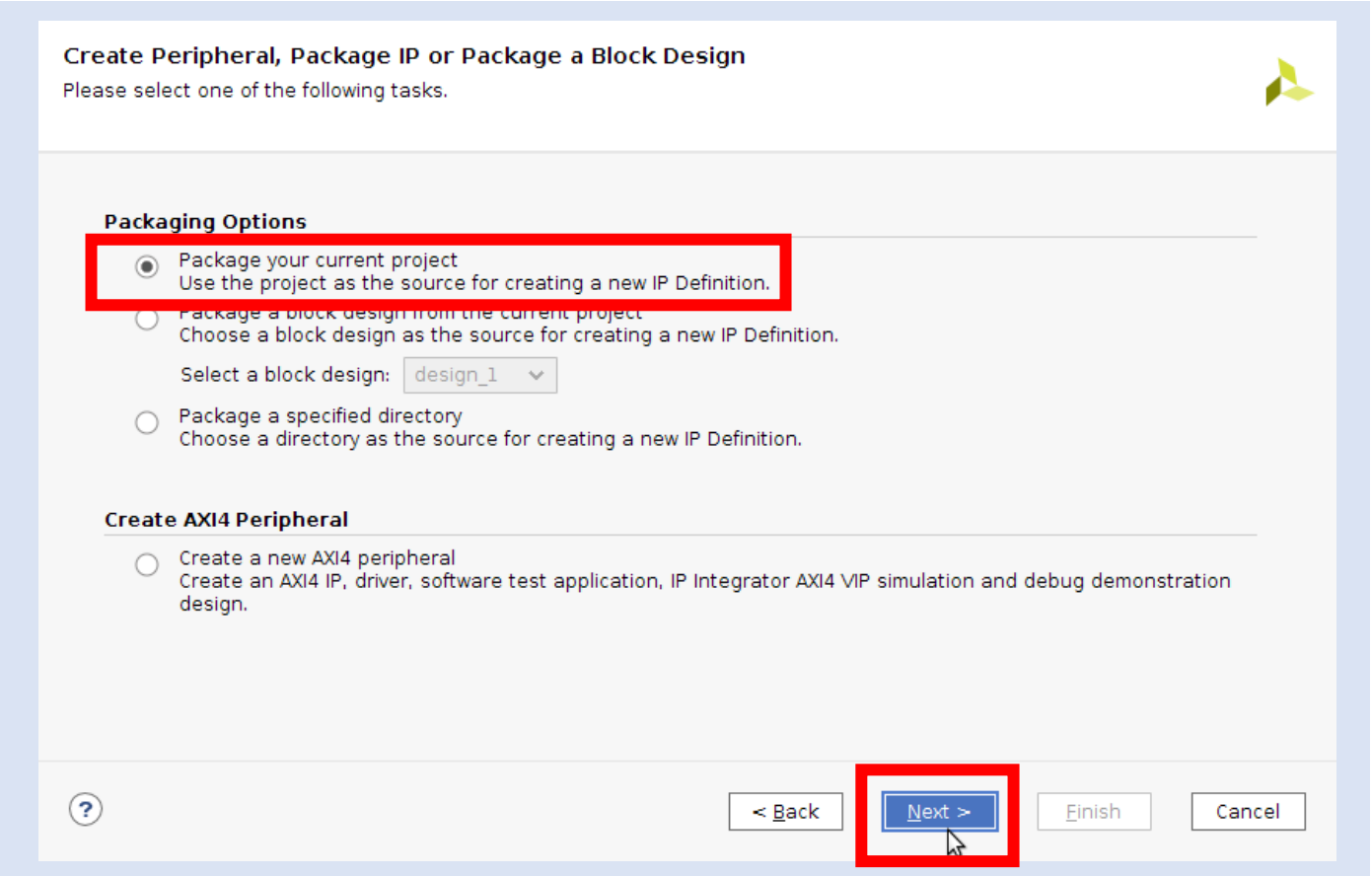
Lab 3: Advanced Vivado

Step 19 – From the Menu bar, select **Tools** → **Create and Package IP**. Select **Next** when the dialog opens.



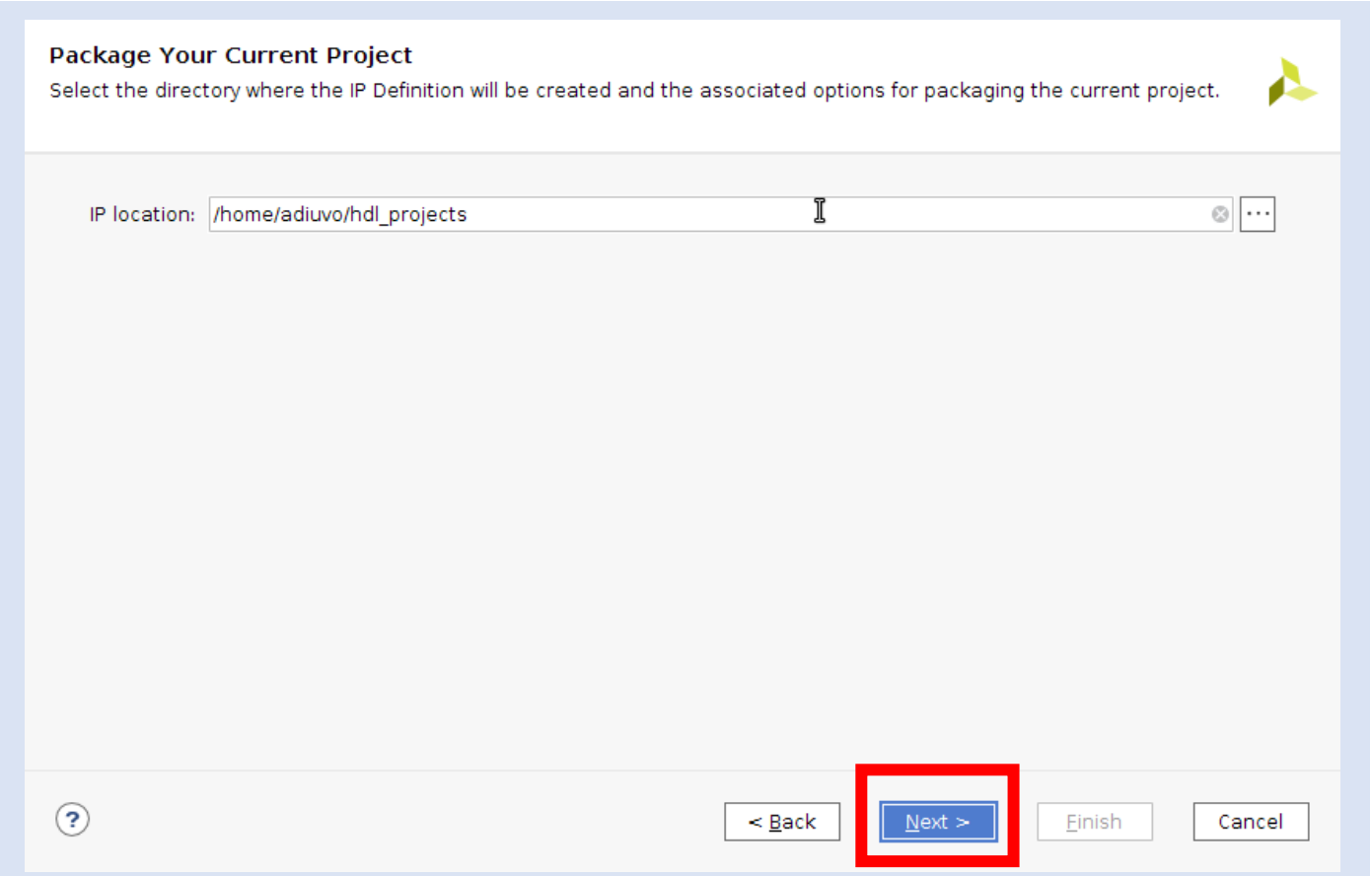
Lab 3: Advanced Vivado

Step 20 – Select **Package your current project** and then **Next**.



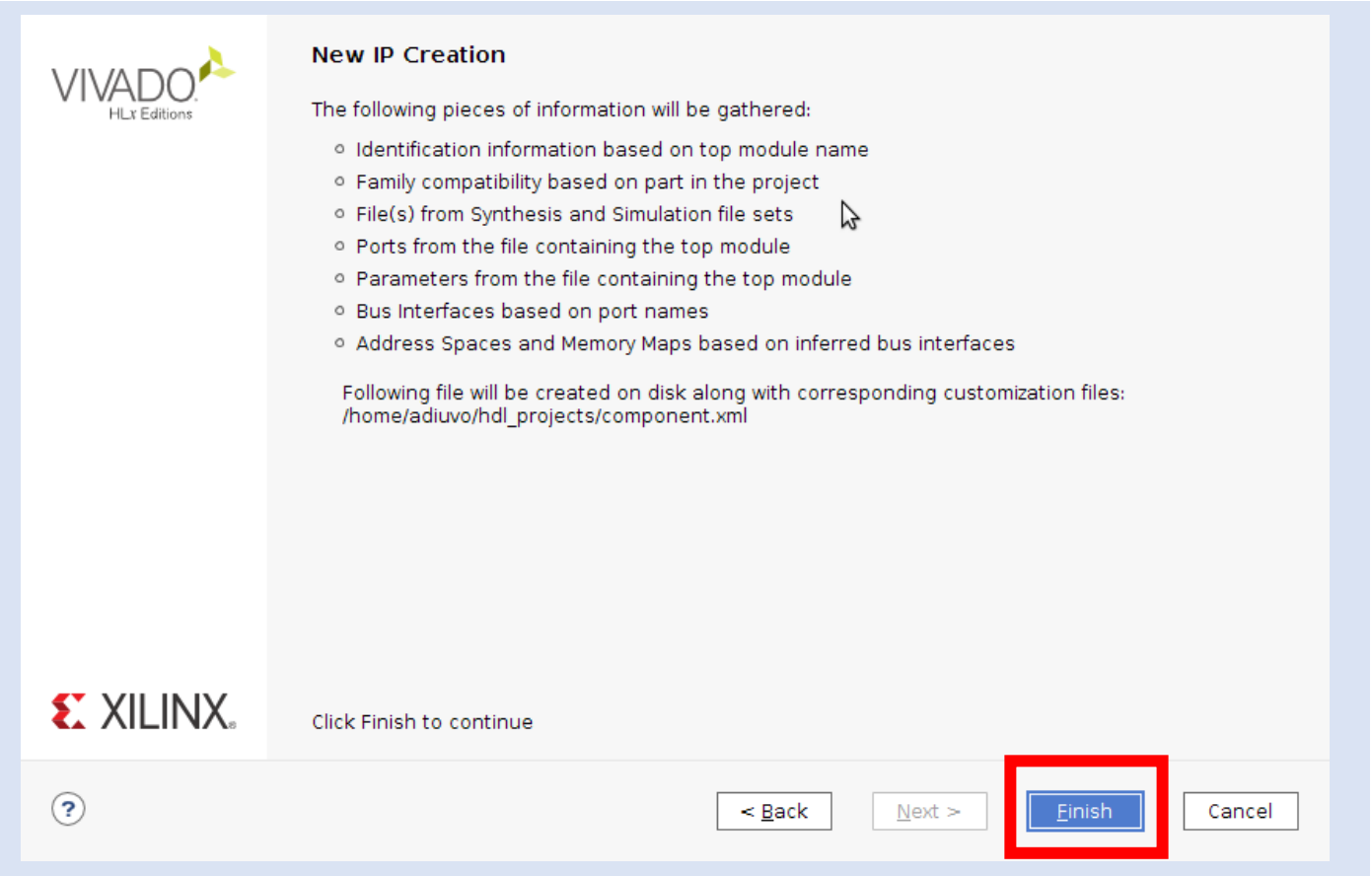
Lab 3: Advanced Vivado

Step 21 – Select the location the IP should be saved in and click **Next**.



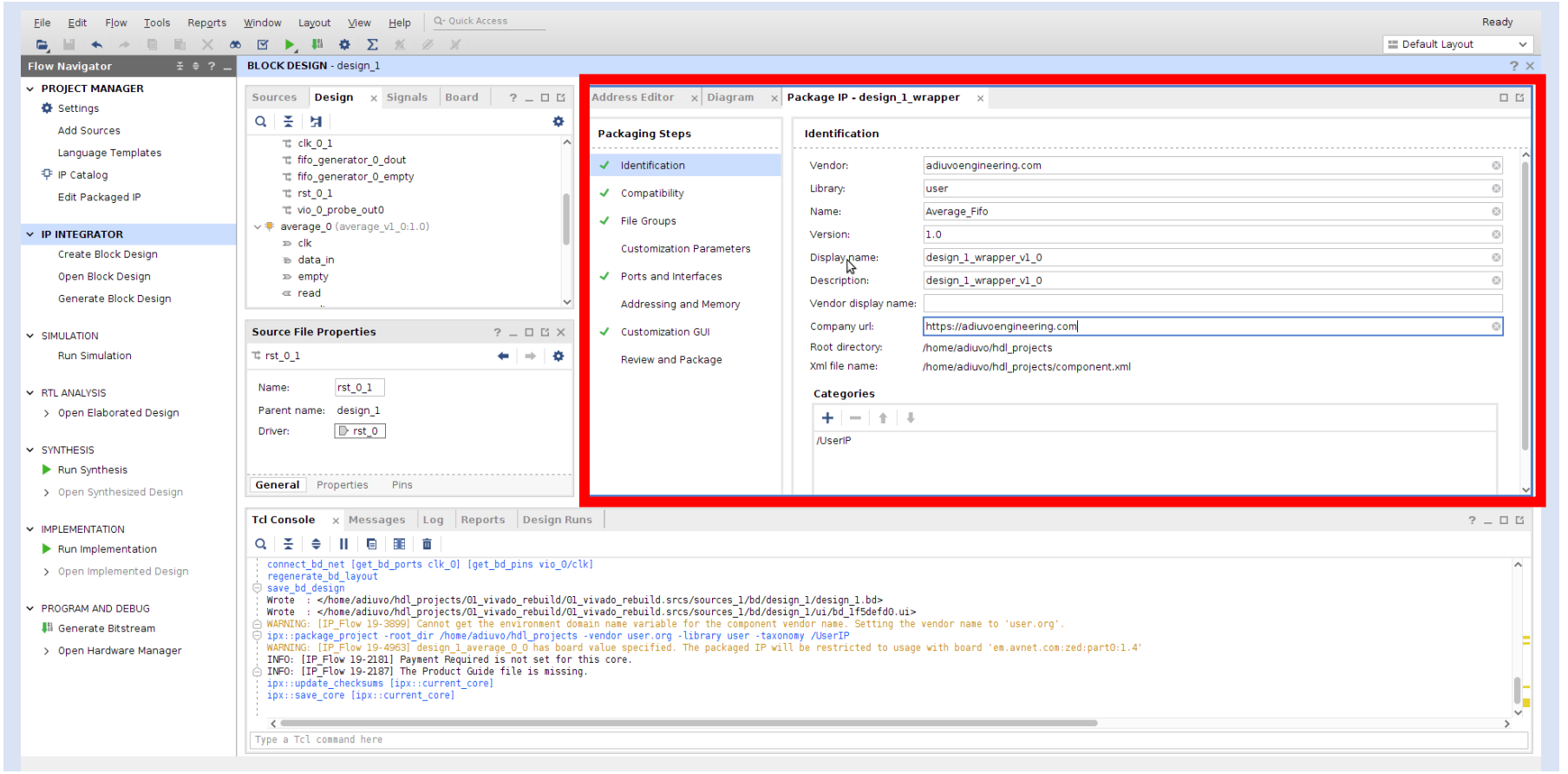
Lab 3: Advanced Vivado

Step 22 – Click on **Finish**.



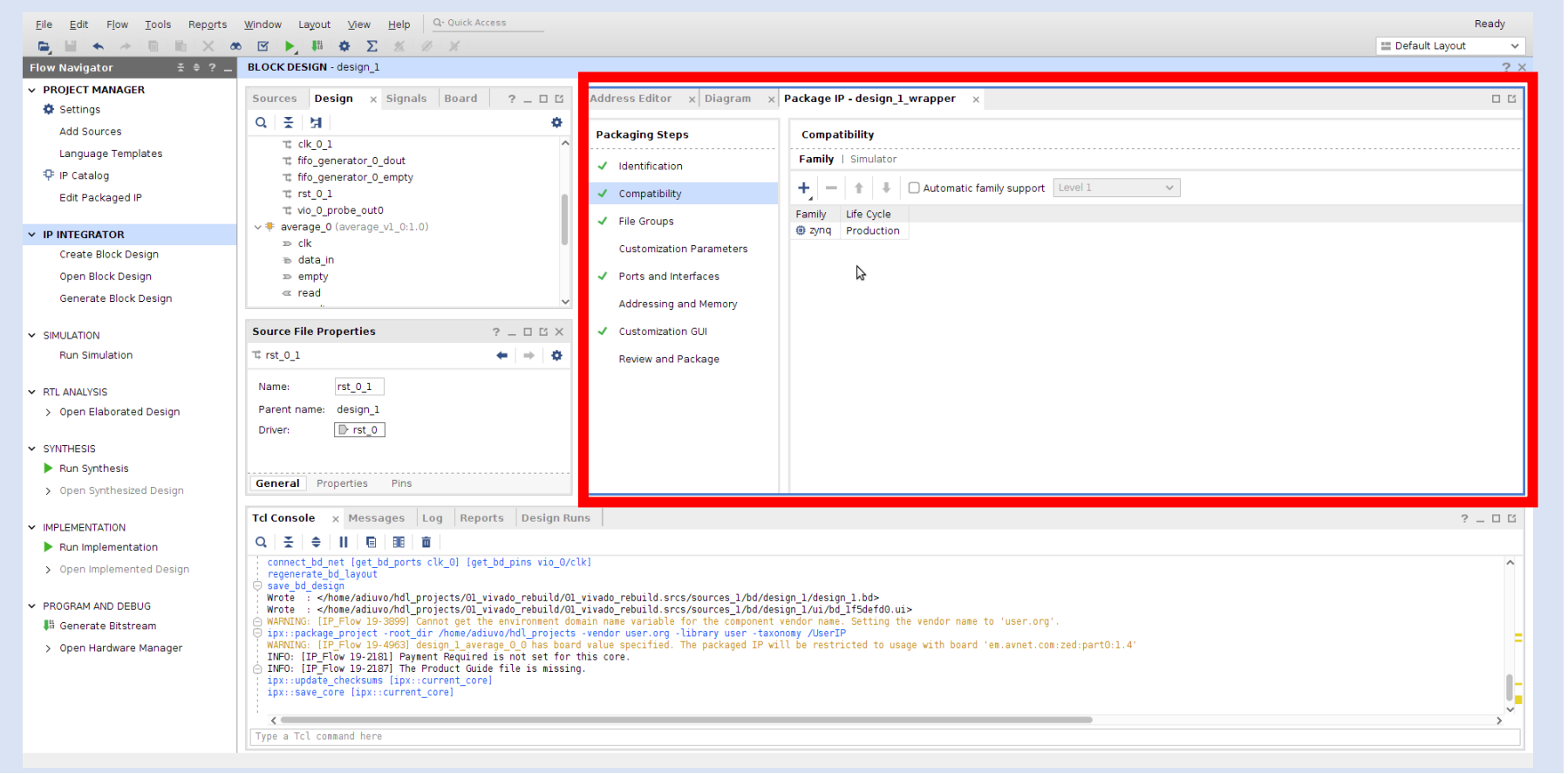
Lab 3: Advanced Vivado

Step 23 – This will open a package view in the project. Enter **Name, Version** and **Company URL**.



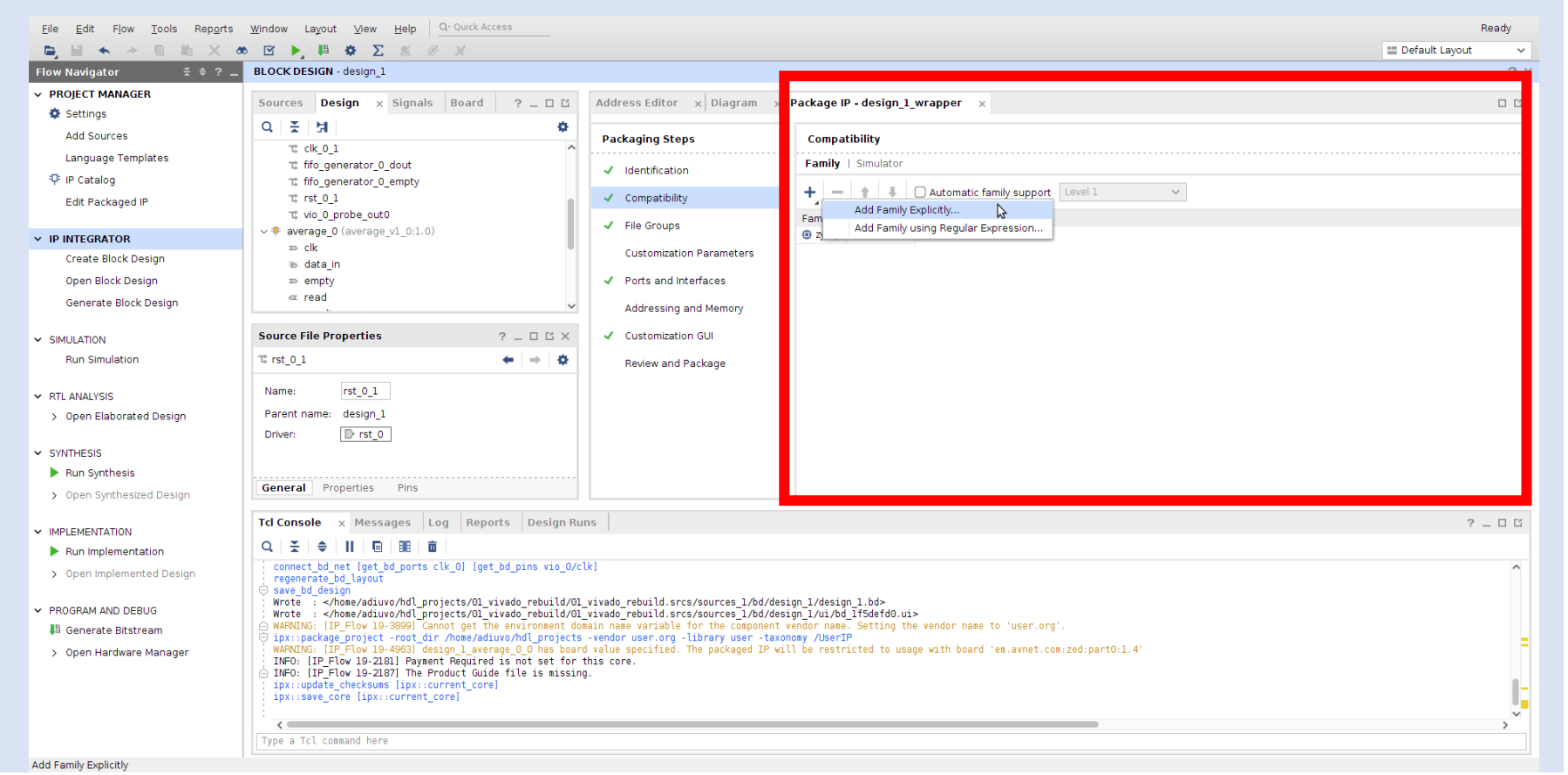
Lab 3: Advanced Vivado

Step 24 – Click on the **Compatibility tab.** This defines what FPGA / SoC the core will work with.



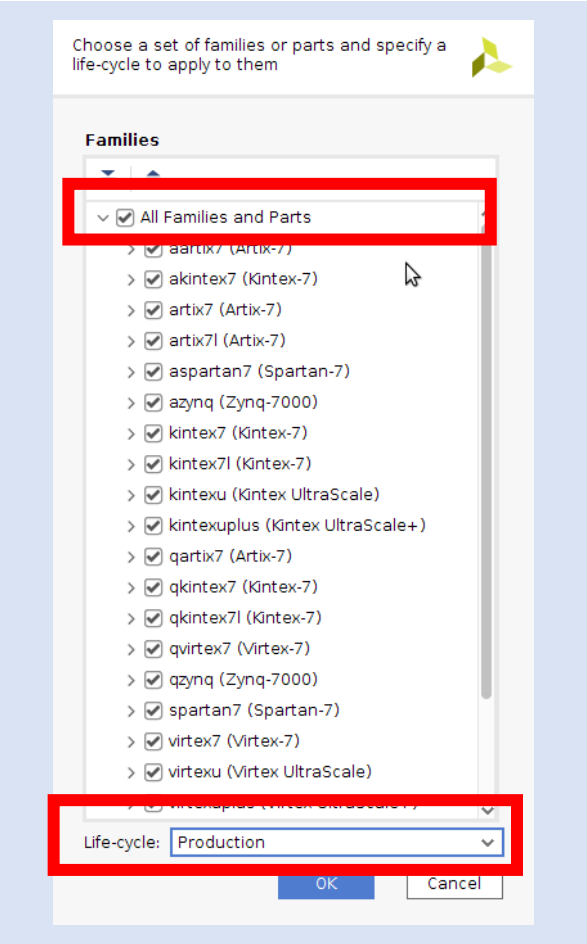
Lab 3: Advanced Vivado

Step 25 – Click on **+** and select **Add Family Explicitly**.



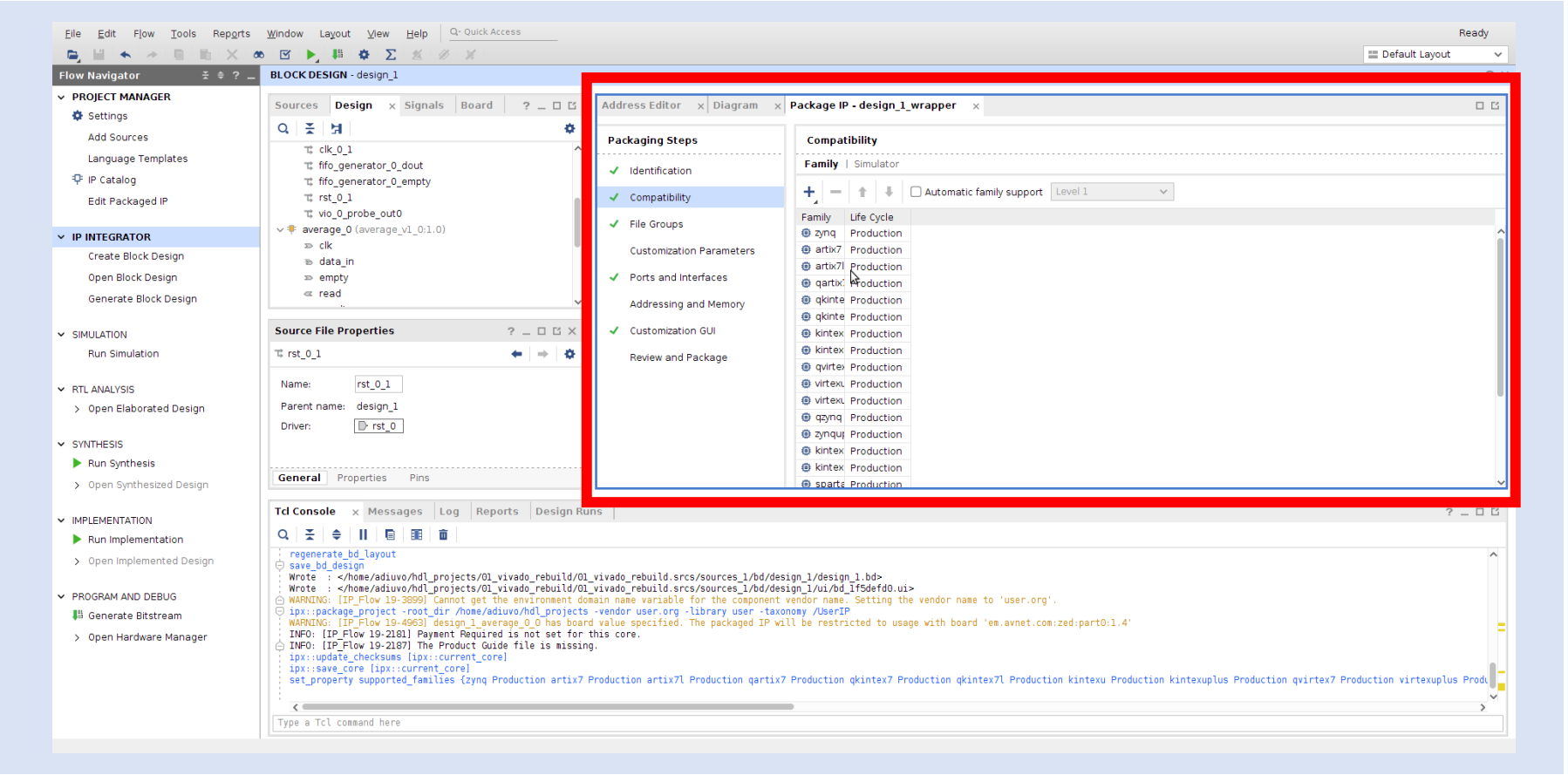
Lab 3: Advanced Vivado

Step 26 – In the resultant dialog, select **All Families** and **Parts** and **Production** from the Life-cycle.



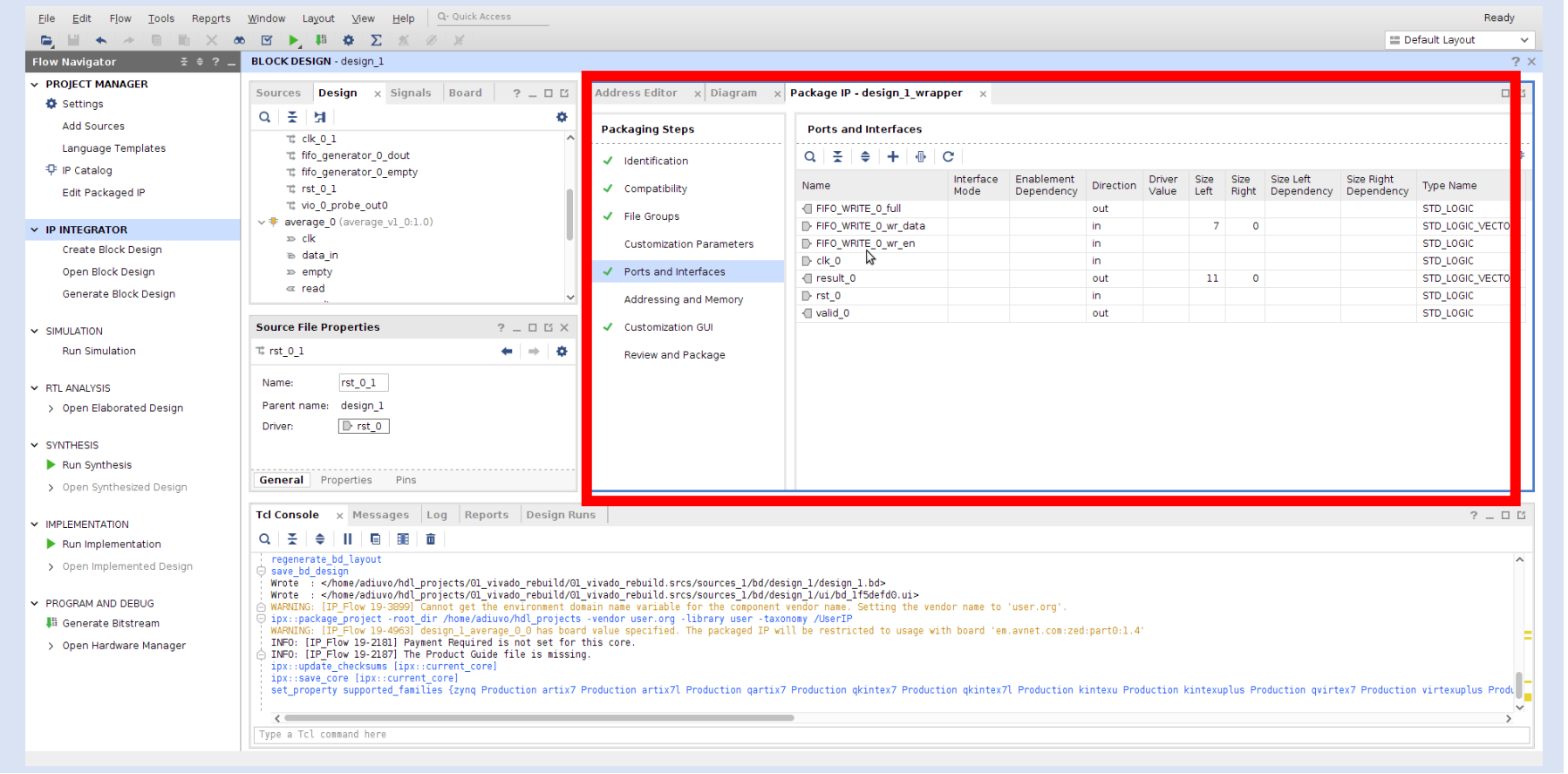
Lab 3: Advanced Vivado

Step 27 – This will make the IP core available to all families and devices.



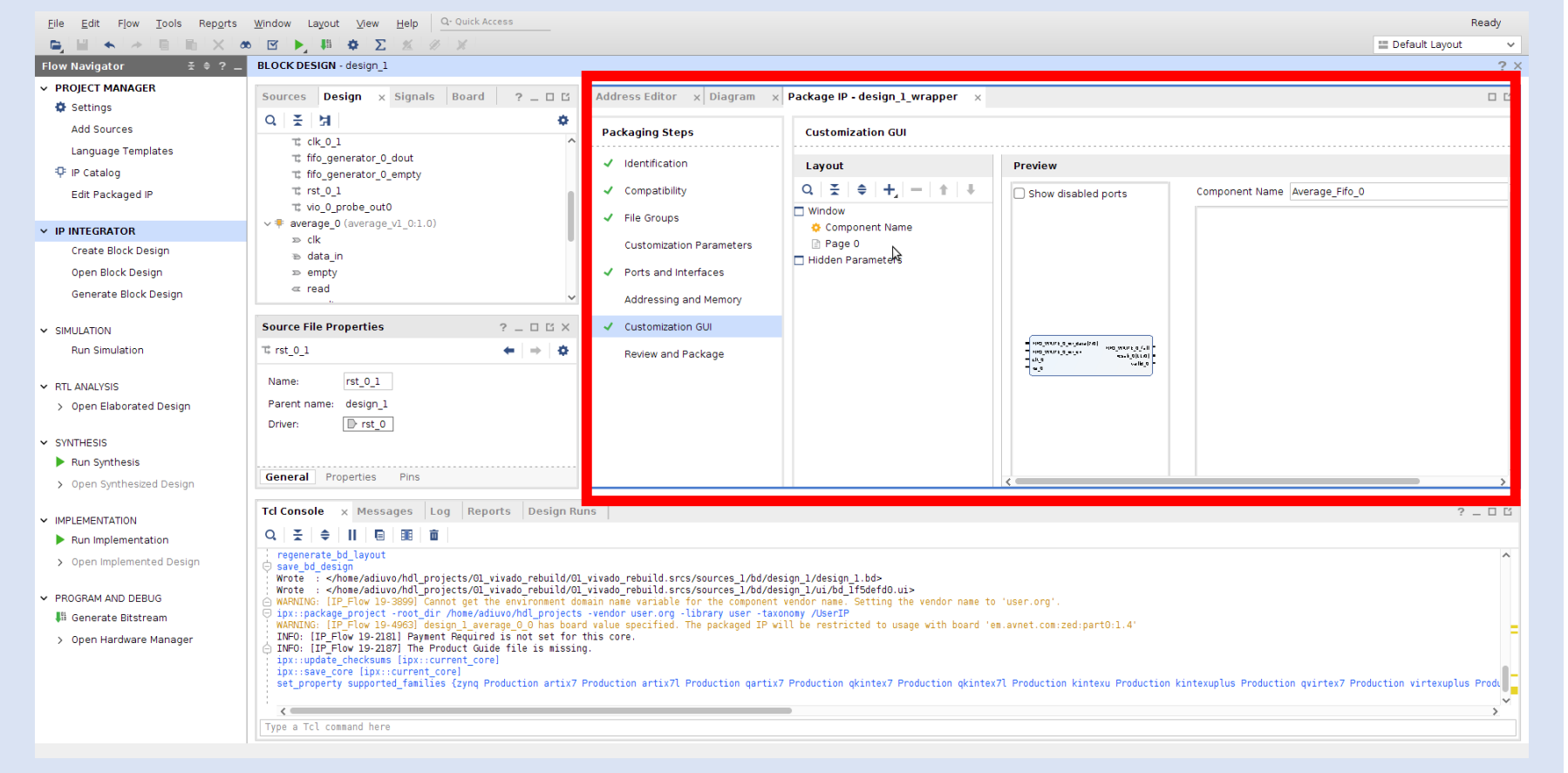
Lab 3: Advanced Vivado

Step 28 – Click on **Ports and Interfaces.** This should show all the blocks' inputs and outputs.



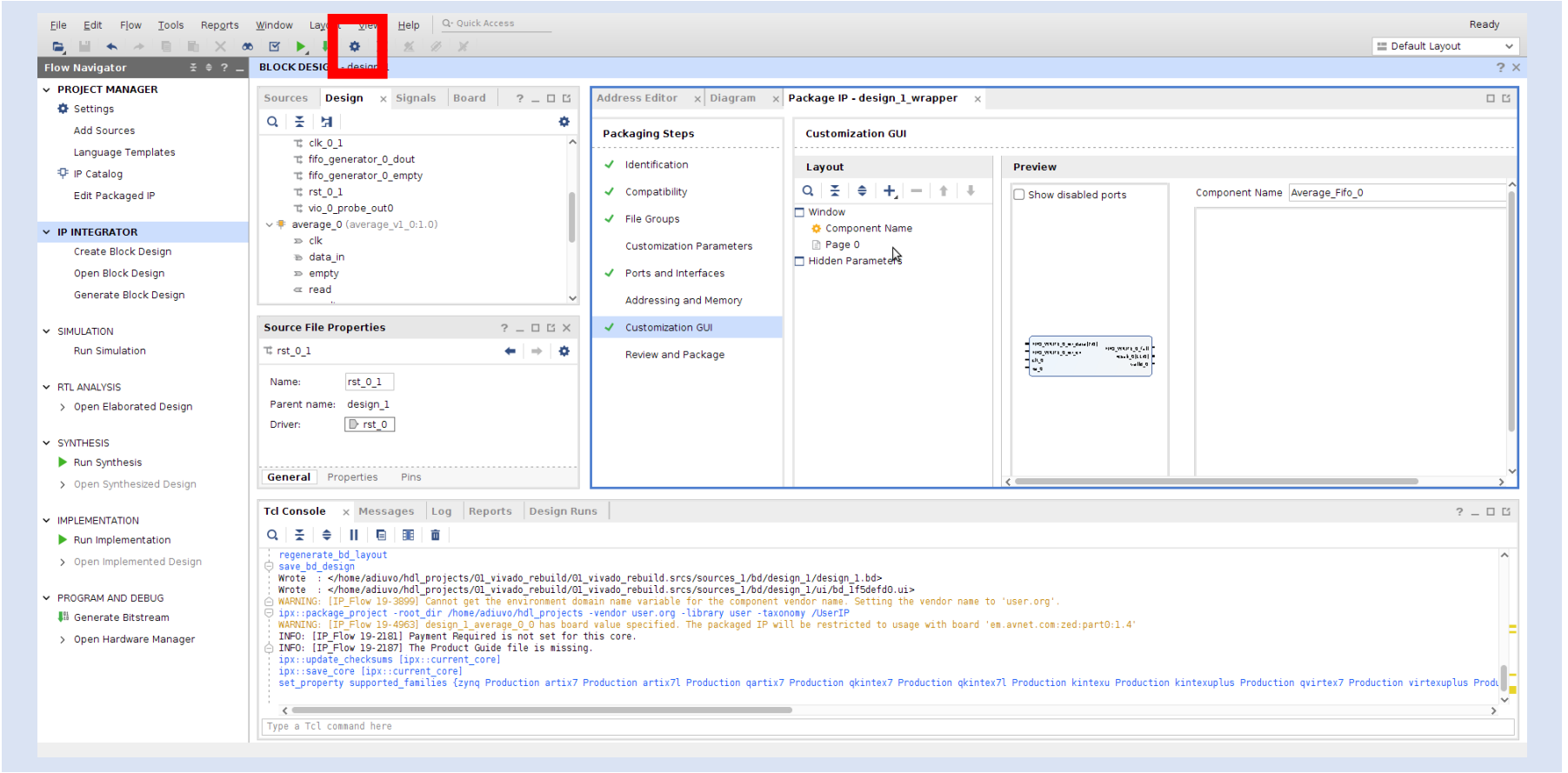
Lab 3: Advanced Vivado

Step 29 – Click on **Customization**. This shows the symbol.



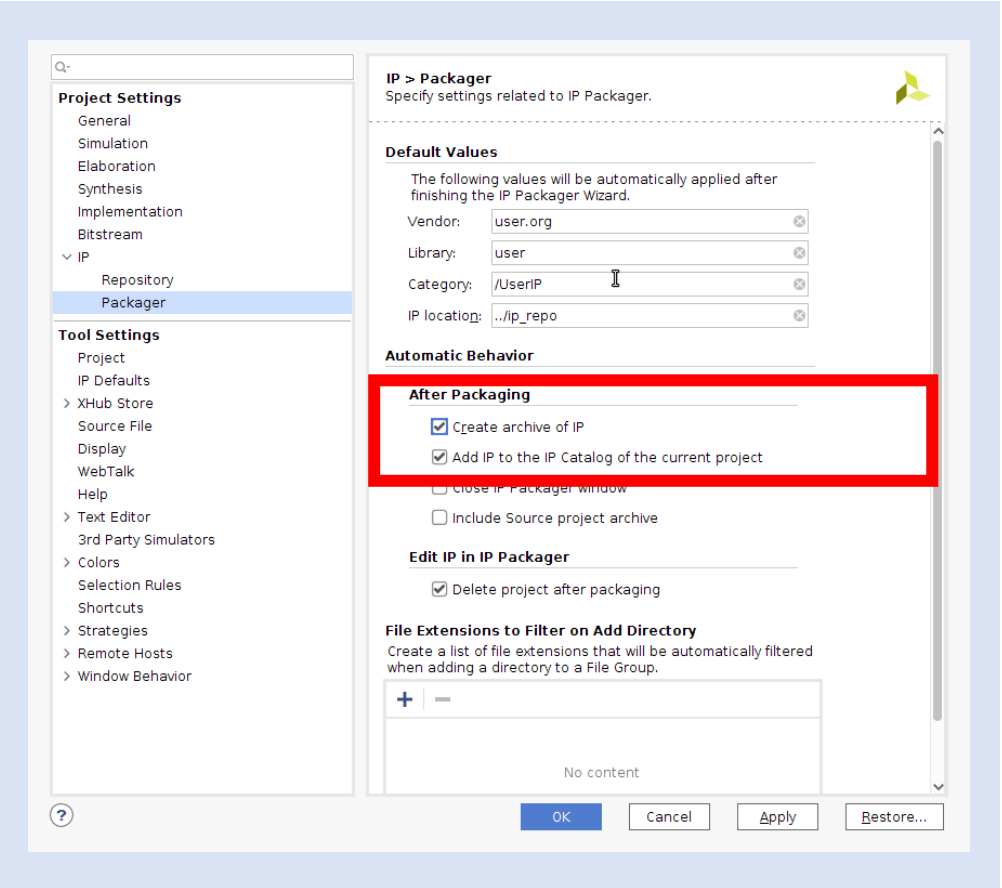
Lab 3: Advanced Vivado

Step 30 – Click on Settings.



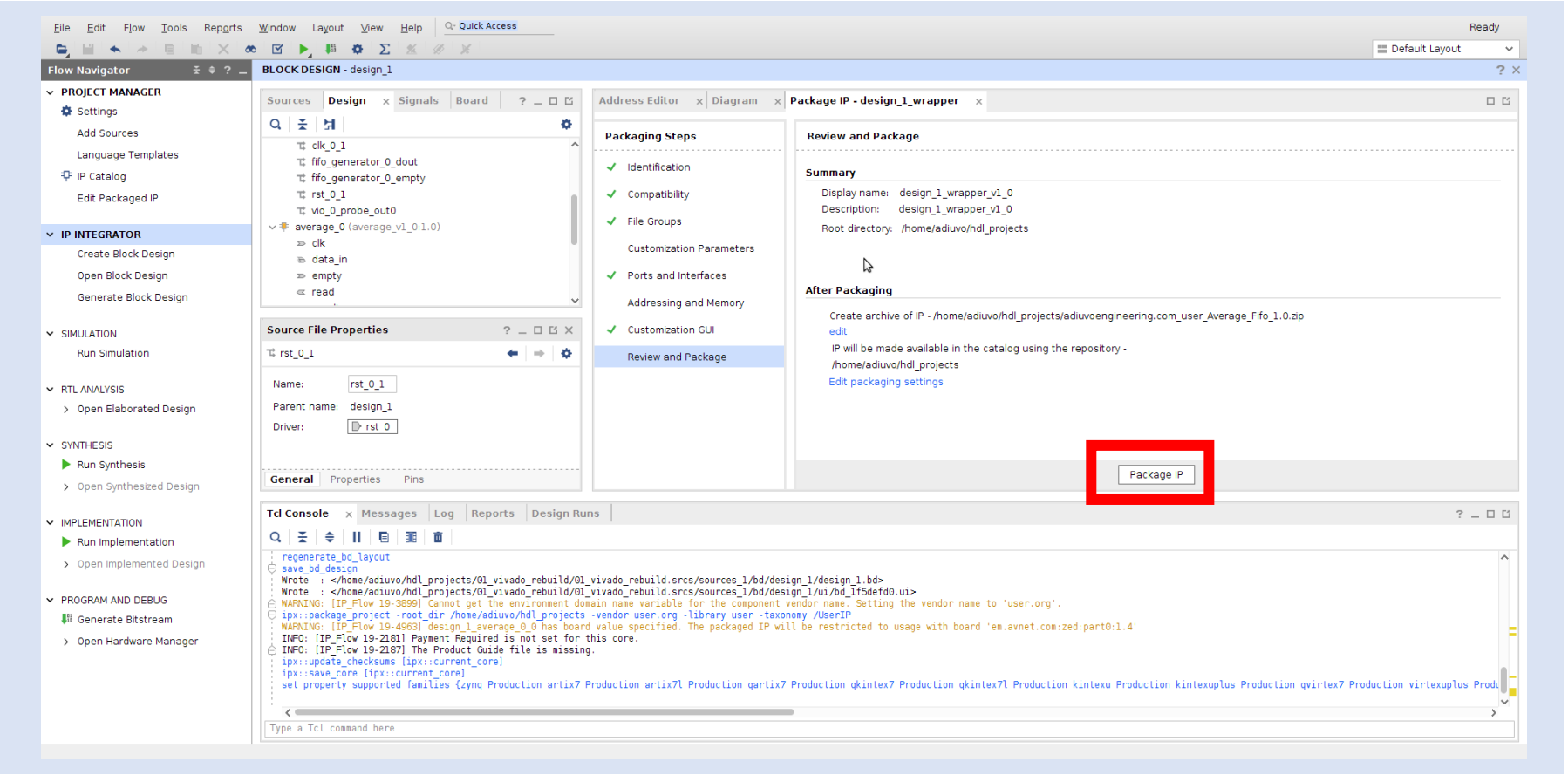
Lab 3: Advanced Vivado

Step 31 – Select **Create archive of IP** and click **OK**.



Lab 3: Advanced Vivado

Step 32 – Click on **Review and Package** and then **Package IP**.

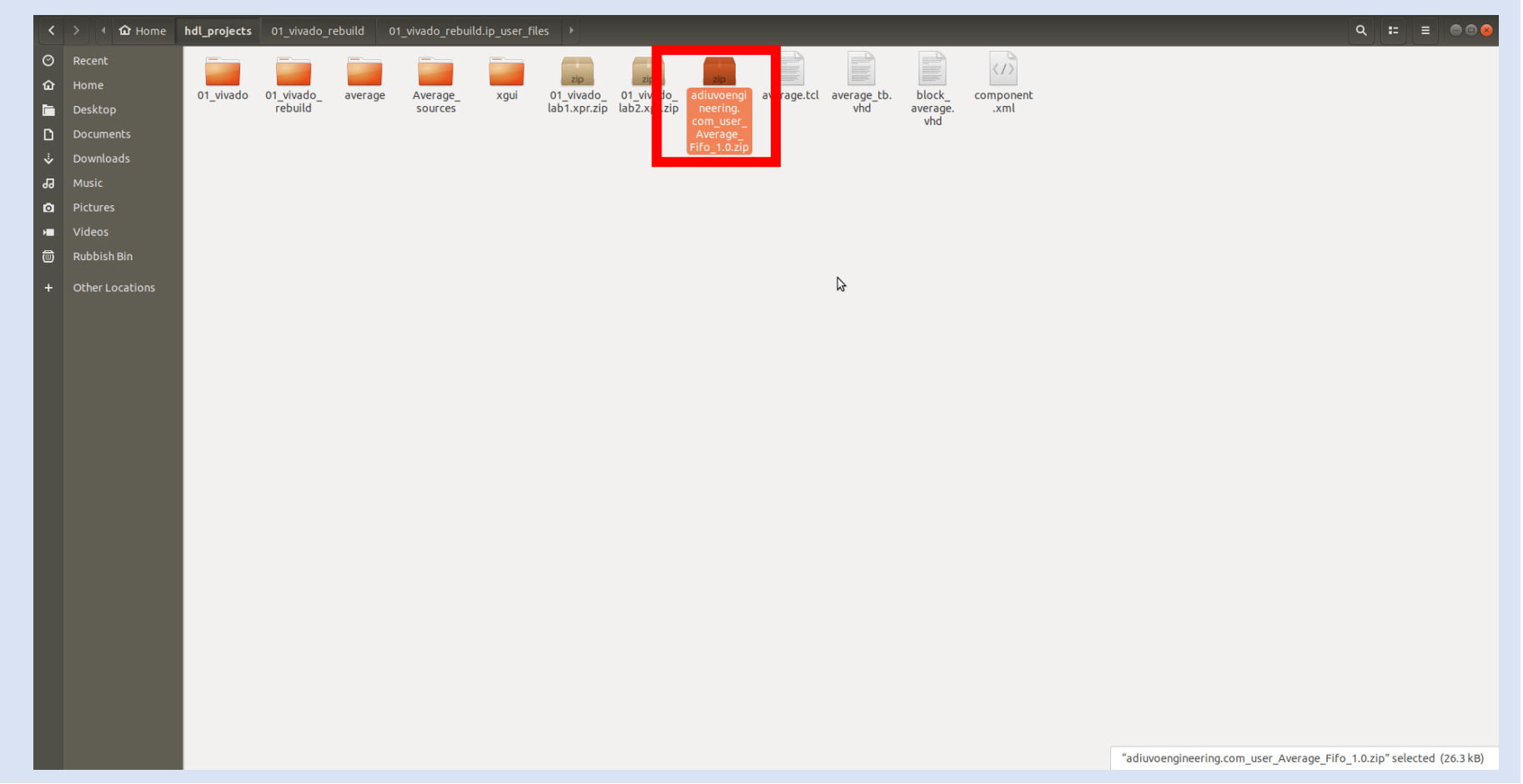


Lab 3: Advanced Vivado

Step 33 – This should show the message below. Click **OK**.

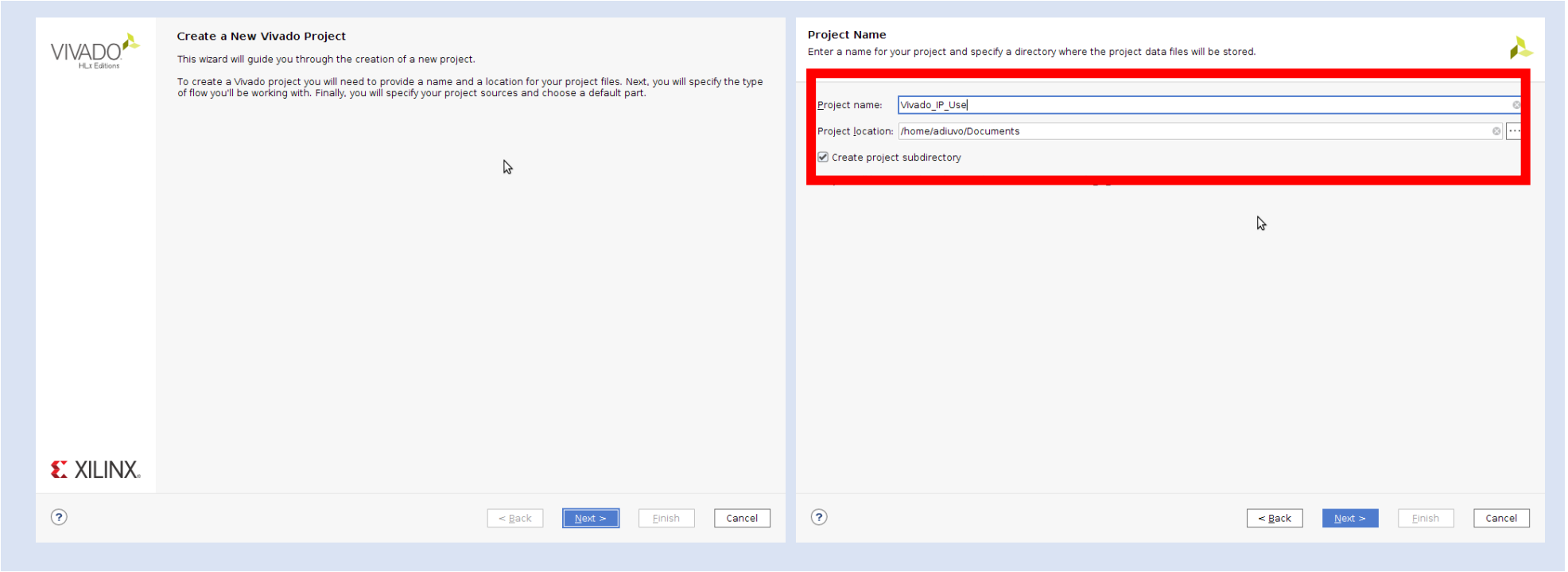
Lab 3: Advanced Vivado

Step 34 – You will see a ZIP file of the component in the directory you identified to save the IP in.



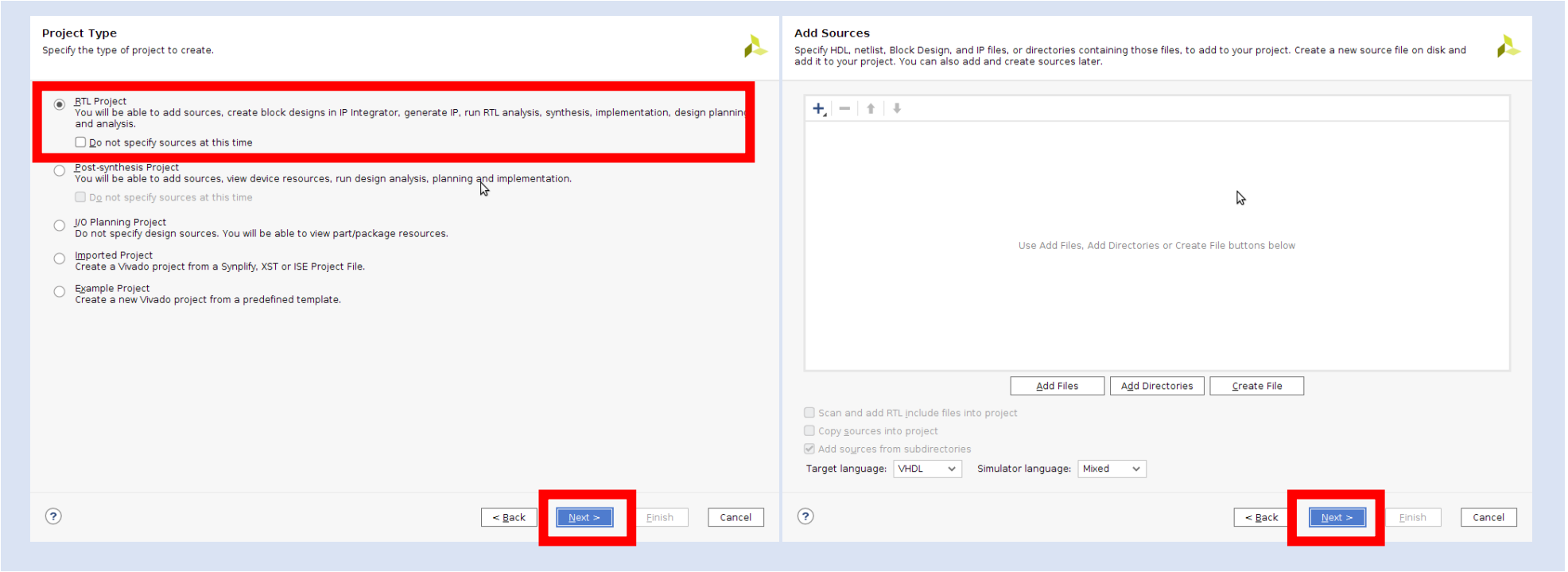
Lab 3: Advanced Vivado

Step 35 – Close the project and create a new Vivado project. In the wizard, click **Next**, then enter the **name and location** and click **Next** again.



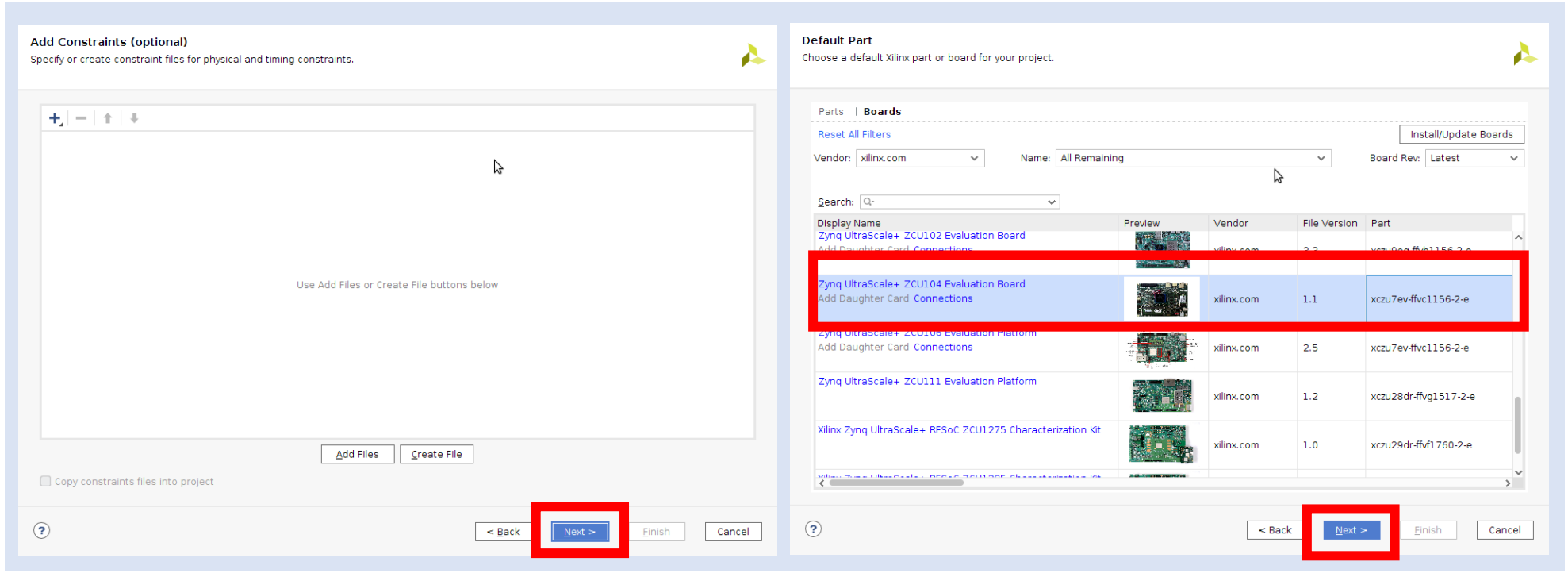
Lab 3: Advanced Vivado

Step 36 – Select **RTL Project** and **Next**, followed by **Next** again.



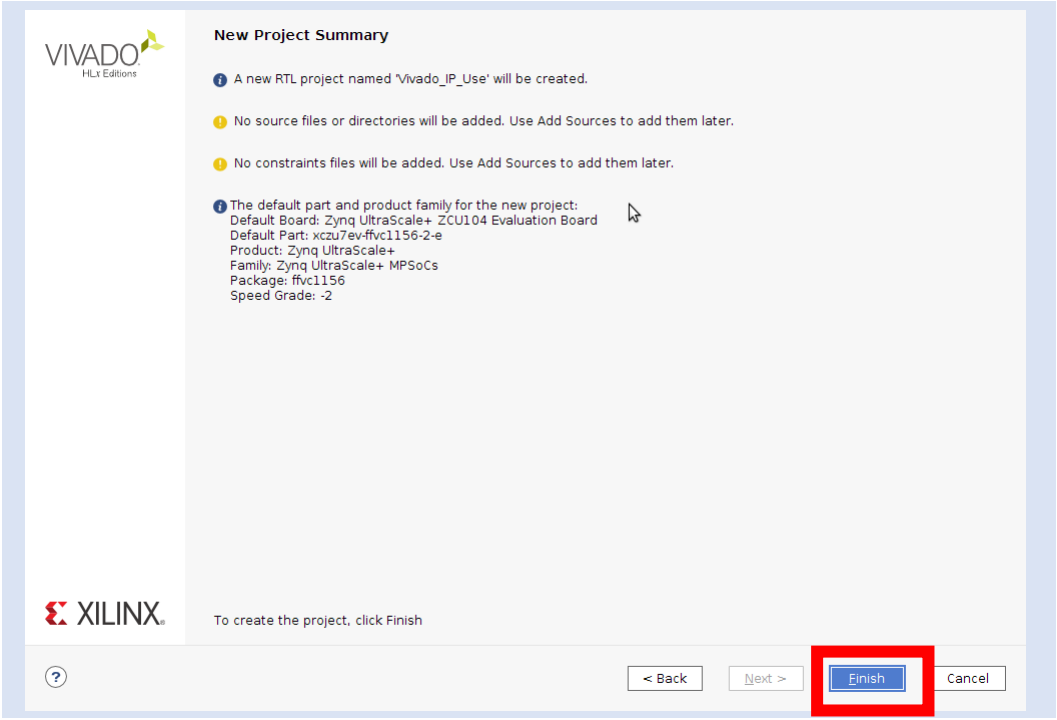
Lab 3: Advanced Vivado

Step 37 – Click **Next** on the Constraints tab. On the Default Part, select the **ZCU104 board** and click **Next**.



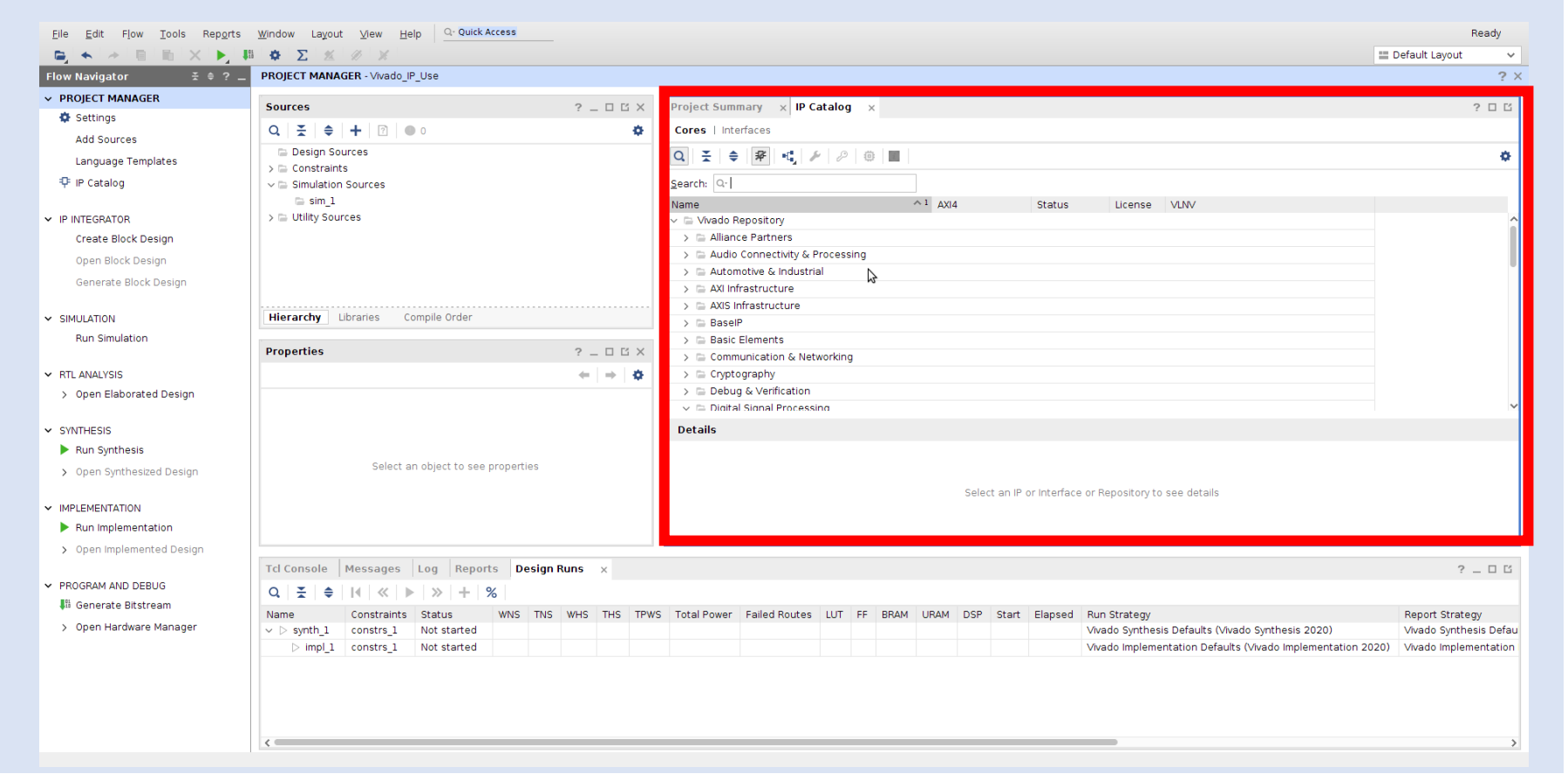
Lab 3: Advanced Vivado

Step 38 – On the final page of the Project Summary, click **OK**.



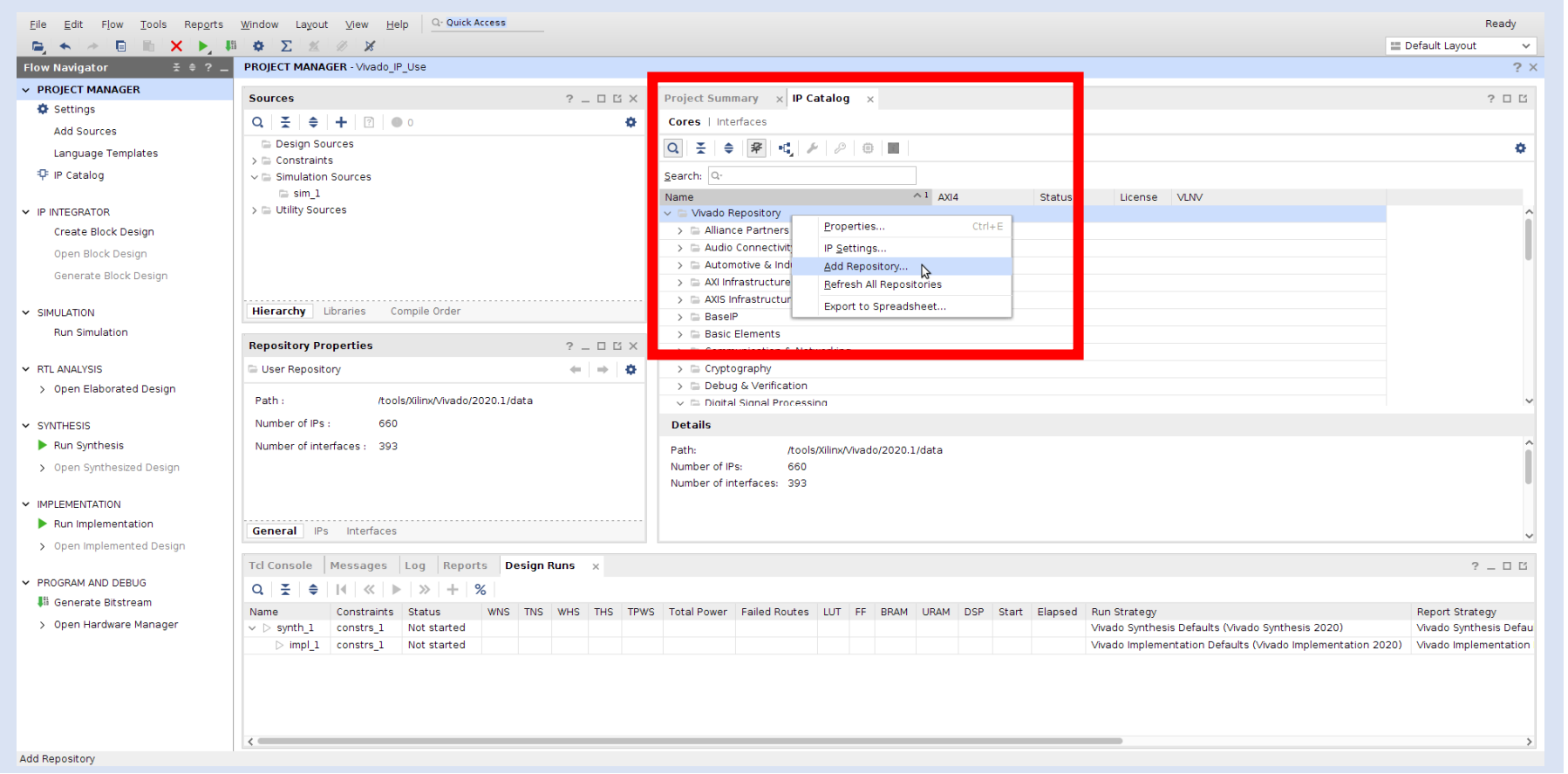
Lab 3: Advanced Vivado

Step 39 – From the menu bar, select **Window → IP Catalog**.



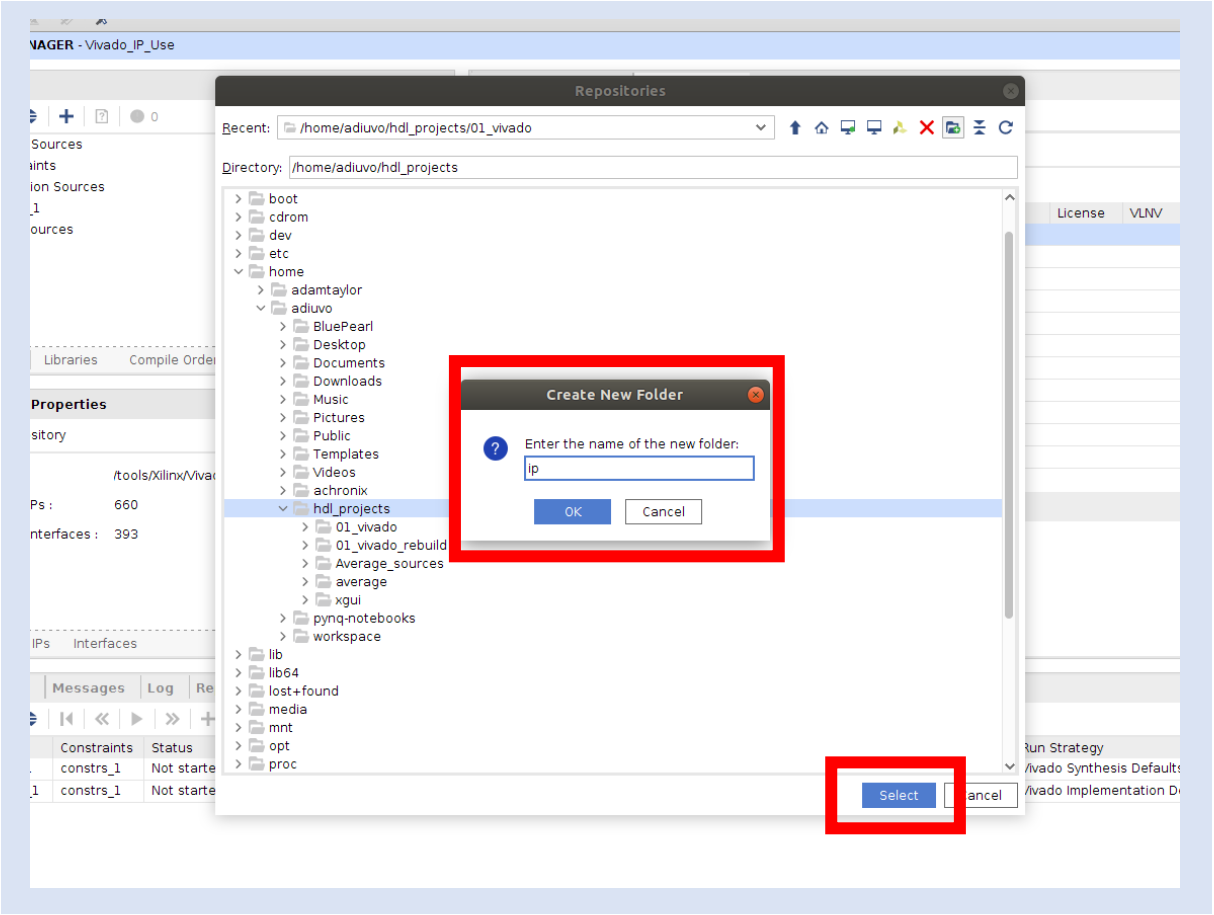
Lab 3: Advanced Vivado

Step 40 – Right click on the **Vivado Repository** and select **Add Repository.**



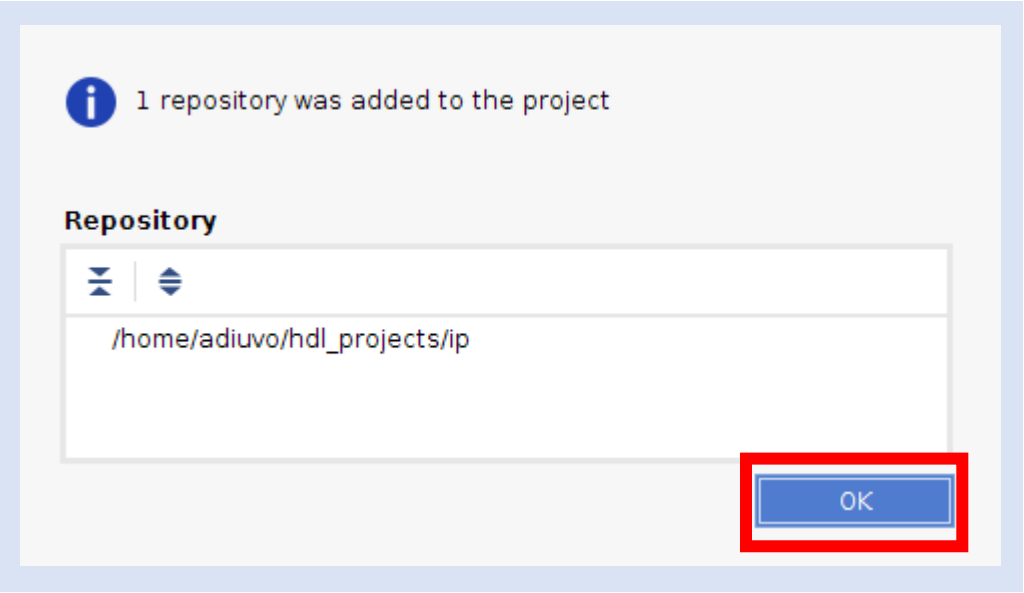
Lab 3: Advanced Vivado

Step 41 – In the open dialog, select **Create New Folder** and name it ***IP*** and click **Select**.



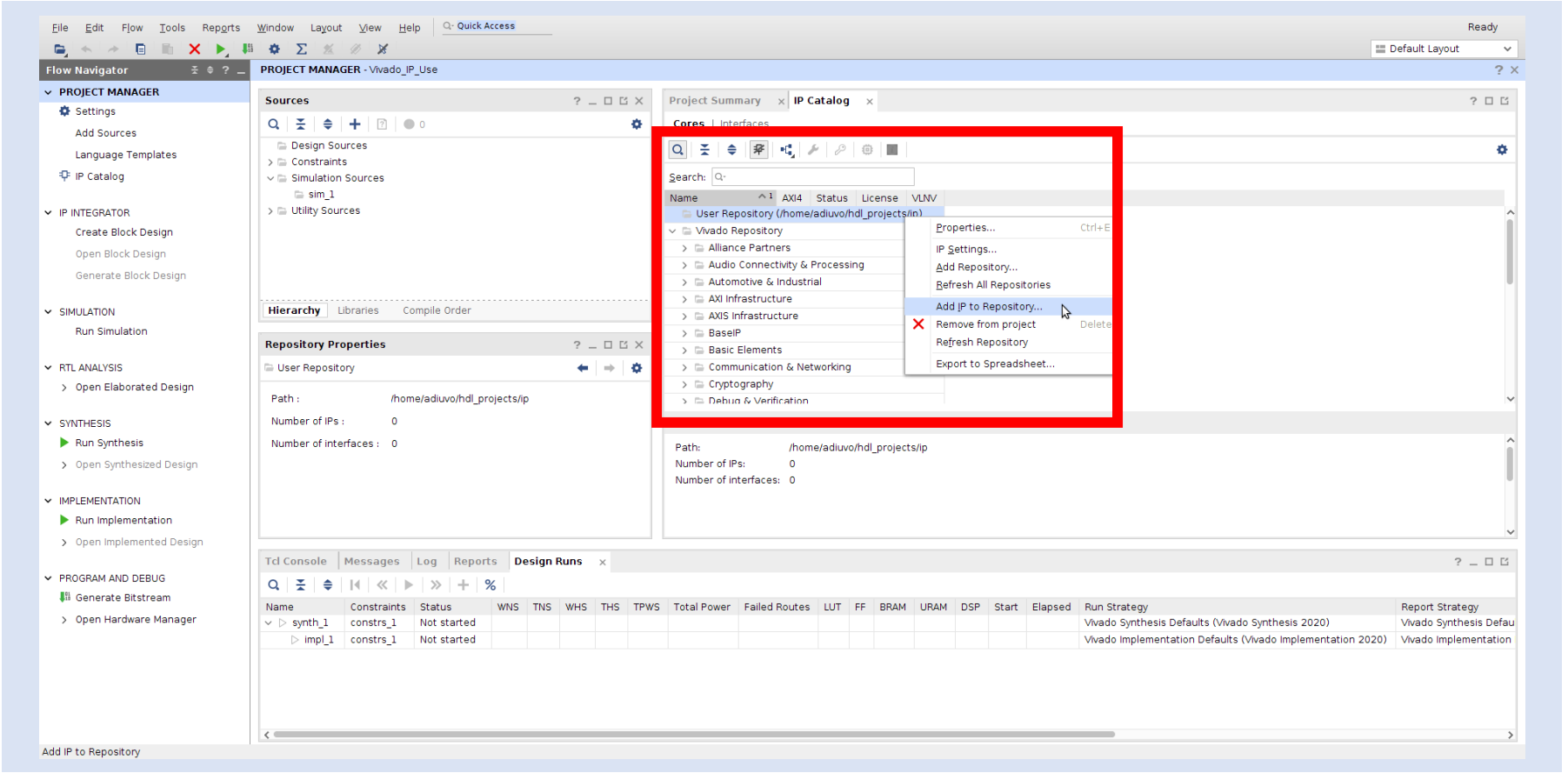
Lab 3: Advanced Vivado

Step 42 – This will show a dialog indicating that one repository was added.



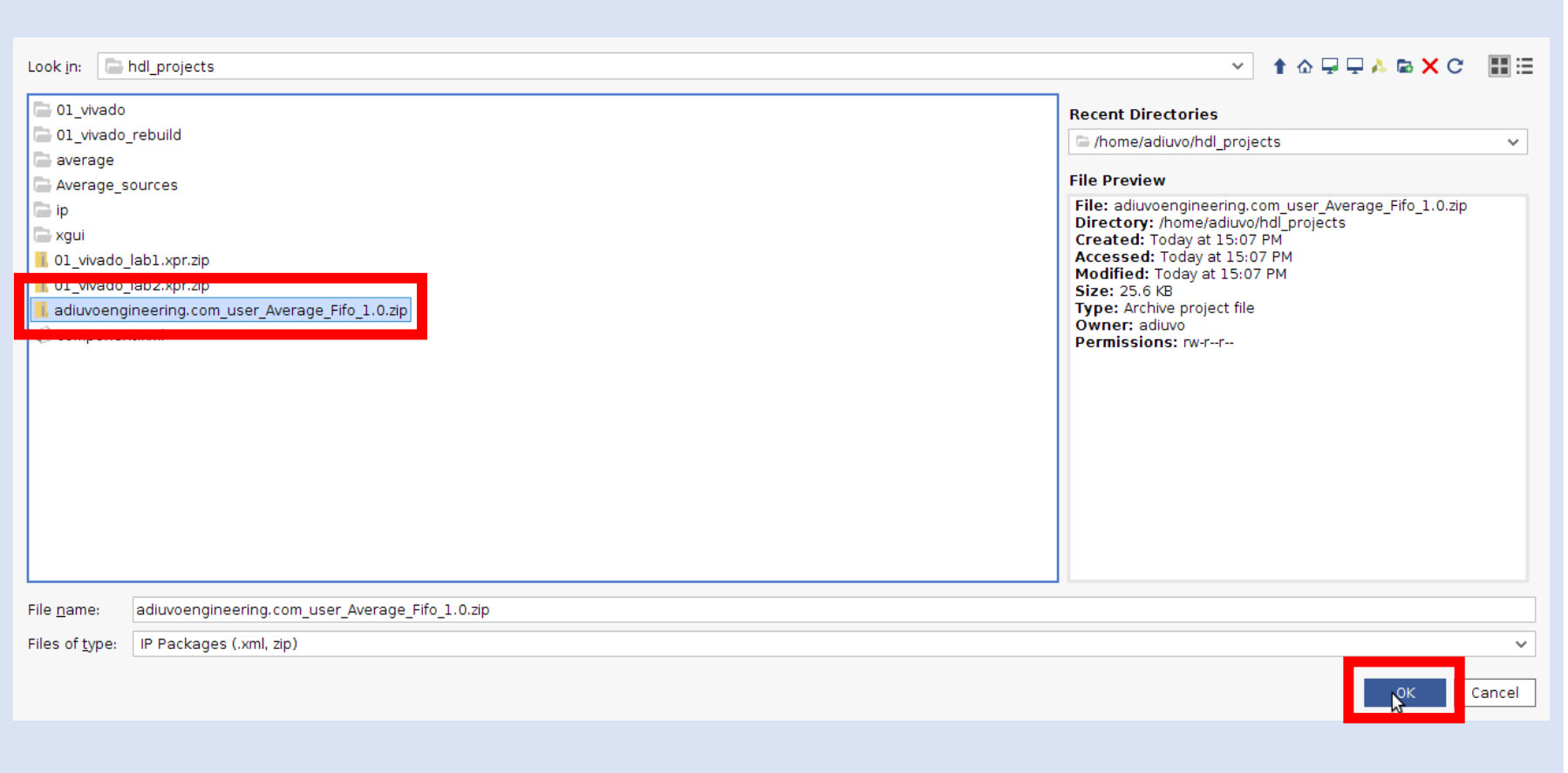
Lab 3: Advanced Vivado

Step 43 – This will add in the repository. Right click on it and select **Add IP to Repository**.



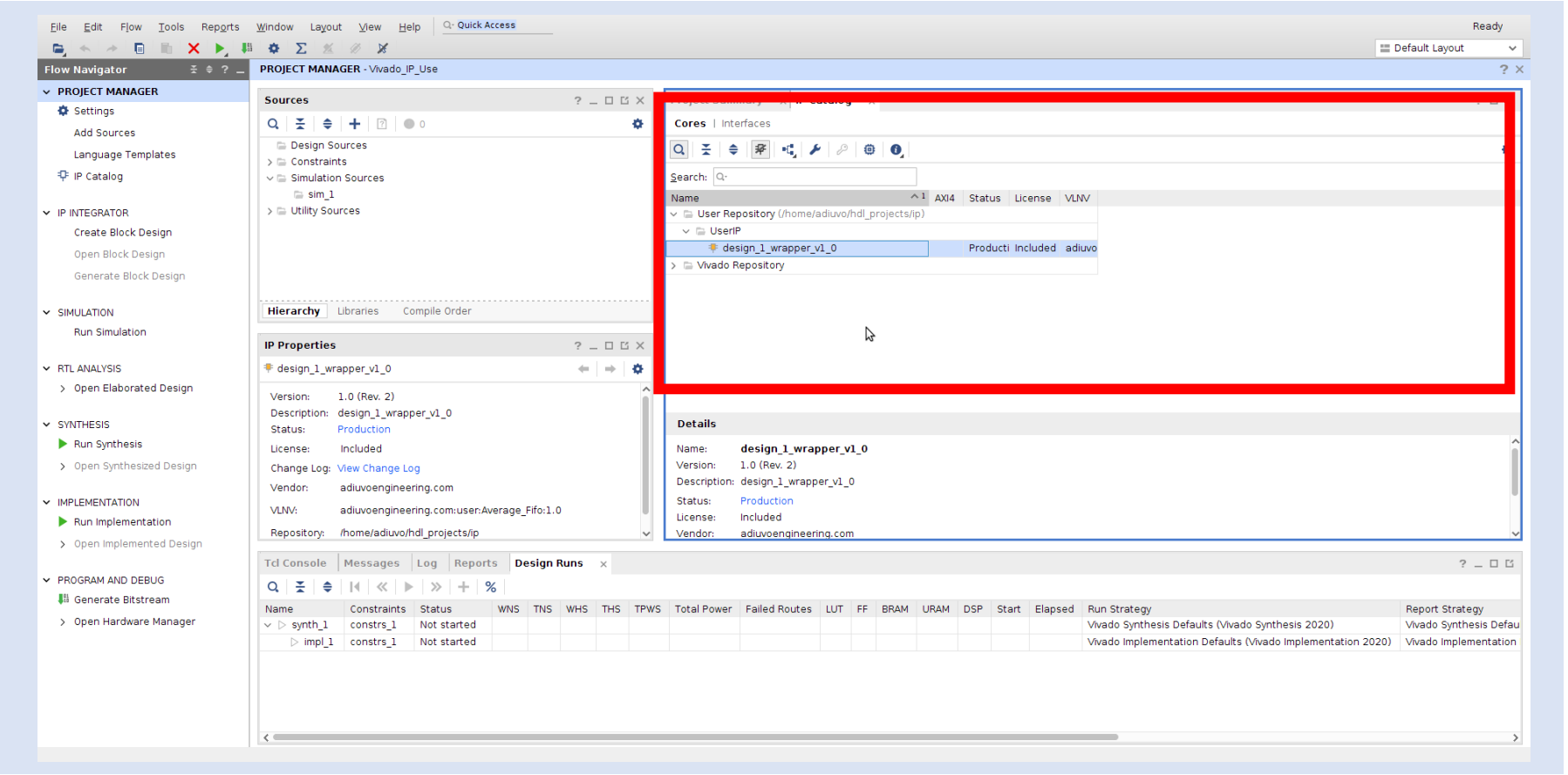
Lab 3: Advanced Vivado

Step 44 – Select the **component ZIP file** in the file dialog and click **OK**.



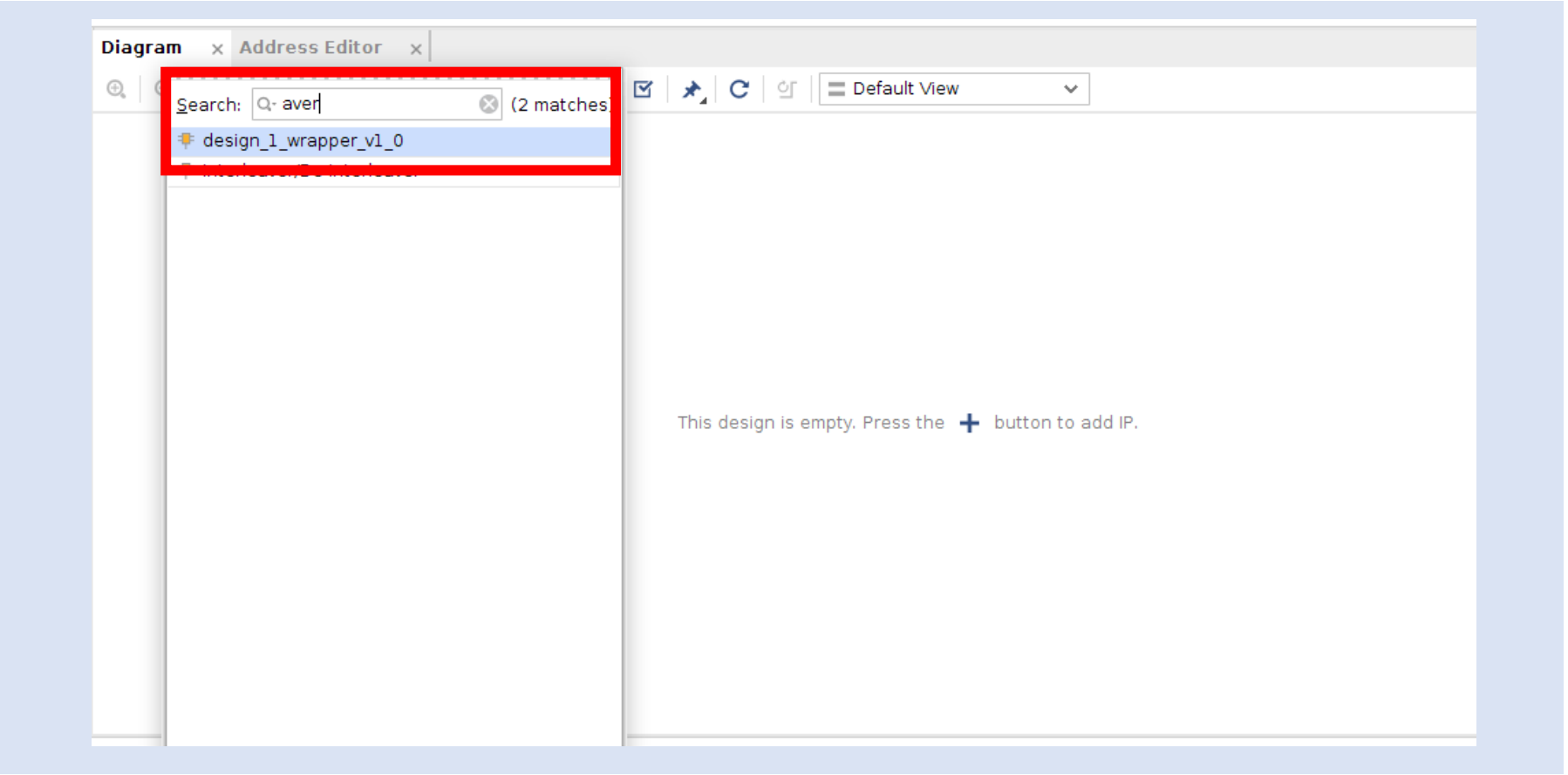
Lab 3: Advanced Vivado

Step 45 – You should now see the IP core in the library ready to go in our new design.



Lab 3: Advanced Vivado

Step 46 – Create a block design and type in the search bar average. Double click on the **design_1_wrapper_V1_0** which comes up.



Lab 3: Advanced Vivado

Step 47 – This will add in the Average block we have created and we are ready to go reusing it in our new developments.