
STM32
CubeMX

1. Description

1.1. Project

Project Name	helloworld
Board Name	STM32F723E-DISCO
Generated with:	STM32CubeMX 6.2.1
Date	05/02/2021

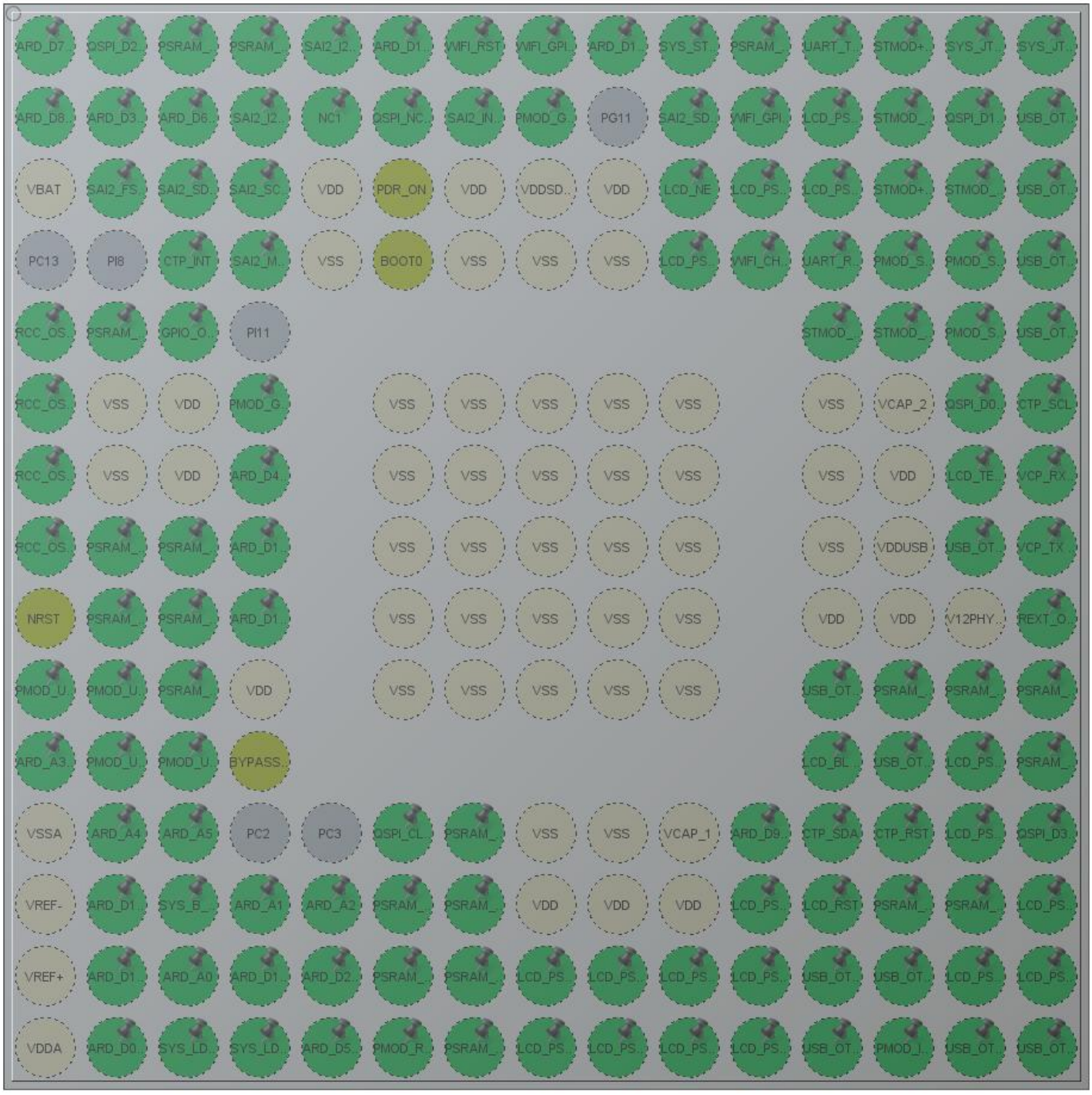
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x3
MCU name	STM32F723IEKx
MCU Package	UFBGA176
MCU Pin number	201

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



UFBGA176 +25 (Top view)

3. Pins Configuration

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	PE3 *	I/O	GPIO_Output	ARD_D7_GPIO
A2	PE2	I/O	QUADSPI_BK1_IO2	QSPI_D2 [MX25L51245G_SIO2]
A3	PE1	I/O	FMC_NBL1	PSRAM_NBL1 [IS66WV51216EBLL_UB]
A4	PE0	I/O	FMC_NBL0	PSRAM_NBL0 [IS66WV51216EBLL_LB]
A5	PB8	I/O	I2C1_SCL	SAI2_I2C1_SCL [WM8994ECS/R_SCLK]
A6	PB5	I/O	SPI1_MOSI	ARD_D11_TIM3_CH2_SPI1_MOSI
A7	PG14 *	I/O	GPIO_Output	WIFI_RST
A8	PG13 *	I/O	GPIO_Output	WIFI_GPIO_0
A9	PB4	I/O	SPI1_MISO	ARD_D12_SPI1_MISO
A10	PB3	I/O	SYS_JTDO-SWO	SYS_STLINK_JTDO_SWO
A11	PD7	I/O	FMC_NE1	PSRAM_NE1 [IS66WV51216EBLL_CS1]
A12	PC12	I/O	UART5_TX	UART_TXD_WIFI_RX
A13	PA15	I/O	TIM2_CH1	STMOD+_TIM2_CH1_2_ETR
A14	PA14	I/O	SYS_JTCK-SWCLK	
A15	PA13	I/O	SYS_JTMS-SWDIO	
B1	PE4 *	I/O	GPIO_Output	ARD_D8_GPIO
B2	PE5	I/O	TIM9_CH1	ARD_D3_TIM9_CH1
B3	PE6	I/O	TIM9_CH2	ARD_D6_TIM9_CH2
B4	PB9	I/O	I2C1_SDA	SAI2_I2C1_SDA [WM8994ECS_SDA]
B5	PB7	I/O	FMC_NL	NC1
B6	PB6	I/O	QUADSPI_BK1_NCS	QSPI_NCS [MX25L51245G_CS]
B7	PG15	I/O	GPIO_EXTI15	SAI2_INT [WM8994ECS_GPIO1]
B8	PG12 *	I/O	GPIO_Output	PMOD_GPIO_0
B10	PG10	I/O	SAI2_SD_B	SAI2_SD_B [SAI2_SD_B_ADCDAT1]
B11	PD6 *	I/O	GPIO_Output	WIFI_GPIO_2
B12	PD0	I/O	FMC_D2	LCD_PSRAM_D2
B13	PC11 *	I/O	GPIO_Output	STMOD_UART4_RXD_s

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
B14	PC10	I/O	QUADSPI_BK1_IO1	QSPI_D1 [MX25L51245G_SIO1]
B15	PA12	I/O	USB_OTG_FS_DP	
C1	VBAT	Power		
C2	PI7	I/O	SAI2_FS_A	SAI2_FS_A [WM8994ECS_LRCLK1]
C3	PI6	I/O	SAI2_SD_A	SAI2_SD_A [WM8994ECS_DACDAT1]
C4	PI5	I/O	SAI2_SCK_A	SAI2_SCK_A [WM8994ECS_BCLK1]
C5	VDD	Power		
C6	PDR_ON	Reset		
C7	VDD	Power		
C8	VDDSDMMC	Power		
C9	VDD	Power		
C10	PG9	I/O	FMC_NE2	LCD_NE
C11	PD5	I/O	FMC_NWE	LCD_PSRAM_NWE
C12	PD1	I/O	FMC_D3	LCD_PSRAM_D3
C13	PI3	I/O	SPI2_MOSI	STMOD+_SPI2_MOSIs
C14	PI2	I/O	SPI2_MISO	STMOD_SPI2_MISOs
C15	PA11	I/O	USB_OTG_FS_DM	
D3	PI9	I/O	GPIO_EXTI9	CTP_INT
D4	PI4	I/O	SAI2_MCLK_A	SAI2_MCLK_A [WM8994ECS_MCLK1]
D5	VSS	Power		
D6	BOOT0	Boot		
D7	VSS	Power		
D8	VSS	Power		
D9	VSS	Power		
D10	PD4	I/O	FMC_NOE	LCD_PSRAM_NWE
D11	PD3 *	I/O	GPIO_Output	WIFI_CH_PD
D12	PD2	I/O	UART5_RX	UART_RXD_WIFI_TX
D13	PH15 *	I/O	GPIO_Output	PMOD_SEL_0
D14	PI1	I/O	SPI2_SCK	PMOD_SPI2_SCK
D15	PA10 *	I/O	GPIO_Output	USB_OTG_FS_ID
E1	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
E2	PF0	I/O	FMC_A0	PSRAM_A0
E3	PI10 *	I/O	GPIO_Output	
E12	PH13	I/O	UART4_TX	STMOD_UART4_TXD
E13	PH14	I/O	UART4_RX	STMOD_UART4_RXD

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
E14	PI0	I/O	SPI2_NSS	PMOD_SPI2_NSS
E15	PA9	I/O	USB_OTG_FS_VBUS	
F1	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
F2	VSS	Power		
F3	VDD	Power		
F4	PH2 *	I/O	GPIO_Output	PMOD_GPIO_1
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F12	VSS	Power		
F13	VCAP_2	Power		
F14	PC9	I/O	QUADSPI_BK1_IO0	QSPI_D0 [MX25L51245G_SIO0]
F15	PA8	I/O	I2C3_SCL	CTP_SCL
G1	PH0-OSC_IN	I/O	RCC_OSC_IN	
G2	VSS	Power		
G3	VDD	Power		
G4	PH3 *	I/O	GPIO_Output	ARD_D4_GPIO
G6	VSS	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G12	VSS	Power		
G13	VDD	Power		
G14	PC8	I/O	GPIO_EXTI8	LCD_TE_INT
G15	PC7	I/O	USART6_RX	VCP_RX [STM32F103CBT6_PA2]
H1	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
H2	PF2	I/O	FMC_A2	PSRAM_A2
H3	PF1	I/O	FMC_A1	PSRAM_A1
H4	PH4	I/O	I2C2_SCL	ARD_D15_STMOD_I2C2_SCL
H6	VSS	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		

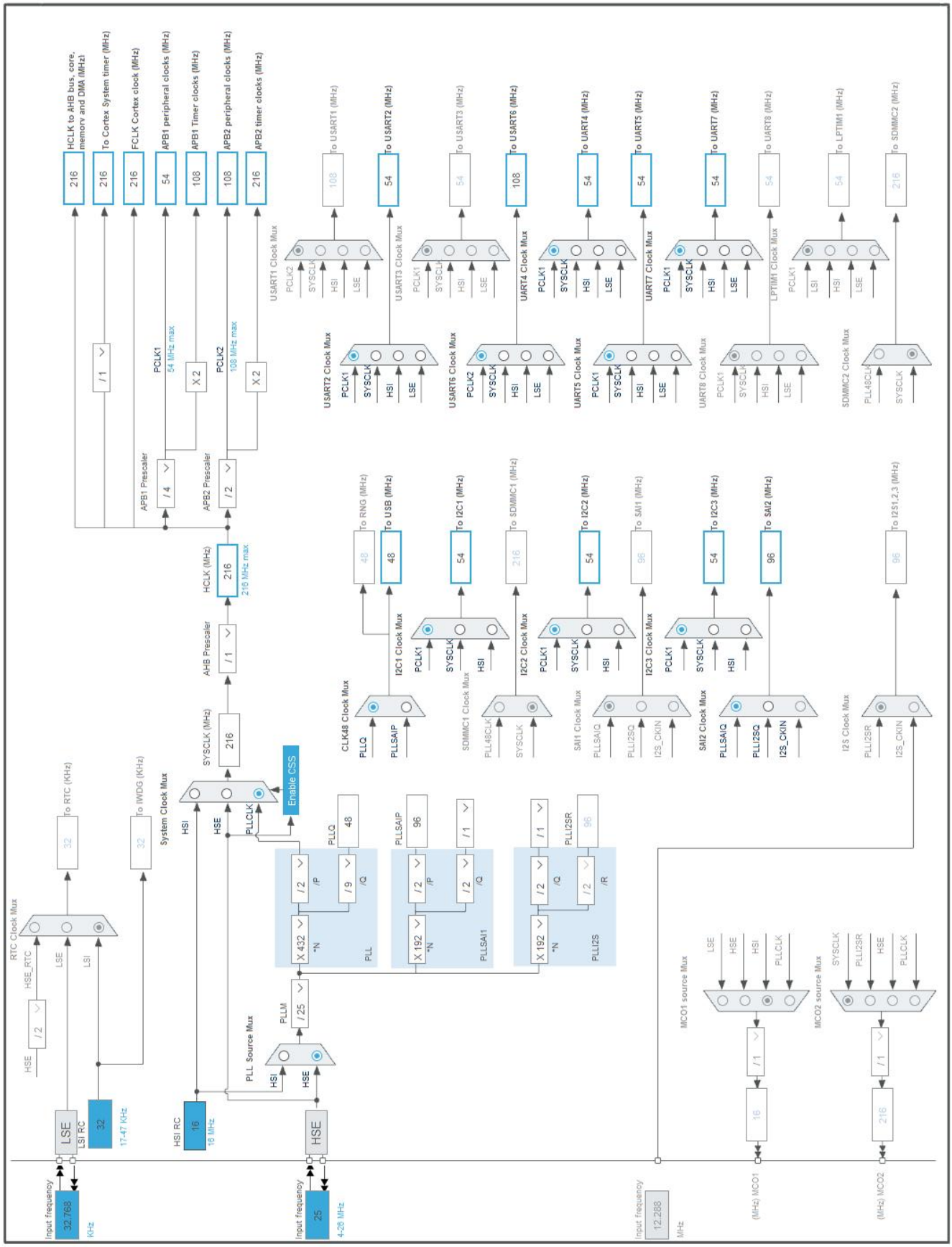
Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
H12	VSS	Power		
H13	VDDUSB	Power		
H14	PG8 *	I/O	GPIO_Output	USB_OTGFS_PPWR_EN
H15	PC6	I/O	USART6_TX	VCP_TX [STM32F103CBT6_PA3]
J1	NRST	Reset		
J2	PF3	I/O	FMC_A3	PSRAM_A3
J3	PF4	I/O	FMC_A4	PSRAM_A4
J4	PH5	I/O	I2C2_SDA	ARD_D14_STMOD_I2C2_SDA
J6	VSS	Power		
J7	VSS	Power		
J8	VSS	Power		
J9	VSS	Power		
J10	VSS	Power		
J12	VDD	Power		
J13	VDD	Power		
J14	V12PHYHS	Power		
J15	REXTPHYHS	MonoIO	USB_OTG_HS_REXTPHYHS	REXT_OTGPHY
K1	PF7	I/O	UART7_TX	PMOD_UART7_TXD
K2	PF6	I/O	UART7_RX	PMOD_UART7_RXD
K3	PF5	I/O	FMC_A5	PSRAM_A5
K4	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K12	PH12 *	I/O	GPIO_Output	USB_OTGHS_PPWR_EN
K13	PG5	I/O	FMC_A15	PSRAM_A15
K14	PG4	I/O	FMC_A14	PSRAM_A14
K15	PG3	I/O	FMC_A13	PSRAM_A13
L1	PF10	I/O	ADC3_IN8	ARD_A3_ADC3_IN8
L2	PF9	I/O	UART7_CTS	PMOD_UART7_CTS
L3	PF8	I/O	UART7_RTS	PMOD_UART7_RTS
L4	BYPASS_REG	Reset		
L12	PH11	I/O	TIM5_CH2	LCD_BL [STLD40DPUR_EN]
L13	PH10 *	I/O	GPIO_Input	USB_OTGHS_OVCR_INT

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
L14	PD15	I/O	FMC_D1	LCD_PSRAM_D1
L15	PG2	I/O	FMC_A12	PSRAM_A12
M1	VSSA	Power		
M2	PC0	I/O	ADC1_IN10, ADC2_IN10	ARD_A4
M3	PC1	I/O	ADC1_IN11, ADC2_IN11	ARD_A5
M6	PB2	I/O	QUADSPI_CLK	QSPI_CLK [MX25L51245G_SCLK]
M7	PG1	I/O	FMC_A11	PSRAM_A11
M8	VSS	Power		
M9	VSS	Power		
M10	VCAP_1	Power		
M11	PH6	I/O	TIM12_CH1	ARD_D9_TIM12_CH1
M12	PH8	I/O	I2C3_SDA	CTP_SDA
M13	PH9 *	I/O	GPIO_Output	CTP_RST
M14	PD14	I/O	FMC_D0	LCD_PSRAM_D0
M15	PD13	I/O	QUADSPI_BK1_IO3	QSPI_D3 [MX25L51245G_SIO3]
N1	VREF-	Power		
N2	PA1	I/O	TIM2_CH2	ARD_D10_TIM2_CH2_SPI1_NSS
N3	PA0-WKUP	I/O	SYS_WKUP1	SYS_B_User
N4	PA4	I/O	ADC1_IN4, ADC2_IN4	ARD_A1
N5	PC4	I/O	ADC1_IN14, ADC2_IN14	ARD_A2
N6	PF13	I/O	FMC_A7	PSRAM_A7
N7	PG0	I/O	FMC_A10	PSRAM_A10
N8	VDD	Power		
N9	VDD	Power		
N10	VDD	Power		
N11	PE13	I/O	FMC_D10	LCD_PSRAM_D10
N12	PH7 *	I/O	GPIO_Output	LCD_RST
N13	PD12	I/O	FMC_A17	PSRAM_A17
N14	PD11	I/O	FMC_A16	PSRAM_A16
N15	PD10	I/O	FMC_D15	LCD_PSRAM_D15
P1	VREF+	Power		
P2	PA2	I/O	USART2_TX	ARD_D1_USART2_TX
P3	PA6	I/O	ADC1_IN6, ADC2_IN6	ARD_A0
P4	PA5	I/O	SPI1_SCK	ARD_D13_SPI1_SCK
P5	PC5 *	I/O	GPIO_Output	ARD_D2_GPIO
P6	PF12	I/O	FMC_A6	PSRAM_A6
P7	PF15	I/O	FMC_A9	PSRAM_A9

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
P8	PE8	I/O	FMC_D5	LCD_PSRAM_D5
P9	PE9	I/O	FMC_D6	LCD_PSRAM_D6
P10	PE11	I/O	FMC_D8	LCD_PSRAM_D8
P11	PE14	I/O	FMC_D11	LCD_PSRAM_D11
P12	PB12 *	I/O	GPIO_Output	USB_OTG_HS_ID
P13	PB13	I/O	GPIO_EXTI13	USB_OTG_HS_VBUS
P14	PD9	I/O	FMC_D14	LCD_PSRAM_D14
P15	PD8	I/O	FMC_D13	LCD_PSRAM_D13
R1	VDDA	Power		
R2	PA3	I/O	USART2_RX	ARD_D0_USART2_RX
R3	PA7 *	I/O	GPIO_Output	SYS_LD_USER1
R4	PB1 *	I/O	GPIO_Output	SYS_LD_USER2
R5	PB0	I/O	TIM3_CH3	ARD_D5_STMOD_TIM3_CH3
R6	PF11 *	I/O	GPIO_Input	PMOD_RESET
R7	PF14	I/O	FMC_A8	PSRAM_A8
R8	PE7	I/O	FMC_D4	LCD_PSRAM_D4
R9	PE10	I/O	FMC_D7	LCD_PSRAM_D7
R10	PE12	I/O	FMC_D9	LCD_PSRAM_D9
R11	PE15	I/O	FMC_D12	LCD_PSRAM_D12
R12	PB10	I/O	GPIO_EXTI10	USB_OTGFS_OVCR_INT
R13	PB11	I/O	GPIO_EXTI11	PMOD_INT
R14	PB14	I/O	USB_OTG_HS_DM	
R15	PB15	I/O	USB_OTG_HS_DP	

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	helloworld
Project Folder	C:\stm32\helloworld
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.16.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ADC1_Init	ADC1
4	MX_ADC2_Init	ADC2
5	MX_ADC3_Init	ADC3
6	MX_FMC_Init	FMC
7	MX_I2C1_Init	I2C1
8	MX_I2C2_Init	I2C2
9	MX_I2C3_Init	I2C3
10	MX_QUADSPI_Init	QUADSPI
11	MX_SAI2_Init	SAI2

Rank	Function Name	Peripheral Instance Name
12	MX_SPI1_Init	SPI1
13	MX_SPI2_Init	SPI2
14	MX_TIM2_Init	TIM2
15	MX_TIM3_Init	TIM3
16	MX_TIM5_Init	TIM5
17	MX_TIM9_Init	TIM9
18	MX_TIM12_Init	TIM12
19	MX_UART4_Init	UART4
20	MX_UART5_Init	UART5
21	MX_UART7_Init	UART7
22	MX_USART2_UART_Init	USART2
23	MX_USART6_UART_Init	USART6
24	MX_USB_HOST_Init	USB_HOST

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x3
MCU	STM32F723IEKx
Datasheet	DS11853_Rev3

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

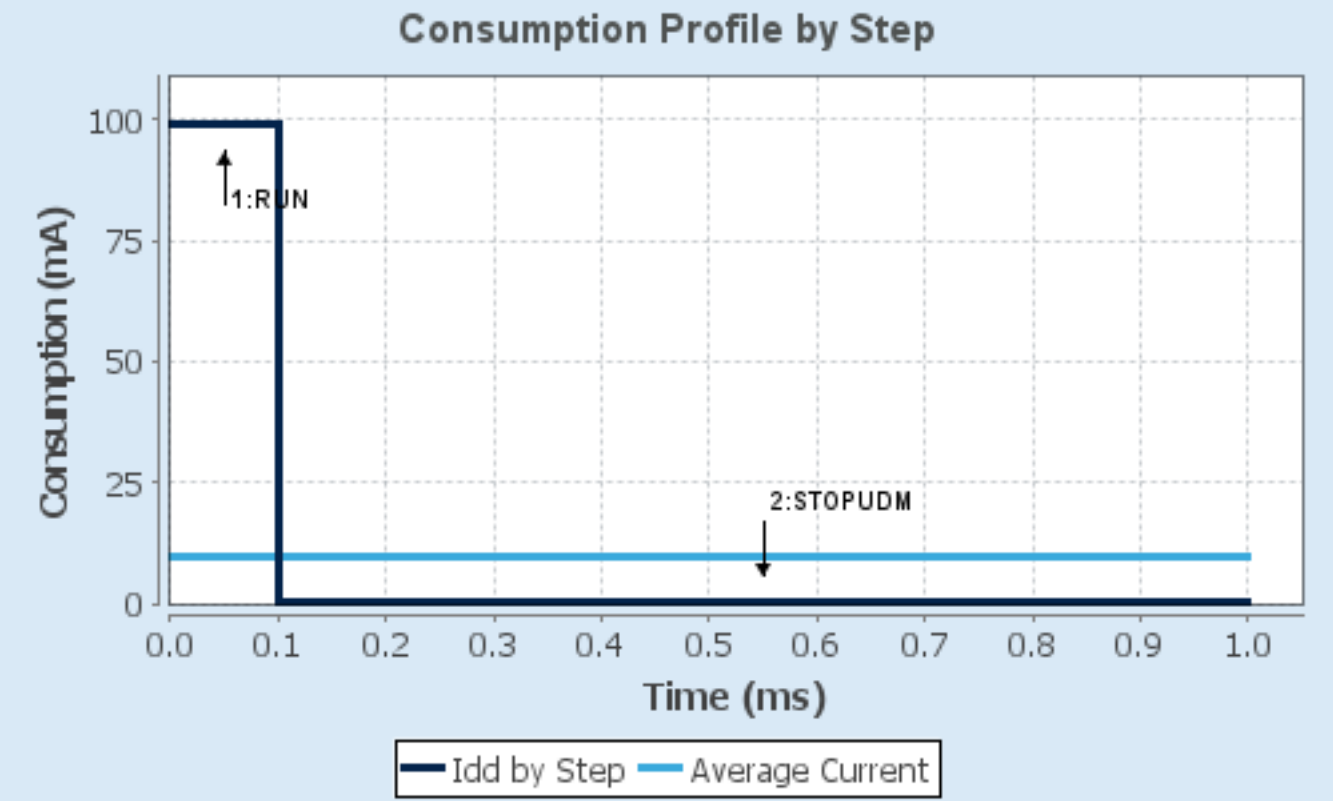
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ITCM RAM REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	99 mA	100 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	91.61	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	9.99 mA
Battery Life	2 days, 14 hours	Average DMIPS	462.24005 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
100
75
50
25
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN4

mode: IN6

mode: IN10

mode: IN11

mode: IN14

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 4
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ADC2

mode: IN4

mode: IN6

mode: IN10

mode: IN11

mode: IN14

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 4
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.3. ADC3

mode: IN8

7.3.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled

End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 8
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.4. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: PSRAM

Address: 18 bits

Data: 16 bits

Address valid: set

Byte enable: 16-bit byte enable

NOR Flash/PSRAM/SRAM/ROM/LCD 2

Chip Select: NE2

Memory type: LCD Interface

LCD Register Select: A0

Data: 16 bits

7.4.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	PSRAM
Bank	Bank 1 NOR/PSRAM 1
Write operation	**Enabled ***
Write FIFO	Enabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	255

Bus turn around time in HCLK clock cycles	15

7.4.2. NOR/PSRAM 2:

NOR/PSRAM control:

Memory type	LCD Interface
Bank	Bank 1 NOR/PSRAM 2
Write operation	Enabled
Write FIFO	Enabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	255
Bus turn around time in HCLK clock cycles	15

7.5. I2C1

I2C: I2C

7.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x6000030D ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.6. I2C2

I2C: I2C

7.6.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.7. I2C3

I2C: I2C

7.7.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x6000030D ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.8. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.8.1. Parameter Settings:

General Parameters:

Clock Prescaler	**1 ***
Fifo Threshold	**16 ***
Sample Shifting	**Sample Shifting Half Cycle ***
Flash Size	**26 ***
Chip Select High Time	**4 Cycles ***
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

7.9. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.9.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.10. SAI2

Mode: Master with Master Clock Out

Mode: Synchronous Slave

7.10.1. Parameter Settings:

SAI A:

Synchronization Inputs	Asynchronous
Basic Parameters	
Protocol	Free
Audio Mode	Master Transmit
Frame Length	8 bits
Data Size	8 Bits
Slot Size	DataSize
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Frame Parameters	
First Bit	MSB First
Frame Synchro Active Level Length	1
Frame Synchro Definition	Start Frame
Frame Synchro Polarity	Active Low
Frame Synchro Offset	First Bit
Slot Parameters	
First Bit Offset	0
Number of Slots	1
Slot Active Final Value	0x00000000
Slot Active	Neither
Clock Parameters	
Master Clock Divider	Enabled
Audio Frequency	192 KHz
Real Audio Frequency	**187.5 KHz ***
Error between Selected	**-2.34 % ***
Clock Strobing	Falling Edge
Advanced Parameters	
Fifo Threshold	Empty
Output Drive	Disabled

SAI B:

Synchronization Inputs	Synchronous with other block of same SAI
Basic Parameters	
Protocol	Free
Audio Mode	Slave Receive
Frame Length (only Even Values)	8
Data Size	8 Bits
Slot Size	DataSize
Output Mode	Stereo
Companding Mode	No companding mode

SAI SD Line Output Mode	Driven
Frame Parameters	
First Bit	MSB First
Frame Synchro Active Level Length	1
Frame Synchro Definition	Start Frame
Frame Synchro Polarity	Active Low
Frame Synchro Offset	First Bit
Slot Parameters	
First Bit Offset	0
Number of Slots	1
Slot Active Final Value	0x00000000
Slot Active	Neither
Clock Parameters	
Real Audio Frequency	0
Error between Selected	0
Clock Strobing	Falling Edge
Advanced Parameters	
Fifo Threshold	Empty
Output Drive	Disabled

7.11. SPI1

Mode: Full-Duplex Master

7.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**27.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.12. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**64 ***
Baud Rate	**843.75 KBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware

7.13. SYS

Debug: Trace Asynchronous Sw

mode: System Wake-Up 1

Timebase Source: TIM1

7.14. TIM2

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.15. TIM3

Channel3: PWM Generation CH3

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.16. TIM5

Channel2: PWM Generation CH2

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.17. TIM9

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable

Fast Mode	Disable
CH Polarity	High

7.18. TIM12

Channel1: PWM Generation CH1

7.18.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.19. UART4

Mode: Asynchronous

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable

Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.20. UART5

Mode: Asynchronous

7.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.21. UART7

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.21.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.22. USART2

Mode: Asynchronous

7.22.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.23. USART6

Mode: Asynchronous

7.23.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.24. USB_OTG_FS

Mode: Host_Only

Activate_VBUS: VBUS sensing

7.24.1. Parameter Settings:

Signal start of frame	Disabled
Speed	Full Speed 12MBit/s

7.25. USB_OTG_HS

Internal Phy HS: Host_Only

7.25.1. Parameter Settings:

Signal start of frame	Disabled
Speed	High Speed 480MBit/s
Enable internal IP DMA	Disabled
Physical interface	Internal Phy

7.26. USB_HOST

Class For HS IP: Audio Host Class

Class for FS IP: Mass Storage Host Class

7.26.1. Parameter Settings:

Host Configuration:

USBH_MAX_NUM_ENDPOINTS (Maximum number of endpoints)	2
USBH_MAX_NUM_INTERFACES (Maximun number of interfaces)	10
USBH_MAX_NUM_SUPPORTED_CLASS (Maximun number of supported class)	1
USBH_MAX_NUM_CONFIGURATION (Maximun number of supported configuration)	1
USBH_KEEP_CFG_DESCRIPTOR (Keep the configuration into RAM)	Enabled
USBH_MAX_SIZE_CONFIGURATION (Maximun size in bytes for the Configuration Descriptor)	256
USBH_MAX_DATA_BUFFER (Maximun size of temporary data)	512
USBH_DEBUG_LEVEL (USBH Debug Level)	0: No debug message

CMSIS_RTOS:

USBH_USE_OS (Enable the support of an RTOS)	Disabled

7.26.2. Platform Settings:

Drive_VBUS_FS	PG8
Drive_VBUS_HS	PH12

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	ARD_A4
	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	ARD_A5
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	ARD_A1
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	ARD_A2
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	ARD_A0
ADC2	PC0	ADC2_IN10	Analog mode	No pull-up and no pull-down	n/a	ARD_A4
	PC1	ADC2_IN11	Analog mode	No pull-up and no pull-down	n/a	ARD_A5
	PA4	ADC2_IN4	Analog mode	No pull-up and no pull-down	n/a	ARD_A1
	PC4	ADC2_IN14	Analog mode	No pull-up and no pull-down	n/a	ARD_A2
	PA6	ADC2_IN6	Analog mode	No pull-up and no pull-down	n/a	ARD_A0
ADC3	PF10	ADC3_IN8	Analog mode	No pull-up and no pull-down	n/a	ARD_A3_ADC3_IN8
FMC	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_NBL1 [IS66WV51216EBLL_UB]
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_NBL0 [IS66WV51216EBLL_LB]
	PD7	FMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_NE1 [IS66WV51216EBLL_CS1]
	PB7	FMC_NL	Alternate Function Push Pull	No pull-up and no pull-down	Very High	NC1
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D2
	PG9	FMC_NE2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_NE
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_NWE
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D3
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_NWE
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A0
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A2
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A1
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A3
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A4
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A5
	PG5	FMC_A15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A15
	PG4	FMC_A14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A14
	PG3	FMC_A13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A13
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D1
	PG2	FMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A12
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A11
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D0
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A7

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A10
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D10
	PD12	FMC_A17	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A17
	PD11	FMC_A16	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A16
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D15
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A6
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A9
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D5
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D6
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D8
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D11
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D14
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D13
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PSRAM_A8
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D4
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D7
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D9
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	LCD_PSRAM_D12
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	SAI2_I2C1_SCL [WM8994ECS/R_SCLK]
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	SAI2_I2C1_SDA [WM8994ECS_SDA]
I2C2	PH4	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	ARD_D15_STMOD_I2C2_SCL
	PH5	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	ARD_D14_STMOD_I2C2_SDA
I2C3	PA8	I2C3_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	CTP_SCL
	PH8	I2C3_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	CTP_SDA
QUADSPI	PE2	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D2 [MX25L51245G_SIO2]
	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_NCS [MX25L51245G_CS]
	PC10	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D1 [MX25L51245G_SIO1]
	PC9	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D0 [MX25L51245G_SIO0]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_CLK [MX25L51245G_SCLK]
	PD13	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D3 [MX25L51245G_SIO3]
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SAI2	PG10	SAI2_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_SD_B [SAI2_SD_B_ADCDAT1]
	PI7	SAI2_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_FS_A [WM8994ECS_LRCLK1]
	PI6	SAI2_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_SD_A [WM8994ECS_DACDAT1]
	PI5	SAI2_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_SCK_A [WM8994ECS_BCLK1]
	PI4	SAI2_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_MCLK_A [WM8994ECS_MCLK1]
SPI1	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARD_D11_TIM3_CH2_SPI1_MOSI
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARD_D12_SPI1_MISO
	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARD_D13_SPI1_SCK
SPI2	PI3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STMOD+_SPI2_MOSIs
	PI2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STMOD_SPI2_MISOs
	PI1	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	PMOD_SPI2_SCK
	PI0	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	PMOD_SPI2_NSS
SYS	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SYS_STLINK_JTDO_SWO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA0-WKUP	SYS_WKUP1	n/a	n/a	n/a	SYS_B_User
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	STMOD+_TIM2_CH1_2_ETR
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARD_D10_TIM2_CH2_SPI1_NSS
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARD_D5_STMOD_TIM3_CH3
TIM5	PH11	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_BL [STLD40DPUR_EN]
TIM9	PE5	TIM9_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARD_D3_TIM9_CH1
	PE6	TIM9_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARD_D6_TIM9_CH2
TIM12	PH6	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ARD_D9_TIM12_CH1
UART4	PH13	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STMOD_UART4_TXD
	PH14	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STMOD_UART4_RXD
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	UART_TXD_WIFI_RX
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	UART_RXD_WIFI_TX
UART7	PF7	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	PMOD_UART7_TXD
	PF6	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	PMOD_UART7_RXD
	PF9	UART7_CTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	PMOD_UART7_CTS
	PF8	UART7_RTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	PMOD_UART7_RTS
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARD_D1_USART2_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ARD_D0_USART2_RX
USART6	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	VCP_RX [STM32F103CBT6_PA2]
	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	VCP_TX [STM32F103CBT6_PA3]
USB_OTG_	PA12	USB_OTG_FS_	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FS		DP			*	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	**n/a**	
USB_OTG_HS	REXTPHYHS	USB_OTG_HS_REXTPHYHS	n/a	n/a	n/a	REXT_OTGPHY
	PB14	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB15	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARD_D7_GPIO
	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WIFI_RST
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WIFI_GPIO_0
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARD_D8_GPIO
	PG15	GPIO_EXTI15	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	SAI2_INT [WM8994ECS_GPIO1]
	PG12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PMOD_GPIO_0
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WIFI_GPIO_2
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	STMOD_UART4_RXD_s
	PI9	GPIO_EXTI9	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	CTP_INT
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WIFI_CH_PD
	PH15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PMOD_SEL_0
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_OTG_FS_ID
	PI10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PH2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PMOD_GPIO_1
	PH3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARD_D4_GPIO
	PC8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	LCD_TE_INT
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_OTGFS_PPWR_EN
	PH12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_OTGHS_PPWR_EN
	PH10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OTGHS_OVCR_INT
	PH9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CTP_RST
	PH7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RST
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ARD_D2_GPIO
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_OTG_HS_ID
	PB13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_OTG_HS_VBUS
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SYS_LD_USER1
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SYS_LD_USER2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PMOD_RESET
	PB10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_OTGFS_OVCR_INT
	PB11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	PMOD_INT

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
USB On The Go FS global interrupt	true	0	0
USB On The Go HS global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
EXTI line[9:5] interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM5 global interrupt	unused		
UART4 global interrupt	unused		
UART5 global interrupt	unused		
USART6 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
USB On The Go HS End Point 1 Out global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
USB On The Go HS End Point 1 In global interrupt	unused		
FPU global interrupt	unused		
UART7 global interrupt	unused		
SAI2 global interrupt	unused		
QUADSPI global interrupt	unused		

8.3.2. NVIC Code generation

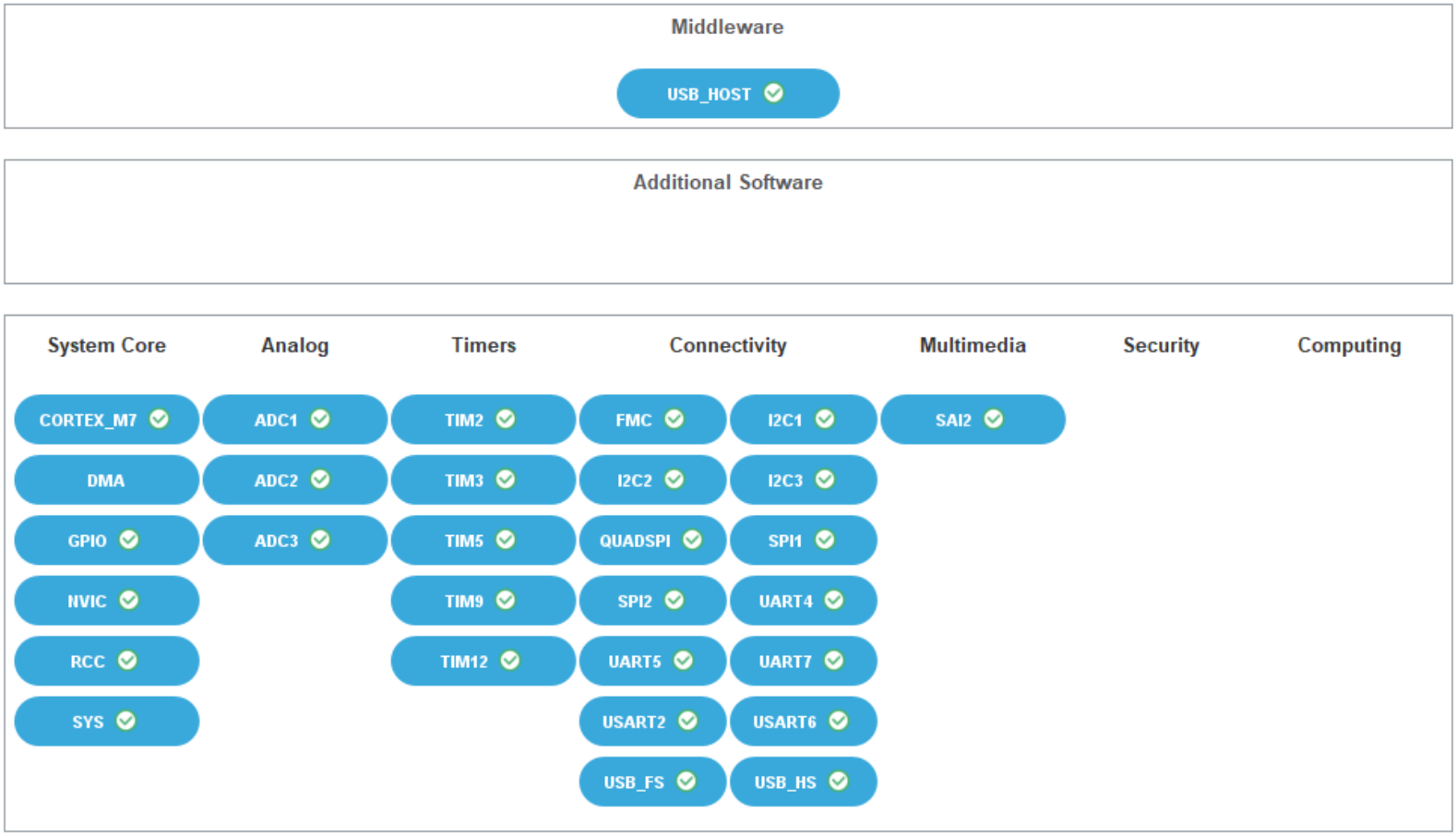
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM1 update interrupt and TIM10 global interrupt	false	true	true
USB On The Go FS global interrupt	false	true	true
USB On The Go HS global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Software Pack Report

10.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronics	X-CUBE-TOUCHGFX	4.16.1	Class : Graphics Group : Application Variant : TouchGFX Generator Version : 4.16.1

11. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00330506.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00305990.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00305994.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00164549.pdf
Application note	http://www.st.com/resource/en/application_note/DM00173083.pdf
Application note	http://www.st.com/resource/en/application_note/DM00210367.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf

Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00340311.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337702.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00600614.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf