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ENGINEERING AND TRAINING, LTD.

Signal Processing with FPGA, Python & no RTL Design!

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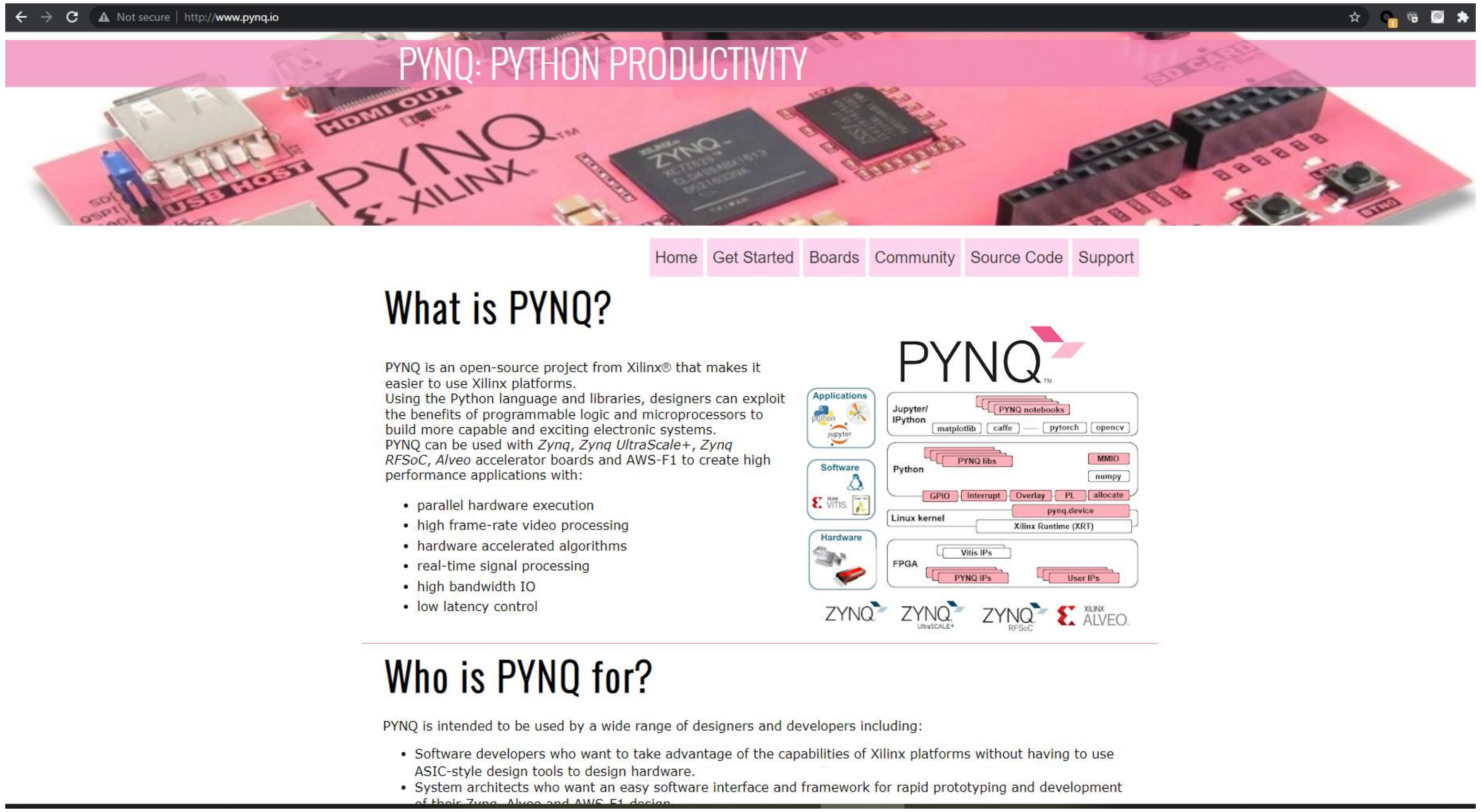
Lab : FFT Acceleration

Open a browser and go to

www.pynq.io



What is PYNQ?

PYNQ is an open-source project from Xilinx® that makes it easier to use Xilinx platforms.
Using the Python language and libraries, designers can exploit the benefits of programmable logic and microprocessors to build more capable and exciting electronic systems.
PYNQ can be used with *Zynq*, *Zynq UltraScale+*, *Zynq RFSoC*, *Alveo* accelerator boards and AWS-F1 to create high performance applications with:

- parallel hardware execution
- high frame-rate video processing
- hardware accelerated algorithms
- real-time signal processing
- high bandwidth IO
- low latency control

Who is PYNQ for?

PYNQ is intended to be used by a wide range of designers and developers including:

- Software developers who want to take advantage of the capabilities of Xilinx platforms without having to use ASIC-style design tools to design hardware.
- System architects who want an easy software interface and framework for rapid prototyping and development of their Zynq, Alveo and AWS-F1 design.

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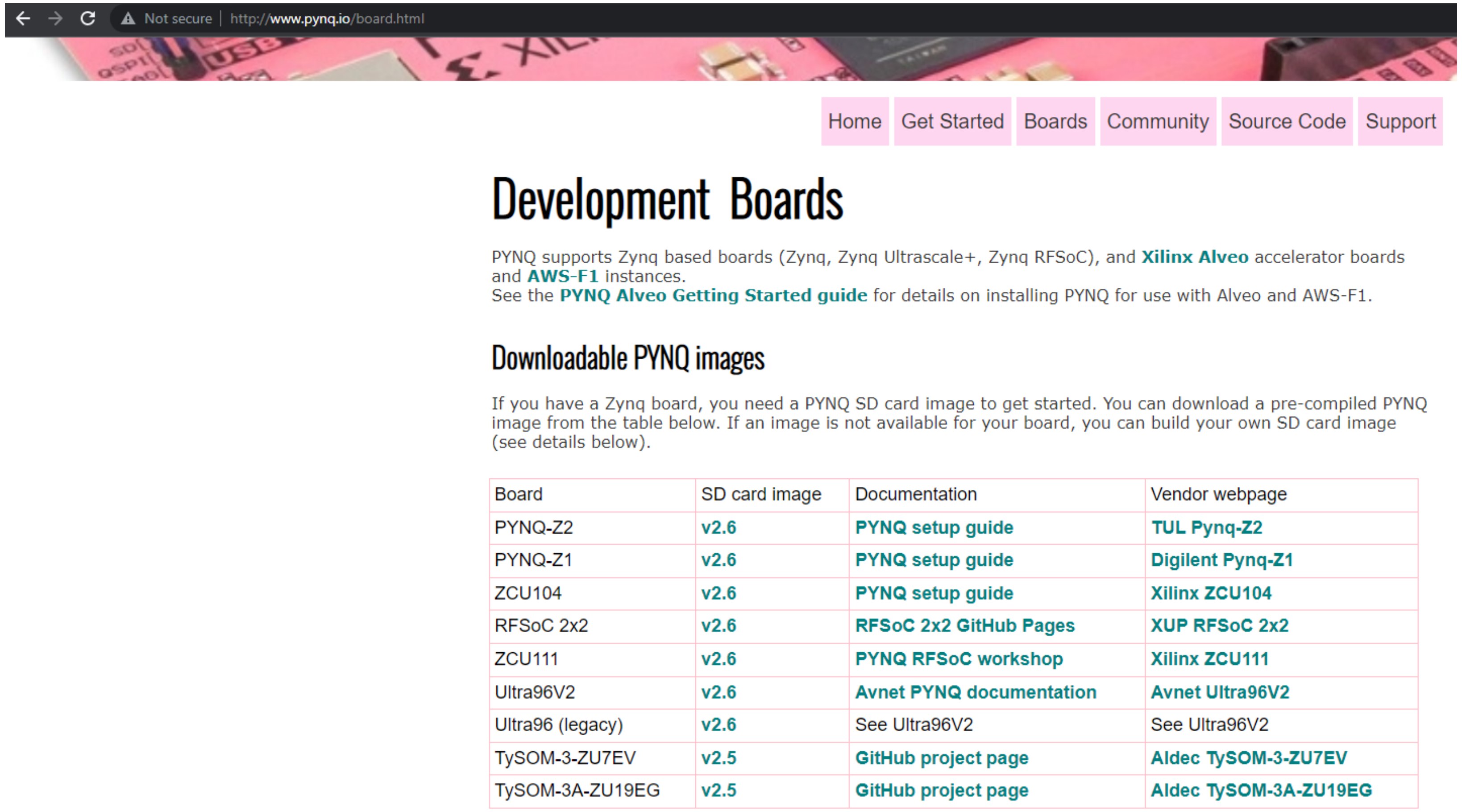
Select the boards page and

download the SD card

image for Pynq Z1 v2.6



Development Boards

PYNQ supports Zynq based boards (Zynq, Zynq Ultrascale+, Zynq RFSoC), and **Xilinx Alveo** accelerator boards and **AWS-F1** instances.
See the **PYNQ Alveo Getting Started guide** for details on installing PYNQ for use with Alveo and AWS-F1.

Downloadable PYNQ images

If you have a Zynq board, you need a PYNQ SD card image to get started. You can download a pre-compiled PYNQ image from the table below. If an image is not available for your board, you can build your own SD card image (see details below).

Board	SD card image	Documentation	Vendor webpage
PYNQ-Z2	**v2.6**	**PYNQ setup guide**	**TUL Pynq-Z2**
PYNQ-Z1	**v2.6**	**PYNQ setup guide**	**Digilent Pynq-Z1**
ZCU104	**v2.6**	**PYNQ setup guide**	**Xilinx ZCU104**
RFSoC 2x2	**v2.6**	**RFSoC 2x2 GitHub Pages**	**XUP RFSoC 2x2**
ZCU111	**v2.6**	**PYNQ RFSoC workshop**	**Xilinx ZCU111**
Ultra96V2	**v2.6**	**Avnet PYNQ documentation**	**Avnet Ultra96V2**
Ultra96 (legacy)	**v2.6**	See Ultra96V2	See Ultra96V2
TySOM-3-ZU7EV	**v2.5**	**GitHub project page**	**Aldec TySOM-3-ZU7EV**
TySOM-3A-ZU19EG	**v2.5**	**GitHub project page**	**Aldec TySOM-3A-ZU19EG**

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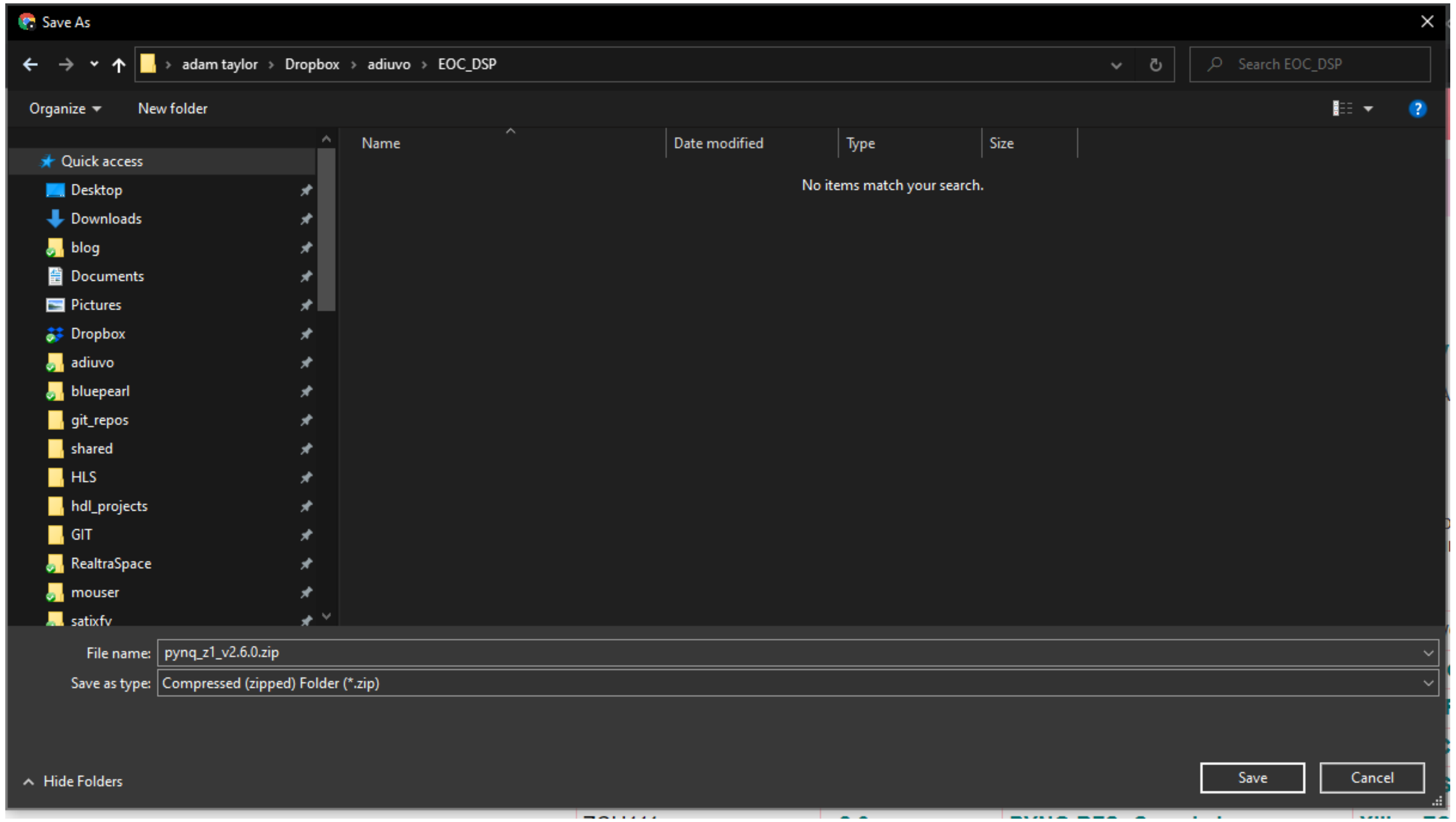
Save the SD Card image to a preferred location on your local computer


Save As

adam taylor › Dropbox › adiuvo › EOC_DSP

Search EOC_DSP

Organize ▾ New folder

Quick access
- Desktop
- Downloads
- blog
- Documents
- Pictures
- Dropbox
- adiuvo
- bluepearl
- git_repos
- shared
- HLS
- hdl_projects
- GIT
- RealtraSpace
- mouser
- satixfy

Name	Date modified	Type	Size

No items match your search.

File name: pynq_z1_v2.6.0.zip

Save as type: Compressed (zipped) Folder (*.zip)

Hide Folders

Save Cancel

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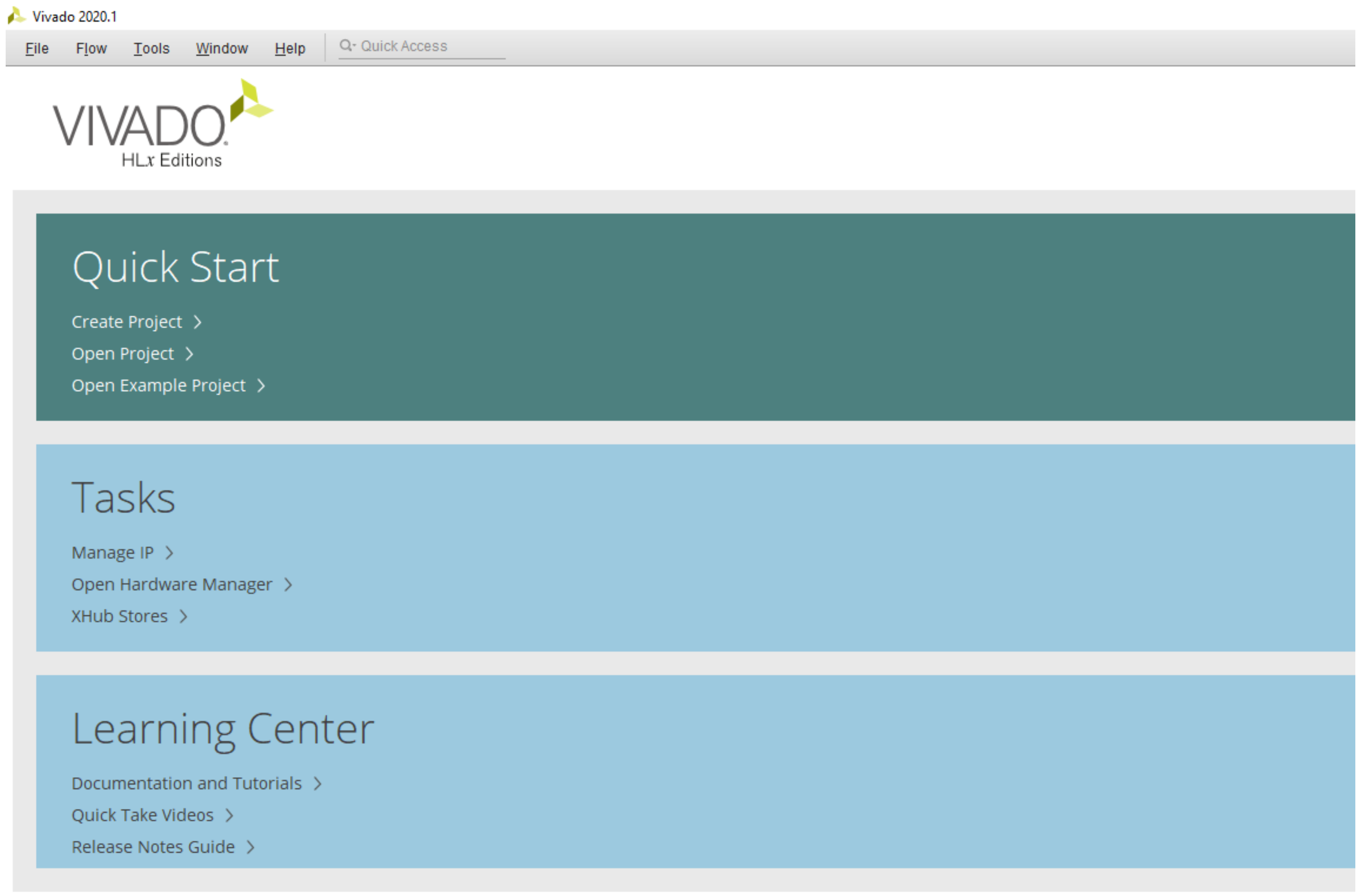
Open Vivado and select Xhub

Stores



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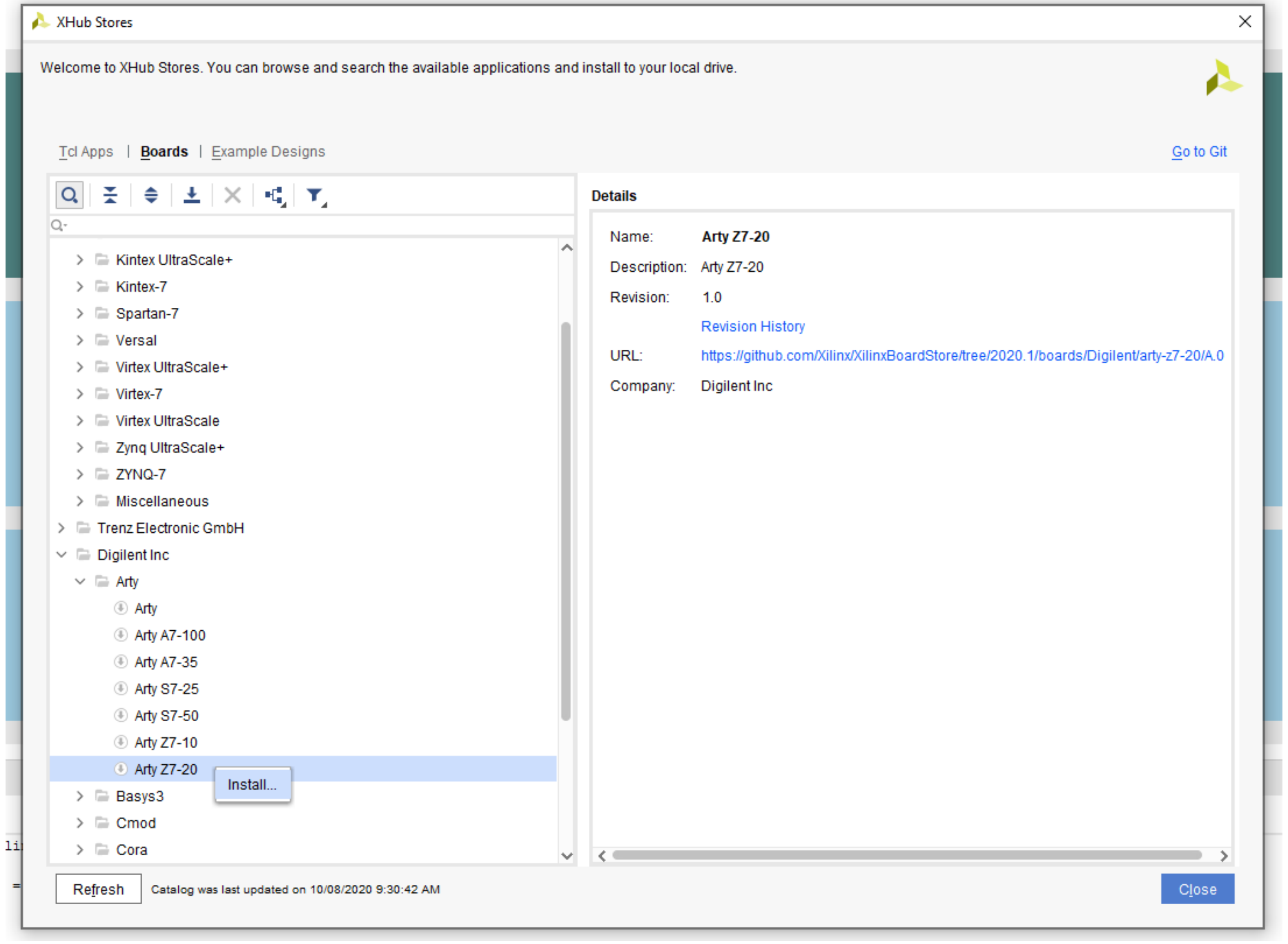
From the boards tab, select Digilent Inc folder. Expand the Arty directory and select Arty.

Right click on the Arty Z7-20 and select install


XHub Stores

Welcome to XHub Stores. You can browse and search the available applications and install to your local drive.

Tcl Apps | **Boards** | Example Designs   Go to Git

- Kintex UltraScale+
- Kintex-7
- Spartan-7
- Versal
- Virtex UltraScale+
- Virtex-7
- Virtex UltraScale
- Zynq UltraScale+
- ZYNQ-7
- Miscellaneous
- Trenz Electronic GmbH
- Digilent Inc
  - Arty
    - Arty
    - Arty A7-100
    - Arty A7-35
    - Arty S7-25
    - Arty S7-50
    - Arty Z7-10
    - Arty Z7-20
  - Basys3
  - Cmod
  - Cora

Details

Name:	**Arty Z7-20**
Description:	Arty Z7-20
Revision:	1.0
	Revision History
URL:	https://github.com/Xilinx/XilinxBoardStore/tree/2020.1/boards/Digilent/arty-z7-20/A.0
Company:	Digilent Inc

Catalog was last updated on 10/08/2020 9:30:42 AM

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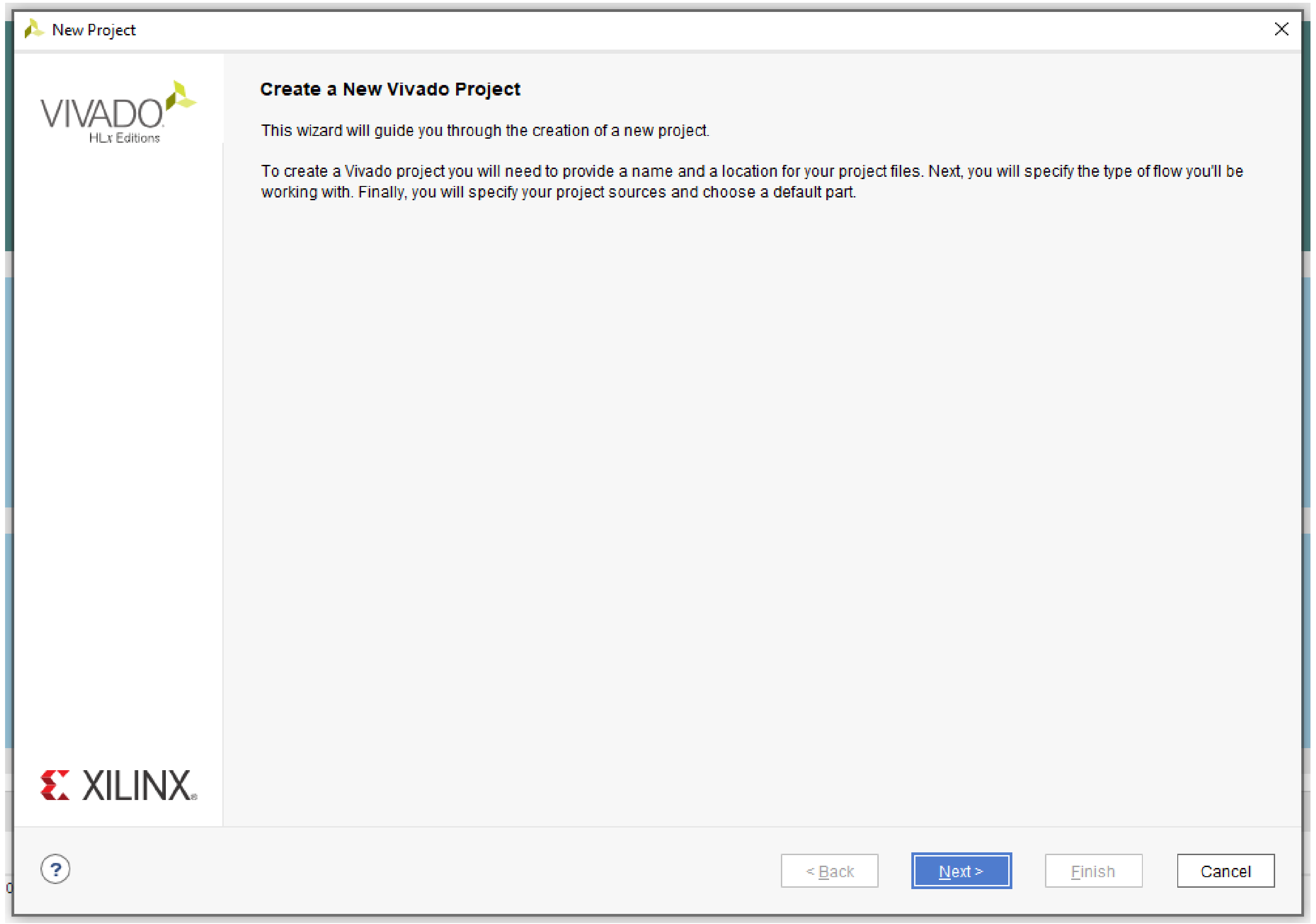
Create a new project



New Project

Create a New Vivado Project

This wizard will guide you through the creation of a new project.

To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.

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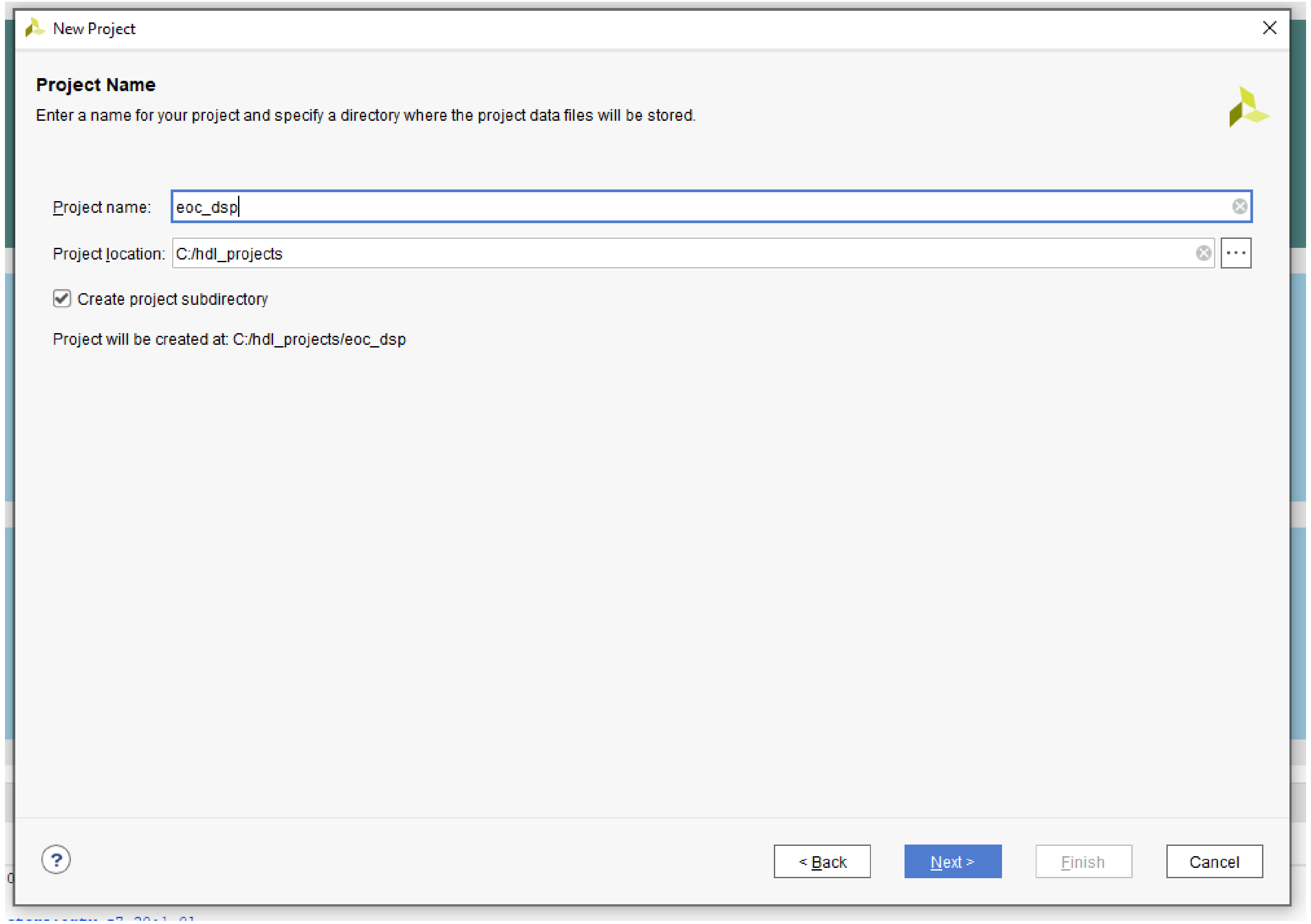
Enter a name and location



New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name: eoc_dsp

Project location: C:/hdl_projects

☑ Create project subdirectory

Project will be created at: C:/hdl_projects/eoc_dsp

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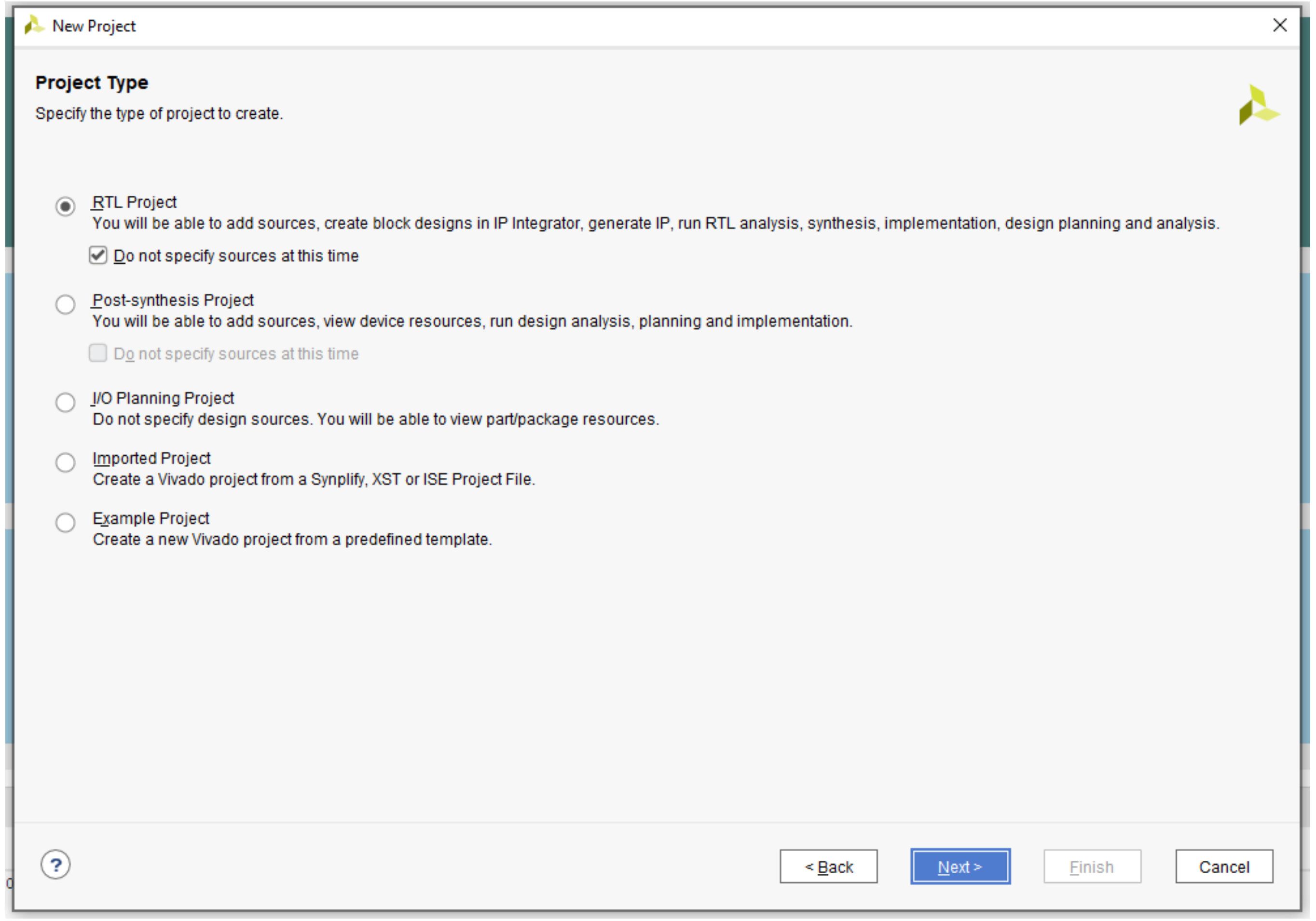
Select RTL Project



New Project

Project Type

Specify the type of project to create.

- [✓ RTL Project]
  You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
  ✓ Do not specify sources at this time
- Post-synthesis Project
  You will be able to add sources, view device resources, run design analysis, planning and implementation.
  Do not specify sources at this time
- I/O Planning Project
  Do not specify design sources. You will be able to view part/package resources.
- Imported Project
  Create a Vivado project from a Synplify, XST or ISE Project File.
- Example Project
  Create a new Vivado project from a predefined template.

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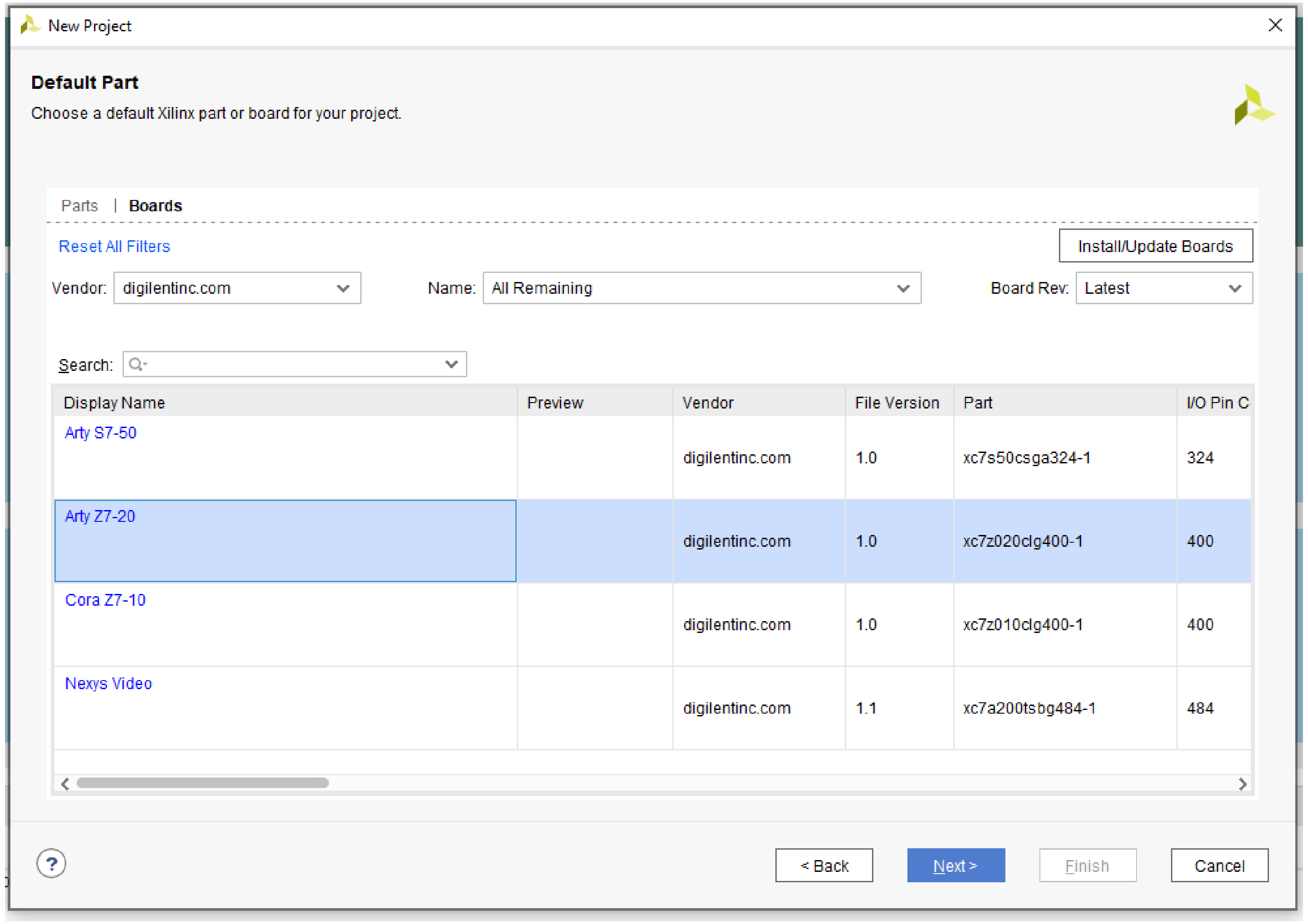
Select the Arty Z7-20 board



New Project

Default Part

Choose a default Xilinx part or board for your project.

Parts | **Boards**

Reset All Filters

Install/Update Boards

Vendor: digilentinc.com

Name: All Remaining

Board Rev: Latest

Search:

Display Name	Preview	Vendor	File Version	Part	I/O Pin C
Arty S7-50		digilentinc.com	1.0	xc7s50csga324-1	324
Arty Z7-20		digilentinc.com	1.0	xc7z020clg400-1	400
Cora Z7-10		digilentinc.com	1.0	xc7z010clg400-1	400
Nexys Video		digilentinc.com	1.1	xc7a200tsbg484-1	484

< Back | Next > | Finish | Cancel

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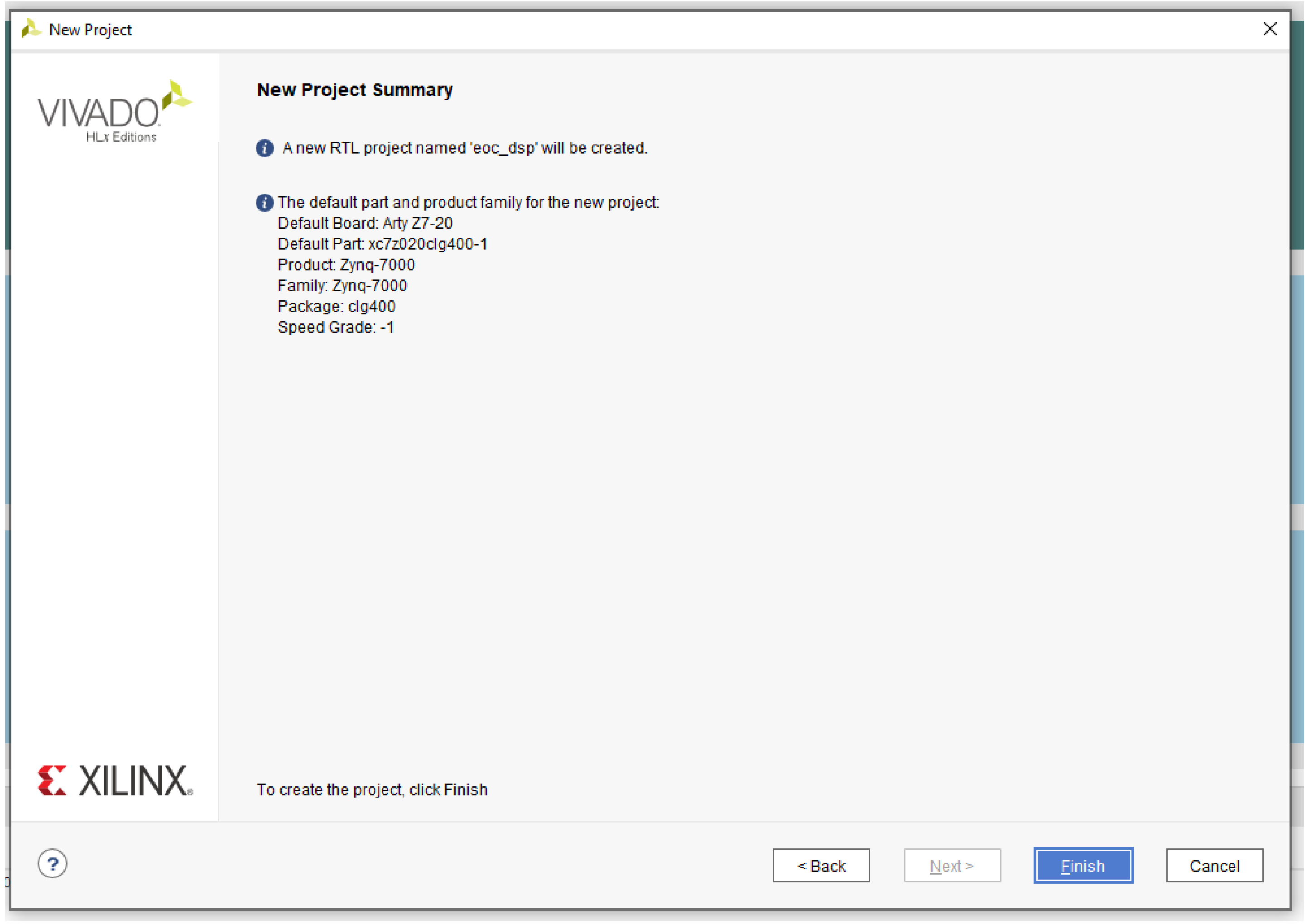
Click Finish to create the project



New Project

New Project Summary

A new RTL project named 'eoc_dsp' will be created.

The default part and product family for the new project:
Default Board: Arty Z7-20
Default Part: xc7z020clg400-1
Product: Zynq-7000
Family: Zynq-7000
Package: clg400
Speed Grade: -1

To create the project, click Finish

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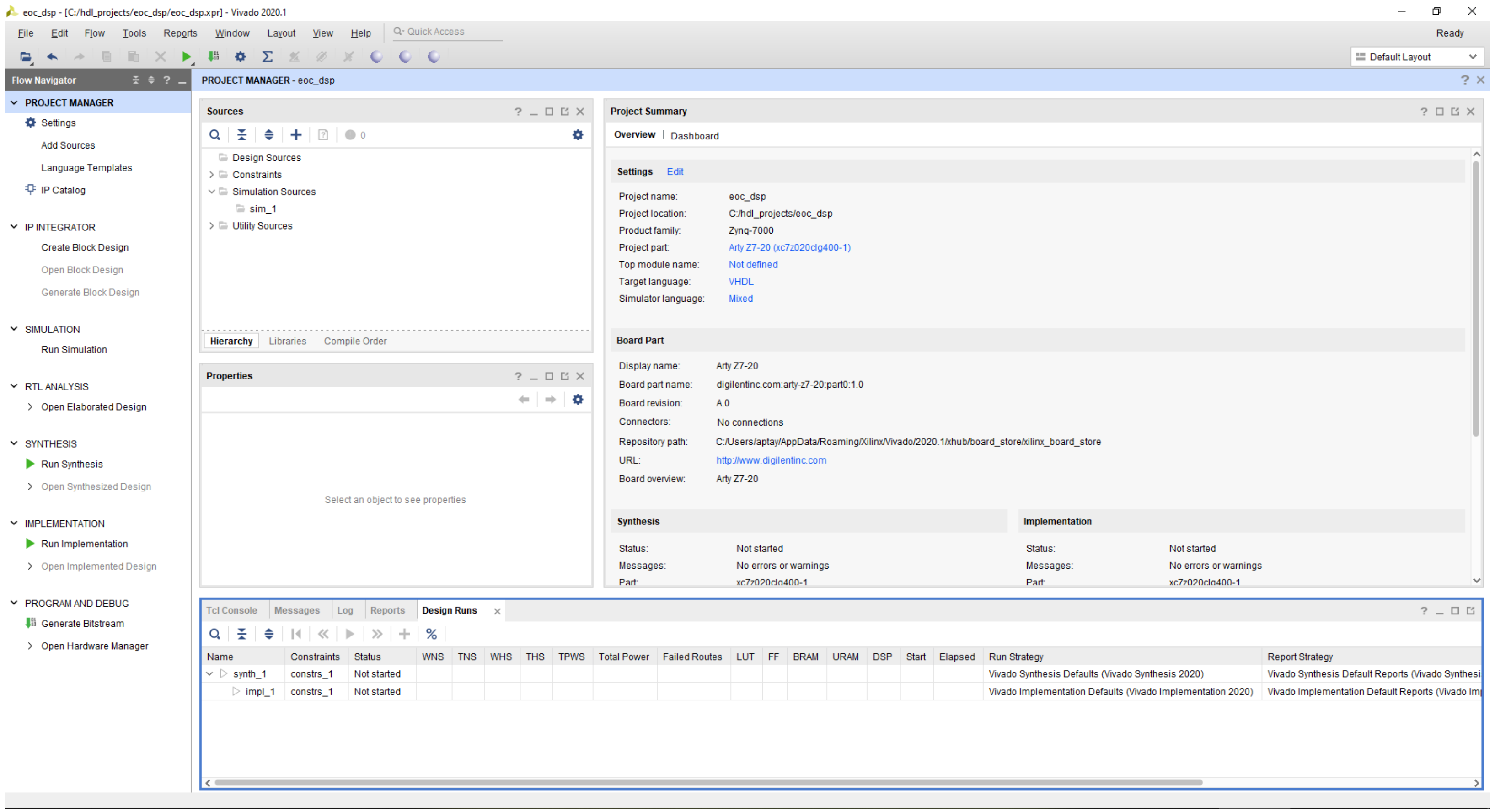
From the Project

Manager, select create

block diagram



Settings Edit

Project name:	eoc_dsp
Project location:	C:/hdl_projects/eoc_dsp
Product family:	Zynq-7000
Project part:	Arty Z7-20 (xc7z020clg400-1)
Top module name:	Not defined
Target language:	VHDL
Simulator language:	Mixed

Board Part

Display name:	Arty Z7-20
Board part name:	digilentinc.com:arty-z7-20:part0:1.0
Board revision:	A.0
Connectors:	No connections
Repository path:	C:/Users/aptay/AppData/Roaming/Xilinx/Vivado/2020.1/xhub/board_store/xilinx_board_store
URL:	http://www.digilentinc.com
Board overview:	Arty Z7-20

Synthesis

Status:	Not started
Messages:	No errors or warnings
Part:	xc7z020clg400-1

Implementation

Status:	Not started
Messages:	No errors or warnings
Part:	xc7z020clg400-1

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Im

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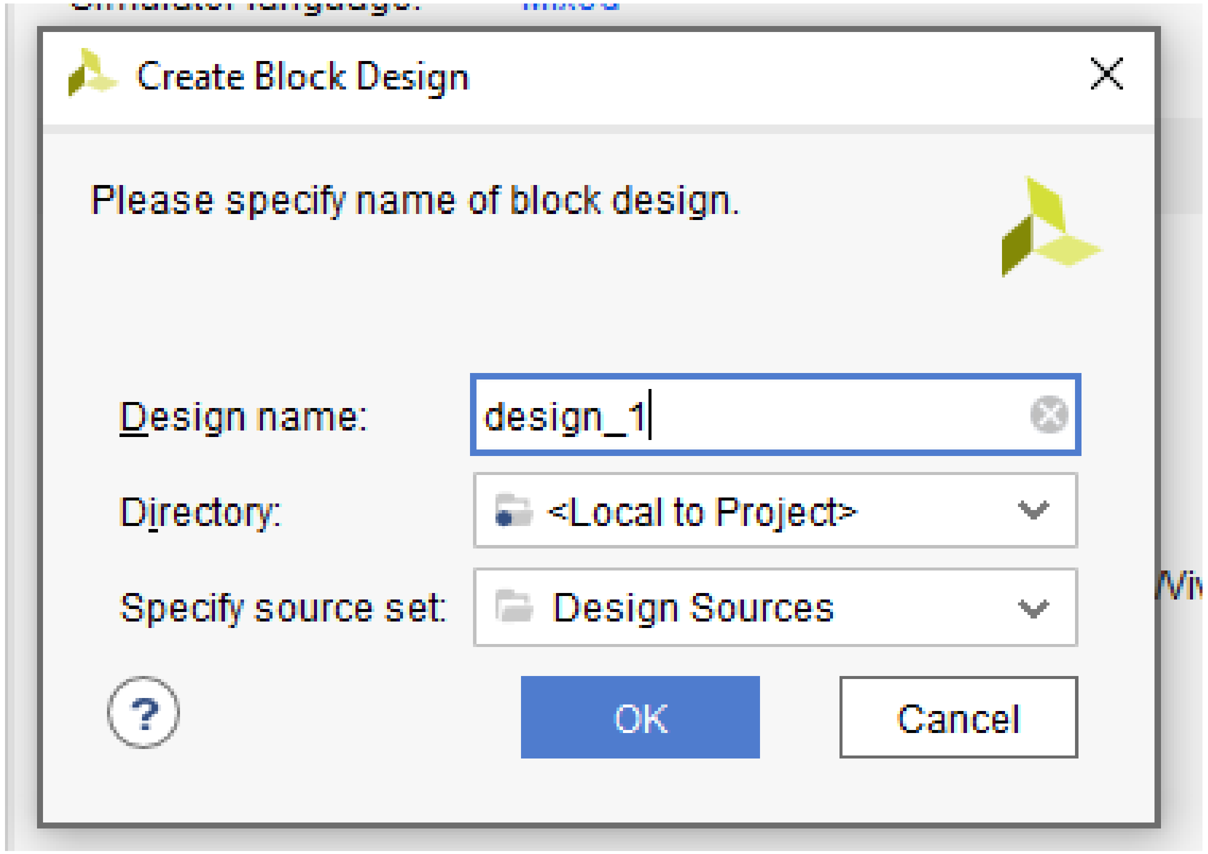
Leave, defaults unchanged and click OK


Create Block Design

Please specify name of block design.

Design name: design_1

Directory: <Local to Project>

Specify source set: Design Sources

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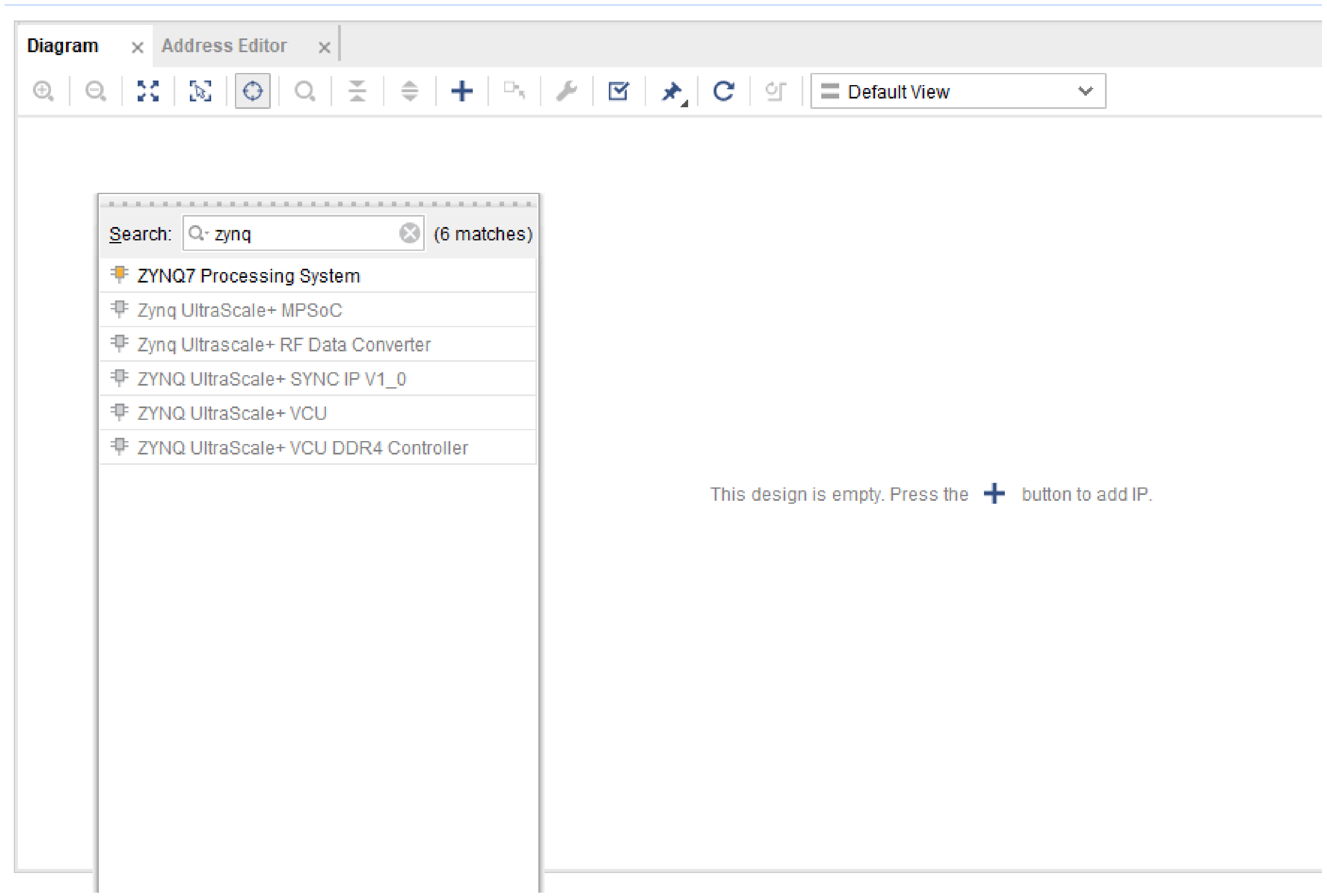
Click on + and in the

search bar type in Zynq

and press enter



Search: zynq (6 matches)

- ZYNQ7 Processing System
- Zynq UltraScale+ MPSoC
- Zynq Ultrascale+ RF Data Converter
- ZYNQ UltraScale+ SYNC IP V1_0
- ZYNQ UltraScale+ VCU
- ZYNQ UltraScale+ VCU DDR4 Controller

This design is empty. Press the + button to add IP.

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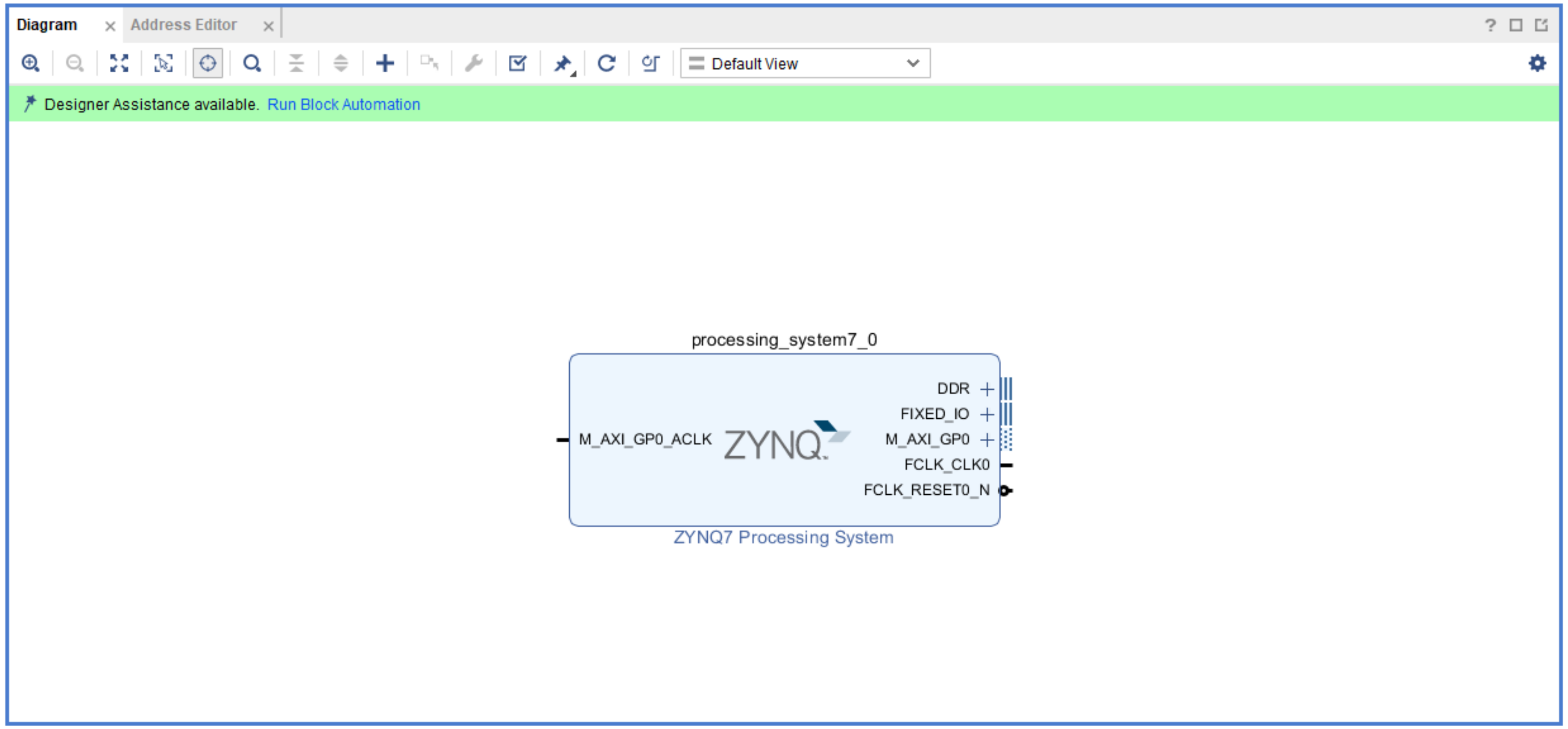
Run the block automation

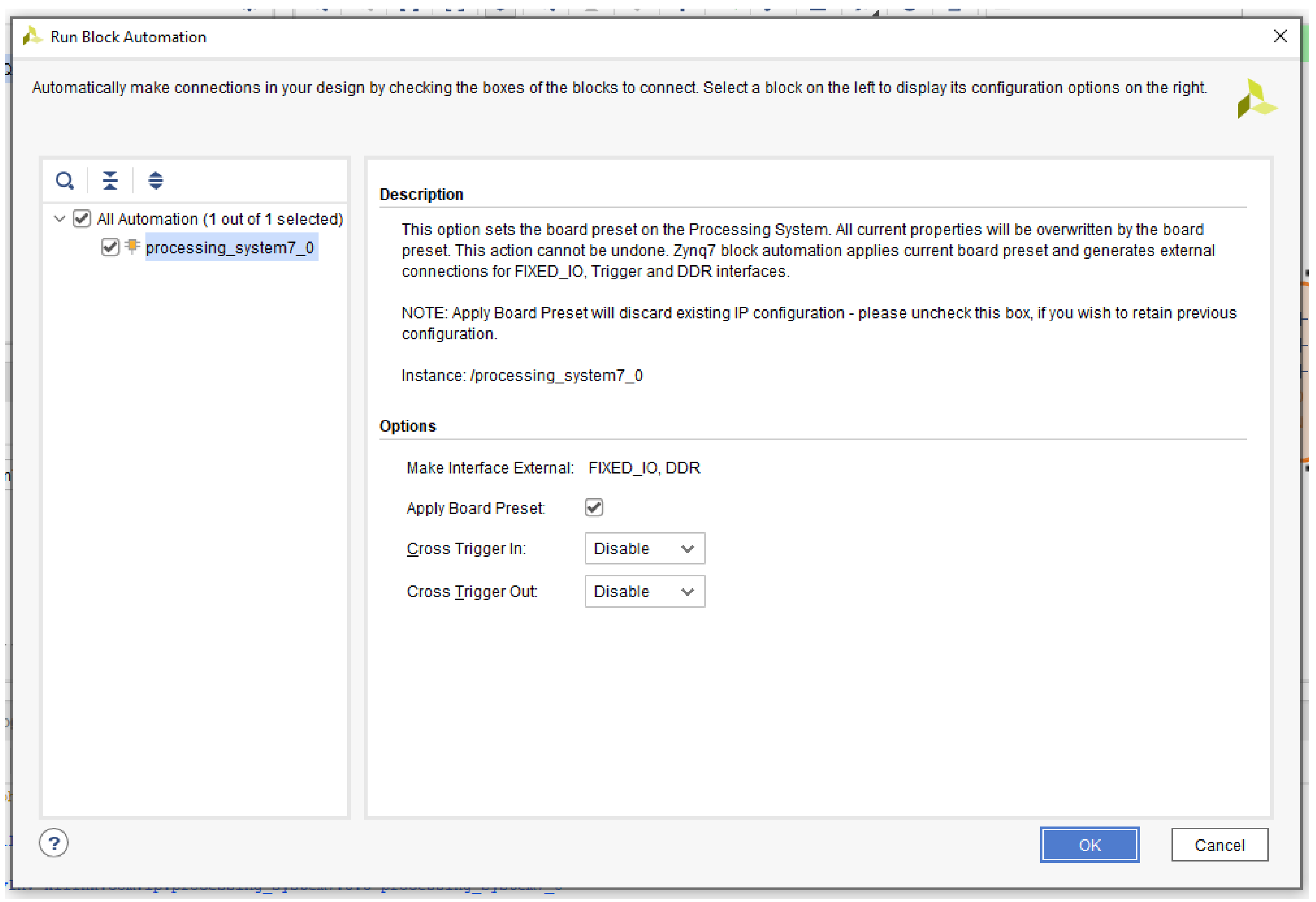


Designer Assistance available. Run Block Automation

Lab : FFT Acceleration

Leave the settings as default and

click OK



Automatically make connections in your design by checking the boxes of the blocks to connect. Select a block on the left to display its configuration options on the right.

- [✓] All Automation (1 out of 1 selected)
  - [✓] processing_system7_0

Description

This option sets the board preset on the Processing System. All current properties will be overwritten by the board preset. This action cannot be undone. Zynq7 block automation applies current board preset and generates external connections for FIXED_IO, Trigger and DDR interfaces.

NOTE: Apply Board Preset will discard existing IP configuration - please uncheck this box, if you wish to retain previous configuration.

Instance: /processing_system7_0

Options

Make Interface External: FIXED_IO, DDR

Apply Board Preset: ✓

Cross Trigger In: Disable

Cross Trigger Out: Disable

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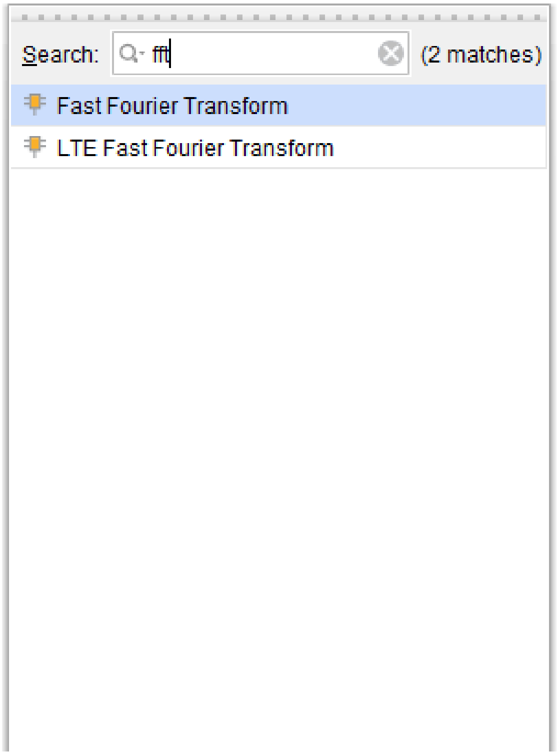
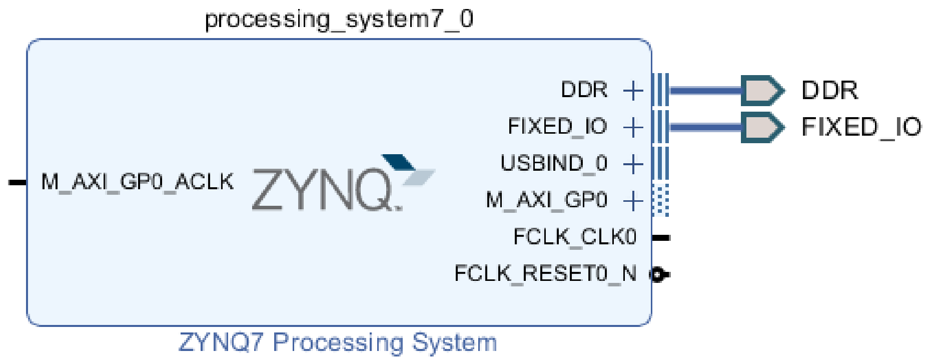
Click on + and add in the

FFT


Search: fft (2 matches)

Fast Fourier Transform

LTE Fast Fourier Transform



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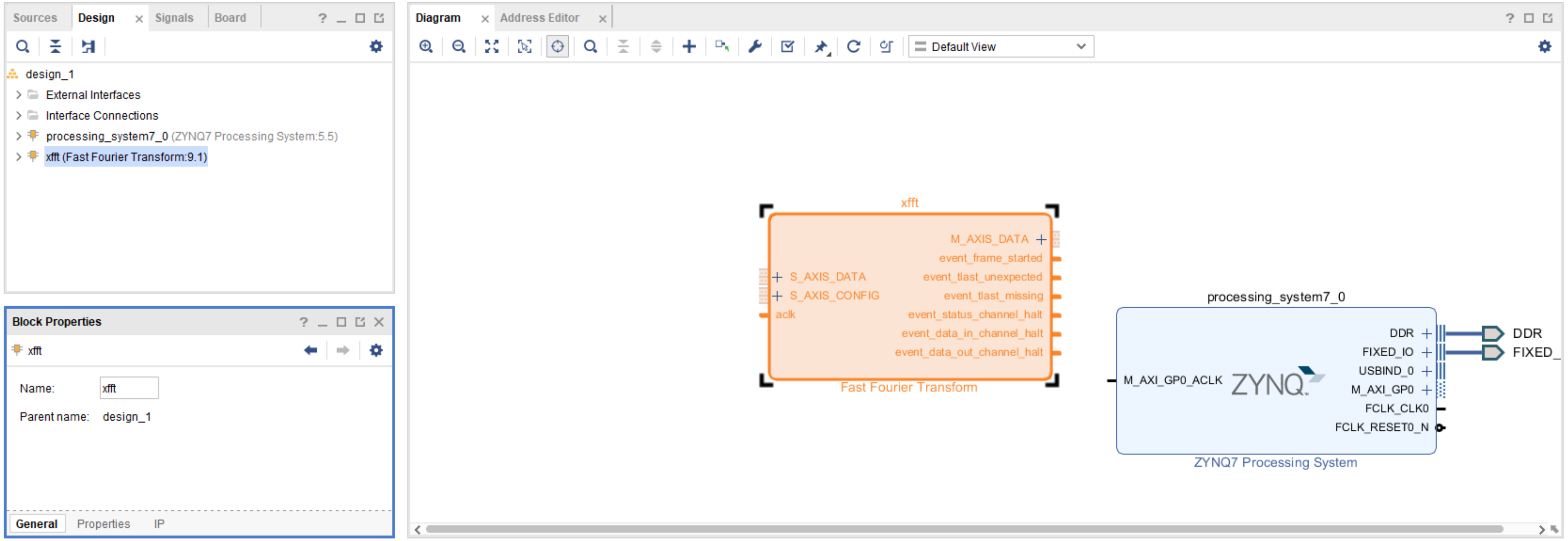
Click on the Fast Fourier Transform and change its name to xfft. Double click on the block to customize it.



design_1
- External Interfaces
- Interface Connections
- processing_system7_0 (ZYNQ7 Processing System:5.5)
- xfft (Fast Fourier Transform:9.1)

Block Properties

xfft

Name: xfft

Parent name: design_1

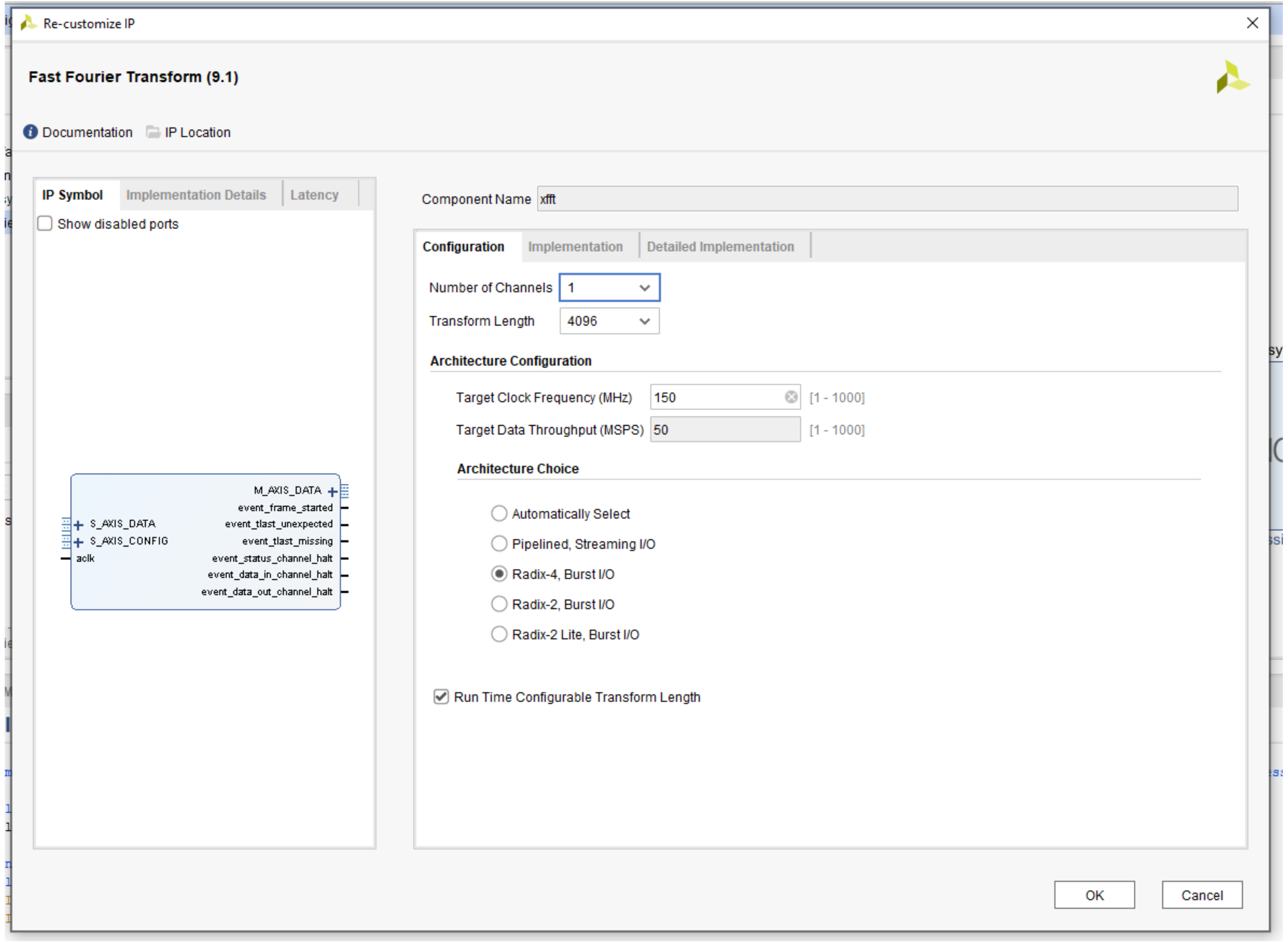
General | Properties | IP

Lab : FFT Acceleration

On the configuration tab, select

- Transform length 4096
- Radix-4 Burst I/O
- Target Frequency 150Mhz
- Enable Run Time

  Configurable transform length



Re-customize IP

Fast Fourier Transform (9.1)

Documentation IP Location

IP Symbol | Implementation Details | Latency

☐ Show disabled ports

Component Name: xfft

Configuration | Implementation | Detailed Implementation

Number of Channels: 1

Transform Length: 4096

Architecture Configuration

Target Clock Frequency (MHz): 150 [1 - 1000]

Target Data Throughput (MSPS): 50 [1 - 1000]

Architecture Choice

- ○ Automatically Select
- ○ Pipelined, Streaming I/O
- ● Radix-4, Burst I/O
- ○ Radix-2, Burst I/O
- ○ Radix-2 Lite, Burst I/O

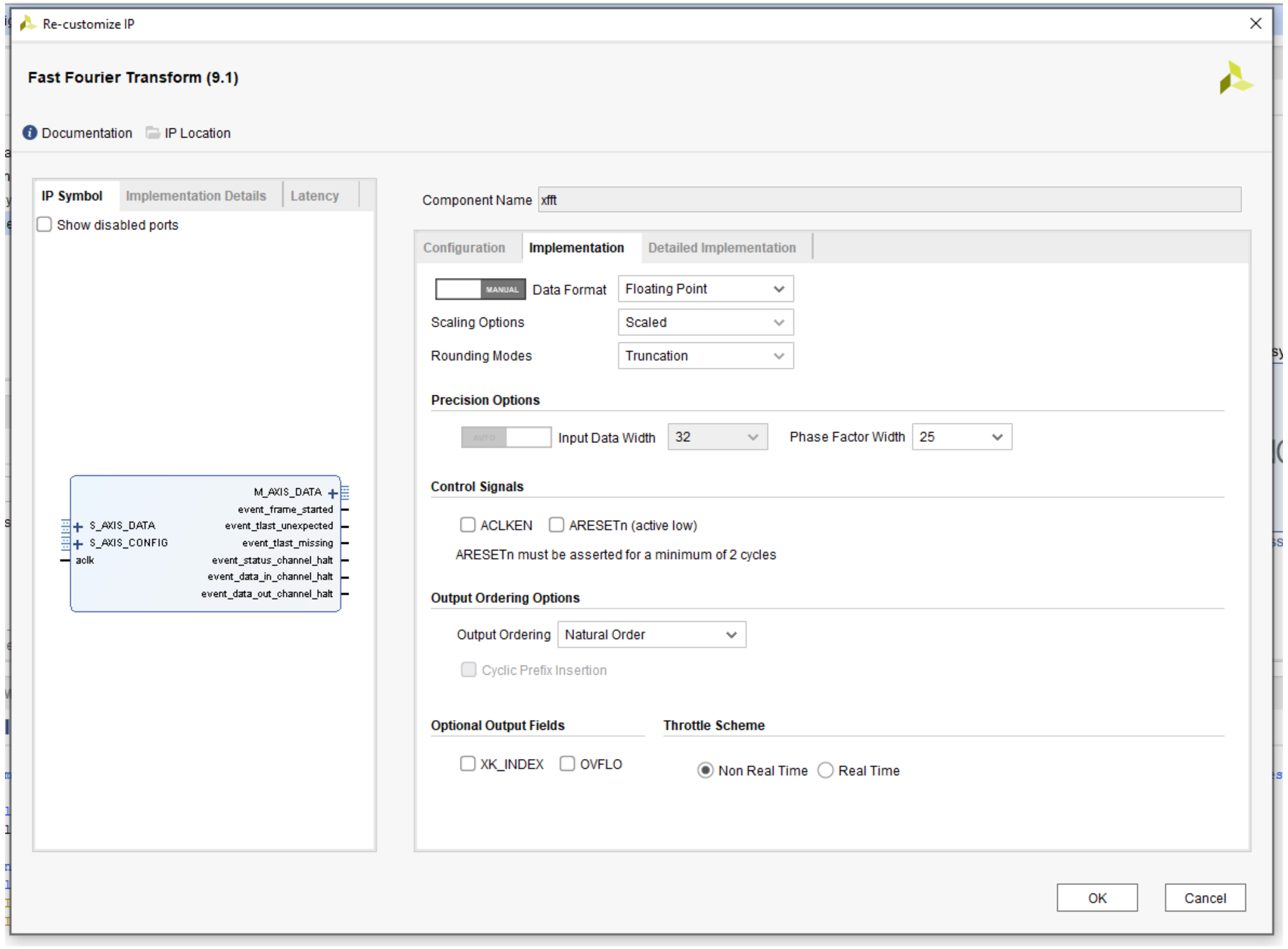
☑ Run Time Configurable Transform Length

OK Cancel

Lab : FFT Acceleration

On the implementation tab select

- Floating Point
- Phase Factor Width 25
- Output Ordering Natural
- Non-Real Time Throttle scheme


Re-customize IP

Fast Fourier Transform (9.1)

Documentation IP Location

IP Symbol | Implementation Details | Latency

Show disabled ports

Component Name: xfft

Configuration | Implementation | Detailed Implementation

Data Format: Floating Point
Scaling Options: Scaled
Rounding Modes: Truncation

Precision Options
Input Data Width: 32 Phase Factor Width: 25

Control Signals
ACLKEN ARESETn (active low)
ARESETn must be asserted for a minimum of 2 cycles

Output Ordering Options
Output Ordering: Natural Order
Cyclic Prefix Insertion

Optional Output Fields
XK_INDEX OVFLO

Throttle Scheme
[✓ Non Real Time] Real Time

OK Cancel

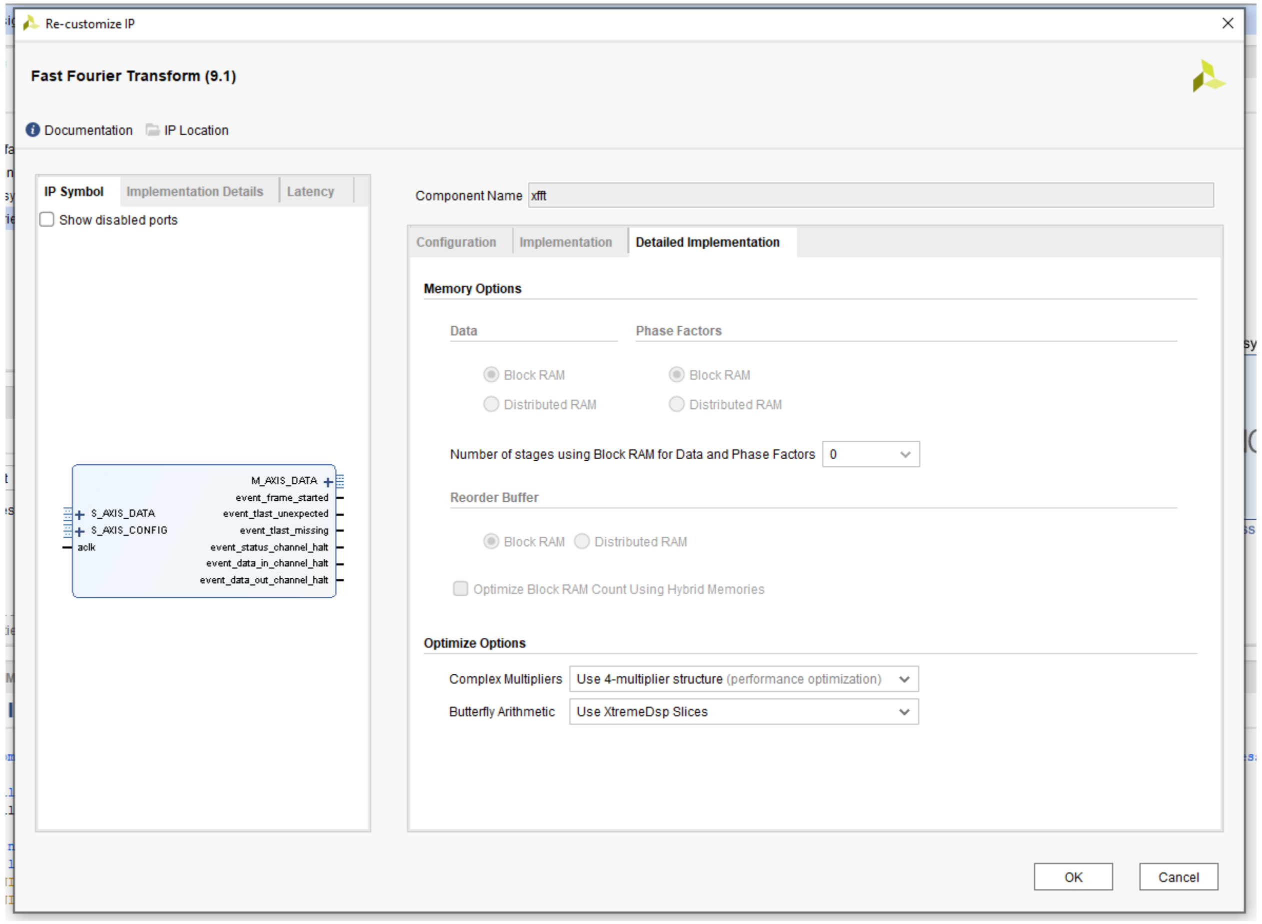
Lab : FFT Acceleration

On the Detailed Implementation tab

select

- Use 4-Multipler Structure

- Use XtremeDSP Slices



Component Name xfft

Memory Options

Data: [✓ Block RAM] Distributed RAM

Phase Factors: [✓ Block RAM] Distributed RAM

Number of stages using Block RAM for Data and Phase Factors: 0

Reorder Buffer: [✓ Block RAM] Distributed RAM

☐ Optimize Block RAM Count Using Hybrid Memories

Optimize Options

Complex Multipliers: Use 4-multiplier structure (performance optimization)

Butterfly Arithmetic: Use XtremeDsp Slices

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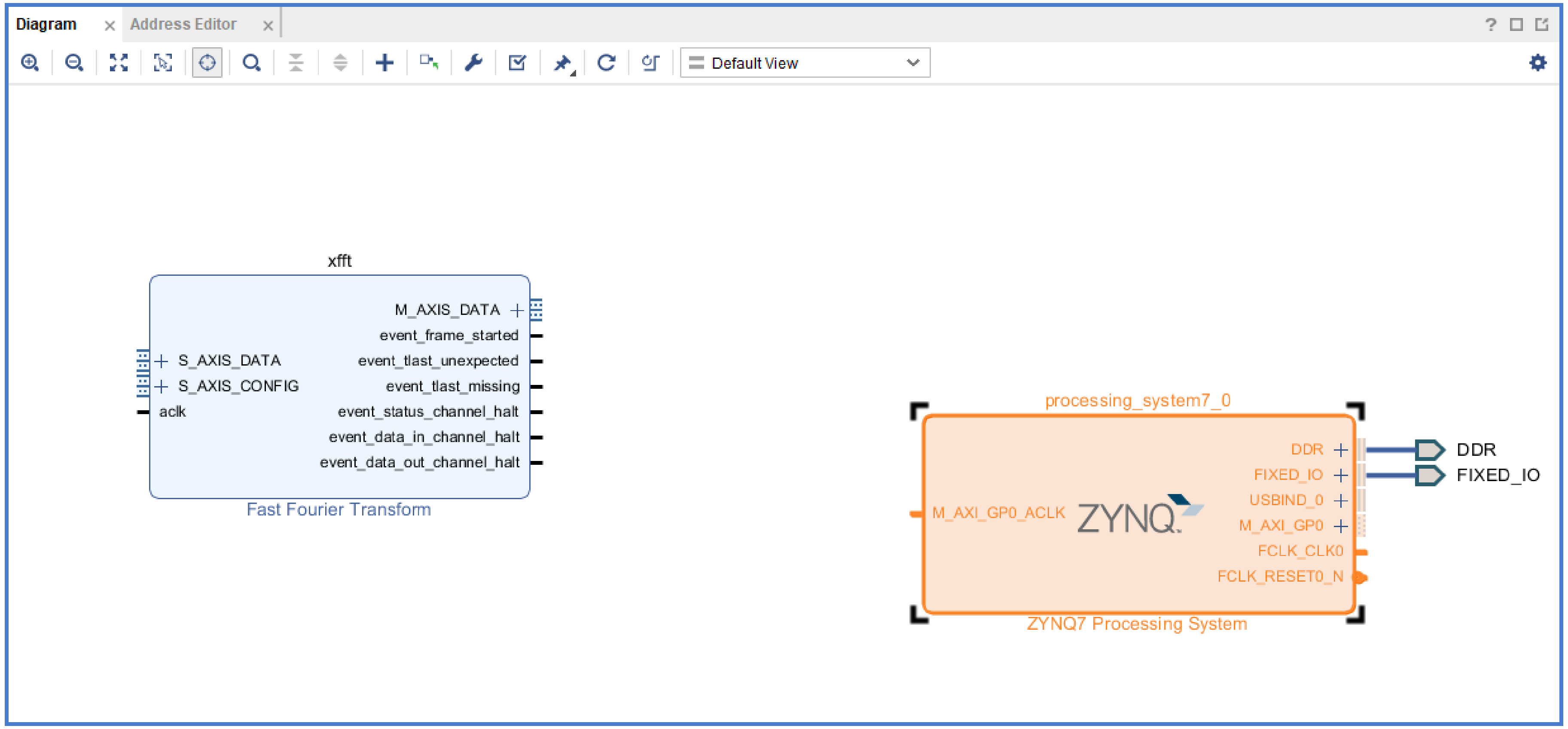
Double click on the Processing System to reconfigure it



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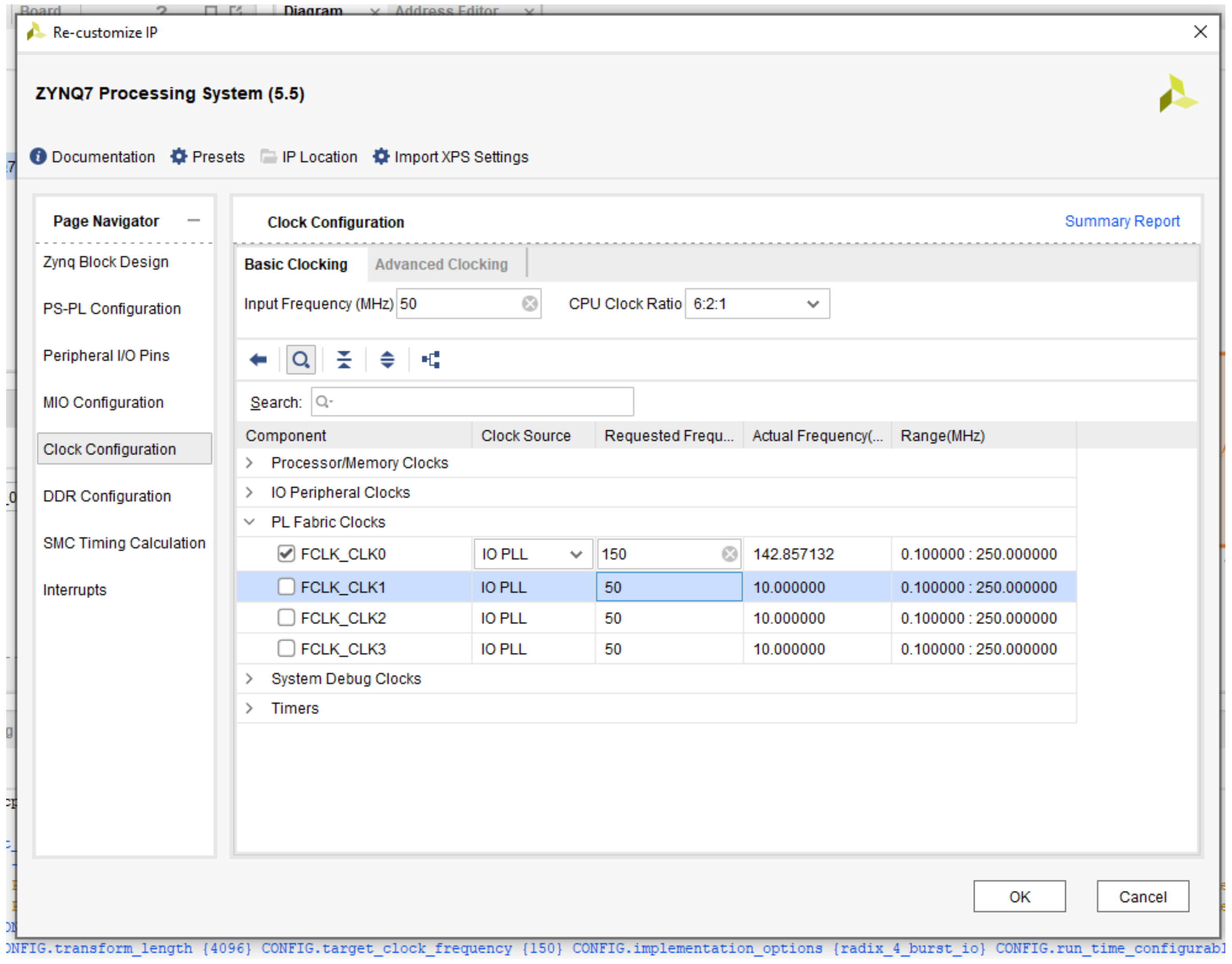
On the clocking tab change the

frequency of clock one to 150MHz



Re-customize IP

ZYNQ7 Processing System (5.5)

Documentation · Presets · IP Location · Import XPS Settings

Page Navigator:
- Zynq Block Design
- PS-PL Configuration
- Peripheral I/O Pins
- MIO Configuration
- Clock Configuration
- DDR Configuration
- SMC Timing Calculation
- Interrupts

Clock Configuration — Summary Report

Basic Clocking | Advanced Clocking

Input Frequency (MHz) 50 CPU Clock Ratio 6:2:1

Search:

Component	Clock Source	Requested Frequ...	Actual Frequency(...	Range(MHz)
Processor/Memory Clocks				
IO Peripheral Clocks				
PL Fabric Clocks				
✓ FCLK_CLK0	IO PLL	150	142.857132	0.100000 : 250.000000
FCLK_CLK1	IO PLL	50	10.000000	0.100000 : 250.000000
FCLK_CLK2	IO PLL	50	10.000000	0.100000 : 250.000000
FCLK_CLK3	IO PLL	50	10.000000	0.100000 : 250.000000
System Debug Clocks				
Timers				

OK Cancel

```
ONFIG.transform_length {4096} CONFIG.target_clock_frequency {150} CONFIG.implementation_options {radix_4_burst_io} CONFIG.run_time_configurabl
```

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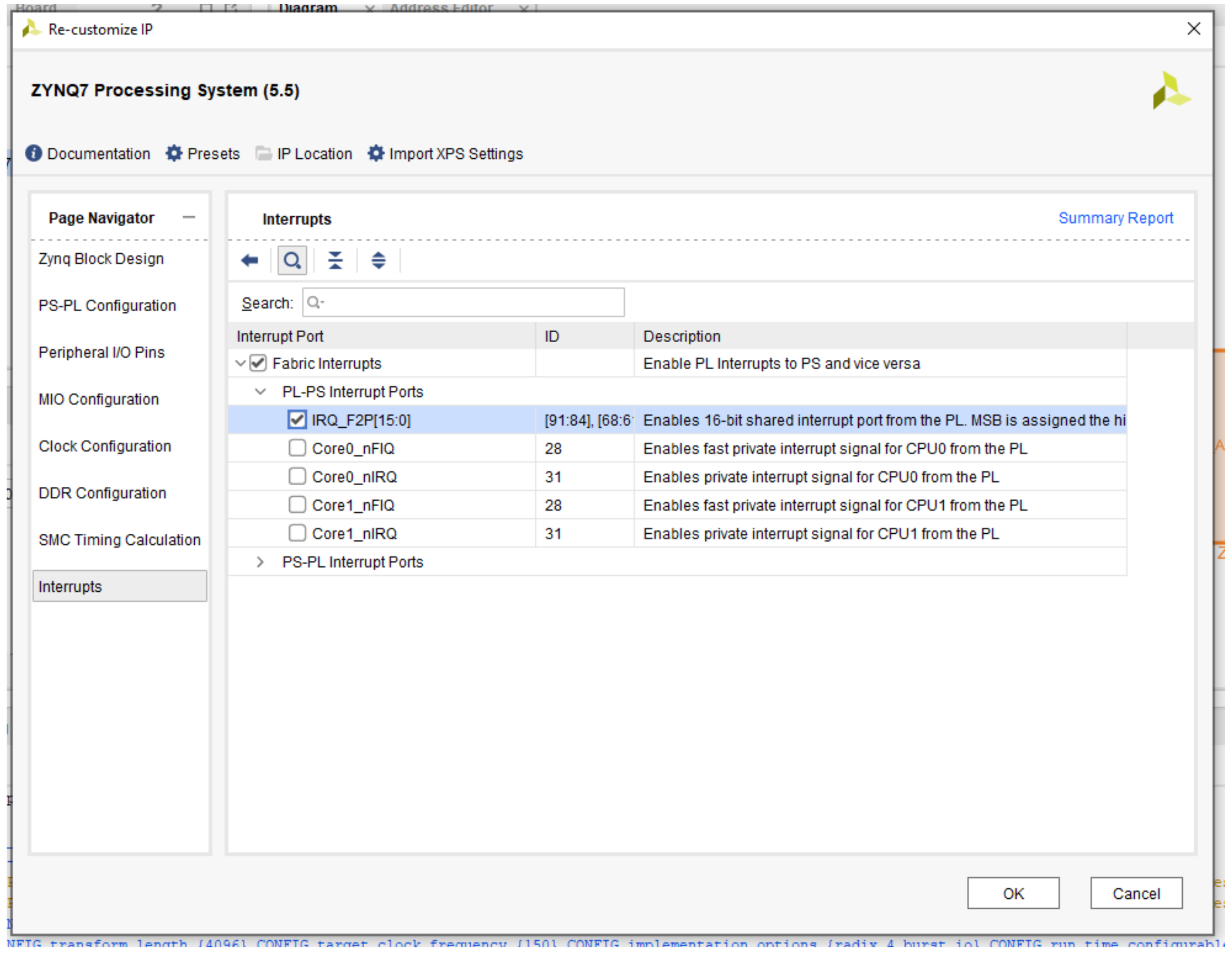
On the Interrupts Tab enable the

IRQ_F2P[15:0]



Re-customize IP

ZYNQ7 Processing System (5.5)

Documentation Presets IP Location Import XPS Settings

Page Navigator

- Zynq Block Design
- PS-PL Configuration
- Peripheral I/O Pins
- MIO Configuration
- Clock Configuration
- DDR Configuration
- SMC Timing Calculation
- Interrupts

Interrupts Summary Report

Search:

Interrupt Port	ID	Description
☑ Fabric Interrupts		Enable PL Interrupts to PS and vice versa
PL-PS Interrupt Ports		
☑ IRQ_F2P[15:0]	[91:84], [68:6	Enables 16-bit shared interrupt port from the PL. MSB is assigned the hi
☐ Core0_nFIQ	28	Enables fast private interrupt signal for CPU0 from the PL
☐ Core0_nIRQ	31	Enables private interrupt signal for CPU0 from the PL
☐ Core1_nFIQ	28	Enables fast private interrupt signal for CPU1 from the PL
☐ Core1_nIRQ	31	Enables private interrupt signal for CPU1 from the PL
PS-PL Interrupt Ports		

OK Cancel

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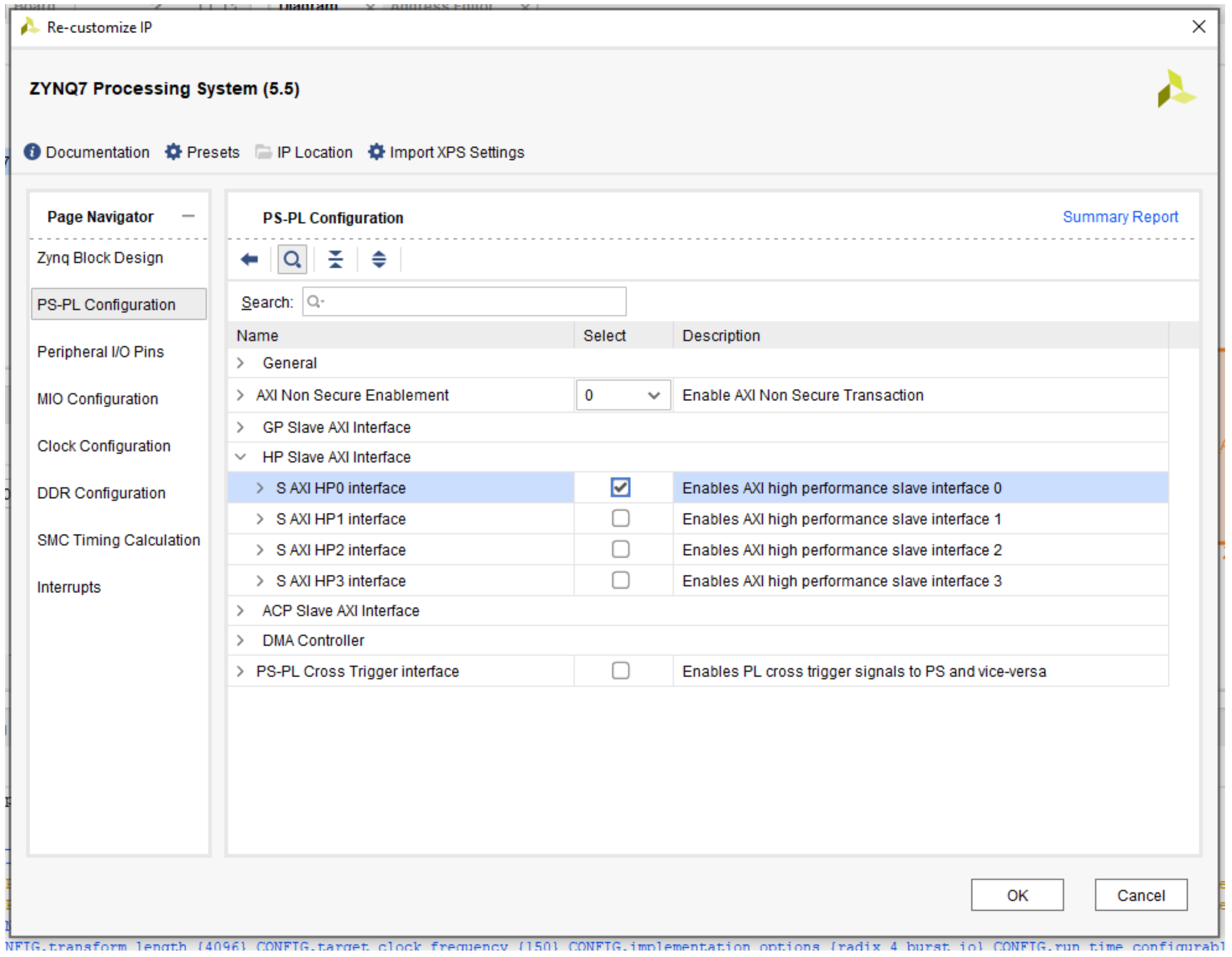
On the PS/PL interface select the HP

Slave AXI Interface

Enable S AXI HP0 Interface



Re-customize IP

ZYNQ7 Processing System (5.5)

Documentation · Presets · IP Location · Import XPS Settings

Page Navigator

- Zynq Block Design
- PS-PL Configuration
- Peripheral I/O Pins
- MIO Configuration
- Clock Configuration
- DDR Configuration
- SMC Timing Calculation
- Interrupts

PS-PL Configuration — Summary Report

Search:

Name	Select	Description
> General		
> AXI Non Secure Enablement	0	Enable AXI Non Secure Transaction
> GP Slave AXI Interface		
˅ HP Slave AXI Interface		
> S AXI HP0 interface	✓	Enables AXI high performance slave interface 0
> S AXI HP1 interface	☐	Enables AXI high performance slave interface 1
> S AXI HP2 interface	☐	Enables AXI high performance slave interface 2
> S AXI HP3 interface	☐	Enables AXI high performance slave interface 3
> ACP Slave AXI Interface		
> DMA Controller		
> PS-PL Cross Trigger interface	☐	Enables PL cross trigger signals to PS and vice-versa

OK · Cancel

```
NFIG.transform_length {4096} CONFIG.target_clock_frequency {150} CONFIG.implementation_options {radix_4_burst_io} CONFIG.run_time_configurabl
```

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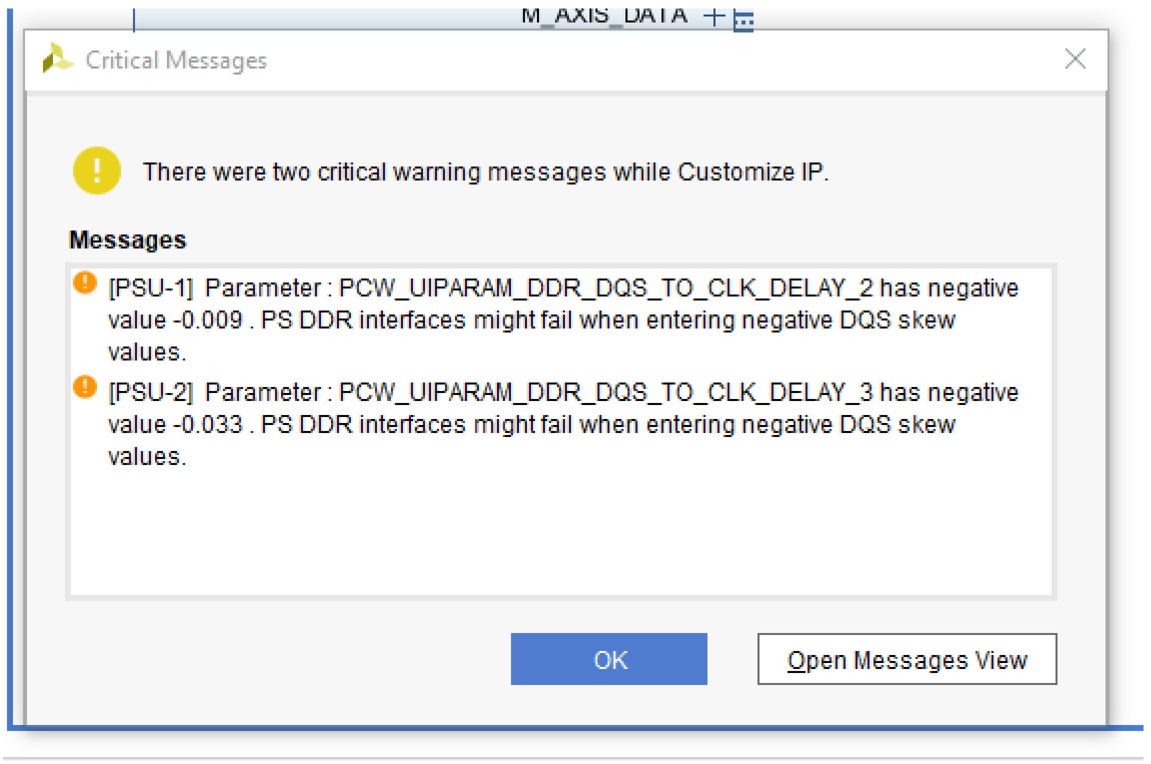
Click OK if the warning appears



There were two critical warning messages while Customize IP.

Messages

[PSU-1] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_2 has negative value -0.009 . PS DDR interfaces might fail when entering negative DQS skew values.

[PSU-2] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_3 has negative value -0.033 . PS DDR interfaces might fail when entering negative DQS skew values.

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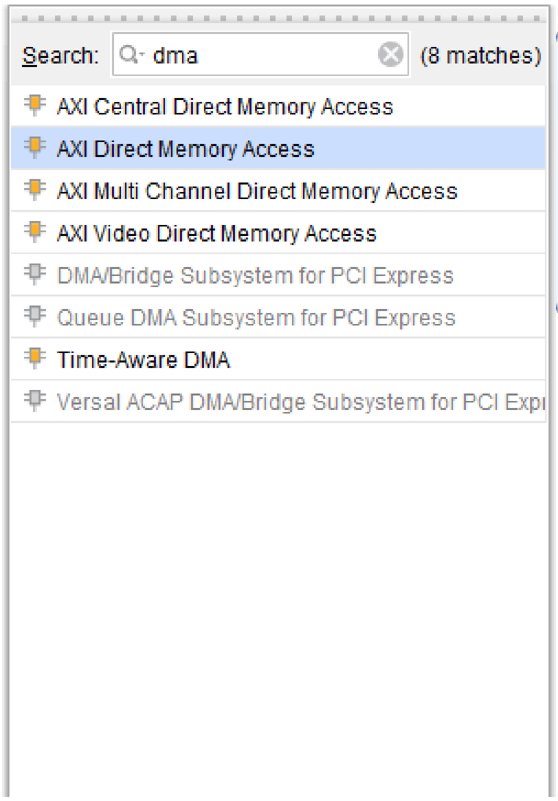
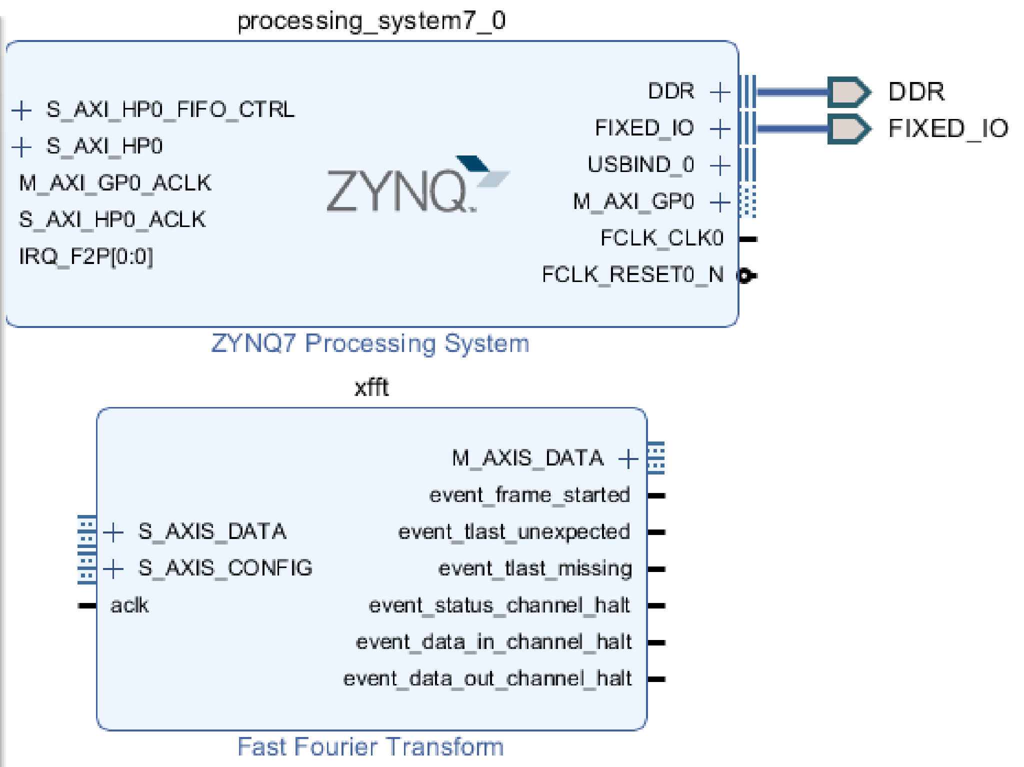
Click + and select AXI

Direct Memory Access



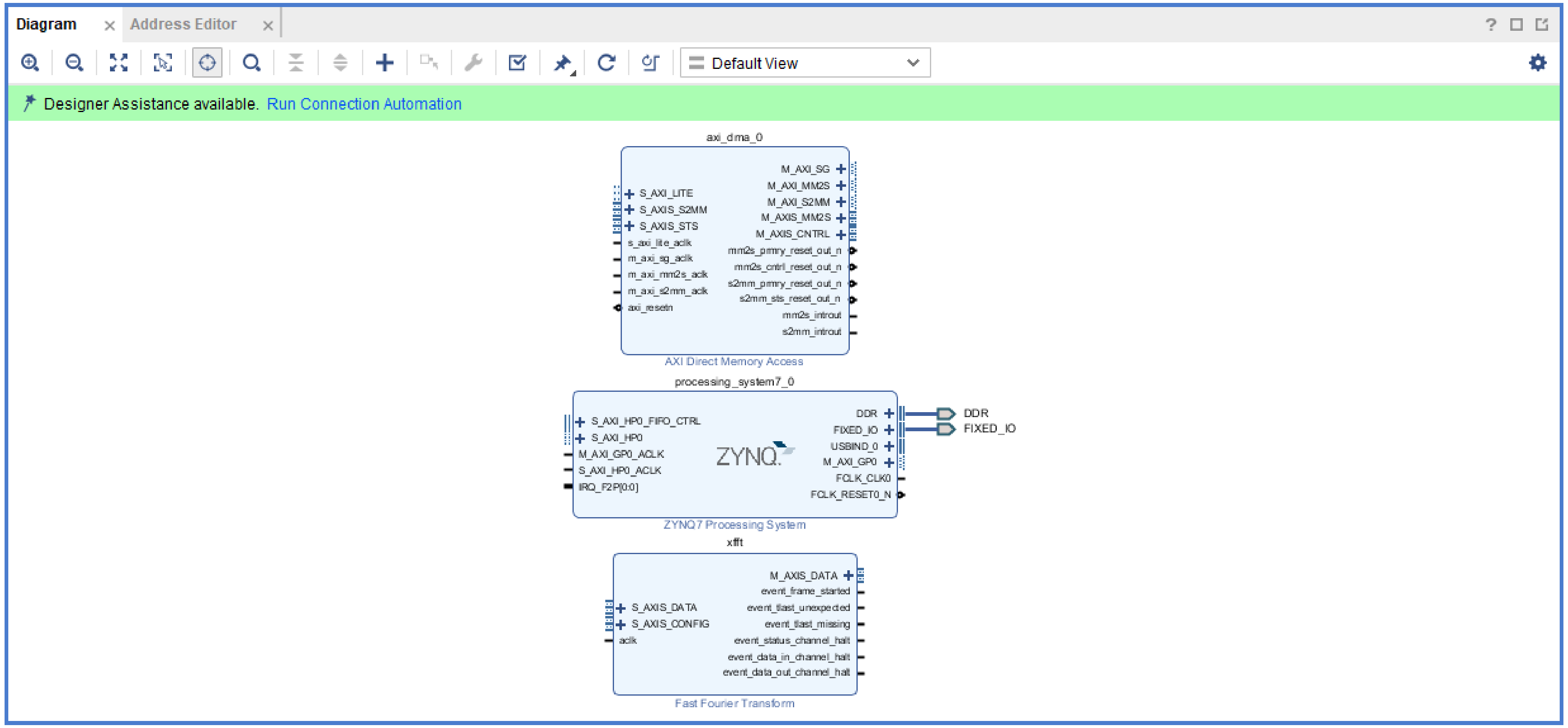
Search: dma (8 matches)

- AXI Central Direct Memory Access
- AXI Direct Memory Access
- AXI Multi Channel Direct Memory Access
- AXI Video Direct Memory Access
- DMA/Bridge Subsystem for PCI Express
- Queue DMA Subsystem for PCI Express
- Time-Aware DMA
- Versal ACAP DMA/Bridge Subsystem for PCI Expr



Lab : FFT Acceleration

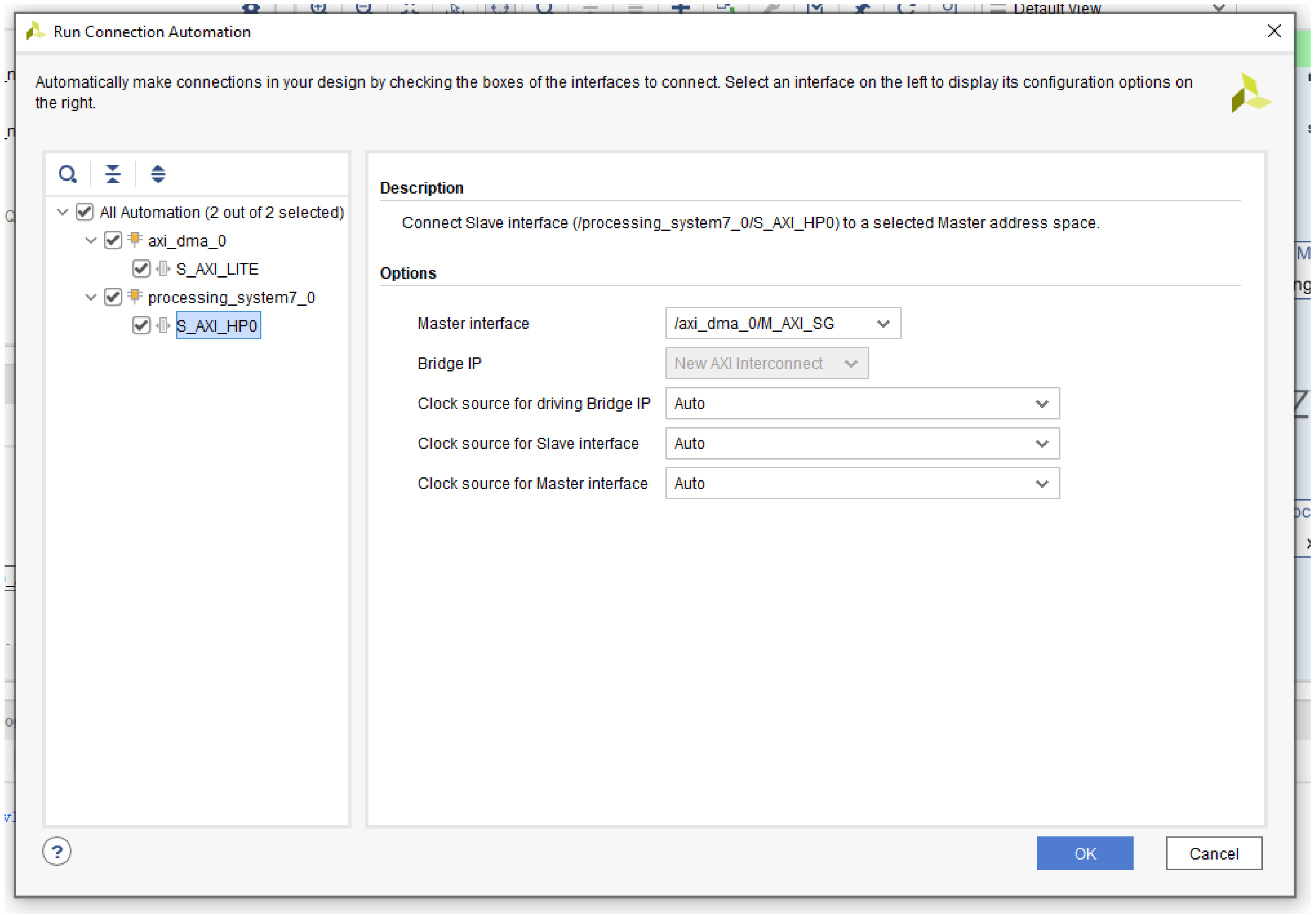
Run the Connection Automation



Lab : FFT Acceleration

Leave the defaults as

standard and click OK


Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

- All Automation (2 out of 2 selected)
  - axi_dma_0
    - S_AXI_LITE
  - processing_system7_0
    - S_AXI_HP0

Description

Connect Slave interface (/processing_system7_0/S_AXI_HP0) to a selected Master address space.

Options

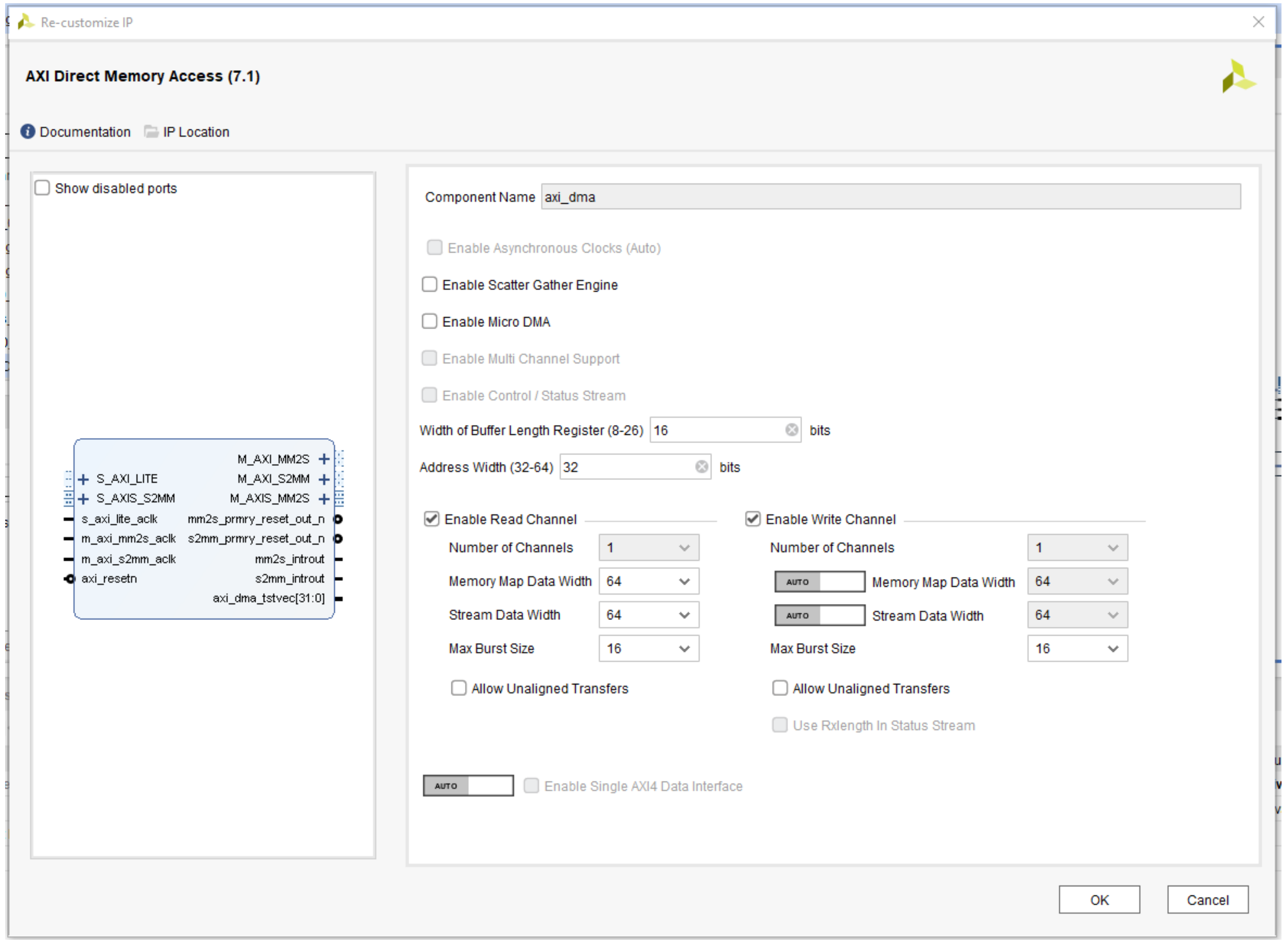
Master interface	/axi_dma_0/M_AXI_SG
Bridge IP	New AXI Interconnect
Clock source for driving Bridge IP	Auto
Clock source for Slave interface	Auto
Clock source for Master interface	Auto

Lab : FFT Acceleration

Select the DMA, double click on it

and configure it

- Width of Buffer length 16
- Stream data width 64
- Max burst size 16



Re-customize IP

AXI Direct Memory Access (7.1)

Documentation   IP Location

☐ Show disabled ports

Component Name axi_dma

☐ Enable Asynchronous Clocks (Auto)
☐ Enable Scatter Gather Engine
☐ Enable Micro DMA
☐ Enable Multi Channel Support
☐ Enable Control / Status Stream

Width of Buffer Length Register (8-26) 16 bits

Address Width (32-64) 32 bits

☑ Enable Read Channel		☑ Enable Write Channel	
Number of Channels	1	Number of Channels	1
Memory Map Data Width	64	AUTO Memory Map Data Width	64
Stream Data Width	64	AUTO Stream Data Width	64
Max Burst Size	16	Max Burst Size	16
☐ Allow Unaligned Transfers		☐ Allow Unaligned Transfers	
		☐ Use Rxlength In Status Stream	

AUTO ☐ Enable Single AXI4 Data Interface

OK   Cancel

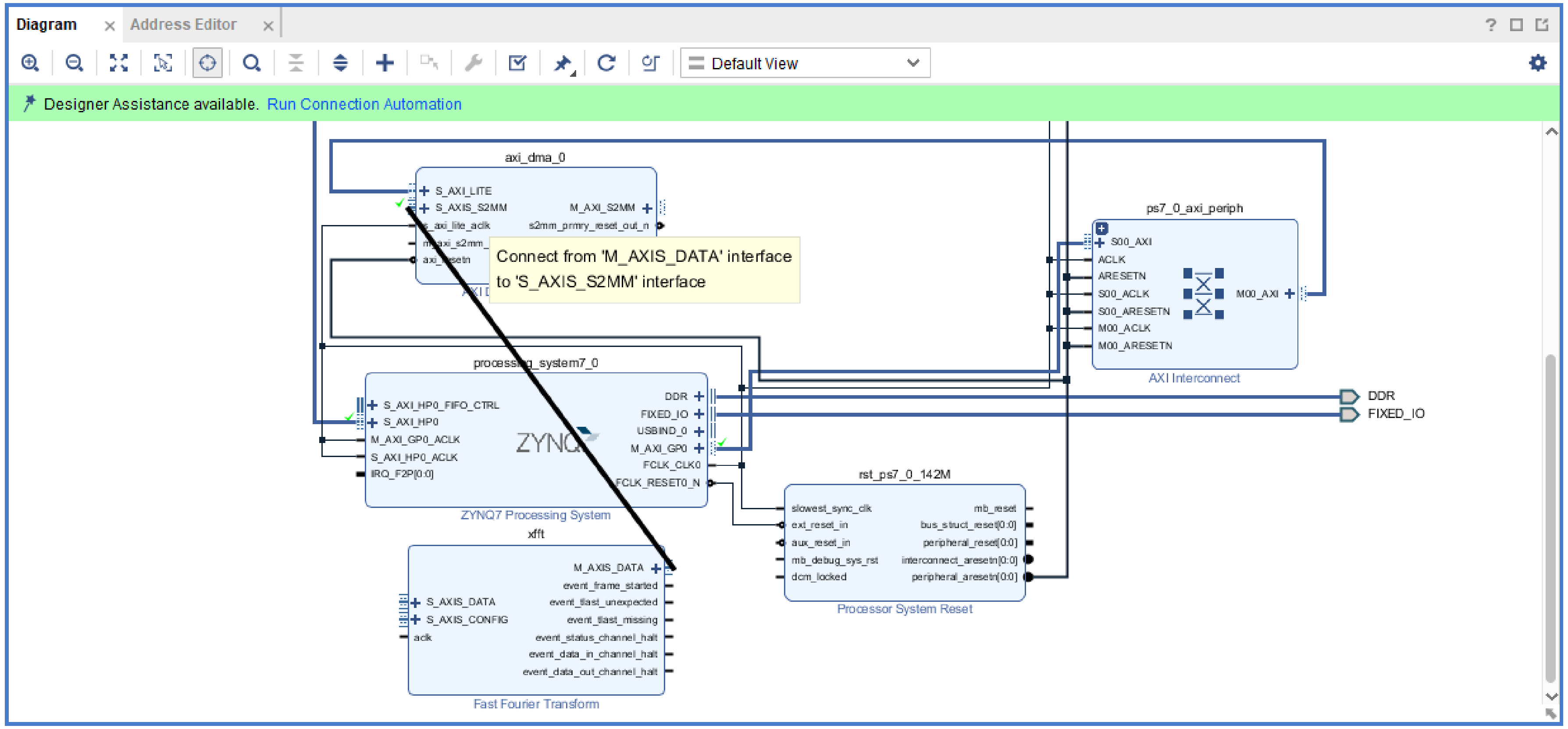
Lab : FFT Acceleration

Connect the xFFT M

AXIS data to the

DMA, S AXIS S2MM

port


Designer Assistance available. Run Connection Automation

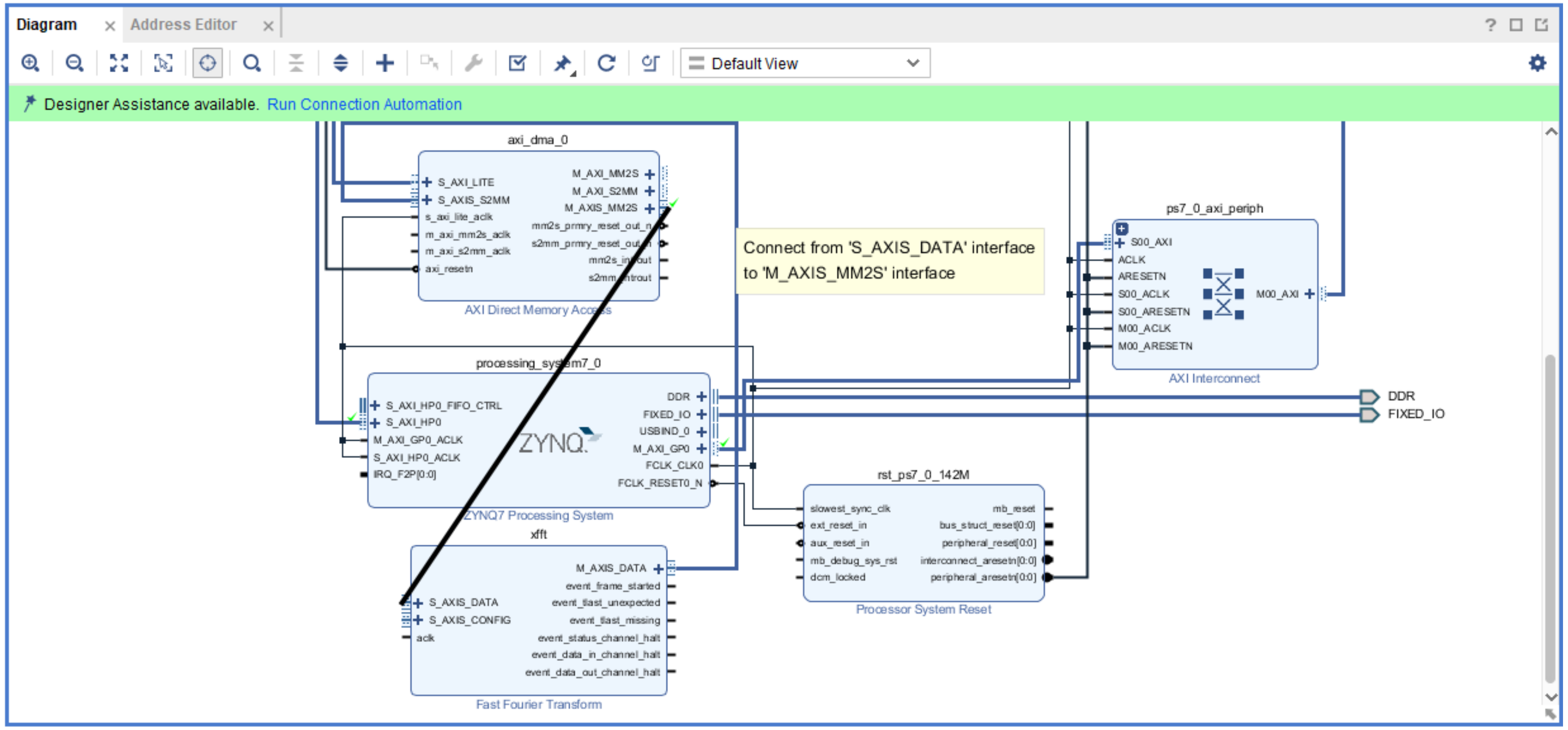
Connect from 'M_AXIS_DATA' interface to 'S_AXIS_S2MM' interface

Lab : FFT Acceleration

Connect the DMA M

AXIS MM2S to the xFFT

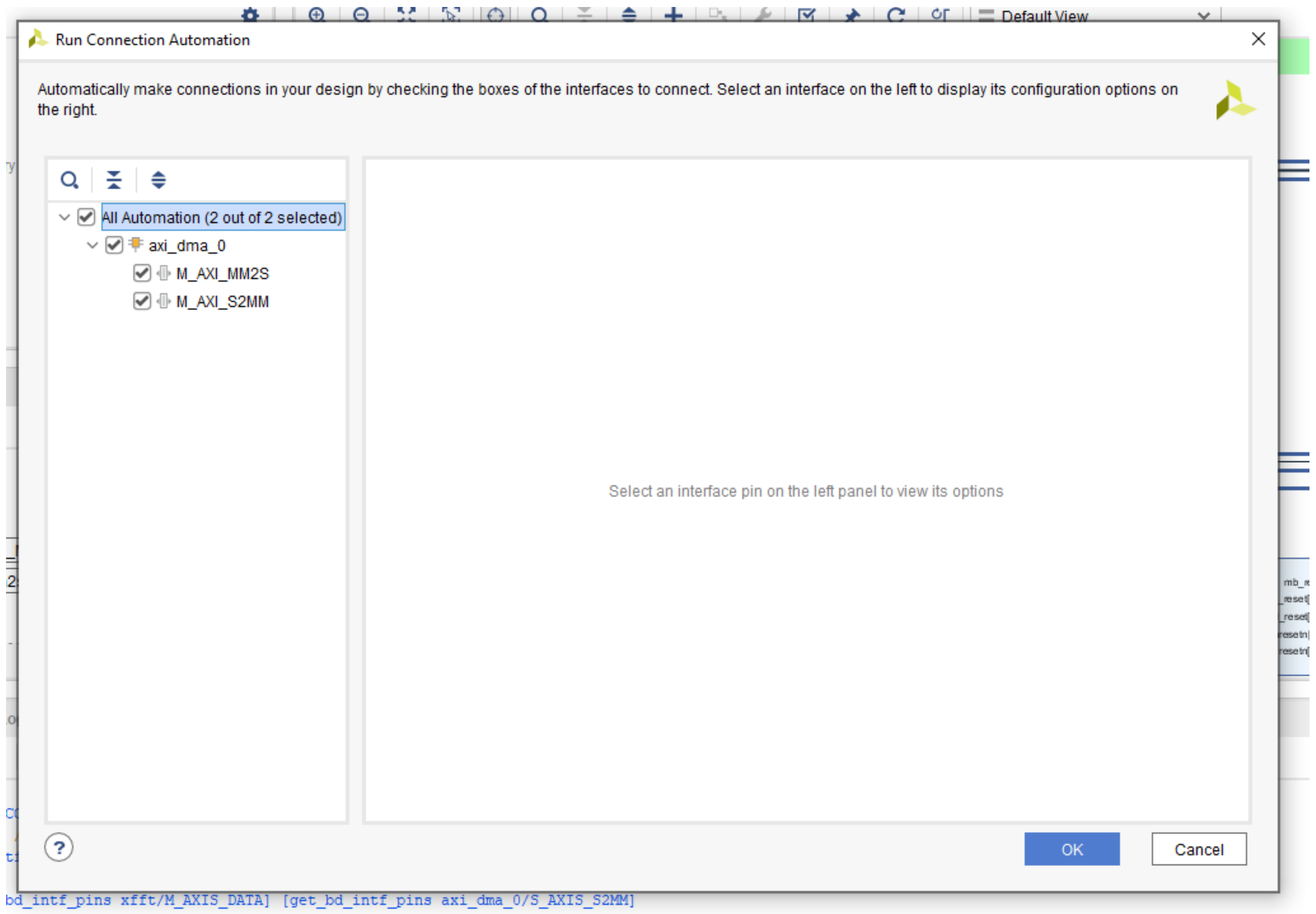
S AXIS Data



Connect from 'S_AXIS_DATA' interface to 'M_AXIS_MM2S' interface

Lab : FFT Acceleration

Run the connection automation


Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

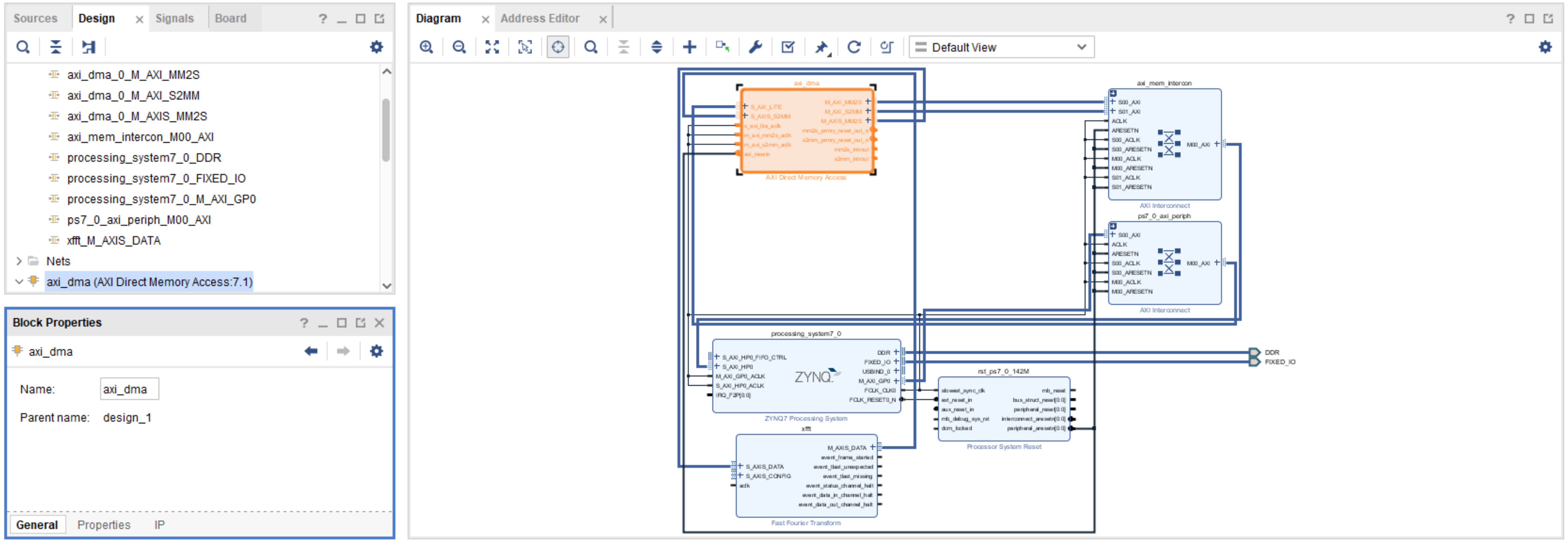
- ☑ All Automation (2 out of 2 selected)
  - ☑ axi_dma_0
    - ☑ M_AXI_MM2S
    - ☑ M_AXI_S2MM

Select an interface pin on the left panel to view its options

```
bd_intf_pins xfft/M_AXIS_DATA] [get_bd_intf_pins axi_dma_0/S_AXIS_S2MM]
```

Lab : FFT Acceleration

The diagram should look like below



- axi_dma_0_M_AXI_MM2S
- axi_dma_0_M_AXI_S2MM
- axi_dma_0_M_AXIS_MM2S
- axi_mem_intercon_M00_AXI
- processing_system7_0_DDR
- processing_system7_0_FIXED_IO
- processing_system7_0_M_AXI_GP0
- ps7_0_axi_periph_M00_AXI
- xfft_M_AXIS_DATA
- Nets
- axi_dma (AXI Direct Memory Access:7.1)

Block Properties

axi_dma

Name: axi_dma

Parent name: design_1

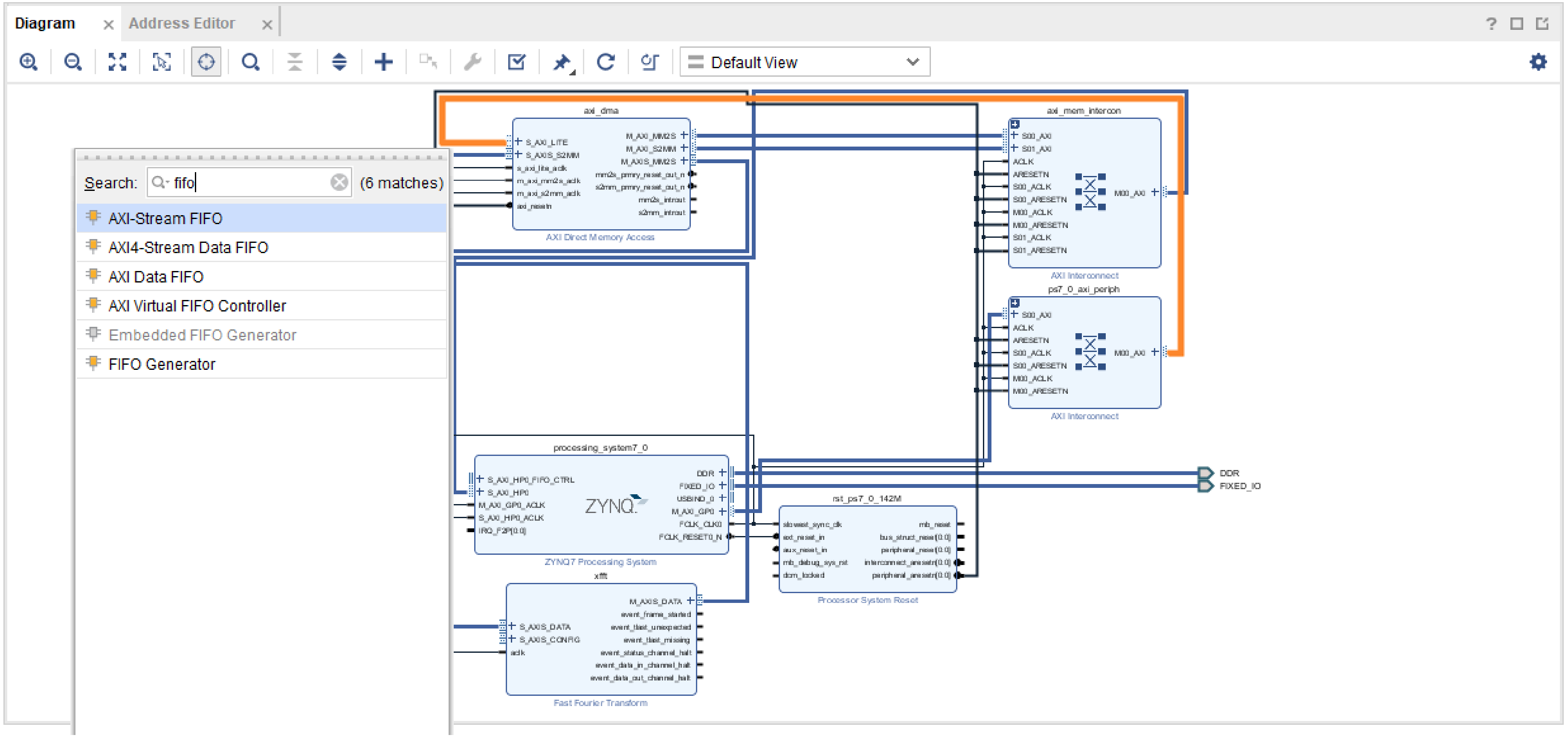
General | Properties | IP

Lab : FFT Acceleration

Click on + and add

in an AXI-Stream

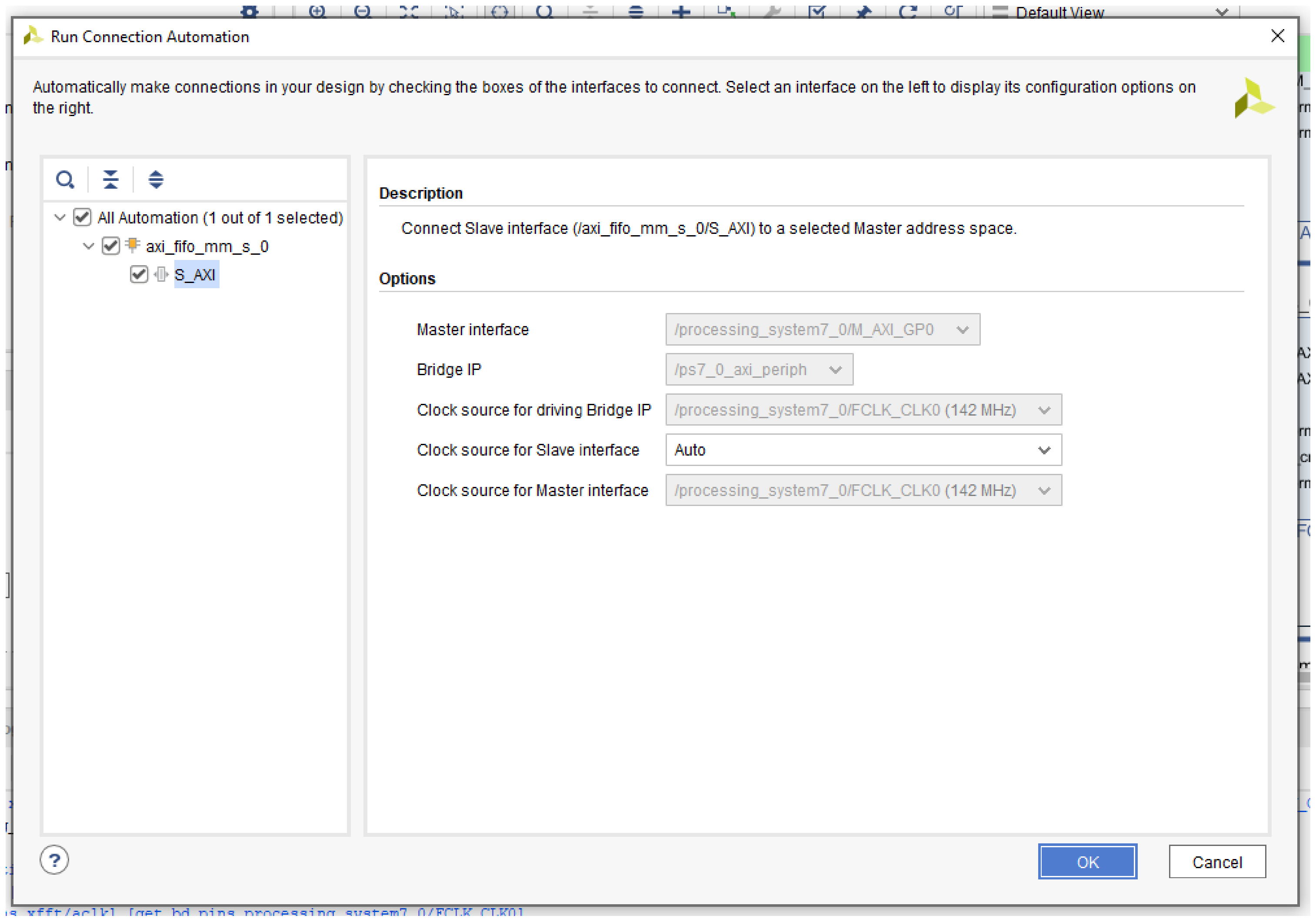
FIFO



Lab : FFT Acceleration

Run the connection

automation and click on OK



Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

- [✓] All Automation (1 out of 1 selected)
  - [✓] axi_fifo_mm_s_0
    - [✓] S_AXI

Description

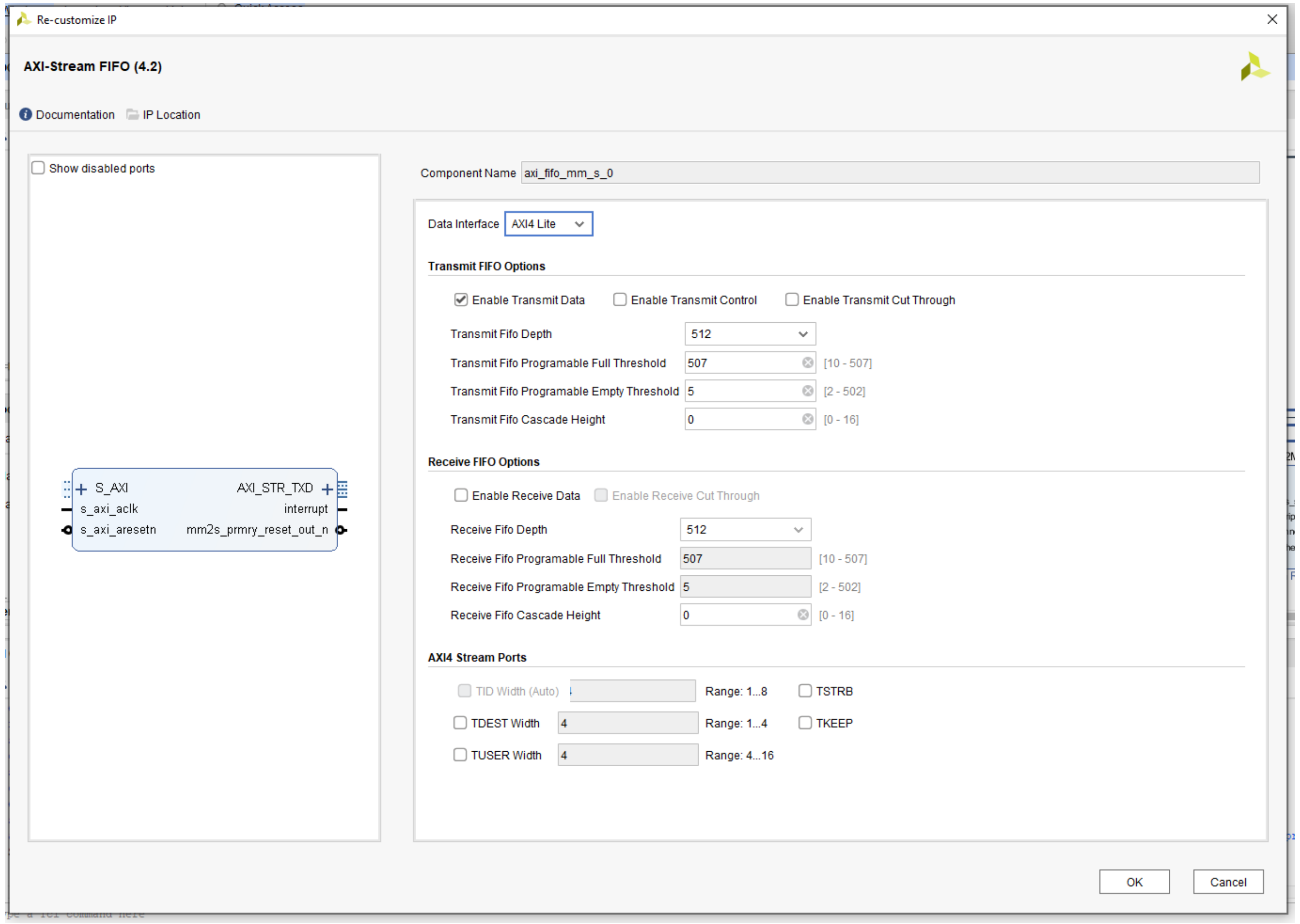
Connect Slave interface (/axi_fifo_mm_s_0/S_AXI) to a selected Master address space.

Options

Master interface	/processing_system7_0/M_AXI_GP0
Bridge IP	/ps7_0_axi_periph
Clock source for driving Bridge IP	/processing_system7_0/FCLK_CLK0 (142 MHz)
Clock source for Slave interface	Auto
Clock source for Master interface	/processing_system7_0/FCLK_CLK0 (142 MHz)

Lab : FFT Acceleration

Double click on the AXI Stream FIFO and configure it to have an AXI Lite Interface and only enable the Transmit Data Interface leave all else unchanged.



Re-customize IP

AXI-Stream FIFO (4.2)

Documentation IP Location

☐ Show disabled ports

Component Name axi_fifo_mm_s_0

Data Interface AXI4 Lite

Transmit FIFO Options

☑ Enable Transmit Data ☐ Enable Transmit Control ☐ Enable Transmit Cut Through

Transmit Fifo Depth	512	
Transmit Fifo Programable Full Threshold	507	[10 - 507]
Transmit Fifo Programable Empty Threshold	5	[2 - 502]
Transmit Fifo Cascade Height	0	[0 - 16]

Receive FIFO Options

☐ Enable Receive Data ☐ Enable Receive Cut Through

Receive Fifo Depth	512	
Receive Fifo Programable Full Threshold	507	[10 - 507]
Receive Fifo Programable Empty Threshold	5	[2 - 502]
Receive Fifo Cascade Height	0	[0 - 16]

AXI4 Stream Ports

☐ TID Width (Auto)		Range: 1..8	☐ TSTRB
☐ TDEST Width	4	Range: 1..4	☐ TKEEP
☐ TUSER Width	4	Range: 4...16	

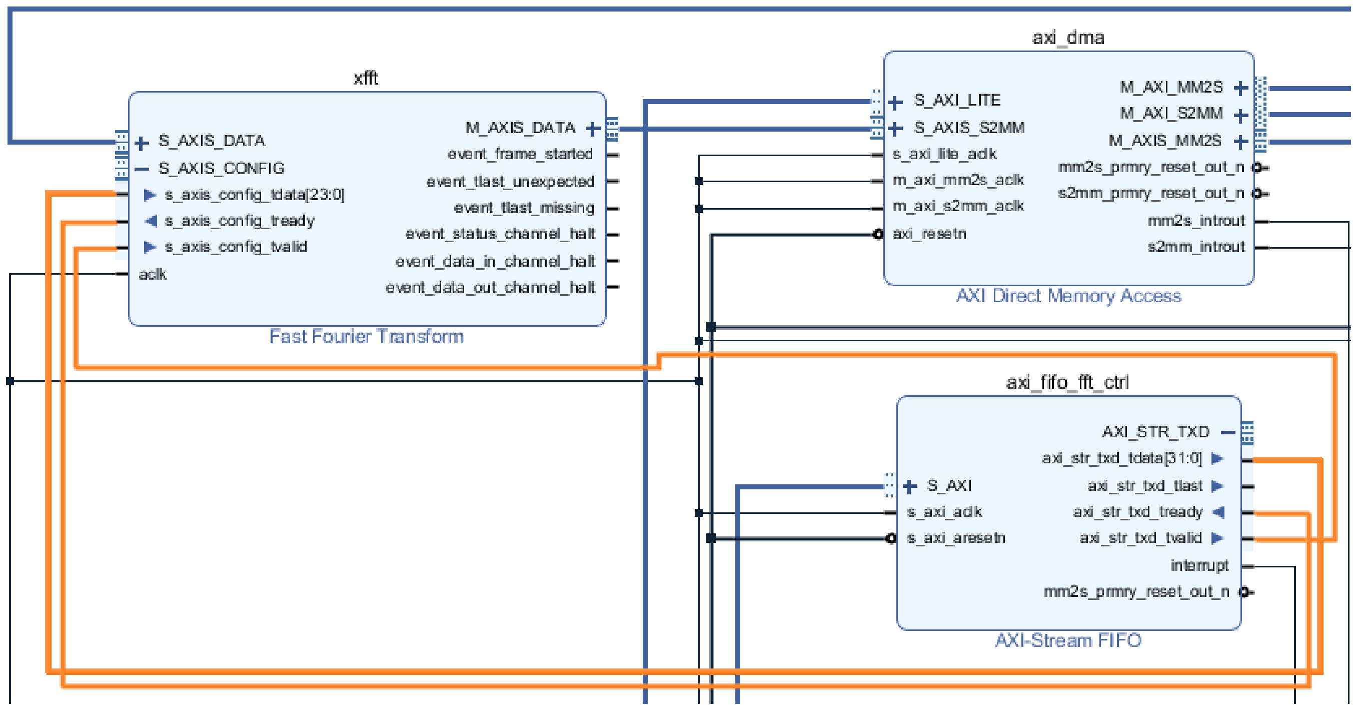
OK Cancel

Lab : FFT Acceleration

Connect the AXI STR TXD tdata,

tlast and tvalid signals to the

xFFT S AXIS config



Lab : FFT Acceleration

Click on + and add in a AXI

Interrupt Controller

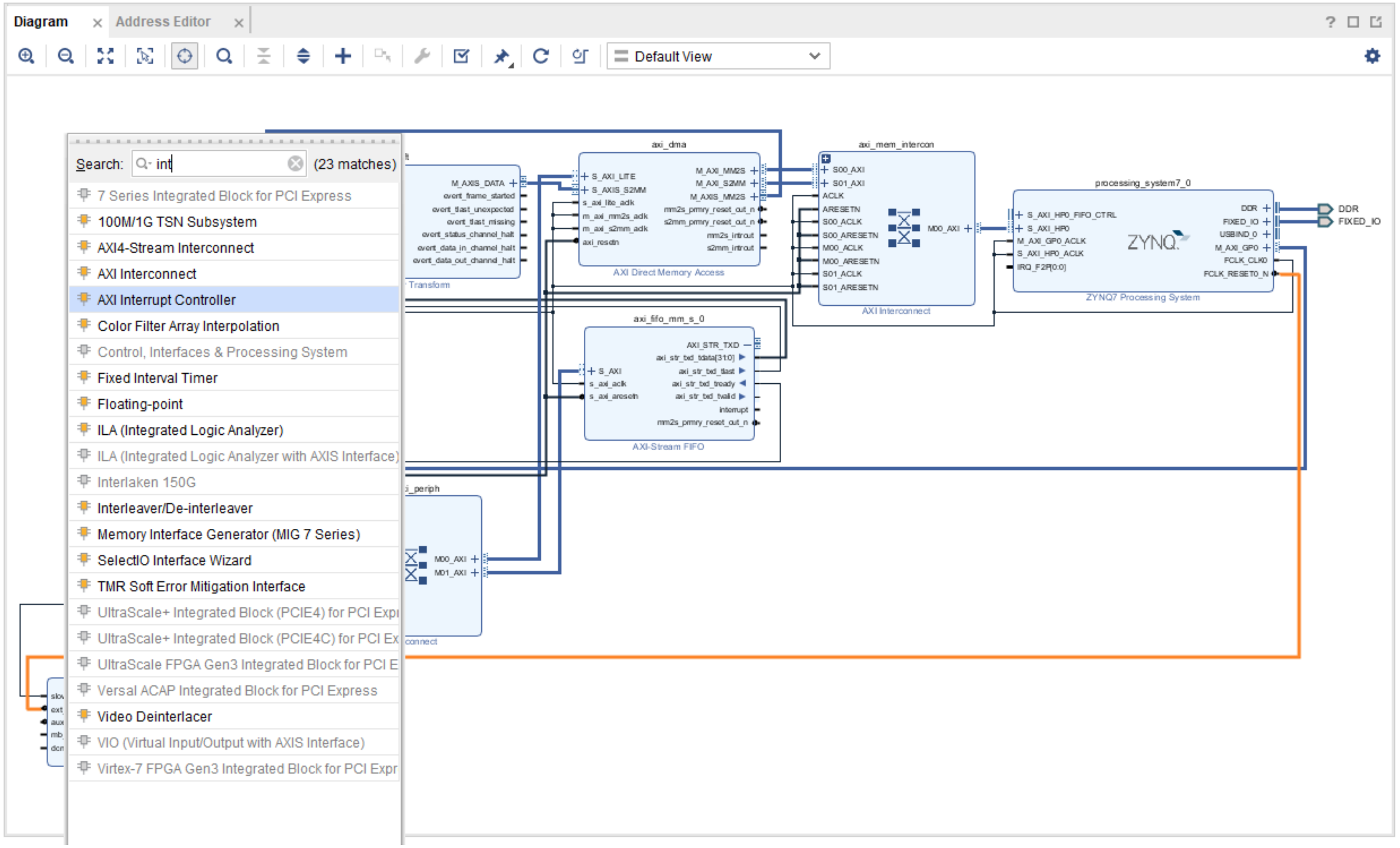
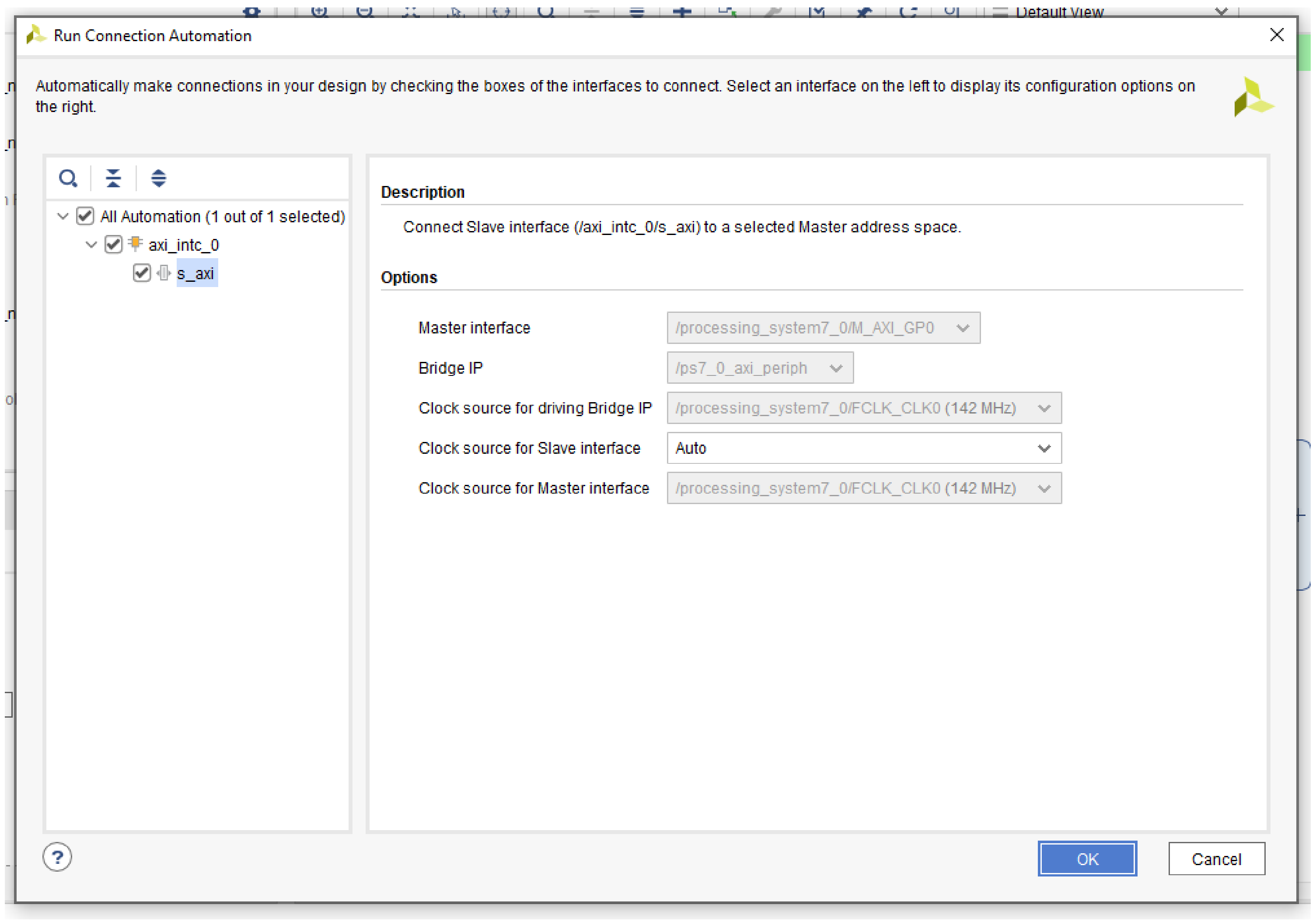


Diagram
Address Editor
Default View
Search: int
(23 matches)
7 Series Integrated Block for PCI Express
100M/1G TSN Subsystem
AXI4-Stream Interconnect
AXI Interconnect
AXI Interrupt Controller
Color Filter Array Interpolation
Control, Interfaces & Processing System
Fixed Interval Timer
Floating-point
ILA (Integrated Logic Analyzer)
ILA (Integrated Logic Analyzer with AXIS Interface)
Interlaken 150G
Interleaver/De-interleaver
Memory Interface Generator (MIG 7 Series)
SelectIO Interface Wizard
TMR Soft Error Mitigation Interface
UltraScale+ Integrated Block (PCIE4) for PCI Exp
UltraScale+ Integrated Block (PCIE4C) for PCI Ex
UltraScale FPGA Gen3 Integrated Block for PCI E
Versal ACAP Integrated Block for PCI Express
Video Deinterlacer
VIO (Virtual Input/Output with AXIS Interface)
Virtex-7 FPGA Gen3 Integrated Block for PCI Expr
axi_dma
AXI Direct Memory Access
axi_mem_intercon
AXI Interconnect
processing_system7_0
ZYNQ7 Processing System
axi_fifo_mm_s_0
AXI-Stream FIFO
DDR
FIXED_IO

Lab : FFT Acceleration

Run the connection

automation



Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

- [✓] All Automation (1 out of 1 selected)
  - [✓] axi_intc_0
    - [✓] s_axi

Description

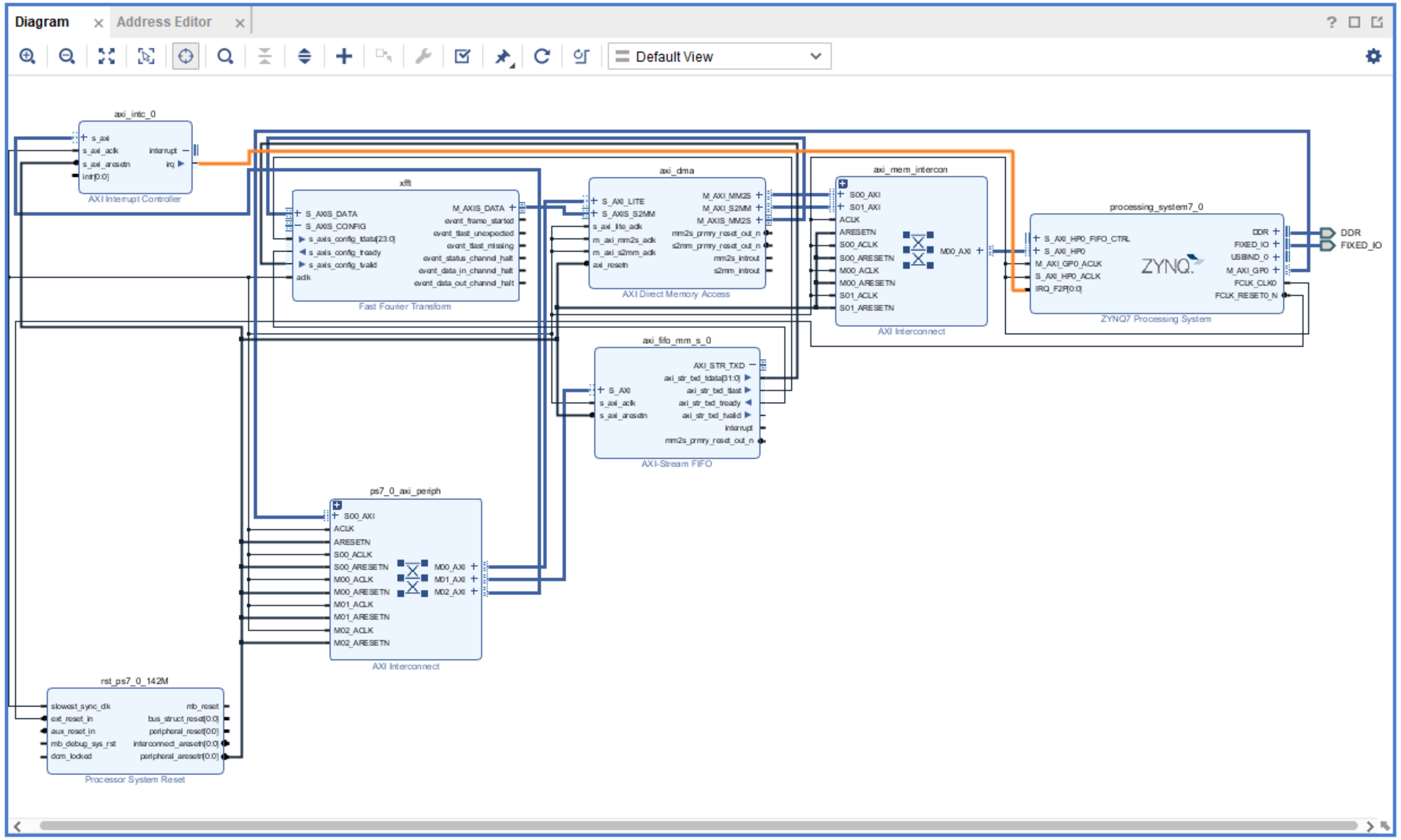
Connect Slave interface (/axi_intc_0/s_axi) to a selected Master address space.

Options

Master interface	/processing_system7_0/M_AXI_GP0
Bridge IP	/ps7_0_axi_periph
Clock source for driving Bridge IP	/processing_system7_0/FCLK_CLK0 (142 MHz)
Clock source for Slave interface	Auto
Clock source for Master interface	/processing_system7_0/FCLK_CLK0 (142 MHz)

Lab : FFT Acceleration

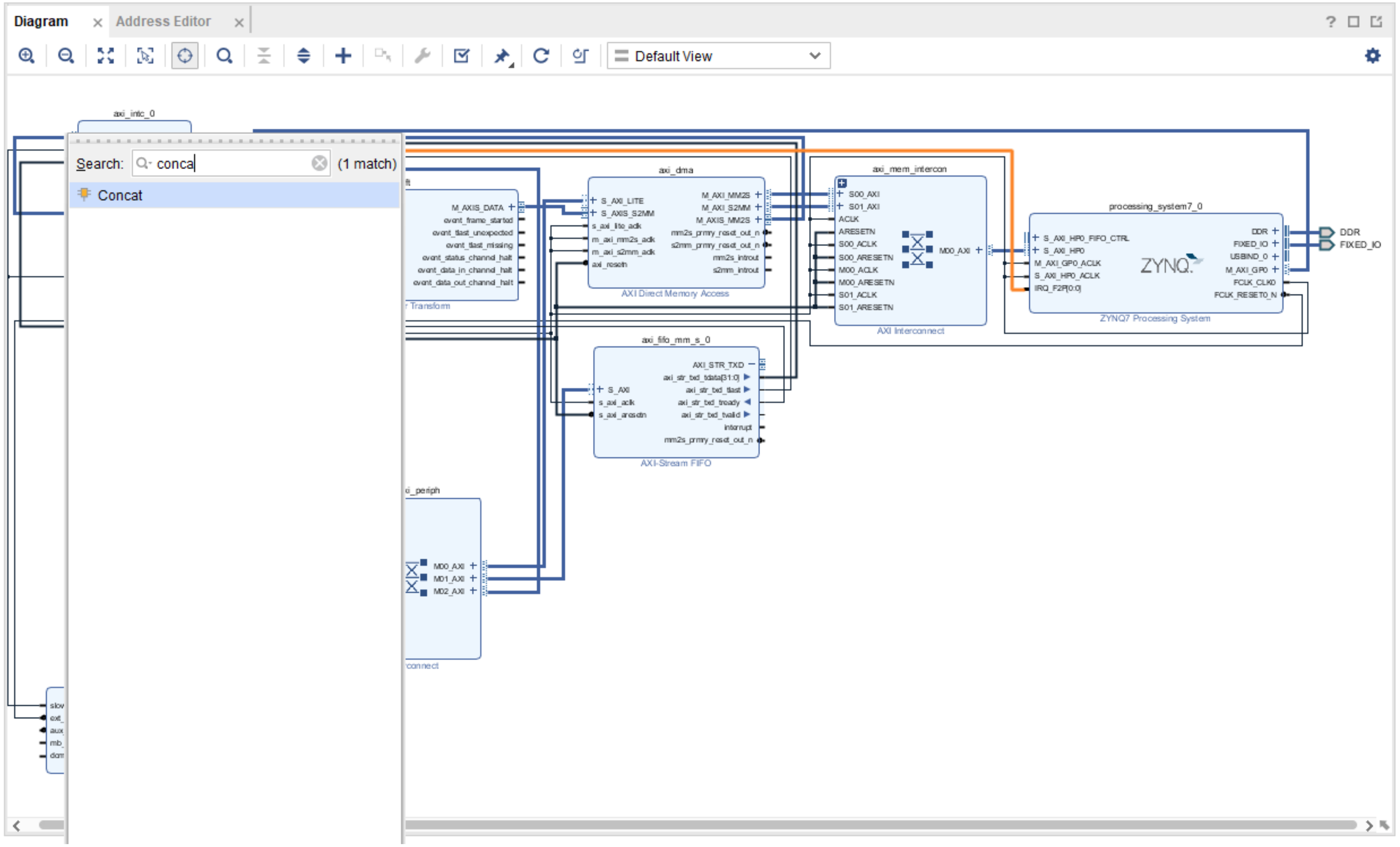
Connect the IRQ output from the AXI Interrupt Controller to the IRQF2P port on the Zynq



Lab : FFT Acceleration

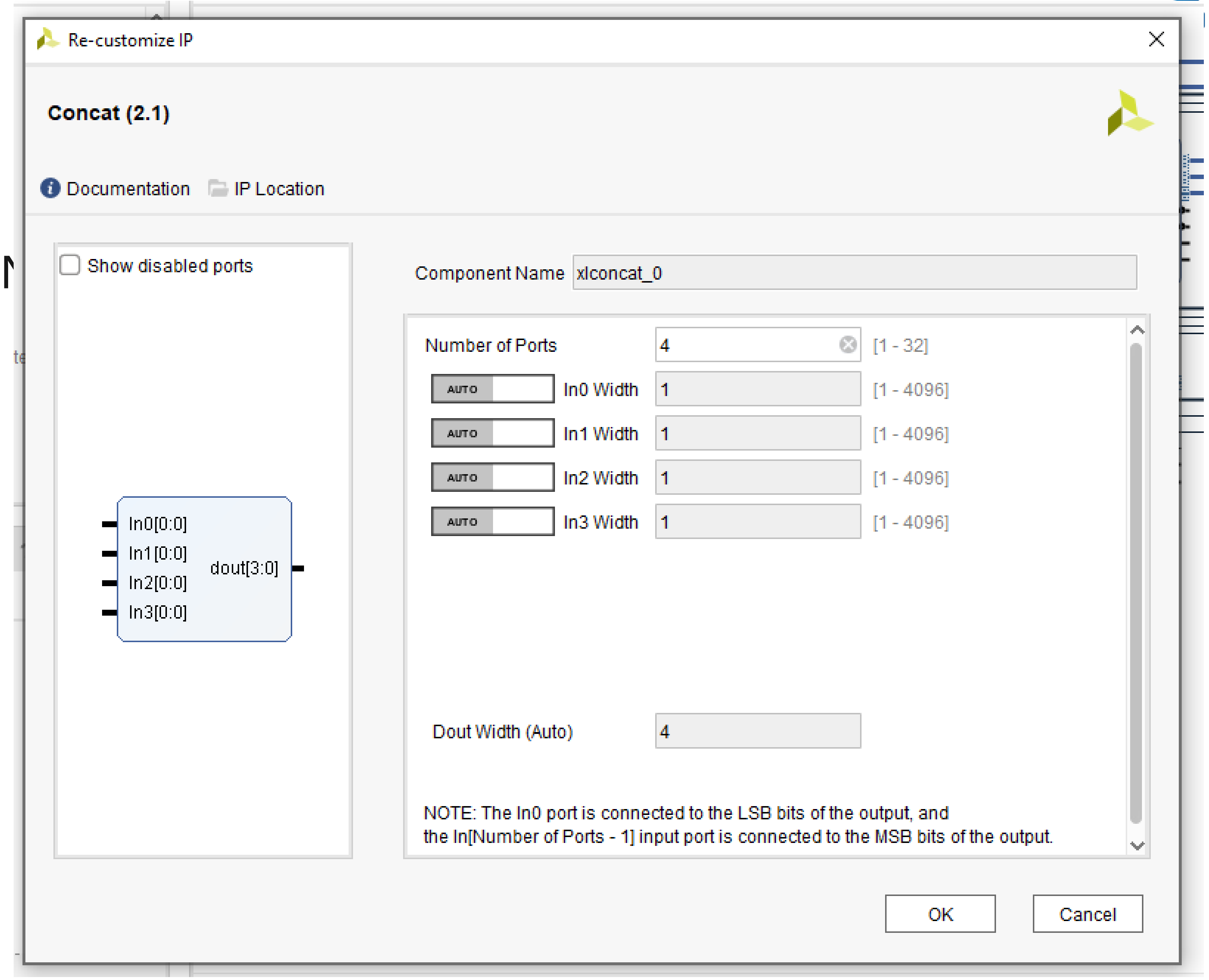
Click on + and add in a

concat block



Lab :

Go to PYN



Re-customize IP

Concat (2.1)

Documentation IP Location

Show disabled ports

Component Name: xlconcat_0

Number of Ports: 4 [1 - 32]

In0 Width: 1 [1 - 4096]

In1 Width: 1 [1 - 4096]

In2 Width: 1 [1 - 4096]

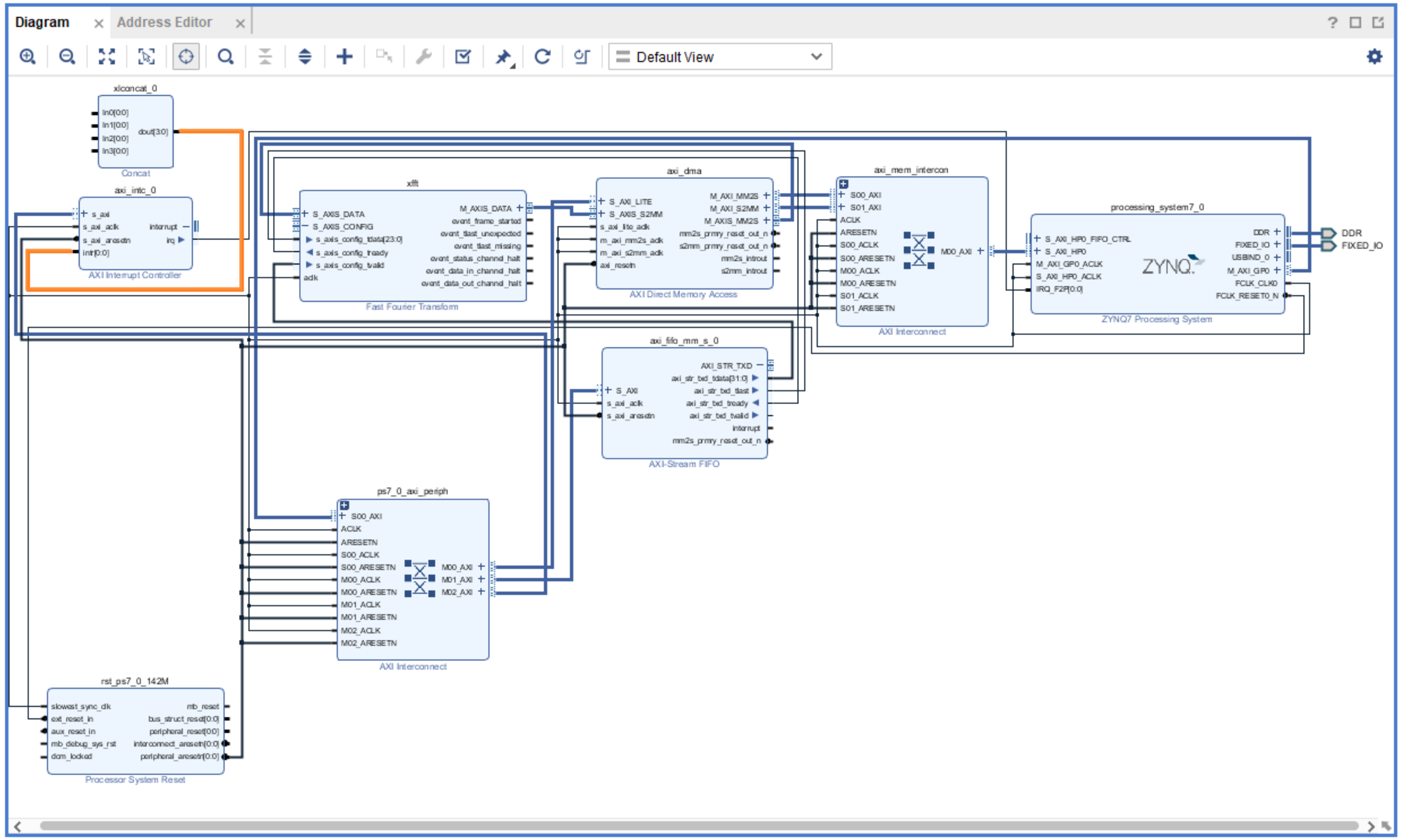
In3 Width: 1 [1 - 4096]

Dout Width (Auto): 4

NOTE: The In0 port is connected to the LSB bits of the output, and
the In[Number of Ports - 1] input port is connected to the MSB bits of the output.

Lab : FFT Acceleration

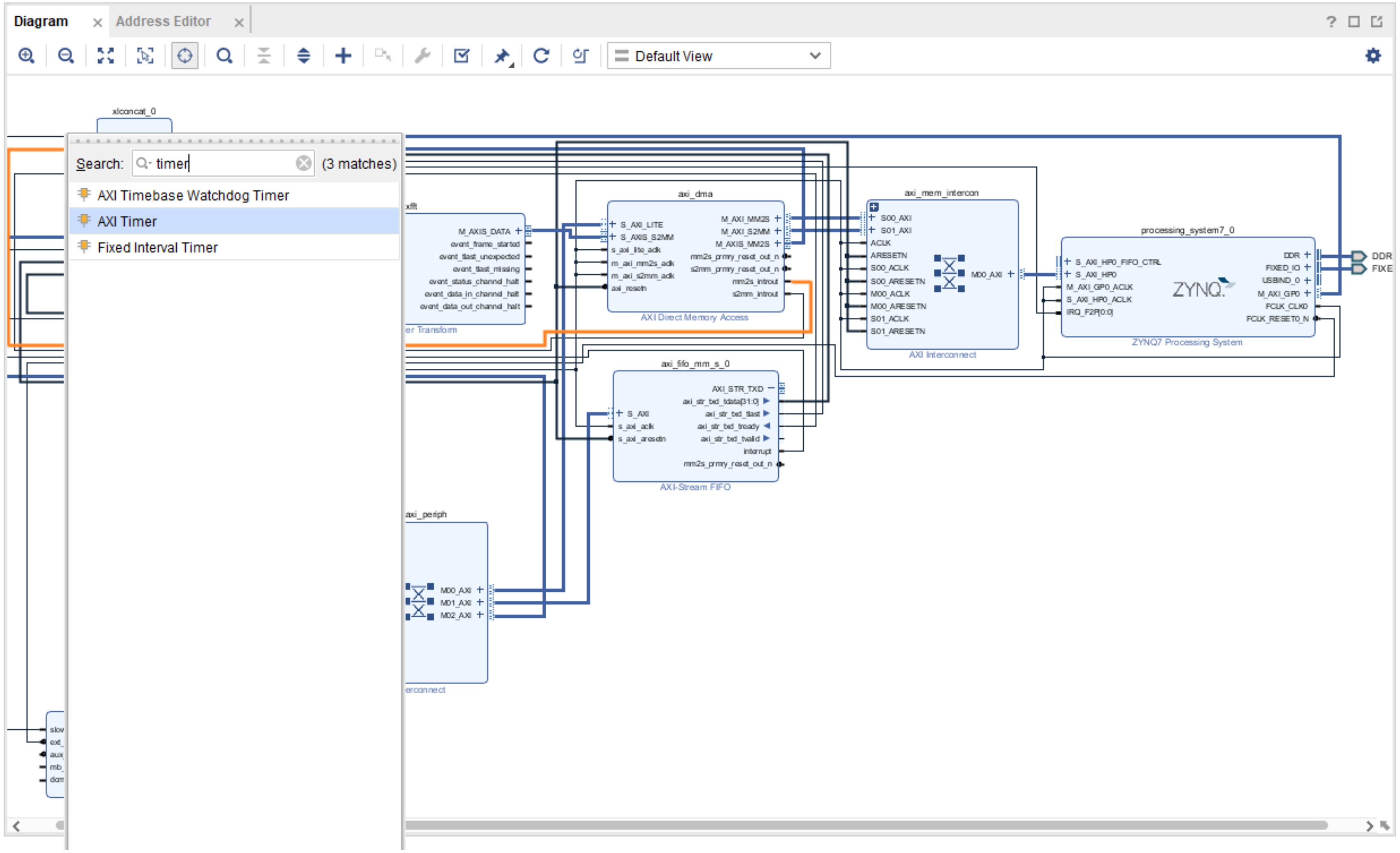
Connect the output of the concat block to the AXI Interrupt controller INT input



Lab : FFT Acceleration

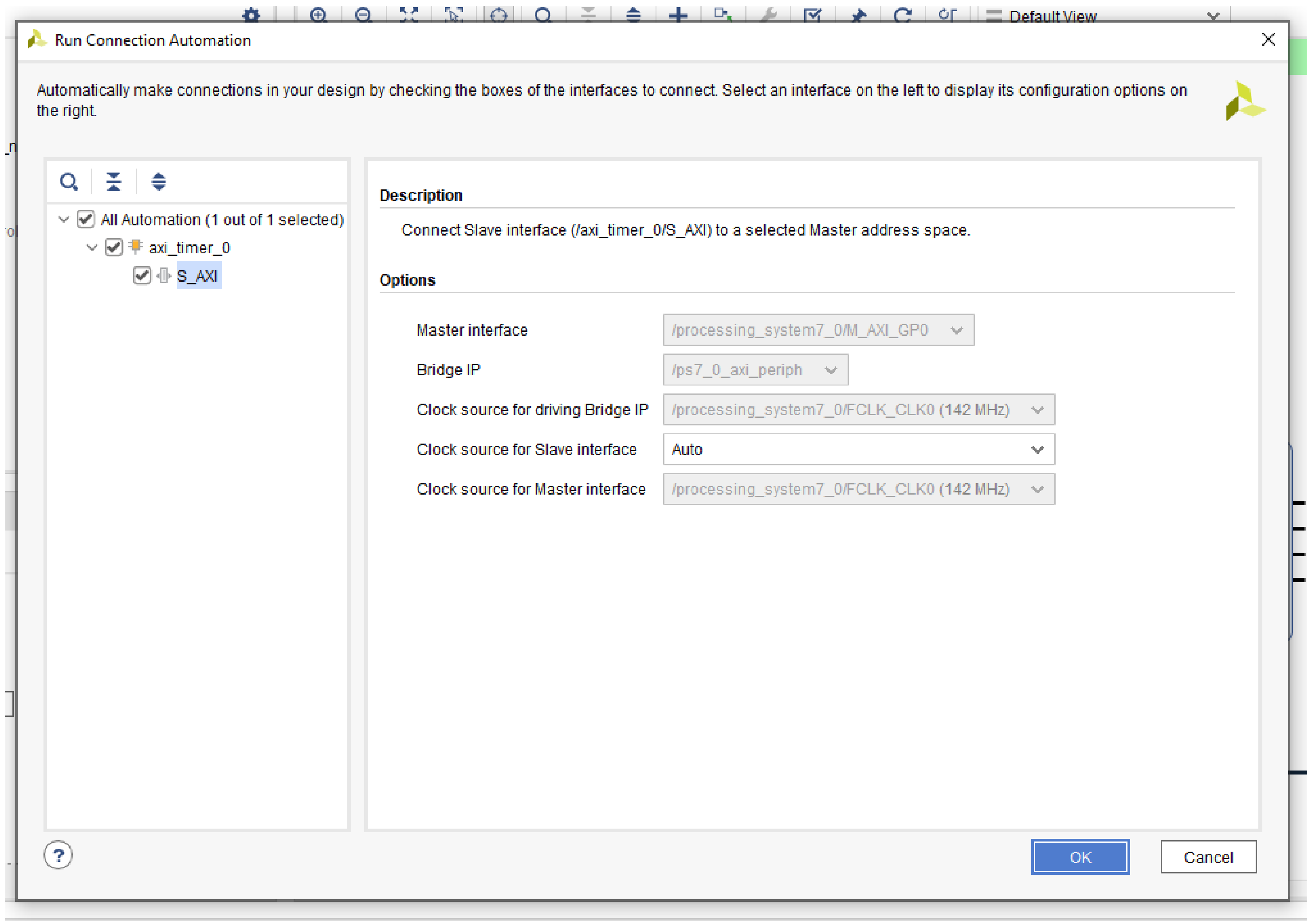
Click on the + symbol

and add in a AXI Timer



Lab : FFT Acceleration

Run the connection automation



Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

- ✓ All Automation (1 out of 1 selected)
  - ✓ axi_timer_0
    - ✓ S_AXI

Description

Connect Slave interface (/axi_timer_0/S_AXI) to a selected Master address space.

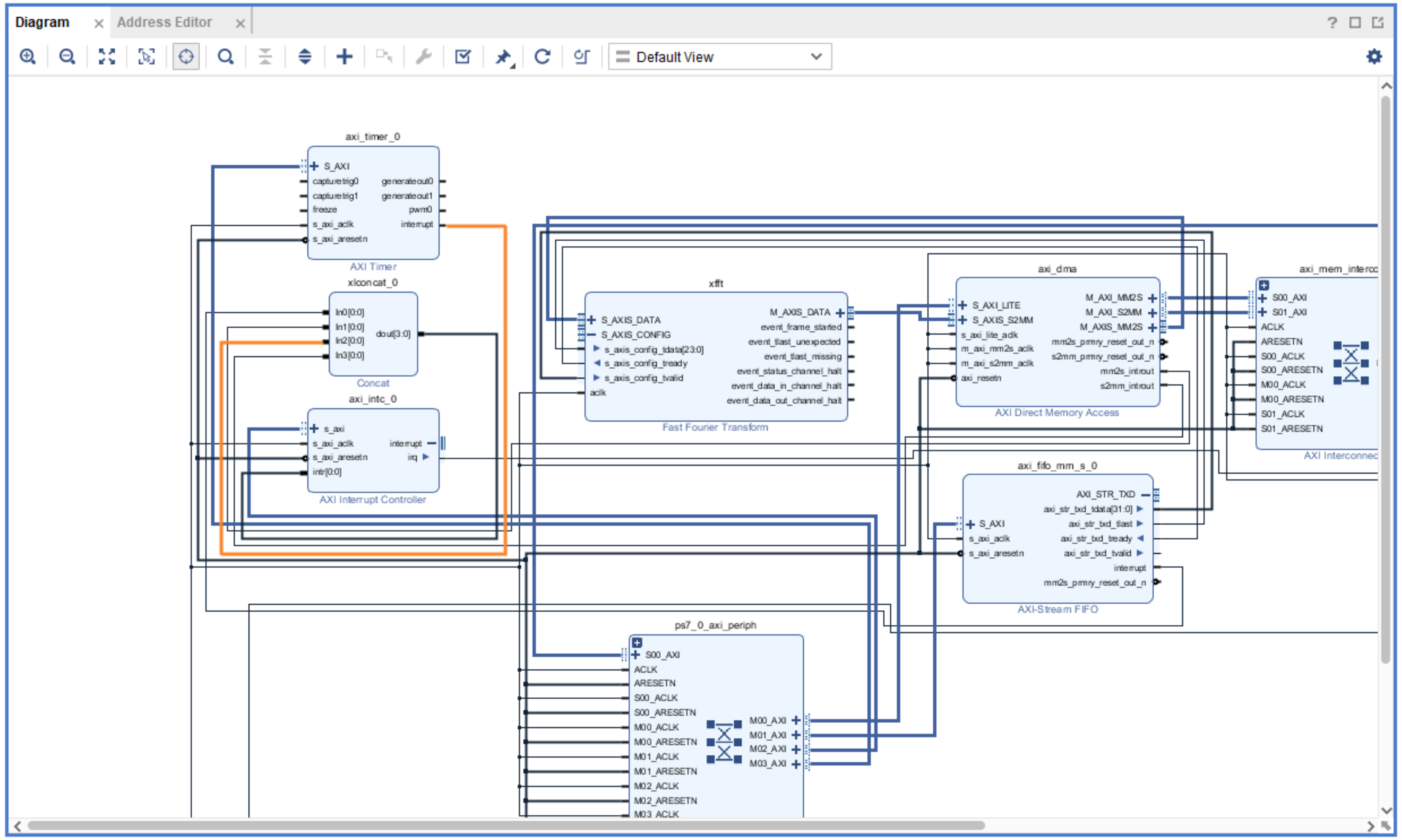
Options

Master interface	/processing_system7_0/M_AXI_GP0
Bridge IP	/ps7_0_axi_periph
Clock source for driving Bridge IP	/processing_system7_0/FCLK_CLK0 (142 MHz)
Clock source for Slave interface	Auto
Clock source for Master interface	/processing_system7_0/FCLK_CLK0 (142 MHz)

Lab : FFT Acceleration

Connect the interrupts to the concat block

- AXI Timer
- AXI DMA MM2S_INTOUT
- AXI DMA S2MM_INTOUT
- AXI Stream FIFO



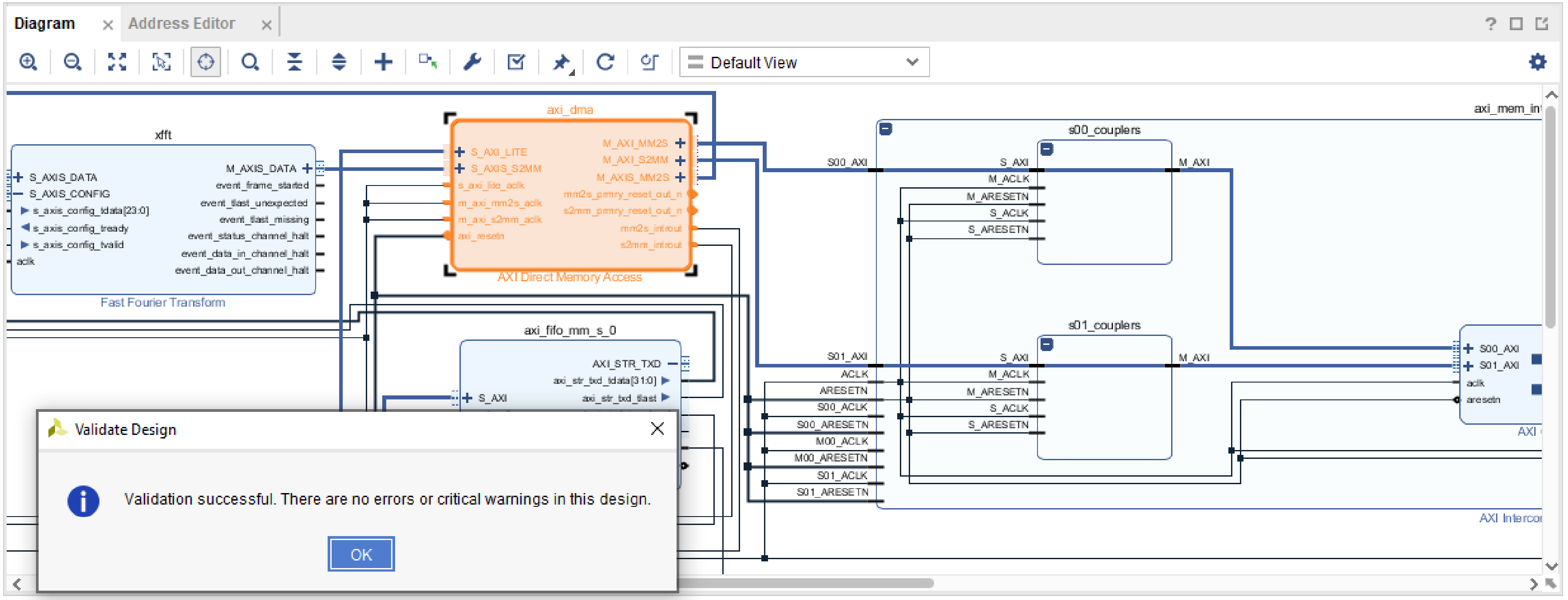
Lab : FFT Acceleration

Validate the design

there should be no

error or critical

warnings



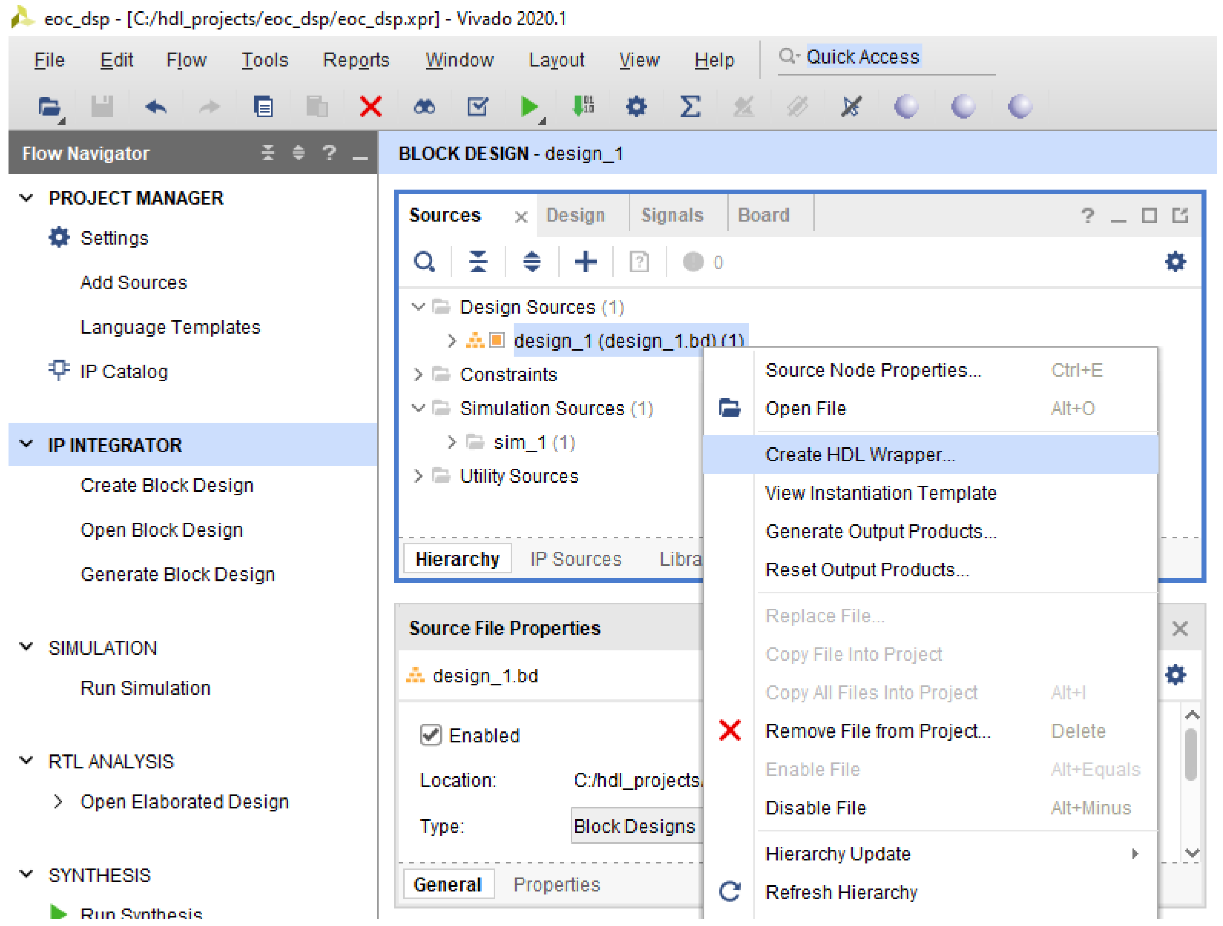
Validate Design

Validation successful. There are no errors or critical warnings in this design.

Lab : FFT Acceleration

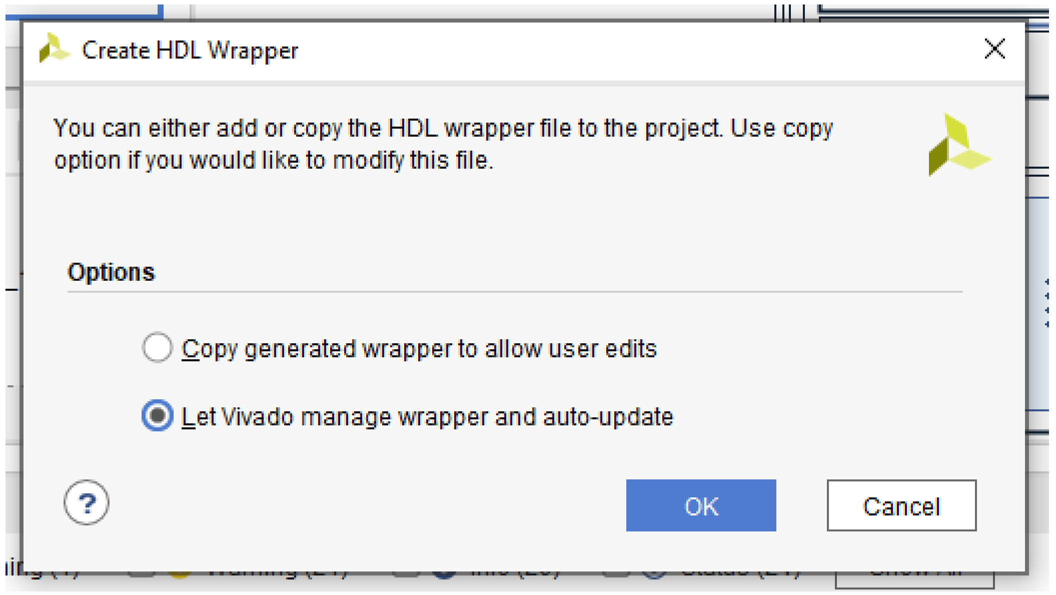
Right click on the design and

select Create HDL Wrapper



Lab : FFT Acceleration

Let Vivado manage the wrapper



Create HDL Wrapper

You can either add or copy the HDL wrapper file to the project. Use copy option if you would like to modify this file.

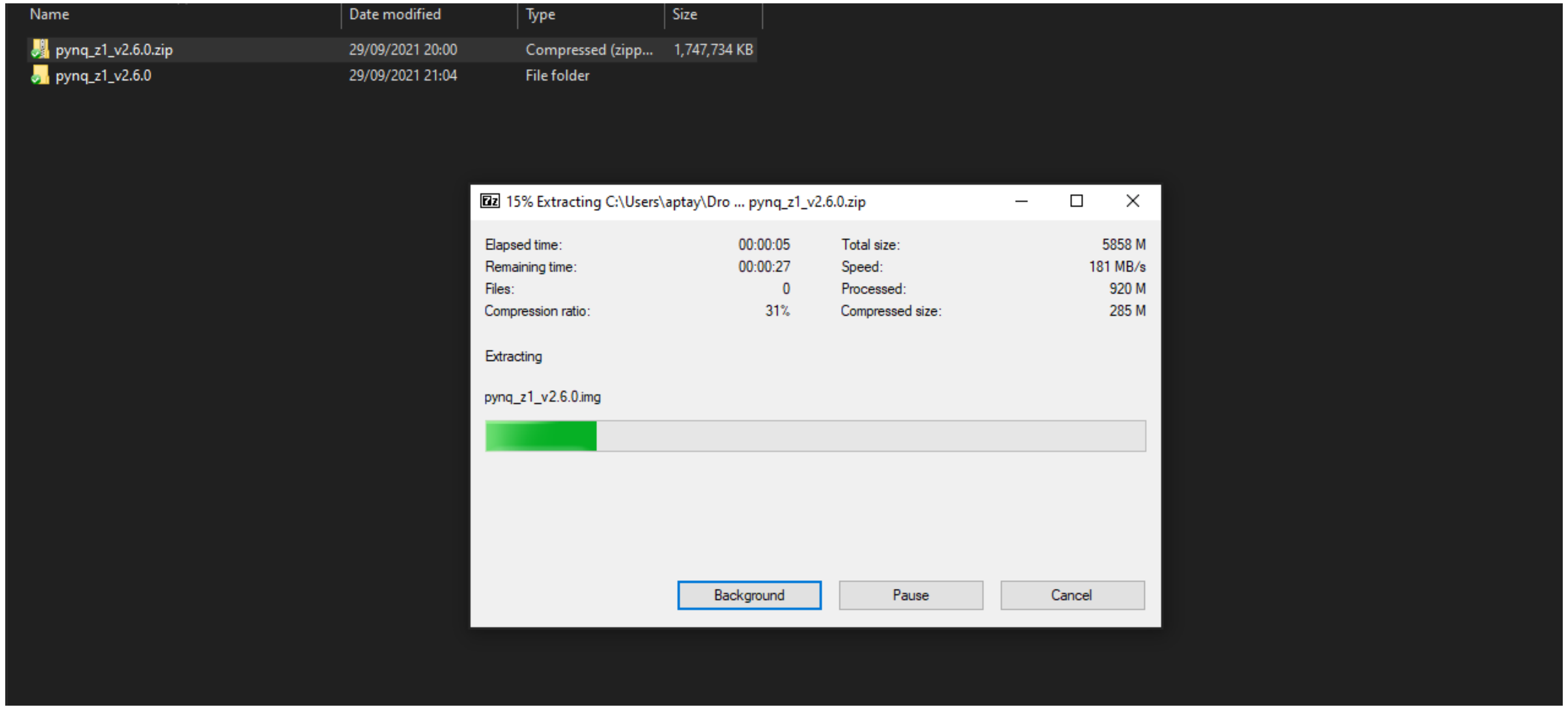
Options

( ) Copy generated wrapper to allow user edits

(●) Let Vivado manage wrapper and auto-update

Lab : FFT Acceleration

Extract the downloaded PYNQ image



Name	Date modified	Type	Size
pynq_z1_v2.6.0.zip	29/09/2021 20:00	Compressed (zipp...	1,747,734 KB
pynq_z1_v2.6.0	29/09/2021 21:04	File folder	

15% Extracting C:\Users\aptay\Dro ... pynq_z1_v2.6.0.zip

Elapsed time:	00:00:05	Total size:	5858 M
Remaining time:	00:00:27	Speed:	181 MB/s
Files:	0	Processed:	920 M
Compression ratio:	31%	Compressed size:	285 M

Extracting

pynq_z1_v2.6.0.img

Lab : FFT Acceleration

Write the image to a SD card. Once completed insert the SD card in the Arty Z7-20. Connect a Ethernet cable and power via a USB cable

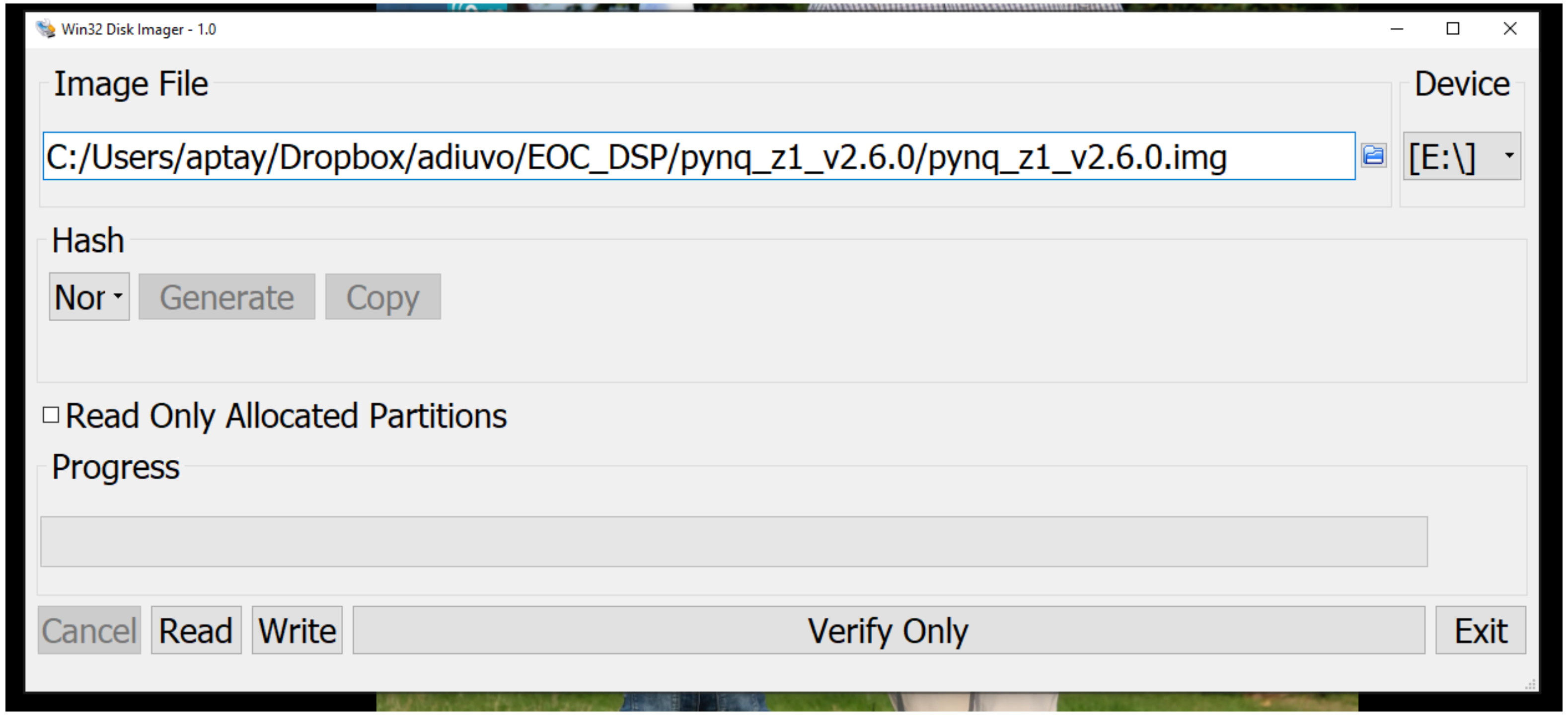

Win32 Disk Imager - 1.0

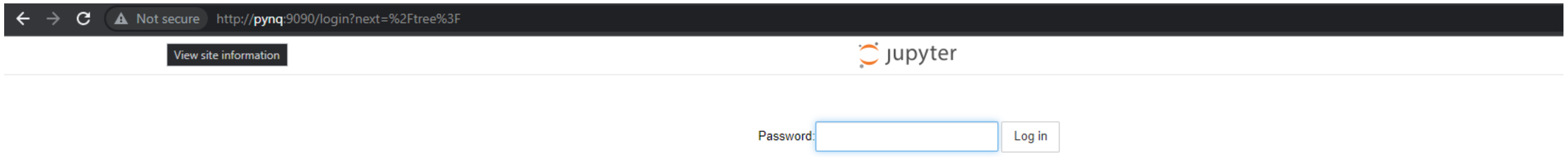
Image File: C:/Users/aptay/Dropbox/adiuvo/EOC_DSP/pynq_z1_v2.6.0/pynq_z1_v2.6.0.img

Device: [E:\]

Lab : FFT Acceleration

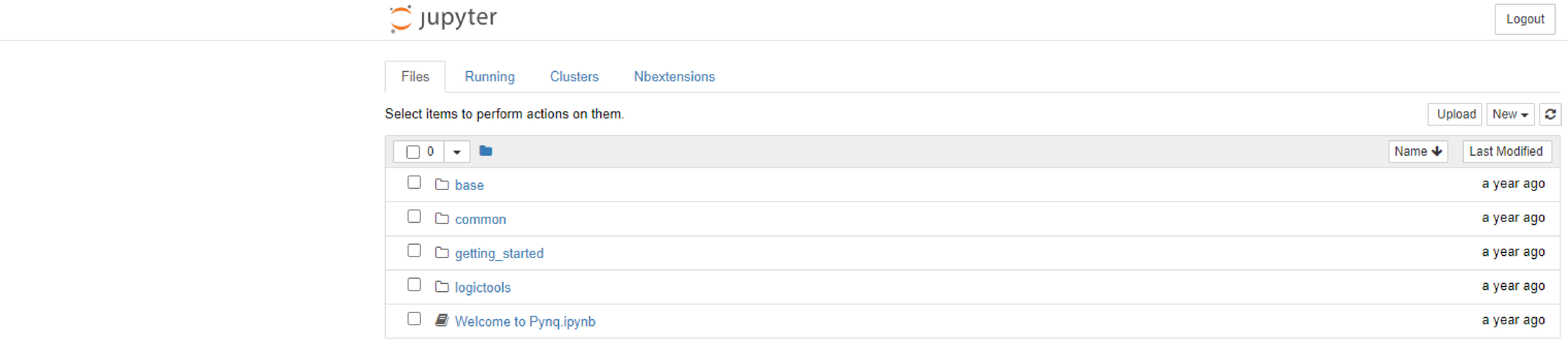
Once the board boots, wait for the LEDs to flash. In a browser enter the address pynq:9090

when prompted enter the password xilinx



Lab : FFT Acceleration

Once logged in you should see the folder structure below



Select items to perform actions on them.

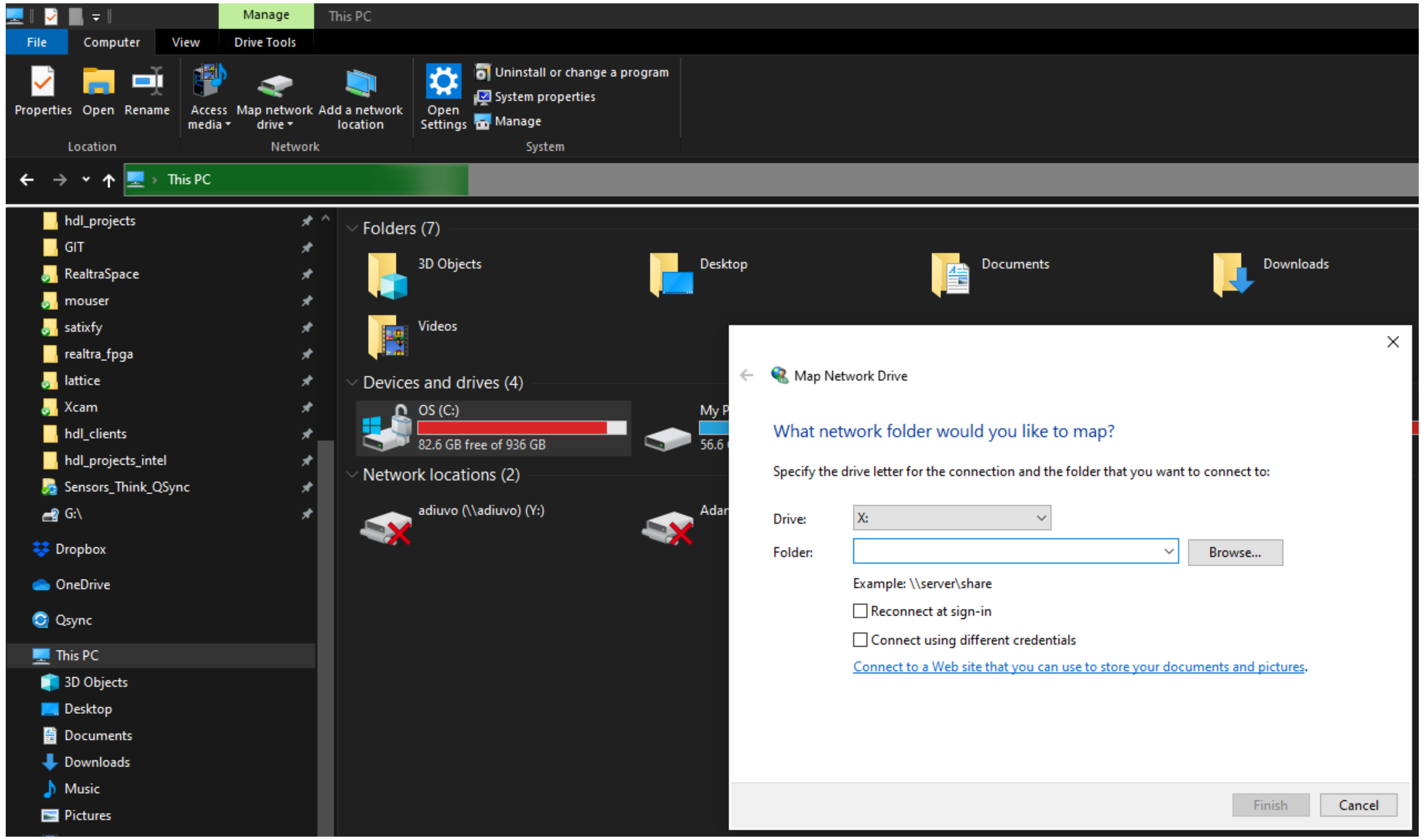
base	a year ago
common	a year ago
getting_started	a year ago
logictools	a year ago
Welcome to Pynq.ipynb	a year ago

Lab : FFT Acceleration

In a file explorer map a network drive to

\\pynq \xilinx

Select connect using different credentials



Map Network Drive

What network folder would you like to map?

Specify the drive letter for the connection and the folder that you want to connect to:

Drive: X:

Folder:

Browse...

Example: \\server\share

☐ Reconnect at sign-in

☐ Connect using different credentials

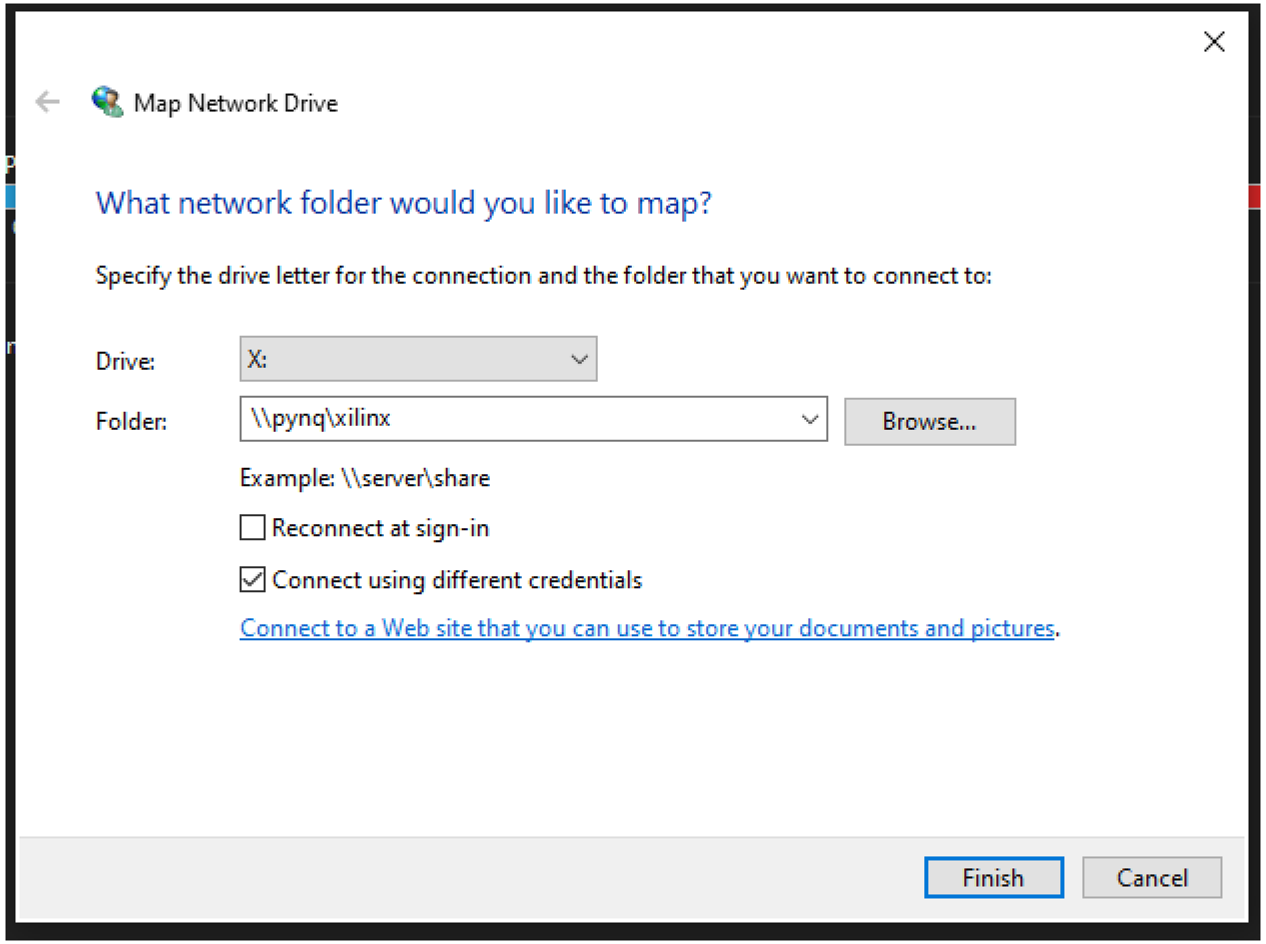
Connect to a Web site that you can use to store your documents and pictures.

Finish

Cancel

Lab : FFT Acceleration

Completed Map drive, click OK


Map Network Drive

What network folder would you like to map?

Specify the drive letter for the connection and the folder that you want to connect to:

Drive: X:

Folder: \\pynq\xilinx

Example: \\server\share

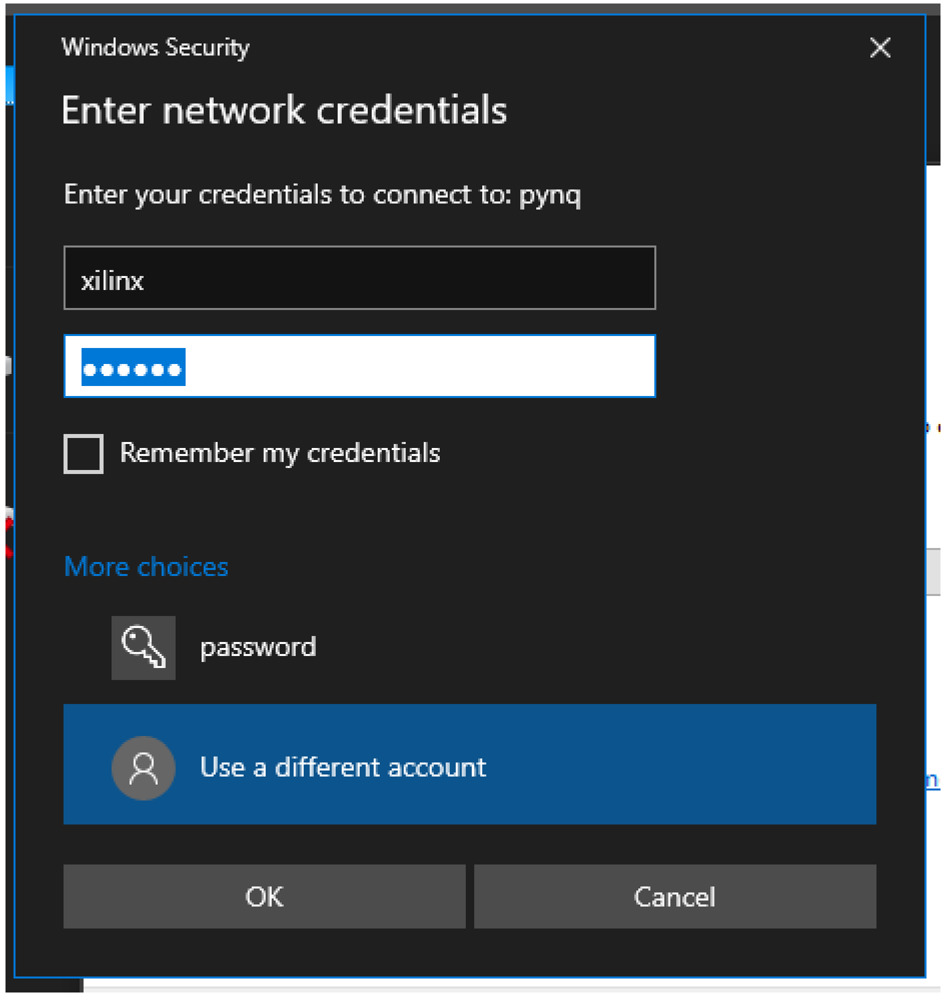
- [ ] Reconnect at sign-in
- [x] Connect using different credentials

Connect to a Web site that you can use to store your documents and pictures.

Lab : FFT Acceleration

Enter the username and password as

Xilinx click OK



Windows Security

Enter network credentials

Enter your credentials to connect to: pynq

xilinx

●●●●●●

☐ Remember my credentials

More choices

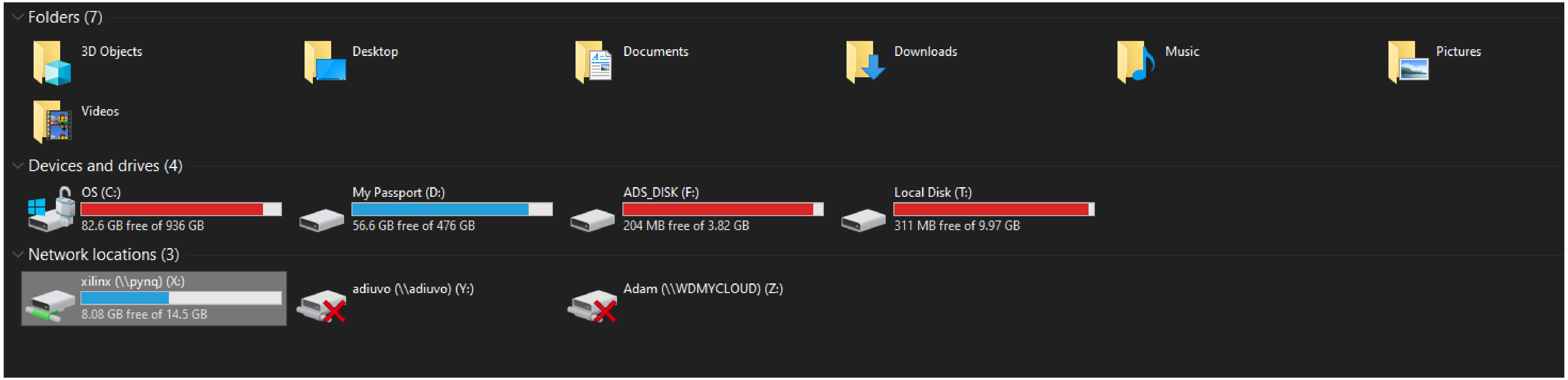
password

Use a different account

OK Cancel

Lab : FFT Acceleration

The pynq drive should not appear as a samba server



Folders (7)

3D Objects
Desktop
Documents
Downloads
Music
Pictures
Videos

Devices and drives (4)

OS (C:)
82.6 GB free of 936 GB

My Passport (D:)
56.6 GB free of 476 GB

ADS_DISK (F:)
204 MB free of 3.82 GB

Local Disk (T:)
311 MB free of 9.97 GB

Network locations (3)

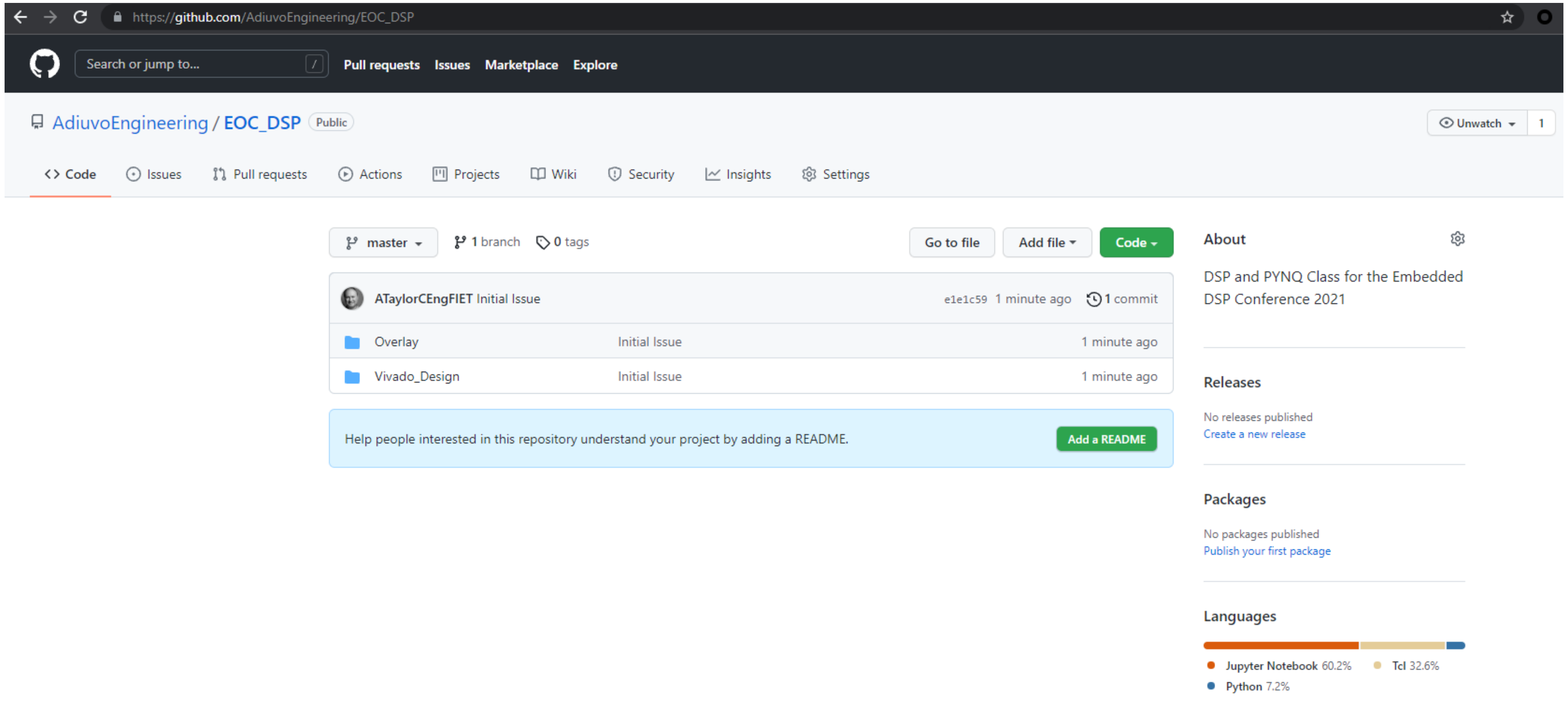
xilinx (\\pynq) (X:)
8.08 GB free of 14.5 GB

adiuvo (\\adiuvo) (Y:)

Adam (\\WDMYCLOUD) (Z:)

Lab : FFT Acceleration

Clone the repository - https://github.com/ATaylorCEngFIET/MZ448



https://github.com/AdiuvoEngineering/EOC_DSP

AdiuvoEngineering / EOC_DSP Public

ATaylorCEngFIET Initial Issue	e1e1c59 1 minute ago	1 commit
Overlay	Initial Issue	1 minute ago
Vivado_Design	Initial Issue	1 minute ago

Help people interested in this repository understand your project by adding a README.

About

DSP and PYNQ Class for the Embedded DSP Conference 2021

Releases

No releases published

Create a new release

Packages

No packages published

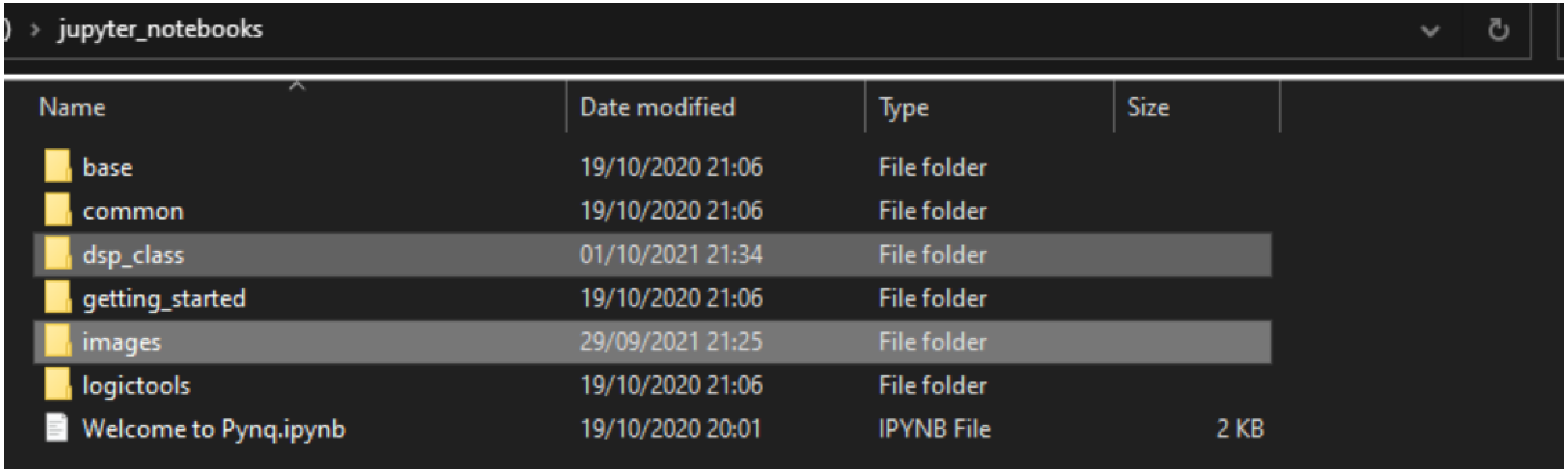
Publish your first package

Languages

● Jupyter Notebook 60.2% ● Tcl 32.6% ● Python 7.2%

Lab : FFT Acceleration

From the Cloned Repo copy the directory Images and dsp_class to the Pynq boards Jupyter notebooks directory

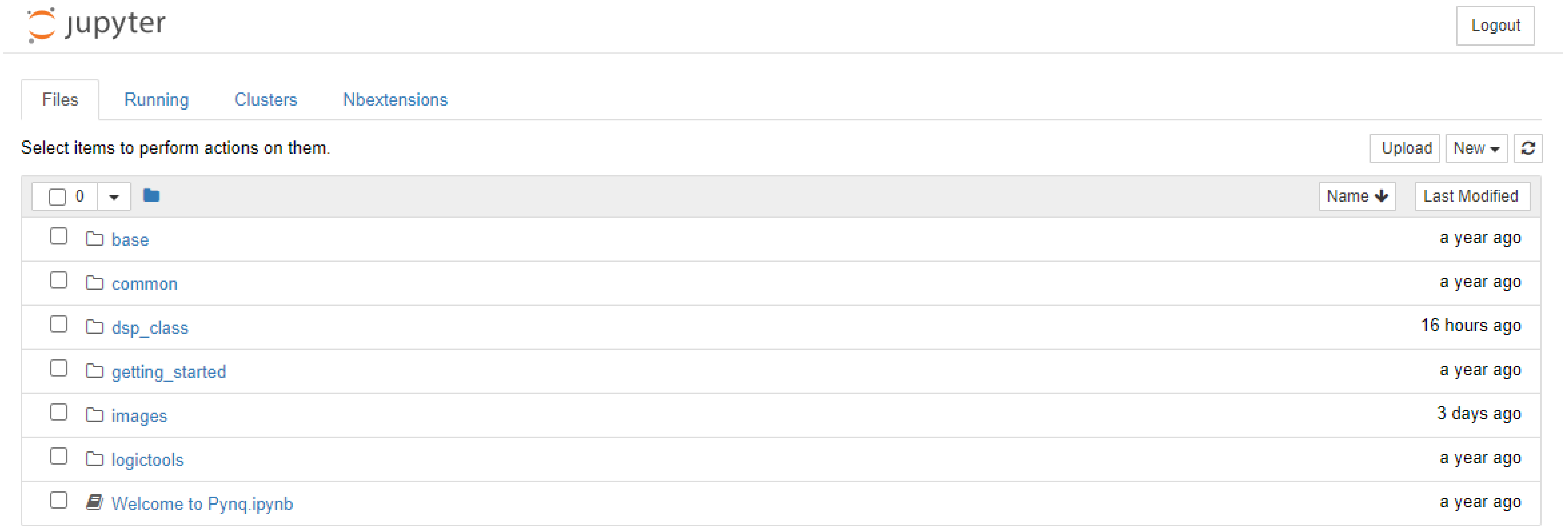


) › jupyter_notebooks

Name	Date modified	Type	Size
base	19/10/2020 21:06	File folder	
common	19/10/2020 21:06	File folder	
dsp_class	01/10/2021 21:34	File folder	
getting_started	19/10/2020 21:06	File folder	
images	29/09/2021 21:25	File folder	
logictools	19/10/2020 21:06	File folder	
Welcome to Pynq.ipynb	19/10/2020 20:01	IPYNB File	2 KB

Lab : FFT Acceleration

You should see a new directory in the PYNQ environment, select DSP_CLASS

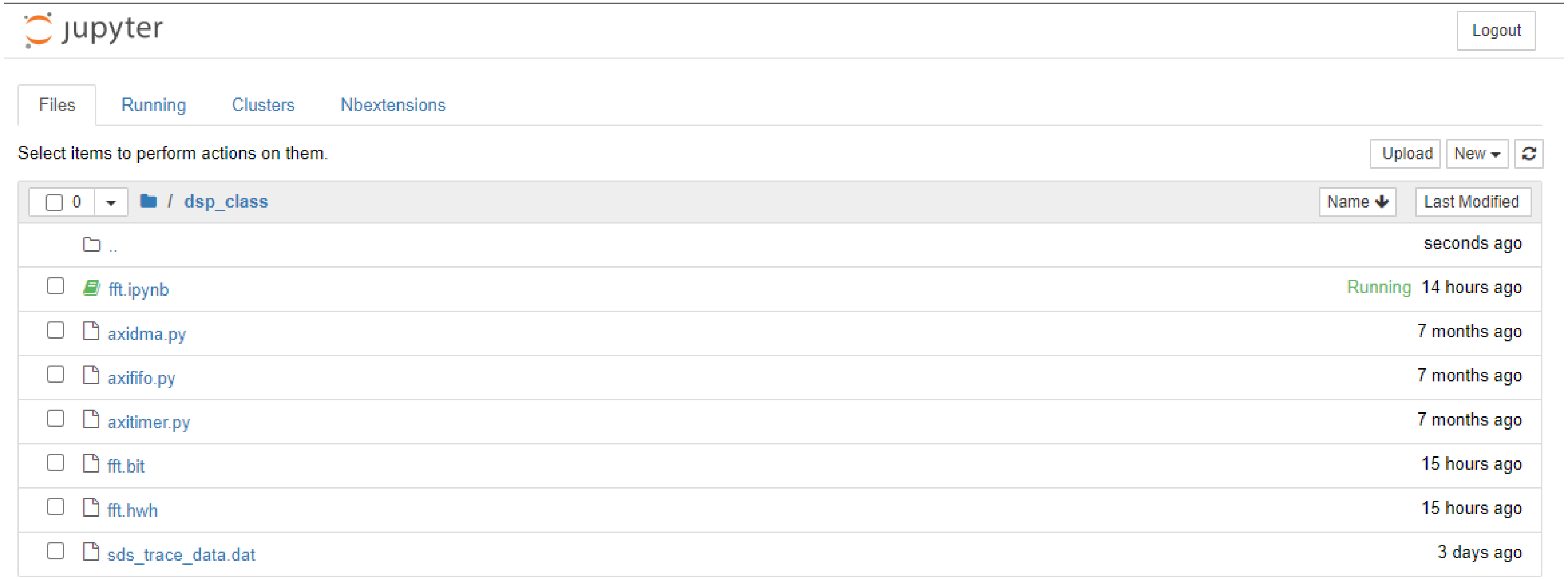


Select items to perform actions on them.

Name	Last Modified
base	a year ago
common	a year ago
dsp_class	16 hours ago
getting_started	a year ago
images	3 days ago
logictools	a year ago
Welcome to Pynq.ipynb	a year ago

Lab : FFT Acceleration

Select fft.ipynb it will open and start running



Select items to perform actions on them.

dsp_class

Name	Last Modified
..	seconds ago
fft.ipynb	Running 14 hours ago
axidma.py	7 months ago
axififo.py	7 months ago
axitimer.py	7 months ago
fft.bit	15 hours ago
fft.hwh	15 hours ago
sds_trace_data.dat	3 days ago

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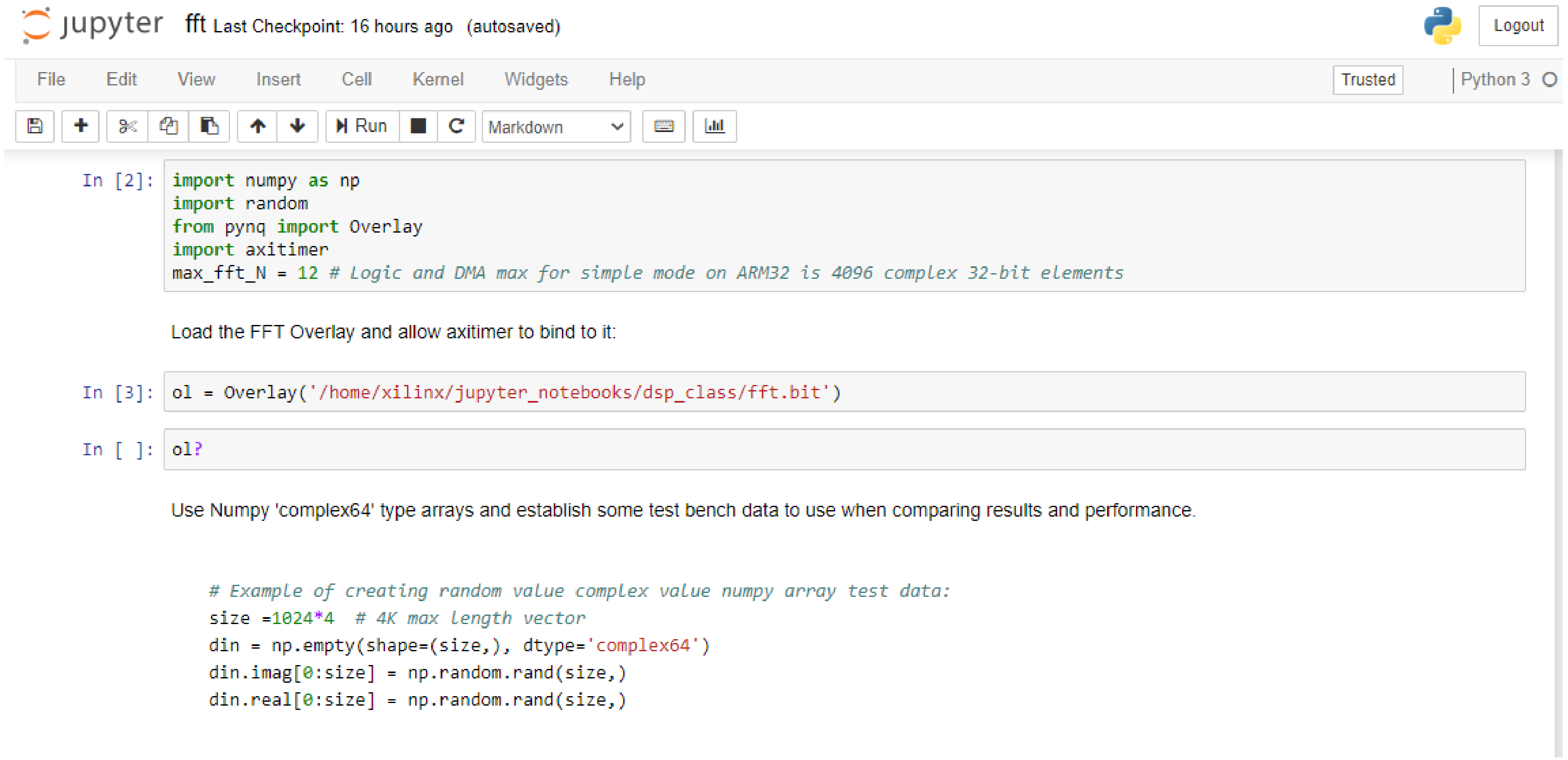
Run each cell in turn in the notebook and notice the difference in performance between SW and HW Implementations



In [2]:
```
import numpy as np
import random
from pynq import Overlay
import axitimer
max_fft_N = 12 # Logic and DMA max for simple mode on ARM32 is 4096 complex 32-bit elements
```

Load the FFT Overlay and allow axitimer to bind to it:

In [3]:
```
ol = Overlay('/home/xilinx/jupyter_notebooks/dsp_class/fft.bit')
```

In [ ]:
```
ol?
```

Use Numpy 'complex64' type arrays and establish some test bench data to use when comparing results and performance.

```
# Example of creating random value complex value numpy array test data:
size =1024*4  # 4K max length vector
din = np.empty(shape=(size,), dtype='complex64')
din.imag[0:size] = np.random.rand(size,)
din.real[0:size] = np.random.rand(size,)
```

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