Mastering MicroBlaze

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07/21/2022

Agenda

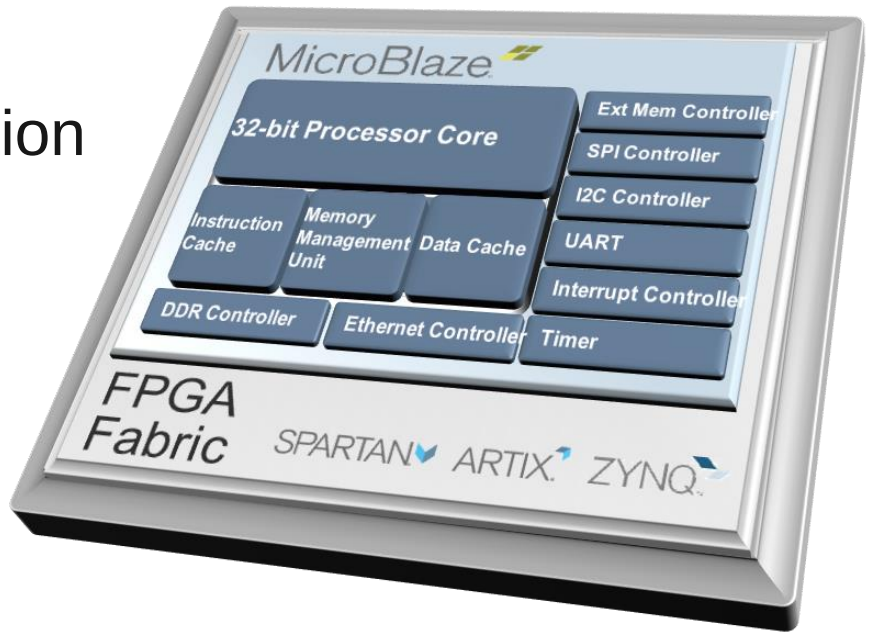
MicroBlaze Introduction

MicroBlaze Deployment

MicroBlaze Operating System and Communication

MicroBlaze Workshop

MicroBlaze Collateral



MicroBlaze Introduction

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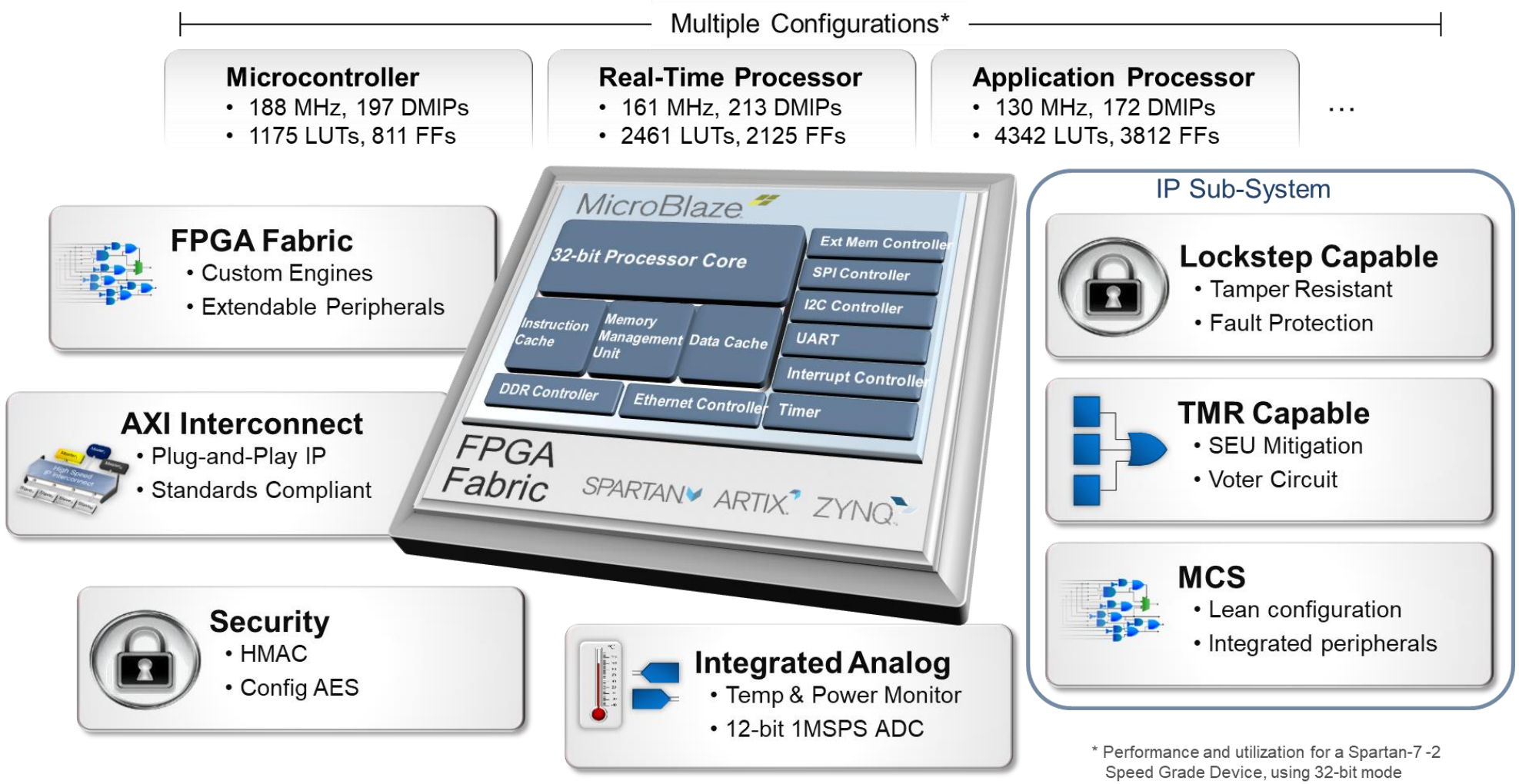
Sequential Processing in a Parallel World?

- Programmable logic is great for parallel signal/data processing high speed interfacing and rapid acceleration
- Not everything we do is in parallel world there is a need for sequential processing as in:
  - Communications
  - Human interfacing
  - Flow control

MicroBlaze Introduction

- MicroBlaze is a soft processor core designed for AMD-Xilinx FPGAs (field-programmable gate arrays).
- MicroBlaze enables more than 70 user-configured options.
  - Examples include:
    - Cache size
    - Pipeline depth
    - Memory management
    - Bus interfaces.
  - The configuration wizard, which takes the form of a GUI (graphical user interface), delivers instant feedback through a meter display on resource utilization and performance.

MicroBlaze turns any Xilinx FPGA into an Embedded System



* Performance and utilization for a Spartan-7 -2 Speed Grade Device, using 32-bit mode

MicroBlaze Operating Systems Support

Xilinx Supported OS

- OS Linux
  - Xilinx PetaLinux
- FreeRTOS
  - Vitis Integration
- Stand-alone BSP
  - Vitis Integration

3rd Party Supported OS

- ENEA OSE
- ExpressLogic X_WARE IoT platform powered by ThreadX
- Silicon Labs uC/OS

Embedded Processing on any Xilinx FPGA

MicroBlaze

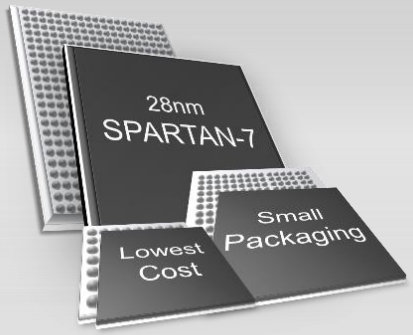
Fast soft-processor performance with the highest flexibility

Programmable Systems Integration	Works with any Xilinx FPGA, including new Versal ACAP. Highly configurable to fit almost any footprint requirement
Increased System Performance	>600 DMIPs performance in select FPGA devices
BOM Cost Reduction	MCS version packs more IP peripherals into a single package, reducing overall processing footprint
Total Power Reduction	Sleep and standby mode and instructions for low-power applications
Accelerated Design Productivity	Three pre-set configurations with seven additional templates, highly scalable across a wide range of applications

AMD-Xilinx Embedded Processing Portfolio

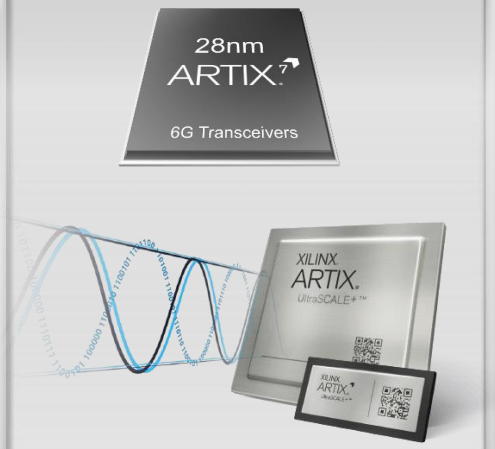
SPARTAN

I/O Optimized



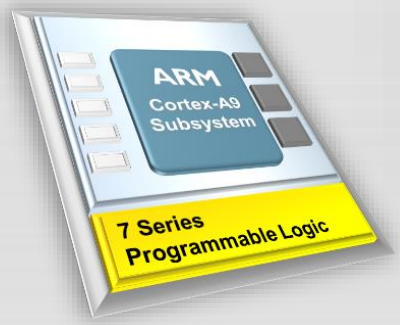
ARTIX

Transceiver Optimized



ZYNQ

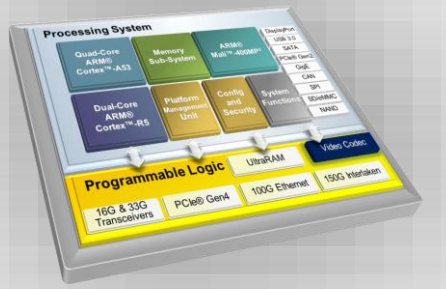
System Optimized



arm Cortex-A9

ZYNQ UltraSCALE+

Performance Optimized

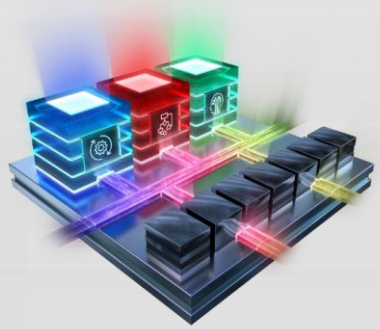


arm Cortex-A53

arm Cortex-R5F

VERSAL™

ACAP



arm Cortex-A72

arm Cortex-R5F

MicroBlaze

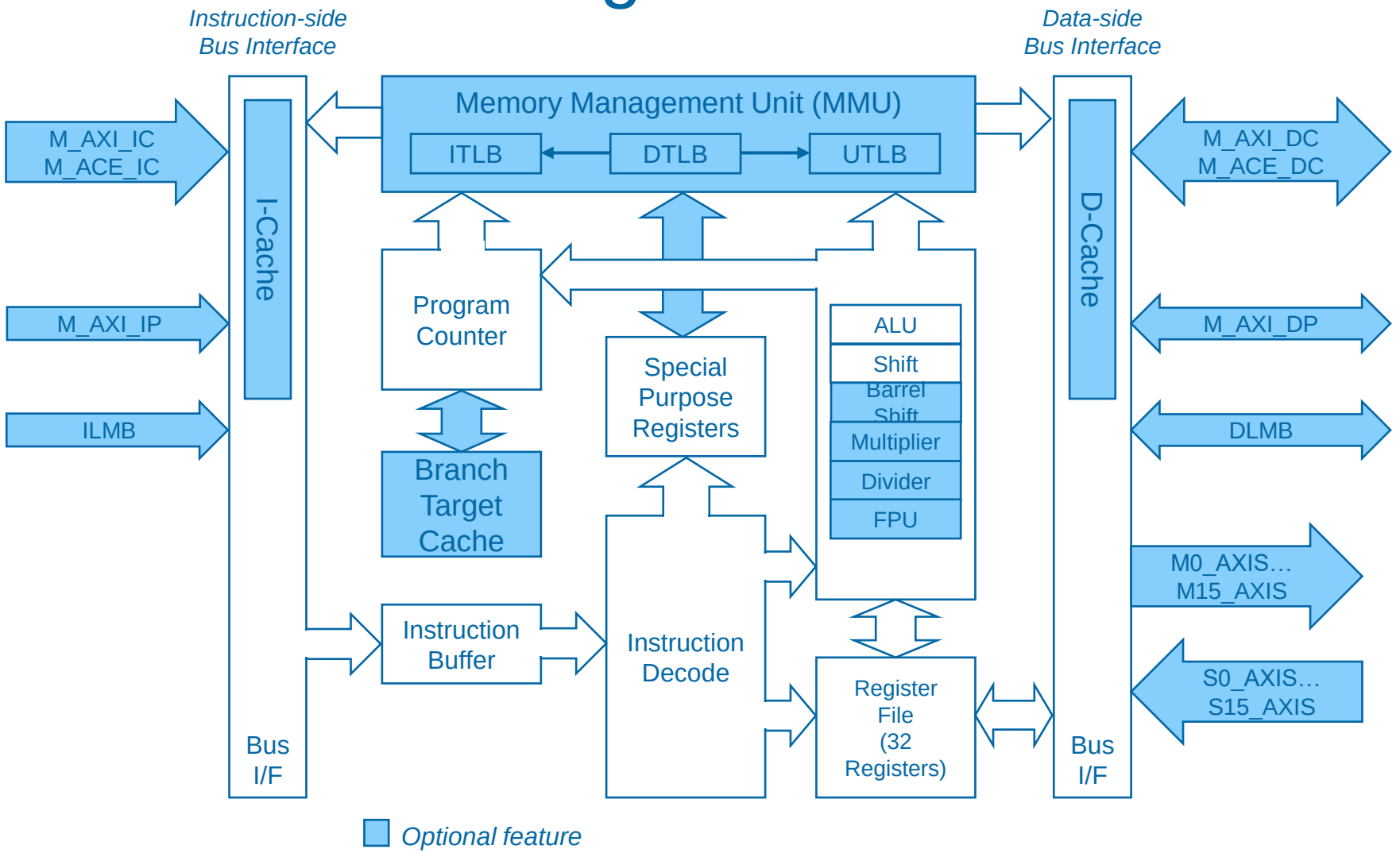
arm Cortex-M1/M3

Performance Benchmarks for FPGAs and SoCs

Device	Microcontroller (1.04 DMIPs/MHz)		Real-Time Processor (1.31 DMIPs/MHz)		Applications Processor (1.31 DMIPs/MHz)	
	Fmax	DMIPS	Fmax	DMIPS	Fmax	DMIPS
Cost-Optimized Portfolio Devices						
Spartan-7 (-2)	178	185	155	203	120	157
Artix-7 (-3)	204	212	172	225	146	191
Zynq 7000S (-2)	187	194	156	204	129	169
Zynq-7000 (-3)	212	220	171	224	141	185
FPGAs, 3D ICs, and MPSoCs						
Kintex-7 (-3)	298	310	228	299	204	267
Virtex-7 (-3)	300	312	238	312	208	272
Kintex UltraScale (-3)	393	409	280	367	242	317
Virtex UltraScale (-3)	384	399	283	371	245	321
Kintex UltraScale+ (-3)	518	539	384	503	345	452
Virtex UltraScale+ (-3)	505	525	396	519	327	428
Zynq UltraScale+ MPSoC (-3)	493	513	379	496	329	431

MicroBlaze Processor Block Diagram

- Full Harvard architecture
- 32-bit instruction word with three operands and two addressing modes
- 32-bit or 64-bit general purpose registers
- Default 32-bit address bus, extensible to 64 bits
- Single issue pipeline
- Majority of instructions execute in a single clock cycle



MicroBlaze is Optimized for Embedded Applications

Efficient Architecture

- Soft processor core based on 32-bit RISC Harvard architecture
- Instruction and Data-side Cache
- 3-stage pipeline – size optimized,
  5-stage pipeline – performance optimized,
  8-stage pipeline – frequency optimized

Flexible configurations

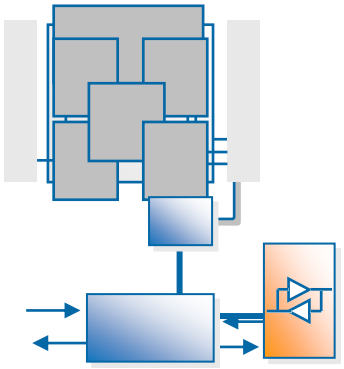
- Three selectable preset configurations with seven additional templates
- Optional Memory Management (MMU) and Floating Point Unit (FPU)
- Native AXI-4 interfaces and/or Local-Memory Bus (LMB)
- 32-bit or 64-bit implementation for maximum memory space utilization

Proven, widely adopted solution

- In production since 2001
- Comprehensive ecosystem of IP and development tools
- Works on any Xilinx FPGA (logic space permitting)

MicroBlaze fits a wide variety of Embedded Systems

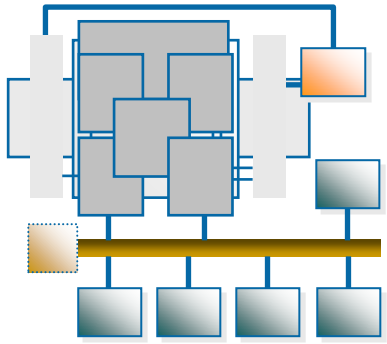
3-stage pipeline



State Machine

- Small footprint
- Few to no peripherals
- No OS
- Vast range of applications
- Baseline processing

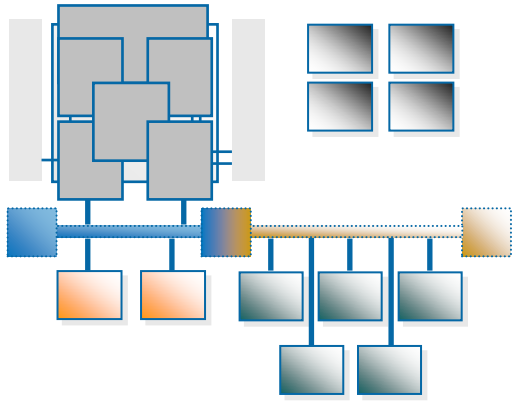
3/5-stage pipeline



Microcontroller

- Medium Footprint
- Moderate peripherals
- Small-footprint OS or standalone
- Performance targeted to Control, automation and instrumentation

5/8-stage pipeline



Custom Microprocessor

- Large Footprint
- Extensive Peripherals
- Linux-ready
- Networking & Wireless
- Highest Performance

MicroBlaze applications

The MicroBlaze processor meets the requirements of many diverse applications including:

- Industrial
- Medical
- Automotive
- Consumer
- Communications






MicroBlaze vs. Arm Cortex-M1/M3

- Arm and AMD-Xilinx have announced support for Arm Cortex-M1 and Cortex-M3 soft processors in Vivado.
- Cortex-M vs MicroBlaze:
  - Cortex-M1/M3:
    - Smaller code size using Thumb ISA
    - Excellent as state machines and smaller microcontrollers (good PicoBlaze replacement)
    - Not very many add-on modules (no MMU, FPU, debug IP…), and few configuration options
    - Fmax of approximately 100MHz maximum
  - MicroBlaze:
    - Larger code size
    - Highly flexible, highly configurable with multiple preset templates
    - Optional MMU, FPU, debug module, etc…
    - Excellent Fmax (almost 600MHz on select devices)

MicroBlaze Deployment

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MicroBlaze Memory Hierarchy

- Local Memory
  - Tightly coupled memory with a very low access latency through a dedicated interface
- AXI Block RAM
  - If local memory is insufficient, or shared memory is required, block RAM connected through an AXI interface
- External Memory
  - External memory is usually either RAM (DDR, SRAM) or some form of non-volatile memory such as QSPI NOR
- Shared Memory
  - With the AXI block RAM or external DDR a common interconnect must be used with other DMA masters, otherwise they won’t be accessible to those masters.

MicroBlaze Interfaces

MicroBlaze can be configured with the following bus interfaces:-

- The AMBA® AXI4 interface (AXI4)
  - The AXI4 interfaces provide a fast non-arbitrated streaming communication mechanism through a connection to both on-chip and off-chip peripheral interfaces and memory.
  - MicroBlaze also supports up to 16 AXI4-Stream interface ports, each with one master and one slave interface.
- ACE interface (ACE).
  - The AMBA AXI4 or AXI Coherency Extension (ACE) Interface provide cache coherent connections to memory.
- Lockstep Interface
  - The lockstep interface is designed to connect a master and one or more slave MicroBlaze instances

MicroBlaze Interfaces

- Debug interface
  - Debug interface to access debug registers, used with the Microprocessor Debug Module (MDM) core which enables JTAG-based debugging of one or more MicroBlaze processors.
- Trace interface
  - Trace interface for performance analysis to funnel and store MicroBlaze program trace in external storage. Program trace from connected MicroBlaze processors can be directly output on an external interface, stored in external memory via the AXI4 master port, or transmitted on an AXI4-Stream interface.

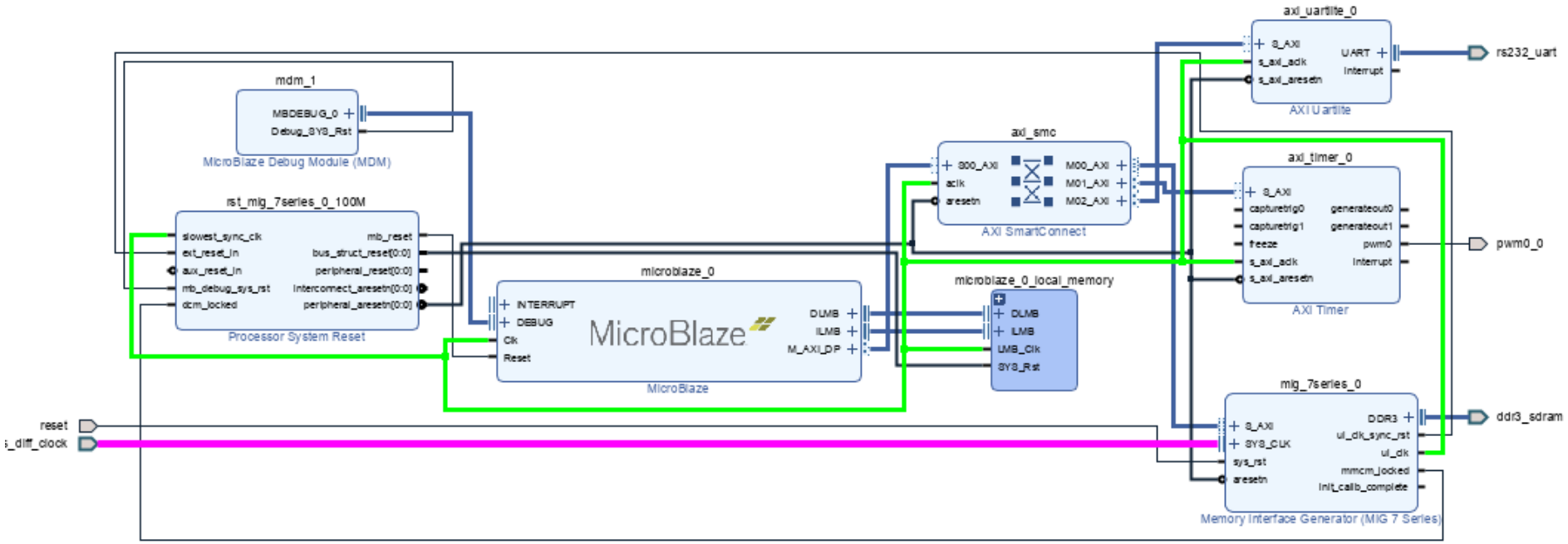
MicroBlaze Interfaces

- Local Memory Bus (LMB)
  - The LMB provides a simple synchronous protocol through a single-cycle access to on-chip dual-port block RAM for efficient block RAM transfers.
  - DLMB – both go to the memory BRAM --
  - ILMB
  - One connected to ddr EXTERNAL CHIP outside the processor
  - BRAM is smaller than DDR
- Instruction Cache
  - MicroBlaze can be used with an optional instruction cache for improved performance when executing code that resides outside the LMB address range.
  - The cache can be implemented in the DDR.
- Data Cache
  - The MicroBlaze processor can be used with an optional data cache for improved performance. The cached memory range must not include addresses in the LMB address range.
- Clock and Reset Interface

MicroBlaze Clocking & Interrupts

Clock MicroBlaze is very simple

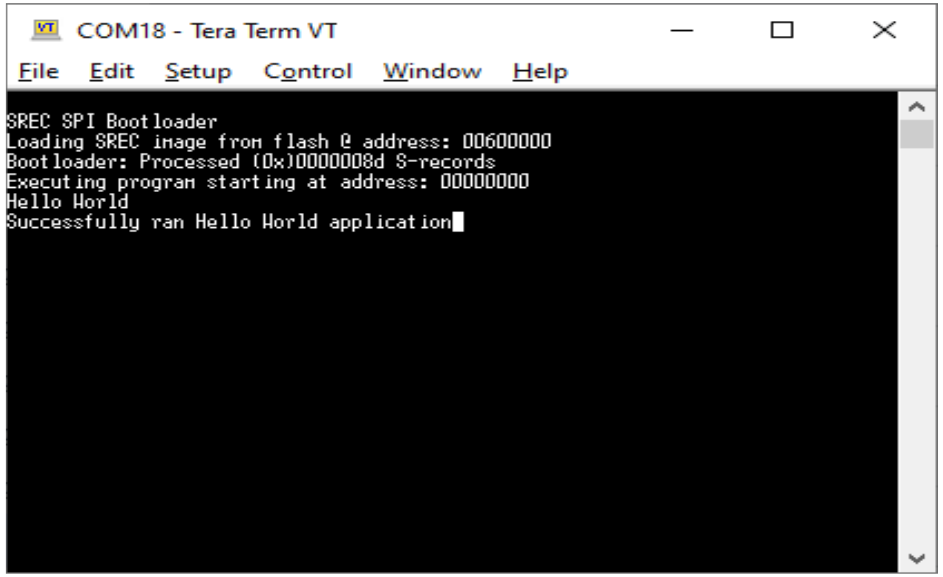
- Single clock - Max frequency depends on the Fabric and Configuration
- If using DDR / MIG clock MB from the User Interface Clock.
- MicroBlaze does provides exceptions and interrupt handling



Build and Configuration

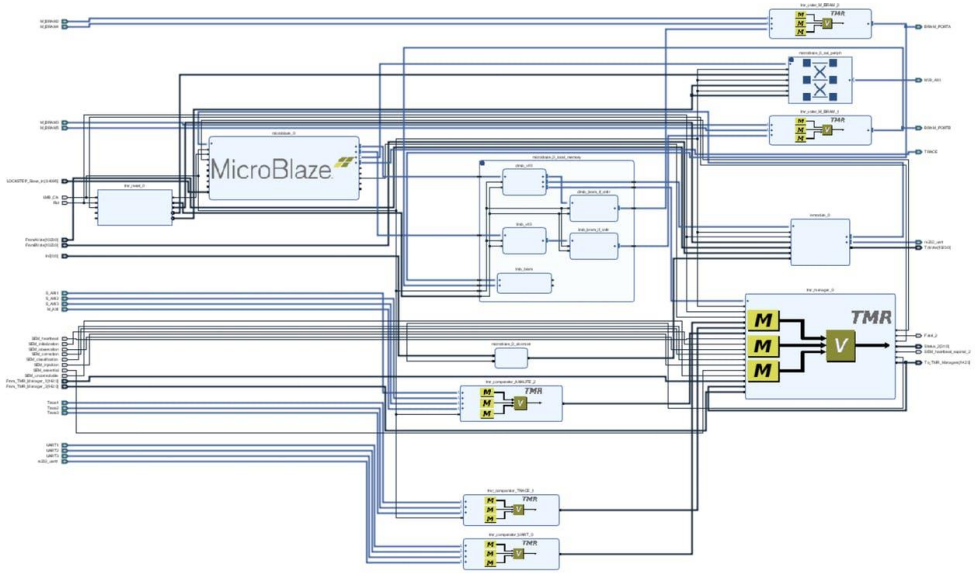
Configuration of the MicroBlaze can occur in several methods

1. Small application running from BRAM – ELF can be merged with the bitstream and on boot the application will start running.
2. Large application running from DDR – more complex. Application needs to be stored in QSPI, bootloader is created and merged FPGA bit stream. On boot the, bootloader cross loads the MicroBlaze from the QSPI to DDR.



MicroBlaze Safety and Security

- MicroBlaze can be implemented in lockstep or TMR solutions for higher reliability applications.
- Capable of graceful degradation
- Security critical solutions can leverage XADC / System Monitor to monitor device parameters and temperature
  - Small application running from internal block RAM for maximum security



MicroBlaze Microcontroller System (MCS)

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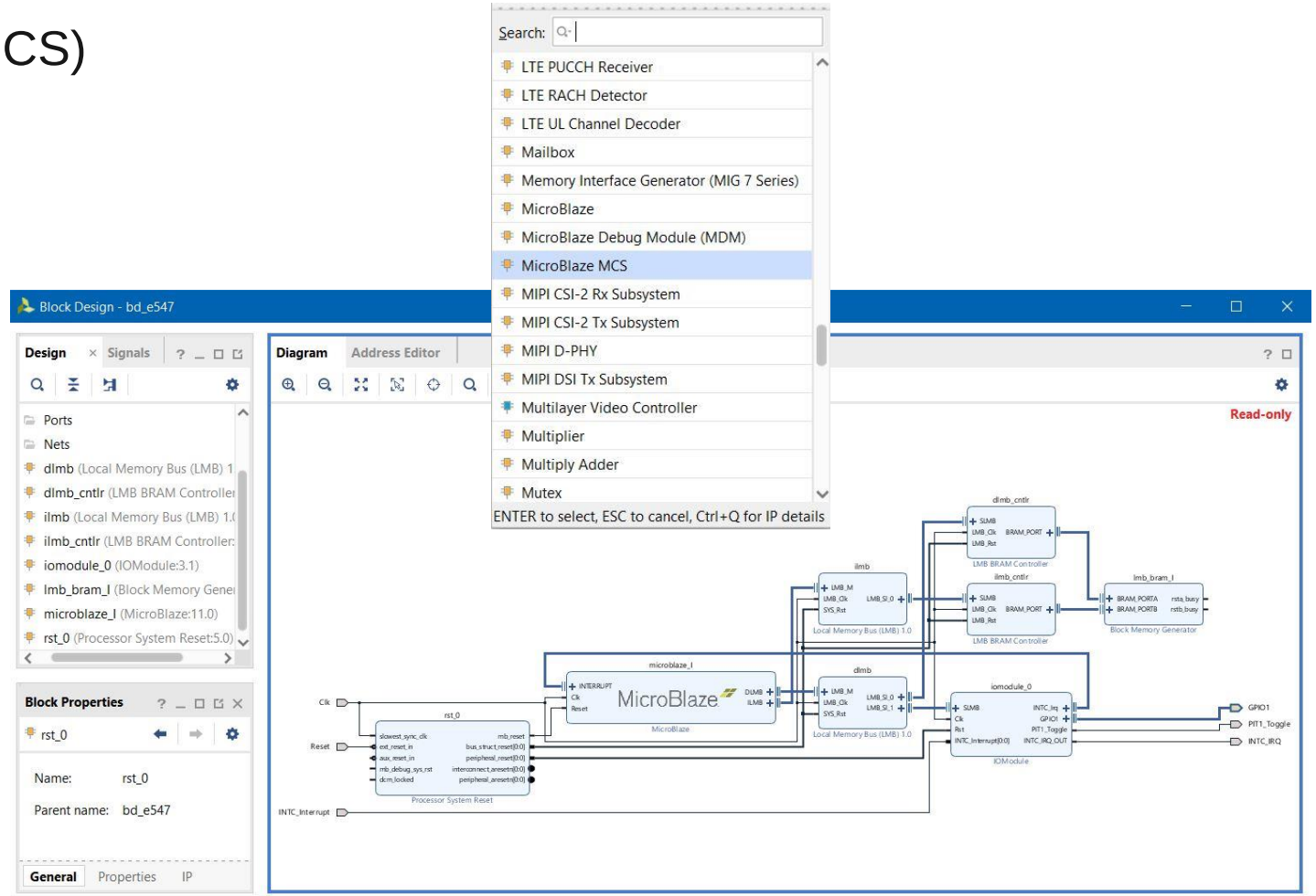
MicroBlaze Microcontroller System (MCS)

MicroBlaze Microcontroller System (MCS)

- The same MicroBlaze IP with fewer configuration options
- Peripherals in a single IO Module and configuration wizard
- Available in all editions of Vivado
- Generates a MicroBlaze-based block design with connected peripherals
- Same MicroBlaze performance
- Usable on any Xilinx device *(as long as programmable logic is available)*
- Ideal for small microcontroller applications
- Ideal for users new to MicroBlaze or processor design



MicroBlaze MCS include

MicroBlaze, pre-configured for 3-stage pipeline mode (area optimized)

- With 5-stage pipeline option

Local Memory Support (4 – 128kB)

IO Module Peripherals:

- MicroBlaze Debug Module (MDM)
- UART
- Interrupt Controller, with 16 external interrupts
- Up to 4 Programmable Interval Timer (PIT)
- Up to 4 Fixed Interval Timers (FIT)
- 4 x 32-bit General Purpose Output (GPO)
- 4 x 32-bit General Purpose Input (GPI)
- Simple IO Bus (compatible with Xilinx Dynamic Reconfiguration Port)

MicroBlaze MCS does not include

Does not include data port (DAXI) for external memory access

Does not include AXI streaming data ports

Does not include AXI interface connections

Does not include Ethernet, SPI, or I2C

Does not support full MicroBlaze configuration options

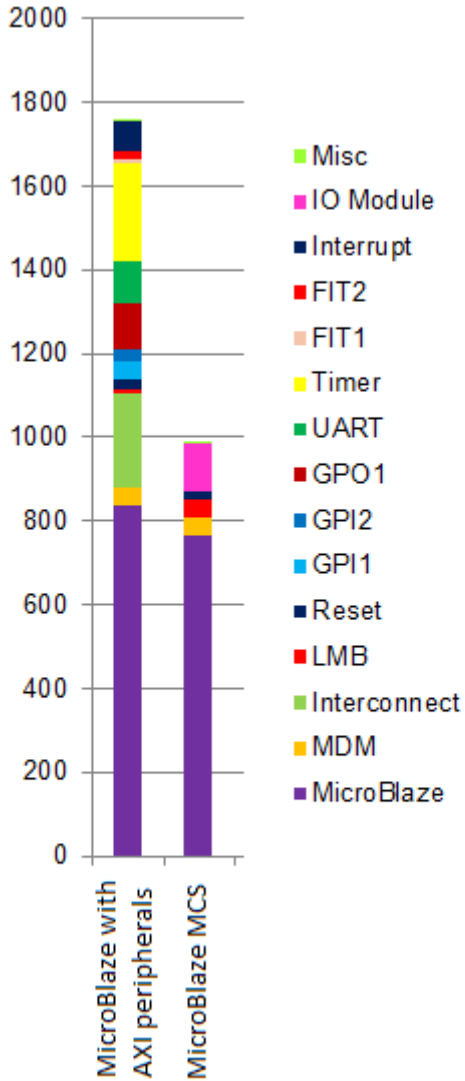
If you need these options, use the full MicroBlaze IP, not MCS

Same MicroBlaze performance, Smaller overall footprint

Same Fmax as MicroBlaze system

Tightly coupled IO Module makes MicroBlaze MCS smaller

- One 32-bit Programmable Interval Timer(PIT),
- Two Fixed Interval Timer (FIT), 500,000 and 216 periods
- Three GPI, 3,4 and 4 bits wide
- Two GPO, 8 and 11 bits wide
- One UART fixed baud rate, no fifo
- Interrupt controller with UART, PIT and one FIT interrupt
- 8 Kbytes of internal memory



MicroBlaze Debug Module

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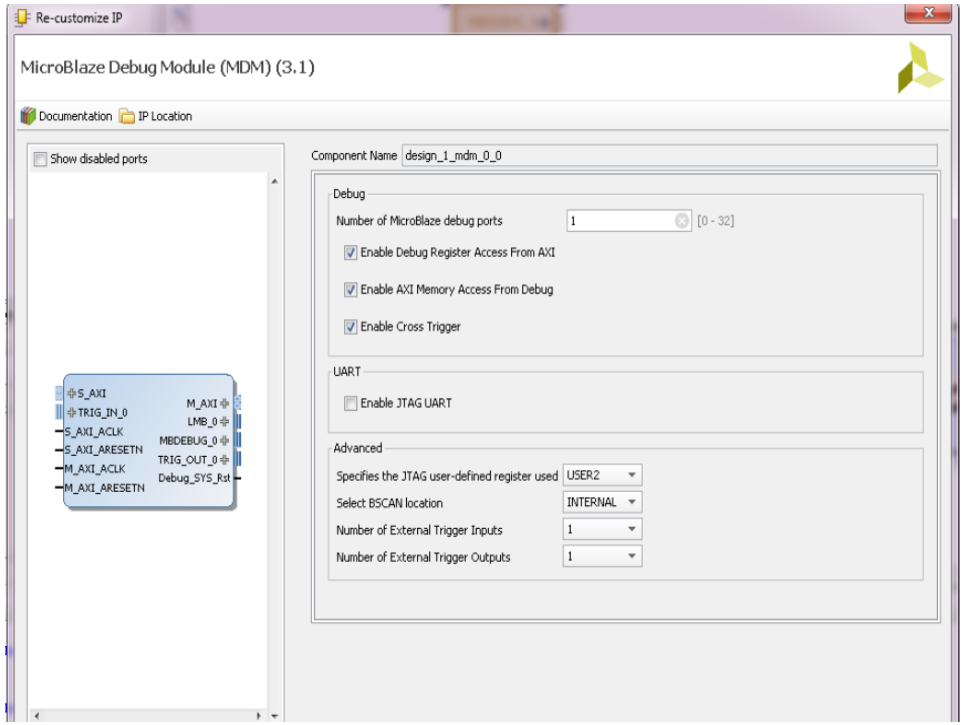
MicroBlaze Debug Module

- Enables JTAG-based debugging of one or more MicroBlaze processors
- Debug up to 32 MicroBlaze processors
- Synchronized control of multiple MicroBlaze processors
- JTAG-based UART with a configurable AXI4-Lite interface
- Based on Boundary Scan (BSCAN) logic in Xilinx FPGAs
- Direct JTAG-based access to memory with a configurable AXI4 master interface



MicroBlaze Debug Module Configuration

Number of MicroBlaze debug ports - Sets the number of ports available to connect to MicroBlaze processors.

Enable JTAG UART - Enables the JTAG UART and the AXI4-Lite interconnect to access the UART registers

Specify the JTAG user-defined register used - Select JTAG user-defined register. Can be set to *USER1*, *USER2*, *USER3* or *USER4*. Should never need to be changed from *USER2*, unless there is a conflict with another IP core in the system.

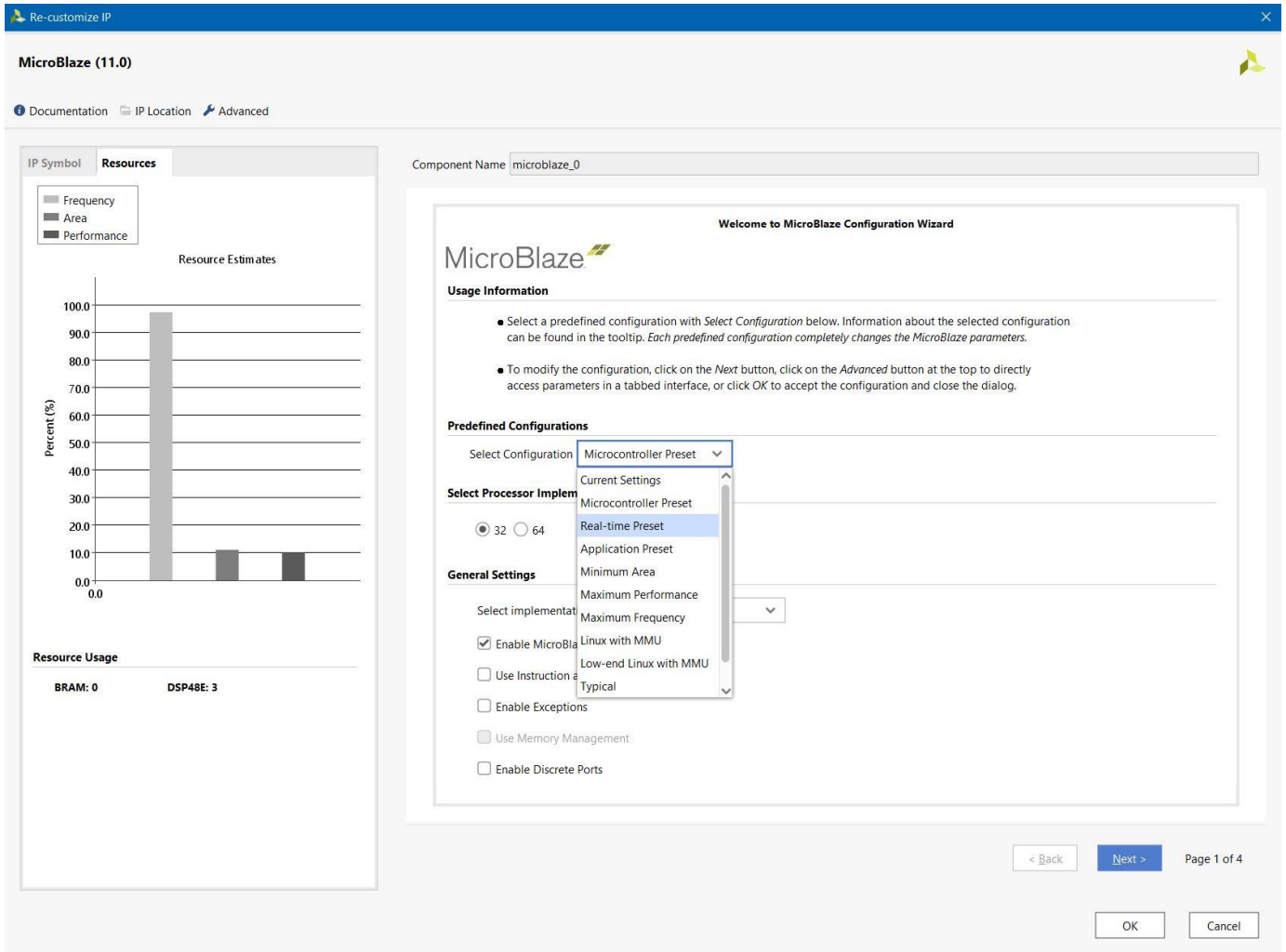
Select BSCAN location - Selects whether internal or external BSCAN is used. Should never need to be changed from *INTERNAL* in an embedded system.

MicroBlaze Configurations

Three Selectable Preset Configurations
- Microcontroller
- Real-Time
- Application

Seven additional Templates
- Minimum Area
- Maximum Performance
- Maximum Frequency
- Linux with MMU
- Low-End Linux with MMU
- Typical
- Frequency Optimized

With Performance, Area, Frequency optimization
- Depending on configuration



IP Sub system

Lockstep Capable

- Tamper Resistant
- Fault Protection

The Microblaze soft processor is Lock-step capable– This is an additional unique value that can be configured in a lock-step configuration in any of the previous profiles, with hardware infrastructure to offer runtime monitoring of the integrity of code execution across each processor.

TMR Capable

- SEU Mitigation
- Voter Circuit

Triple Module Redundancy (**TMR**) technology was developed for SEU mitigation.

MicroBlaze OS and Communication

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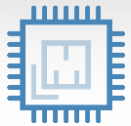
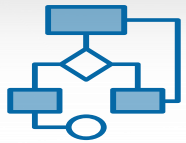
Operating systems and Configurations



Microcontroller
200 MHz, 1.1 DMIPS/MHz
Logic Cells: 1,900

Real-Time Processor
160 MHz, 1.3 DMIPS/MHz
Logic Cells: 4,000



Application Processor
120 MHz, 1.4 DMIPS/MHz
Logic Cells: 7,000

Microcontroller profile at 200MHz offering 1.1 DMIPS/MHz, typically running from external memory with a number of low performance peripherals. This configuration is comparable to the Arm® Cortex®-M0/M1 processors, which typically run at 40-50MHz.

Real-Time profile processor with **RTOS** support for systems needing deterministic response and performance offering 1.3 DMIPS/MHz. The configuration includes a memory protection unit, scalable instruction cache and data cash, and soft DDR controller. This profile is comparable to Arm Cortex-M3/M4 processors.

Application Processor profile offering 1.4 DMIPS/MHz supports embedded **Linux** and includes a memory management unit and Ethernet controller– since they're common in Linux systems. This is comparable to Arm Cortex-A5 processors.

Libraries and APIs

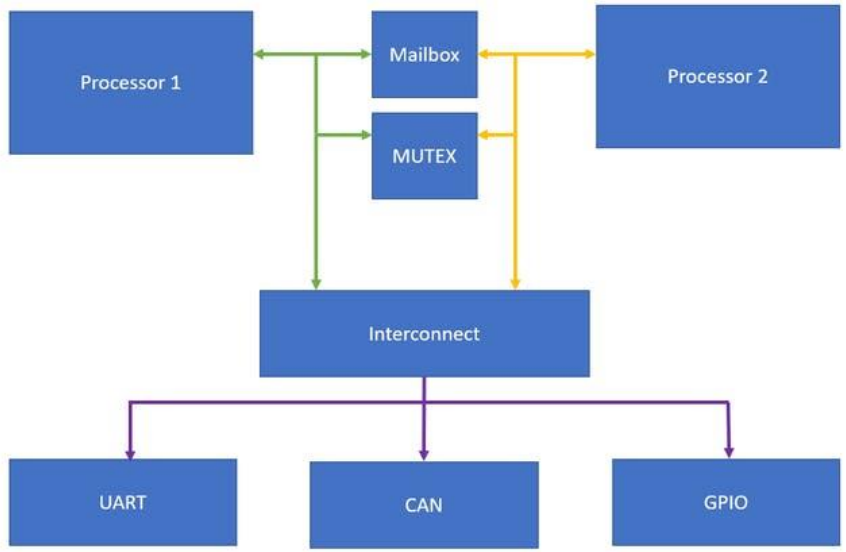
MicroBlaze Libraries:

- wip – Network TCP/IP stack
- xilisf – Serial Flash
- standalone BSP – Board support package
- xilffs – FAT File System
- xilfpga – PL/FPGA management (bitstream loading)
- xilskey – Security Key management
- xilsecure – Security
- xilrsa – Security RSA Authentication

MicroBlaze Communications

Multi Processor Communications needs care to ensure safe communication and resources are shared.

- Mailbox — Allows bi-directional communication between multiple processors using a FIFO based approacl to messaging.
- Mutex — Implement mutual exclusion locks, this allows processors to lock shared resources preventing multiple accesses at the same time.

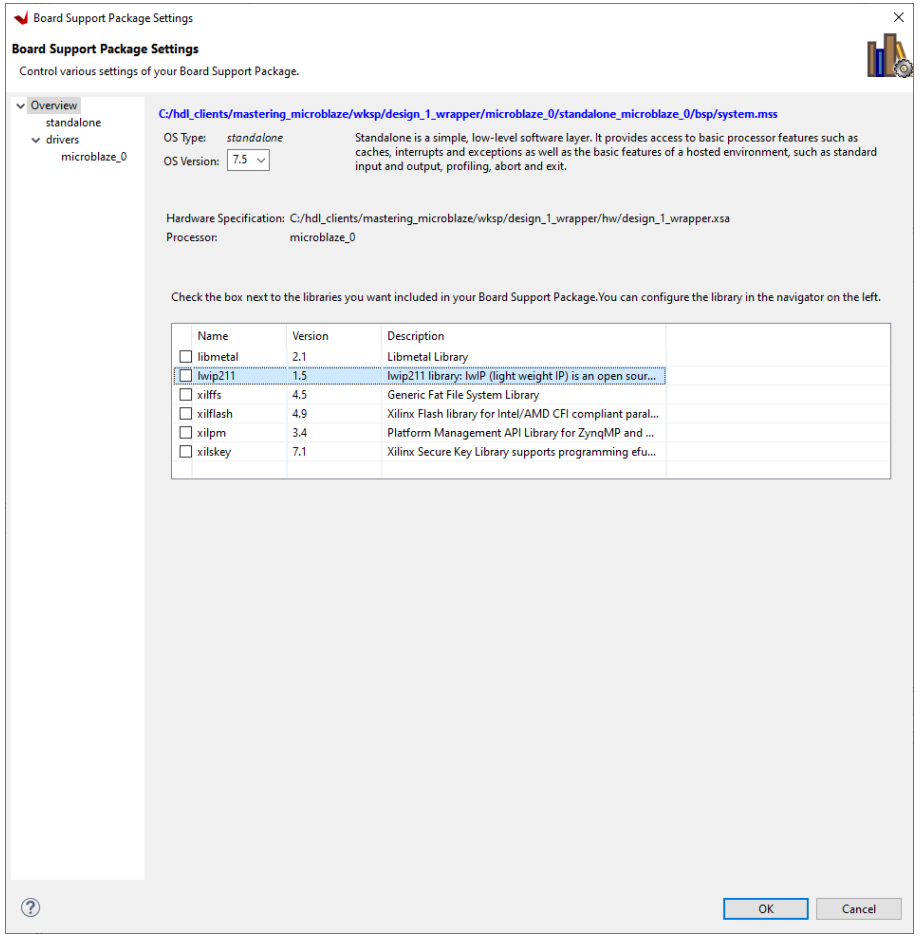


MicroBlaze External Communications

Role of MicroBlaze is often to handle external communications. This could be via simple interfaces e.g. UART or via more complex interfaces e.g. Ethernet.

To support more complex interfaces such as Ethernet, Xilinx Vitis provides support for Lightweight IP Stack.

Additional interfaces such as CAN, I2C, SPI etc are provided as IP with drivers and examples.



Tool and Ecosystem Support

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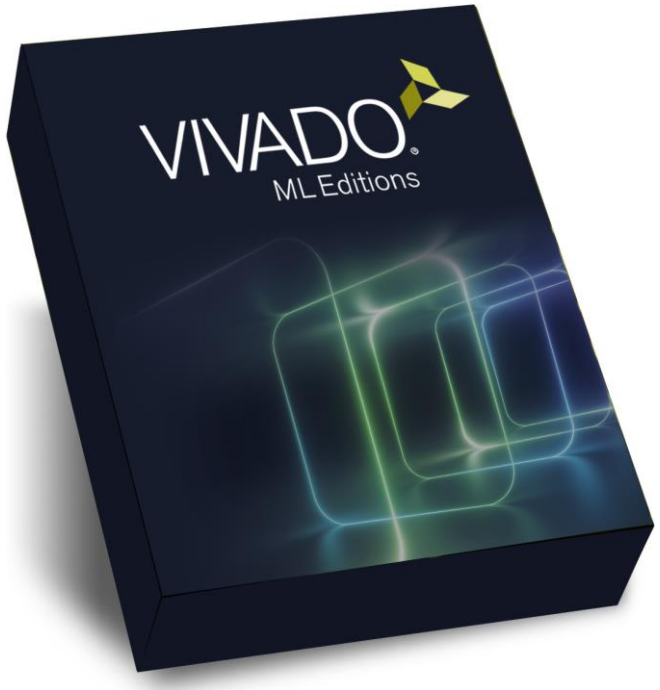
Design Tools for MicroBlaze

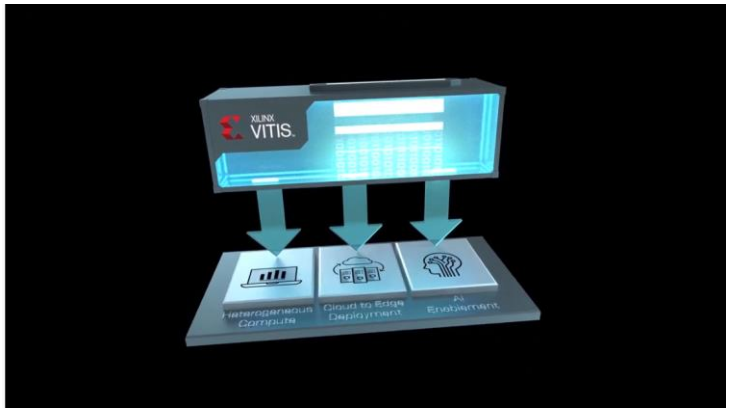
MicroBlaze works with all versions of Vivado ML

- No charge, no licensing, no royalties
- Extensive configuration wizard with built-in templates
- Configurable example designs
- MicroBlaze, MicroBlaze MCS, and MDM are built into all Vivado Design Suites, including Vivado ML

MicroBlaze works with Vitis Unified Software Platform

- Debug using Breakpoints, Watchpoints, XSCT, hardware-server, halt and resume, register updates…
- Single or multiple MicroBlaze instantiations
- FPGA soft-processor
  - On any Xilinx FPGA
- MicroBlaze co-processing alongside Arm
  - Heterogenous Debug and Development
  - Zynq-7000, Zynq UltraScale+, and Versal





MicroBlaze Workshop

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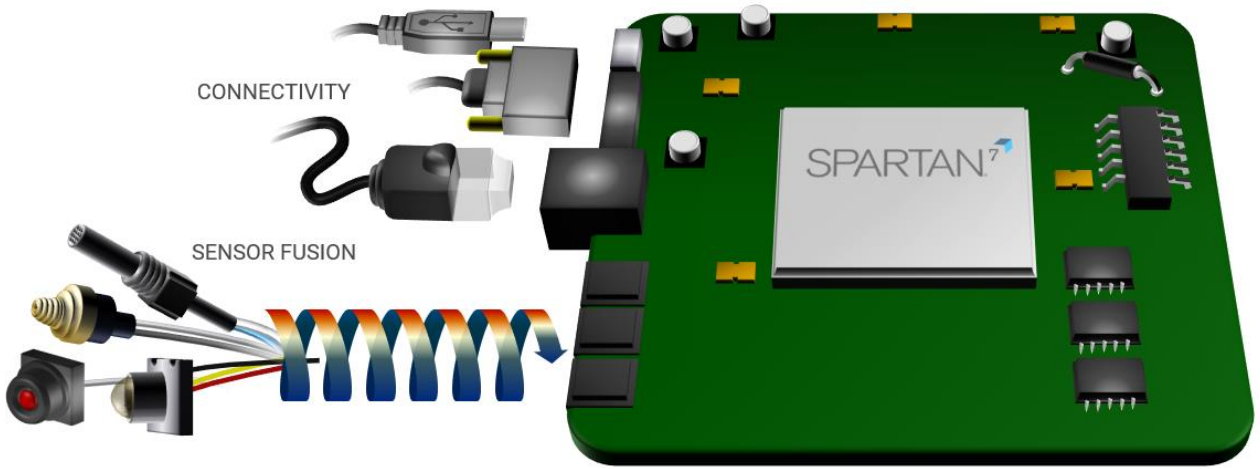
Demonstration Time!

Bare Metal application with MicroBlaze

- Create Project **Vivado ML**
- Target SP701 Evaluation Kit
- Build MicroBlaze Design
- Synthesize and implement
- Pin allocation
- Export to **Vitis**
- Create a basic application that interact with SP701 peripherals
- Power on board and set UART communication
- Download application



Both demonstrations available **On-Demand** to follow along later

Demonstrations use Software Release 2022.1

MicroBlaze Collateral

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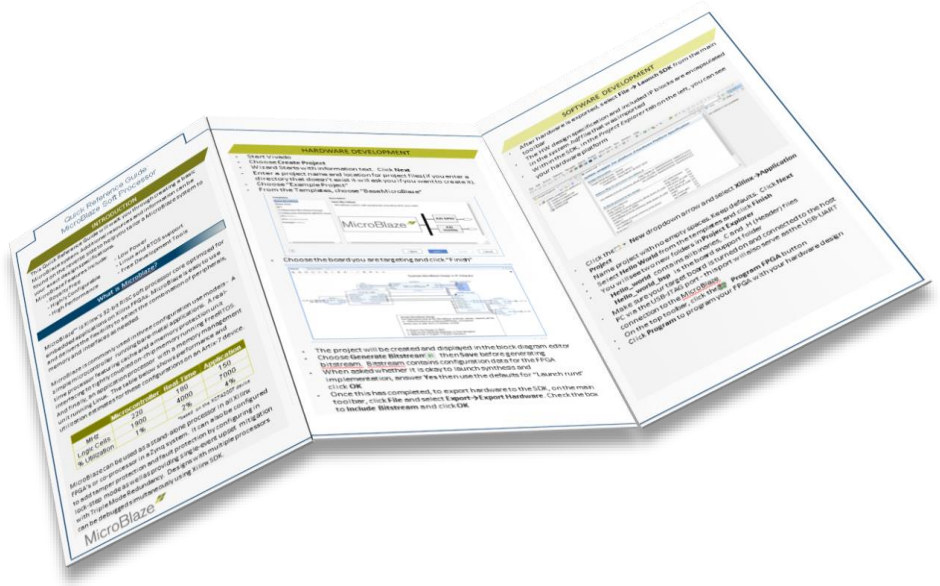
MicroBlaze™ Quick Start Guide – Start Programming in Minutes



MicroBlaze

HARDWARE DEVELOPMENT in VIVADO ML

- **Step-by-step wizard** for target board
- Instantiate MicroBlaze design from templates
- Compile design and export to **Vitis**

SOFTWARE DEVELOPMENT in VITIS

- **Launch Vitis** from Vivado
- Launch “Hello World” from template
- Connect USB-JTAG port and **program board**

FAQ and ADDITIONAL RESOURCES

- Common questions on OS support, debug, etc.
- Links to wiki, reference guides, more tutorials
- Links to other supported boards and partners

Available at: www.xilinx.com/microblaze

Opal Kelly Development Platform Available Now

Featuring the Artix® UltraScale+™ AU25P device

Versatile platform for multiple markets

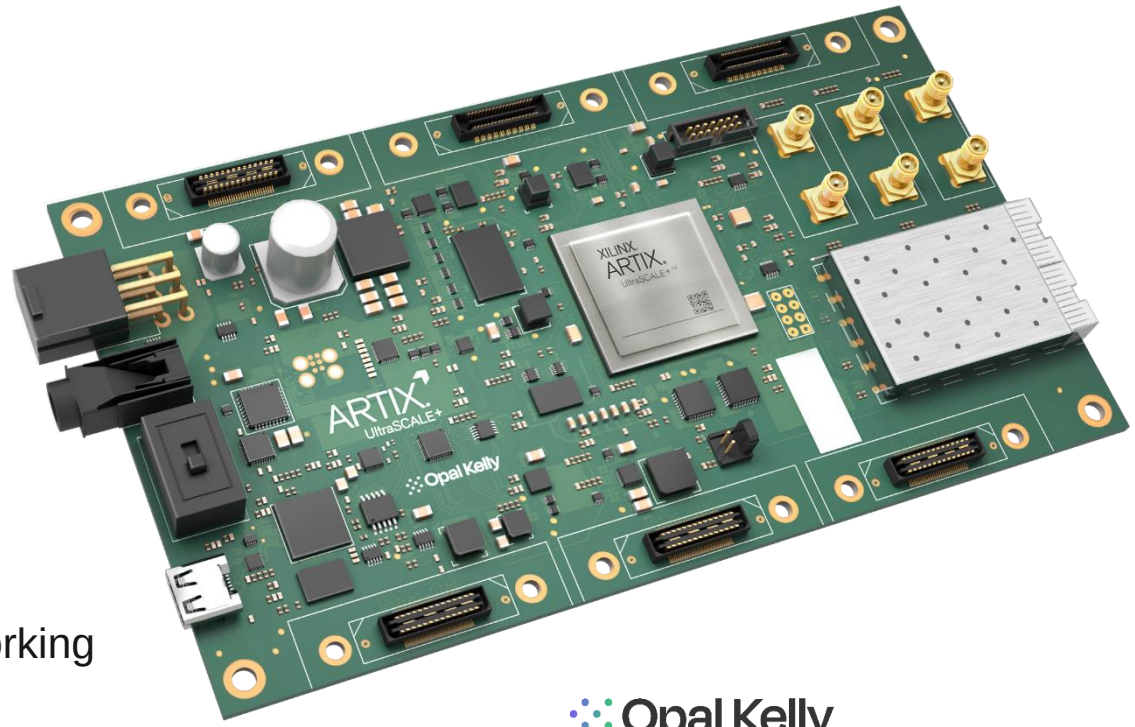
- AU25P production device (largest in portfolio)
- 1GiB DDR4-2666 memory, 32MiB QSPI Flash
- Superspeed USB 3.0 host interface
- Ideal for capturing and processing large data streams

FrontPanel SDK for SW/HW integration

- Stand-alone desktop app or API for custom integration
- Ideal for prototyping, proof-of-concept, and production
- Included with XEM8320 (no additional charge)

SYZYGY modular connectivity

- Compact connectors for data acquisition, sensing, networking
- 4 SYZYGY standard ports
- 2 SYZYGY transceiver ports



Opal Kelly

$1,349.95

Product Page

Avnet Development Board Available Q4’22

Featuring the Zynq® UltraScale+™ ZU1CG device

Based on ZU1CG, the newest Zynq® UltraScale+™ device

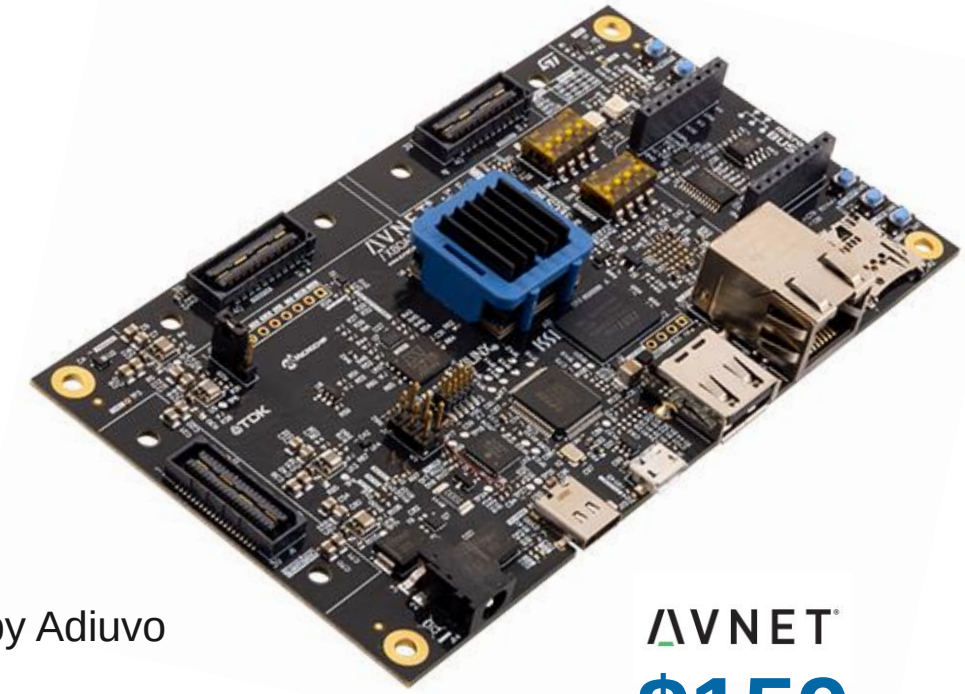
- Targets XCZU1CG-1SBVA484E device
- Ideal for entry level development activities
- One Click and three SYZYGY expansion ports

Target applications

- Artificial Intelligence / Machine Learning
- Embedded processing
- Robotics

Availability and training

- Available for pre-orders
- Free 3-day online technical training in Q4’22 – Developed by Adiuvo



AVNET

$159

Product Page

Summary

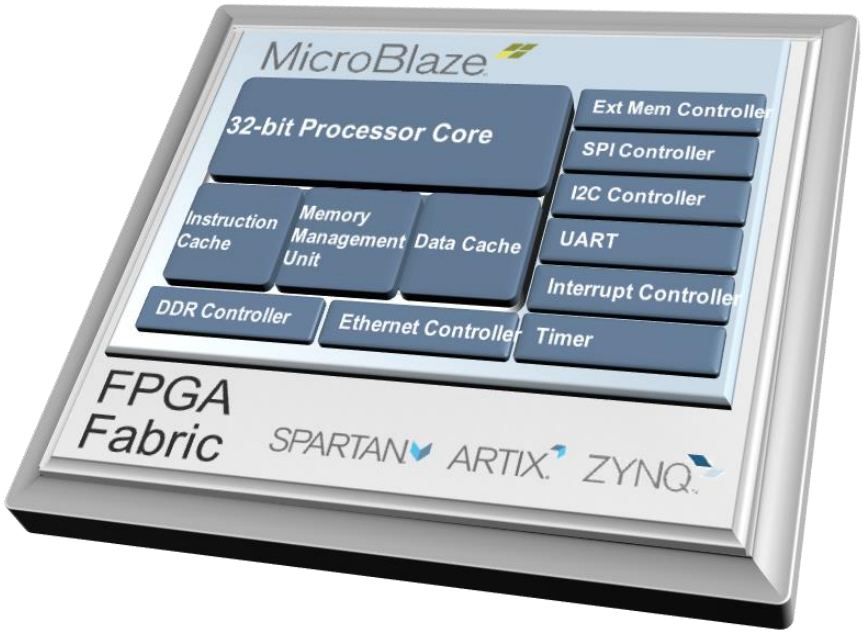
Xilinx provides industry leading 32-Bit and 64-bit soft-processor MicroBlaze

MicroBlaze MCS is light-weight, general purpose MicroBlaze-based sub-system suitable for ISM, DSP, Automotive segments and applications

MicroBlaze Debug Module provides JTAG based debugging option for MicroBlaze

Full ecosystem support for MicroBlaze in hardware and software tools

MicroBlaze



Next Steps and Q&A

- Follow Adiuvo Weekly blogs and projects
  - » Visit https://www.adiuvoengineering.com
- Access more information about MicroBlaze
  - » Visit www.xilinx.com/products/microblaze
- Buy an evaluation kit
  - » Opal Kelly XEM8320: https://opalkelly.com/products/xem8320/
  - » Avnet ZUBoard 1CG: https://www.avnet.com/wps/portal/us/products/avnet-boards/avnet-board-families/zuboard-1cg/
- Download tools
  - » Xilinx Vivado® ML/Vitis™ Tools: www.xilinx.com/downloads
- Learn more about device pricing and availability
  - » Contact your local sales representative

Ask Your Questions in the Chat Window Now

Thank You!

AMD XILINX

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