Mastering MicroBlaze™ Processor

Adam Taylor – Founder and Principal Consultant | Adiuvo Eng.

Romisaa Samhoud – Product Line Manger | AMD Inc.

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Agenda

- MicroBlaze™ Processor Introduction
- MicroBlaze Processor Deployment
- MicroBlaze Processor Operating System and Communication
- MicroBlaze Processor Workshop
- MicroBlaze Processor Collateral

MicroBlaze™ Processor Introduction

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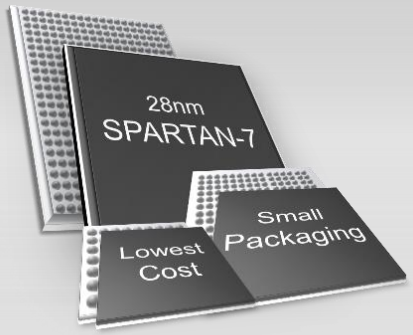
Sequential Processing in a Parallel World?

- Programmable logic is great for parallel signal/data processing, high speed interfacing and rapid acceleration
- Not everything we do is in parallel world; there is a need for sequential processing as in:
  - Communications
  - Human interfacing
  - Flow control

AMD-Xilinx Embedded Processing Portfolio

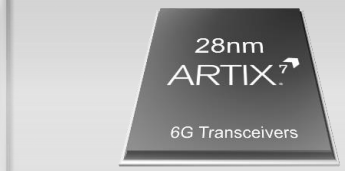
SPARTAN

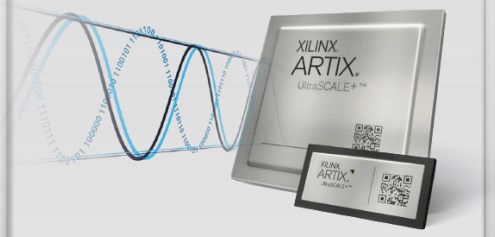
I/O Optimized



ARTIX

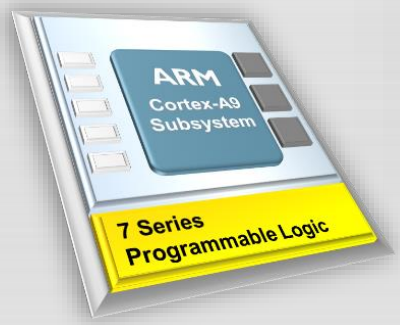
Transceiver Optimized





ZYNQ

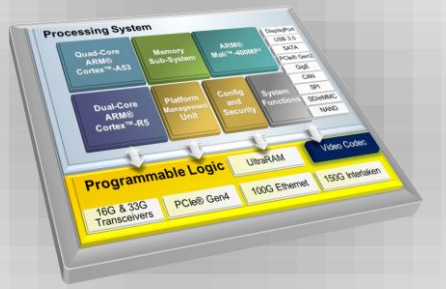
System Optimized



arm Cortex-A9

ZYNQ UltraSCALE+

Performance Optimized

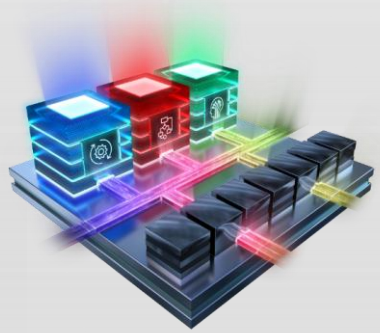


arm Cortex-A53

arm Cortex-R5F

VERSAL

ACAP



arm Cortex-A72

arm Cortex-R5F

MicroBlaze

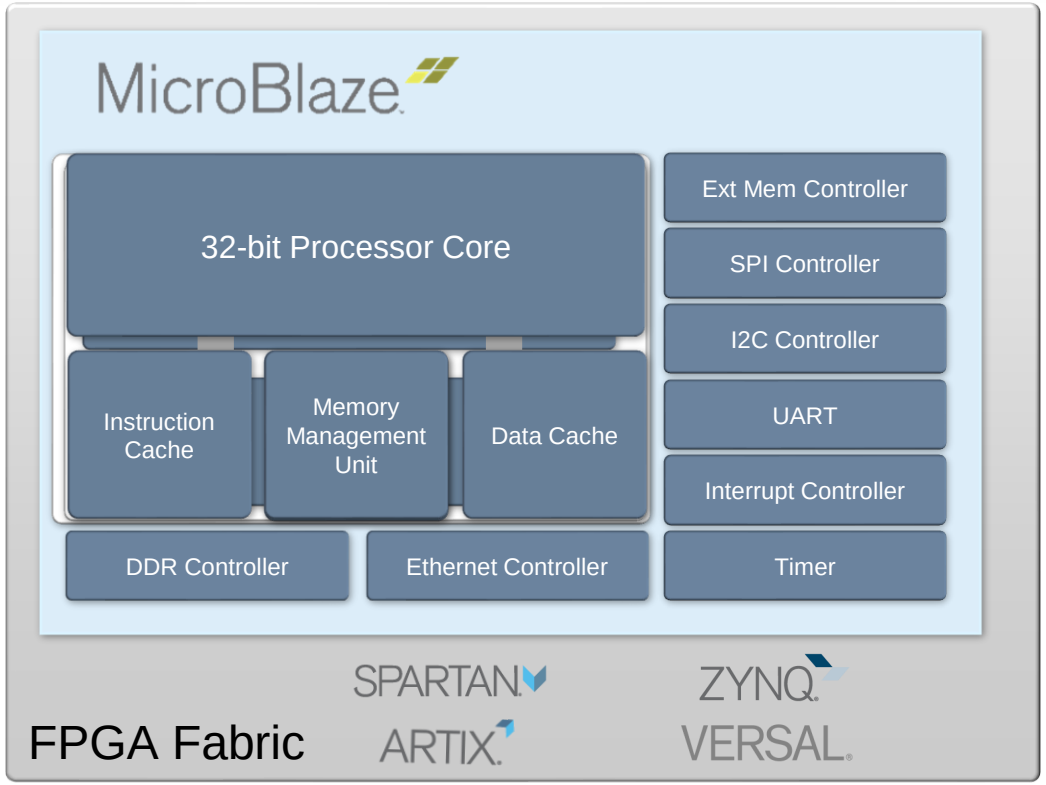
arm Cortex-M1/M3

MicroBlaze™ Processor Based Embedded System

Microcontroller	Real-Time Processor	Application Processor
1.1 DMIPS/MHz	1.3 DMIPS/MHz	1.4 DMIPS/MHz
Logic Cells: 1,900	Logic Cells: 4,000	Logic Cells: 7,000

Lockstep Capable
- Tamper Resistant
- Fault Protection

TMR Capable
- SEU Mitigation
- Voter Circuit



License free RISC processor with an extensive IP catalog of peripherals

MicroBlaze™ Processor Software Solutions

Xilinx Supported OS

- OS Linux
  - AMD-Xilinx PetaLinux
- FreeRTOS
  - Vitis™ Tools Integration
- Stand-alone Bare Metal
  - Vitis Tools Integration

3rd Party Supported OS

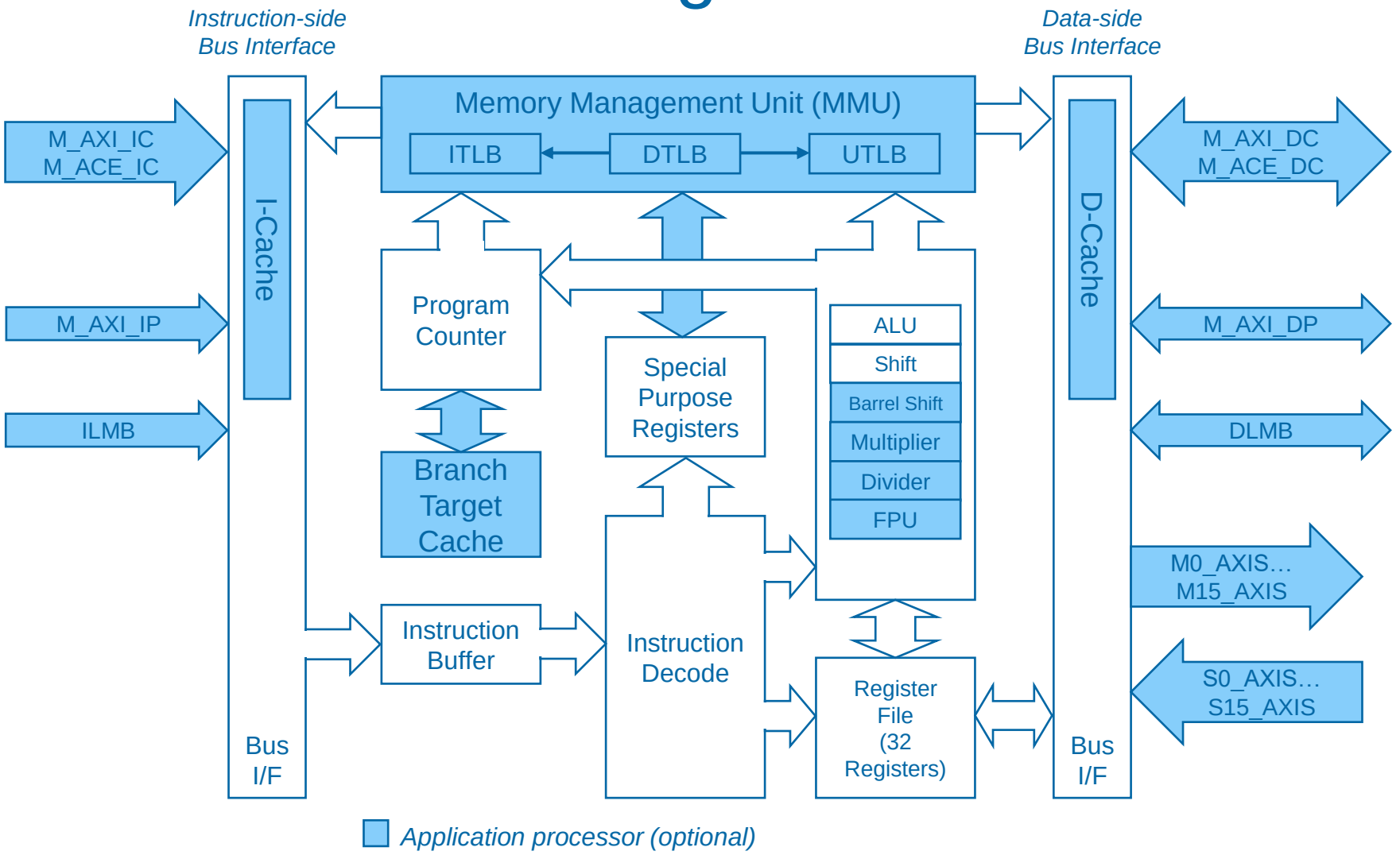
- ENEA OSE
- ExpressLogic X_WARE IoT platform powered by ThreadX
- Silicon Labs uC/OS

Performance Benchmarks for FPGAs and SoCs

Device	Microcontroller (1.1 DMIPs/MHz)		Real-Time Processor (1.3 DMIPs/MHz)		Applications Processor (1.4 DMIPs/MHz)	
	Fmax	DMIPS	Fmax	DMIPS	Fmax	DMIPS
Cost-Optimized Portfolio Devices						
Spartan®-7 FPGA (-2)	178	185	155	203	120	157
Artix®-7 FPGA (-3)	204	212	172	225	146	191
Zynq® 7000S SoC (-2)	187	194	156	204	129	169
Zynq-7000 SoC (-3)	212	220	171	224	141	185
FPGAs, 3D ICs, and MPSoCs						
Kintex®-7 FPGA (-3)	298	310	228	299	204	267
Virtex®-7 FPGA (-3)	300	312	238	312	208	272
Kintex UltraScale™ FPGA (-3)	393	409	280	367	242	317
Virtex UltraScale FPGA (-3)	384	399	283	371	245	321
Kintex UltraScale+™ FPGA (-3)	518	539	384	503	345	452
Virtex UltraScale+ FPGA (-3)	505	525	396	519	327	428
Zynq UltraScale+ MPSoC (-3)	493	513	379	496	329	431

MicroBlaze™ Processor Block Diagram

- Full Harvard architecture
- 32-bit instruction set and general-purpose registers
- 32-bit address bus, extensible to 64 bits
- Optional floating point unit
- Sleep, Hibernate, and Suspend Mode/Instructions



MicroBlaze™ Processor Optimized for Embedded Applications

Efficient Architecture

- Soft processor core based on 32-bit RISC Harvard architecture
- Instruction and Data-side Cache
- 3-stage pipeline – size optimized
- 5-stage pipeline – performance optimized
- 8-stage pipeline – frequency optimized

Flexible Configurations

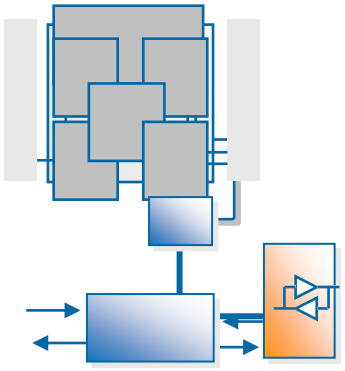
- Three selectable preset configurations with seven additional templates
- Optional Memory Management (MMU) and Floating Point Unit (FPU)
- Native AXI-4 interfaces and/or Local-Memory Bus (LMB)
- 32-bit or 64-bit implementation for maximum memory space utilization

Proven, Widely Adopted Solution

- In production since 2001
- Comprehensive ecosystem of IP and development tools
- Works on any AMD-Xilinx device (logic space permitting)

MicroBlaze™ Processor fits a wide variety of Embedded Systems

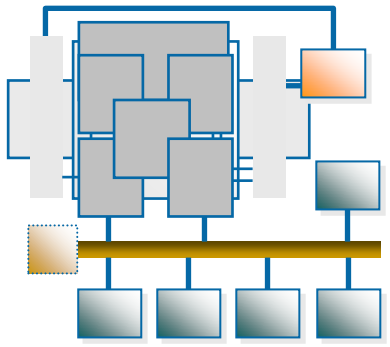
3-stage pipeline



Microcontroller

- Small footprint
- Few to no peripherals
- No OS
- Vast range of applications
- Baseline processing

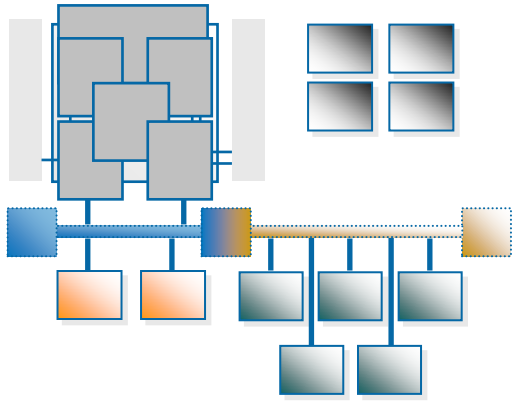
3/5-stage pipeline



Realtime Processor

- Medium footprint
- Moderate peripherals
- Small-footprint OS or standalone
- Performance targeted to control, automation and instrumentation

5/8-stage pipeline



Application Processor

- Large footprint
- Extensive peripherals
- Linux-ready
- Networking & Wireless
- Highest performance

MicroBlaze™ Processor Applications

The MicroBlaze™ processor meets the requirements of many diverse applications including:

- Industrial
- Medical
- Automotive
- Consumer
- Communications






MicroBlaze™ Processor Deployment

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MicroBlaze™ Processor Memory Hierarchy

- Local Memory
  - Tightly coupled memory with a very low access latency through a dedicated interface
- Block RAM
  - Block RAM connected through an AXI interface if local memory is insufficient or shared memory is required
- External Memory
  - External memory is usually either RAM (DDR, SRAM) or some form of non-volatile memory such as QSPI NOR
- Shared Memory
  - With the AXI block RAM or external DDR a common interconnect must be used with other DMA, otherwise they won’t be accessible to those memories

MicroBlaze™ Processor Interfaces

MicroBlaze processor can be configured with the following bus interfaces:

- The AMBA® AXI4 interface (AXI4)
  - The AXI4 interfaces provide a fast, non-arbitrated streaming communication mechanism through a connection to both on-chip and off-chip peripheral interfaces and memory
  - MicroBlaze processor also supports up to 16 AXI4-Stream interface ports, each with one primary and one secondary interface
- ACE interface (ACE)
  - The AMBA AXI4 or AXI Coherency Extension (ACE) Interface provides cache coherent connections to memory
- Lockstep Interface
  - The lockstep interface is designed to connect a primary to one or more of MicroBlaze processor instances

MicroBlaze™ Processor Interfaces

- Debug interface
  - Debug interface to access debug registers, used with the Microprocessor Debug Module (MDM) core which enables JTAG-based debugging of one or more MicroBlaze processors
- Trace interface
  - Trace interface for performance analysis to funnel and store MicroBlaze processor program trace in external storage
  - Program trace from connected MicroBlaze processors can be directly output on an external interface, stored in external memory via the AXI4 port, or transmitted on an AXI4-Stream interface

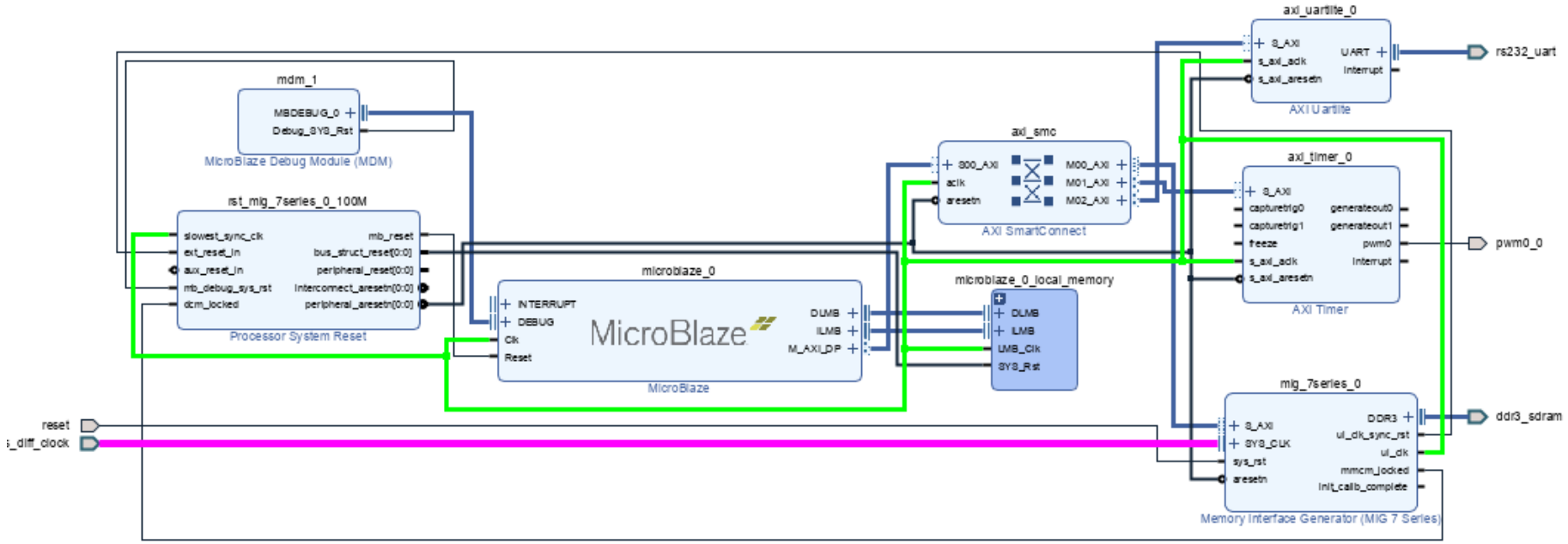
MicroBlaze™ Processor Interfaces

- Local Memory Bus (LMB)
  - The LMB module is used as the LMB interconnect for AMD-Xilinx FPGA based embedded processor systems.
  - The LMB is a fast, local bus for connecting MicroBlaze instruction and data ports to high-speed peripherals, primarily on-chip block RAM (BRAM).
- Instruction Cache Bus Interface
  - MicroBlaze processor can be used with an optional instruction cache for improved performance when executing code that resides outside the LMB address range
  - Cache can be implemented in the DDR
- Data Cache Bus Interface
  - The MicroBlaze processor can be used with an optional data cache for improved performance
  - Cached memory range must not include addresses in the LMB address range
- Clock and Reset Interface

MicroBlaze™ Processor Clocking & Interrupts

Clocking MicroBlaze processor is simple:

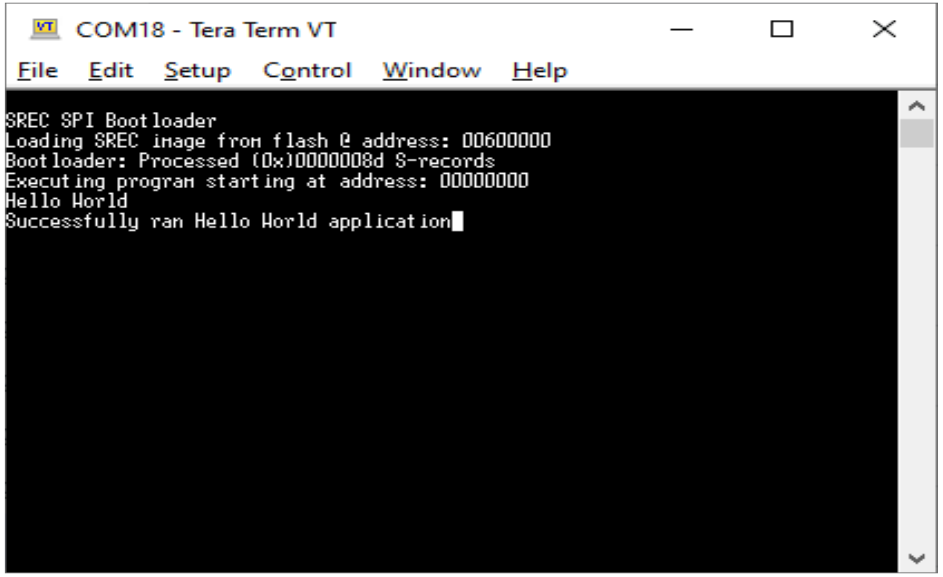
- Single input clock - max frequency depends on the Fabric and Configuration
- DDR / MIG clock MB is derived from the User Interface Clock
- MicroBlaze processor provides exceptions and interrupt handling
    - Use AXI Interrupt Module to connect Interrupts



Build and Configuration

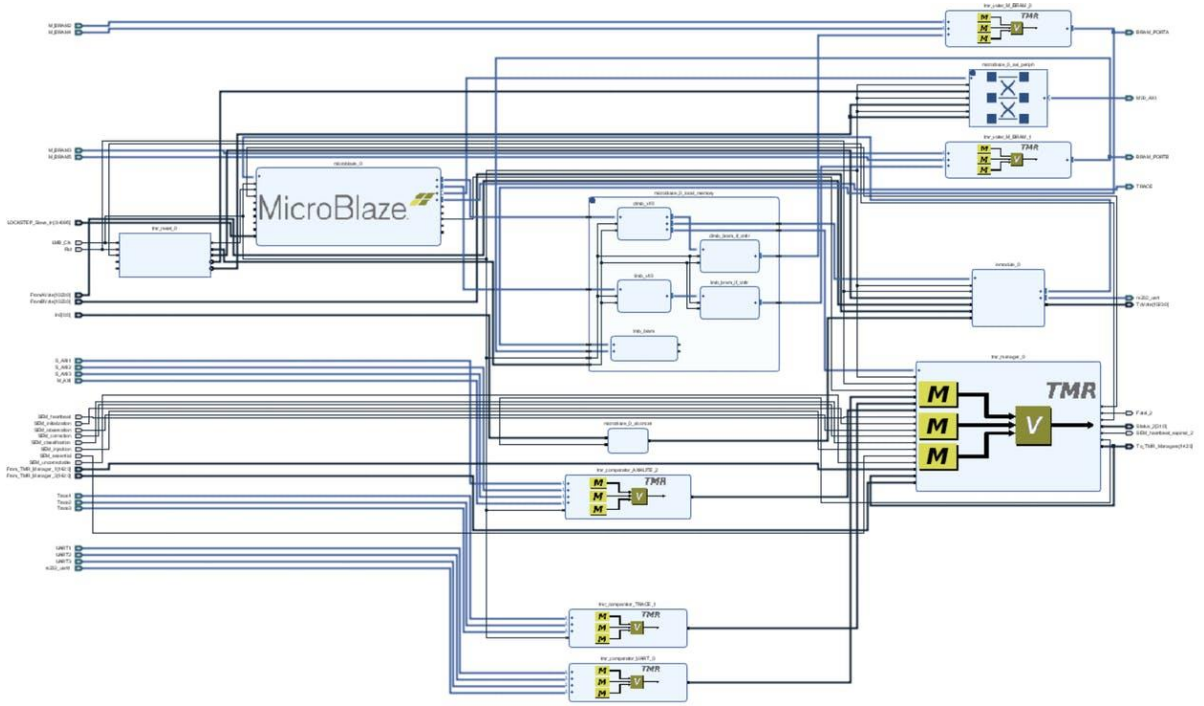
Configuration of the MicroBlaze™ processor can occur in several methods:

- Small application running from BRAM – ELF can be merged with the bitstream
  - Application starts running on boot
- Large application running from DDR – more complex
  - Application needs to be stored in QSPI, bootloader is created and merged FPGA bit stream
  - Bootloader cross loads the MicroBlaze processor from the QSPI to DDR on boot



MicroBlaze™ Processor Safety and Security

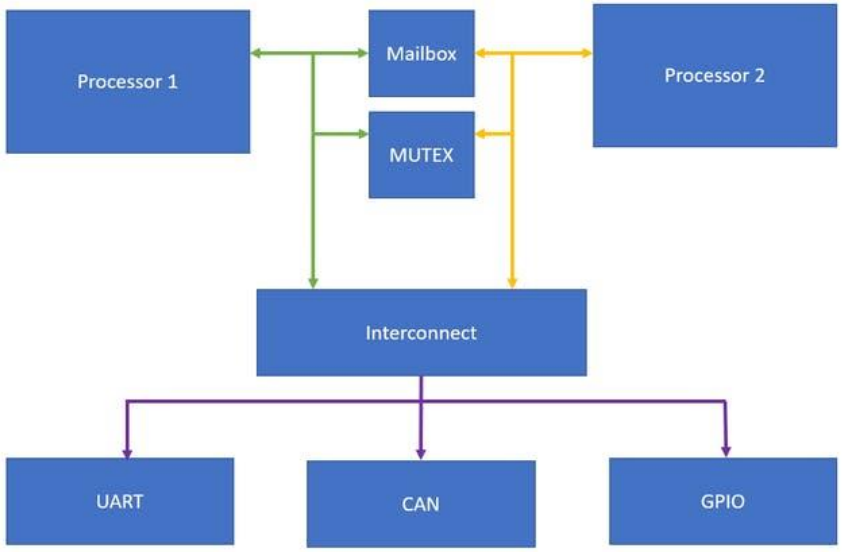
- MicroBlaze processor can be implemented in Lockstep or TMR solutions for higher reliability applications for Safety
- Security and Safety critical solutions can leverage XADC / System Monitor to monitor device parameters and temperature
  - Small application running from internal block RAM for maximum security



MicroBlaze™ Processor Safe Communications

Multi Processor Communications need care to ensure safe communication and resources are shared

- Mailbox – allows bi-directional communication between multiple processors using a FIFO based approach to messaging
- Mutex – implement mutual exclusion locks, allowing processors to lock shared resources, preventing multiple accesses at the same time



MicroBlaze™ Processor Microcontroller System (MCS)

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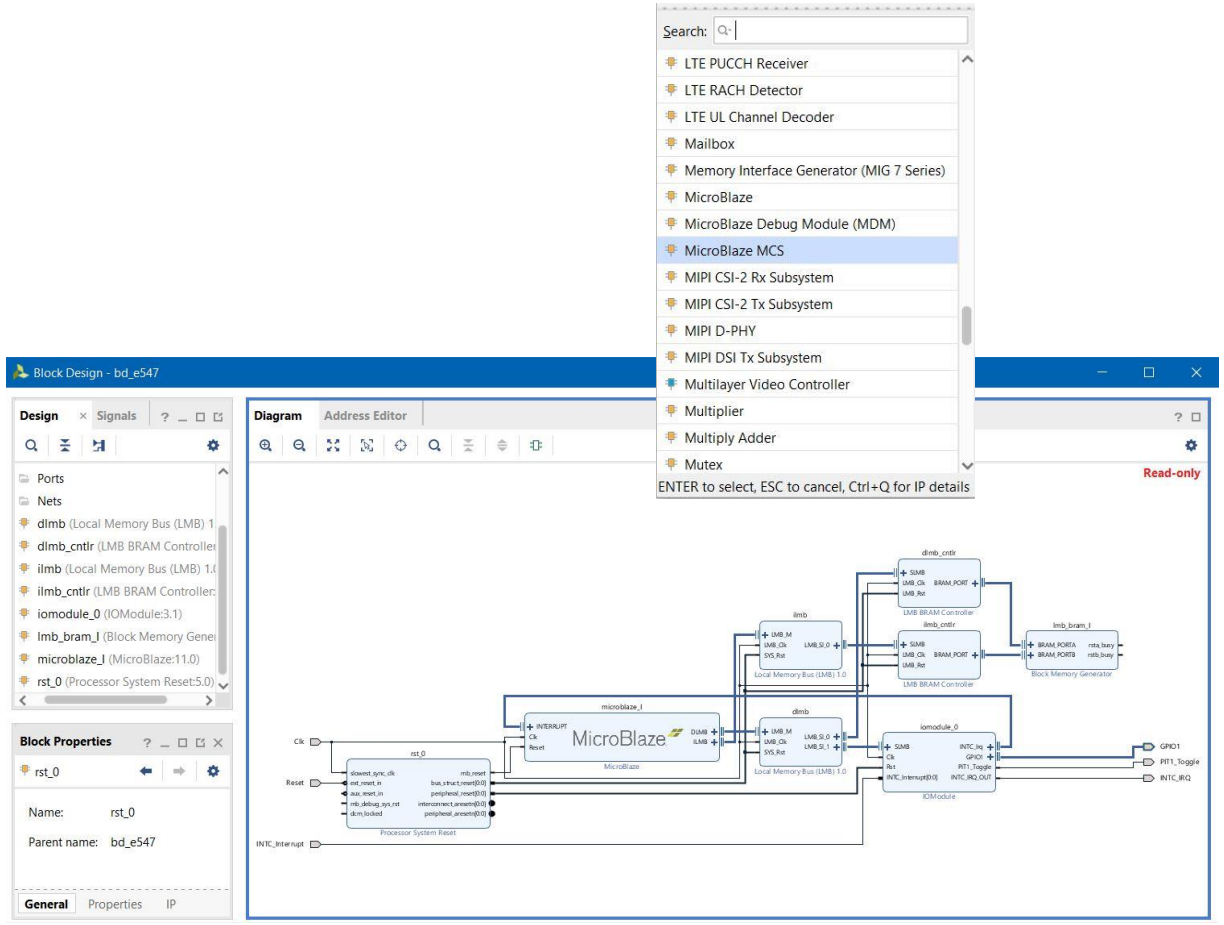
MicroBlaze™ Processor Microcontroller System (MCS)

MicroBlaze Processor Microcontroller System (MCS):

- The same MicroBlaze processor IP with fewer configuration options
- Peripherals in a single IO module and configuration wizard
- Available in all editions of Vivado® ML
- Generates a MicroBlaze processor-based block design with connected peripherals
- Same MicroBlaze performance
- Ideal for small microcontroller applications
- Ideal for users new to MicroBlaze or processor design



MicroBlaze™ Processor MCS includes

- MicroBlaze processor, pre-configured for 3-stage pipeline mode (area optimized)
  - With 5-stage pipeline option
- Local Memory Support (4 – 128kB)
- IO Module Peripherals:
  - MicroBlaze Debug Module (MDM)
  - UART
  - Interrupt Controller, with 16 external interrupts
  - Up to 4 Programmable Interval Timer (PIT)
  - Up to 4 Fixed Interval Timers (FIT)
  - 4 x 32-bit General Purpose Output (GPO)
  - 4 x 32-bit General Purpose Input (GPI)
  - Simple IO Bus (compatible with Xilinx Dynamic Reconfiguration Port)

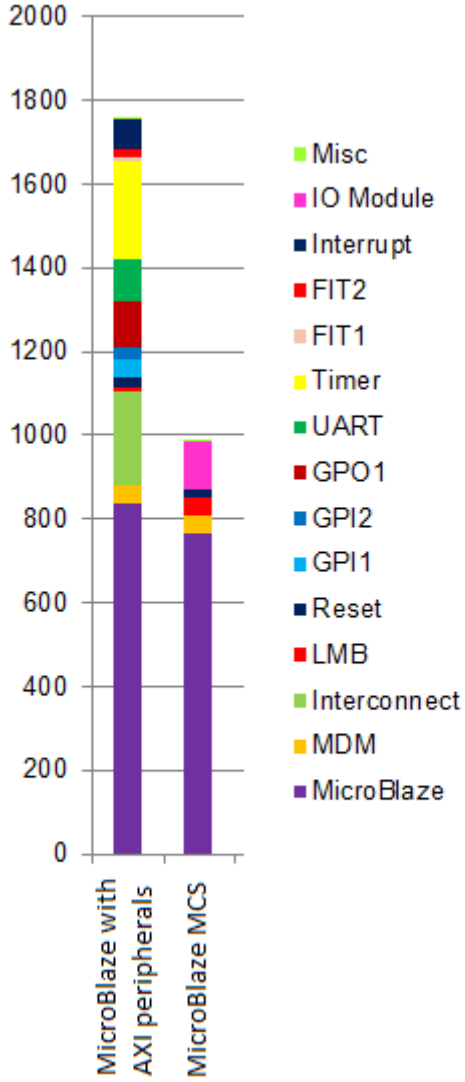
MicroBlaze™ Processor MCS does not include

- Does not include data port (DAXI) for external memory access
- Does not include AXI streaming data ports
- Does not include AXI interface connections
- Does not include Ethernet, SPI, or I2C
- Does not support full MicroBlaze processor configuration options

If you need these options, use the full MicroBlaze processor IP, not MCS

Same MicroBlaze™ Processor Performance, Smaller Overall Footprint

- Same Fmax as MicroBlaze processor system
- Tightly coupled IO module makes MicroBlaze processor MCS smaller
  - One 32-bit Programmable Interval Timer(PIT),
  - Two Fixed Interval Timer (FIT), 500,000 and 216 periods
  - Three GPI, 3,4 and 4 bits wide
  - Two GPO, 8 and 11 bits wide
  - One UART fixed baud rate, no fifo
  - Interrupt controller with UART, PIT and one FIT interrupt
  - 8 Kbytes of internal memory



MicroBlaze™ Processor Debug Module

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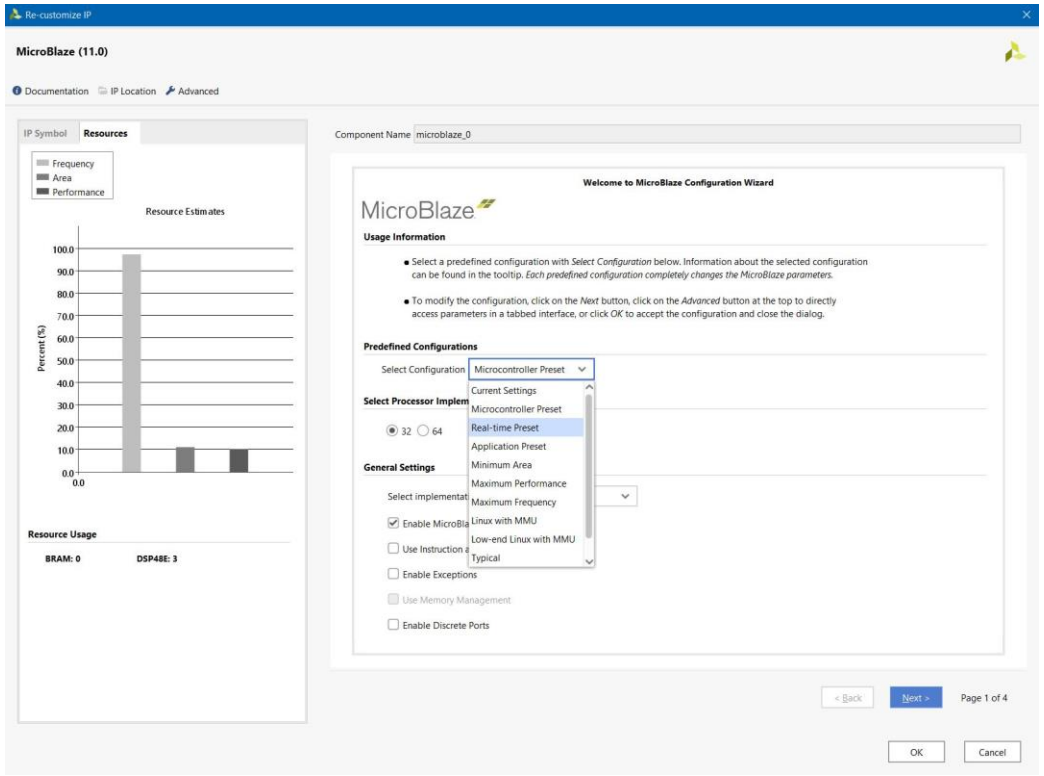
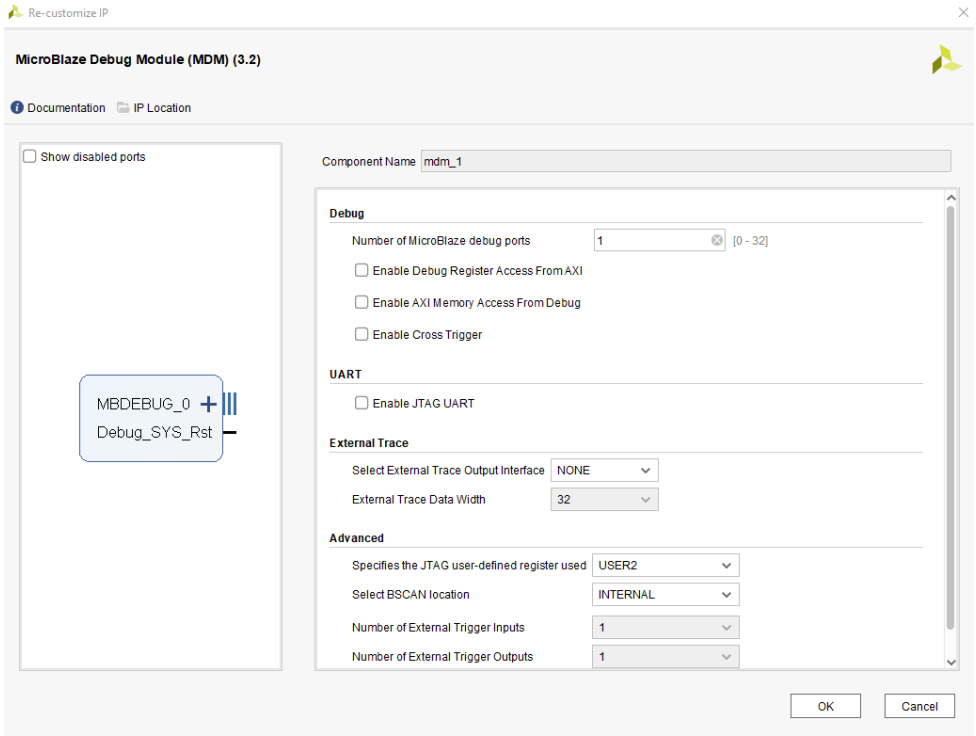
MicroBlaze™ Processor Configurations

- Three selectable preset configurations
  - Microcontroller
  - Real-Time
  - Application
- Seven additional templates
  - Minimum Area
  - Maximum Performance
  - Maximum Frequency
  - Linux with MMU
  - Low-End Linux with MMU
  - Typical
  - Frequency Optimized
- With Performance, Area, Frequency optimization
  - Depending on configuration



MicroBlaze™ Processor Debug Module

- Enables JTAG-based debugging of one or more MicroBlaze processors
- Debug up to 32 MicroBlaze processors
- Synchronized control of multiple MicroBlaze processors
- JTAG-based UART with a configurable AXI4-Lite interface
- Based on Boundary Scan (BSCAN) logic in AMD-Xilinx devices
- Direct JTAG-based access to memory with a configurable AXI4 interface



MicroBlaze™ Processor OS and Communication

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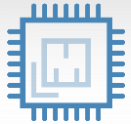
Operating Systems and Configurations

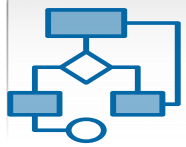


Microcontroller
1.1 DMIPS/MHz
Logic Cells: 1,900

Microcontroller profile at 200MHz offering 1.1 DMIPS/MHz, typically running from external memory with a number of low performance peripherals. This configuration is comparable to the Arm® Cortex®-M0/M1 processors, which typically runs at 40-50MHz.

Real-Time Processor
1.3 DMIPS/MHz
Logic Cells: 4,000

Real-Time profile processor with RTOS support for systems needing deterministic response and performance offering 1.3 DMIPS/MHz. This configuration includes scalable instruction cache and data cache, and soft DDR controller. This profile is comparable to Arm Cortex-M3/M4 processors.

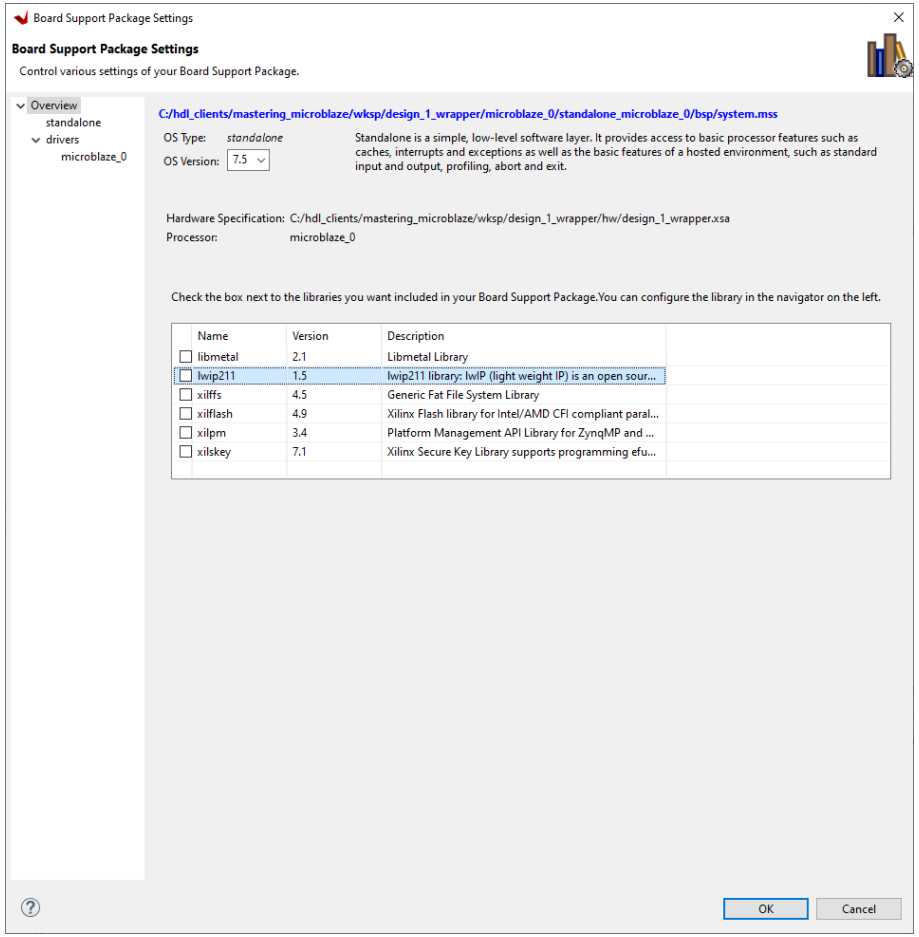


Application Processor
1.4 DMIPS/MHz
Logic Cells: 7,000

Application Processor profile offering 1.4 DMIPS/MHz supports embedded Linux and includes a memory management unit and Ethernet controller– since they're common in Linux systems. This is comparable to Arm Cortex-A5 processors.

MicroBlaze™ Processor External Communications

- Role of MicroBlaze processor is often to handle external communications
  - Via simple interfaces, e.g., UART
  - Via more complex interfaces, e.g., Ethernet
- Any IP supported in Vivado® ML Canvas has supported drivers with MicroBlaze processors
  - e.g., CAN, I2C, SPI



Tools Support

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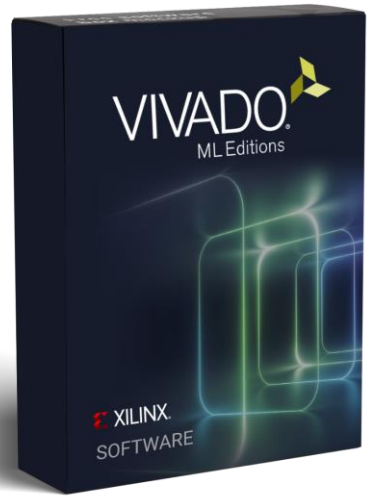
Design Tools for MicroBlaze™ Processor

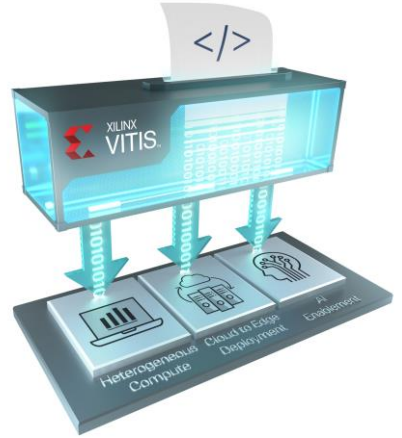
Implement MicroBlaze processor-based designs with Vivado® ML

- No charge, no licensing, no royalties
- Extensive configuration wizard with built-in templates
- Configurable example designs

Design MicroBlaze processor software with Vitis™ unified software platform

- Debug using Breakpoints, Watchpoints, XSCT, hardware-server, halt and resume, register updates…
- Single or multiple MicroBlaze processor instantiations
- FPGA soft-processor
  - On any Xilinx FPGA
- MicroBlaze processor co-processing alongside Arm
  - Heterogenous debug and development
  - Zynq®-7000, Zynq UltraScale+ devices, and Versal® ACAP





MicroBlaze™ Processor Workshop

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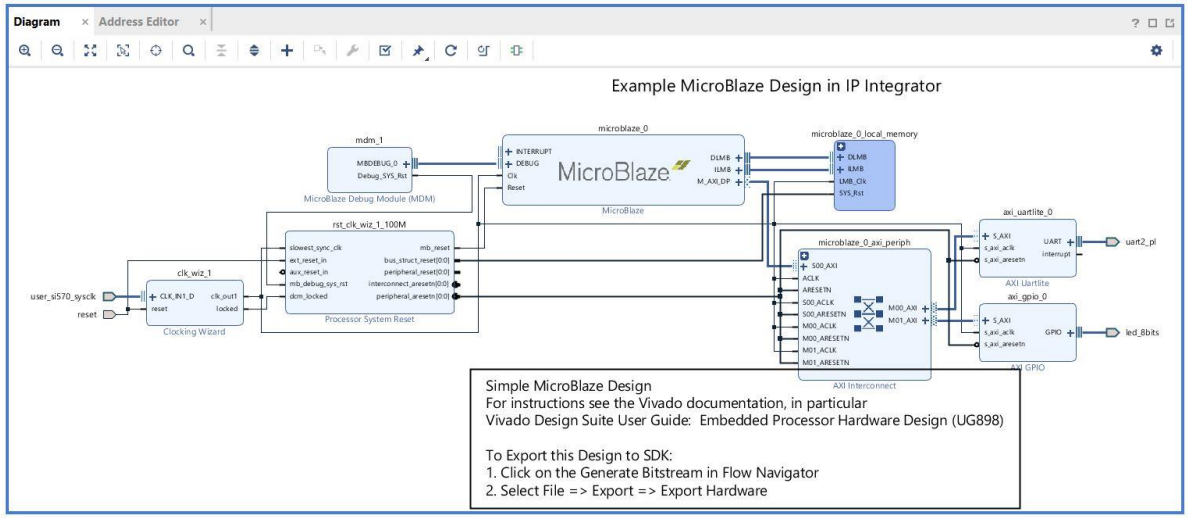
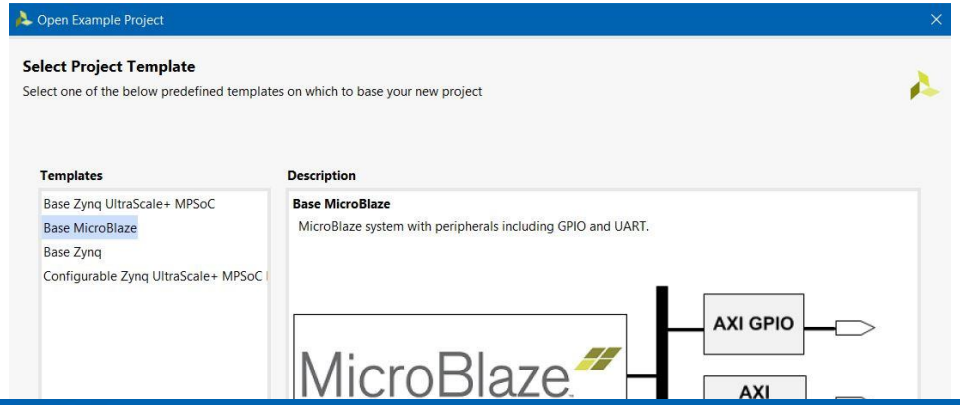
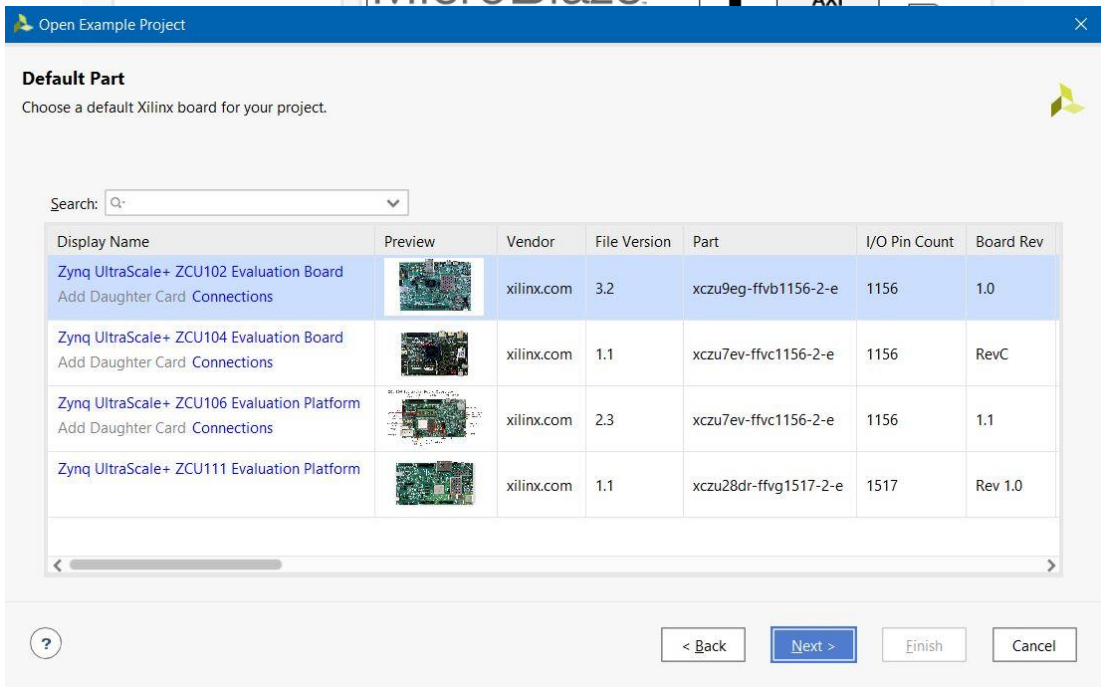
MicroBlaze™ Processor Example Design

- One of four configurable example designs included in Vivado® ML
- Example design can be applied to multiple Xilinx or partner boards
- Drag and drop board interfaces
- Design Assistance to help connecting I/O and peripherals



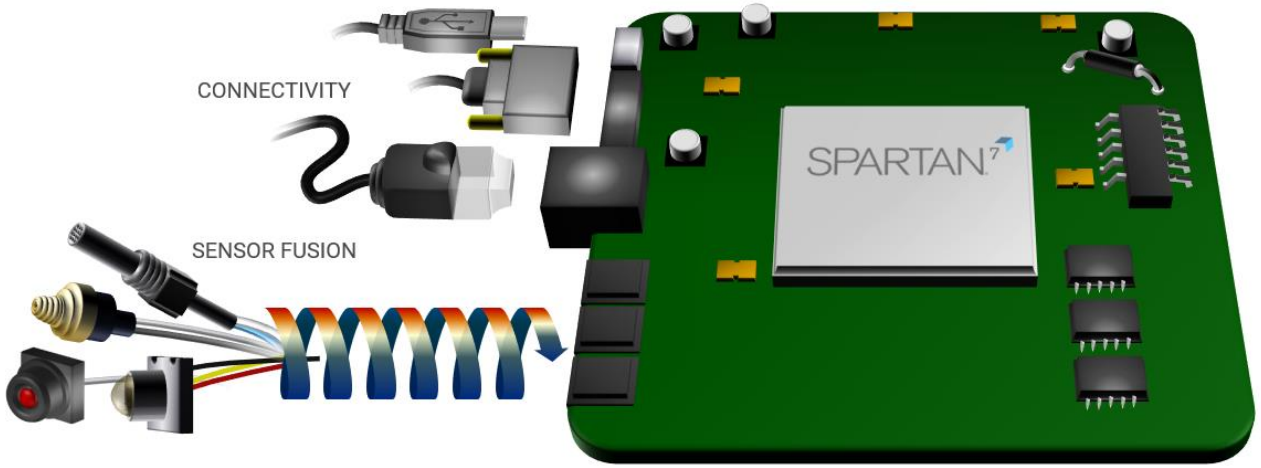




Demonstration Time!

Bare Metal Application with MicroBlaze™ Processor

- Create Project **Vivado® ML**
- Target SP701 Evaluation Kit
- Build MicroBlaze™ Processor Design
- Synthesize and implement
- Pin allocation
- Export to **Vitis™** development platform
- Create a basic application that interacts with SP701 peripherals
- Power on board and set UART communication
- Download application



Both demonstrations available **On-Demand** to follow along later

Demonstrations use Software Release 2022.1

MicroBlaze™ Processor Collateral

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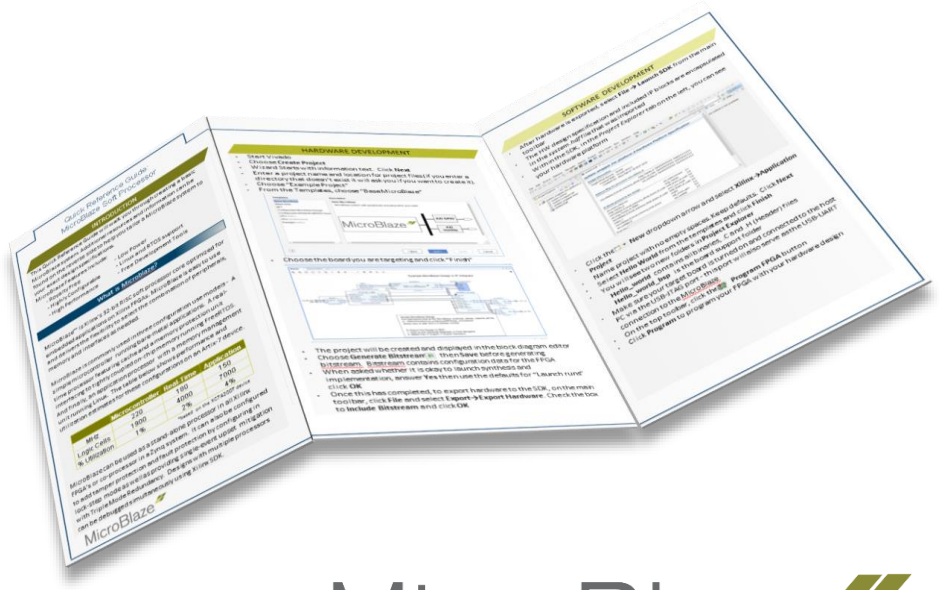
MicroBlaze™ Processor Quick Start Guide

Start Programming in Minutes



MicroBlaze™

HARDWARE DEVELOPMENT IN VIVADO® ML

- **Step-by-step wizard** for target board
- Instantiate MicroBlaze processor design from templates
- Compile design and export to **Vitis™** software platform

SOFTWARE DEVELOPMENT IN VITIS

- **Launch Vitis** software platform from Vivado ML
- Launch “Hello World” from template
- Connect USB-JTAG port and **program board**

FAQ & ADDITIONAL RESOURCES

- Common questions on OS support, debug, etc.
- Links to wiki, reference guides, more tutorials
- Links to other supported boards and partners

Available at: www.xilinx.com/microblaze

Opal Kelly Development Platform Available Now

Featuring the Artix® UltraScale+™ AU25P device

Versatile platform for multiple markets

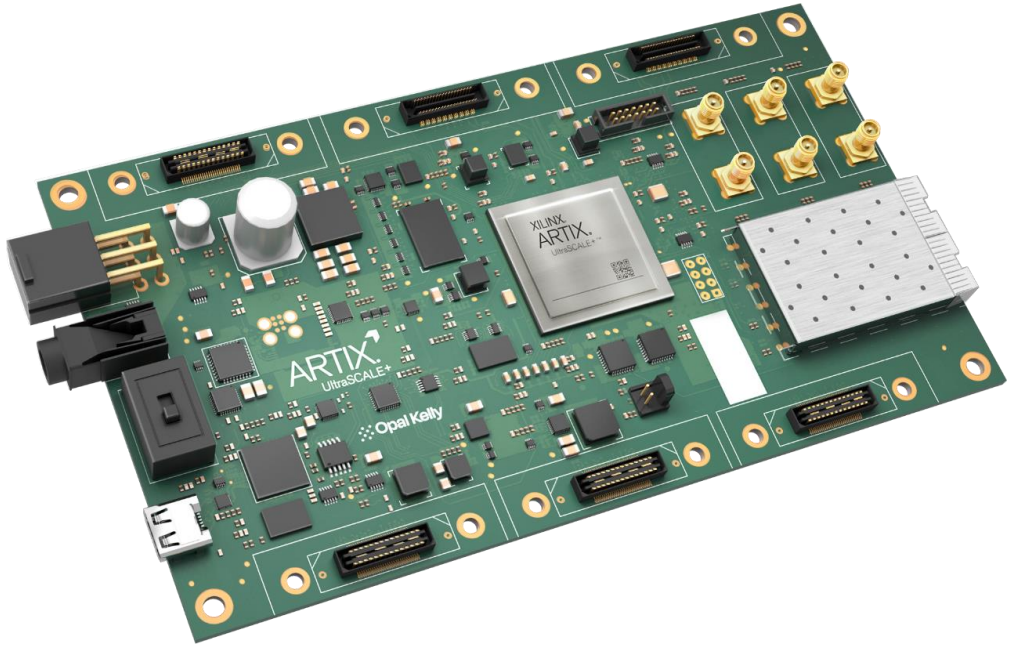
- AU25P production device (largest in portfolio)
- 1GiB DDR4-2666 memory, 32MiB QSPI Flash
- Superspeed USB 3.0 host interface
- Ideal for capturing and processing large data streams

FrontPanel SDK for SW/HW integration

- Stand-alone desktop app or API for custom integration
- Ideal for prototyping, proof-of-concept, and production
- Included with XEM8320 (no additional charge)

SYZYGY modular connectivity

- Compact connectors for data acquisition, sensing, networking
- 4 SYZYGY standard ports
- 2 SYZYGY transceiver ports



Opal Kelly

$1,349.95

Product Page

Avnet Development Board Available Q4’22

Featuring the Zynq® UltraScale+™ ZU1CG device

Based on ZU1CG, the newest Zynq® UltraScale+™ device

- Targets XCZU1CG-1SBVA484E device
- Ideal for entry level development activities
- One Click and three SYZYGY expansion ports

Target applications

- Artificial Intelligence / Machine Learning
- Embedded processing
- Robotics

Availability and training

- Available for pre-orders
- Free 3-day, online technical training in Q4’22

AVNET

$159

Product Page

Summary

MicroBlaze

Fast soft-processor performance with the highest flexibility

Programmable Systems Integration	Works with any AMD-Xilinx device Highly configurable to fit almost any footprint requirement
Increased System Performance	500+ DMIPs performance in select FPGA devices
BOM Cost Reduction	MCS version packs more IP peripherals into a single package, reducing overall processing footprint
Total Power Reduction	Sleep and standby mode and instructions for low-power applications
Accelerated Design Productivity	Three pre-set configurations with seven additional templates, highly scalable across a wide range of applications

Next Steps and Q&A

- Learn more about COP FPGAs and SoCs
  - » Visit www.xilinx.com/products/silicon-devices/cost-optimized-portfolio
- Access more information about the MicroBlaze™ Processor
  - » Visit www.xilinx.com/products/microblaze
- Buy an evaluation kit
  - » Opal Kelly XEM8320: www.opalkelly.com/products/xem8320
  - » Avnet ZUBoard 1CG: www.avnet.com/wps/portal/us/products/avnet-boards/avnet-board-families/zuboard-1cg
  - » Xilinx SP701: www.xilinx.com/products/boards-and-kits/sp701.html
- Download tools
  - » Xilinx® Vivado® ML / Vitis™ Tools: www.xilinx.com/downloads
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Ask Your Questions in the Chat Window Now

Thank You!

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