

## 5. Supply Voltage

Conventional integrated circuits must be powered by supply voltages ranging from 3 to 5 v. At these voltages, the design of efficient power supplies that can provide the required power is difficult. MOS devices, on the other hand, typically are powered by supply voltages ranging from 10 to 30 v. At these voltages, supply design is easier and efficiency is higher.

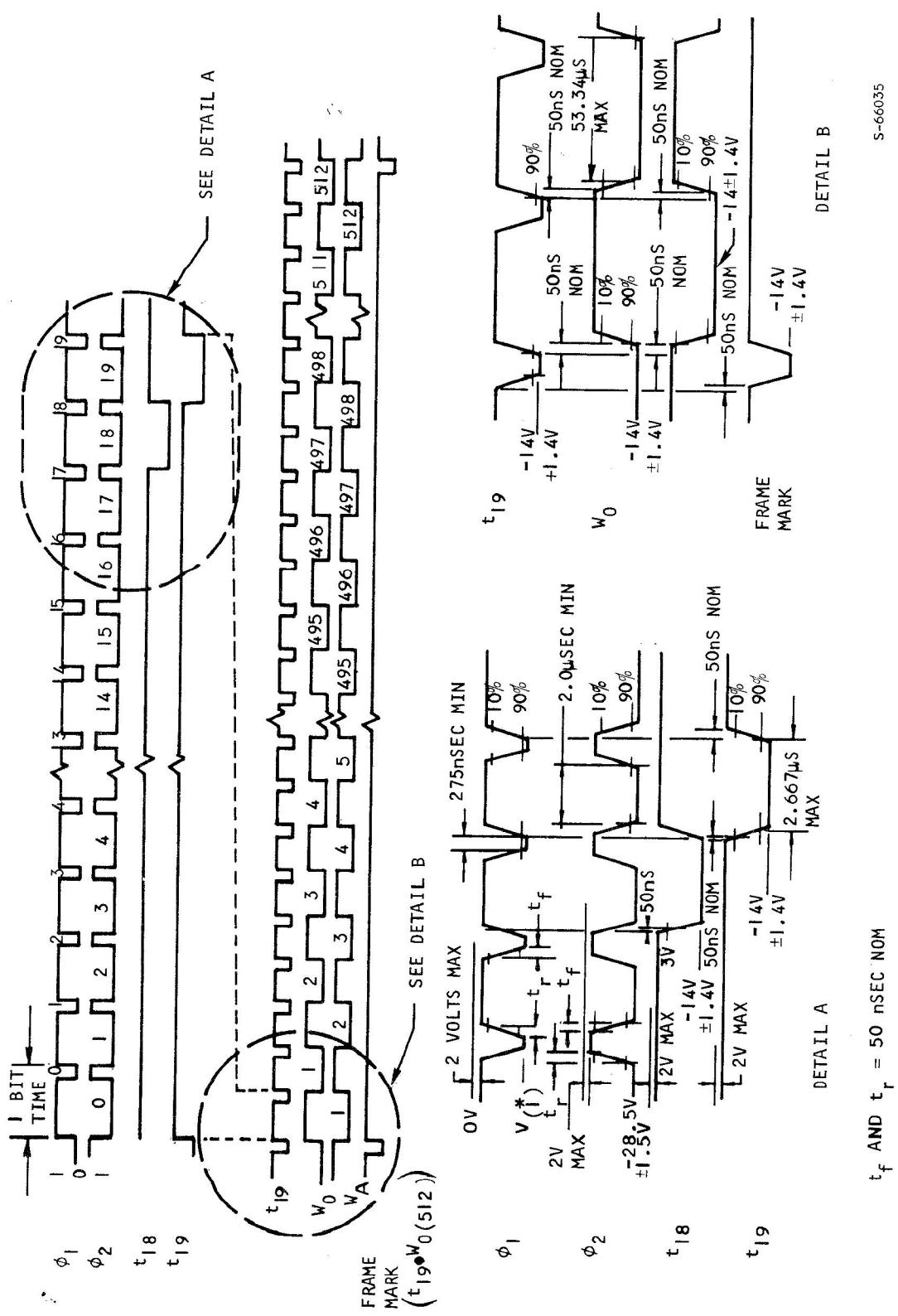
## SYSTEM TIMING

The CADC system clock is a 1.5-MHz oscillator. This is divided down to produce two clocks, phase one ( $\phi_1$ ) and phase two ( $\phi_2$ ), at a frequency of 375 kHz. One complete clock period ( $\phi_2$  to  $\phi_2$ ) is defined as a bit time (see Figure 1-2), which is 2.666  $\mu$ sec. Every 20 consecutive bit times are defined as a word. The first bit time of a word is called T<sub>0</sub>, and the last bit time of the word is called T<sub>19</sub>. Two types of words in the system are  $W_A$  and  $W_0$ .

In  $W_A$ , the parallel arithmetical algorithms operate and control (instruction) words are shifted serially into the units. In  $W_0$ , computational inputs and outputs are shifted serially among the units. A word mark used to distinguish word times is a signal coincident with T<sub>18</sub> of every word time. Two consecutive word times,  $W_A$  and  $W_0$ , is called an operation (OP) time. The total number of operations used in the CADC is 512.

To distinguish the final OP time, a frame mark is generated. This is a signal coincident with T<sub>18</sub> of the final word time of the final OP. The time between frame marks is called a frame. A frame includes one complete computational cycle.





\*AT ROOM TEMPERATURE  $V_{(t_r)}$  = -28.5

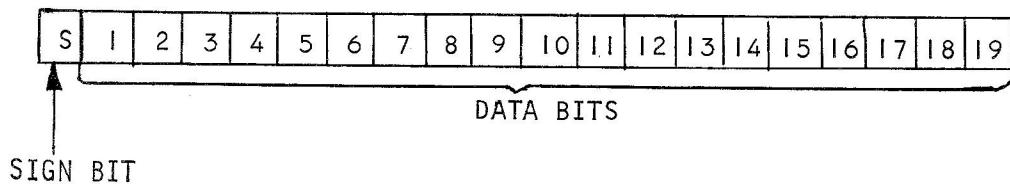
AT  $-55^{\circ}\text{C}$ ,  $-28.5 \pm 1.5\text{ V}$ , AT  $125^{\circ}\text{C}$ ,  $-29.5 + 1$ ,  $-0.5\text{ V}$

1. CLOCK VOLTAGE WILL NOT GO POSITIVE.

**NOTES:** 1. CLOCK VOLTAGE WILL NOT GO POSITIVE.  
2. MAX OVERLAP  $\phi_1$  AND  $\phi_2$  VOLTAGE IS  $3.0 \text{ V}$ .

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The processor is a fractional fixed point machine with the most significant bit a sign bit (0 = plus, 1 = minus) and the other 19 bits representing data. Negative numbers are represented in 2's complement notation.



Fractional equivalent of each bit:

S = 0 (plus) 1 (minus)

1 = 0.50000000

2 = 0.25000000

3 = 0.12500000

4 = 0.06250000

5 = 0.03125000

6 = 0.01562500

7 = 0.00781250

8 = 0.00390625

9 = 0.00195312

10 = 0.00097656

11 = 0.00048828

12 = 0.00024414

13 = 0.00012207

14 = 0.00006103

15 = 0.00003051

16 = 0.00001525

17 = 0.00000762

18 = 0.00000381

19 = 0.00000191



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### Examples:

During bit time  $T_0$ , information in the computer registers is properly oriented, i.e., all the bits of a data word are contained in properly corresponding register positions. Control words are shifted serially into the logic chips from ROM's during  $W_A$  of every OP, and thereby specify various details of the present and subsequent operations. Meaningful data transfers into and out of the logic chips and registers occur during  $W_0$  of every OP. The LSB is transferred first and the MSB (sign bit) last. The functions of each circuit are defined below.

## CIRCUIT FUNCTIONS

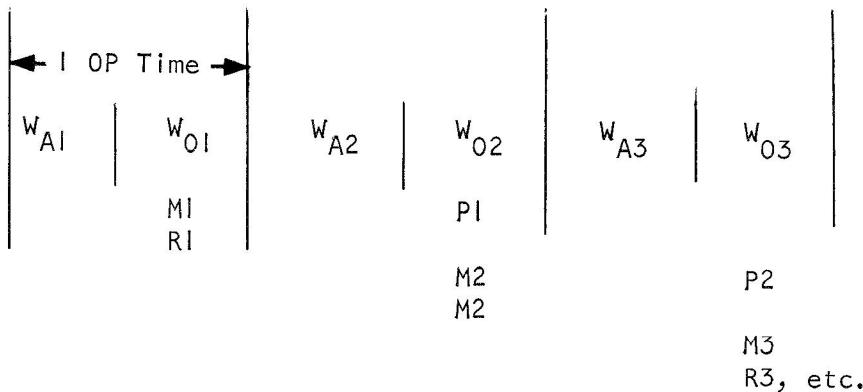
## Parallel Multiplier Unit (PMU), PN 94411

The PMU accepts two serial inputs, multiplicand and multiplier, in one word time ( $W_0$ ) and produces their properly rounded product by means of a parallel algorithm in one more word time ( $W_A$ ). The product is shifted out in the next  $W_0$ , while inputs for the next operation are simultaneously shifted in.



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where

$W_{01}$  = Operands for the first multiply are shifted into the PMU.

$W_{A2}$  = Product of MI and RI is produced by the PMU.

$W_{02}$  = Product of MI and RI shifted out of PMU and also the operands for the second multiply are shifted into the PMU.

$W_{A3}$  = Product of M2 and R2 is produced by the PMU.

The contents of the M register are also shifted out the same time as the product. The multiplication operation is achieved by using Booth's algorithm (see Appendix A). The PMU does not need a control word to operate, but is capable of operating continuously in the prescribed manner.

The inputs to the PMU are  $M_{IN}$  (multiplicand input), R (multiplier),  $\phi_1$ ,  $\phi_2$ , TI8,  $W_0$ ,  $V_{DD}$  (-14V), and ground. The two outputs are  $M_0$  (multiplicand out) and P (product). The package pin assignments are shown in Figure I-3. The PMU is packaged in a 24-pin dual in-line package as shown in Figure I-4.

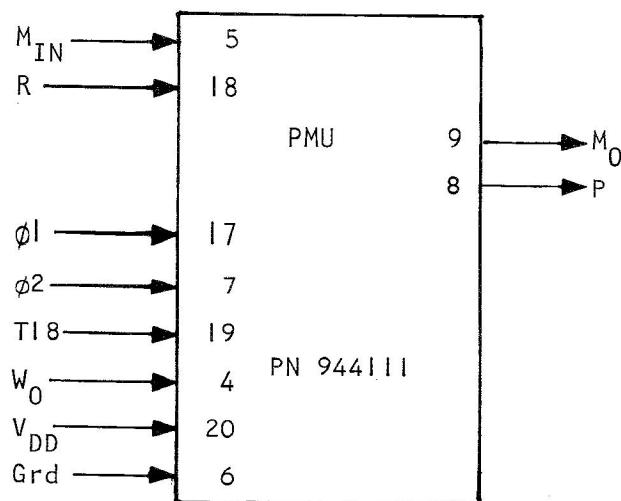


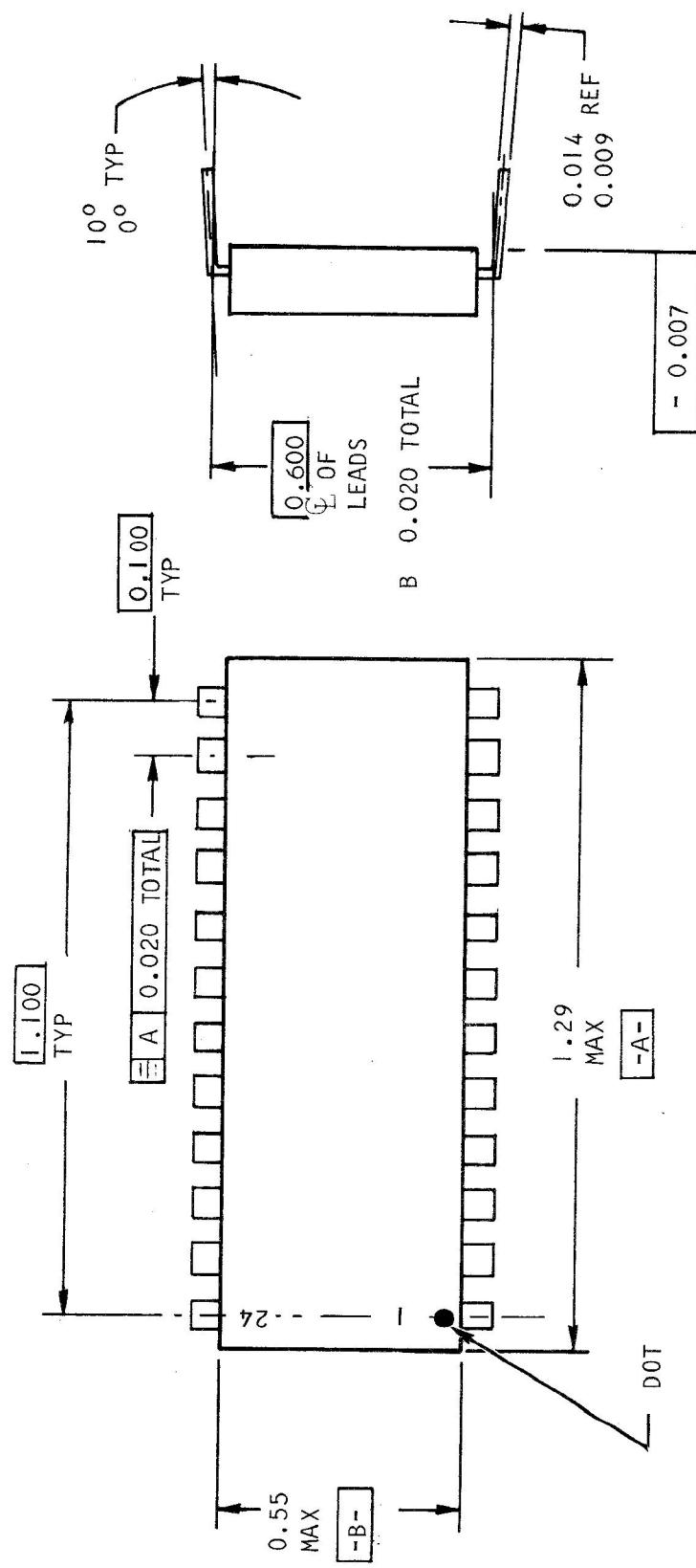
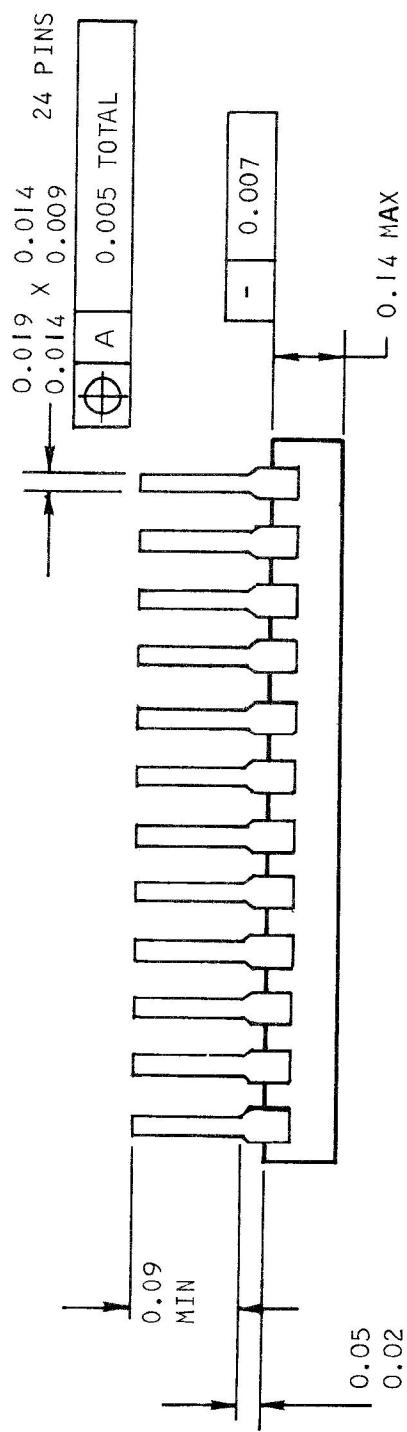
Figure I-3. PMU I/O



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Figure 1-4. PMU Package Outline

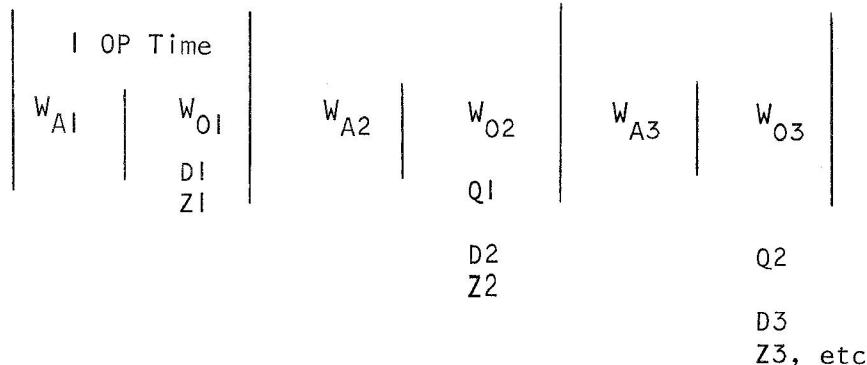
When using the PMU in a system, there are certain timing and propagation delay considerations. These considerations will be discussed later under Software System and Considerations.

Electrical characteristics and logic diagrams of the PMU can be obtained from Source Control Drawing 944111.

The PMU contains 1063 active MOS devices and has a chip size of 150 by 153 MILS. A photograph of an actual chip is shown in Figure I-5.

#### Parallel Divider Unit (PDU), PN 944112

The PDU accepts two serial inputs, dividend and divisor, in one word time ( $W_0$ ) and produces the proper truncated quotient by means of a parallel algorithm in one more word time ( $W_A$ ). The quotient is shifted out in the next  $W_0$ , while inputs for the next operation are simultaneously shifted in.



where

$W_{O1}$  = Operands for the first divide are shifted into the PMU.

$W_{A2}$  = Quotient of  $D_1$  and  $Z_1$  is produced by the PDU.

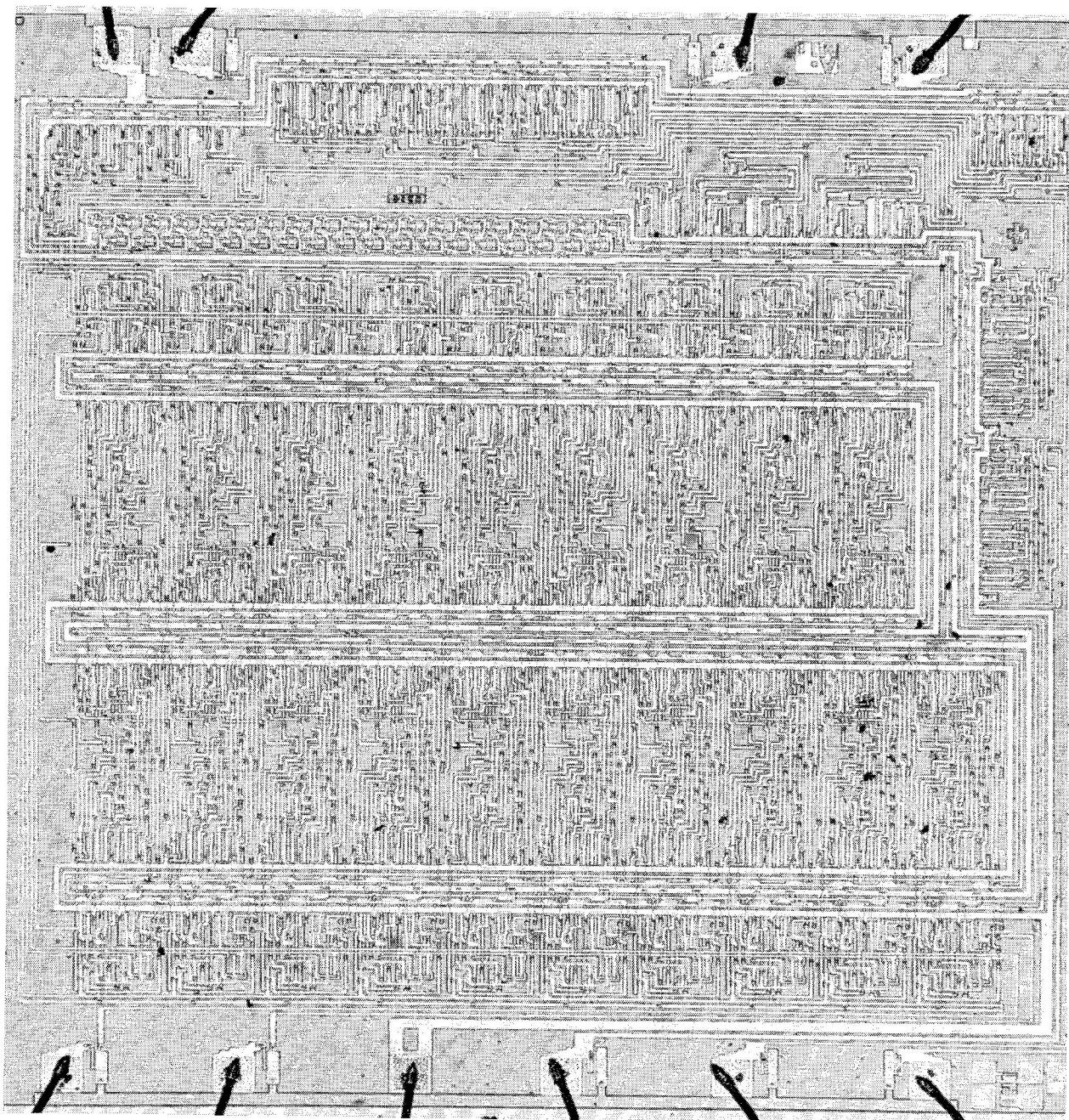
$W_{O2}$  = Product of  $D_1$  and  $Z_1$  shifted out of PDU and also the operands for the second divide are shifted into the PDU.

$W_{A3}$  = Quotient of  $D_2$  and  $Z_2$  is produced by the PDU.

The division operation is achieved by using a nonrestoring division algorithm (see Appendix B). The PDU does not need a control word to operate but is capable of operating continuously in the predescribed manner.

The inputs to the PDU are D (dividend), Z (divisor),  $\phi_1$ ,  $\phi_2$ , T18,  $W_0$ ,  $V_{DD}$  (-14V), and ground. The only output is the quotient (Q). The package pin assignments are shown in Figure I-6. The PDU is packaged in a 24-pin dual in-line package as shown in Figure I-7.





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Figure I-5. Parallel Multiplier Unit PN 944111, 1063 Devices



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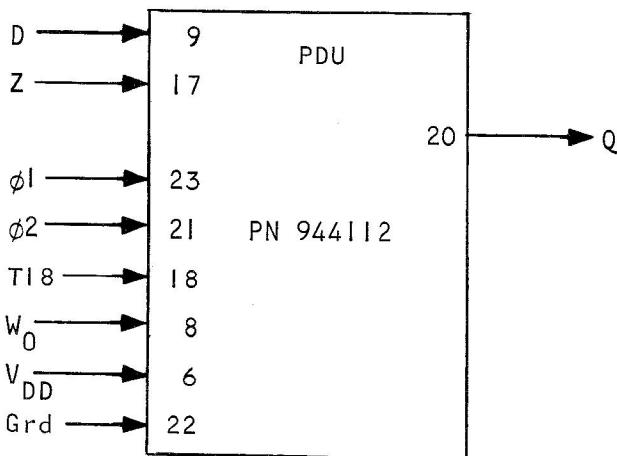


Figure I-6. PDU I/O

When using the PDU in a system, there are certain timing and propagation delay considerations. These considerations will be discussed later under Software System and Considerations.

Electrical characteristics and logic diagrams of the PDU can be obtained from Source Control Drawing 944112.

The PDU contains 1241 active MOS devices and has a chip size of 141 by 151 MILS. A photograph of an actual chip is shown in Figure I-8.

#### Special Logic Function (SLF), PN 944113

The SLF performs logical operations and generates specific data and logic outputs. The unit accepts a control word of 4 bits. This control word specifies details of the operation as described below.

The fundamental logical operation of this unit is the limit function. It consists of three registers (U, P, and L) whose inputs arrive in  $W_0$  via corresponding input pins. One of these registers is picked at the end of  $W_0$  by associated comparison logic as follows:

Pick L if  $P < L$  (algebraically)

Pick U if  $P > U$  and not  $< L$  (algebraically)

Otherwise, pick P if  $U \geq P \geq L$  (algebraically)

The contents of the picked register are delivered to the output (Line 1) in the next  $W_0$  (while new U, P, and L inputs arrive), unless overridden by particular logical combinations.



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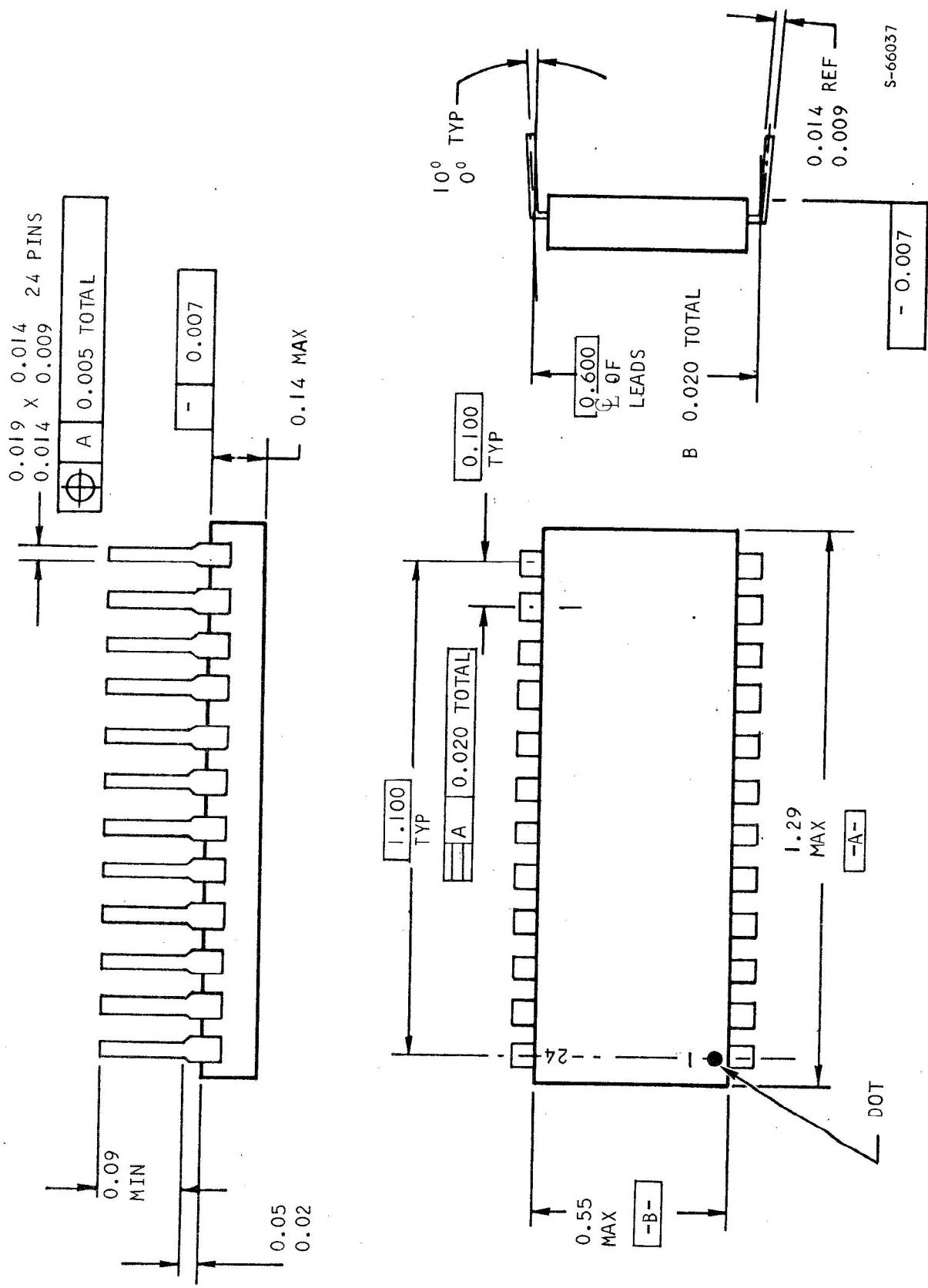
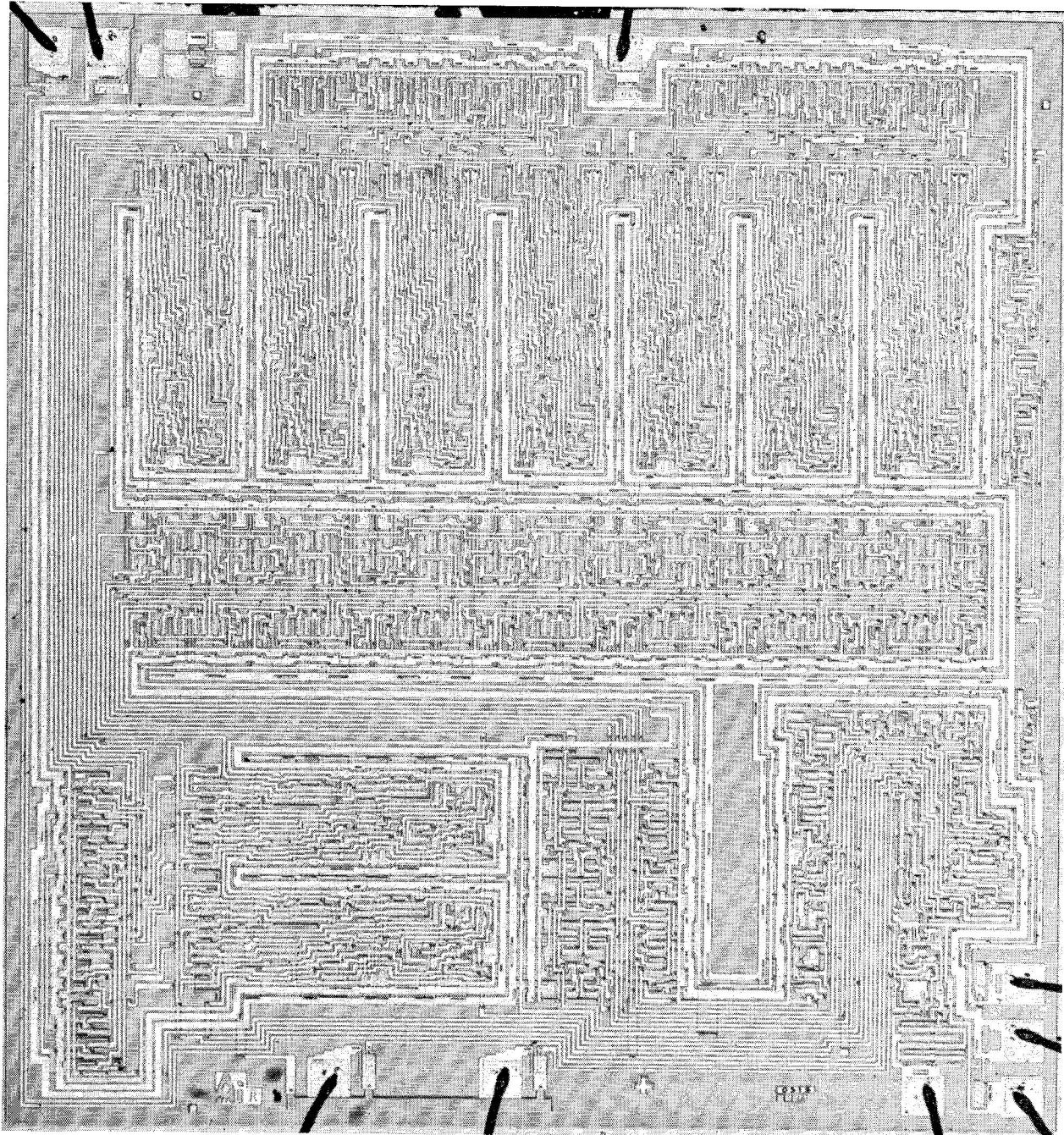


Figure I-7. PDU Package Outline



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Figure I-8. Parallel Divider Unit PN 944112, 1241 Devices



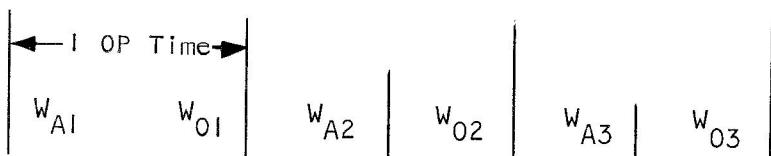
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The single logic input to the unit is the D input. It needs to be valid during T18 of the  $W_A$  word. This input is used in conjunction with the control word to determine various output combinations.

The unit consists of five outputs, two data outputs, and three logic outputs. The two data outputs are Line 1 and Line 2, and the three logic outputs are B,  $\bar{B}$ , and C. Data outputs deliver 20 bits of data every  $W_0$  word time. Logic outputs deliver a single bit of data for a complete word time ( $W_0$  for C output and  $W_A$  for B,  $\bar{B}$  output). The B logic output is true in  $W_A$  if P has been picked at the end of the immediately preceding  $W_0$ . It is always false in  $W_0$ . The  $\bar{B}$  output is the complement of B in  $W_A$  and always false in  $W_0$ . The C output is true in  $W_0$  if certain logical combinations (described below) are recognized at the end of the immediately preceding  $W_A$ . It is always false during  $W_A$ .

The following describes actions that occur in response to various control words and D input combinations. This description will refer to actions in response to the following timing.



A control word entered during  $W_{A2}$  will affect Line 1, Line 2, and C outputs during  $W_{02}$  and B and  $\bar{B}$  outputs during  $W_{A3}$ .

#### I. Input

L	M
CW	0 0 0 0 ( $W_{A2}$ )
D	1 or 0 ( $W_{A2}$ )

#### Output Action

- (a) Data entering on the P input ( $W_{02}$ ) will be delivered to Line 1 during  $W_{02}$ .
- (b) Data in the P register (entered at some previous OP) will be delivered to Line 2 during  $W_{02}$ .
- (c) If U was picked at the end of  $W_{01}$ , the C output will be set true during  $W_{02}$ .
- (d) The B and  $\bar{B}$  outputs during  $W_{A3}$  will be as previously defined.



2. Input

L M

CW 0 0 0 1 ( $w_{A2}$ )

D 1 or 0 ( $w_{A2}$ )

Output Action

- (a) The logical product of the P and U inputs ( $w_{02}$ ) will be delivered to Line 1 ( $w_{02}$ ).
- (b) The logical product of the P and L inputs ( $w_{02}$ ) will be delivered to Line 2 ( $w_{02}$ ).
- (c) The C output will be false during  $w_{02}$ .
- (d) The B and  $\bar{B}$  outputs during  $w_{A3}$  will be as previously defined.

3. Input

L M

CW 0 0 1 0 ( $w_{A2}$ )

D 1 or 0 ( $w_{A2}$ )

Output Action

- (a) The contents of the register picked at the end of  $w_{01}$  will be delivered to Line 1 during  $w_{02}$ .
- (b) The Gray code conversion (see Appendix C) of the data entering on the P input during  $w_{02}$  will be delivered to Line 2 during  $w_{02}$ .
- (c) The C output will be false during  $w_{02}$ .
- (d) The B and  $\bar{B}$  outputs during  $w_{A3}$  will be as previously defined.

4. Input

L M

CW 0 0 1 1 ( $w_{A2}$ )

D 0 ( $w_{A2}$ )



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### Output Action

- (a) The contents of the P register at the end of  $W_{01}$  will be delivered to Line 1 during  $W_{02}$  with a logic "1" in the LSB position.
- (b) Line 2 during  $W_{02}$  will contain all zeros.
- (c) The C output will be false during  $W_{02}$ .
- (d) The B and  $\bar{B}$  outputs during  $W_{A3}$  will be as previously defined.

### 5. Input

L M  
CW 0 0 1 1 ( $w_{A2}$ )  
D 1 ( $w_{A2}$ )

### Output Action

- (a) The contents of the P register at the end of  $W_{01}$  will be delivered to Line 1 during  $W_{02}$  with a logic "1" in the LSB position and also a logic "1" in the MSB position if P was picked during  $W_{01}$ .
- (b) Line 2 during  $W_{02}$  will contain all zeros.
- (c) The C output will be false during  $W_{02}$ .
- (d) The B and  $\bar{B}$  outputs during  $W_{A3}$  will be as previously defined.

### 6. Input

L M  
CW 0 1 0 0, 0 1 0 1, 0 1 1 0, 0 1 1 1, 1 0 0 0, 1 0 0 1, 1 0 1 0,  
1 0 1 1 ( $w_{A2}$ )  
D 0 ( $w_{A2}$ )

### Output Action

- (a) The contents of the picked register at the end of  $W_{01}$  will be delivered to Line 1 during  $W_{02}$ .
- (b) Line 2 during  $W_{02}$  will contain all zeros.



- (c) Line C output will be false during  $W_{02}$ .
- (d) The B and  $\bar{B}$  outputs during  $W_{A3}$  will be as previously defined.

7. Input

L M

CW 0 1 0 0, 0 1 0 1, 0 1 1 0, 0 1 1 1, 1 0 0 0, 1 0 0 1, 1 0 1 0,  
1 0 1 1 ( $w_{A2}$ )  
D I ( $w_{A2}$ )

Output Action

- (a) The contents of the picked register at the end of  $W_{01}$  will be delivered to Line 1 during  $W_{02}$ .
- (b) Line 2 during  $W_{02}$  will contain all zeros.
- (c) The C output will be true during  $W_{02}$ .
- (d) The B and  $\bar{B}$  outputs during  $W_{A3}$  will be as previously defined.

8. Input

L M

CW 1 1 0 0, 1 1 0 1, 1 1 1 0, 1 1 1 1 ( $w_{A2}$ )  
D 0 ( $w_{A2}$ )

Output Action

- (a) The contents of the picked register at the end of  $W_{01}$  will be delivered to Line 1 during  $W_{02}$  and also to the P register input during  $W_{02}$ .
- (b) The contents of the P register at the end of  $W_{01}$  will be delivered to Line 2 during  $W_{02}$ .
- (c) The C output will be false during  $W_{02}$ .
- (d) The B and  $\bar{B}$  outputs during  $W_{A3}$  will be as previously defined.

9. Input

L M

CW 1 1 0 0, 1 1 0 1, 1 1 1 0, 1 1 1 1, ( $w_{A2}$ )  
D I ( $w_{A2}$ )



### Output

- (a) The data entering the P input during  $W_{02}$  will be delivered to Line 1 during  $W_{02}$ .
- (b) The contents of the P register at the end of  $W_{01}$  will be delivered to Line 2 during  $W_{02}$ .
- (c) The C output will be false during  $W_{02}$ .
- (d) The B and  $\bar{B}$  outputs during  $W_{A3}$  will be as previously defined.

The SLF is a very useful unit when programming a variety of functions. How this unit is programmed from a mathematical function point of view, along with examples, is discussed under Software.

The inputs to the SLF are U (upper limit), P (parameter), L (lower limit), D (discrete), CW (control word),  $\phi_1$ ,  $\phi_2$ , TI8,  $W_0$ ,  $V_{DD}$ , ground. The outputs are Line 1, Line 2, C, B, and  $\bar{B}$ . Figure I-9 shows the package pin arrangements, and Figure I-10 shows the 24-pin dual in-line package outline.

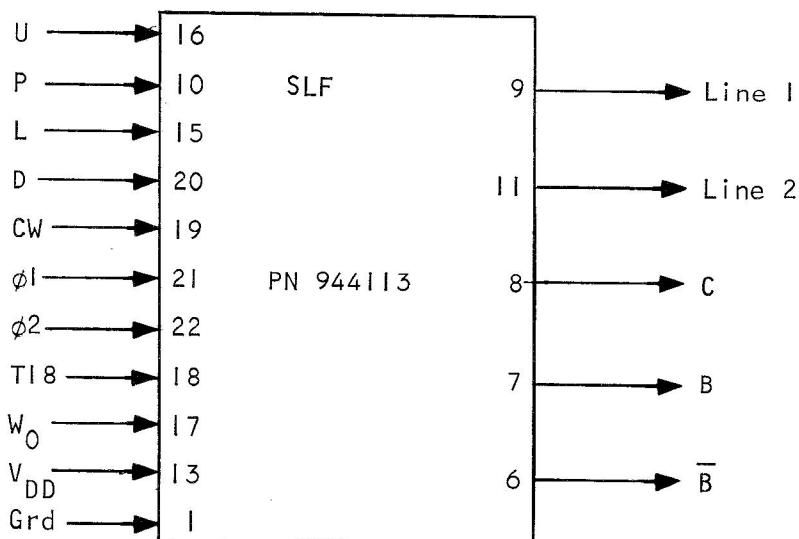


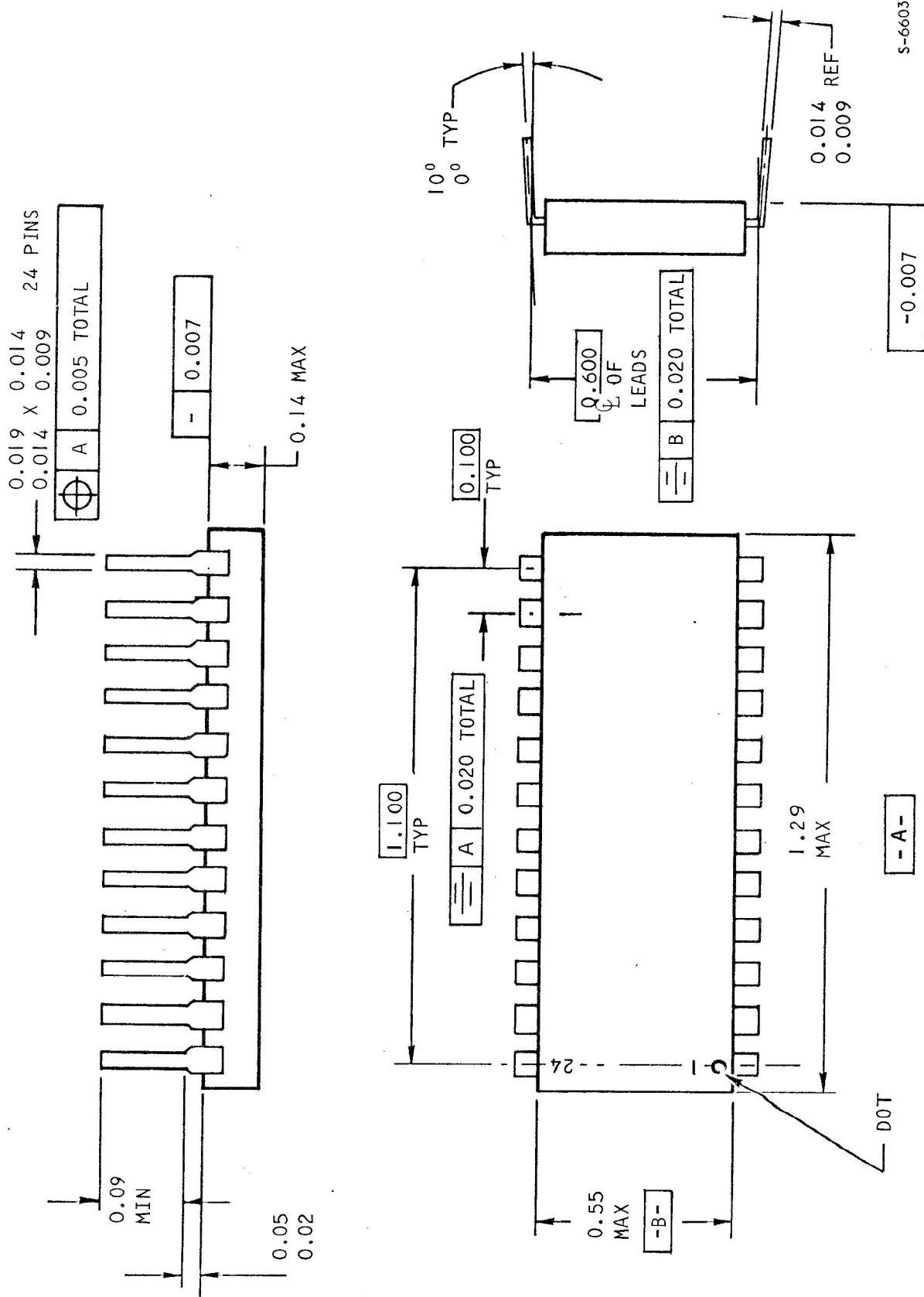
Figure I-9. SLF I/O

When using the SLF in a system, there are certain timing and propagation delay considerations. These will be discussed later under Software System and Considerations.

Electrical characteristics and logic diagrams of the SLF can be obtained from Source Control Drawing 944113.

The SLF contains 743 active MOS devices and has a chip size of 120 by 130 MILS. A photograph of an actual chip is shown in Figure I-11.

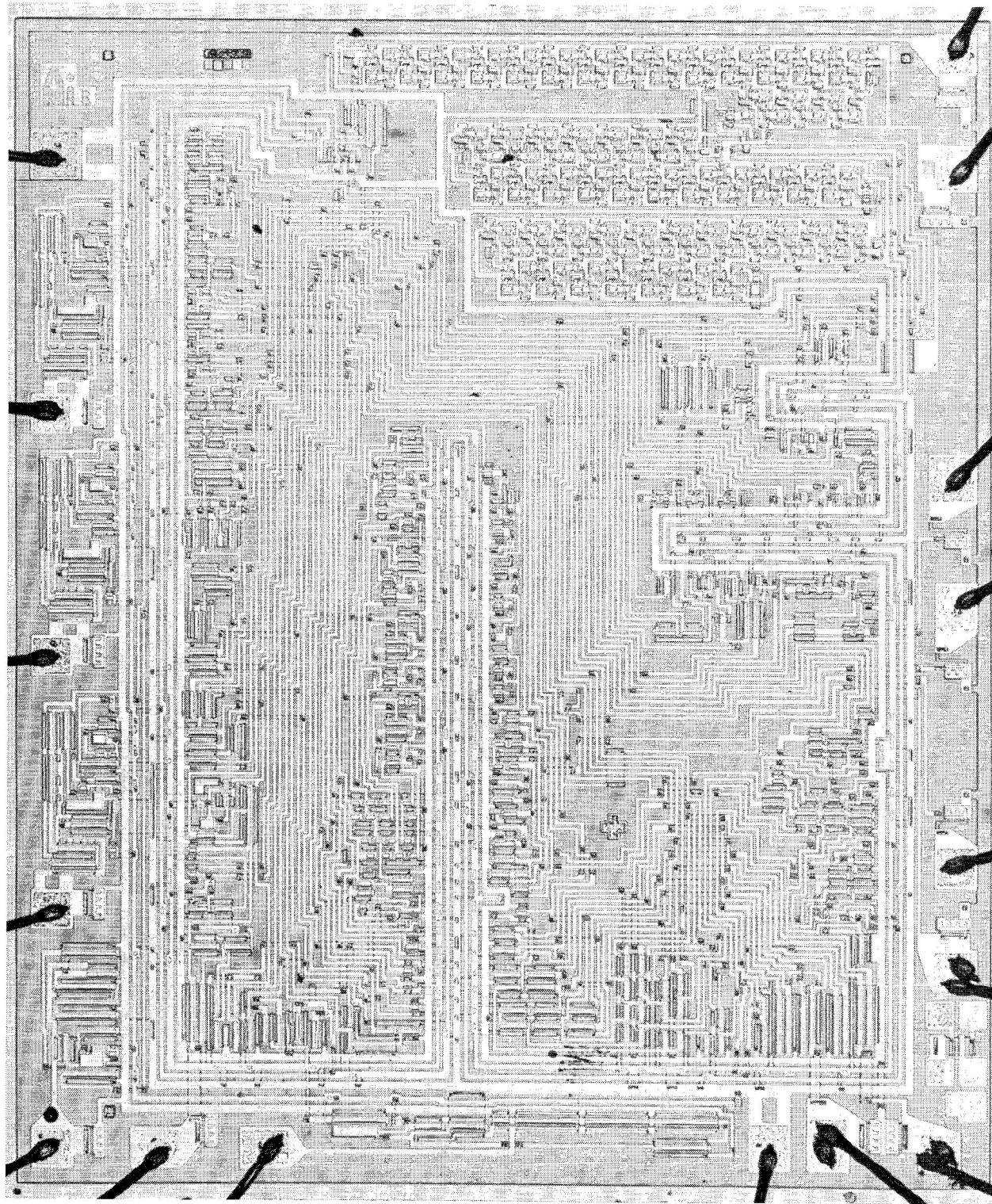




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Figure 1-10. SLF Package Outline



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Figure I-11. Special Logic Function PN 944113, 743 Devices



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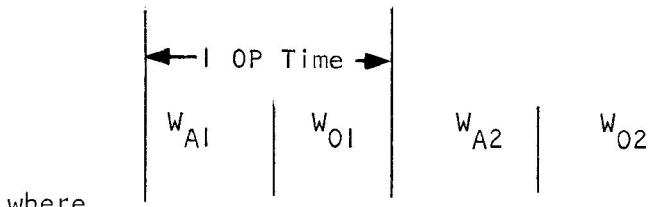
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Random Access Storage (RAS), PN 944114

The RAS operates as a 16-word random access read-write storage device. Information is shifted serially into and out of selected registers during  $W_0$ . Memory readout is nondestructive, i.e., if a register is selected to be read only, then the data are also rewritten into the selected register. The RAS accepts a control word of 5 bits during  $W_A$ . The least significant four bits of the control word specifies one of sixteen 20-bit serial registers. The contents of the selected register is shifted out to the data output serially during the next  $W_0$  and  $W_A$ . At the  $W_0$  time, information from the data input is written into the selected register if the fifth control bit is a "1." If the fifth bit is a "0," the register contents remain unaffected. An external logic input "inhibit write" is provided to inhibit writing. This will occur when the "inhibit write" input is true. The "inhibit write" should be true during  $W_0$  and false during  $W_A$ . The control selects registers according to the following configuration:

M	L	Selected Register
0	0 0 0 0	16
	0 0 0 1	1
	0 0 1 0	2
	0 0 1 1	3
	0 1 0 0	4
	0 1 0 1	5
	0 1 1 0	6
	0 1 1 1	7
	1 0 0 0	8
	1 0 0 1	9
	1 0 1 0	10
	1 0 1 1	11
	1 1 0 0	12
	1 1 0 1	13
	1 1 1 0	14
	1 1 1 1	15
0		Read
1		Read and Write





where

$W_{AI}$  = Enter control word

$W_{O1}$  = Contents of selected register from CW- $W_{AI}$  is shifted out.

= If the "write" bit is true, a new data will also be written into the selected register providing the "IW" signal is not true.

$W_{A2}$  = Contents of selected register from CW- $W_{AI}$  is shifted out.

= Enter new control card.

The inputs to the RAS are DI (data in), DW (control word), IW (inhibit write), T18,  $W_0$ ,  $\phi_1$ ,  $\phi_2$ ,  $V_{DD}$ , and ground. The only output is DO (data out). Figure I-12 shows the package pin assignment, and Figure I-13 shows the 14-pin dual in-line package outline.

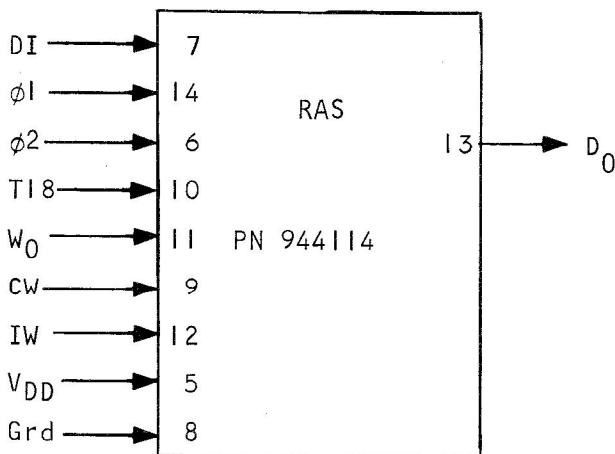


Figure I-12. RAS I/O

When using the RAS in a system, there are certain timing and propagation delay considerations. These will be discussed later in this report under Software System and Considerations.

Electrical characteristics and logic diagrams of the RAS can be obtained from Source Control Drawing 944114.



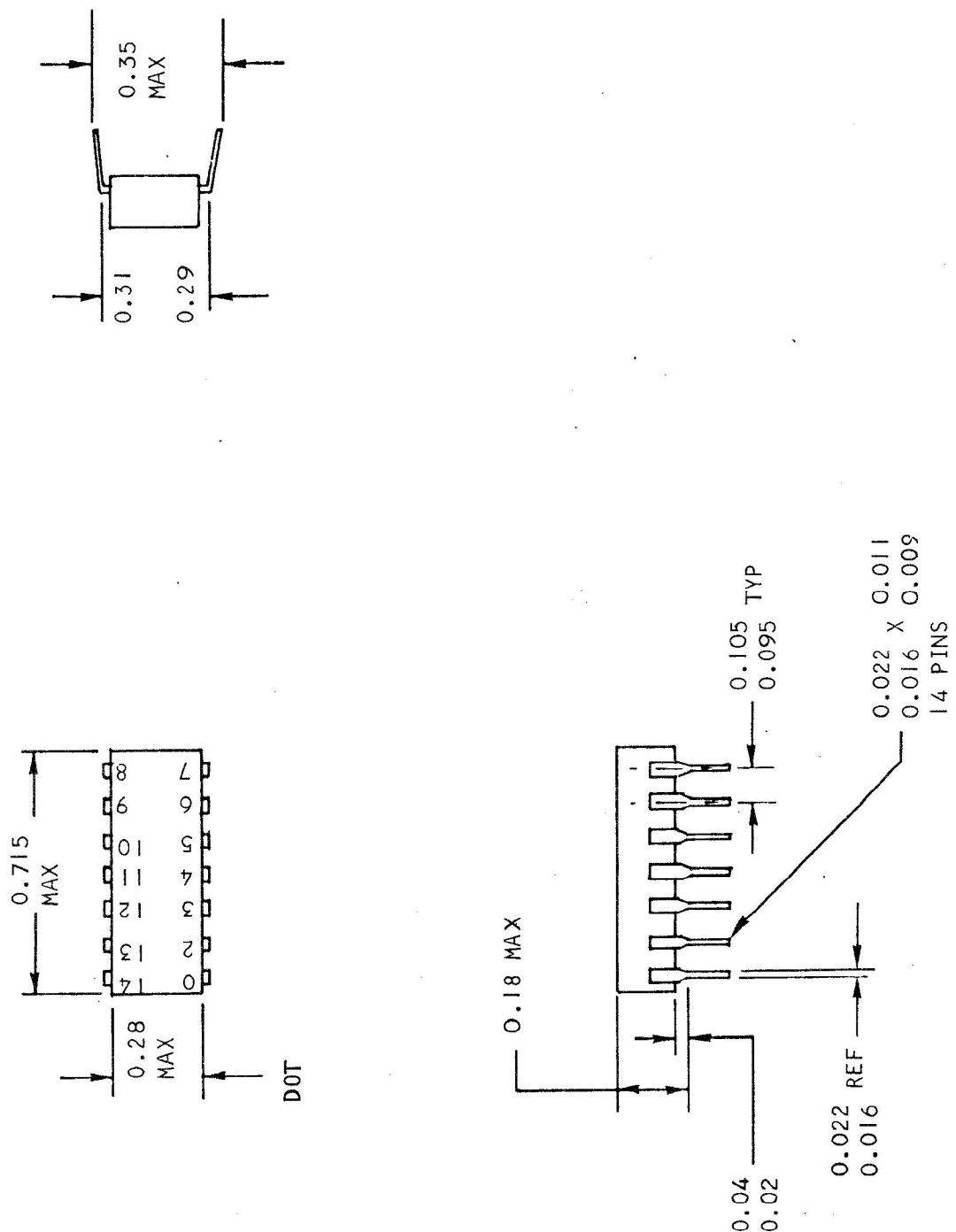


Figure 1-13. RAS Package Outline

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The RAS contains 2330 active MOS devices and has a chip size of 115 by 130 MILS. A photograph of an actual chip is shown in Figure 1-14.

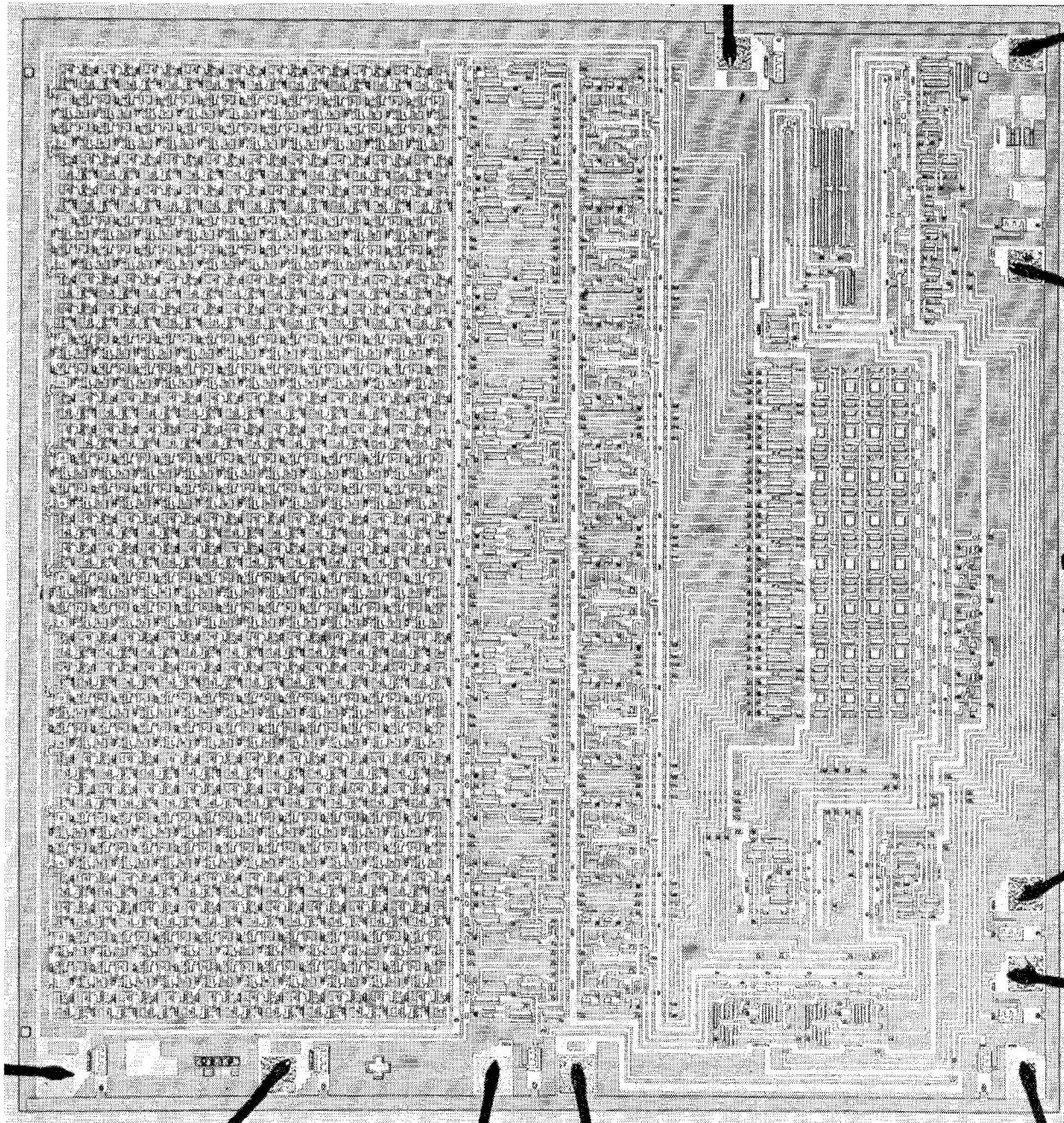
### Steering Logic (SL), PN 944118

The steering logic operates as a three-channel serial digital data multiplexer. Information is shifted serially through the device during  $W_0$ . A 15-bit control word is accepted during  $W_A$  that specifies which input or input combination is to be steered to each of three data outputs. The control word is the last 15 bits of the 20-bit control word. From the least significant end, the first four bits specifies the selection for Output 1. The next four bits specifies the selection for Output 2 and the last seven bits specifies the selection for Output 3. Specific codes are interpreted as follows:

LSB

6	7	8	9	Selected to Output 1
0	0	0	0	EXT 1
0	0	0	1	EXT 2
0	0	1	0	EXT 3
0	0	1	1	EXT 4
0	1	0	0	EXT 5
0	1	0	1	EXT 6
0	1	1	0	EXT 7
0	1	1	1	EXT 8
1	0	0	0	EXT 9
1	0	0	1	EXT 10
1	0	1	0	EXT 13
1	0	1	1	EXT 11
1	1	0	0	EXT 9 + EXT 4
1	1	0	1	EXT 10 + EXT 4
1	1	1	0	EXT 4 + EXT 8
1	1	1	1	EXT 2 - EXT 8





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Figure 1-14. Random Access Storage PN 944114, 2330 Devices



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<u>10</u>	<u>11</u>	<u>12</u>	<u>13</u>	Selected to Output 2
0	0	0	0	EXT 1
0	0	0	1	EXT 2
0	0	1	0	EXT 3
0	0	1	1	EXT 4
0	1	0	0	EXT 5
0	1	0	1	EXT 6
0	1	1	0	EXT 7
0	1	1	1	EXT 8
1	0	0	0	EXT 9
1	0	0	1	EXT 10
1	0	1	0	0.1111111111111111 ( <u>T19</u> )
1	0	1	1	EXT 11
1	1	0	0	EXT 9 + EXT 4
1	1	0	1	EXT 10 + EXT 4
1	1	1	0	EXT 4 + EXT 8
1	1	1	1	EXT 2 - EXT 8
<u>14</u>	<u>15</u>	<u>16</u>	<u>17</u>	Selected to Output 3
0	0	0	0	EXT 1
0	0	0	1	EXT 2
0	0	1	0	EXT 3
0	0	1	1	EXT 4
0	1	0	0	EXT 5
0	1	0	1	EXT 6
0	1	1	0	EXT 7
0	1	1	1	EXT 9
1	0	0	0	EXT $\Sigma_1$
1	0	0	1	EXT $\Sigma_2$
1	0	1	0	EXT 11
1	0	1	1	EXT 2 + EXT 4
1	1	0	0	EXT 2 - EXT 8
1	1	0	1	EXT 2 - EXT 4
1	1	1	0	EXT 4 - EXT 2
1	1	1	1	EXT 4 + EXT 8



18

$$| \qquad \text{EXT } 12 + \text{EXT } 8 = \Sigma_1$$

		MSB
19	20	
0	0	$\Sigma_1 + \text{EXT } 2 = \Sigma_2$
0	1	$\Sigma_1 - \text{EXT } 2 = \Sigma_2$
1	0	$\Sigma_1 + \text{EXT } 4 = \Sigma_2$
1	1	$\Sigma_1 - \text{EXT } 4 = \Sigma_2$

The inputs to the steering are EXT 1 through EXT 13 (13 data inputs), T18,  $W_0$ , CW,  $\phi_1$ ,  $\phi_2$ ,  $V_{DD}$  (-14V), and ground. Four outputs are provided, three data outputs M/D (Output 1), D/Z (Output 2), STOR (Output 3), and one control word output. The CW output contains the input CW delayed by 15 bits. Figure I-15 shows the package pin assignments for the SL, and Figure I-16 shows the 24-pin dual in-line package outline.

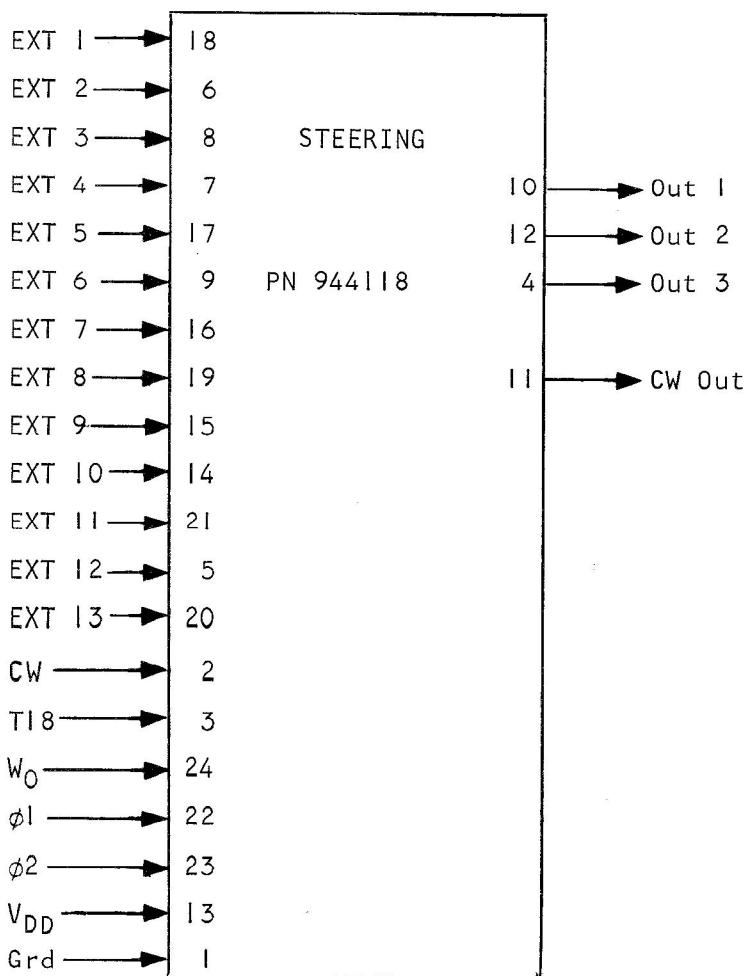
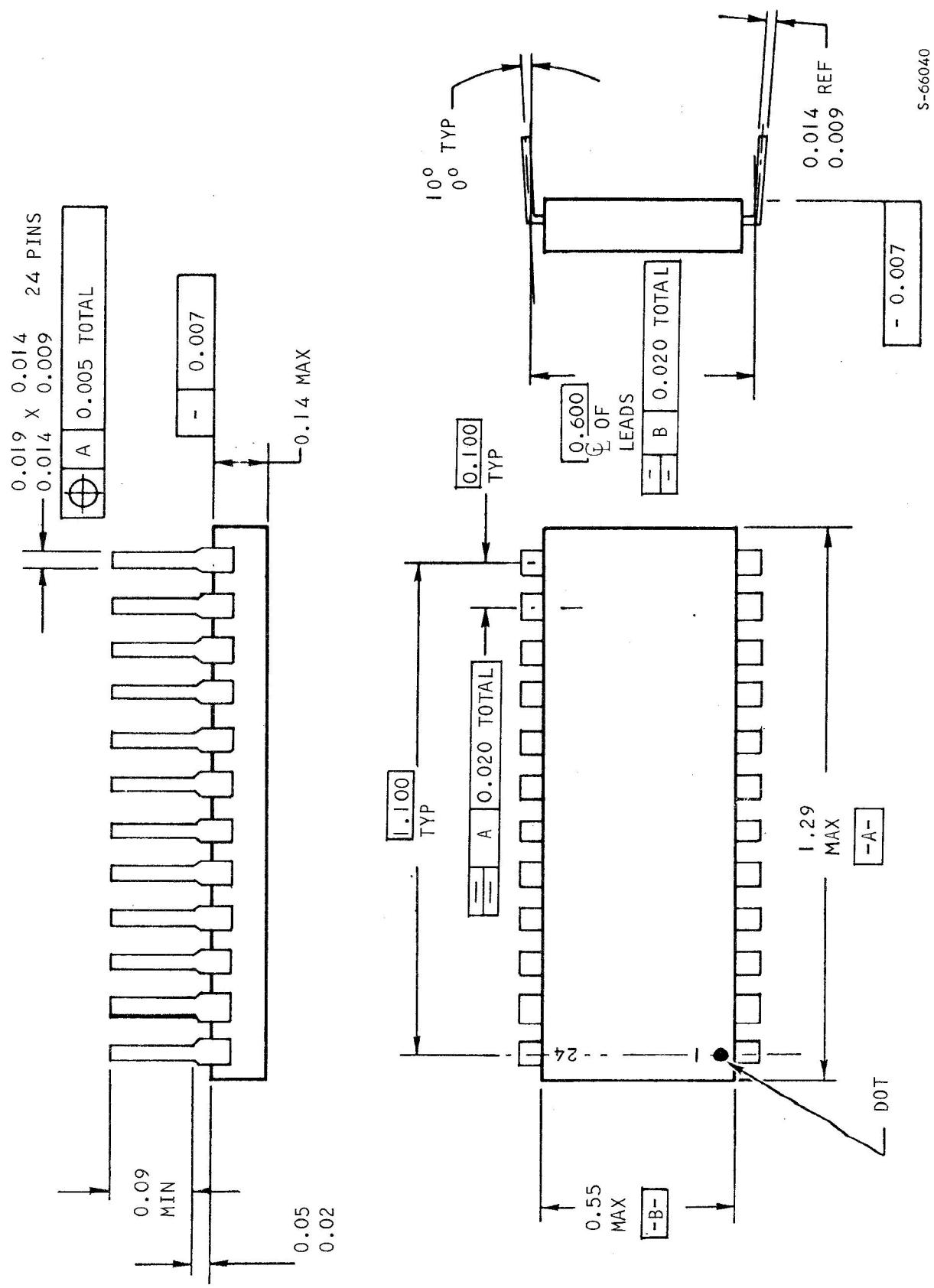


Figure I-15. SL I/O



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When using the SL in a system, there are certain timing and propagation delay considerations. These will be discussed later under Software System and Considerations.

Electrical characteristics and logic diagrams of the SL can be obtained from Source Control Drawing 944118.

The SL contains 771 active MOS devices and has a chip size of 128 by 133 MILS. A photograph of an actual chip is shown in Figure I-17.

#### Read-Only Memory (ROM), PN 944125

The ROM operates as a 2560-bit random access/sequential access device. It internally stores fixed patterns of 128 words of 20 bit length for serial readout. The patterns are specified by the user. The format for the patterns is described under Computer Aids. The ROM has provision to accept a 20-bit serial binary word address. The first seven bits indicates which of the 128 words is to be accessed, and the next three bits specifies, by manufacture mask decoding, which ROM out of a possible eight ROM group should have its output enabled. (The present hardware limit for a ROM group is four. This is due to limited output buffer drive capability.)

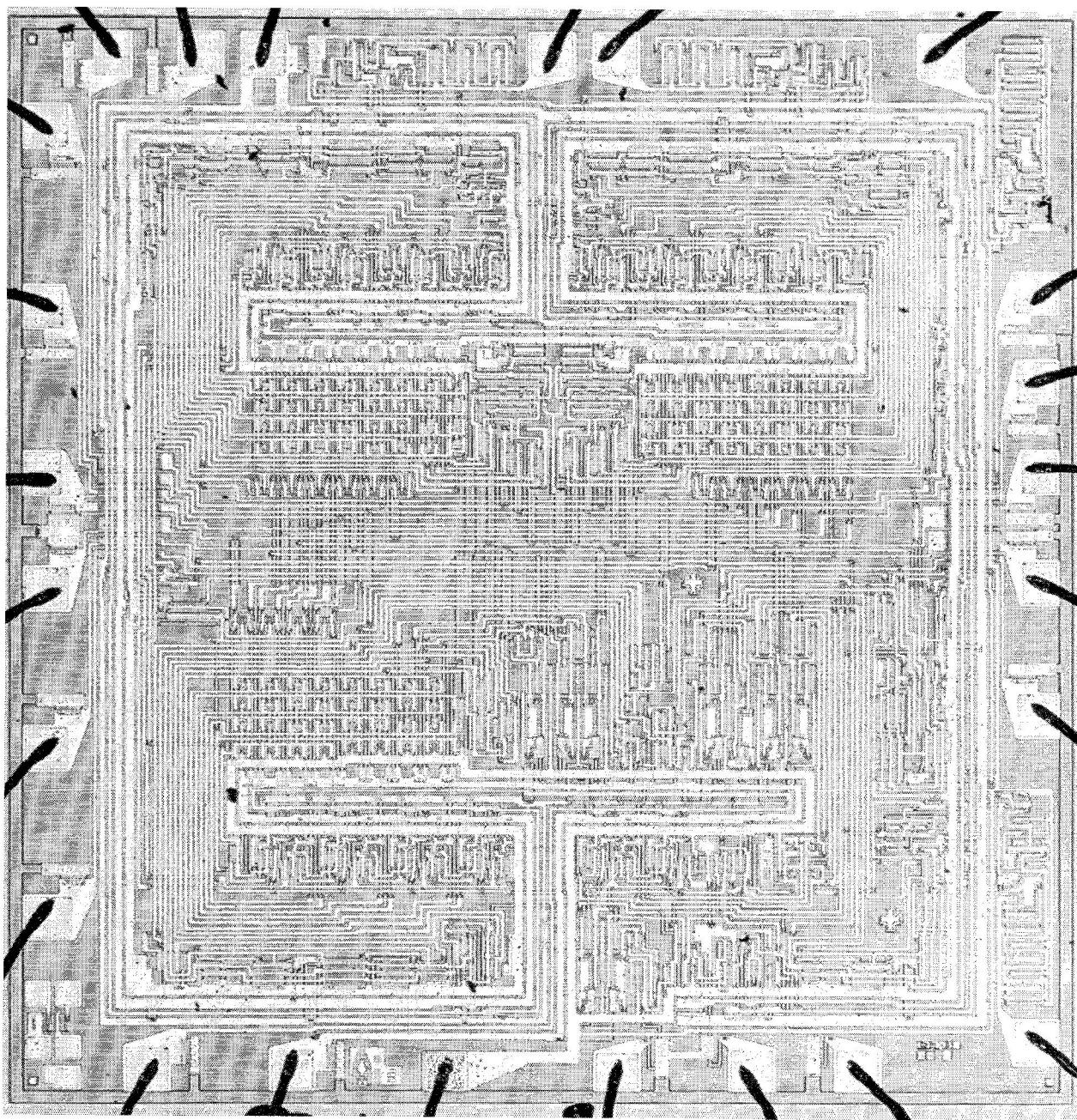
The address management is accomplished by a register counter contained within the ROM. This counter has the following capability: (1) resettable, (2) steppable such that the memory can be sequenced through the 128-word field, (3) accepts a retain address command and holds the present address, and (4) accepts a numerical input for independent address modifying or loading. To accomplish the above address management, six logic inputs (reset (R), retain, increment, load, add, sub) and one address data input are provided. The logic of their operation is as follows:

The address field is defined as follows: the first seven LSB's will select one of 128 20-bit words. The next three will be used to select one of eight ROM's, the remaining ten will be zero. The three-bit select field will determine, by mask decoding, which chip's (ROM) output is to be enabled. ROM's that are not enabled by the chip select field have disabled their outputs. The access period ( $W_{ACC}$ ) is defined as the period during which none of the following is at a logical "1": retain, increment, load, add, subtract.

The reset, increments, load, and retain inputs are mutually exclusive.

The R input, on its negative transition, resets the bits of the address register to all zeros. If the R signal occurs during  $W_{ACC}$ , it does not affect that data. The next state of the address counter is all zeros. The R input will be coincident with T18. The R input will override retain, increment, load, add, and sub inputs. The retain input holds the current address of the counter. The nature of this signal will be such that it will be a logical "1" during the count interval ( $\overline{W_{ACC}}$ ).





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Figure I-17. Steering Logic PN 944118, 771 Devices



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The increment input will be a 20-bit logic level. If this is a logical "1," the address counter is increased by one, and the newly addressed data is shifted out during the next  $W_{ACC}$ . The load input will be a logical "1" when a new address is to be loaded into the address register. The new address will appear on the address input coincidentally with the load signal. When the add input is a logical "1," the address input will be added to the contents of the previous address. When the sub input is a logical "1," the address input will be subtracted from the contents of the previous address. The address input will contain data to be used as commanded by the logical inputs. Valid inputs will appear during the nonaccess ( $\overline{W}_{ACC}$ ) period.

The reset, increment, load, and retain inputs are mutually exclusive. The add and subtract inputs are mutually exclusive. The reset, increment, load, or retain inputs override the add and subtract inputs.

The ROM has two outputs, data output and parity error. The data output contains the 20-bit serial data word addressed by the address register. The output device is constructed such that it may be wire or'ed with the outputs of associated ROM's, there being normally only one out of a group of wire or'ed ROM's which is enabled.

The parity error output is from a device that changes state for every occurrence of state change in the enabled data output of an ROM. During  $T_0$  of every 20-bit period, the parity device will be set for a "1" output and, if there is an odd number of state changes on the data line, the state of the parity device during phase one (negative transition) of  $T_{19}$  should go to "0" (negative transition) and will last until phase of  $T_0$ .

All parity devices in an associated group of ROM's are reading the same signal, i.e., the wire or'ed data output signal, as the point of takeoff for parity on a chip is the output pad. The parity error outputs in an associated group of ROM's will be wire or'ed together. If the retain, increment, load, add, or subtract inputs is a logical "1," the parity error output is reset to "0" during  $W_{ACC}$  at  $\phi_1$  of  $T_0$  and lasts to the next  $\phi_1$  of  $T_0$ .

The F-14A CADC uses only the increment address capability of the ROM. This is accomplished by grounding all data and address inputs except increment. Increment is then connected to the appropriate signal to control the sequential addressing of the ROM. Discussions under Software Executive Control will consider the appropriate nature of this signal.

Figure I-18 shows the pin assignments for the ROM, and Figure I-19 shows the 14-pin dual in-line package outline.

When using the ROM in a system, there are certain timing and propagation delay considerations. These will be discussed later under Software System and Considerations.

Electrical characteristics and logic diagrams of the ROM can be obtained from Source Control Drawing 944125.



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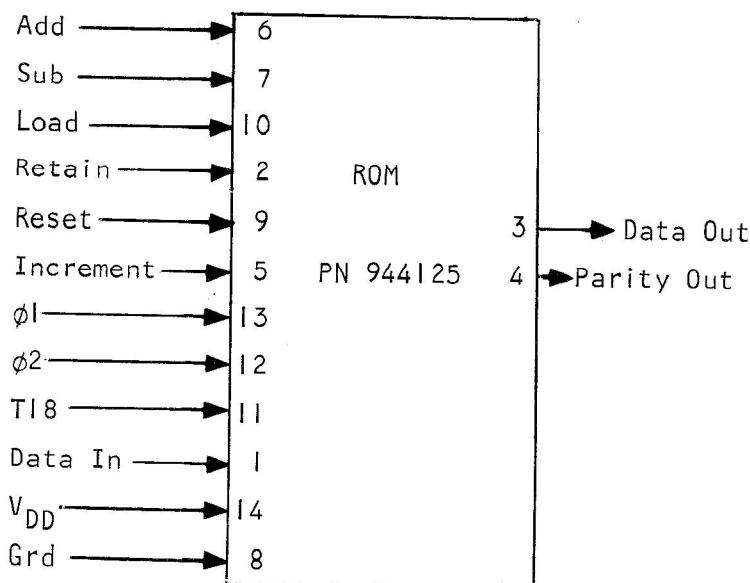


Figure I-18. ROM I/O

The ROM contains 3268 active MOS devices and has a chip size of 143 by 150 MILS. A photograph of an actual chip is shown in Figure I-20.

#### HARDWARE SYSTEM AND CONSIDERATIONS

The F-14A CADC processor uses a total of 28 circuits. The breakdown is as follows:

- 1 -- PMU
- 1 -- PDU
- 1 -- SLF
- 3 -- RAS's
- 3 -- SL's
- 19 -- ROM's -- 9 Program Control  
6 Fixed Data Storage  
4 Executive Control

Figure I-21 shows the interconnection of the data and control word paths between the circuits. The system has been divided into three modules, each module identified by its arithmetic unit. The modules are as follows:



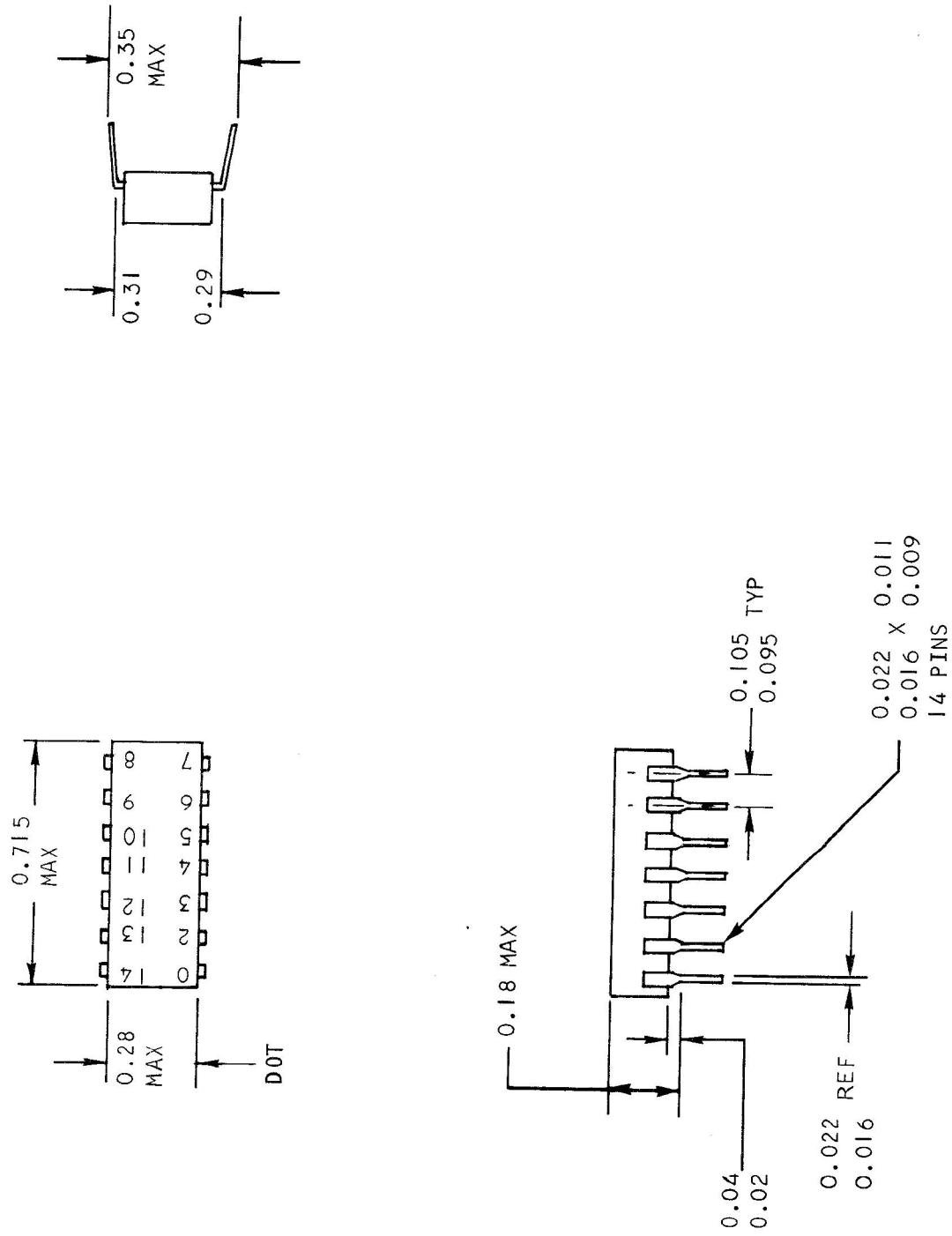


Figure I-19. ROM Package Outline



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