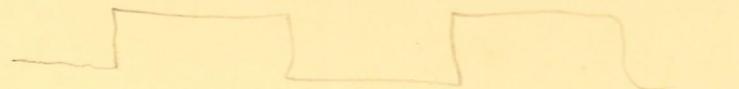
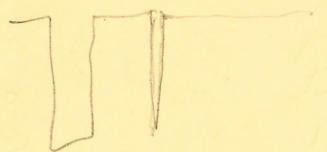
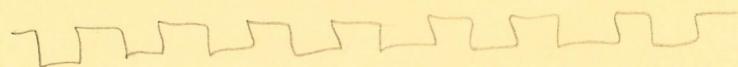
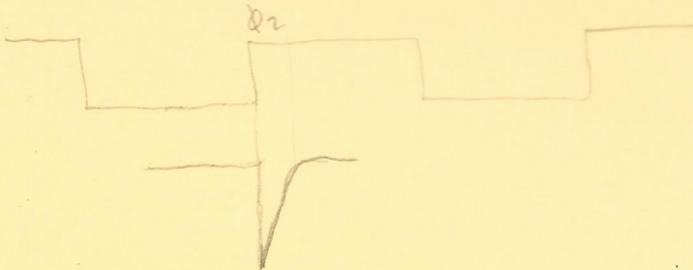


w_0



\bar{w}_0
($T^2 L$)



'o' following a 'I'

944114
RAS

4.0 LOGICAL SPECIFICATION

4.1 DEFINITION OF SYSTEM TERMS

BIT TIME: ONE COMPLETE CLOCK PERIOD, 2.66 μ SEC AT 375 KHZ.

SEE FIGURE 2.

WORD TIME: 20 CONSECUTIVE BIT TIMES (t_0 THROUGH t_{19}). THERE ARE TWO TYPES OF "WORDS".

IN W_A , THE PARALLEL ARITHMETICAL ALGORITHMS OPERATE, AND CONTROL WORDS ARE SHIFTED INTO THE UNITS (SERIALLY).

IN W_0 , COMPUTATIONAL INPUTS AND OUTPUTS ARE SHIFTED SERIALLY AMONG THE UNITS.

THESE WORDS ALTERNATE, AND ARE OF EQUAL DURATION; i.e., THEY ARE COMPLEMENTARY.

WORD MARK: A SIGNAL COINCIDENT WITH t_{18} OF EVERY WORD TIME.

OPERATION ("Op") TIME: TWO CONSECUTIVE WORD TIMES (W_A AND W_0).

FRAME MARK: FINAL BIT TIME OF THE FINAL Op.

WORD LENGTH IS 20 BITS. FOR DATA WORDS THIS IS NORMALLY SIGN AND 19 BITS.

DATA IS SHIFTED LSB FIRST. TWO'S COMPLEMENT REPRESENTATION IS USED FOR NEGATIVE NUMBERS. DURING BIT TIME t_0 , INFORMATION IN THE COMPUTER REGISTERS IS "PROPERLY" ORIENTED; i.e., ALL THE BITS OF A DATA WORD ARE CONTAINED IN PROPERLY CORRESPONDING REGISTER POSITIONS. CONTROL WORDS ARE SHIFTED INTO THE LOGIC CHIPS FROM READ-ONLY MEMORIES (ROM'S) SERIALLY DURING W_A OF EVERY Op, AND THEREBY SPECIFY VARIOUS DETAILS OF THE PRESENT AND SUBSEQUENT OPERATIONS. MEANINGFUL DATA TRANSFERS INTO AND OUT OF THE LOGIC CHIPS AND REGISTERS OCCUR DURING W_0 OF EVERY Op.

4.2 GENERAL DESCRIPTION

RAS SHALL OPERATE AS A 16 WORD RANDOM ACCESS READ-WRITE STORAGE DEVICE. INFORMATION SHALL BE SHIFTED INTO AND OUT OF SELECTED REGISTERS SERIALLY DURING W_0 .



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MEMORY READOUT SHALL BE NONDESTRUCTIVE. FIGURE 3 IS A SUGGESTED BLOCK DIAGRAM FOR PERFORMING THIS FUNCTION.

4.3 CONTROL WORD

THE UNIT SHALL ACCEPT A CONTROL WORD OF 5 BITS DURING W_A AS DESCRIBED FURTHER IN 4.5.1. THIS CONTROL WORD WILL SPECIFY DETAILS OF THE OPERATION AS DESCRIBED THROUGHOUT THIS SPECIFICATION. APPROPRIATE HOLDING AND DECODING LOGIC SHALL BE PROVIDED TO ACCOMPLISH THESE FUNCTIONS.

4.4 INPUTS AND OUTPUTS

PROVISION SHALL BE MADE FOR ACCEPTING OTHER ELECTRICAL AND LOGICAL INPUTS AS FOLLOWS: PHASE 1 AND PHASE 2 CLOCKS, V_{DD} , GROUND, A W_0 SIGNAL (20 CLOCK PERIODS LONG), A WORD MARK (t_{18}), DATA INPUT AND ONE EXTERNAL LOGIC INPUT. THE OUTPUT SHALL BE PROVIDED AS DESCRIBED IN PARAGRAPHS 4.5.1. THIS OUTPUT IS REFERRED TO AS "DATA".

4.5 LOGIC FUNCTIONS TO BE IMPLEMENTED

4.5.1 THE CONTROL WORD WILL CONTAIN 5 BITS. THESE WILL BE THE FIRST FIVE BITS OF A 20 BIT CONTROL WORD DELAYED 15 BITS. IT WILL ARRIVE ONLY DURING W_A . THE LEAST SIGNIFICANT FOUR BITS OF THE CONTROL WORD WILL SPECIFY ONE OF SIXTEEN 20-BIT SERIAL SHIFT REGISTERS. THE CONTENTS OF THE SELECTED REGISTER SHALL BE SHIFTED OUT TO THE "DATA" OUTPUT SERIALLY (LSB FIRST) DURING THE NEXT W_0 AND W_A . AT THE W_0 TIME, INFORMATION FROM DATA INPUT SHALL BE WRITTEN INTO THE SELECTED REGISTER IF THE FIFTH CONTROL BIT IS A "ONE". IF THE FIFTH CONTROL BIT IS "ZERO", THE REGISTER'S CONTENTS SHALL REMAIN UNAFFECTED. AN EXTERNAL LOGIC INPUT "INHIBIT WRITE" SHALL INHIBIT WRITING WHEN ACTIVE. IT WILL BE ACTIVE DURING THE W_0 PERIOD AND ZERO DURING THE W_0 PERIOD. THE CONTROL WORD SELECTS REGISTERS ACCORDING TO THE FOLLOWING CONFIGURATION:



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M L
S S
B B

5 4 3 2 1

0 0 0 0	SELECT STORAGE REGISTER NO.	16
0 0 0 1	" " "	1
0 0 1 0	" " "	2
0 0 1 1	" " "	3
0 1 0 0	" " "	4
0 1 0 1	" " "	5
0 1 1 0	" " "	6
0 1 1 1	" " "	7
1 0 0 0	" " "	8
1 0 0 1	" " "	9
1 0 1 0	" " "	10
1 0 1 1	" " "	11
1 1 0 0	" " "	12
1 1 0 1	" " "	13
1 1 1 0	" " "	14
1 1 1 1	" " "	15

0 DO NOT WRITE INTO RAS

1 WRITE INTO RAS

4.6 THE LOGIC DIAGRAM IN FIGURE 4 IS INCLUDED AS A SUPPLEMENT TO THE WRITTEN SPECIFICATION. IT HAS NOT BEEN CHECKED BY SIMULATION AND MAY CONTAIN DETAIL LOGIC ERRORS. REFER TO SPECIFICATION.

4.7 SYSTEM CONSIDERATIONS

THE RAS WILL BE TYPICALLY CONNECTED IN THE SYSTEM AS SHOWN IN FIGURE. THE CONTROL WORD WILL ORIGINATE IN AN ROM AND WILL BE DELAYED 15 BITS THROUGH THE STEERING CIRCUIT BEFORE ENTERING THE RAS. THE DATA INPUT WILL COME FROM A STEERING CIRCUIT OUTPUT. THE ORIGINATOR OF THE DATA WILL BE ONE OF THE FOLLOWING: MULTIPLIER, DIVIDER, SLF, ROM, RAS. THE DATA OUTPUT WILL FEED INTO A STEERING CIRCUIT. ALL TIMING SIGNALS WILL BE GENERATED FROM THE SYSTEM TIMING GENERATOR. OUTPUT DRIVE CAPABILITY IS DISCUSSED IN PARAGRAPH 4.8.5.



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4.7.1 PROPAGATION DELAYS

TO INSURE PROPER INTERFACE OF THIS CIRCUIT WITH THE OTHERS IN THE SYSTEM, THE FOLLOWING PROPAGATION DELAY TIMES MUST BE MET. ALL TIMES ARE MAXIMUM AND ARE MEASURED FROM THE 90% LOGICAL "1" LEVEL OF THE CLOCK TO THE 90% LEVEL OF THE SIGNAL.

<u>FROM</u>	<u>TO</u>	<u>TIME (NS)</u>
DATA INPUT	SELECTED REGISTER	200
SELECTED REGISTER	DATA OUT	250 (UNDER CONDITIONS OF PARA. 4.8.5)

ALL DATA OUTPUTS SHALL BE CHANGED ON THE NEGATIVE TRANSITION OF THE PHASE I CLOCK.

4.7.2 THE ABOVE CALCULATED WORST CASE PROPAGATION DELAYS SHALL BE SUBMITTED TO AIRESearch FOR APPROVAL NO LATER THAN 45 DAYS AFTER AWARD OF CONTRACT.



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SCALE	REV	SHEET 12

4.8 ELECTRICAL CHARACTERISTICS

THE ELECTRICAL CHARACTERISTICS SHALL APPLY AT ROOM AMBIENT TEMPERATURE.

4.8.1 POWER SUPPLIES: THE INPUT POWER SUPPLY CHARACTERISTICS ARE DEFINED BELOW:

$$V_{SS} = 0 \text{ V}$$

0.0 VDC (GROUND POTENTIAL ABOUT WHICH V_{SS} AND V_{DD} ARE REFERENCED)

$$V_{DD} = -14.0 \pm 1.0 \text{ V}$$

$$V_{\phi} = -28.5 \pm 1.5 \text{ VDC}$$

4.8.2 POWER DISSIPATION:

4.8.2.1 CALCULATED POWER: THE DC POWER DISSIPATION SHALL AT -55°C AND $+125^{\circ}\text{C}$ BE CALCULATED FOR THE DEVICE COVERED BY THIS SPECIFICATION. THE CALCULATED VALUE SHALL BE SUBMITTED TO AIRESEARCH WITHIN 45 DAYS AFTER AWARD OF CONTRACT.

4.8.2.2 MEASURED POWER: THE DC POWER DISSIPATION AT -55°C AND $+125^{\circ}\text{C}$ OF THIS DEVICE SHALL NOT EXCEED THE CALCULATED VALUE BY MORE THAN 15 PERCENT.

4.8.3 CLOCK CHARACTERISTICS: THE CLOCK CHARACTERISTICS ARE DEFINED IN FIGURE 2 OF THIS SPECIFICATION.

4.8.4 LOGIC LEVELS: THE MOS INPUT AND OUTPUT LOGIC LEVELS ARE DEFINED IN THE MATRIX BELOW:

	(MIN)	(MAX)
INPUT LOGIC "0"	-3.0 V	0.0 V
INPUT LOGIC "1"	V_{DD}	-9.0 V
OUTPUT LOGIC "0"	-2.0 V	0.0 V
OUTPUT LOGIC "1"	V_{DD}	-10.0 V

W_0 , t_{18} , FRAME MARK AND DISCRETE INPUT LOGIC LEVELS ARE DEFINED IN THE MATRIX BELOW:

	(MIN)	(MAX)
INPUT LOGIC "0"	-0.6 V	0.0 V
INPUT LOGIC "1"	-15.4 V	-12.6 V



4.8.5 OUTPUT DRIVE CAPABILITY: EACH OUTPUT SHALL BE CAPABLE OF DRIVING A LOAD TO GROUND OF 75.0 KOHMS RESISTIVE IN PARALLEL WITH A 10 PF CAPACITOR PLUS A CAPACITOR EQUAL TO FOUR TIMES THE MAXIMUM INPUT CAPACITANCE ON ANY SINGLE INPUT (EXCEPT POWER, CLOCK AND TIMING INPUTS) FOR ANY OF THE FOLLOWING CIRCUITS (P/N 944125, P/N 944111, P/N 944112, P/N 944113, P/N 944114, P/N 944118). THE CALCULATED CAPACITANCE LOAD AT -55°C AND +125°C PER ABOVE SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.8.6 INPUT LOADING

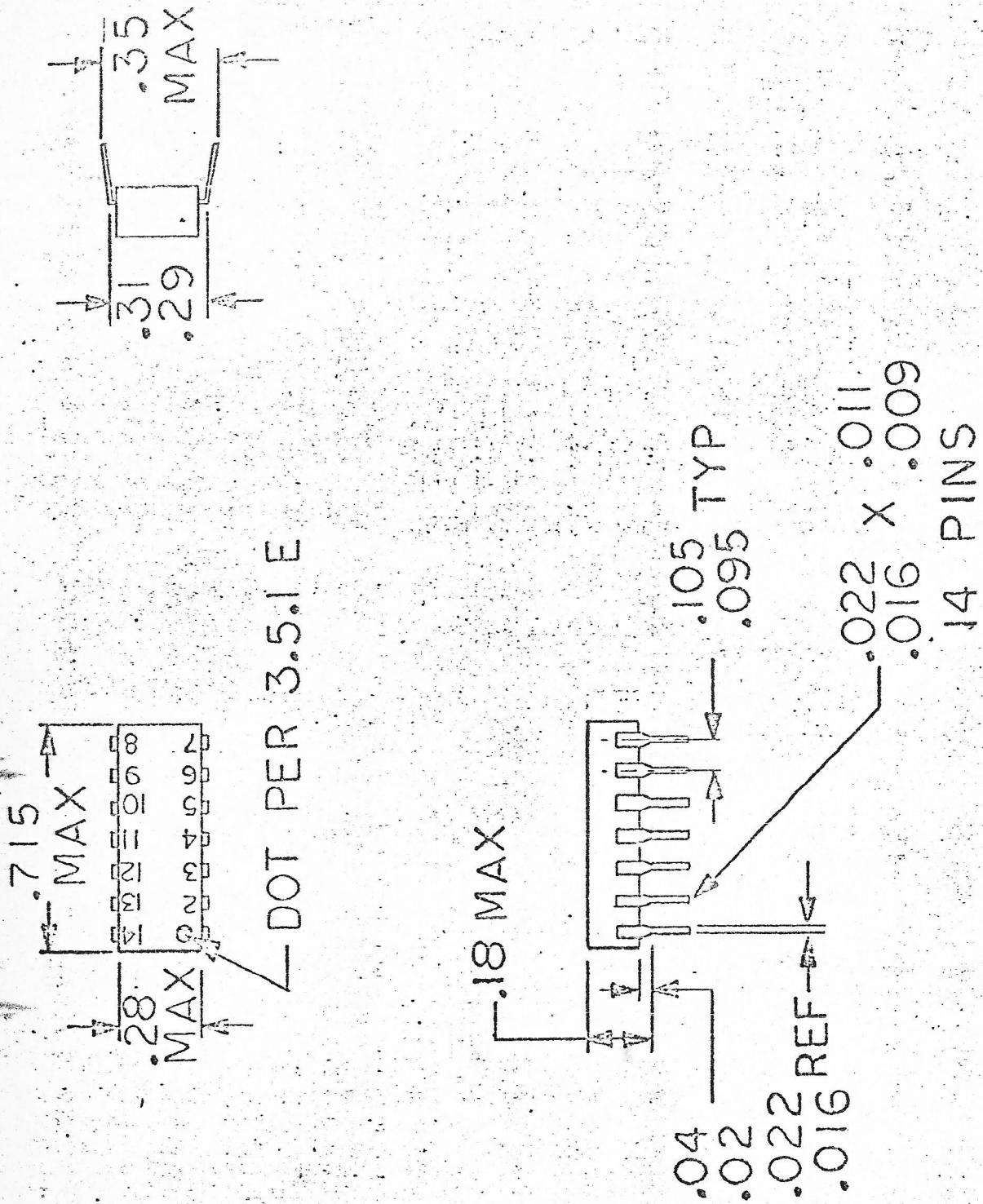
4.8.6.1 TIMING AND LOGIC INPUTS: THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL TIMING AND LOGIC INPUTS (EXCEPTCLOCKS ϕ_1 AND ϕ_2) SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.8.6.2 THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL CLOCK INPUTS (ϕ_1 AND ϕ_2) SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.8.6.3 DATA INPUTS: THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL DATA INPUTS SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

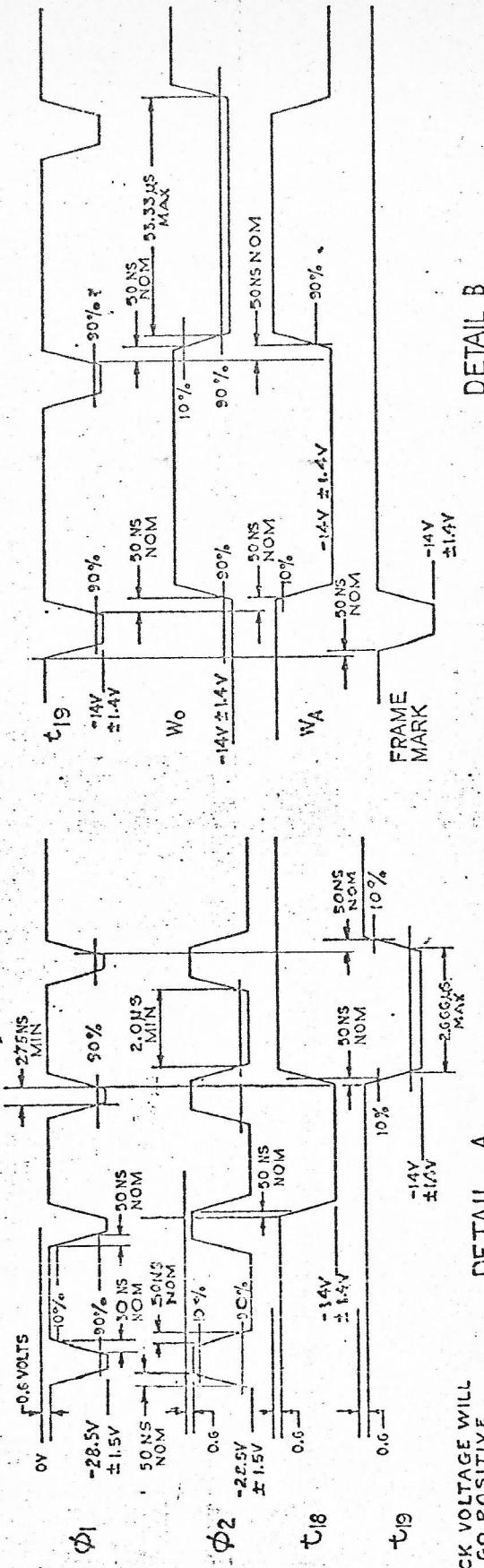
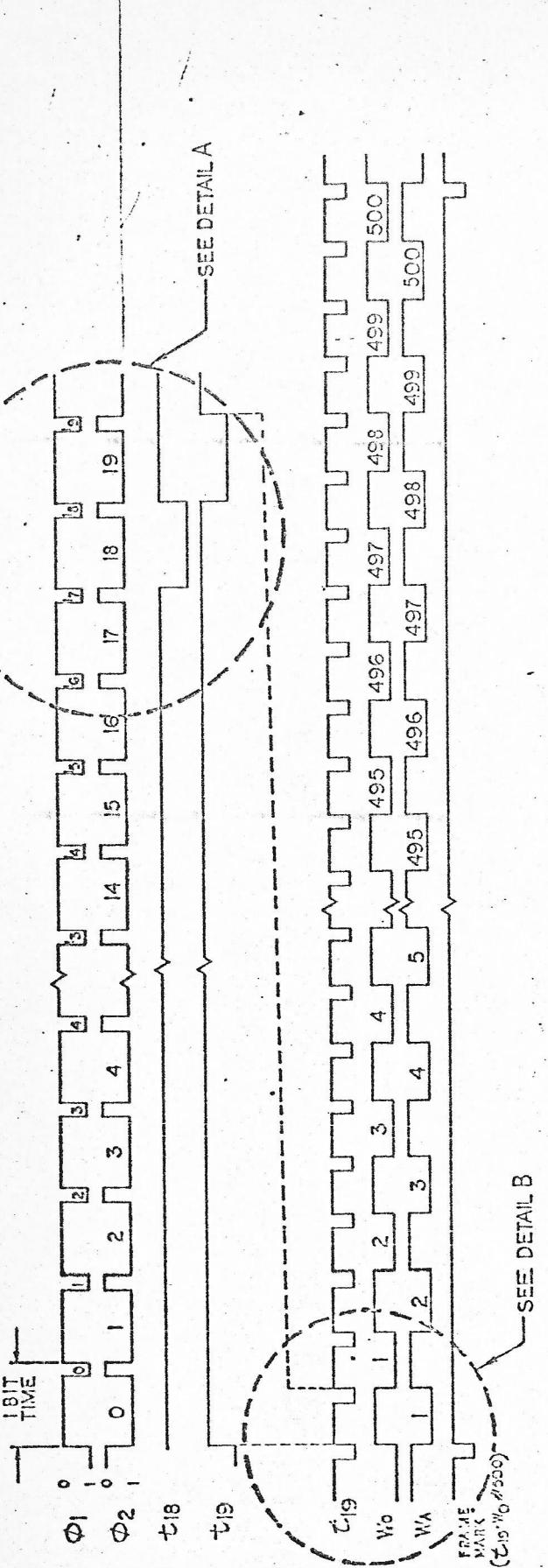


FIGURE 1 PACKAGE DRAWING



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DETAIL A

DETAIL B

FIGURE 2 a TIMING DIAGRAM

1. CLOCK VOLTAGE WILL
NOT GO POSITIVE.
2. MAX OVERLAP Φ_1 AND Φ_2
VOLTAGE IS 3.0 VOLTS

NOTES:



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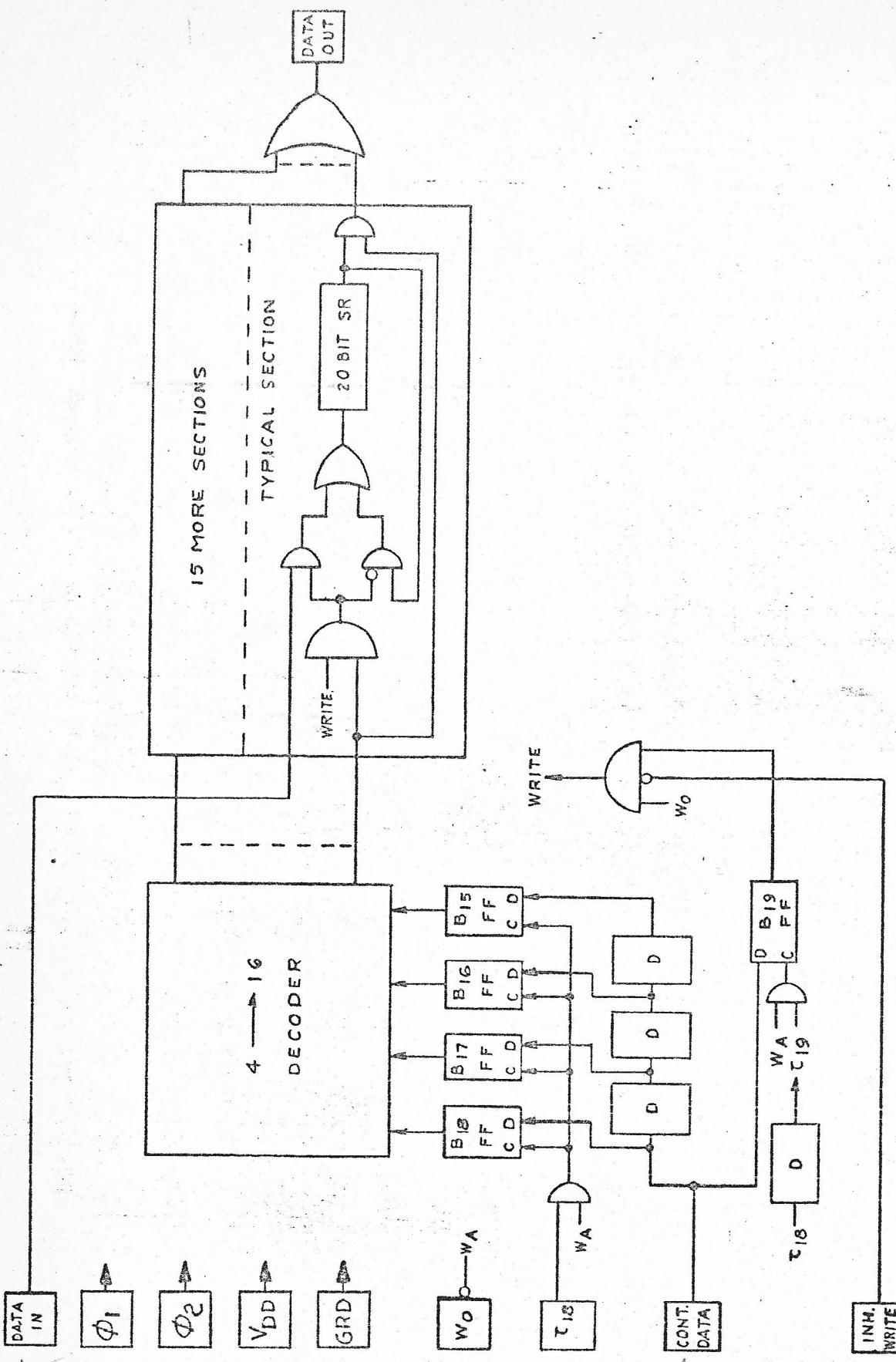
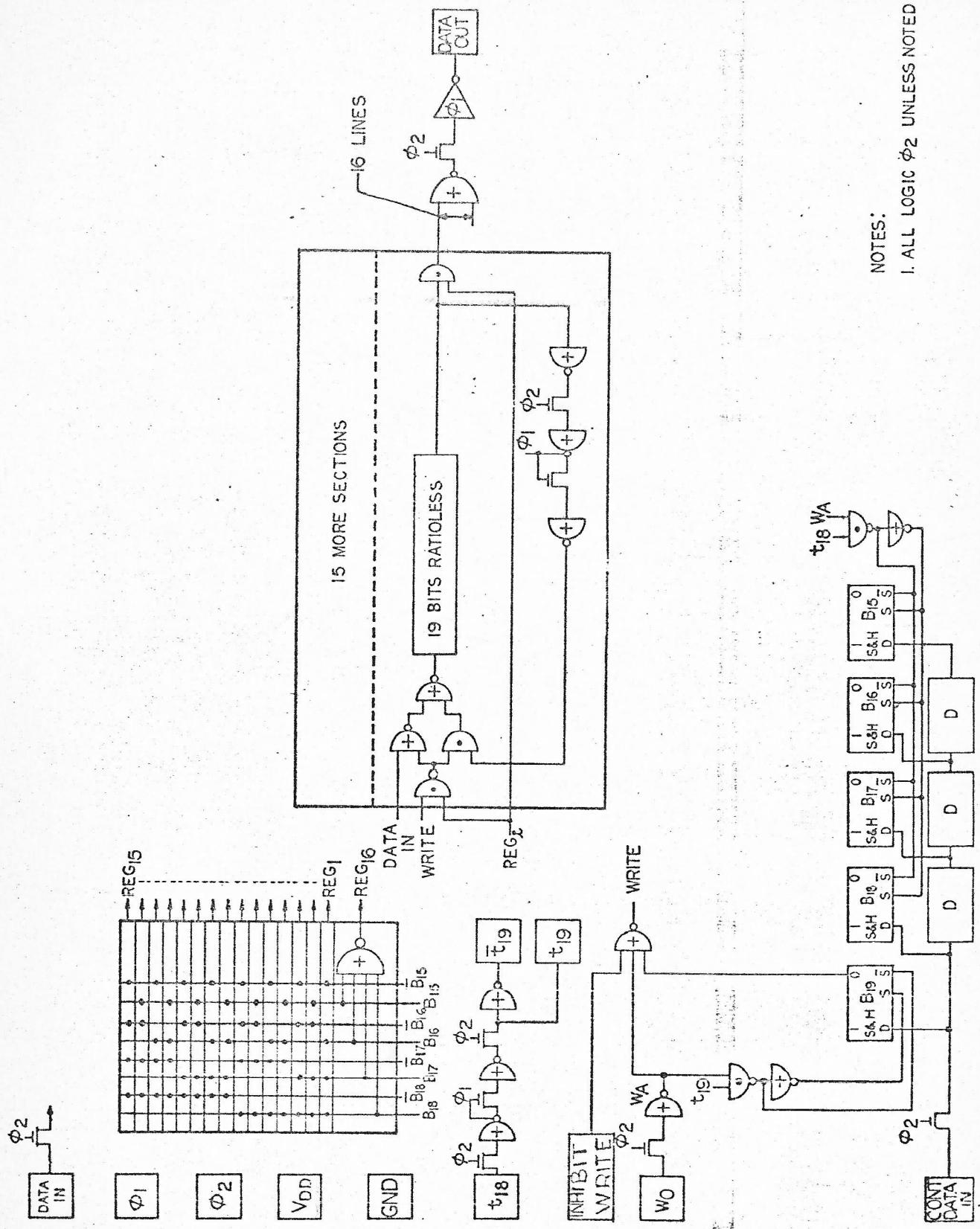


FIGURE 3 RANDOM ACCESS STORAGE - BLOCK DIAGRAM



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		SHEET 24



THIS DIAGRAM HAS NOT BEEN
CHECKED BY SIMULATION.

FIGURE 4 RANDOM ACCESS STORAGE - LOGIC DIAGRAM



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25		

RAS P/N 944114-1

PIN NAME	PIN NUMBER	INPUT CAP.		INPUT RES.	
		MAX -55°C	+125°C	MIN -55°C	+125°C
IN	DATA IN	7	10 pf	10 M _Ω	10 M _Ω
	Ø ₁	14	115 pf	115 pf	8.6K _Ω
	Ø ₂	6	115 pf	115 pf	1.75K _Ω
	W ₀	11	10 pf	10 pf	10 M _Ω
	t ₁₈	10	10 pf	10 pf	10 M _Ω
	CW IN	9	10 pf	10 pf	10 M _Ω
	I.W.	12	10 pf	10 pf	10 M _Ω
	V _{DD}	5			
OUT	GROUND	8			
	DATA OUT	13			

Chip Size: 130 x 115 mils

Number Devices: 2330

Package Type: 14-pin dual in-line package

DC Power Dissipation -55°C 1.34 W +125°C 400 mW

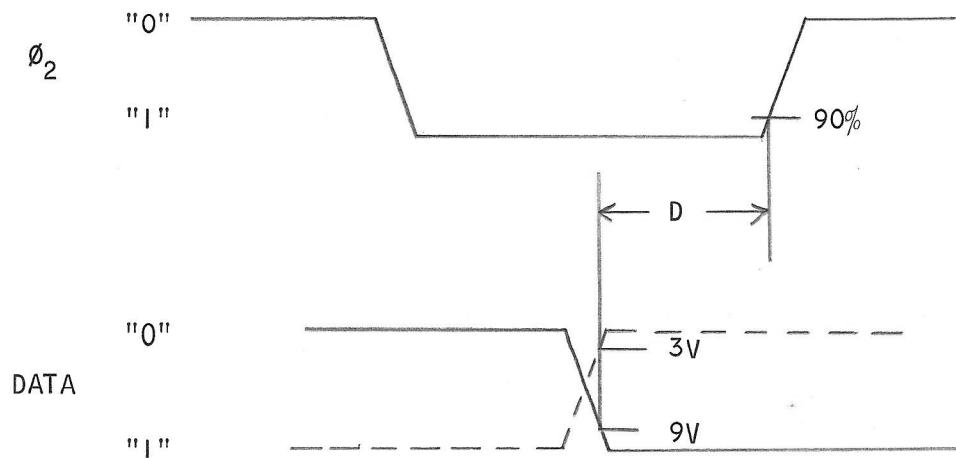
DC Power Dissipation (measured) -55°C _____ +125°C _____

Output Drive Capability Res. -55°C 75K_Ω +125°C 75K_Ω
Cap. -55°C 50pf +125°C 50pf

R. M. Holt
Dept. 93-9
July 24, 1970

PROPAGATION DELAYS - \emptyset_2 INPUT TERMINATIONS

CIRCUIT RAS 944114-1

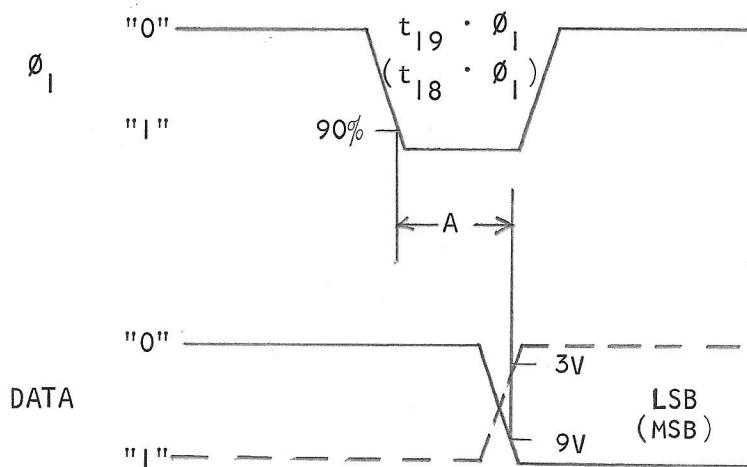


TERMINAL NAME	PACKAGE TERMINAL	DATA SET-UP TIME (D) MIN
w_0	11	800 nS
t_{18}	10	500 nS
CW IN	9	250 nS
I.W.	12	800 nS
DATA IN	7	150 nS

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July 24, 1970

PROPAGATION DELAYS - \emptyset_1 OUTPUT INITIATIONS

CIRCUIT RAS 944114-1



TERMINAL NAME	PACKAGE TERMINAL	PROPAGATION DELAY (A) MAX
DATA OUT	13	275 nS

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July 24, 1970

