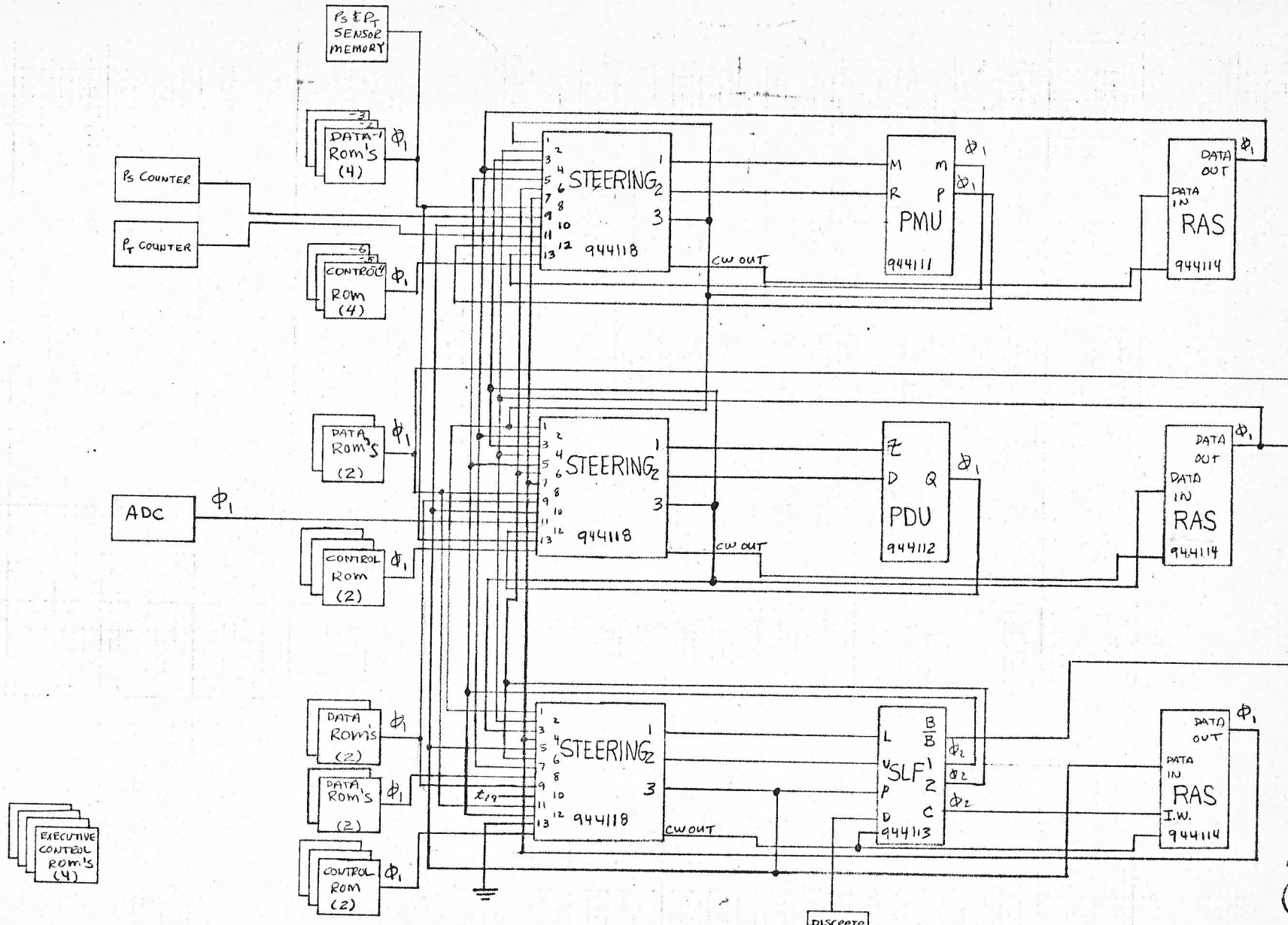
SYSTEM
DATA

F-14A
CADC



DATA PATH INTERCONNECT

F-14A
CADC

4-10-70
HOLT

F-14A CADC MOS-LSI PIN ASSIGNMENTS

PIN	PMU 944111	PDU 944112	SLF 944113	RAS 944114	SL 944118	ROM 944125	PIN
1			GRD		GRD	DATA IN	1
2					CW IN	RETAIN	2
3					t 18	DATA OUT	3
4	W 0				OUT 3	PARITY	4
5	M IN			V DD	EXT 12	INCREMENT	5
6	GRD	V DD	$\overline{\text{BEE}}$ OUT	Ø 2	EXT 2	ADD	6
7	Ø 2		BEE OUT	DATA IN	EXT 4	SUB	7
8	P OUT	W ρ	CEE OUT	GRD	EXT 3	GRD	8
9	M OUT	D IN	ONE OUT	CW IN	EXT 6	RESET (FM)	9
10			P IN	t 18	OUT 1	LOAD	10
11			TWO OUT	W 0	CW OUT	t 18	11
12				IW	OUT 2	Ø 2	12
13			V DD	DATA OUT	V DD	Ø 1	13
14				Ø 1	EXT 10	V DD	14
15			L IN	--	EXT 9	--	15
16			U IN	--	EXT 7	--	16
17	Ø 1	Z IN	W 0	--	EXT 5	--	17
18	R IN	t 18	t 18	--	EXT 1	--	18
19	t 18		CW IN	--	EXT 8	--	19
20	V DD	Q OUT	D IN	--	EXT 13	--	20
21		Ø 2	Ø 1	--	EXT 11	--	21
22		GRD	Ø 2	--	Ø 1	--	22
23		Ø 1		--	Ø 2	--	23
24		Ø		--	W 0	--	24

LSI PIN ASSIGNMENT

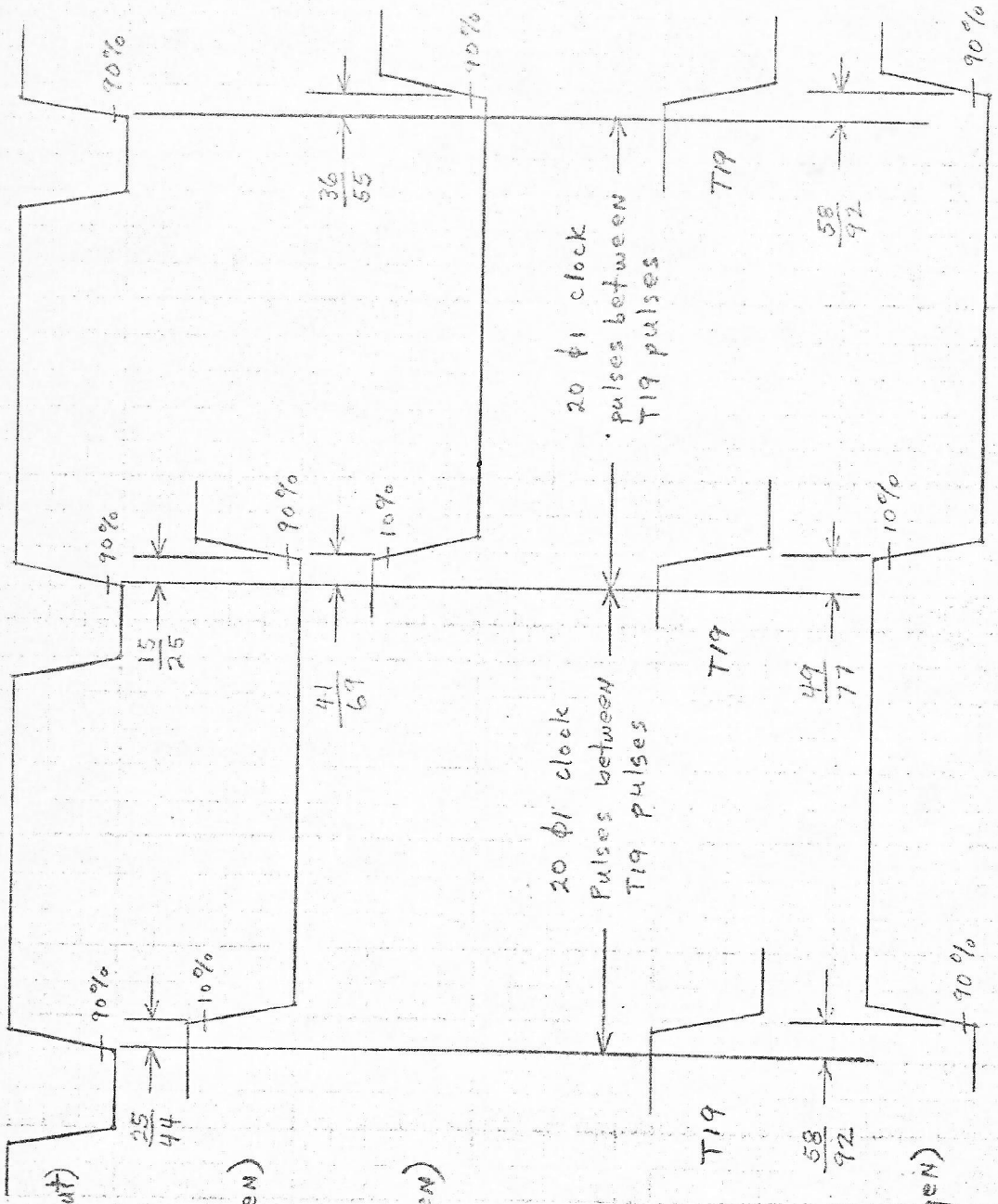
PIN	PMU 944111	PDU 944112	SLF 944113	RAS 944114	SL 944118	ROM 944125
1			GRD		GRD	DATA IN
2					CW IN	RETAIN
3					t_{18}	DATA OUT
4	W_0				OUT 3	PARITY
5	MIN			V_{DD}	EXT 12	INC
6	GRD	V_{DD}	$\overline{B}$ OUT	ϕ_2	EXT 2	ADD
7	ϕ_2		BOUT	DATA IN	EXT 4	SUB
8	POUT	W_0	COUT	GRD	EXT 3	GRD
9	MOUT	DIN	ONE OUT	CW IN	EXT 6	RESET
10			PIN	t_{18}	OUT 1	LOAD
11			TWO OUT	W_0	CW OUT	t_{18}
12				IW	OUT 2	ϕ_2
13			V_{DD}	DATA OUT	V_{DD}	ϕ_1
14				ϕ_1	EXT 10	V_{DD}
15			LIN		EXT 9	
16			UIN		EXT 7	
17	ϕ_1	ZIN	W_0		EXT 5	
18	RIN	t_{18}	t_{18}		EXT 1	
19	t_{18}		CW IN		EXT 8	
20	V_{DD}	QOUT	DIN		EXT 13	
21		ϕ_2	ϕ_1		EXT 11	
22		GRD	ϕ_2		ϕ_1	
23		ϕ_1			ϕ_2	
24					W_0	

Form 2427

AiRESEARCH MFG. CO.

DATE 6-20-70
PREPARED BY W. Nemecek
CHECKED BY

CALC. NO.
MODEL
PART NO.



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DATE 6-19-70
PREPARED BY W. Nemecek
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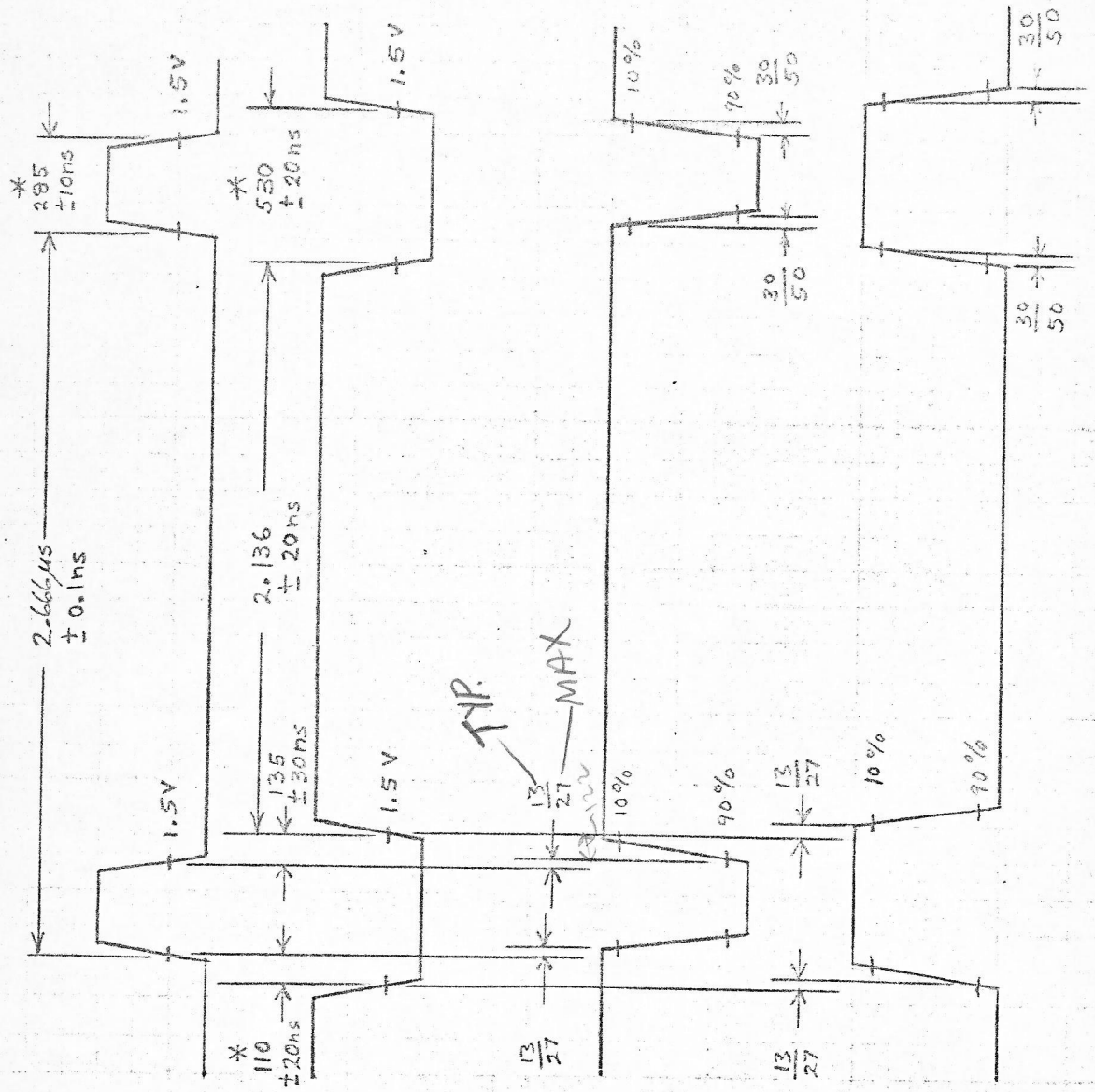
MODEL
PART NO.

Clock Generator Timing



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