

944118
STEERING

4.0 LOGICAL SPECIFICATION

4.1 DEFINITION OF SYSTEM TERMS

BIT TIME: ONE COMPLETE CLOCK PERIOD, 2.66 SEC AT 375 KHZ.

SEE FIGURE 2.

WORD TIME: 20 CONSECUTIVE BIT TIMES (t_0 THROUGH t_{19}). THERE ARE TWO TYPES OF "WORDS".

IN W_A , THE PARALLEL ARITHMETICAL ALGORITHMS OPERATE, AND CONTROL WORDS ARE SHIFTED INTO THE UNITS SERIALLY.

IN W_0 , COMPUTATIONAL INPUTS AND OUTPUTS ARE SHIFTED SERIALLY AMONG THE UNITS.

THESE WORDS ALTERNATE, AND ARE OF EQUAL DURATION; i.e., THEY ARE COMPLEMENTARY.

WORD MARK: A SIGNAL COINCIDENT WITH t_{18} OF EVERY WORD TIME.

OPERATION ("OP") TIME: TWO CONSECUTIVE WORD TIMES (W_A AND W_0)

FRAME MARK: FINAL BIT TIME OF THE FINAL OP.

WORD LENGTH IS 20 BITS. FOR DATA WORDS THIS IS NORMALLY SIGN AND 19 BITS.

DATA IS SHIFTED LSB FIRST. TWO'S COMPLEMENT REPRESENTATION IS USED FOR NEGATIVE NUMBERS. DURING BIT TIME t_0 , INFORMATION IN THE COMPUTER REGISTERS IS "PROPERLY" ORIENTED; i.e., ALL THE BITS OF A DATA WORD ARE CONTAINED IN PROPERLY CORRESPONDING REGISTER POSITIONS. CONTROL WORDS ARE SHIFTED INTO THE LOGIC CHIPS FROM READ-ONLY MEMORIES (ROM'S) SERIALLY DURING W_A OF EVERY OP, AND THEREBY SPECIFY VARIOUS DETAILS OF THE PRESENT AND SUBSEQUENT OPERATIONS.

MEANINGFUL DATA TRANSFERS INTO AND OUT OF THE LOGIC CHIPS AND REGISTERS OCCUR DURING W_0 OF EVERY OP.

4.2 GENERAL DESCRIPTION

STEERING SHALL OPERATE AS A THREE-CHANNEL SERIAL DIGITAL DATA MULTIPLEXER.

INFORMATION SHALL BE SHIFTED THROUGH THE DEVICE DURING W_0 . FIGURE 4 IS A



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SUGGESTED BLOCK DIAGRAM FOR PERFORMING THIS FUNCTION.

4.3 CONTROL WORD

THE UNIT SHALL ACCEPT A CONTROL WORD DURING W_A AS DESCRIBED FURTHER IN 4.5.1.

THIS CONTROL WORD WILL SPECIFY DETAILS OF THE OPERATION AS DESCRIBED THROUGHOUT THIS SPECIFICATION. APPROPRIATE HOLDING AND DECODING LOGIC SHALL BE PROVIDED TO ACCOMPLISH THESE FUNCTIONS.

4.4 INPUTS AND OUTPUTS

PROVISION SHALL BE MADE FOR ACCEPTING OTHER ELECTRICAL AND LOGICAL INPUTS AS FOLLOWS:

PHASE 1 AND PHASE 2 CLOCKS, V_{DD}, GROUND, A W₀ SIGNAL (20 CLOCK PERIODS LONG), A t₁₈ SIGNAL AND 13 DATA INPUTS. THE 13 DATA INPUTS SHALL BE REFERRED TO AS EXT 1 THROUGH EXT 13. FOUR OUTPUTS SHALL BE PROVIDED, THESE SHALL BE REFERRED TO AS OUTPUT 1, OUTPUT 2, OUTPUT 3, AND CONTROL WORD OUT.

4.5 LOGIC FUNCTIONS TO BE IMPLEMENTED

4.5.1 THE CONTROL WORD WILL BE THE LAST 15 BITS OF A 20-BIT CONTROL WORD.

THE FIRST 5 BITS WILL BE SHIFTED THROUGH THE UNIT AND OUT ON CONTROL WORD OUTPUT. FROM THE LEAST SIGNIFICANT END THE FIRST FOUR BITS WILL SPECIFY THE SELECTION FOR OUTPUT 1 FOR THE FORTHCOMING OPERATION.

SPECIFIC CODES SHALL BE INTERPRETED AS FOLLOWS:

CW BITS

L
S
B

6 7 8 9

SELECTED TO OUTPUT NO. 1

0 0 0 0	EXT 1
0 0 0 1	EXT 2
0 0 1 0	EXT 3
0 0 1 1	EXT 4
0 1 0 0	EXT 5



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6 7 8 9

SELECTED TO OUTPUT NO. 1

0 1 0 1	EXT 6
0 1 1 0	EXT 7
0 1 1 1	EXT 8
1 0 0 0	EXT 9
1 0 0 1	<u>EXT 10</u>
1 0 1 0	EXT 13
1 0 1 1	EXT 11
1 1 0 0	EXT 9 + EXT 4
1 1 0 1	EXT 10 + EXT 4
1 1 1 0	EXT 4 + EXT 8
1 1 1 1	EXT 2 - EXT 8

4.5.2 THE NEXT FOUR BITS WILL SPECIFY THE SELECTION FOR OUTPUT 2. SPECIFIC CODES SHALL BE INTERPRETED AS FOLLOWS:

CW BITS

10 11 12 13

SELECTED TO OUTPUT NO. 2

0 0 0 0	EXT 1
0 0 0 1	EXT 2
0 0 1 0	EXT 3
0 0 1 1	EXT 4
0 1 0 0	EXT 5
0 1 0 1	EXT 6
0 1 1 0	EXT 7
0 1 1 1	EXT 8
1 0 0 0	EXT 9
1 0 0 1	EXT 10
1 0 1 0	<u>t₁₉</u>
1 0 1 1	EXT 11
1 1 0 0	EXT 9 + EXT 4
1 1 0 1	EXT 10 + EXT 4
1 1 1 0	EXT 4 + EXT 8
1 1 1 1	EXT 2 - EXT 8



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4.5.3 THE NEXT FOUR BITS WILL SPECIFY THE SELECTION FOR OUTPUT 3. SPECIFIC CODES SHALL BE INTERPRETED AS FOLLOWS:

CW BITS

<u>14 15 16 17</u>	<u>SELECTED TO OUTPUT 3</u>
0 0 0 0	EXT 1
0 0 0 1	EXT 2
0 0 1 0	EXT 3
0 0 1 1	EXT 4
0 1 0 0	EXT 5
0 1 0 1	EXT 6
0 1 1 0	EXT 7
0 1 1 1	EXT 9
1 0 0 0	Σ_1 (PARA. 4.5.4)
1 0 0 1	Σ_2 (PARA. 4.5.5)
1 0 1 0	EXT 11
1 0 1 1	EXT 2 + EXT 4
1 1 0 0	EXT 2 - EXT 8
1 1 0 1	EXT 2 - EXT 4
1 1 1 0	EXT 4 - EXT 2
1 1 1 1	EXT 4 + EXT 8

4.5.4 THE NEXT BIT WILL SPECIFY THE SELECTION FOR THE SIGMA-1 (Σ_1) ADDER OUTPUT. REFER TO THE BLOCK DIAGRAM (FIGURE 3). SPECIFIC CODES SHALL BE INTERPRETED AS FOLLOWS:

CW BITS

<u>18</u>	<u>SELECTED TO Σ_1 ADDER OUTPUT</u>
1	EXT 12 + EXT 8
0	EXT 12 + 0



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4.5.5 THE NEXT TWO BITS WILL SPECIFY THE SELECTION FOR THE SIGMA-2 (Σ_2) ADDER OUTPUT. REFER TO THE BLOCK DIAGRAM (FIGURE 3). SPECIFIC CODES SHALL BE INTERPRETED AS FOLLOWS:

CW BITS

<u>19 20</u>	<u>SELECTED TO Σ_2 ADDER OUTPUT</u>
0 0	+ EXT 2
0 1	- EXT 2
1 0	+ EXT 4
1 1	- EXT 4

4.6 THE LOGIC DIAGRAM IN FIGURE 4 IS INCLUDED AS A SUPPLEMENT TO THE WRITTEN SPECIFICATION. IT HAS NOT BEEN CHECKED BY SIMULATION AND MAY CONTAIN DETAIL LOGIC ERRORS.

4.7 SYSTEM CONSIDERATIONS

THE STEERING CIRCUIT WILL BE TYPICALLY CONNECTED IN THE SYSTEM AS SHOWN IN FIGURE 6. THE 13 EXTERNAL INPUTS WILL ORIGINATE FROM ANY DATA OUTPUT PIN ON ANY CHIP. OUTPUTS 1, 2 AND 3 CAN BE CONNECTED AS THE DATA INPUTS TO THE ROM, PMU, PDU, RAS, SLF, OR ANOTHER STEERING CIRCUIT. ALL TIMING SIGNALS WILL BE GENERATED FROM THE SYSTEM TIMING GENERATOR. OUTPUT DRIVE CAPABILITY IS DISCUSSED IN PARAGRAPH 4.8.5.

4.7.1 PROPAGATION DELAYS

TO INSURE PROPER INTERFACE OF THIS CIRCUIT WITH THE OTHERS IN THE SYSTEM, THE FOLLOWING PROPAGATION DELAY TIMES MUST BE MET. ALL TIMES ARE MAXIMUM AND ARE MEASURED FROM THE 90% LOGICAL "1" LEVEL OF THE CLOCK TO THE 90% LEVEL OF THE SIGNAL.



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CW BITS

L

S

B

TO OUTPUT 1 (UNDER CONDITIONS OF PARA. 4.8.5)

<u>6 7 8 9</u>	<u>FROM</u>	<u>TIME (NS)</u>
0 0 0 0	EXT 1	350
0 0 0 1	EXT 2	350
0 0 1 0	EXT 3	350
0 0 1 1	EXT 4	350
0 1 0 0	EXT 5	350
0 1 0 1	EXT 6	350
0 1 1 0	EXT 7	350
0 1 1 1	EXT 8	350
1 0 0 0	EXT 9	350
1 0 0 1	EXT 10	350
1 0 1 0	EXT 13	350
1 0 1 1	EXT 11	350
1 1 0 0	EXT 9 + EXT 4	500
1 1 0 1	EXT 10 + EXT 4	500
1 1 1 0	EXT 4 + EXT 8	500
1 1 1 1	EXT 2 - EXT 8	500

CW BITS

TO OUTPUT 2 (UNDER CONDITIONS OF PARA. 4.8.5)

<u>10 11 12 13</u>	<u>FROM</u>	<u>TIME (NS)</u>
0 0 0 0	EXT 1	350
0 0 0 1	EXT 2	350
0 0 1 0	EXT 3	350
0 0 1 1	EXT 4	350
0 1 0 0	EXT 5	350
0 1 0 1	EXT 6	350
0 1 1 0	EXT 7	350
0 1 1 1	EXT 8	350
1 0 0 0	EXT 9	350
1 0 0 1	EXT 10	350
1 0 1 0	t ₁₉	350
1 0 1 1	EXT 11	350
1 1 0 0	EXT 9 + EXT 4	500
1 1 0 1	EXT 10 + EXT 4	500
1 1 1 0	EXT 4 + EXT 8	500
1 1 1 1	EXT 2 - EXT 8	500

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CW BITS TO OUTPUT 3 (UNDER CONDITIONS OF PARA. 4.8.5)

<u>14 15 16 17</u>	<u>FROM</u>	<u>TIME (NS)</u>
0 0 0 0	EXT 1	350
0 0 0 1	EXT 2	350
0 0 1 0	EXT 3	350
0 0 1 1	EXT 4	350
0 1 0 0	EXT 5	350
0 1 0 1	EXT 6	350
0 1 1 0	EXT 7	350
0 1 1 1	EXT 9	350
1 0 0 0	(SEE BELOW)	
1 0 0 1	(SEE BELOW)	
1 0 1 0	EXT 11	350
1 0 1 1	EXT 2 + EXT 4	500
1 1 0 0	EXT 2 - EXT 8	500
1 1 0 1	EXT 2 - EXT 4	500
1 1 1 0	EXT 4 - EXT 2	500
1 1 1 1	EXT 4 + EXT 8	500

CW BITS TO OUTPUT 3 (VIA Σ_1)

<u>18</u>	<u>FROM</u>	<u>TIME (NS)</u>
1	EXT 12 + EXT 8	500
0	EXT 12 + 0	500

CW BITS TO OUTPUT 3 (VIA Σ_2)

<u>19 20</u>	<u>FROM</u>	<u>TIME (NS)</u>
0 0	(EXT 12 + EXT 8) + EXT 2	650
0 0	(EXT 12 + 0) + EXT 2	650
0 1	(EXT 12 + EXT 8) - EXT 2	650
0 1	(EXT 12 + 0) - EXT 2	650
1 0	(EXT 12 + EXT 8) + EXT 4	650
1 0	(EXT 12 + 0) + EXT 4	650
1 1	(EXT 12 + EXT 8) - EXT 4	650
1 1	(EXT 12 + 0) - EXT 4	650

4.7.2 THE ABOVE CALCULATED WORST CASE PROPAGATION DELAYS SHALL BE SUBMITTED TO AIRRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.



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LOS ANGELES, CALIFORNIA

SIZE A	CODE NO. 70210	DWG NO. 944118
SCALE	REV	SHEET 15

4.8 ELECTRICAL CHARACTERISTICS

THE ELECTRICAL CHARACTERISTICS SHALL APPLY AT ROOM AMBIENT TEMPERATURE.

4.8.1 POWER SUPPLIES: THE INPUT POWER SUPPLY CHARACTERISTICS ARE DEFINED BELOW:

$$V_{SS} = 0 \text{ V}$$

0.0 VDC (GROUND POTENTIAL ABOUT WHICH V_{SS} AND V_{DD} ARE REFERENCED)

$$V_{DD} = +14.0 \pm 1.0 \text{ V}$$

$$V_{\phi} = -28.5 \pm 1.5 \text{ VDC}$$

4.8.2 POWER DISSIPATION:

4.8.2.1 CALCULATED POWER: THE DC POWER DISSIPATION SHALL AT -55°C AND $+125^{\circ}\text{C}$ BE CALCULATED FOR THE DEVICE COVERED BY THIS SPECIFICATION. THE CALCULATED VALUE SHALL BE SUBMITTED TO AIRESEARCH WITHIN 45 DAYS AFTER AWARD OF CONTRACT.

4.8.2.2 MEASURED POWER: THE DC POWER DISSIPATION AT -55°C AND $+125^{\circ}\text{C}$ OF THIS DEVICE SHALL NOT EXCEED THE CALCULATED VALUE BY MORE THAN 10 PERCENT.

4.8.3 CLOCK CHARACTERISTICS: THE CLOCK CHARACTERISTICS ARE DEFINED IN FIGURE 2 OF THIS SPECIFICATION.

4.8.4 LOGIC LEVELS: THE MOS INPUT AND OUTPUT LOGIC LEVELS ARE DEFINED IN THE MATRIX BELOW:

	(MIN)	(MAX)
INPUT LOGIC "0"	-3.0 V	0.0 V
INPUT LOGIC "1"	V_{DD}	-9.0 V
OUTPUT LOGIC "0"	-2.0 V	0.0 V
OUTPUT LOGIC "1"	V_{DD}	-10.0 V

W_0 , L_{18} : FRAME MARK AND DISCRETE INPUT LOGIC LEVELS ARE DEFINED IN THE MATRIX BELOW:

	(MIN)	(MAX)
INPUT LOGIC "0"	-0.6 V	0.0 V
INPUT LOGIC "1"	-15.4 V	-12.6 V



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CORPORATION

SIZE	CONTRACT NO.	DATE
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SCALE	REV	SHEET / 6

4.8.5 OUTPUT DRIVE CAPABILITY: EACH OUTPUT SHALL BE CAPABLE OF DRIVING A LOAD TO GROUND OF 75.0 NOMS RESISTIVE IN PARALLEL WITH A 10 pF CAPACITOR PLUS A CAPACITOR EQUAL TO FOUR TIMES THE MAXIMUM INPUT CAPACITANCE ON ANY SINGLE INPUT (EXCEPT POWER, CLOCK AND TIMING INPUTS) FOR ANY OF THE FOLLOWING CIRCUITS (V/H 944125, P/N 944111, P/N 944112, F/N 944113, P/N 944114, P/N 944118). THE CALCULATED CAPACITANCE LOAD AT -55°C AND +125°C PER ABOVE SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.8.6 INPUT LOADING

4.8.6.1 HOLDING AND LOGIC INPUTS: THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL TIMING AND LOGIC INPUTS (EXCEPTCLOCKS ϕ_1 AND ϕ_2) SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.8.6.2 THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL CLOCK INPUTS (ϕ_1 AND ϕ_2) SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.8.6.3 DATA INPUTS: THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL DATA INPUTS SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

15
4
62
70



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GENERAL ELECTRIC COMPANY

SIZE	CODE NO.	QWG NO.
A	70210	944118
SCALE	REV.	SHEET 17

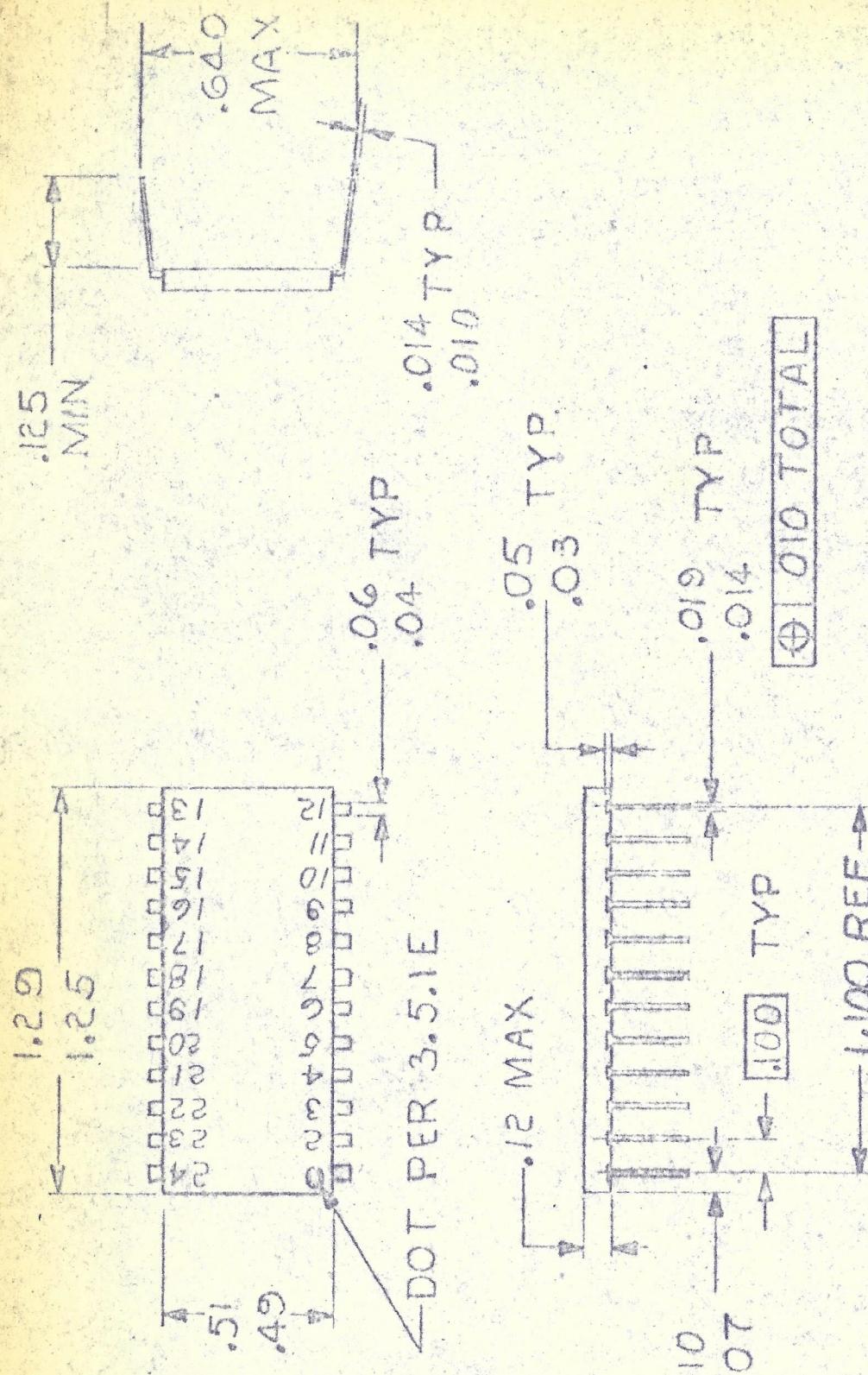
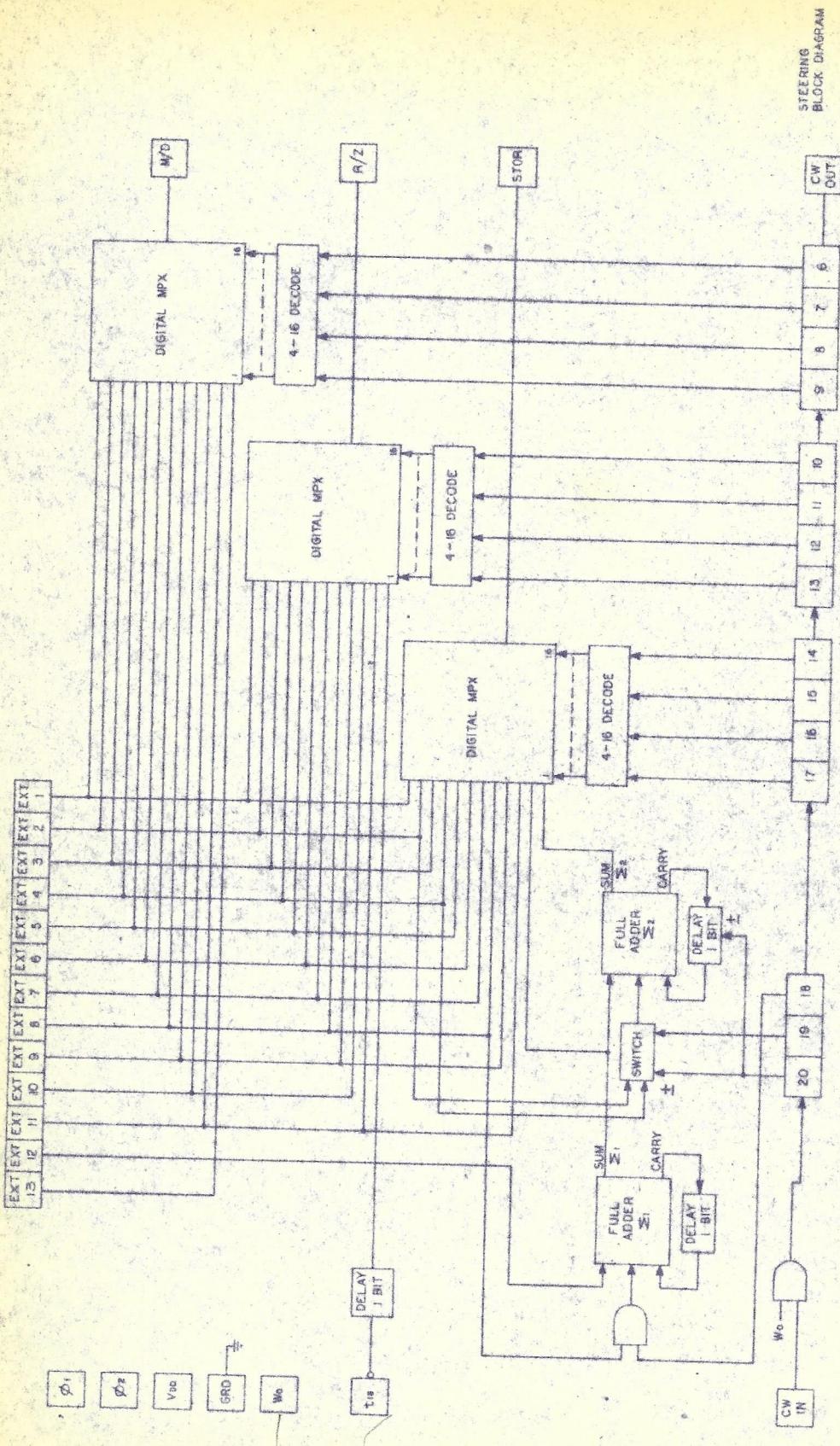


FIGURE 1 PACKAGE DRAWING

AIRRESEARCH MANUFACTURING COMPANY
A DIVISION OF THE DEXXET CORPORATION
100 KELLOGG, DALTON, MA 01226

SIZE	CODE NO.	DWG NO.
A	70210	944118
SCALE	REV	SHLT
A		24

FIGURE 3 STEERING - BLOCK DIAGRAM

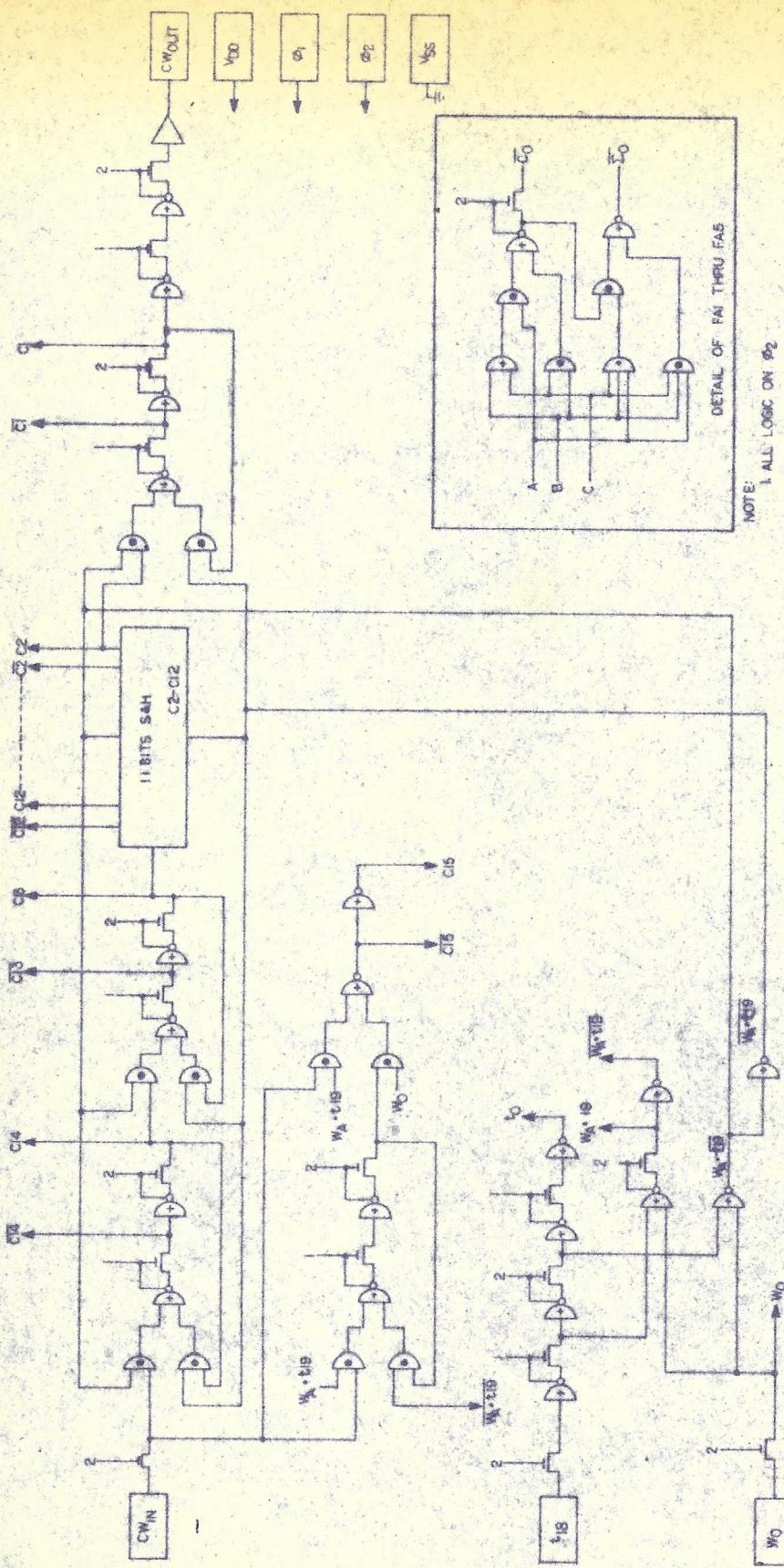


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SIZE	CODE NO.	DWG NO.
A	70210	944118
SCALE	REV	SHEET
		27

THIS DIAGRAM HAS NOT BEEN
CHECKED BY SIMULATION.

FIGURE 4a STEERING - LOGIC DIAGRAM



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A	70210.	944118
SCALE	REV	SHEET 28

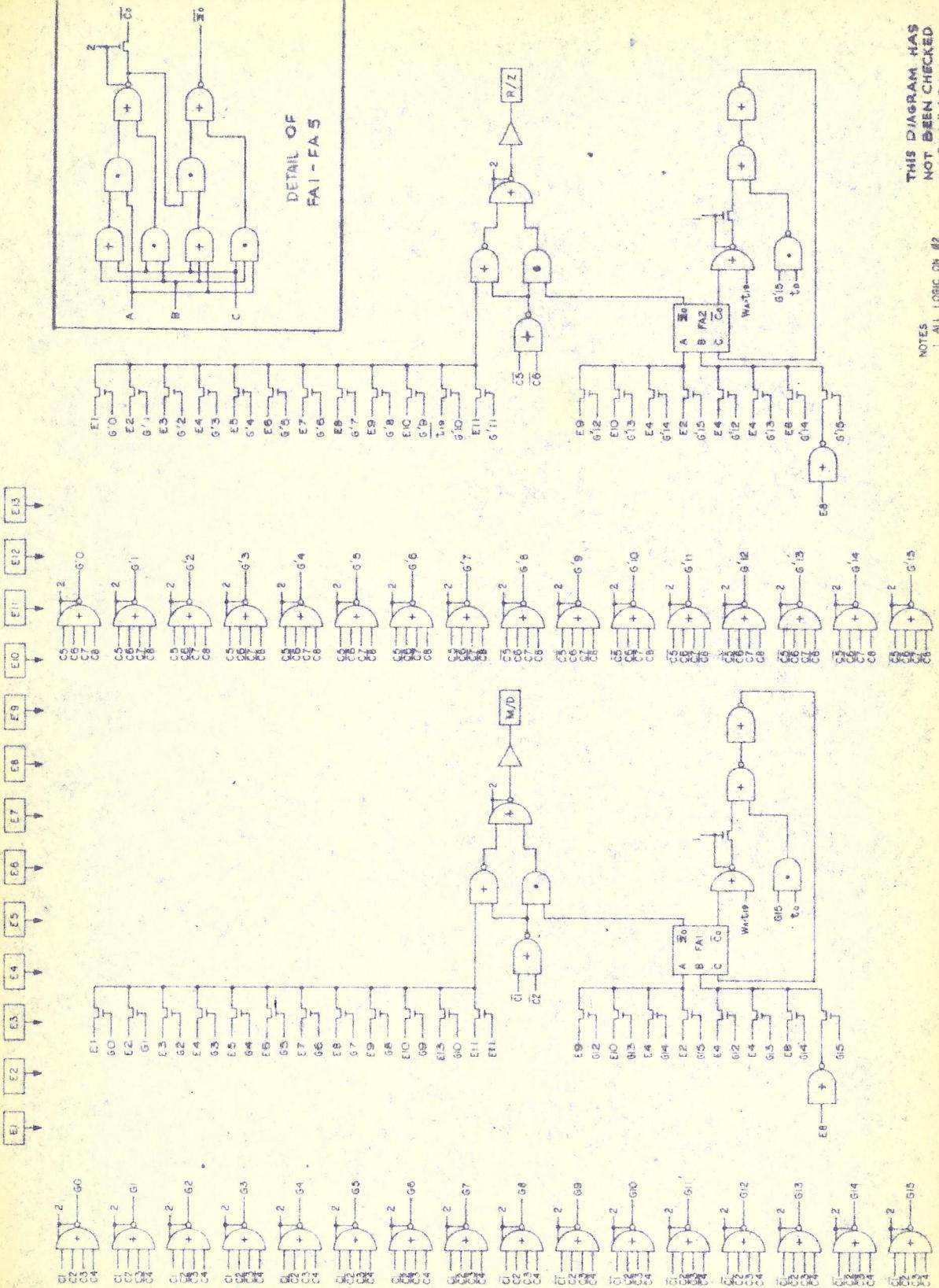


FIGURE 4b STEERING LOGIC

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SIZE	CODE NO.	DWG NO.
A	70210	944118
SCALE	REV	SHEET
		29

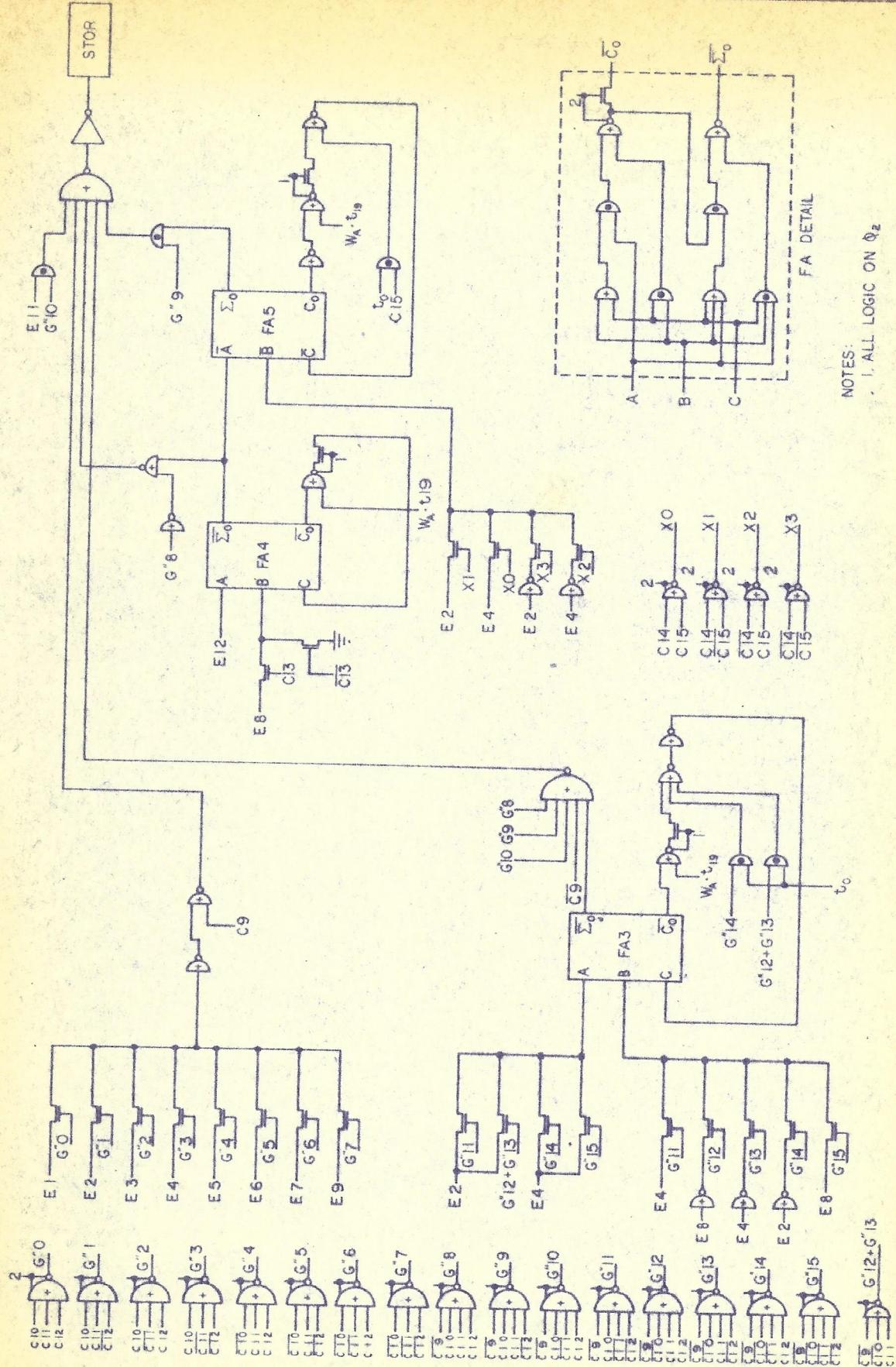


FIGURE 4C STEERING LOGIC



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SCALE	REV	SHEET
1	1	10

LOGIC STEERING P/N 944118-1

PIN NAME	PIN NUMBER	INPUT CAP.		INPUT RES.	
		MAX -55°C	MAX +125°C	MIN -55°C	MIN +125°C
IN	EXT. 1	18	10 pf	10 pf	1 M Ω
	EXT. 2	6	10 pf	10 pf	1 M Ω
	EXT. 3	8	10 pf	10 pf	1 M Ω
	EXT. 4	7	10 pf	10 pf	1 M Ω
	EXT. 5	17	10 pf	10 pf	1 M Ω
	EXT. 6	9	10 pf	10 pf	1 M Ω
	EXT. 7	16	10 pf	110 pf	1 M Ω
	EXT. 8	19	10 pf	10 pf	1 M Ω
	EXT. 9	15	10 pf	10 pf	1 M Ω
	EXT. 10	14	10 pf	10 pf	1 M Ω
	EXT. 11	21	10 pf	10 pf	1 M Ω
	EXT. 12	5	10 pf	10 pf	1 M Ω
	EXT. 13	20	10 pf	10 pf	1 M Ω
	CW IN	2	10 pf	10 pf	1 M Ω
	\emptyset_1	22	50 pf	50 pf	1 M Ω
	\emptyset_2	23	50 pf	50 pf	50 mA
	W_0	24	10 pf	10 pf	1 M Ω
OUT	t_{18}	3	10 pf	10 pf	1 M Ω
	V_{DD}	13			
	GROUND	1			
	M/D-1	10			
	R/Z-2	12			
	STORAGE-3	4			
	CW OUT	11			

Chip Size: 128 x 133 mils

Number Devices: 771

Package Type: 24-pin dual in-line package

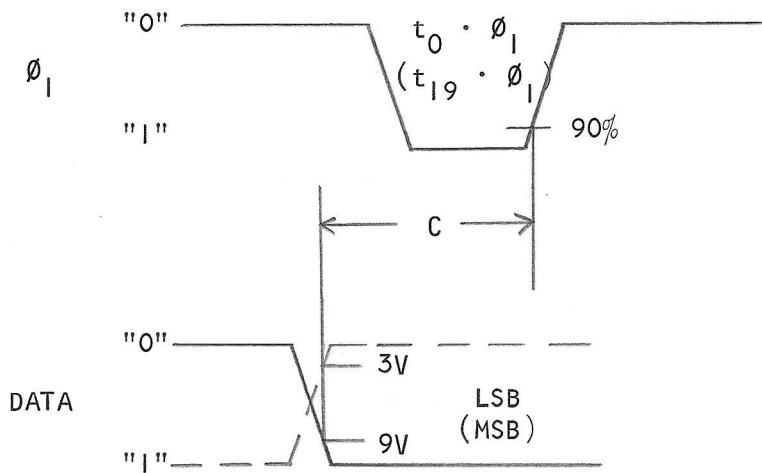
DC Power Dissipation -55°C 2W +125°C 800mW (75% from \emptyset_2)

DC Power Dissipation (measured) -55°C _____ +125°C _____

Output Drive Capability Res. -55°C 75K Ω +125°C 75K Ω
Cap. -55°C 50pf +125°C 50pfR. M. Holt
Dept. 93-9
July 24, 1970

PROPAGATION DELAYS - \emptyset_1 INPUT TERMINATIONS

CIRCUIT STEERING 944118-1



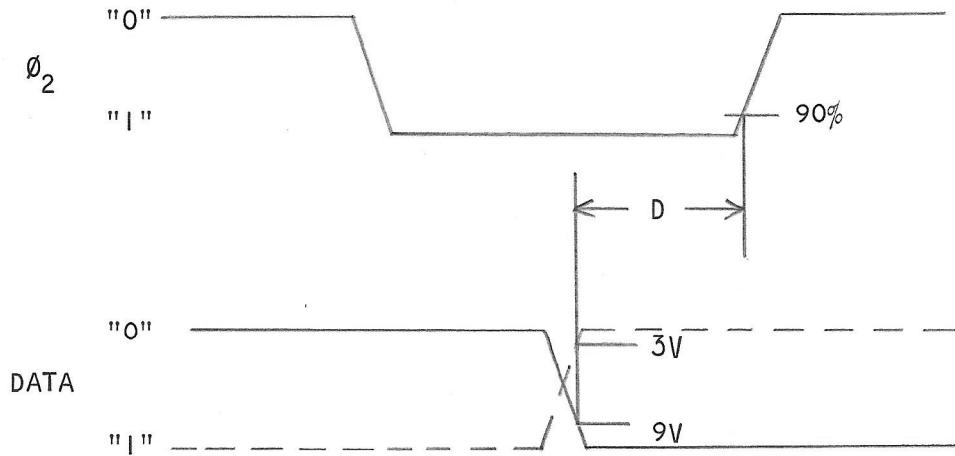
NOTES: DATA MUST NOT CHANGE DURING \emptyset_1 .

TERMINAL NAME	PACKAGE TERMINAL	DATA SET-UP TIME (C) MIN
t_{18}	3	275 nS

R. M. Holt
Dept. 93-9
July 24, 1970

PROPAGATION DELAYS - ϕ_2 INPUT TERMINATIONS

CIRCUIT STEERING 944118-1

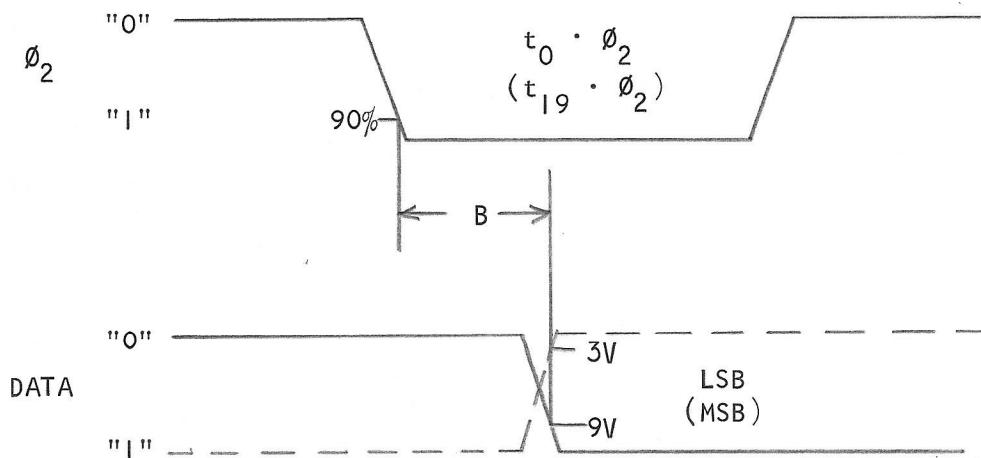


TERMINAL NAME	PACKAGE TERMINAL	DATA SET-UP TIME (D) MIN
CW IN	2	275 nS
W_0	24	1000 nS

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PROPAGATION DELAYS - \emptyset_2 OUTPUT INITIATIONS
AND STRAIGHT THROUGHS

CIRCUIT STEERING 944118-1



S.T. = STRAIGHT THROUGH

S.A. = SINGLE ADDER

TERMINAL NAME	PACKAGE TERMINAL	PROPAGATION DELAY (B) MAX
CW OUT	11	800 nS
S.T. to OUT-1	10	450 nS
S.T. to OUT-2	12	450 nS
S.T. to OUT-3	4	570 nS
S.A. to OUT-1	10	720 nS
S.A. to OUT-2	12	720 nS
S.A. to OUT-3	4	803 nS
E12 + 0 to OUT-3	4	570 nS
E12 + E8 to OUT-3	4	937 nS
E12 ± 2 , ± 4 to OUT-3	4	735 nS
E12 ± 8 ± 2 , ± 4 to OUT-3	4	1125 nS

STEERING TEST SEQUENCE (DOUBLE ADDER)

PAGE "1

Ext 1

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

2

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

3

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

4

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

5

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

6

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

7

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

8

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

9

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

10

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

11

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

12

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

13

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

14

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

15

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

16

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

17

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

18

0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

output
2

X X X X X X X X X X X X X X X X X X X X

output
3

X X X X X X X X X X X X X X X X X X X X

cw out

0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 1 1 0

t_{18}

30

4-13-704

STEERING TEST SEQUENCE.

(D4)

Page 2

EXT 1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
2	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
11	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
CW IN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
w ₀	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	0
t ₁₈	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0
output ₁	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x
output ₂	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x
output ₃	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x
C.W OUT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

30

40

10

40

4-13-70

STEERING TEST SEQUENCE
(DA)

PAGE 3

EXT 1	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	
2	0	-	0	1	1	0	0	1	0	1	1	0	-	0	-	0	-	0	-	0	-	0	-	0
3	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-
4	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-
5	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-
6	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-
7	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-
8	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-
9	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-
10	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-
11	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-
12	0	-	0	0	0	1	1	0	1	1	0	-	-	-	-	-	-	-	0	1	0	1	1	1
13	0	-	0	0^2	0^2	0	-	0	-	0	-	0	-	-	-	-	-	-	-	-	-	-	0	-
IN	0	0	0	1	0	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
W ₀	0	0	0	0	0	0	0	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
t ₁₈	0	-	0	1	0	-	0	-	0	-	0	-	-	-	-	-	-	-	-	-	-	-	-	-
output	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-
out put	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-
out put	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-	X	-
IN OUT	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
W OUT	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

20

90

4-13-70

4-13-70

40 42 44 46 48

49

50 52 54 56 58

60

CW OUT 00000000000000000000000000000000

OUTPUT 3.01101X1111111111111111

OUTPUT 2 X|X|X|X|X|X|X|X|X|X|X|X|X|X|X|X|X|

OUTPUT 1 X|X|X|X|X|X|X|X|X|X|X|X|X|X|X|X|X|

816

W.

CW IN 0000000000000000

13

12

11

10

9

8

7

6

5

4

3

2

1

EXT 1 0

PAGE 4

STEEP TEST SECTION 2

STEERING TEST SEQUENCE (SA)

PAGE 2

STEERING TEST SEQUENCE
(SA)

PAGE 3

0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 0

1 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

2 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

3 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

4 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

5 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

6 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

7 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

8 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

9 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

10 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

11 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

12 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

13 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

cw IN 0 - 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

t,g 0 - 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0

out 1 x x x x 1 0 1 1 0 0 0 1 1 x - x

out 2 x x x 1 0 1 1 0 0 0 1 1 x - x

out 3 x x x 1 0 1 1 0 0 0 1 1 x - x

out 4 1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1

STEERING TEST SEQUENCE

(SA)

PAGE 4

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	-	0	0	0	1	1	0	1	1	0	-	-	-	-	-	-	-	0
3	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
4	0	-	-	0	1	1	0	0	1	0	-	-	-	-	-	-	-	-	0
5	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
6	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
7	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
8	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
9	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
10	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
11	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
12	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
13	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
cur in	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W ₀	0	-	-	-	-	0	1	-	-	1	0	-	-	-	-	-	-	-	1
t ₁₈	0	-	-	-	-	0	1	0	0	-	-	-	-	-	-	-	-	-	0
out 1	1	-	-	-	-	-	X	X	-	-	-	-	-	-	-	-	-	-	X
out 2	2	-	-	-	-	-	X	X	-	-	-	-	-	-	-	-	-	-	X
out 3	3	-	-	-	-	-	X	1	0	1	0	0	1	X	-	-	-	-	X
cur out	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

STEERING TEST SEQUENCE P/N 944118

(STRAIGHT THROUGHS)

PAGE 1

 Ext 1 ϕ_2 0

 2 ϕ_2 0

 3 ϕ_2 0

 4 ϕ_2 0

 5 ϕ_2 0

 6 ϕ_2 0

 7 ϕ_2 0

 8 ϕ_2 0

 9 ϕ_2 0

 10 ϕ_2 0

 11 ϕ_2 0

 12 ϕ_2 0

 13 ϕ_2 0

 CW IN ϕ_2 0

 W₆ ϕ_2 0 1

 t_{1,8} ϕ_2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0

 OUTPUT ϕ_2 X <= X 1 0 1 X <= X 0 1 0 X <= X 1 0

 OUTPUT ϕ_2 X <= X 1 0 1 X <= X 1 0 1 X <= X 1 0

 OUTPUT ϕ_2 X <= X 1 0 1 X <= X 1 0 1 X <= X 1 0

 CW OUT ϕ_2 X <= X 1 0 1 X <= X 1 0 1 X <= X 1 0

 CW OUT ϕ_2 X <= X 1 0 1 X <= X 1 0 1 X <= X 1 0

SWIN

OUTPUTS

 OUTPUT ₂ X <

 OUTPUT ₃ X <

SWIN

 W_{0,3}

 W_{0,2}

20

 W_{0,1}

Ext	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
C_{ST}	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
w_0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
w_1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
z	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
cw_{in}	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
out	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
out	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
cw_{out}	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

cw_{out} was 10 w_0 was 10 w_1 was 10 z was 9

AIRSEARCH MFG. CO.

DATE _____

CALC. NO. _____

PREPARED BY _____

MODEL _____

CHECKED BY _____

PART NO. _____

STEERING TEST SEQUENCE

(S.T.)

<u>CYCLE</u>	SELECTED <u>EXT OUT DATA 1 2 3</u>	L S B	CONTROL WD IN STEERING															SHIFTED IN NEXT OP
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
W ₀₁	1, 2, 3	L	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1 1 0 1 0
W ₀₂	2, 3, 4	S	0	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0 0 0 1 0
W ₀₃	3, 4, 5	B	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1 0 1 0
W ₀₄	4, 5, 6	L	0	0	1	1	0	0	0	0	1	0	1	0	1	0	1	0 0 1 0
W ₀₅	5, 6, 7	S	0	1	0	0	0	0	1	0	1	1	0	0	1	0	1	1 1 1 0 0
W ₀₆	6, 7, 9	B	0	1	0	1	0	1	0	0	1	1	1	1	0	0	0	1 0 0
W ₀₇	7, 8, X	L	0	1	1	0	0	1	1	1	1	0	0	0	1	0	0	1 1 0 0
W ₀₈	8, 9, X	S	0	1	1	1	1	0	0	0	1	0	0	1	1	0	0	1 0 1 0 0
W ₀₉	9, 10, 11	B	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	1 1 0 0 0
W ₀₁₀	10, E ₉ , X	L	1	0	0	1	1	0	1	0	1	0	1	1	0	0	0	0 0 0 0 0
W ₀₁₁	13, 11, 1	S	1	0	1	0	1	0	1	0	0	0	0	0	0	0	1	0 0 0
W ₀₁₂	11, 1, 2	B	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	X X X X X

L
S
B

←

Before shift	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	A	B	C	D	E
After 5 bit shift left	5	6	7	8	9	10	11	12	13	14	15	A	B	C	D	E				

AIRESEARCH MFG. CO.

DATE 3-1-70
 PREPARED BY R HOLT
 CHECKED BY _____

CALC. NO. _____
 MODEL _____
 PART NO. _____

STEERING ADDER TEST PATTERNS

L
S
B

CAB
 ✓000 ✓
 ✓001 ✓
 ✓010 ✓
 ✓011 ✓
 ✓100 ✓
 ✓101 ✓
 ✓110 ✓
 ✓111 ✓

0 0	1 1 1 1	0 0 0 0	carry
1 1	0 1 1 0	1 0 0 0	A
0 0	0 1 0 1	1 0 1 0	B
1 1	1 1 0 0	0 1 1 0	= A+B

A SINGLE ADD

0 1	1 1 1 0	0 0 0 1	present
0 0	1 1 0 1	1 0 0 0	A
0 0	1 0 1 1	0 1 0 0	B
0 1	1 0 0 0	1 1 0 1	= A-B

SINGLE SUB

0 0	1 1 0 1	1 0 0 0	L
1 1	0 1 0 0	1 0 1 1	S
			B
			C

1 1 0 1 1 0	1 1 0 0	A
0 0 0 1 0 1	1 1 0 1	+B
1 1 1 1 0 0	0 0 1 1	A+B
1 1 0 0 0 1	0 1 0 1	+C
1 0 1 1 0 1	0 0 0 1	= D

DOUBLE ADD

0 1 0 1 1 0	1 0 1 1 0 0	A
0 0 0 1 0 1	1 1 0 1	B
0 1 1 1 0 0	0 0 1 1	A+B
1 1 0 1 1 0	0 1 0 0	-C
0 1 0 0 1 0	1 0 1 1	= D

SINGLE ADD
AND SUBTRACT

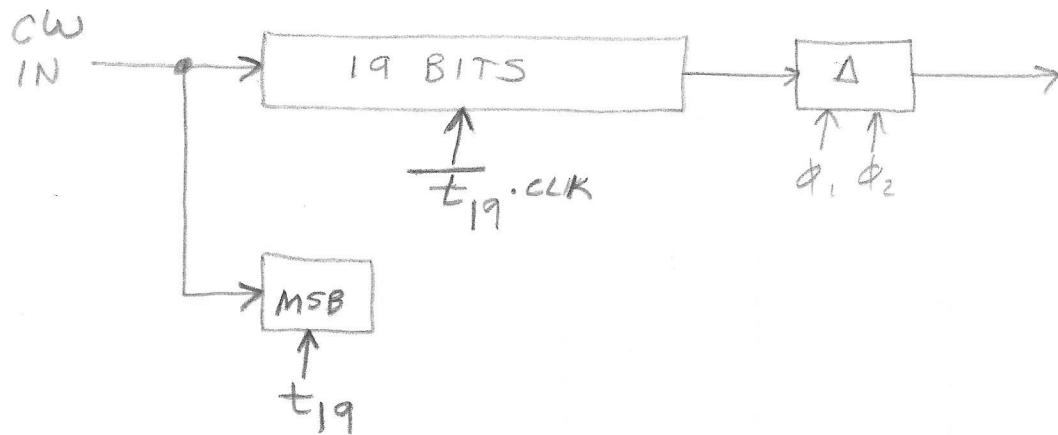
$$C = 0010011011$$

AI RESEARCH MFG. CO.

DATE 3-10-70
 PREPARED BY R. HOLT
 CHECKED BY _____

CALC. NO. _____
 MODEL _____
 PART NO. _____

STEERING CW PATH


C.W. OUTPUT
DURING Wₙ shift cycle

Previous CW lsb twice and minus the msb

C.W. OUTPUT
DURING W₀ shift cycle

lsb from the present cw