



AIRESEARCH MANUFACTURING COMPANY
Los Angeles, California

INTERNAL REPORT

MOS PROCESSOR FOR THE F-14A CADC

Report No. 71-7266 April 1971

Number of pages 122

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Original date April 1971

Revision	Date	Pages Affected (Revised, Added, Eliminated)

INTRODUCTION

Although the F-14A CADC processor was classified as a special purpose machine during its initial development, the processor is actually quite simple to understand and certainly general in its application. The three sections presented herein describe this processor and emphasize its general capabilities. The section contents are briefly described below.

Section 1--Discussion of hardware including LSI circuits, timing, and overall construction

Section 2--Discussion of programming aspects (software) from mathematical model to programming examples

Section 3--Discussion of computer programming aids developed to support the programming of the processor

Pertinent discussions, examples, and illustrations that would clarify a number of questions encountered during formal presentations are included to facilitate an overall understanding of the processor system.



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SECTION I

HARDWARE

The hardware for the F-14A CADC processor consists of six different types of circuit: parallel multiplier unit (PMU), parallel divider unit (PDU), special logic function (SLF), steering logic (SL), random access storage (RAS), and read-only memory (ROM). These circuits are derived from the metal-oxide-semiconductor (MOS) integrated circuit technology. Functional operation of each circuit will be discussed in detail after System Timing.

MOS THEORY

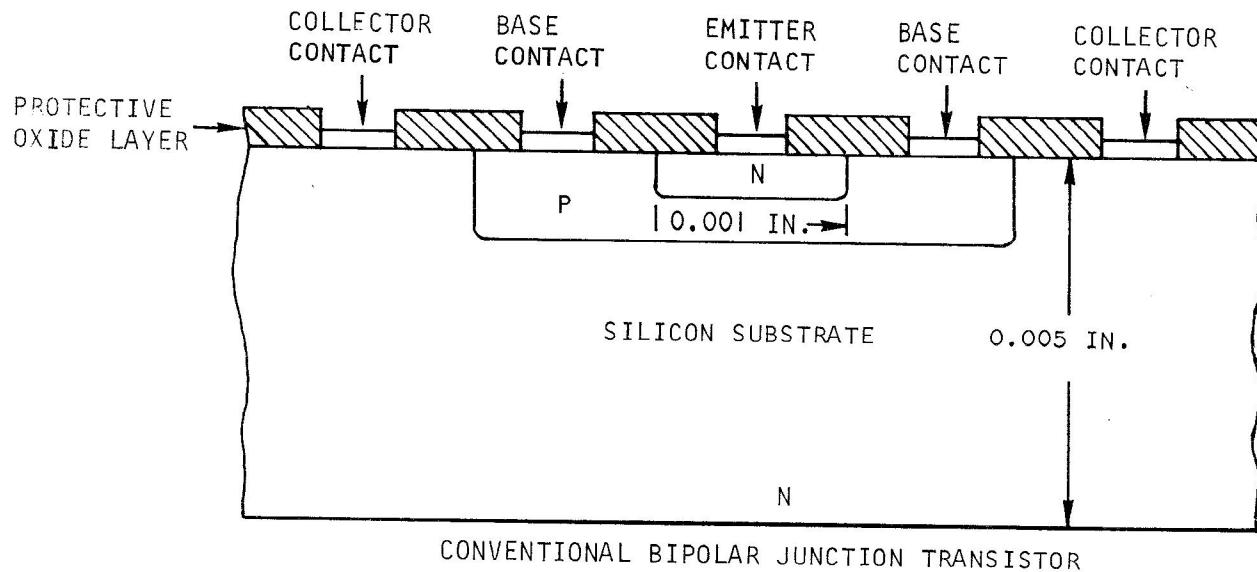
The MOS transistor is a voltage-controlled device that exhibits an extremely high input resistance (10^{12} to 10^{14} ohms). With its insulated gate, it maintains a high input resistance regardless of the magnitude or polarity of the input gate voltage. Even at elevated temperatures, the gate leakage is negligible. These characteristics permit the use of direct-coupled circuitry and provide isolation between input and output.

A single MOS transistor is a simple device (Figure I-1). Two highly doped P-type areas are diffused into an N-type silicon substrate. These two diffusion areas are referred to as the source and the drain and are located closely to each other (0.0005 in. typically). A thin (0.000005 in. typically) insulating layer, usually silicon dioxide, is placed over the surface of the silicon between the source and the drain. The gate is a metallic conductor deposited over the oxide layer and insulated from the source, drain, and substrate by the oxide. Metal is also deposited on the diffusion areas so that electrical contacts can be attached.

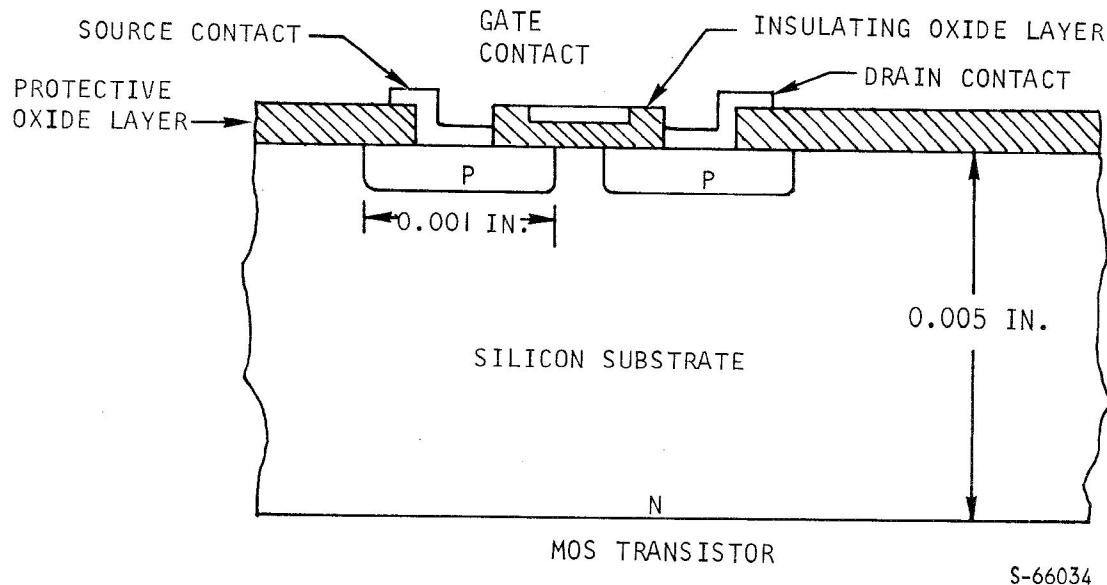
If a voltage is applied from source to drain with no gate voltage, current will not flow, and the device remains in the off state. As the gate electrode is given a negative voltage with respect to the substrate, electrons are repelled from the surface region immediately beneath the gate. At a sufficiently negative voltage, called the threshold, the surface region inverts and becomes P-type. This induced P-type channel provides a path for conduction of current between source and drain, and the device turns on. Hence, the signal on the gate can modulate the flow of current in the channel in a manner quite analogous to the pentode vacuum tube.

The device described is shown as a P-channel enhancement mode device because the application of gate voltage enhances the flow of current between source and drain. This is the material mode with which the computer LSI chips are implemented.





CONVENTIONAL BIPOLAR JUNCTION TRANSISTOR



MOS TRANSISTOR

S-66034

Figure I-1. Cross Section of Typical Bipolar Junction Transistor and MOS Transistor (Dimensions are not necessarily to scale)



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Comparison with Conventional Bipolar Junction Transistors

The comparisons given below will clarify the differences between MOS transistors and conventional bipolar junction transistors.

1. Size

A single MOS transistor requires far less substrate area than a bipolar junction transistor. For example, a typical bipolar junction transistor within an integrated circuit requires an area of about 0.020 to 0.025 sq in., while a comparable MOS transistor requires about 0.001 to 0.002 sq in. Size is closely related to manufacturing yield. Defects are randomly located throughout a wafer so that many small devices will have a higher yield than a few large devices. At any one time, therefore, there is an economically optimal substrate area. Using MOS construction, this substrate can have five to ten times the functional complexity of a conventional integrated circuit.

2. Process

The MOS manufacturing process has been estimated to be about 30 percent simpler than the conventional planar junction process. Only one diffusion step is required to make a MOS device, while bipolar junction integrated circuits require four or five. MOS integrated circuits require four photomask steps, while bipolar junction integrated circuits require at least six photo-mask steps. Furthermore, all terminals of a MOS device are inherently isolated from the substrate without special diffusion steps. Conventional integrated circuits often require extra diffusion steps to provide this isolation.

3. Input Impedance

The bipolar junction transistor is basically a current-controlled device. Typically, input resistance is a few thousand ohms. Current is required at the input to change the state of the device if the circuit is digital, or to modulate the current flow at the output if the circuit is linear. This input current must be supplied by the preceding device. Therefore, each bipolar junction transfer can drive only a limited number of following stages without becoming quite large. By way of contrast, MOS devices have almost unlimited dc fan-out. As mentioned previously, the MOS transistor is voltage-controlled and draws a negligible input current. This high input impedance permits the use of direct-coupled circuitry with fewer components and no coupling devices.

4. Speed

The speed limitation of the MOS device is related to the time constants of stray circuit capacitances through which logical voltage levels must discharge. With a limited current capability, there is a frequency beyond which the voltage levels will not thoroughly transmit. Current MOS devices are operating at 2 MHz, which is about four times higher than will be required for the computer operation.

