

944113
SLF

4.0 LOGICAL SPECIFICATION

4.1 DEFINITION OF SYSTEM TERMS

BIT TIME: ONE COMPLETE CLOCK PERIOD, 2.66 SEC AT 375 KHZ.
SEE FIGURE 2.

WORD TIME: 20 CONSECUTIVE BIT TIMES (t_0 THROUGH t_{19}). THERE
ARE TWO TYPES OF "WORDS".

IN w_A , THE PARALLEL ARITHMETICAL ALGORITHMS OPERATE,
AND CONTROL WORDS ARE SHIFTED INTO THE UNITS (SERIALLY).

IN w_0 , COMPUTATIONAL INPUTS AND OUTPUTS ARE SHIFTED
SERIALLY AMONG THE UNITS.

THESE WORDS ALTERNATE, AND ARE OF EQUAL DURATION;
i.e., THEY ARE COMPLEMENTARY.

WORD MARK: A SIGNAL COINCIDENT WITH t_{18} OF EVERY WORD TIME.

OPERATION ("OP") TIME: TWO CONSECUTIVE WORD TIMES (w_A AND w_0).

FRAME MARK: FINAL BIT TIME OF THE FINAL OP.

WORD LENGTH IS 20 BITS. FOR DATA WORDS THIS IS NORMALLY SIGN AND 19 BITS.

DATA IS SHIFTED LSB FIRST. TWO'S COMPLEMENT REPRESENTATION IS USED FOR
NEGATIVE NUMBERS. DURING BIT TIME t_0 , INFORMATION IN THE COMPUTER REGISTERS
IS "PROPERLY" ORIENTED; i.e., ALL THE BITS OF A DATA WORD ARE CONTAINED IN
PROPERLY CORRESPONDING REGISTER POSITIONS. CONTROL WORDS ARE SHIFTED INTO THE
LOGIC CHIPS FROM READ-ONLY MEMORIES (ROM'S) SERIALLY DURING w_A OF EVERY OP, AND
THEREBY SPECIFY VARIOUS DETAILS OF THE PRESENT AND SUBSEQUENT OPERATIONS.

MEANINGFUL DATA TRANSFERS INTO AND OUT OF THE LOGIC CHIPS AND REGISTERS OCCUR
DURING w_0 OF EVERY OP.

4.2 GENERAL DESCRIPTION

SLF SHALL PERFORM LOGICAL OPERATIONS AND GENERATE SPECIFIC DATA AND LOGIC
OUTPUTS AS DESCRIBED HEREIN. FIGURE 3 IS A SUGGESTED BLOCK DIAGRAM.



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4.3 CONTROL WORD

THE UNIT SHALL ACCEPT A CONTROL WORD OF 4 BITS WHICH WILL ARRIVE DURING BIT TIMES t_{15} THROUGH t_{18} OF w_A . THIS CONTROL WORD WILL SPECIFY DETAILS OF THE OPERATION AS DESCRIBED THROUGHOUT THIS SPECIFICATION. APPROPRIATE HOLDING AND DECODING LOGIC SHALL BE PROVIDED TO ACCOMPLISH THESE FUNCTIONS.

4.4 INPUTS AND OUTPUTS

PROVISION SHALL BE MADE FOR ACCEPTING ELECTRICAL, DATA AND LOGICAL INPUTS AS FOLLOWS: PHASE 1 AND PHASE 2 CLOCKS, V_{DD} , GROUND, A w_0 SIGNAL (20 CLOCK PERIODS LONG), A WORD MARK (t_{18}), THREE DATA INPUTS (CALLED U, P AND L), AND ONE LOGIC INPUT (CALLED D). TWO DATA OUTPUTS (LINE 1 AND LINE 2) AND THREE LOGIC OUTPUTS (B, \bar{B} AND C) SHALL BE PROVIDED AS DESCRIBED IN 4.5.

4.5 FORMAL DESCRIPTION OF THE UNIT'S OPERATION

DATA INPUTS: U, P, L (POSITIVE AND NEGATIVE NUMBERS)

LOGIC INPUT: D (WILL BE VALID THROUGHOUT w_A)

CONTROL WORD: 4 BITS, ARRIVING DURING BIT TIMES t_{15} THROUGH t_{18} OF w_A .

DATA OUTPUTS: LINE 1, LINE 2 (LINE 1 DOES NOT HAVE TO BE VALID DURING w_A)

LOGIC OUTPUTS: B, \bar{B} , C

FUNDAMENTAL LOGICAL DEVICE CONSISTS OF THREE REGISTERS (U, P, L), WHOSE INPUTS ARRIVE IN w_0 VIA CORRESPONDINGLY NAMED INPUT PINS. ONE OF THESE IS "PICKED" AT THE END OF w_0 BY ASSOCIATED COMPARISON LOGIC AS FOLLOWS:

PICK L IF $P < L$ (ALGEBRAICALLY)

PICK U IF $P > U$ AND NOT $< L$ (ALGEBRAICALLY)

OTHERWISE PICK P ($U \geq P \geq L$) (ALGEBRAICALLY)

THE CONTENTS OF THE "PICKED" REGISTER ARE DELIVERED TO THE LINE 1 OUTPUT IN THE NEXT w_0 (WHILE NEW U, P AND L INPUTS ARRIVE) UNLESS OVERRIDDEN BY PARTICULAR LOGICAL COMBINATIONS AS DESCRIBED BELOW. DATA SHALL BE DELIVERED TO THE LINE 2 OUTPUT AS INDICATED.



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THE B LOGIC OUTPUT SHALL BE TRUE IN w_A IF P HAS BEEN PICKED AT THE END OF THE IMMEDIATELY PRECEDING w_0 . IT SHALL ALWAYS BE FALSE IN w_0 . THE \bar{B} OUTPUT SHALL BE THE COMPLEMENT OF B IN w_A , AND FALSE IN w_0 .

THE C LOGIC OUTPUT SHALL BE TRUE IN w_0 IF CERTAIN LOGICAL COMBINATIONS ARE RECOGNIZED AT THE END OF THE IMMEDIATELY PRECEDING w_A , AS DESCRIBED BELOW. IT SHALL ALWAYS BE FALSE IN w_A .

ACTIONS SHALL OCCUR AS LISTED IN THE TABLE IN RESPONSE TO VARIOUS CW AND D INPUT COMBINATIONS.

L	M
S	S
B	B

CW 15 16 17 18

D

ACTION

0 0 0 0 ✓

IMMATERIAL

1) SWITCH P INPUT TO LINE 1 AND P OUTPUT TO LINE 2.

0 0 0 1 ✓

IMMATERIAL

2) IF U WAS PICKED AT END OF PREVIOUS w_0 , SET THE C OUTPUT IN THE NEXT w_0 .

0 0 1 0 ✓

IMMATERIAL

1) BIT-BY-BIT LOGICAL PRODUCT OF P AND U INPUTS TO LINE 1.

0 0 1 1

0

2) BIT-BY-BIT LOGICAL PRODUCT OF P AND L INPUTS TO LINE 2.

0 1 0 0 THROUGH

ETA

1 ✓

1) PICKED OUTPUT TO LINE 1. L, u, P

1 0 1 1 INCLUSIVE

2) GRAY CODE CONVERSION OF P INPUT TO LINE 2.

1 1 0 0 THROUGH

0

P OUTPUT WITH "1" IN LSB TO LINE 1.

1 1 1 1 INCLUSIVE

SAME AS ABOVE WITH "1" IN MSB IF P WAS PICKED AT END OF PREVIOUS w_0 .

SET THE C OUTPUT.

1 1 0 0 THROUGH

0

1) PICKED OUTPUT TO LINE 1 AND ALSO TO P INPUT. L, u, P

1 1 1 1 INCLUSIVE

2) P OUTPUT TO LINE 2.

1

SWITCH P INPUT TO LINE 1 AND P OUTPUT TO LINE 2.

4.6 THE LOGIC DIAGRAM IN FIGURE 4 IS INCLUDED AS A SUPPLEMENT TO THE WRITTEN SPECIFICATION. IT HAS NOT BEEN CHECKED BY SIMULATION AND MAY CONTAIN DETAIL LOGIC ERRORS.



AIRESEARCH MANUFACTURING COMPANY
A DIVISION OF THE BANTAM CORPORATION
LOS ANGELES, CALIFORNIA

SIZE A	CODE NO. 70210	DWG NO. 944113
SCALE	REV	SHEET 11

4.7 SYSTEM CONSIDERATIONS

THE SLF CIRCUIT WILL BE TYPICALLY CONNECTED IN THE SYSTEM AS SHOWN IN FIGURE 6.

THE THREE DATA INPUTS (U, P, L) AND THE CW CAN COME FROM THE STEERING CIRCUIT.

THE D INPUT WILL COME FROM EXTERNAL LOGIC. OUTPUT LINE 1 AND LINE 2 CAN BECOME DATA INPUTS TO THE PMU, PDU, RAS, OR STEERING OUTPUTS B, \bar{B} , AND C CAN BECOME LOGIC LEVEL INPUTS TO THE APPROPRIATE INPUTS ON THE ROM AND RAS.

ALL TIMING SIGNALS WILL BE GENERATED FROM THE SYSTEM TIMING GENERATOR. OUTPUT DRIVE CAPABILITY IS DISCUSSED IN PARAGRAPH 4.8.5.

4.7.1 PROPAGATION DELAYS

TO INSURE PROPER INTERFACE OF THIS CIRCUIT WITH THE OTHERS IN THE SYSTEM, THE FOLLOWING PROPAGATION DELAY TIMES MUST BE MET. ALL TIMES ARE MAXIMUM AND ARE MEASURED FROM THE 90% LOGICAL "1" LEVEL OF THE CLOCK TO THE 90% LEVEL OF THE SIGNAL.

FROM	TO	TIME (NS)
U INPUT	COMPARATOR OR LIMITER REGISTER	250
P INPUT	COMPARATOR OR LIMITER REGISTER	250
L INPUT	COMPARATOR OR LIMITER REGISTER	250
REGISTER OUTPUT	LINE 1 OR LINE 2	350 (UNDER CONDITIONS OF PARA. 4.8.5)
PICK P SIGNAL	LINE 1 OR LINE 2	350 (UNDER CONDITIONS OF PARA. 4.8.5)
U INPUT	LINE 1 OR LINE 2	500 (UNDER CONDITIONS OF PARA. 4.8.5)
P INPUT	LINE 1 OR LINE 2	500 (UNDER CONDITIONS OF PARA. 4.8.5)
L INPUT	LINE 1 OR LINE 2	500 (UNDER CONDITIONS OF PARA. 4.8.5)

4.7.2 THE ABOVE CALCULATED WORST CASE PROPAGATION DELAYS SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 DAYS AFTER AWARD OF CONTRACT.



AIRESEARCH MANUFACTURING COMPANY
A DIVISION OF THE AEROTRONIC CORPORATION
LOS ANGELES, CALIFORNIA

SIZE	CODE NO.	EWG NO.
A	70210	944113
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4.8 ELECTRICAL CHARACTERISTICS

THE ELECTRICAL CHARACTERISTICS SHALL APPLY AT ROOM AMBIENT TEMPERATURE.

4.8.1 POWER SUPPLIES: THE INPUT POWER SUPPLY CHARACTERISTICS ARE DEFINED BELOW:

$$V_{SS} = 0 \text{ V}$$

0.0 VDC (GROUND POTENTIAL ABOUT WHICH V_{SS} AND V_{DD} ARE REFERENCED)

$$V_{DD} = -14.0 \pm 1.0 \text{ V}$$

$$V_{\phi} = -28.5 \pm 1.5 \text{ VDC}$$

4.8.2 POWER DISSIPATION:

4.8.2.1 CALCULATED POWER: THE DC POWER DISSIPATION SHALL AT -55°C AND $+125^{\circ}\text{C}$ BE CALCULATED FOR THE DEVICE COVERED BY THIS SPECIFICATION. THE CALCULATED VALUE SHALL BE SUBMITTED TO AIRESEARCH WITHIN 45 DAYS AFTER AWARD OF CONTRACT.

4.8.2.2 MEASURED POWER: THE DC POWER DISSIPATION AT -55°C AND $+125^{\circ}\text{C}$ OF THIS DEVICE SHALL NOT EXCEED THE CALCULATED VALUE BY MORE THAN 15 PERCENT.

4.8.3 CLOCK CHARACTERISTICS: THE CLOCK CHARACTERISTICS ARE DEFINED IN FIGURE 2 OF THIS SPECIFICATION.

4.8.4 LOGIC LEVELS: THE MOS INPUT AND OUTPUT LOGIC LEVELS ARE DEFINED IN THE MATRIX BELOW:

	(MIN)	(MAX)
INPUT LOGIC "0"	-3.0 V	0.0 V
INPUT LOGIC "1"	V_{DD}	-9.0 V
OUTPUT LOGIC "0"	-2.0 V	0.0 V
OUTPUT LOGIC "1"	V_{DD}	-10.0 V

W_0 , t_{18} , FRAME MARK AND DISCRETE INPUT LOGIC LEVELS ARE DEFINED IN THE MATRIX BELOW:

	(MIN)	(MAX)
INPUT LOGIC "0"	-0.6 V	0.0 V
INPUT LOGIC "1"	-15.4 V	-12.6 V



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A Division of Airesearch Laboratories

SIZ	CODE NO.	DES. I.D.
A	70210	
SCALE	REV.	SHUTTLE 73

944113

4.8.5 OUTPUT DRIVE CAPABILITY: EACH OUTPUT SHALL BE CAPABLE OF DRIVING A LOAD TO GROUND OF 75.0 KOHNS RESISTIVE IN PARALLEL WITH A 10 pF CAPACITOR PLUS A CAPACITOR EQUAL TO FOUR TIMES THE MAXIMUM INPUT CAPACITANCE ON ANY SINGLE INPUT (EXCEPT POWER, CLOCK AND TIMING INPUTS) FOR ANY OF THE FOLLOWING CIRCUITS (P/N 244103, P/N 244111, P/N 944112, P/N 944113, P/N 944114; P/N 944118). THE CALCULATED CAPACITANCE LOAD AT -55°C AND +125°C PER ABOVE SHALL BE SUBMITTED TO AIRSEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.8.6 INPUT LOADING

4.8.6.1 TIMING AND LOGIC INPUTS: THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL TIMING AND LOGIC INPUTS (EXCEPTCLOCKS φ_1 AND φ_2) SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRSEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.8.6.2 THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL CLOCK INPUTS (φ_1 AND φ_2) SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRSEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.8.6.3 DATA INPUTS: THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL DATA INPUTS SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRSEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.



AIRSEARCH MANUFACTURING COMPANY
A Division of the General Electric Company
Schenectady, New York

SIZE	CODE NO.	DRAWING NO.
A	70210	E
SCALE	REV.	944113
		SHEET 14

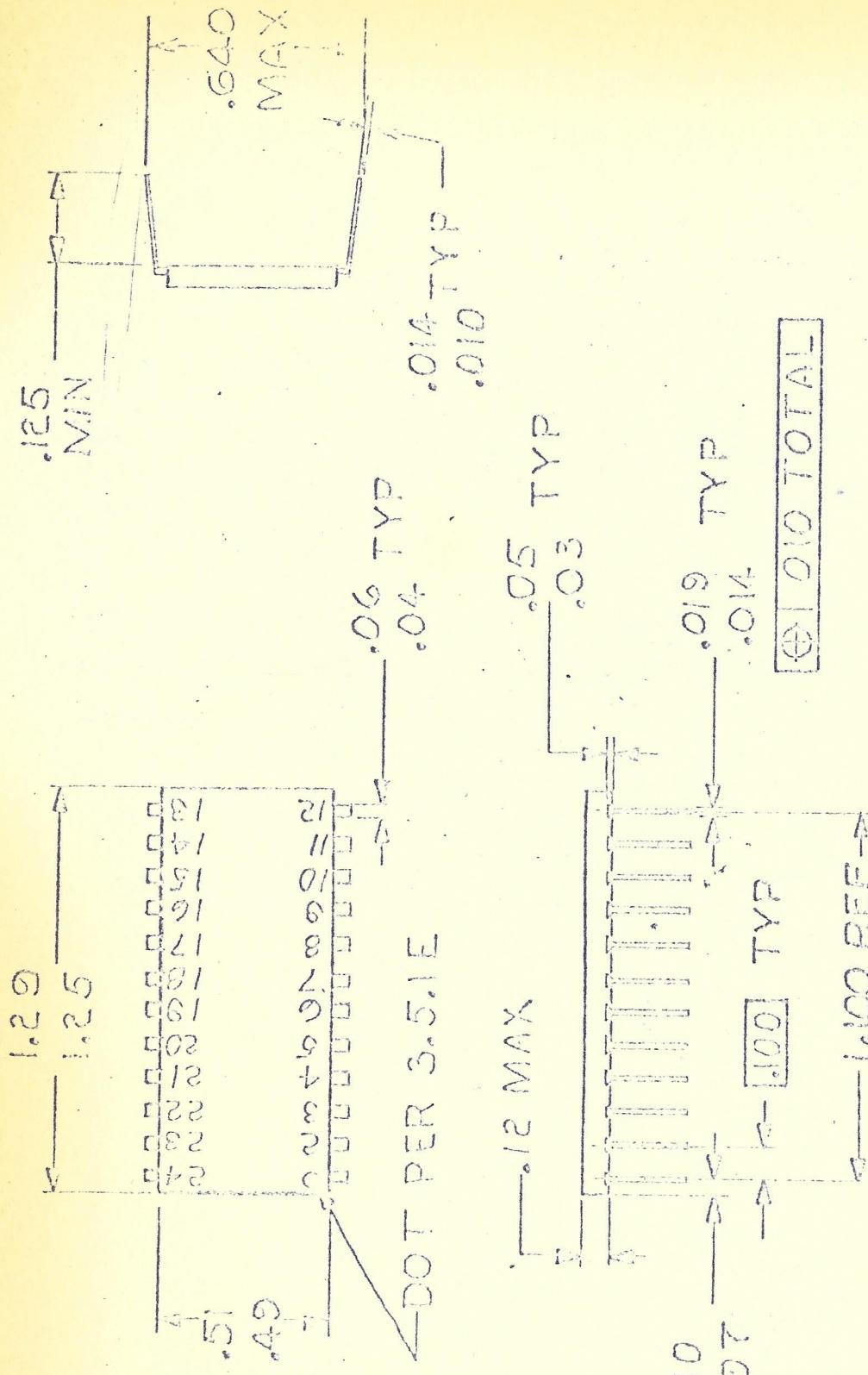
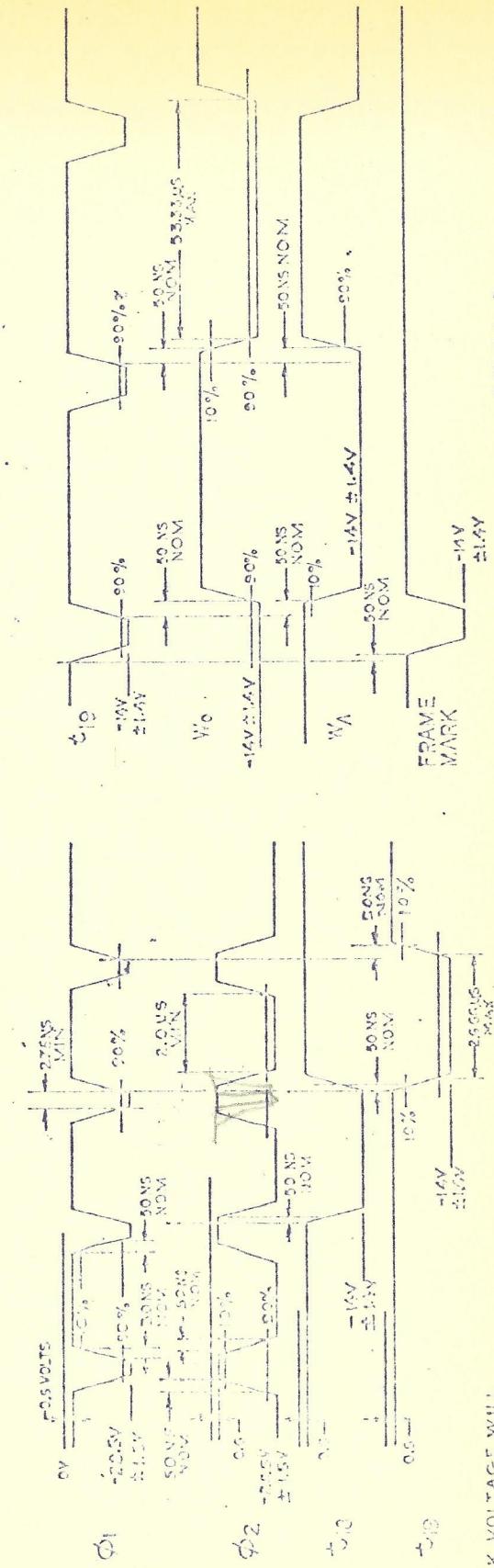
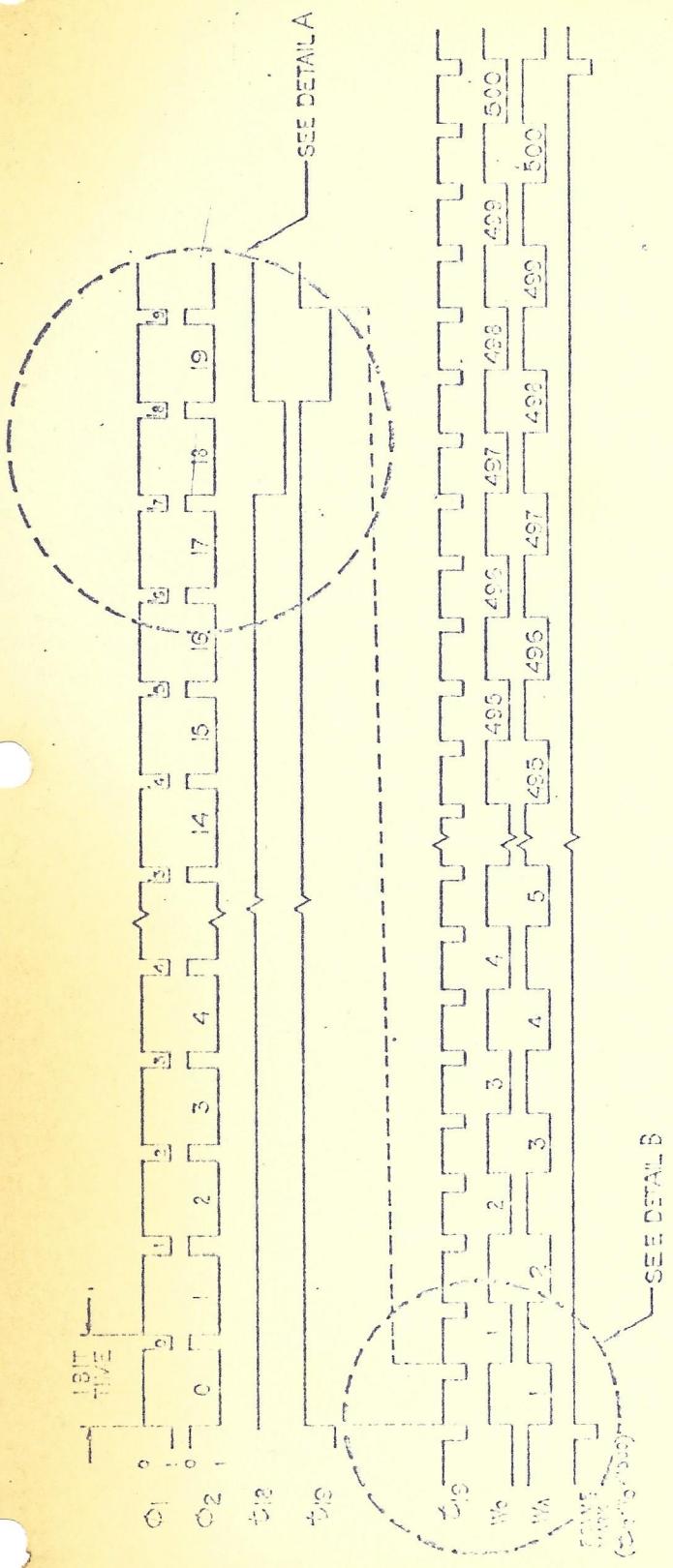


FIGURE 1 PACKAGE DRAWING

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SCALE	REV.	SHEET
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DETAIL 3

FIGURE 2a TIMING DIAGRAM

- STATIONEIS DE VADUZ. MAX DABERLE, DIAPOGRAMM POSITIVE OF THE STATION OF VADUZ.

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**AIRPORT ANGEL IS AN INDEPENDENT COMMUNITY
A CITY OF THE STATE OF TEXAS**

SIZE
A
SCALE

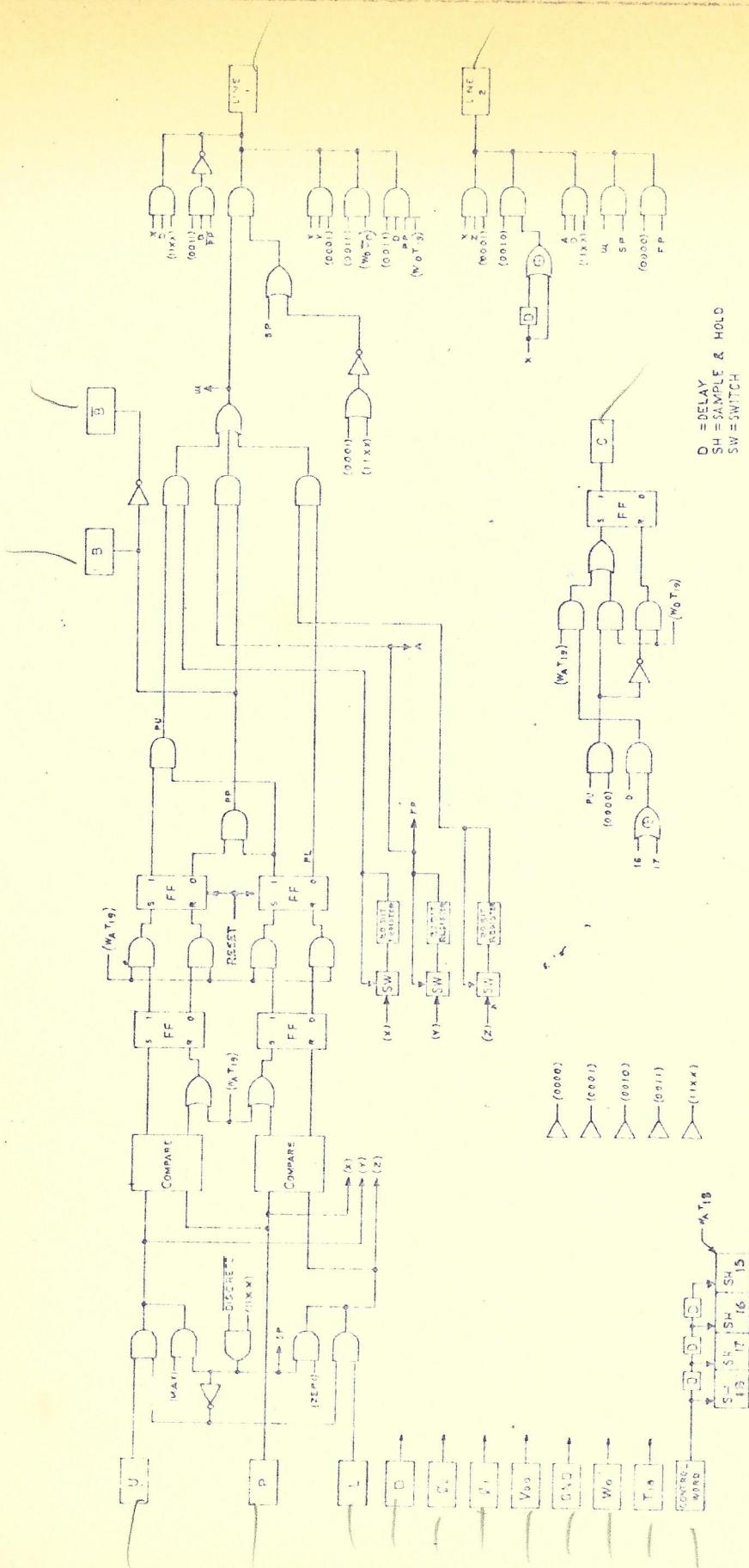
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FIGURE 3 SPECIAL LOGIC FUNCTION - BLOCK DIAGRAM



SIZE	CODE NO.	DWG NO.
A	70210	S41113
SCALE	REV	CHEK
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LOS ANGELES, CALIFORNIA

FIGURE 4 SLE = LOGIC DIAGRAM

THIS DIAGRAM HAS NOT BEEN
CHECKED BY STANUATION.

SLF P/N 944113-1

PIN NAME	PIN NUMBER	INPUT CAP.		INPUT RES.	
		MAX -55°C	+125°C	MIN -55°C	+125°C
IN	U	16	5 pf	5 M _Ω	5 M _Ω
	P	10	6 pf	5 M _Ω	5 M _Ω
	L	15	5 pf	5 M _Ω	5 M _Ω
	D	20	5 pf	5 M _Ω	5 M _Ω
	Ø ₁	21	25 pf	5 mA	2 mA
	Ø ₂	22	30 pf	18 mA	7 mA
	W ₀	17	12 pf	1 M _Ω	1 M _Ω
	t ₁₈	18	5 pf	5 M _Ω	5 M _Ω
	CW	19	5 pf	5 M _Ω	5 M _Ω
	V _{DD}	13			
OUT	GROUND	1			
	C	8			
	B	7			
	—B	6			
	L-1	9			
	L-2	11			

Chip Size: 130 x 120 mils

Number Devices: 743

Package Type: 24-pin dual in-line package

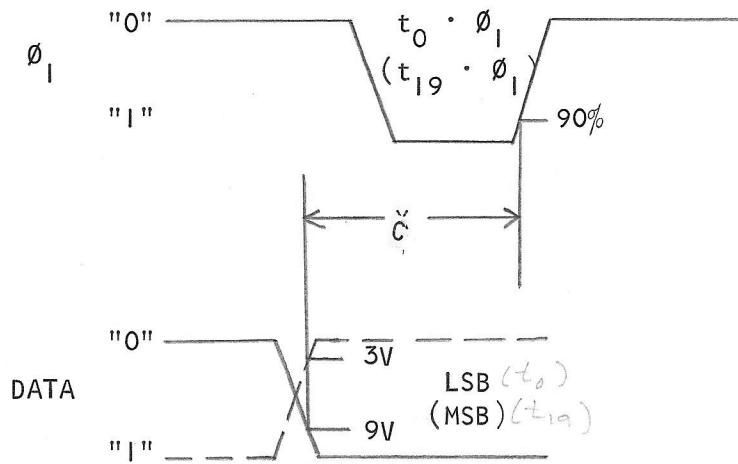
DC Power Dissipation -55°C 880 mW +125°C 365 mW

DC Power Dissipation (measured) -55°C _____ +125°C _____

Output Drive Capability Res. -55°C 75K_Ω +125°C 75K_Ω
Cap. -55°C 50pf +125°C 50pfR. M. Holt
Dept. 93-9
July 24, 1970

PROPAGATION DELAYS - ϕ_1 INPUT TERMINATIONS

CIRCUIT SLF 944113-1



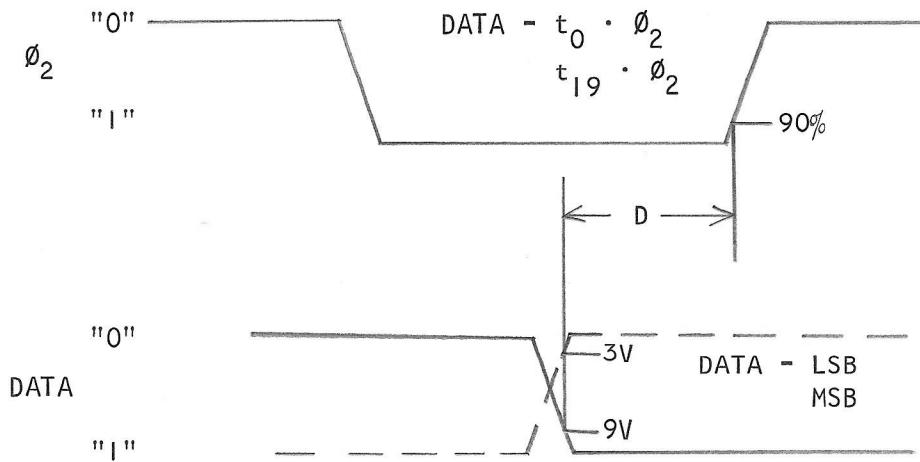
NOTES: DATA MUST NOT CHANGE DURING ϕ_1 .

TERMINAL NAME	PACKAGE TERMINAL	DATA SET-UP TIME (C) MIN
t_{18}	18	275 nS

R. M. Holt
Dept. 93-9
July 24, 1970

PROPAGATION DELAYS - \emptyset_2 INPUT TERMINATIONS

CIRCUIT SLF 944113-1

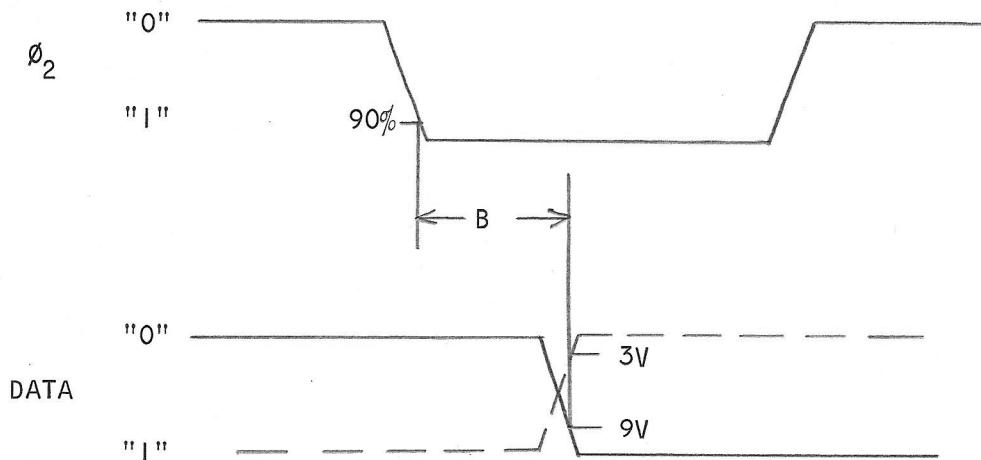


TERMINAL NAME	PACKAGE TERMINAL	DATA SET-UP TIME (D) MIN
U	16	250 nS
P	10	250 nS
L	15	250 nS
D	20	250 nS ($\emptyset_2 \cdot t_{18} \cdot w_A$)
CW IN	19	500 nS
w_0	17	1000 nS

R. M. Holt
Dept. 93-9
July 24, 1970

PROPAGATION DELAYS - \emptyset_2 OUTPUT INITIATIONS
AND STRAIGHT THROUGHS

CIRCUIT SLF 944113-1



TERMINAL NAME	PACKAGE TERMINAL	PROPAGATION DELAY (B) MAX
LINE 1 AND LINE 2 INIT.	LINE-1 9 LINE-2 11	350 nS
LINE 1 AND LINE 2 S.T.	LINE-1 9 LINE-2 11	500 nS (FROM 9V OF DATA IN)
B	7	≈ 1000 nS $(W_A \cdot t_0 \cdot \emptyset_2)$
\bar{B}	6	≈ 1000 nS $(W_A \cdot t_0 \cdot \emptyset_2)$
C	8	≈ 600 nS $(W_A \cdot t_0 \cdot \emptyset_2)$

Front
June 1970

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P	0101	1110	0000	1110	0110
L	1000	1111	0110	1001	0100
D	1110	0110	1110	0110	1001
cwin	0001	0000	0000	0000	1111
t ₁₈	0011	1011	0011	1100	1111
W ₀	1111	1111	1111	1111	1111
LINE 1	1001	XXXX	1100	XXXX	0111
LINE 2	0000	XX	0000	XX	0010

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SLF INITIATIONS
PAGE 3

SLF INIT
PAGE 3 OF 3

200

161	PAGE 3	1001	20
0 0 0	1 1 0 0	0 0 0 0	1 0 0 1
1 0 0	1 0 0 0	1 0 0 0	1 0 1 1
0 1 0	1 0 0 0	1 1 1 1	0 0 0 0
1 1 1	0 0 0 0	0 0 0 1	1 1 1 1

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LINE

LINE 2

THE JOURNAL OF CLIMATE

1. *Leucosia* *leucostoma* (L.)
2. *Leucosia* *leucostoma* (L.)

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THE LITERATURE OF THE AMERICAN RENAISSANCE

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Hector
Terry

SLF B-G
PAGE 1 OF

Y	0010	1000	1000	0000	0000	1111
P	1110	0000	0010	0010	0010	0010
L	0000	1110	0100	0100	1110	1001
D						
N	0101	0110	0110	0110	0110	0110

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NOTES 1. BLANKS ARE
 2. ZEROS.

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S-Typus

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Oct '70
Steve

SLF - STRAIGHT THROUGHS # C.E.E.
PAGE 1

SLF-ST & CEE
PAGE 1 of 3

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4	ϕ_2	00001101	10101101	01010101	10101101	00001101	00001101
P	ϕ_2	10110111	01110111	01100111	01100111	10100111	10100111
L	ϕ_2	00101011	01010101	01010101	01010101	10110101	10110101
D	ϕ_2	000100001111	000000001111	000000001111	000000001111	000000001111	000000001111

t₁₈ & 1

W. & H. [REDACTED] / [REDACTED] / [REDACTED] / [REDACTED] / [REDACTED]

LINE #2

B

P 0100 0110

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NOTES

1. BLANKS ARE
ZERO'S
 2. X'S ARE
DON'T CARES

18

Holt
5 June '70

SLF - S.T. & CEE

AIRESSEARCH MFG. Co.

(1)

DATE 4 JUNE '70

PREPARED BY R. HOLT

CHECKED BY _____

CALC. NO. _____
 MODEL _____
 PART NO. _____

	CW	U	P	L	L-1	L-2	CEE	D
1 Wo	-	0000	1011	0010	1011	-	1	0
WA	0000						0	0
2 Wo	0001	1101	0111	0101	0111	-	0	0
WA							0	0
3 Wo	0001	1010	0110	0101	0010	0100	0	0
WA							0	0
4 Wo	0010	0101	0110	1010	0100	0010	0	1
WA							0	0
5 Wo	0010	1111	0001000	0000	-	0110	0	0
WA							0	0
6 Wo	0010	1111	00100	0000	-	0110	0	0
WA							0	0
7 Wo	0010	1111	00110	0000	-	0101	0	0
WA							0	0
8 Wo	0100						0	1
WA							1	0
9 Wo	0100						0	0
WA							0	0
10 Wo	0101						0	1
WA							1	0
11 Wo	1100	0110	1010	0101	1010	-	0	1
WA		0110	1010	0101	1010		0	1
12 Wo	0110						0	1
WA							1	0
13 Wo	0110						0	0
WA							0	0
14 Wo	0111						0	1
WA							1	0
15 Wo	1110	1110	0111	1010	0111	-	0	1
WA		1110	0111	1010	0111		0	1
16 Wo	1000						0	1
WA							1	0
17 Wo	1000						0	0
WA							0	0
18 Wo	1001						0	1
WA							1	0
19 Wo	1001						0	0
WA							0	0
20 Wo	1010						0	1
WA	2 bits						1	0
WA	1010						0	0

SLF - S.T. & C.E.E.
AIRESARCH MFG. CO.

(2)

DATE 4 JUNE '70
PREPARED BY R. HOLT
CHECKED BY _____CALC. NO. _____
MODEL _____
PART NO. _____

	CW	U	P	L	L-1	L-2	CEE	D
21 W ₀	L M -2 bits						0 ✓	0
WA	1 0 1 1						0	1
22 W ₀	2 bits						1 ✓	
WA	1 0 1 1						0	0
23 W ₀	2 bits						0	0
WA	0 1 0 0						0	0
24 W ₀	2 bits						0	0
WA	1 1 0 1						0	1
25 W ₀	2 bits	0 1	1 0	1 1	1 0		0	0
WA	0 1 1 1						0	0
26 W ₀	2 bits	0 1	1 1	0 0	Picks L		0	0
WA	1 1 1 1						0	1
27 W ₀	W ₀ =2 bits	0 0	0 1	1 1	0 1	Picks U	0	0
WA	0 0 0 0						0	1

SLF TEST B-B
AIRESARCH MFG. CO.

(1)

DATE 4 JUNE '70

PREPARED BY R Holt

CHECKED BY _____

POSITIVE
VALUESCALC. NO. _____
MODEL _____
PART NO. _____

SLF COMPARATOR COMBINATIONS - I

	M	L	PICKED	B	B
U	0 1 1 1				
P	0 1 0 0				
L	0 0 0 1				
U	0 0 1 1	U > P > L	P	1	0
P	0 0 1 1				
L	0 0 1 0				
U	0 1 0 0	U > P > L	P	1	0
P	0 0 1 0				
L	0 0 1 0				
Y	0 1 0 0				
P	0 1 0 0	U > P > L	P	1	0
L	0 1 0 0				
U	0 1 1 1				
P	0 0 0 1	U > L > P	L	0	1
L	0 1 0 0				
U	0 1 0 0				
P	0 1 1 1	P > U > L	U	0	1
L	0 0 0 0				
U	0 0 0 1				
P	0 0 0 0	L > U > P	L	0	1
L	0 1 1 1				
Y	0 0 0 1				
P	0 1 0 0	P > L > U	U	0	1
L	0 0 1 0				
U	0 0 0 0				
P	0 1 0 0	L > P > U	L	0	1
L	0 1 1 1				

SLF TEST B-B
AIRESARCH MFG. CO.

(2)

DATE 9 June '70
PREPARED BY R. Holt
CHECKED BY _____NEGATIVE
VALUESCALC. NO. _____
MODEL _____
PART NO. _____

SLF COMPARATOR COMBINATIONS - 2

	m	l	PICKED	B	<u>B</u>
U	1 1 1 1		U > P > L	P	1 0
P	1 1 0 0				
L	1 0 0 1				
U	1 0 1 1				
P	1 0 1 1		U ≥ P > L	P	1 0
L	1 0 1 0				
U	1 1 0 0				
P	1 0 1 0		U > P ≥ L	P	1 0
L	1 0 1 0				
U	1 1 0 0				
P	1 1 0 0		U ≥ P ≥ L	P	1 0
L	1 1 0 0				
U	1 1 1 1				
P	1 0 0 1		U > L > P	L	0 1
L	1 1 0 0				
U	1 1 0 0				
P	1 1 1 1		P > U > L	U	0 1
L	1 0 0 0				
U	1 0 0 1				
P	1 0 0 0		L > U > P	L	0 1
L	1 1 1 1				
U	1 0 0 1				
P	1 1 0 0		P > L > U	U	0 1
L	1 0 1 0				
U	1 0 0 0				
P	1 1 0 0		L > P > U	L	0 1
L	1 1 1 1				

SLF TEST B - B
AIRESEARCH MFG. CO.

(3)

DATE 4 JUNE '70
PREPARED BY R. HOLT
CHECKED BY _____

POSITIVE

NEGATIVE
VALUESCALC. NO. _____
MODEL _____
PART NO. _____

SLF COMPARATOR COMBINATIONS - 3

	M	L	PICKED	B	B
U	0 1 1 1				
P	1 1 0 0	U > P > L	P	1	0
L	1 0 0 1				
U	0 0 1 1				
P	0 0 1 1	U ≥ P > L	P	1	0
L	1 0 1 0				
U	0 1 0 0				
P	1 0 1 0	U > P ≥ L	P	1	0
L	1 0 1 0				
U	1 1 0 0				
P	1 1 0 0	U ≥ P ≥ L	P	1	X 0
L	1 1 0 0				
U	0 1 1 1				
P	1 0 0 1	U > L > P	L	0	1
L	1 1 0 0				
U	1 1 0 0				
P	0 1 1 1	P > U > L	U	0	1
L	1 0 0 0				
U	1 0 0 1				
P	1 0 0 0	L > U > P	L	0	1
L	0 1 1 1				
U	1 0 0 1				
P	0 1 0 0	P > L > U	U	0	1
L	1 0 1 0				
U	1 0 0 0				
P	0 1 0 0	L > P > U	L	0	X
L	0 1 1 1				

SLF INITIATIONS
AIRESEARCH MFG. CO.

(1)

DATE 5 JUNE
PREPARED BY R. Holt
CHECKED BY _____

CALC. NO. _____
MODEL _____
PART NO. _____

0111W₀

L

M

U	0	1	0	1	1	1	0	1	1	0	1	1	0	1	1	0	0	0	4-picked
P	0	1	1	0	0	1	1	1	0	0	1	0	0	1	0	1	1	0	
L	0	0	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0	0	

L-1 00001110110111100000

L-2 000000000000000000000000

WA

W_A

0000

20
4W₀

OUT

IN

U	1	1	1	0	1	1	1	0	1	1	0	1	1	0	0	1	0	1	1
P	0	1	1	1	0	0	1	0	1	0	1	1	0	0	1	1	0	0	0
L	1	0	1	1	0	1	1	0	1	1	0	0	0	1	1	1	0	1	L

L-1 XXXX

L-2 0111

WA

4 28

W_A

0000

4 32

W₀

IN

U	1	1	1	0	1	1	0	0	1	1	1	0	1	1	1	1	1	1	
P	0	1	0	1	0	1	0	0	0	1	0	0	1	0	1	1	0	1	P
L	1	1	0	1	1	0	0	0	1	1	1	0	0	1	0	1	0	1	

L-1 XXXX

L-2 0101

WA

4 36

W_A

0000

4 40

W₀

IN

U	0	1	0	1	1	0	1	1	1	1	1	1	0	0	1	1	0	0	
P	0	1	1	0	0	1	0	0	1	0	1	0	1	1	0	0	1	0	P
L	0	0	0	1	1	1	0	1	1	0	0	1	1	0	0	0	0	0	

L-1 XXXX

L-2 0110

WA

4 44

SLF INITIATIONS
AIRESARCH MFG. CO.

(2)

DATE 5 June
PREPARED BY R Holt
CHECKED BY _____CALC. NO. _____
MODEL _____
PART NO. _____WA 0001 ^{WA}

4 48

W ₀	U	1 1 1 0	1 1 1 1	1 1 0 0	0 1 1 0	1 0 0 1	0 0 1 0	U
P	0 0 1 0	1 1 0 1	0 1 1 0	0 0 0 1	0 0 0 1	0 1 1 0		
L	0 1 1 0	1 0 0 1	1 0 0 1	0 1 0 0	1 1 1 0	0 1 0 0		

L-1 XXXX

L-2 XXXX

4 52

WA 0010

4 56

W ₀	U	1 1 0 0	0 1 1 0	1 0 0 1	0 0 1 0	1 1 1 1	1 0 0 1	
P	0 1 1 0	0 0 1 0	0 0 0 0	1 0 1 1	0 1 1 0	1 0 1 0	L	
L	1 0 0 1	0 1 0 0	1 1 1 0	0 1 0 0	1 0 0 1	1 1 1 0		

L-1 1100 Picked

L-2 XXXX

4 60

WA

WA

Y	1 0 0 1	0 0 1 0	1 1 1 1	1 0 0 1	0 1 1 0	0 1 1 0	
P	0 0 0 1	0 1 1 0	1 1 0 1	0 1 0 1	0 0 1 0	0 0 0 1	0
L	1 1 1 0	0 1 0 0	1 0 0 1	1 1 1 0	0 0 0 1	0 0 0 1	0 0 0

L-1 1110 Picked output

L-2 XXXX

4 68

WA

WA

0010

4 72

Y	1 1 1 1	1 0 0 1	0 1 1 0	0 0 1 1	0 0 0 1	0 0 1 0	
P	1 1 0 1	0 1 0 1	0 0 1 0	0 0 1 0	0 1 1 0	1 1 0 0	
L	1 0 0 1	1 1 0 0	0 1 0 0	0 1 0 0	0 1 0 0	0 1 0 0	0 0 0 0

L-1 1101 PICKED

L-2 XXXX

4 76

WA

WA

0001

4 80

Y	0 1 1 0	0 1 1 0 0 0	1 0 0 1 0 0	1 0 0 1 0 0	0 0 1 0	
P	0 0 1 0	0 0 1 0 0 1	0 1 1 0 0 0	0 1 0 0 0 1	0 0 0 0 0	
L	0 1 0 0	0 1 0 0 0 1	0 0 1 0 0 0	1 1 1 0 0 1	0 0 0 0 0	L

L-1 XXXX

L-2 XXXX

4 84

SLF INITIATIONS
AIRESEARCH MFG. CO.

3

DATE 6 JUNE 70
PREPARED BY R. HOLT
CHECKED BY _____

CALC. NO. _____
MODEL _____
PART NO. _____

WA 0011 w₀ w₀ w_A D = 1 488

w₀ OUT w₀ IN

Y	0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 1 0 0 1 1 0
P	0 1 1 0 1 1 0 0 0 1 0 1 0 0 0 0 0 1 0 0 1 0 0
L	0 1 0 0 1 0 0 0 1 1 1 0 0 1 0 0 0 1 0 0 0 1 0 1

L-1 1110
L-2 0000

W_A 0011 $D=0$ 496

y	1 00100100110011001000000	}	y
p	010100000010010011001000		
l	111001000100010110000111		

L-1 1101
L-2 0000

WA 0011 D = 1 4104
 W0 U 011001100100000000101100
 P 001001001100100000000010000 P
 L 010001011000011101000001

L-1 1010
L-2 0000

W_A 0100 4/12

W_0	U	P
	0 1 0 0 0 0 0 0 0 0 1 0 1 1 0 0 0 1 1 0 0 0 1 0	
P	1 1 0 0 1 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 1 0	
L	1 0 0 0 0 1 1 1 0 1 0 0 0 0 0 1 0 1 0 1 0 1 1 1	
$L-1$	1 1 0 0	
$L-2$	0 0 0 0	

SLF INITIATIONS
AIRESARCH MFG. CO.

(4)

DATE 6 JUNE 70
PREPARED BY R. HOLT
CHECKED BY _____CALC. NO. _____
MODEL _____
PART NO. _____

WA 0011

D = 1 4120

W_o Y P L

001011000110001000000010101
000010000100001010001000
010000010101011101111110

L-1 1001
L-2 0000

WA 0011

D = 0 4128

W_o Y P L

0110001000000010111001110
0100001010001000100010001111
0101011011111000010110

L-1 1100
L-2 0000

WA 1011

D = 0 4136

W_o Y P L

0000010110011100010000000000
100010001000111100101110
011111100001011001111001

L-1 0111
L-2 0000

WA 0011

D = 0 4144

W_o Y P L

1100111000100000001011110
100011110010111010001100
0001011011100111100110110

L-1 1000
L-2 0000

4148

SLF INITIATIONS
AI RESEARCH MFG. CO.

(5)

DATE 6 June '70
PREPARED BY R Holt
CHECKED BY _____CALC. NO. _____
MODEL _____
PART NO. _____ $W_A = 1100$ $D=0 \quad 4/152$ W_0

Y	0010000001011101110 0110 P
P	001011101000110011110 0110 recirculate
L	011110011110000001101001

 $L-1 \quad 0111$ $L-2 \quad 0010$

4 156

 $W_A = 1111$ $D=1 \quad 4/160$

Y	0101111011100110000000000 U
P	100011001110111111101000
L	111000000110100110010101

 $L-1 \quad \text{XXXX}$ $L-2 \quad 1000$

4 164

 $W_A = 1101$ $D=0 \quad 4/168$ W_0

Y	111001100000100011101100 P
P	1111011110000011001100 recirculate
L	01101001100101010001000 Tapped

 $L-1 \quad 1110$ $L-2 \quad 1111$

4 172

 $W_A = 1110$ $D=0 \quad 4/176$ W_0

Y	000010001110110001100000 U
P	111000001100111001100110 recirculate
L	100101010000100010011111

 $L-1 \quad 1110$ $L-2 \quad 1110$

4 180

INITIATIONS

AI RESEARCH MFG. CO.

(6)

DATE 6 June '70
 PREPARED BY R. Holt
 CHECKED BY _____

1110
1010
1000

CALC. NO. _____
 MODEL _____
 PART NO. _____

WA 0101

D = 0

4 184

W₀

Y	111011000110100000000	1001
P	110011100110000	11101111
L	0000100010010101	1111111012

Picked

L-1 1110
L-2 0000

4 188

WA 0110

D = 1

4 192

W₀

Y	011010000000010011100	1110
P	01110000111011111100000	0000
L	100101011111110110000000	0000

P

L-1 0111
L-2 0000

4 196

WA 0111

4 200

end of WA

Y	100000000100111001110
P	00001101101111000000
L	01011111111100000000

Error

1111

0000110101100001110

Pin 185-189 Preq previous 193-197 Uin 13-17
 169-173 Pin 13-17

145-149
Limit

AIRESARCH MFG. CO.

6

DATE _____

CALC. NO. _____

PREPARED BY _____

MODEL _____

CHECKED BY _____

PART NO. _____

WA 0101

D=0

Y	1110	110001	100000	1000	1001
P	1100	111001	111000	100000	1111 P
L	0000	1000100	111110101	1101	

Wain

L-1 1110
L-2 0000

UP 0110

D=1

Y	01100000	1000	1001	1100	1110
P	01111110	0000	1111	1110	00000 P
L	1001	11110101	1101	1000	0000

L-1 0111
L-2 0000

10001001	1100	1100000	
00001111	(1100000)	1110	
01011011000	0000	1111	

16 Nov 1920