

FI4A CADC
PROCESSOR
MOS DEVICE
CHARACTERISTICS

Holt

AML ENGINEERS

JIM KAWAKAMI - Project Eng.

GORDON LEIGHTON

BRIAN SHUBERT

KEN ROSE - SUPERVISOR (SYSTEMS)

PMU
944111

	# DEVICES	# CHIPS	TOTAL
PMU	1063	1	1063
PD U	1241	1	1241
SLF	743	1	743
RAS	2330	3	6990
SL	771	3	2313
ROM	3268	19	62092

SYSTEM TOTAL 74,442

ACTIVE MOS

DEVICES

PROCESSOR CARD 61,370 MOS DEVICES

4.0 LOGICAL SPECIFICATION

4.1 DEFINITION OF SYSTEM TERMS

BIT TIME: ONE COMPLETE CLOCK PERIOD, 2.66 μ SEC AT 375 KHZ.

SEE FIGURE 2.

WORD TIME: 20 CONSECUTIVE BIT TIMES (t_0 THROUGH t_{19}). THERE ARE

TWO TYPES OF "WORDS".

IN w_A , THE PARALLEL ARITHMETICAL ALGORITHMS OPERATE,
AND CONTROL WORDS ARE SHIFTED INTO THE UNITS (SERIALLY).

IN w_0 , COMPUTATIONAL INPUTS AND OUTPUTS ARE SHIFTED
SERIALLY AMONG THE UNITS.

THESE WORDS ALTERNATE, AND ARE OF EQUAL DURATION;
i.e., THEY ARE COMPLEMENTARY.

WORD MARK: A SIGNAL COINCIDENT WITH t_{18} OF EVERY WORD TIME.

OPERATION ("Op") TIME: TWO CONSECUTIVE WORD TIMES (w_A AND w_0).

FRAME MARK: FINAL BIT TIME OF THE FINAL Op.

WORD LENGTH IS 20 BITS. FOR DATA WORDS THIS IS NORMALLY SIGN AND 19 BITS.

DATA IS SHIFTED LSB FIRST. TWO'S COMPLEMENT REPRESENTATION IS USED FOR
NEGATIVE NUMBERS. DURING BIT TIME t_0 , INFORMATION IN THE COMPUTER REGISTERS
IS "PROPERLY" ORIENTED, i.e., ALL THE BITS OF A DATA WORD ARE CONTAINED IN
PROPERLY CORRESPONDING REGISTER POSITIONS. MEANINGFUL DATA TRANSFERS INTO AND
OUT OF THE LOGIC CHIPS AND REGISTERS OCCUR DURING w_0 OF EVERY Op.

4.2 GENERAL DESCRIPTION

PMU SHALL ACCEPT TWO SERIAL INPUTS AS MULTIPLICAND AND MULTIPLIER IN ONE WORD
TIME (w_0), PRODUCE THEIR PROPERLY ROUNDED PRODUCT BY MEANS OF A PARALLEL
ALGORITHM IN ONE MORE WORD TIME (w_A), AND SHIFT THE PRODUCT OUT IN THE NEXT w_0
WHILE INPUTS FOR THE NEXT OPERATION ARE SIMULTANEOUSLY SHIFTED IN. THE
CONTENTS OF THE M REGISTER SHALL ALSO BE SHIFTED OUT DURING THIS TIME. THIS
OPERATION SHOULD BE ACHIEVED USING BOOTH'S ALGORITHM. THE UNIT SHALL BE



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A	70210	E 944111
SCALE	REV	SHEET
		2

CAPABLE OF OPERATING CONTINUALLY IN THIS MANNER. FIGURE 3 IS A SUGGESTED BLOCK DIAGRAM FOR PERFORMING THIS FUNCTION.

4.3 INPUTS AND OUTPUTS

PROVISIONS SHALL BE MADE FOR ACCEPTING ELECTRICAL AND LOGICAL INPUTS AS FOLLOWS: PHASE 1 AND PHASE 2 CLOCKS, V_{DD} , GROUND, A W_0 SIGNAL (20 CLOCK PERIODS LONG), A ± 18 SIGNAL, AND TWO DATA INPUTS. THE TWO DATA INPUTS SHALL BE REFERRED TO AS M_{IN} (MULTIPLICAND IN) AND R (MULTIPLIER). TWO OUTPUTS SHALL BE PROVIDED, THESE SHALL BE REFERRED TO AS M (MULTIPLICAND) AND P (PRODUCT).

4.4 THE LOGIC DIAGRAM IN FIGURE 4 IS INCLUDED AS A SUPPLEMENT TO THE WRITTEN SPECIFICATION.

4.5 SYSTEM CONSIDERATIONS

THE MULTIPLIER WILL BE TYPICALLY CONNECTED IN THE SYSTEM AS SHOWN IN FIGURE 6. THE MULTIPLICAND INPUT CAN COME FROM STEERING OUTPUT 1, THE MULTIPLIER FROM STEERING OUTPUT 2. THE M AND P OUTPUTS CAN BE CONNECTED TO ANY OF THE STEERING INPUTS. ALL TIMING SIGNALS WILL BE GENERATED FROM THE SYSTEM TIMING GENERATOR. OUTPUT DRIVE CAPABILITY IS DISCUSSED IN PARAGRAPH 4.6.5.

4.5.1 PROPAGATION DELAYS

TO INSURE PROPER INTERFACE OF THIS CIRCUIT WITH THE OTHERS IN THE SYSTEM, THE FOLLOWING PROPAGATION DELAY TIMES MUST BE MET. ALL TIMES ARE MAXIMUM AND ARE MEASURED FROM THE 90% LOGICAL "1" LEVEL OF THE CLOCK TO THE 90% LEVEL OF THE SIGNAL.

FROM	TO	TIME (NS)
M INPUT	M REGISTER	125
R INPUT	R REGISTER	125
M_1 REGISTER STAGE	M OUTPUT	250 (UNDER CONDITIONS OF PARA. 4.6.5)
LSB ADDER STAGE	P OUTPUT	250 (UNDER CONDITIONS OF PARA. 4.6.5)



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~~ALL DATA OUTPUTS SHALL BE CHANGED ON THE NEGATIVE TRANSITION OF THE
PHASE 1 CLOCK.~~

4.5.2 THE ABOVE CALCULATED WORST CASE PROPAGATION DELAYS SHALL BE SUBMITTED TO
AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF
CONTRACT.

4.5.1 Propagation Delays

To insure proper interface
of this circuit with others in the
system the propagation delays
in Figures — — — must be
met



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		SHEET 11

4.6 ELECTRICAL CHARACTERISTICS

THE ELECTRICAL CHARACTERISTICS SHALL APPLY AT ROOM AMBIENT TEMPERATURE.

4.6.1 POWER SUPPLIES: THE INPUT POWER SUPPLY CHARACTERISTICS ARE DEFINED BELOW:

$$V_{SS} = 0 \text{ V}$$

0.0 VDC (GROUND POTENTIAL ABOUT WHICH V_{SS} AND V_{DD} ARE REFERENCED)

$$V_{DD} = -14.0 \pm 1.0 \text{ V}$$

$$V_{\phi} = -28.5 \pm 1.5 \text{ VDC}$$

4.6.2 POWER DISSIPATION:

4.6.2.1 CALCULATED POWER: THE DC POWER DISSIPATION SHALL AT -55°C AND $+125^{\circ}\text{C}$ BE CALCULATED FOR THE DEVICE COVERED BY THIS SPECIFICATION. THE CALCULATED VALUE SHALL BE SUBMITTED TO AIRESEARCH WITHIN 45 DAYS AFTER AWARD OF CONTRACT.

4.6.2.2 MEASURED POWER: THE DC POWER DISSIPATION AT -55°C AND $+125^{\circ}\text{C}$ OF THIS DEVICE SHALL NOT EXCEED THE CALCULATED VALUE BY MORE THAN 15 PERCENT.

4.6.3 CLOCK CHARACTERISTICS: THE CLOCK CHARACTERISTICS ARE DEFINED IN FIGURE 2 OF THIS SPECIFICATION.

4.6.4 LOGIC LEVELS: THE MOS INPUT AND OUTPUT LOGIC LEVELS ARE DEFINED IN THE MATRIX BELOW:

	(MIN)	(MAX)
INPUT LOGIC "0"	-3.0 V	0.0 V
INPUT LOGIC "1"	V_{DD}	-9.0 V
OUTPUT LOGIC "0"	-2.0 V	0.0 V
OUTPUT LOGIC "1"	V_{DD}	-10.0 V

W_0 , t_{18} , FRAME MARK AND DISCRETE INPUT LOGIC LEVELS ARE DEFINED IN THE

MATRIX BELOW:

	(MIN)	(MAX)
INPUT LOGIC "0"	-0.6 V	0.0 V
INPUT LOGIC "1"	-15.4 V	-12.6 V



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SCALE	REV.	SHEET 12

4.6.5 OUTPUT DRIVE CAPABILITY: EACH OUTPUT SHALL BE CAPABLE OF DRIVING A LOAD TO GROUND OF 75.0 KOMS RESISTIVE IN PARALLEL WITH A 10 pF CAPACITOR PLUS A CAPACITOR EQUAL TO FOUR TIMES THE MAXIMUM INPUT CAPACITANCE ON ANY SINGLE INPUT (EXCEPT POWER, CLOCK AND TIMING INPUTS) FOR ANY OF THE FOLLOWING CIRCUITS (P/N 944125, P/N 944111, P/N 944112, P/N 944113, P/N 944114; P/N 944118). THE CALCULATED CAPACITANCE LOAD AT -55°C AND +125°C PER ABOVE SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.6.6 INPUT LOADING

4.6.6.1 TIMING AND LOGIC INPUTS: THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL TIMING AND LOGIC INPUTS (EXCEPTCLOCKS ϕ_1 AND ϕ_2) SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.6.6.2 THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL CLOCK INPUTS (ϕ_1 AND ϕ_2) SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.6.6.3 DATA INPUTS: THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL DATA INPUTS SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.



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THE HILLSIDE, CALIFORNIA

SIZE	CODE NO.	DWG NO.
A	70210	944111
SCALE	REV.	CLIENT
		10

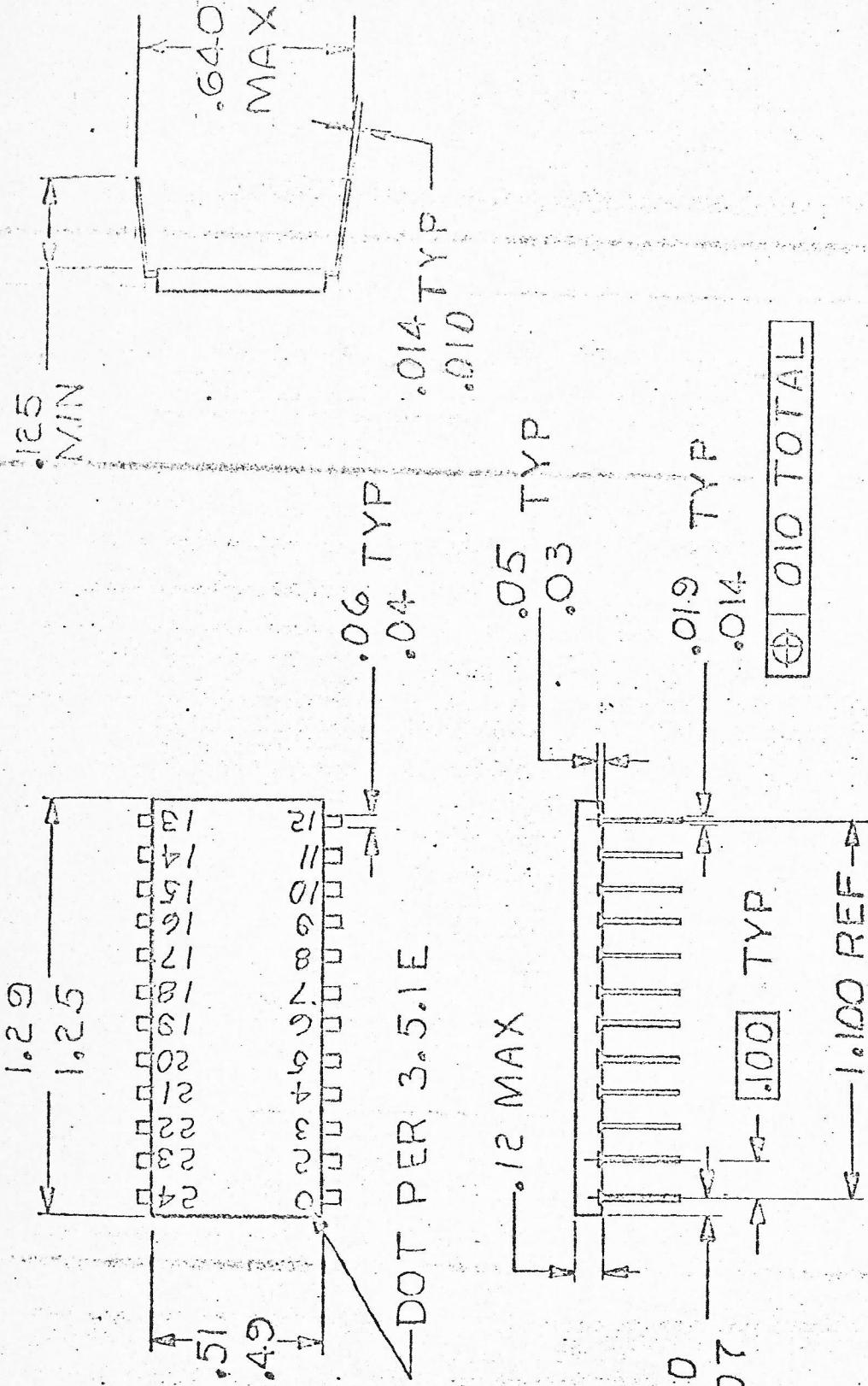
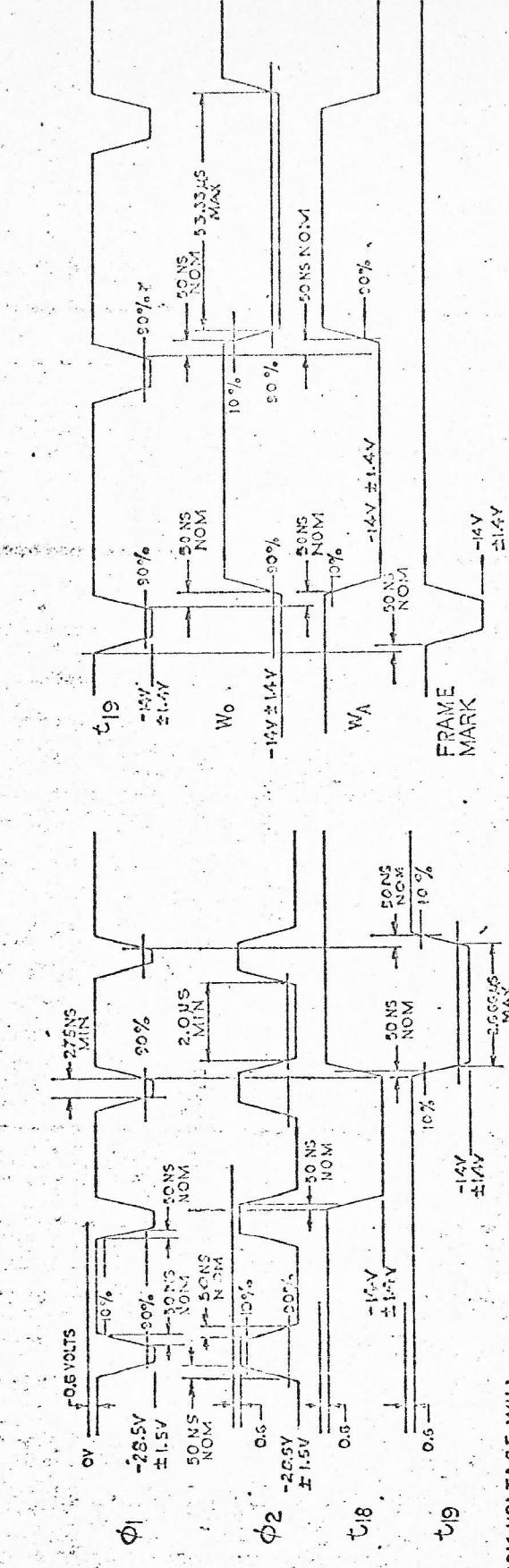
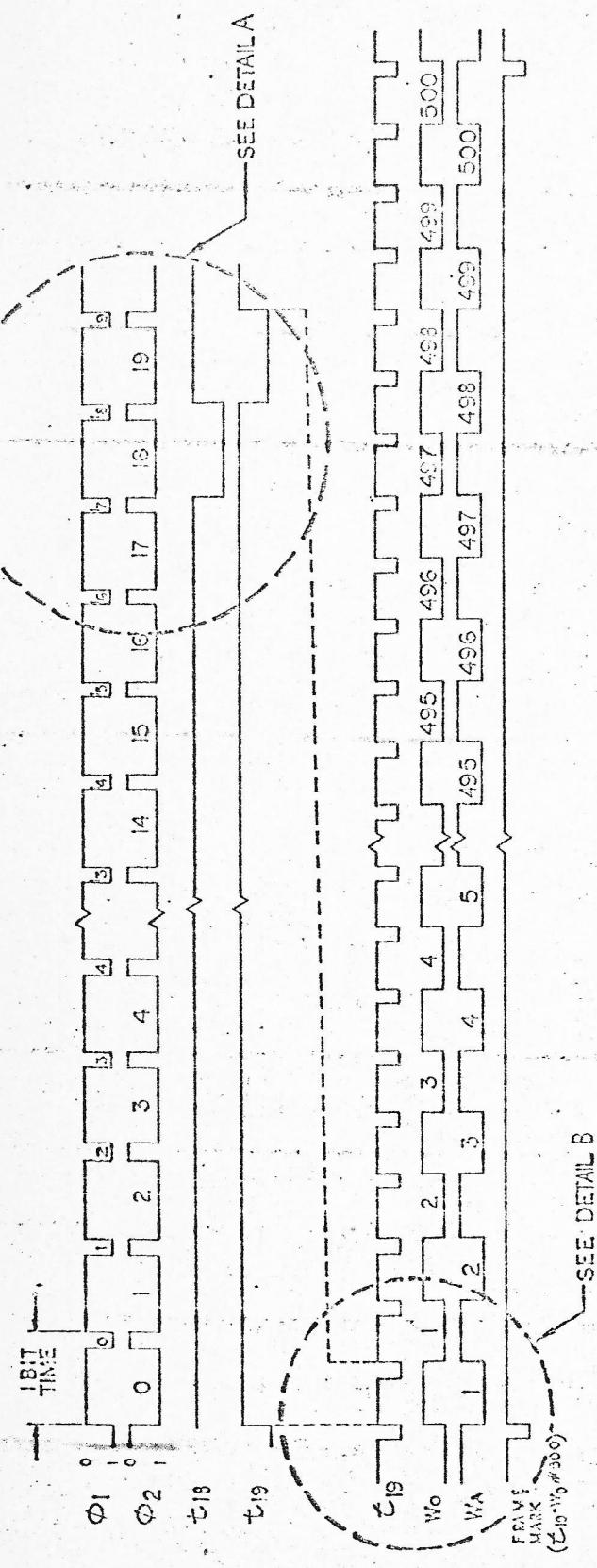


FIGURE 1. PACKAGE DRAWING



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SCALE	REV	SHEET 20



DETAIL B

FIGURE 2a TIMING DIAGRAM

DETAIL A

- CLOCK VOLTAGE WILL NOT GO POSITIVE
- MAX OVERLAP ϕ_1 AND ϕ_2 VOLTAGE IS 3.0 VOLTS

NOTES:



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SCALE	REV	SHEET 21

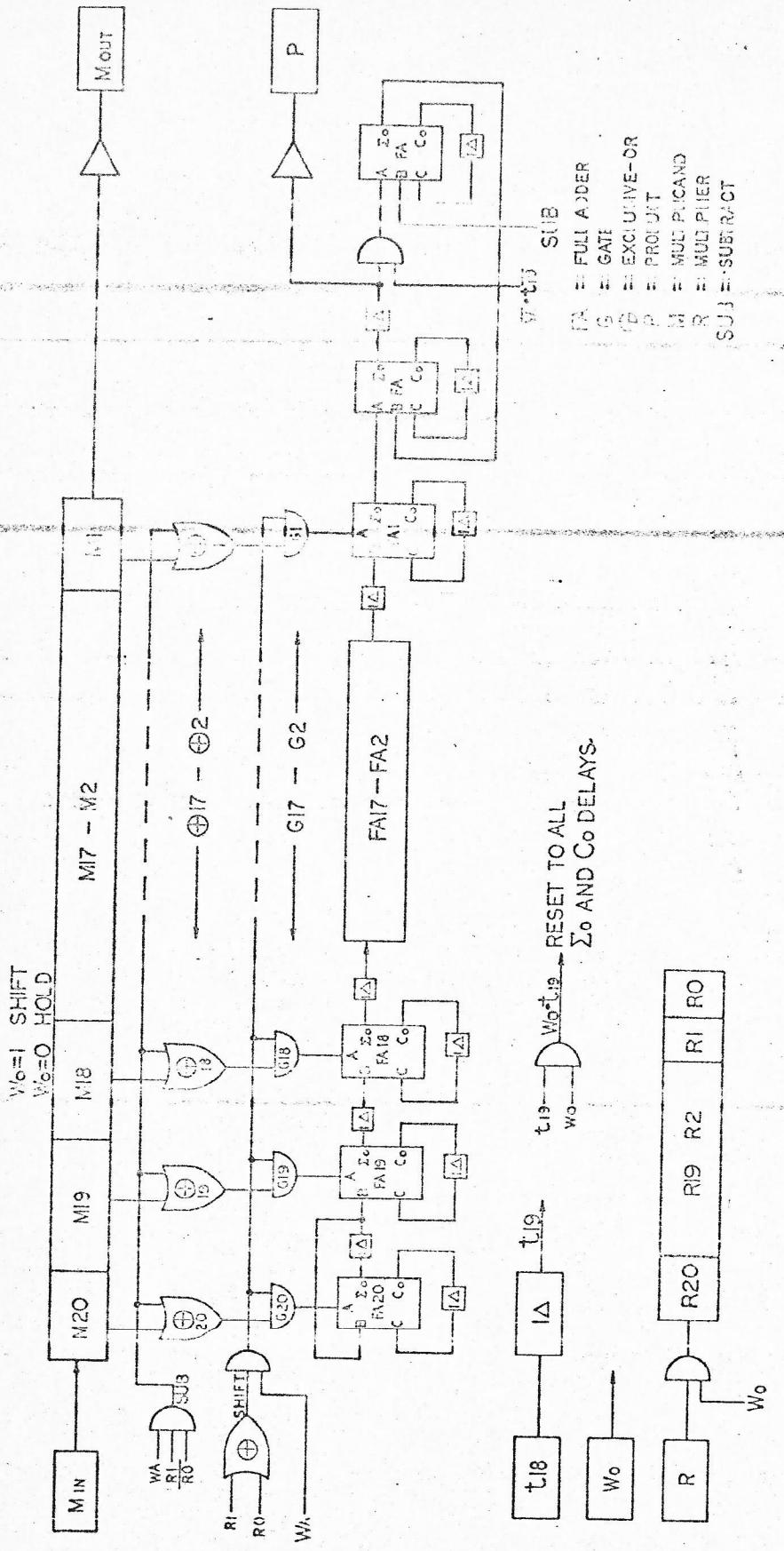


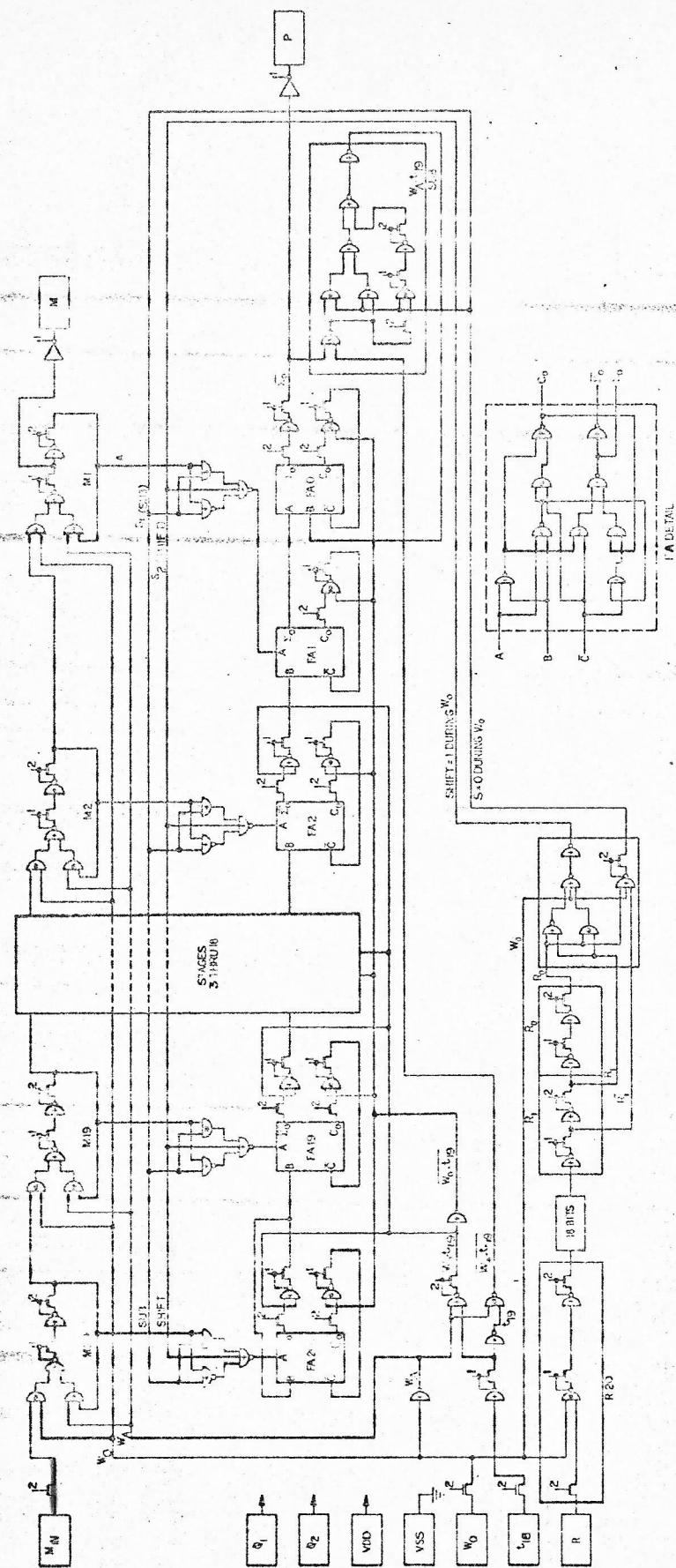
FIGURE 3 PMU - BLOCK DIAGRAM



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SCALE	REV	SHEET
		944111

FIGURE 4 PMU - LOGIC DIAGRAM



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SIZE	CODE NO.	DWG NO.
A	70210	944111
SCALE	REV	SHEET
1	1	24

PARALLEL MULTIPLIER P/N 944111-1

PIN NAME	PIN NUMBER	INPUT CAP.		INPUT RES.	
		MAX -55°C	+125°C	MIN -55°C	+125°C
IN {	5	5 pf	5 pf	5 M _Ω	5 M _Ω
	18	5 pf	5 pf	5 M _Ω	5 M _Ω
	19	5 pf	5 pf	5 M _Ω	5 M _Ω
	4	15 pf	15 pf	1 M _Ω	1 M _Ω
	17	40 pf	40 pf	6 mA	3 mA
	7	45 pf	45 pf	4 mA	2 mA
OUT {	9				
	8				
	20				
	6				

Chip Size: 150 x 153 mils

Number Devices: 1063

Package Type: 24-pin dual in-line package

DC Power Dissipation -55°C 1.15W +125°C .450W

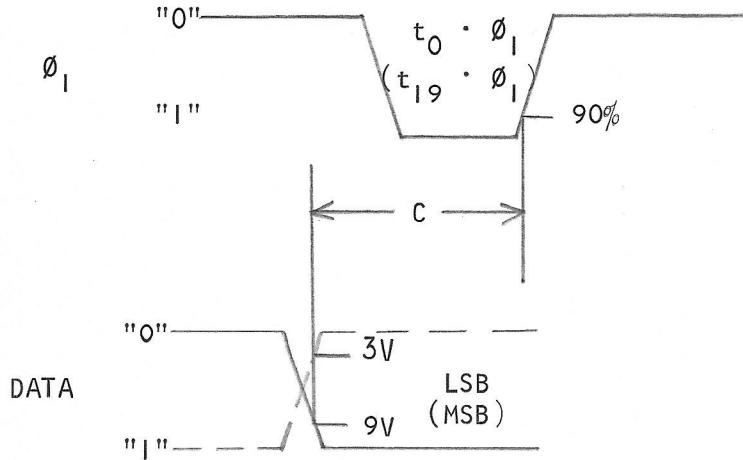
DC Power Dissipation (measured) -55°C _____ +125°C _____

Output Drive Capability Res. +55°C 75K_Ω +125°C 75K_Ω
Cap. +55°C 50pf +125°C 50pf

R. M. Holt
Dept. 93-9
July 24, 1970

PROPAGATION DELAYS - \emptyset_1 INPUT TERMINATIONS

CIRCUIT PMU - 944111-1

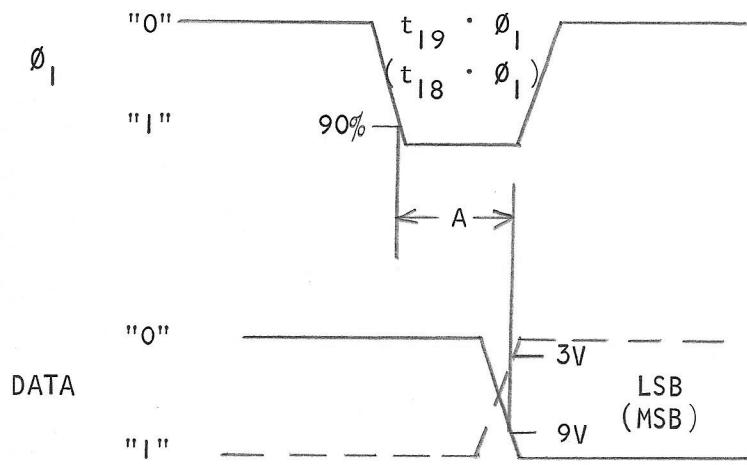


NOTES: DATA MUST NOT CHANGE DURING \emptyset_1 .

TERMINAL NAME	PACKAGE TERMINAL	DATA SET-UP TIME (C) MIN
M IN	5	275 nS
R IN	18	275 nS
t_{18}	19	275 nS

PROPAGATION DELAYS - \emptyset , OUTPUT INITIATIONS

CIRCUIT PMU 944111-1

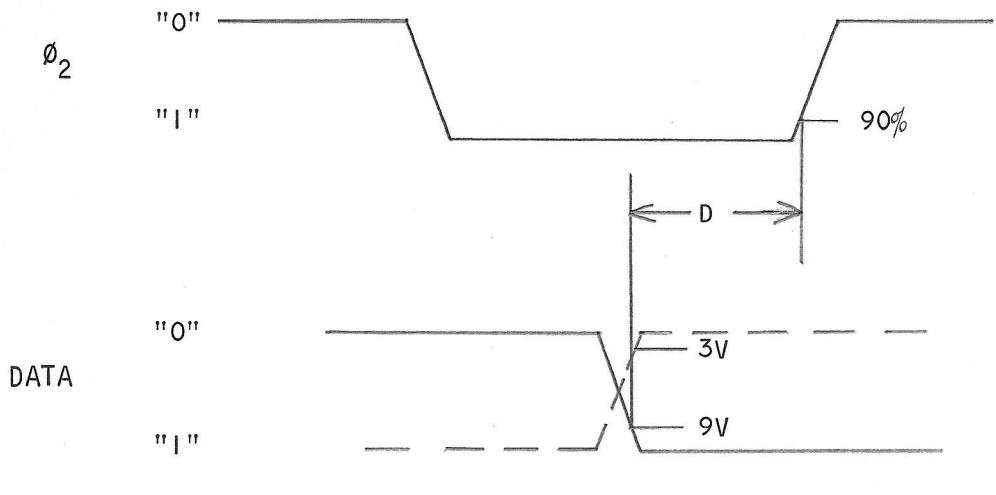


TERMINAL NAME	PACKAGE TERMINAL	PROPAGATION DELAY (A) MAX
M OUT	9	300 nS
P OUT	8	300 nS

R. M. Holt
Dept. 93-9
July 24, 1970

PROPAGATION DELAYS - ϕ_2 INPUT TERMINATIONS

CIRCUIT PMU 944111-1



TERMINAL NAME	PACKAGE TERMINAL	DATA SET-UP TIME (D) MIN
W_0	4	1000 nS

R. M. Holt
Dept. 93-9
July 24, 1970

AIRESEARCH MFG. CO.

DATE 3-28-70PREPARED BY Holt

CHECKED BY _____

CALC. NO. _____

MODEL _____

PART NO. _____

Test Words PMU

#1 $M = 1\ 000\ 0\ 1000\ 1\ 0000\ 1\ 100\ 1\ 0\ 222$
 $R = 1\ 001\ 0\ 1010\ 1\ 1010\ 1\ 0100\ 1$
 $P = (0) \begin{smallmatrix} m_{SB} \\ 0 \end{smallmatrix} 1\ 100\ 1\ 1100\ 001\ 0001\ 1110\ ---$
 $1\ 111101000100000010x$

$\Sigma = 421$ ↑ double sign from previous word.

#2 $M = 0\ 1111\ 0111011110001101\ 205$
 $R = 1\ 001\ 0\ 101010101010001$
 $P = (0) \begin{smallmatrix} 1 \\ 00 \end{smallmatrix} 1\ 1000111101110011---$
 $1\ 101101100001010101x$

$\Sigma = 421$

#3 $M = 0\ 0\ 1\ 01100100011001111$
 $R = 1\ 001\ 0000101010101010$
 $P = (0) \begin{smallmatrix} 1 \\ 10 \end{smallmatrix} 1\ 101100101000000001\ 33$
 $00001101110110110x$

$\Sigma = 454$

#4 $M = 1\ 001\ 00000000000000100$
 $R = 0\ 000000000000001000101$
 $P = (0) \begin{smallmatrix} 1 \\ 10 \end{smallmatrix} 1\ 11111111111000100$
 $1010000000100010100x$

#5 $M = 1\ 1000001111110101011$
 $R = 1\ 00000010101000111011$
 $P = (0) \begin{smallmatrix} 00 \\ 11 \end{smallmatrix} 1\ 1100101111011111$
 $1010101101001101001x$

$$\frac{2}{2} \cdot \frac{4}{4} \\ \frac{1}{1} \cdot \frac{0}{0} \\ \frac{1}{1} \cdot \frac{5}{5} \\ \frac{1}{1} \cdot \frac{0}{0}$$

$$\frac{4}{4} \cdot \frac{6}{6} \\ \frac{2}{2} \cdot \frac{10}{10} \\ \frac{1}{1} \cdot \frac{2}{2} \\ \frac{1}{1} \cdot \frac{0}{0}$$

$$\frac{1}{1} \cdot \frac{8}{8} \\ \frac{2}{2} \cdot \frac{14}{14} \\ \frac{1}{1} \cdot \frac{2}{2} \\ \frac{1}{1} \cdot \frac{0}{0}$$

$$\frac{1}{1} \cdot \frac{8}{8} \\ \frac{2}{2} \cdot \frac{14}{14} \\ \frac{1}{1} \cdot \frac{2}{2} \\ \frac{1}{1} \cdot \frac{0}{0}$$

$$2.2 \cdot \frac{10}{10} \\ \text{LOADING ON M.O.S. CHIP UNIT}$$

$$4.6 \cdot \frac{10}{10} \\ \text{CAPACITIVE LOADING ON M.O.S. CHIP OUTPUTS}$$

PKG #	Pin Output #	CHIP NAME	CIRCUIT CAP. LOAD (C_L) _{pf}	P.C. BD.	BD CAP. \times (C_B) _{pf}	TOTAL CAP. LOAD $C_L + C_B$ pf	MAX LENGTH OF P.C. CONDUCTOR(m)
U9	10 OUT 1	SL-PNU	5	7.8	1.95	8.8	5.8
	12 OUT 2		5	5.0	1.95	6.9	5.8
	4 OUT 3		10 40	5.5	1.95	7.4	5.8
U10	10 OUT 1	SL-PNU	5	1.0	1.0	2.0	1.0
	12 OUT 2		5	1.0	1.0	2.0	1.0
	4 OUT 3		10 40	1.0	1.0	2.0	1.0
U11	10 OUT 1	SL-SLF	5	27	0.675	27.675	1.0
	12 OUT 2		5	27	0.675	27.675	1.0
	4 OUT 3		10 46	27	0.675	27.675	1.0
U12	10 OUT 1	RNU	5	1.0	0.25	1.25	0.25
	12 OUT 2		5	1.0	0.25	1.25	0.25
	4 OUT 3		10 46	1.0	0.25	1.25	0.25
U13	19 MOUNT	PNU	10	24.5	0.25	24.75	0.25
	8 P OUT		10	19.2	0.25	19.45	0.25
	20 Q OUT		10	19.2	0.25	19.45	0.25
U14	29 ONE	SLF	30	7.4	0.25	7.65	0.25
	Two		30	7.4	0.25	7.65	0.25
	B		5	7.4	0.25	7.65	0.25
U15	11 C	RAS-PNU	10	2.8	0.1	2.9	0.1
U16	13 DATA OUT	RAS-PDU	30+5	2.4	0.1	2.5	0.1
U17	13 DATA OUT	RAS-SLF	30+5	2.4	0.1	2.5	0.1
	13 DATA OUT	ROM (1-3)	30+5	2.4	0.1	2.5	0.1
	13 DATA OUT	ROM (5-7)	40	2.0	0.1	2.1	0.1
	13 DATA OUT	ROM (8)	22	2.0	0.1	2.1	0.1
	13 DATA OUT	ROM (9-11)	22	2.0	0.1	2.1	0.1
	13 DATA OUT	ROM (12)	20	2.0	0.1	2.1	0.1
	13 DATA OUT	ROM (13)	10	2.0	0.1	2.1	0.1
	13 DATA OUT	ROM (4-16)	22	2.0	0.1	2.1	0.1
	13 DATA OUT	ROM (17-20)	18+5	2.0	0.1	2.1	0.1

AIRESARCH MFG. CO.

DATE _____

CALC. NO. _____

PREPARED BY _____

MODEL _____

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PART NO. _____

$$T_p = \sqrt{Lc}$$

$$\sqrt{\frac{L}{c}} = z$$

$$T^2 = LC$$

$$\frac{L}{C} = z^2$$

$$C = \frac{T^2}{L} = \frac{z^2}{0.22}$$

$$L = C \cdot 22$$

~~a. $c^2 = \frac{z^2}{2^2}$~~

~~$\frac{2.41 \text{ pF}}{in}$~~

~~$\frac{0.2}{.01} \frac{5}{4.45}$~~

~~$c = \frac{T}{z} =$~~

~~$0.6 \text{ ns} \times 2.54 \text{ in}$~~

~~$c = \frac{(0.6)(2.54)}{40} \times 10^{-9} \Rightarrow 1 \text{ pF}$~~

~~$C = 3.82 \text{ pF}$~~

~~$\frac{100}{4}$~~

~~$\frac{200}{42}$~~

~~$3 / \frac{(0.6)(2.54)}{25} = \frac{152.5}{25} = 6.1 \text{ pF}$~~

REPORT

PAGE

OF

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$$\frac{(9)(4)(5)}{1 - \frac{2.8}{20}} = \frac{(9)(5)}{\frac{17.2}{20}} = \frac{9(4.5)(5)}{17.2}$$

$$\frac{(4.5)(5)}{17.2} = 5.23 \text{ pF/inch}$$

JRC TM□

5.23 pF/inch

□

2.25 pF/in

3.82

1361meas

5 pF

6.1

AIRESEARCH MFG. CO.

4 (1675
3.75

DATE _____

CALC. NO. _____

PREPARED BY _____

MODEL _____

CHECKED BY _____

PART NO. _____

4 to 1 scale

Package Pin

Z 36	415	13
Z 37	416	13
Z 38	417	13
Z 33	412	8
Z 33		9
Z 34	413	20
Z 35	414	16
Z 35		20
Z 35		11
Z 30	49	2
		4
		10
Z 31	410	12
		2
		4
		10
		12
Z 32	411	2
		4
		10
		12

$$9\frac{1}{2} + 8 = 17\frac{1}{2} \quad \frac{1}{4} = 4.4''$$

ON BD $46/4 = 12''$ OFF BD $13.5''$ 5.4 $\frac{1}{4}$

(1) J18-19
1 J06-09

13.5

t = .01

J17-19

J07-09

25.5"

.212

AIRESEARCH MFG. CO.

REV 1

DATE 7-16-70
PREPARED BY R. Holt
CHECKED BY _____CALC. NO. _____
MODEL _____
PART NO. _____

FI4A CAD/CAM TIMING SIGNAL LOADING REQ'D

	ϕ_1 CAP pf	ϕ_1 RES μ	ϕ_2 CAP pf	ϕ_2 RES μ	t_{18} pf	W_0 pf
PMU	40	6 ma / 3 ma	45	4 ma / 2 ma	5-5M	15-1M
PDU	35	6.3 / 3.2 ma	45	0	5-5M	13-1M
SLF	25	5 / 2 ma	30	18 / 7 ma	5-5M	12-1M
SL-PMU	50	1M	50	50 / 20 ma	10-1M	10-1M
SL-PDU	50	1M	50	50 / 20 ma	10-1M	10-1M
SL-SLF	50	1M	50	50 / 20 ma	10-1M	10-1M
RAS-PMU	115	3.5 / 1 ma	115	17.2 / 6 ma	10 - 10M	10 - 10M
RAS-PDU	115	3.5 / 1 ma	115	17.2 / 6 ma	10 - 10M	10 - 10M
RAS-SLF	115	3.5 / 1 ma	115	17.2 / 6 ma	10 - 10M	10 - 10M
ROW-1	10	1.5 / .6 ma	35	0.1 / .04 ma	5-10M	—
-2	10	1.5 / .6	35	0.1 / .04	5-10M	—
-3	10	1.5 / .6	35	0.1 / .04	5-10M	—
-5	10	1.5 / .6	35	0.1 / .04	5-10M	—
-6	10	1.5 / .6	35	0.1 / .04	5-10M	—
-7	10	1.5 / .6	35	0.1 / .04	5-10M	—
-8	10	1.5 / .6	35	0.1 / .04	5-10M	—
-9	10	1.5 / .6	35	0.1 / .04	5-10M	—
-10	10	1.5 / .6	35	0.1 / .04	5-10M	—
-11	10	1.5 / .6	35	0.1 / .04	5-10M	—
-12	10	1.5 / .6	35	0.1 / .04	5-10M	—
-13	10	1.5 / .6	35	0.1 / .04	5-10M	—
-14	10	1.5 / .6	35	0.1 / .04	5-10M	—
-15	10	1.5 / .6	35	0.1 / .04	5-10M	—
-16	10	1.5 / .6	35	0.1 / .04	5-10M	—
-17	10	1.5 / .6	35	0.1 / .04	5-10M	—
-18	10	1.5 / .6	35	0.1 / .04	5-10M	—
-19	10	1.5 / .6	35	0.1 / .04	5-10M	—
-20	10	1.5 / .6	35	0.1 / .04	5-10M	—
<u>785</u>		<u>56.4</u>	<u>1280</u>	<u>225.5</u>	<u>170 pf</u>	<u>100 pf</u>
<u>pb</u>		<u>22.69</u>	<u>pb</u>	<u>(87.76)</u>	<u>174 ma</u>	<u>189 ma</u>
<u>ma</u>						

WITHOUT SAFETY FACTORS

ADD 15% Safety factor plus
board capacitance.

REPORT

PAGE

OF