

SECTION 3

COMPUTER AIDS

Throughout the development phase of the processor, several computer programs were developed to aid the engineer in his analysis and ROM bit pattern verification.

The first of these were the two single failure analysis programs written for the PMU and the PDU. The objective of these programs was to determine a set of operands that could be used as test words for the inflight diagnostics. These programs essentially took each module of combinational logic (adders) on the chips and determined single failure modes for them. By stepping the program through the appropriate arithmetic algorithm, different types of input binary patterns were seen to propagate to the output particular single failures. Five sets of operands were finally chosen for each arithmetic unit such that each set would propagate at least 98 percent of the single failures, i.e., to the result (product or quotient). A subsequent report will discuss in detail the procedure used to determine these test words. The program was written by Jim Lallas of Dept. 93-34.

The second computer program was the simulation program. The objective of this program was to verify the accuracy of the organization of the processor and to provide a convenient means of obtaining, via printout, immediate data generated during the computational cycle of the CADC. The purpose was to eliminate errors in system definition that would result in large amounts of nonrecurring dollars being spent on respecifying LSI circuits, especially ROM's. The program was set up to accomplish the following:

- (a) Proof that the simulation will check all errors in the organization of the CADC.
- (b) Proof that the program will be versatile enough to obtain data printouts at any point in the timing of the system.
- (c) Proof that the cost of performing this simulation will pay for itself.
- (d) Proof that a digital CADC can be adequately checked out on a large-scale computing system.
- (e) Proof that the programming approach will be general enough to be used on other digital systems similar to this one.

The simulation was written at the bit level from a functional point of view. Each defined LSI circuit (PMU, PDU, steering, RAS, SLF, and ROM) was written as a subroutine. Then through a wiring subroutine, the different circuits could be connected. The simulation then steps through the program and performs all the calculations exactly as they would be performed by the hardware. An additional check is made on the propagation delays of each programmed path and indicates if the maximum allowable time has been exceeded.



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Several different forms of printout are available from the program. These are shown in Figures 3-1 through 3-11.

- (1) Title page with date, time, user name
- (2) Control ROM listing
- (3) Data ROM listing
- (4) Sensor memory data listing
- (5) Input coding form listing
- (6) Pictorial of wiring connection
- (7) Listing of inputs used (P_{si} , P_{ti} , A/D, discretes, etc.)
- (8) Diagnostic printout of each operation for each chip input and output
- (9) Propagation delay time summary
- (10) Output data summary
- (11) Listing of ROM with AMI format

An option is provided to punch out a ROM card deck containing the bit patterns of all the ROM's. This card deck is in format as required by AMI, the ROM vendor. Figure 3-11 shows a listing of a ROM in this format.

The program thus far has been successfully used on two F-14A CADC mechanizations because only 1 error out of 104,960 bits (41 ROM's) went undetected. A succeeding report will describe the details of the simulation. The program was written by Bill Holt, Jim Lallas, and K. T. Chang of Dept. 93-34.

The third program is a plotting program that plots via CalComp plotter the computer program drawing. Inputs to the program are the data set from the simulation and a valid output matrix from the responsible engineer. This matrix contains valid programmed chip outputs versus operation number. Figure 3-12 shows a sample plot from this program. Each block contains complete information necessary to follow the transferring of data. This includes data words, control words, steering inputs and outputs, and RAS inputs and outputs. The total time to plot the computer program is approximately 15 hr. If desirable, an option is available to plot in section. The program was written by Jessica Kuo of Dept. 93-34.

The fourth and final program is presently being developed. This is the software package that is to be delivered to GAC to support flight test. Since complete documentation will be available at a later date, only a brief description of the program is given below.



The package is set up to enable the customer (GAC) to reprogram certain functions with minimum turnaround. The input to the package is raw data points and the outputs are data listings, printer plots, CalComp plots, AMI card decks, and REM tapes. All of the above are available for each function.

The program was initially started by Jim Lallas and Bill Holt. Pete Miller, Murray Lubliner, K. T. Chang, C. Y. Chin, Jessica Kuo, and Al Gaede are presently continuing the program.



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LOS ANGELES, CALIFORNIA

1100 Wilshire Boulevard • Los Angeles, California 90017 • (213) 637-1000

F14A CENTRAL AIR DATA COMPUTER SIMULATION PROGRAM

PROGRAM USER W. B. HOLT

DATE 17 NOV 70 TIME 14:01:44

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Figure 3-1. Simulation Title Page



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CONTROL #	READY-ONLY MEMORY F/N 944226-23	NAME & B, MDT	DATE 17 NOV 70 TUE 14101 44
1	2	3	4
00011000000001111000	00010000000001111000	0111010100000001000100	00011000000001000100
7	8	9	10
0000000100000001000100	00101000000001000100	0000010100000001000100	00111000000001000100
13	23	14	15
0000010100000001000100	01001000000001000100	0010100011011110000	000001010000001000100
19	33	20	21
0011001001111001010	01011001111100000	00110000000001000100	01011000000001000100
25	39	26	40
00000001000111111000	0000001010000001000100	00011000000001000100	00000001000111111000
31	53	32	34
00100001101111111000	0000001010000001000100	00111000000001000100	00101000000001000100
37	57	38	39
00100001010111111000	000001010000001000100	0001000110000001000100	0000010100000001000100
43	71	44	45
00100000000001000100	01001000000001000100	01010001101111111000	01000000000001000100
49	79	50	54
000001010000000001000100	0010100000000001000100	001110010011100001000	0000010100000001000100
55	92	56	57
00010000000001000100	00000001001111111000	01010001101111111000	01000000000001000100
61	116	62	63
0100000000011000000	010011001011100100	0000010100000001000100	00011100101111000000
67	122	68	123
00000100000001000100	0001100010111100100	00000101000001000100	00000101000001000100
73	128	74	75
00000100000001000100	00011000101111000100	000001010000001000100	00011000101111000100
79	134	80	135
00000100000001000100	01010100101111000100	000001010000001000100	00011000101111000100
85	140	56	141
00000100000001000100	00000000000001000100	00000000000001000100	00000000000001000100
91	146	92	147
0101000000001111000	111101110111110000	00000000000001111000	00000000000001111000
97	152	98	153
0000000000001111000	00000000000001111000	00000000000001111000	00000000000001111000
103	158	104	159
11110001011111000	0001100020000100000	00000000000001111000	00000000000001111000

Figure 3-2. Simulation - Control ROM Listing Pm4 Control 4

(CONTINUED)

READ-ONLY MEMORY P/N 94-125-25

NAME W. B. HOLT DATE 17 NOV 70 TIME 14101114

109	169	110	170	111	176	112	179	113	180	114	185
0001000010111000000	0001010000001000100	111101010000001000100	111100001000100	1111000010110100000	1111000010110100000	111100001000100	111100001000100	1111100000001020103			
115	186	116	187	117	188	118	189	119	190	120	191
111100001011111000	00000101000001000100	0001110100011010000	00010110111010000	001011101111000100	000001001011111000100	000001001011111000100	000001001011111000100	11100101000001020100			
121	192	122	196	123	197	124	198	125	199	126	200
1111010100001000100	00000001100011000100	0110100000001000000	0110110000000100000	0110110000000100000	000000000101111111000	000000000101111111000	000000000101111111000				
127	201	128	202								
000101000001000100	000101000001000100										



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Figure 3-2. (Continued)

CONSTANTINE

READ-ONLY MEMORY P/N 944125-23

2

NAME W. B. HOLT DATE 17 NOV 32 TIME 111211 A

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Figure 3-3. Simulation - Data ROM Listing Pin# DATA /

(CONTINUED) READ-ONLY MEMORY P/N 944125-24 NAME W. R. HOLT DATE 17 NOV 78 TIME 14:01:44

109	181	110	182	111	183	112	184	113	185	114	186
01100110G311110J0110	001110110101111101	0011101001100001011	0011101011101100110	001100000101011000010	0011100001100	01110	001100001100	01110	001100001100	01110	001100001100
,54971750	,48192406	,454610A2	,46455002	,46455002	,46455002	,46455002	,46455002	,46455002	,46455002	,46455002	,46455002
115	187	116	188	117	189	118	190	119	191	120	192
011100010111010001	01110111010001	001100010011010001	001100010011010001	000011000110100011	000011000011100001	0011000011100001	0011000011100001	0011000011100001	0011000011100001	0011000011100001	0011000011100001
,90909004	,89399962	,26822090	,123	,194	,123	,195	,124	,196	,199	,126	,200
121	193	122	194	123	195	124	196	125	199	126	,3696020
1101110001000110	0001000011100001011	000100010011110100	000100010011110100	00000001100101001111	00010001010101001111	00010001010101001111	00010001010101001111	00010001010101001111	0100001110110101	0100001110110101	000001
,2891922	,15345692	,128	,202	,16110992	,16110992	,16110992	,16110992	,16110992	,13350386	,152801794	
127	201	128	202	16110992	16110992	16110992	16110992	16110992	16110992	16110992	
0110110011111110001	01100100010110001001	01100100010110001001	01100100010110001001	01100100010110001001	01100100010110001001	01100100010110001001	01100100010110001001	01100100010110001001	01100100010110001001	01100100010110001001	01100100010110001001
,65153389	,78295271										



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Figure 3-3. (Continued)



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NUMBER	D	NAME	W, B, HOLT	DATE	17 NOV 70	TIME	14:01:14
1	2	3	4	5	6		
0000000000000000	0111111111111111	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
7	8	9	10	11	12		
0000000000000000	0111111111111111	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
13	20	14	15	16	17	18	19
0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
19	26	20	21	22	23	24	25
0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
1	27	21	28	22	23	24	31
0111111111111111	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
999999809	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
*	*	*	*	*	*	*	*

NUMBER	B	NAME	W, B, HOLT	DATE	17 NOV 70	TIME	14:01:14
1	2	3	4	5	6		
0000000000000000	0111111111111111	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
7	8	9	10	11	12	13	14
0000000000000000	0111111111111111	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
13	20	14	15	16	17	18	19
0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
19	26	20	21	22	23	24	25
0111111111111111	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
999999809	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
*	*	*	*	*	*	*	*

Figure 3-4. Simulation - Sensor Memory Listing

SENSOR MEMORY

PMU - STEERING CODING FORM

DATE 17 NOV 70

	* N *	* R *	* SELECTED *	* SELECTED *	* S *	* S *	
	STORAGE	TO	TO	TO	TO	TO	COMMENTS
	* 14	* 14	* 14	* 14	* 14	* 14	
	SELECTED	OUTPUT 1*	OUTPUT 2*	OUTPUT 3*	OUTPUT 4*	OUTPUT 5*	
	P	E	E	E	E	E	
	* 1 2 3 4 * 5 *	* 6 7 8 9 *	* 0 1 2 3 *	* 4 5 6 7 *	* 8 9 0 *		
	*****	*****	*****	*****	*****	*****	*****
1	0 0 0 1	0	0 0 0 1	0	0 0 0 1	0	
2	1 0 0 1	0	0 0 1 0	0	0 1 1 1	0	
3	0 1 1 1	0	1 0 1 0	0	0 0 0 0	1	
4	0 1 1 1	0	0 0 1 0	0	0 1 1 1	0	
5	0 1 1 1	0	0 0 1 0	0	0 0 0 0	1	
6	0 1 1 1	0	0 0 1 0	0	0 1 1 1	0	
7	0 1 1 1	0	0 0 1 0	0	0 1 1 1	0	
8	0 0 0 1	1	0 0 1 0	0	0 0 0 1	1	
9	0 0 0 0	0	0 0 1 0	0	0 1 1 1	0	
10	0 0 0 0	0	0 0 1 0	0	0 1 1 1	0	
11	0 0 0 0	0	0 0 1 0	0	0 0 0 0	1	
12	0 0 0 0	0	0 0 1 0	0	0 0 0 0	1	
13	0 0 0 0	0	0 0 1 0	0	0 0 0 0	1	
14	0 0 0 0	0	0 0 1 0	0	0 0 0 0	1	
15	0 0 1 0	1	0 0 1 0	0	0 1 1 1	1	
16	0 0 1 0	0	0 0 1 0	0	0 1 1 1	1	
17	0 0 1 0	0	0 0 1 0	0	0 0 0 0	1	
18	0 0 1 0	0	0 0 1 0	0	0 0 0 0	1	
19	0 0 1 0	0	0 0 1 0	0	0 0 0 0	1	
20	0 0 1 0	0	0 0 1 0	0	0 0 0 0	1	
21	0 0 1 1	1	0 0 1 1	0	0 1 1 1	1	
22	0 0 1 0	0	0 0 1 1	0	0 0 0 0	1	
23	0 0 1 0	0	0 0 1 0	0	0 0 0 0	1	
24	0 0 1 0	0	0 0 1 0	0	0 0 0 0	1	
25	0 0 1 0	0	0 0 1 1	0	0 0 0 0	1	
26	0 0 1 0	1	0 0 1 1	0	0 0 0 0	1	
27	0 0 1 0	0	0 0 1 1	0	0 0 0 0	1	
28	0 0 1 0	0	0 0 0 0	0	0 0 0 0	1	
29	0 0 1 0	0	0 0 0 0	0	0 0 0 0	1	
30	0 0 0 1	0	0 0 1 1	0	0 0 0 0	1	
31	0 0 0 1	0	0 0 1 1	0	0 0 0 0	1	
32	0 1 0 0	1	0 0 1 0	0	0 0 0 0	1	
33	0 0 1 0	1	0 0 1 0	0	0 1 1 0	0	
34	0 0 1 0	1	0 0 1 0	0	0 1 1 0	0	
35	0 0 1 1	0	0 0 1 0	0	0 1 0 0	0	
36	0 1 0 1	1	0 0 1 0	0	0 0 0 0	1	
37	0 0 1 0	1	0 0 1 0	0	0 0 0 0	1	
38	0 0 1 0	0	0 0 1 0	0	0 1 1 1	1	
39	0 0 0 0	0	0 0 1 0	0	0 1 1 1	1	
40	0 0 0 0	0	1 0 1 0	0	0 0 0 0	1	
41	0 0 0 0	0	1 0 1 0	0	0 0 0 0	1	
42	0 0 0 0	0	1 0 1 0	0	0 0 0 0	1	
43	0 0 0 1	1	0 0 1 0	0	0 0 0 0	1	
44	0 0 0 0	0	0 0 1 0	0	0 1 1 1	0	
45	0 0 0 0	0	0 0 1 0	0	0 1 1 1	0	
46	0 0 0 0	0	0 0 1 0	0	0 0 0 0	1	
47	0 0 0 0	0	0 0 1 0	0	0 0 0 0	1	
48	0 0 0 0	0	0 0 1 0	0	0 0 0 0	1	
49	0 0 0 0	0	0 0 1 0	0	0 0 0 0	1	
50	0 0 0 0	0	0 0 1 0	0	0 0 0 0	1	

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Figure 3-5. Simulation - Input Coding Form

PHU - CONSTANT ROM

DATE 17 NOV 70

S	O	P	G	N	1	2	3	4	5	6	7	8	COMMENTS
301	*	*	*	*	0	1	0	0	0	0	0	0	
302	*	*	*	*	0	1	0	0	0	0	0	0	
303	*	*	*	*	0	1	0	0	1	0	0	0	
304	*	*	*	*	0	2	7	7	9	1	0	0	
305	*	*	*	*	0	0	1	5	4	3	7	2	
306	*	*	*	*	0	1	4	2	2	3	0	9	
307	*	*	*	*	0	1	5	9	4	1	1	2	
308	*	*	*	*	0	1	3	0	6	8	9	8	
309	*	*	*	*	0	1	3	3	5	2	9	7	
310	*	*	*	*	0	1	5	4	3	5	5	0	
311	*	*	*	*	0	1	0	3	5	6	2	1	
312	*	*	*	*	0	1	2	3	4	5	7	9	
313	*	*	*	*	0	1	2	3	4	5	4	2	
314	*	*	*	*	0	1	2	6	5	0	9	4	
315	*	*	*	*	0	1	0	0	1	5	4	2	
316	*	*	*	*	0	1	0	0	0	4	0	2	
317	*	*	*	*	0	1	0	0	0	4	0	2	
318	*	*	*	*	0	1	0	0	0	4	3	0	
319	*	*	*	*	0	1	0	0	2	4	2	1	
320	*	*	*	*	0	1	0	0	7	1	9	7	
321	*	*	*	*	0	1	5	4	1	5	5	6	
322	*	*	*	*	0	1	0	0	1	0	6	8	
323	*	*	*	*	0	1	0	0	0	1	6	9	
324	*	*	*	*	0	1	0	0	0	1	4	7	
325	*	*	*	*	0	1	0	0	2	9	4	7	
326	*	*	*	*	0	1	0	0	4	9	1	2	
327	*	*	*	*	0	1	1	4	1	1	3	0	
328	*	*	*	*	0	1	0	4	3	9	0	1	
329	*	*	*	*	0	1	0	0	4	3	9	1	
330	*	*	*	*	0	1	2	9	1	3	2	2	
331	*	*	*	*	0	1	0	0	4	8	1	2	
332	*	*	*	*	0	1	1	4	1	1	3	0	
333	*	*	*	*	0	1	1	4	1	1	3	0	
334	*	*	*	*	0	1	5	4	0	0	0	0	
335	*	*	*	*	0	1	5	4	0	0	0	0	
336	*	*	*	*	0	1	5	4	0	0	0	0	
337	*	*	*	*	0	1	5	4	0	0	0	0	
338	*	*	*	*	0	1	5	5	0	0	0	0	
339	*	*	*	*	0	1	5	5	0	0	0	0	
340	*	*	*	*	0	1	0	7	1	1	1	1	
341	*	*	*	*	0	1	0	8	2	3	2	2	
342	*	*	*	*	0	1	0	8	2	3	2	2	
343	*	*	*	*	0	1	0	8	2	3	2	2	
344	*	*	*	*	0	1	0	8	3	0	0	0	
345	*	*	*	*	0	1	0	8	3	0	0	0	
346	*	*	*	*	0	1	0	8	3	0	0	0	
347	*	*	*	*	0	1	0	8	3	0	0	0	
348	*	*	*	*	0	1	0	8	3	0	0	0	
349	*	*	*	*	0	1	0	8	3	0	0	0	
350	*	*	*	*	0	1	0	8	3	0	0	0	

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Figure 3-5. (Continued)



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STEERING HARDWARE CONNECTIONS

PMU STEER OUT 3	* EXT 1	***** OUTPUT 1
RAS (PDU)	* EXT 2	
PDU STEER OUT 3	* EXT 3	
RAS (PMU)	* EXT 4	***** OUTPUT 2
SLF CHIP LINE 1	* EXT 5	
SLF CHIP LINE 2	* EXT 6	PMU
RIS (SLF)	* EXT 7	
SENSOR MEMORY	* EXT 8	***** OUTPUT 3
COUNTER (PS)	* EXT 9	
SLF STEER OUT 3	* EXT 10	
COUNTER (PT)	* EXT 11	***** SIGMA 1
PRODUCT (PMU)	* EXT 12	
MULTIPLICAND REG	* EXT 13	***** SIGMA 2

PMU STEER OUT 3	* EXT 1	***** OUTPUT 1
RAS (PDU)	* EXT 2	
PDU STEER OUT 3	* EXT 3	
RAS (PDU)	* EXT 4	***** OUTPUT 2
SLF CHIP LINE 1	* EXT 5	
SLF CHIP LINE 2	* EXT 6	PDU
RAS (SLF)	* EXT 7	
ROM (SLF 22)	* EXT 8	***** OUTPUT 3
SLF STEER OUT 3	* EXT 9	
ADC	* EXT 10	***** SIGMA 1
GUGENT (PDU)	* EXT 11	
SENSOR MEMORY	* EXT 12	***** SIGMA 2
	* EXT 13	

PMU STEER OUT 3	* EXT 1	***** OUTPUT 1
RAS (PDU)	* EXT 2	
PDU STEER OUT 3	* EXT 3	
RAS (SLF)	* EXT 4	***** OUTPUT 2
SLF STEER OUT 3	* EXT 5	
SLF CHIP LINE 2	* EXT 6	SLF
RAS (PMU)	* EXT 7	
ROM (SLF 1)	* EXT 8	***** OUTPUT 3
ROM (SLF 2)	* EXT 9	
T 19	* EXT 10	***** SIGMA 1
ROM (PDU)	* EXT 11	
SLF CHIP LINE 1	* EXT 12	***** SIGMA 2
*	EXT 13	



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Figure 3-6. Simulation - Wiring Pictorial

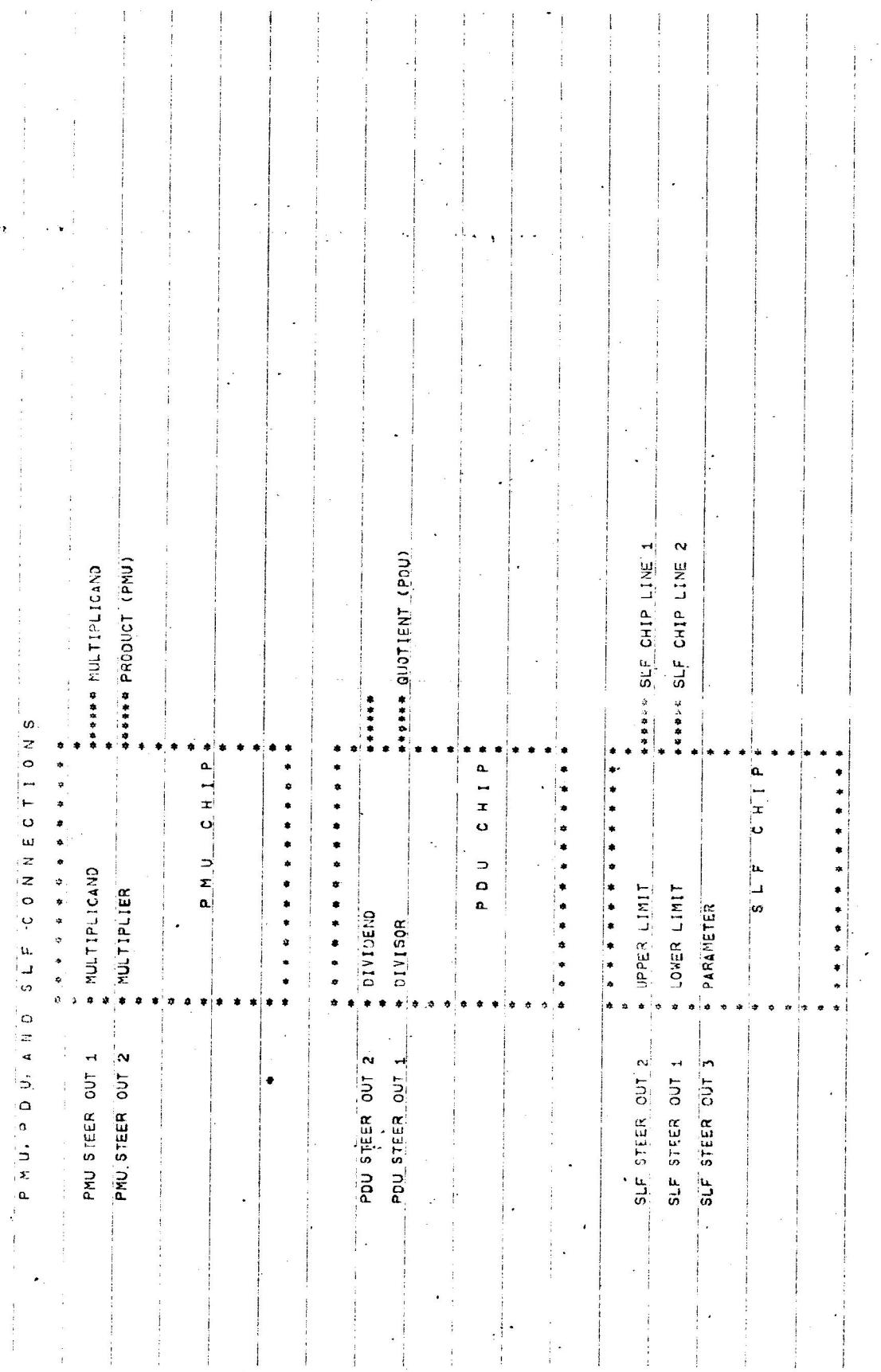


Figure 3-6. (Continued)



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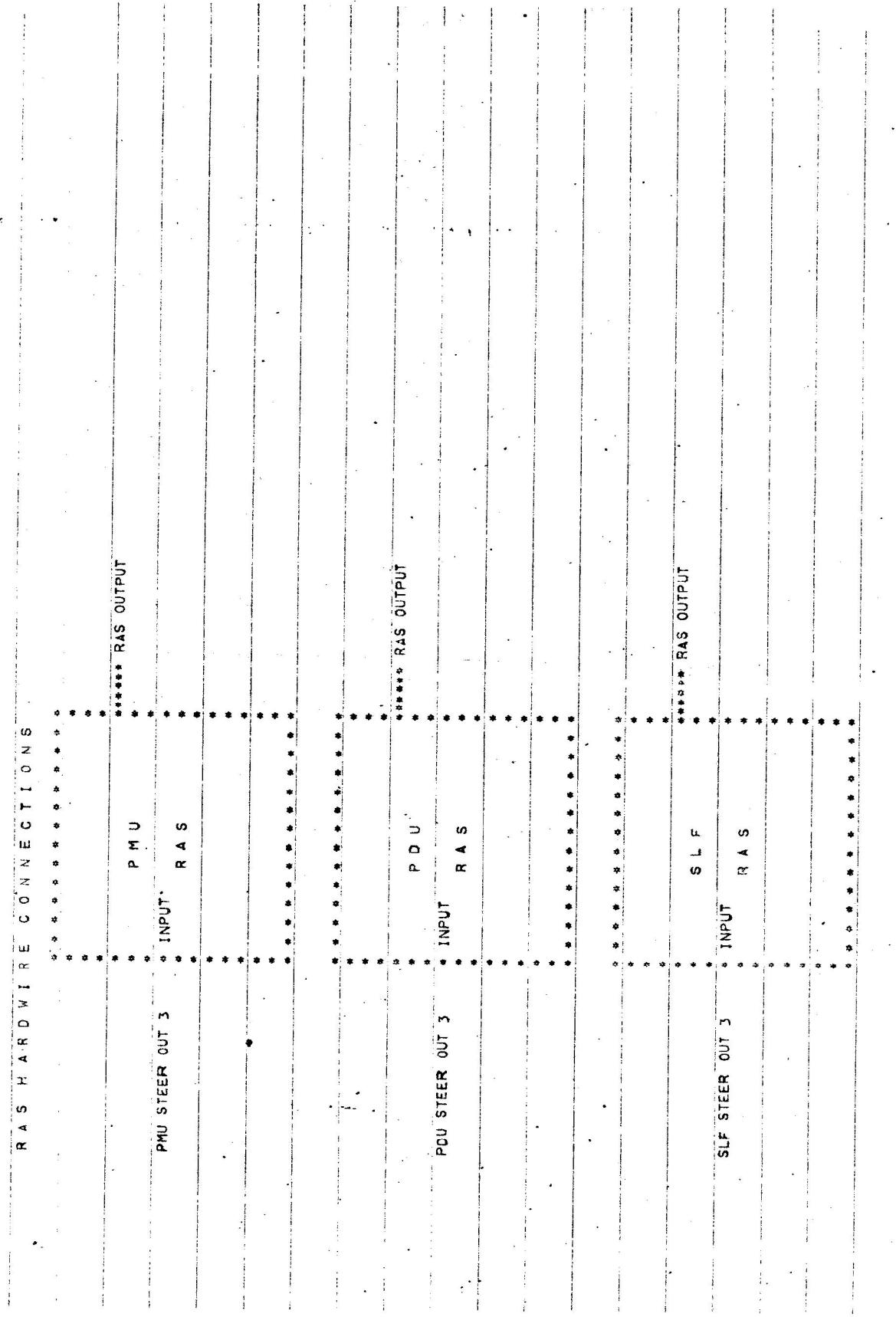


Figure 3-6. (Continued)



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DATA TRANSFERRED FROM FRAME TO FRAME PROBLEM NO. 5-1

THESE DATA ARE USED DURING FRAME ONE

DATE 14 NOV 70 TIME 11:01:42

RAS REGISTERS

P M U

SLF

	CODE	BINARY	DECIMAL	CODE	BINARY	DECIMAL	CODE	BINARY	DECIMAL
1000	01000000000000000000	50000000	1000	01000000000000000000	.50000000	1000	01000000000000000000	.50000000	1
0100	01000000000000000000	50000000	0100	01000000000000000000	.50000000	0100	0011100011000000	.236037	1
1100	00000000000000000000	00000000	1100	01000000000000000000	.50000000	1100	001011000110100000	.173492	3
0101	01000000000000000000	50000000	0010	01000000000000000000	.50000000	0010	01000000000000000000	.50000000	0
1010	01000000000000000000	50000000	1010	01000000000000000000	.50000000	1010	01000000000000000000	.50000000	0
0110	01000000000000000000	50000000	0110	01000000000000000000	.50000000	0110	011000110010010011	.399999	2
1110	01000000000000000000	50000000	1110	01000000000000000000	.50000000	1110	0101110100100101000	.727127	8
0001	000100111010010100	.1535231	0001	01000000000000000000	.50000000	0001	01000000000000000000	.50000000	0
1001	01010000000000000000	.50000000	1001	11000000000000000000	.50000000	1001	01000000000000000000	.50000000	0
0101	01000000000000000000	.50000000	0101	01000000000000000000	.50000000	0101	01010000000000000000	.312500	0
-1101	01000000000000000000	.50000000	-1101	01000000000000000000	.50000000	-1101	01011010010010010010	.727127	8
0011	00000000000000000000	.50000000	0011	01000000000000000000	.50000000	0011	01000000000000000000	.50000000	0
1011	01000000000000000000	.50000000	1011	01000000000000000000	.50000000	1011	01000000000000000000	.50000000	0
0111	01100000000000000000	.37457395	0111	01000000000000000000	.50000000	0111	01000000000000000000	.50000000	0
1111	01000000000000000000	.50000000	1111	01000000000000000000	.50000000	1111	11000010011100110000	.461334	3
0000	01000000000000000000	.50000000	0000	01000000000000000000	.50000000	0000	01000000000000000000	.50000000	0

INTERNAL SWITCHES

	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
DT1 = 0	0	0	0	0	0	0	0	0	0	0
DT2 = 1	0	1	0	0	0	0	0	0	0	0
DT3 = 1	0	0	1	0	0	0	0	0	0	0
DT4 = 1	0	0	0	1	0	0	0	0	0	0
DT5 = 1	0	0	0	0	1	0	0	0	0	0
WESTIFF = 0										

SLF DISCRETE INPUT SEQUENCE

00	1	0P	10	DD	6	0P	153	DO	4	OP	255	DO	18	OP	386	DO	15	OP	454
00	1	0P	39	DD	23	0P	153	DO	5	OP	274	DO	10	OP	415	DO	21	OP	456
00	1	0P	41	DD	3	0P	154	DO	6	OP	276	DO	7	OP	418	DO	25	OP	465
00	5	0P	97	DO	1	0P	155	DO	23	OP	278	DO	8	OP	420	DO	22	OP	467
00	6	0P	99	DO	2	0P	154	DO	5	OP	280	DO	23	OP	422	DO	17	OP	507
00	23	0P	101	DO	5	0P	157	DO	6	OP	282	DO	11	OP	429	DO	20	OP	511
00	5	0P	143	DO	6	0P	159	DO	23	OP	284	DO	16	OP	436				
00	6	0P	145	DO	23	0P	201	DO	12	OP	365	DO	19	OP	439				
00	23	0P	147	DO	15	0P	234	DO	13	OP	371	DO	16	OP	445				
00	5	0P	151	DO	15	0P	236	DO	14	OP	373	DO	16	OP	447				

Figure 3-7. Simulation - Inputs Used

DATA TRANSFERRED FROM FRAME TO FRAME PROBLEM NO. 5-1

THESE DATA ARE USED DURING FRAME ONE DATE 14 NOV 70 TIME 11:01:42

DATA INPUTS

PS = .15351868
PT = .10698509

ADC INPUTS

PS TEMP RATIO	= .5000000
PS OFFSET	= .5000000
PS SLOPE	= .5000000
PT TEMP RATIO	= .5000000
PT OFFSET	= .5000000
PT SLOPE	= .5000000
ANGLE OF ATTACK	= .7990469
QC	= .0847266
PT7-R	= .2500000
PT7-L	= .2500000
TOTAL TEMPERATURE	= .39257613
WING SWEET F/B	= .77709961
MAN. FLAP ACT.	= .14135742
MAN. FLAP HANDLE	= .04380469
MAN. FLAP THUMBWHEEL	= .99975506



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Figure 3-7. (Continued)



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Figure 3-8. Simulation = Diagnostic Output

OPERATION NUMBER 511. PASS NUMBER 1 PROBLEM NO. 5-1, NAME W. B. HOLT DATE 14 NOV 70 TIME 11:01:42

PMU	CW	1000	1	0000	0000	0001	0	00						
PDU	CW	0110	1	0000	0000	0100	0	00						
PREV PROD	010000111101101101110	+52671323	PREV QUOT	01111111111111111111	.999999809	SLF	CW	1101	0	0000	0000	0001	0	00
SENS MEM	00000000000000000000000000000000	.00000000	ROM	- 28	00000000000000000000000000000000	.000000000	LIN	E-1	0101111010001010101000	.17212776				
ROM - 24	00000000000000000000000000000000	.00000000	SUT-1	OUT-1	0101101111100010100	.73392487	DISCRETE-B	1	010110100010101000	.72742706				
SUT-2	0101110111100010100	.73392487	OUT-2	0101101111100010100	.73392487	OUT-1	0101101111100010100	.73392487	DISCRETE-C	0				
SUT-3	0101110111100010100	.73392487	OUT-3	0101101111100010100	.72712708	OUT-2	0101101111100010100	.73392487						
FR R.A.S.	00000000000000000000000000000000	.50000000	FR R.A.S.	0101101111100010100	.73392487	FR R.A.S.	0101101111100010100	.73392487	DISCRETE-B	0				
M	0101110111100010100	.73392487	D	0101101111100010100	.73392487	U	0101101111100010100	.72615820						
R	0101110111100010100	.73392487	Z	0101101111100010100	.73392487	P	0101101111100010100	.73392487						
L 0101101111100010100														.73392487
DISCRETE-D 0														
M EXT 1 0101110111100010100														.73392487
2	01000000000000000000000000000000	.50000000	D EXT 1 0101110111100010100	.73392487	SL EXT 1 010110111100010100	.73392487								
3	0101101111100010100	.72712708	2	0101101111100010100	.72712708	3	010110100010101000	.72712708						
4	0101110111100010100	.73392487	3	010110100010101000	.73392487	4	01011011111000101000	.73392487						
5	0101110111100010100	.72712708	5	01011011111000101000	.72712708	5	01011011111000101000	.73392487						
6	0101110111100010100	.72712708	6	01011011111000101000	.72712708	6	010110100010101000	.72712708						
7	0101110111100010100	.72615820	7	01011011111000100001	.72615820	7	01000000000000000000	.50000000						
8	00000000000000000000000000000000	.00000000	8	00000000000000000000000000000000	.00000000	8	11111110001010101	*.0072 2657						
9	00000000000000000000000000000000	.05600000	9	00000000000000000000000000000000	.00000000	9	00000000000000000000000000000000	*.0001 0010						
10	0101110111100010100	.73392487	10	0101110111100010100	.73392487	10	10000000000000000000000000000000	*.0001 0010						
11	0101110111100010100	.10698209	11	01000000000000000000000000000000	.00000000	11	01000000000000000000000000000000	*.0001 0010						
12	0101110111100010100	.5231323	12	0101110111100010100	.99999999	12	0101110111100010100	.00000000						
13	0101110111100010100	.72712708	13	00000000000000000000000000000000	.00000000	13	00000000000000000000000000000000	.00000000						
EXE ROM 00000000000000000000000000000000														
+ + + + + NAME W. B. HOLT														
PROBLEM NO. 5-1, PASS NUMBER 1														
PMU	CW	0001	1	0000	0000	0111	0	00						
PDU	CW	0110	0	0000	0000	0000	0	00						
PREV PROD	01000110011110010101	.53564479	PREV QUOT	01111111111111111111	.999999809	LINE-1	010111010031010101000	.727 2756						
SENS MEM	00000000000000000000000000000000	.00000000	ROM	- 28	00000000000000000000000000000000	.00000000	LINE-2	010111010031010101000	.727 2756					
ROM - 24	00000000000000000000000000000000	.00000000	SUT-1	OUT-1	00000000000000000000000000000000	.00000000	DISCRETE-B	1	0101110100310101000	.727 2756				
SUT-2	00011001110100000000000000000000	.15351868	OUT-2	0101110100310101000	.15351868	OUT-1	00010011101000001010101	.15311056						
SUT-3	00010011101000000000000000000000	.15351868	OUT-3	00010011101000001010100	.15351868	OUT-2	00010011101000001010100	.15311056						
FR R.A.S.	01011101111000010100	.73232269	FR R.A.S.	01011101111000010100	.72712708	FR R.A.S.	01011101111000010100	.727 2756						
M	0C-10011101111000010100	.15351868	D	00010000000000000000000000000000	.00000000	U	015351868	.15311056						
R	00010000000000000000000000000000	.15351868	Z	00010000000000000000000000000000	.15351868	P	0101101000101000101000	.15311056						
L 0101101000101000101000														.15311056
DISCRETE-D 0														
M EXT 1 000100111101001101000														.15351868
2	01000000000000000000000000000000	.2	01000000000000000000000000000000	.2	0101101000101000101000	.15311056								
3	00010000000000000000000000000000	.3	00010000000000000000000000000000	.3	00010000000000000000000000000000	.15311056								
4	01010000000000000000000000000000	.4	01010000000000000000000000000000	.4	0101101000101000101000	.15311056								
5	01011101110100000000000000000000	.5	01011101110100000000000000000000	.5	0101101000101000101000	.15311056								
6	01011101110100000000000000000000	.6	01011101110100000000000000000000	.6	0101101000101000101000	.727 2756								
7	01011101110100000000000000000000	.7	01011101110100000000000000000000	.7	0101101000101000101000	.727 2756								
8	00000000000000000000000000000000	.8	00000000000000000000000000000000	.8	00000000000000000000000000000000	.15311056								
9	00000000000000000000000000000000	.9	00000000000000000000000000000000	.9	00000000000000000000000000000000	.15311056								
10	01011101110100000000000000000000	.10	01011101110100000000000000000000	.10	01011101110100000000000000000000	.15311056								
11	00010000000000000000000000000000	.11	00010000000000000000000000000000	.11	00010000000000000000000000000000	.0000 0000								
12	01000000000000000000000000000000	.12	01000000000000000000000000000000	.12	01000000000000000000000000000000	.0000 0000								
13	01011101110100000000000000000000	.13	01011101110100000000000000000000	.13	01011101110100000000000000000000	.0000 0000								
EVE ROM 10000000000000000000000000000000														



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Figure 3-8. (Continued)

PROPAGATION DELAY TIME SUMMARY
*** NO EXCEEDANCES ***



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Figure 3-9. Simulation - Propagation Delay Summary



AIRESRACH MANUFACTURING COMPANY
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OUTPUT DATA SUMMARY FRAME ONE

PROBLEM NO. 5-1 DATE 14 NOV 70 TIME 11:01:42

THE FOLLOWING IS A CHECK OF INTERMEDIATE AND/OR FINAL OUTPUT DATA VALUES OR LOGICAL STATES

CHECK SEQUENCE	EXEC OUTPUT BIT NUMBER	OUTPUT FUNCTION	OUTPUT NAME	OPERATION NUMBER			MINIMUM	MAXIMUM	CALCULATED	NOMINAL
				OUTPUT	INPUT	VALUE				
1	3	DAT - PWR ON	SLF COMPARATOR	6	-	-	-	-	-	0
2	12	SELF TEST - ONE TEST	SLF COMPARATOR	39	-	-	-	-	-	1
3	12	SELF TEST - ZERO TEST	SLF COMPARATOR	43	-	-	-	-	-	0
4	8	5 TRUE ANGLE OF ATTACK	RAS (PDU)	102	-48500000	-48906708	-49088542	-48828125	-	
5	0	1.D. CODE PT/95	ROM (PDU)	102	-62500000	-62500000	-62500000	-62500000	-	
6	70	P6/36	RAS (PDU)	158	-10719280	-10721397	-10737720	-10720000	-	
7	70	4 ALTITUDE/128K	RAS (PDU)	165	-15367917	-15368391	-15391643	-15343300	-	
8	9	1 PRESSURE ALTITUDE	RAS (PDU)	181	-3128750	-31250381	-31288250	-31250000	-	
9	6	1.J. CODE	ROM (PDU)	185	-48706054	-46628697	-46951945	-4828125	-	
10	70	16 DELTA PRESSURE ALTITUDE	RAS (PDU)	186	-12200000	-12200000	-12500000	-12200000	-	
11	12	11 PRESSURE ALTITUDE	RAS (PDU)	195	-60000000	-60000000	-60000000	-60000000	-	
12	12	1.D. CODE	ROM (PDU)	195	-62200000	-62200000	-62500000	-62500000	-	
13	0	37 TOTAL TEMPERATURE SWITCH	SLF COMPARATOR	203	-	0	-	-	-	0
14	7	1.2 PRESSURE ALTITUDE	RAS (PDU)	205	-68910155	-68749428	-6858844	-68750000	-	
15	8	1.D. CODE	ROM (PDU)	205	-50000000	-50000000	-50000000	-50000000	-	
16	70	6 FREE AIRSTREAM TEMP. (TS)	RAS (PDU)	213	-45142500	-44030762	-42986750	-44140625	-	
17	8	15 INDICATED AIR SPEED	ROM (PDU)	213	-75000000	-75000000	-75000000	-75000000	-	
18	0	1.J. CODE	ROM (PDU)	222	-33721555	-33722135	-3401444	-33721555	-	
19	8	15 INDICATED AIR SPEED	ROM (PDU)	222	-12200000	-12200000	-12500000	-12200000	-	
20	5	7 35 MACH SWITCH	SLF COMPARATOR	223	-	1	-	-	-	1
21	7	31 MACH SWITCH	SLF COMPARATOR	224	-	0	-	-	-	0
22	7	7 62 MACH SWITCH	SLF COMPARATOR	225	-	0	-	-	-	0
23	7	51 MACH NUMBER	SLF COMPARATOR	226	-	0	-	-	-	0
24	7	4 MACH NUMBER	RAS (PDU)	230	-23632812	-23787498	-23974365	-23803711	-	
25	6	1.D. CODE	ROM (PDU)	230	-50000000	-50000000	-50000000	-50000000	-	
26	7	1.8 PRESSURE ALTITUDE RATE	RAS (PDU)	243	-00179000	-00000000	-00179000	-00000000	-	
27	7	2 PRESSURE ALTITUDE RATE	RAS (PDU)	245	-00369451	-00000000	-00169451	-00000000	-	
28	8	2 AUTHORITY SCHEDULE YAW	ROM (PDU)	245	-25000000	-25000000	-25000000	-25000000	-	
29	7	22 AUTHORITY SCHEDULE YAW	RAS (PDU)	252	-51564900	-5152100	-51515369	-51515369	-	
30	7	MACH4.026	RAS (PDU)	252	-23779897	-23787498	-23803700	-23803700	-	
31	0	8 13 TRUE AIRSPEED	RAS (PDU)	256	-15402055	-15520960	-15661360	-15534194	-	
32	0	1.D. CODE	ROM (PDU)	258	-37500000	-37500000	-37500000	-37500000	-	
33	0	7 22X PASSENGER ALT. SYNCRO	RAS (PDU)	261	-63981074	-63981074	-63981074	-63981074	-	
34	7	30X PRESSURE ALT. SYNCRO	RAS (PDU)	261	-8662166	-8662166	-8662166	-8662166	-	
35	7	29Y PRESSURE ALT. SYNCRO	RAS (PDU)	263	-83981620	-83981620	-83981620	-83981620	-	
36	7	30Y PRESSURE ALT. SYNCRO	RAS (PDU)	263	-86593156	-86593156	-86593156	-86593156	-	
37	8	9 PRESSURE ALT. SYNCRO	RAS (PDU)	267	-83981620	-83981620	-83981620	-83981620	-	
38	8	9 PRESSURE ALT. SYNCRO	RAS (PDU)	267	-003930625	-00000000	-003930625	-00000000	-	
39	0	1.D. CODE	ROM (PDU)	267	-87500000	-87500000	-87500000	-87500000	-	
40	7	17 DELTA MACH NUMBER	RAS (PDU)	268	-02000000	-02000000	-02000000	-02000000	-	
41	8	3 TRUE AIRSPEED	RAS (PDU)	276	-22887573	-23036003	-22887573	-23060107	-	

Figure 3-10. Simulation - Output Data Summary

CHECK	EXEC OUTPUT SEQUENCE	BIT NUMBER	OUTPUT FUNCTION	OUTPUT NAME	OPERATION NUMBER	MINIMUM	OUTPUT VALUE	MAXIMUM	NOMINAL
42	5.0	36A	1.D. CODE	RDM (PDU)	276	-37500000	37500000	37500000	37500000
43	7	38B	ENGINE PRESSURE RATIO	RAS (PDU)	279	.969799	.9999609	.9999809	.9999809
44	7	38B	ENGINE PRESSURE RATIO	RAS (PDU)	287	.969799	.99974251	.99974251	.9999809
45	7	34	MACH NUMBER	RAS (PDU)	296	.34465000	.34803200	.35179000	.34822000
46	8	14	MACH NUMBER	RAS (PDU)	298	.18632381	.1945079	.18866863	.18866863
47	70	1.0	CODE	RDM (PDU)	296	-25000000	-25000000	-25000000	-25000000
48	7	28	PRESSURE ALTITUDE (IFF)	RAS (PDU)	299	.96289063	.96337891	.9686527	.96289063
49	7	23	MACH SCHEDULE	RAS (PDU)	300	.32642603	.34788513	.37000000	.38421400
50	7	20	AUTHORITY SCHEDULE DOWN	RAS (PDU)	312	.00000000	.00000000	.04167200	.00000000
51	7	36	MAX. SAFE MACH SWITCH	SLF COMPARATOR	332	-	0	0	0
52	7	35X	MAX. SAFE MACH SYNCRO	RAS (PDU)	351	.76085759	.76702680	.77206691	.76649143
53	7	35Y	MAX. SAFE MACH SYNCRO	RAS (PDU)	356	-.18155385	-.17226601	-.16433684	-.1729543
54	7	41X	WING SWEEP SYNCRO	RAS (PDU)	436	-.92447548	-.94410000	-.9551945	-.94331290
55	3	41X	DT2 - WS(H).LT.WS(P)	SLF COMPARATOR	444	-	0	0	0
56	7	40	WING SWEEP POSITION	RAS (PDU)	445	.76566230	.77600861	.78859050	.77712639
57	3	41	DT3 - H.F. HOLE,NOT,ZERO	SLF COMPARATOR	450	-	0	0	0
58	3	41	DT4 - G(A),G(GLTH)	SLF COMPARATOR	451	-	1	1	1
59	77	41Y	WING SWEEP SYNCRO	RAS (PDU)	451	.15207053	.18697929	.23584791	.18421611
60	7	44	MANEUVER FLAP CONTROL	RAS (PDU)	470	-.08314740	.24980932	.27470880	.17692810
61	7	47	GLOVE VANE CONTROL	RAS (PDU)	484	.004991924	.79408660	.3698230	.3698230
62	7	19	MACH SCHEDULE	RAS (PDU)	492	.25541600	.27663375	.2970800	.27655200
63	70	SELF TEST REG	PMU	RAS (PDU)	499	-.37475395	-.37475395	-.37475395	-.37475395
64	7C	SELF TEST REG = PDU STEER OUT 3		RAS (PDU)	509	.67410660	.67410660	.67410660	.67410660

64. OUTPUT VALUES WERE CHECKED
C. OUTPUT VALUES EXCEEDED THEIR SPECIFIED ERROR BOUNDS

**EXCEEDANCES



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Figure 3-10. (Continued)

ROM DATA FORMATTED AND PINCH ON CARDS TO AMI'S SPECIFICATIONS ON DATE = 01 DEC 70 TIME = 16107148

AIRESEARCH PART NO. 944125-23	ANI NO. C8401
(0101010111 1101101010)	(011101010111) (00011010110 1111001010) C8401-1
(0101010111 0101010100)	(0111011111 0111001010) (01110010100) C8401-2
(1101000000 0000000000)	(000101010100 0000000000) (0111111111 1111111111) C8401-3
(00000011001 0000001101)	(0000001111 10000010101) (1111010101 0110100111) C8401-4
(00000011001 0100001010)	(1111111100 0001100010) (0000010010 1110011001) C8401-5
(1101111110 0110110100)	(0001001011 1110001000) (0000010010 1001011000) C8401-6
(00000011000 0000001100)	(1101010101 0101010101) (0000001100 0003000000) C8401-7
(0110101010 0001010101)	(0000010010 1001011000) (0000000000 0000000000) C8401-8
(1101011101 0101010101)	(0000000000 0000000000) (0110101010 0001010101) C8401-9
(11000011001 1000110101)	(0000110100 0100101010) (1010111100 0100100011) C8401-10
(00000010010 0111110101)	(00000101010 0101110101) (0000110101 0001101010) C8401-11
(11110001001 1101010100)	(0000001010 0100101010) (0010010000 1110041111) C8401-12
(0101001000 0101111111)	(0101010000 0101111111) (0010010001 0101110101) C8401-13
(0000000000 0000000000)	(0110111110 0001011101) (0000000000 0000000000) C8401-14
(0000000000 0000000000)	(0000000000 0000000000) (0000000000 0000000000) C8401-15
(0111000000 0000000000)	(1101010100 0100101111) (1111111111 0111111111) C8401-16
(0111000000 0110110000)	(1101010100 0100101111) (1101100110 1101111001) C8401-17
(0101010100 1010110000)	(0101010100 0100101111) (0000001010 0111101001) C8401-18
(0101011100 1111110000)	(1110100101 0111101111) (0010110111 0111101111) (0010110110 1011100001) C8401-19
(0101010100 1011100000)	(0000000000 10000011011) (1111111110 1111111010) C8401-20
(1111111111 0101110112)	(1111111110 1100001040) (1111111110 0100010101) C8401-21
(0100101001 1100011111)	(0000000000 1000110000) (1111111111 1111111111) C8401-22
(0000000000 1100011011)	(0000000001 1000101011) (0000000001 0101101111) C8401-23
(0000000000 0101010101)	(0000000000 1000110112) (0000000000 0001000000) C8401-24
(00210001100 1001011010)	(0000000000 0000000000) (0000000000 0000000000) C8401-25
(01010001010 0000000000)	(0110101010 0000000000) (0000000000 0000000000) C8401-26
(01010001010 0000000000)	(0000000000 0000000000) (0110101010 0000000000) C8401-27
(0000000000 0000000000)	(0000000000 0000000000) (0000000000 0000000000) C8401-28
(0000000000 0000000000)	(0000000000 0000000000) (0000000000 0000000000) C8401-29
(0110101010 0000000000)	(1101010101 0101010101) (0000000000 0000000000) C8401-30
(0110101010 0000000000)	(0000000000 0000000000) (0000000000 0000000000) C8401-31
(0110101010 0000000000)	(0110101010 0000000000) (0001010101 0001010101) C8401-32
(0000000000 0000000000)	(0000000000 0000000000) (0000000000 0000000000) C8401-33
(0000000000 0000000000)	(0000000000 0000000000) (0000000000 0000000000) C8401-34
(0110101010 0000000000)	(0000000000 0000000000) (0000000001 1011000000) C8401-35
(0000000000 0000000000)	(0000000000 0000000000) (0111110111 0101101101) (0101101111 0101101101) C8401-36
(0000000000 0000000000)	(0000000000 0000000000) (0000000000 0000000000) (0000000000 0000000000) C8401-37
(0000000000 0000000000)	(0111111111 1111111111) (1111111111 1111111111) (1111111111 1111111111) C8401-38
(0000000000 0000000000)	(0000000000 0000000000) (0000000000 0000000000) (0000000000 0000000000) C8401-39
(1111010011 0011110111)	(0000000000 0000000000) (0000000000 0000000000) (0000000000 0000000000) C8401-40
(0000000000 0000000000)	(0000000000 0000000000) (0000000000 0000000000) (0000000000 0000000000) C8401-41
(0000000000 0000000000)	(0000000000 0000000000) (0000000000 0000000000) (0000000000 0000000000) C8401-42
(0000000000 0000000000)	(0000000000 0000000000) (0000000000 0000000000) (0000000000 0000000000) C8401-43

Figure 3-11. Simulation - Listing of ROM with AMI Format



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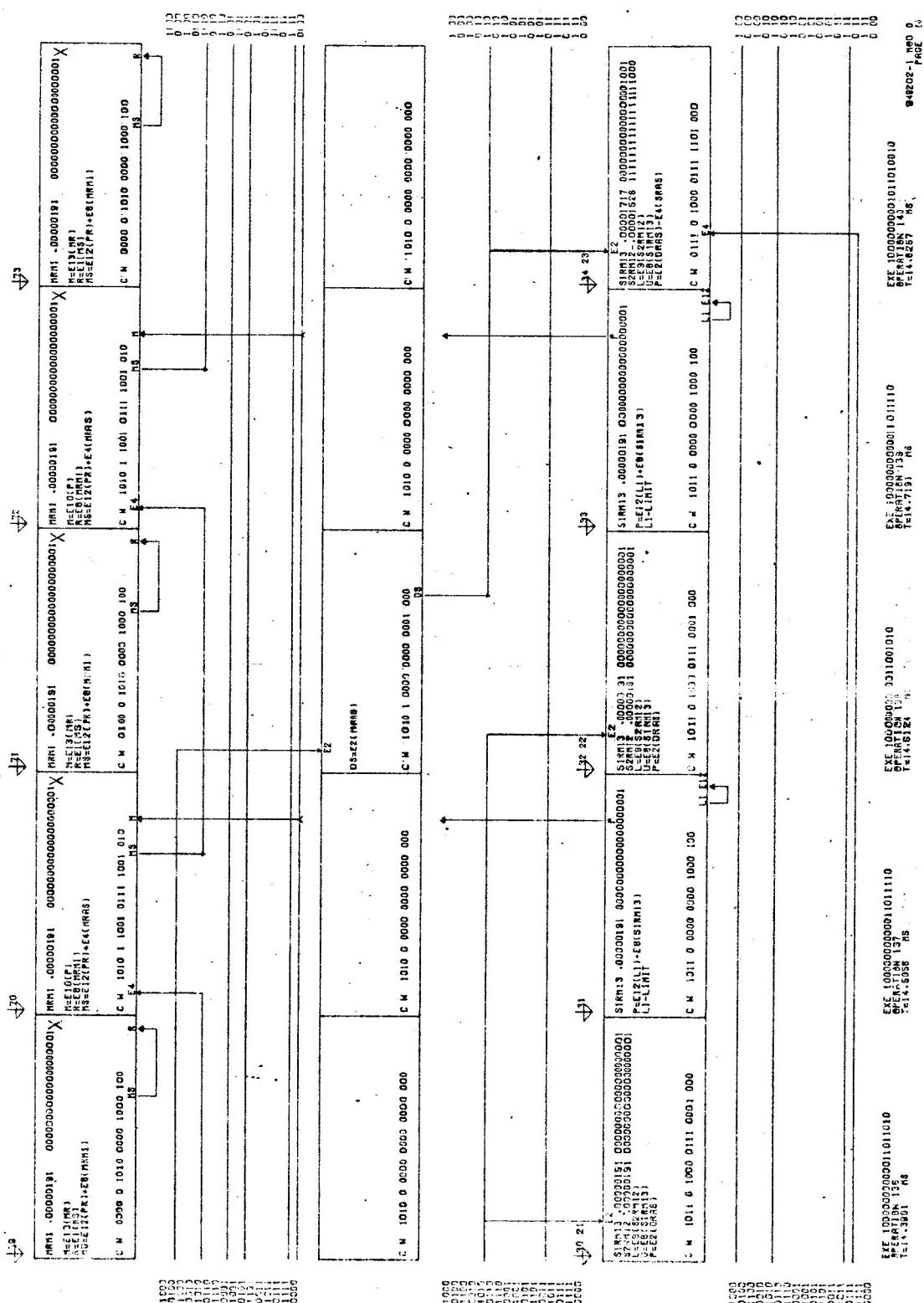


Figure 3-12. Computer Program Drawing - CAL Comp Plotter



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APPENDIX A
BOOTH'S ALGORITHM*

Booth's algorithm is a method developed for binary multiplication for numbers in signed 2's complement representation. This method requires no sensing of the sign digit of the multiplicand or multiplier. The algorithm works as follows:

- (a) Start from the LSB of the multiplier and look at the bits in groups of two. An initial reference bit of a 0 should be added to the LSB end of the word.
- (b) For certain conditions of the multiplier bits, various operations are performed with the multiplicand and partial product. These conditions are as follows:

<u>Multiplicator</u> <u>Bits</u>		<u>Operation</u>
$y_i \quad y_{i+1}$		
0 1		Add multiplicand X to partial product, then shift partial product right 1 bit.
1 0		Subtract multiplicand X from partial product, then shift partial product right 1 bit.
0 0		Shift partial product right 1 bit.
1 1		Shift partial product right 1 bit.

No shift operation is required after the last operation. Since the multiplicand is a signed number, the shifting algorithm should be observed. This is such that if shifting is to the left, all added digits are 0's and if shifting is to the right, all added digits are equivalent to the sign digit. The sign digits remains unchanged.

*CHU, YOAHAN, "Digital Computer Design Fundamentals," 1962, McGraw Hill, Inc., page 32.



Example:

X = Multiplicand = 1.0011

Y = Multiplier = 0.1010

1.0011 = X

0.1010(0) = Y

0.0000 0 Initial condition in partial product register

Y_i	Y_{i+1}	Operation		
0	0	Shift Right	0.00000	1st Partial Product
1	0	Subtract X	<u>1.0011</u> 0.11010	2nd Partial Product
		Shift Right	0.01101	
1	0	Add X	<u>1.0011</u> 1.10011	3rd Partial Product
		Shift Right	1.11001	
1	0	Subtract A	<u>1.0011</u> 0.10011	4th Partial Product
		Shift Right	0.01001	
0	1	Add X	<u>1.0011</u> 1.01111	
			<u>1</u>	Round off bit added
			1.1000	= XY

Other examples are offered in CHU, page 34.



AIRESEARCH MANUFACTURING COMPANY
Los Angeles, California

APPENDIX B

NONRESTORING DIVISION*

Nonrestoring division makes use of the sign of the divisor and that of the partial remainder. If the two signs agree, a subtraction is performed and the quotient digit is 1. The subtraction is replaced by the addition of the 2's complement of the divisor. If the signs do not agree, an addition is performed and the quotient digit is 0. In either case, a new partial remainder is next formed by a proper (left) shift, and the process continues until the remainder is zero or the desired number of quotient digits is obtained. The true result (quotient) requires an addition of $-2 + 2^{-n}$ to the indicated quotient.

Example:

$$X = \text{Dividend} = 0.1000$$

$$Y = \text{Divisor} = 0.1010$$

0.1000	=	X	
<u>0.1010</u>	=	Y	q ₁ = 1
1.0000	=	2r ₀	Shift Left
<u>1.0110</u>	=	-Y	Sub Divisor
0.0110	=	r ₁	q ₂ = 1
0.1100	=	2r ₁	Shift Left
<u>1.0110</u>	=	-Y	Sub Divisor
0.0010	=	r ₂	q ₃ = 1
0.0100	=	2r ₂	Shift Left
<u>1.0110</u>	=	-Y	Sub Divisor
1.1010	=	r ₃	q ₄ = 0
1.0100	=	2r ₃	Shift Left
<u>0.1010</u>	=	+Y	Add Divisor
1.1110	=	r ₄	q ₅ = 0
1.1100	=		Pseudo Quotient Digits
<u>+1.0001</u>	=		Correction
0.1101	=		Quotient

Other examples are given in CHU, page 42.

*CHU, YOAHAN, "Digital Computer Design Fundamentals," 1962, McGraw Hill, Inc., page 39.

