

944 112  
PDU

## 4.0 LOGICAL SPECIFICATION

### 4.1 DEFINITION OF SYSTEM TERMS

BIT TIME: ONE COMPLETE CLOCK PERIOD, 2.66  $\mu$ SEC AT 375 KHZ.

SEE FIGURE 2.

WORD TIME: 20 CONSECUTIVE BIT TIMES ( $t_0$  THROUGH  $t_{19}$ ). THERE ARE TWO TYPES OF "WORDS".

IN  $W_A$ , THE PARALLEL ARITHMETICAL ALGORITHMS OPERATE, AND CONTROL WORDS ARE SHIFTED INTO THE UNITS (SERIALLY).

IN  $W_0$ , COMPUTATIONAL INPUTS AND OUTPUTS ARE SHIFTED SERIALLY AMONG THE UNITS.

THESE WORDS ALTERNATE AND ARE OF EQUAL DURATION; i.e., THEY ARE COMPLEMENTARY.

WORD MARK: A SIGNAL COINCIDENT WITH  $t_{18}$  OF EVERY WORD TIME.

OPERATION ("Op") TIME: TWO CONSECUTIVE WORD TIMES ( $W_A$  AND  $W_0$ ).

FRAME MARK: FINAL BIT TIME OF THE FINAL Op.

WORD LENGTH IS 20 BITS. FOR DATA WORDS THIS IS NORMALLY SIGN AND 19 BITS.

DATA IS SHIFTED LSB FIRST. TWO'S COMPLEMENT REPRESENTATION IS USED FOR NEGATIVE NUMBERS. DURING BIT TIME  $t_0$ , INFORMATION IN THE COMPUTER REGISTERS IS "PROPERLY" ORIENTED; i.e., ALL THE BITS OF A DATA WORD ARE CONTAINED IN PROPERLY CORRESPONDING REGISTER POSITIONS. MEANINGFUL DATA TRANSFERS INTO AND OUT OF THE LOGIC CHIPS AND REGISTERS OCCUR DURING  $W_0$  OF EVERY Op.

### 4.2 GENERAL DESCRIPTION

PDU SHALL ACCEPT TWO SERIAL INPUTS IN  $W_0$  AS DIVIDEND AND DIVISOR

AND SHALL PRODUCE THE PROPER QUOTIENT BY MEANS OF A PARALLEL ALGORITHM IN  $W_A$ , AND SHIFT THE RESULT OUT IN THE NEXT  $W_0$  WHILE INPUTS FOR THE NEXT OPERATION ARE SIMULTANEOUSLY SHIFTED IN.

THIS OPERATION SHOULD BE ACHIEVED BY A NONRESTORING DIVISION ALGORITHM. THE UNIT SHALL BE CAPABLE OF OPERATING CONTINUALLY IN THIS MANNER.



AIRESEARCH MANUFACTURING COMPANY  
A DIVISION OF THE GARRETT CORPORATION  
LOS ANGELES, CALIFORNIA

SIZE	CODE NO.	DWG NO.
A	70210	944112
SCALE	REV	SHEET
		9

## 4.6 ELECTRICAL CHARACTERISTICS

THE ELECTRICAL CHARACTERISTICS SHALL APPLY AT ROOM AMBIENT TEMPERATURE.

### 4.6.1 POWER SUPPLIES: THE INPUT POWER SUPPLY CHARACTERISTICS ARE DEFINED BELOW:

$$V_{SS} = 0 \text{ V}$$

0.0 VDC (GROUND POTENTIAL ABOUT WHICH  $V_{SS}$  AND  $V_{DD}$  ARE REFERENCED)

$$V_{DD} = +14.0 \pm 1.0 \text{ V}$$

$$V_{\phi} = -28.5 \pm 1.5 \text{ VDC}$$

### 4.6.2 POWER DISSIPATION:

4.6.2.1 CALCULATED POWER: THE DC POWER DISSIPATION SHALL AT  $-55^{\circ}\text{C}$  AND  $+125^{\circ}\text{C}$  BE CALCULATED FOR THE DEVICE COVERED BY THIS SPECIFICATION. THE CALCULATED VALUE SHALL BE SUBMITTED TO AIRESEARCH WITHIN 45 DAYS AFTER AWARD OF CONTRACT.

4.6.2.2 MEASURED POWER: THE DC POWER DISSIPATION AT  $-55^{\circ}\text{C}$  AND  $+125^{\circ}\text{C}$  OF THIS DEVICE SHALL NOT EXCEED THE CALCULATED VALUE BY MORE THAN 15 PERCENT.

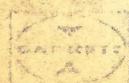
4.6.3 CLOCK CHARACTERISTICS: THE CLOCK CHARACTERISTICS ARE DEFINED IN FIGURE 2 OF THIS SPECIFICATION.

4.6.4 LOGIC LEVELS: THE MOS INPUT AND OUTPUT LOGIC LEVELS ARE DEFINED IN THE MATRIX BELOW:

	(MIN)	(MAX)
INPUT LOGIC "0"	-3.0 V	0.0 V
INPUT LOGIC "1"	$V_{DD}$	-9.0 V
OUTPUT LOGIC "0"	-2.0 V	0.0 V
OUTPUT LOGIC "1"	$V_{DD}$	-10.0 V

$W_0$ ,  $I_{18}$ , FRAME MARK AND DISCRETE INPUT LOGIC LEVELS ARE DEFINED IN THE MATRIX BELOW:

	(MIN)	(MAX)
INPUT LOGIC "0"	-0.6 V	0.0 V
INPUT LOGIC "1"	-15.4 V	-12.6 V



AIRESEARCH MANUFACTURING COMPANY  
4000 EAST 10TH STREET  
LOS ANGELES, CALIFORNIA

SIZE	CODE NO.	DRAW NO.
A	70210	E
SCALE	PCV	SHEET //
944112		

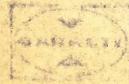
4.6.5 OUTPUT DRIVE CAPABILITY: EACH OUTPUT SHALL BE CAPABLE OF DRIVING A LOAD TO GROUND OF 75.0 KOMMS RESISTIVE IN PARALLEL WITH A 10 PF CAPACITOR PLUS A CAPACITOR EQUAL TO FOUR TIMES THE MAXIMUM INPUT CAPACITANCE ON ANY SINGLE INPUT (EXCEPT POWER, CLOCK AND TIMING INPUTS) FOR ANY OF THE FOLLOWING CIRCUITS (P/N 944125, P/N 944111, P/N 944112, P/N 944113, P/N 944114, P/N 944118). THE CALCULATED CAPACITANCE LOAD AT -55°C AND +125°C PER ABOVE SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.6.6 INPUT LOADING

4.6.6.1 TIMING AND LOGIC INPUTS: THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL TIMING AND LOGIC INPUTS (EXCEPTCLOCKS  $\phi_1$  AND  $\phi_2$ ) SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.6.6.2 THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL CLOCK INPUTS ( $\phi_1$  AND  $\phi_2$ ) SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.6.6.3 DATA INPUTS: THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL DATA INPUTS SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.



AIRESEARCH MANUFACTURING COMPANY  
A Division of TRW Incorporated

SIZE	CODE NO.	DWG NO.
A	70210	944112
SCALE	REV.	SHEET
		12

4.7 PIN ASSIGNMENTS

INTENTIONALLY LEFT BLANK

TO BE DETERMINED BY CIRCUIT LAYOUT  
AND TO BE APPROVED BY AIRSEARCH



MASSACHUSETTS  
MANUFACTURING COMPANY  
GENERAL PLANT AND OFFICES  
BOSTON, MASS.

SIZE	CODE NO.	LOG NO.
A	70210	E
SCALE	REV.	SHEET /3

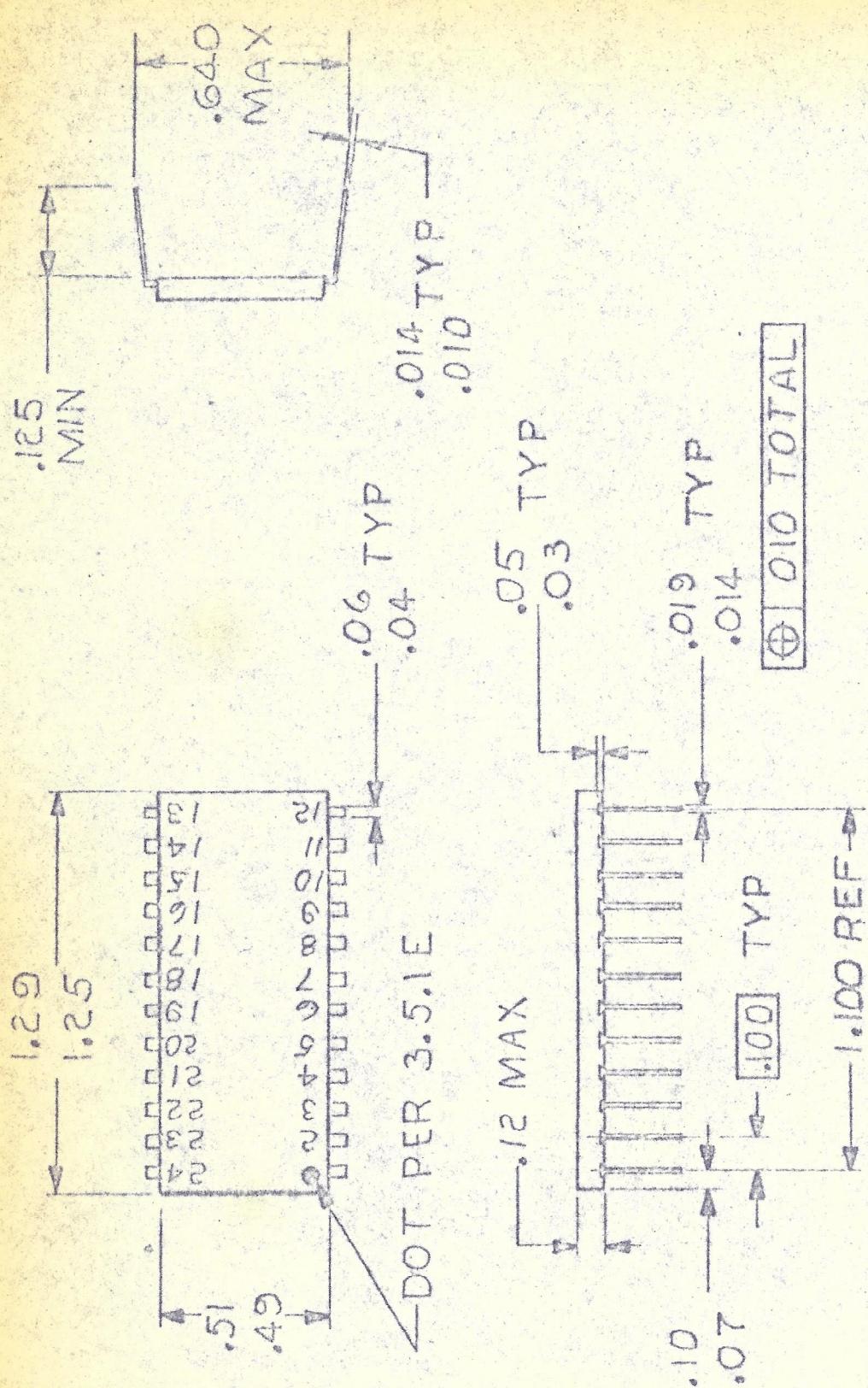
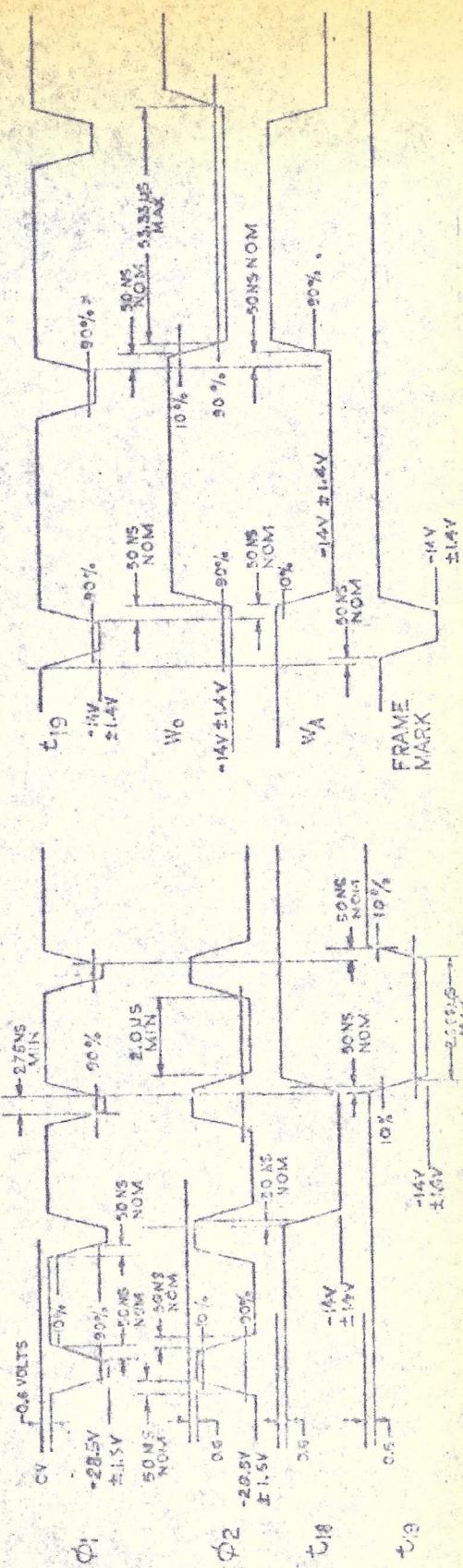
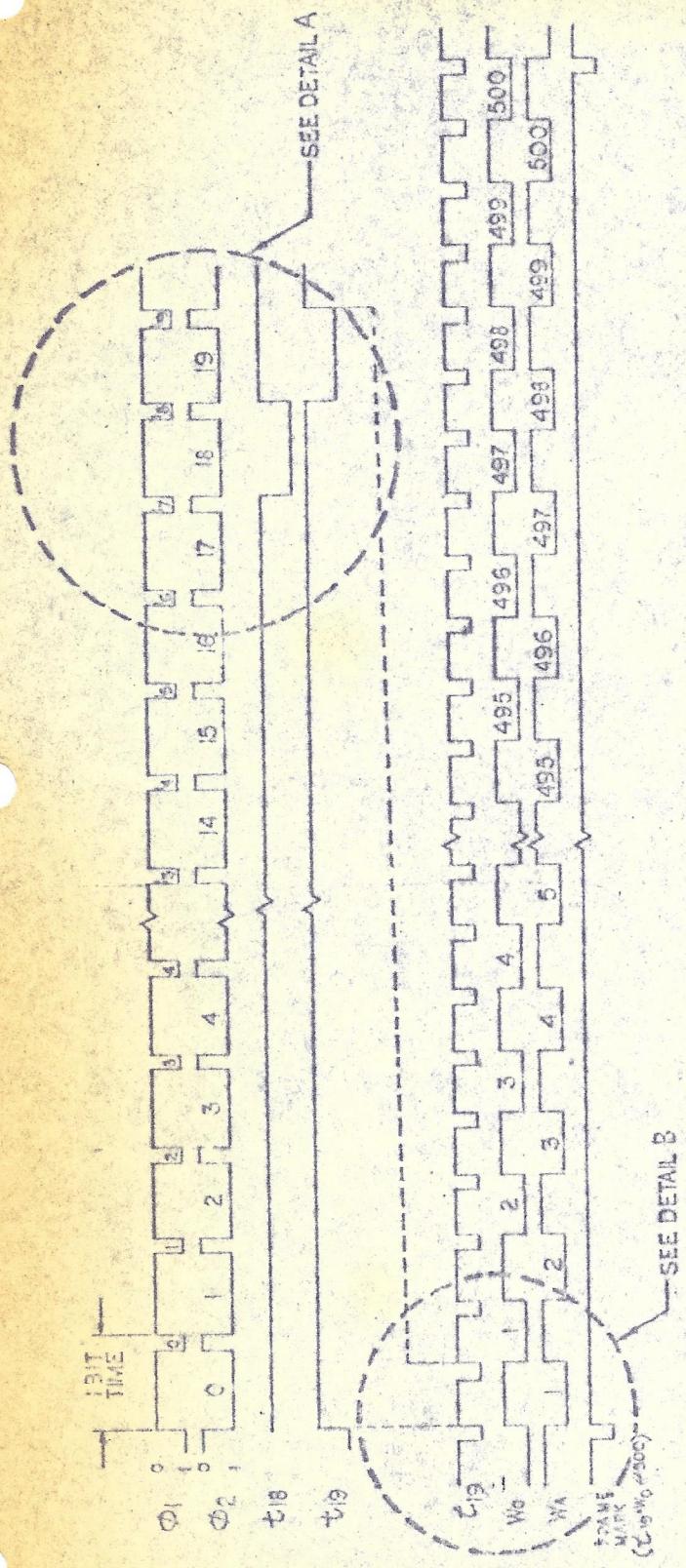


FIGURE 1 PACKAGE DRAWING



AIRESEARCH MANUFACTURING COMPANY  
A DIVISION OF THE FALKENBERG CORPORATION  
LOS ANGELES, CALIFORNIA

SIZE	CODE NO.	DWG NO.
A	70210	944112
SCALE	REV.	SHEET
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DETAIL A

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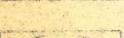
FIGURE 2a TIMING DIAGRAM

1. CLOCK VOLTAGE WILL NOT GO POSITIVE.
  2. MAX OVERLAP AND  $\frac{V_2}{V_1}$  VOLTAGE IS 3.0 VOLTS

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AIR RESEARCH MANUFACTURING COMPANY  
A DIVISION OF THE TRACOR INCORPORATION  
LOS ANGELES, CALIFORNIA

 <b>AIRESEARCH MANUFACTURING COMPANY</b> A DIVISION OF THE PHILCO CORPORATION SAN CARLOS, CALIFORNIA	SIZE	CODE NO.	DWG NO.
	<b>A</b>	<b>70210</b>	<b>944112</b>
	SCALE	REV	<b>SHEET 20</b>

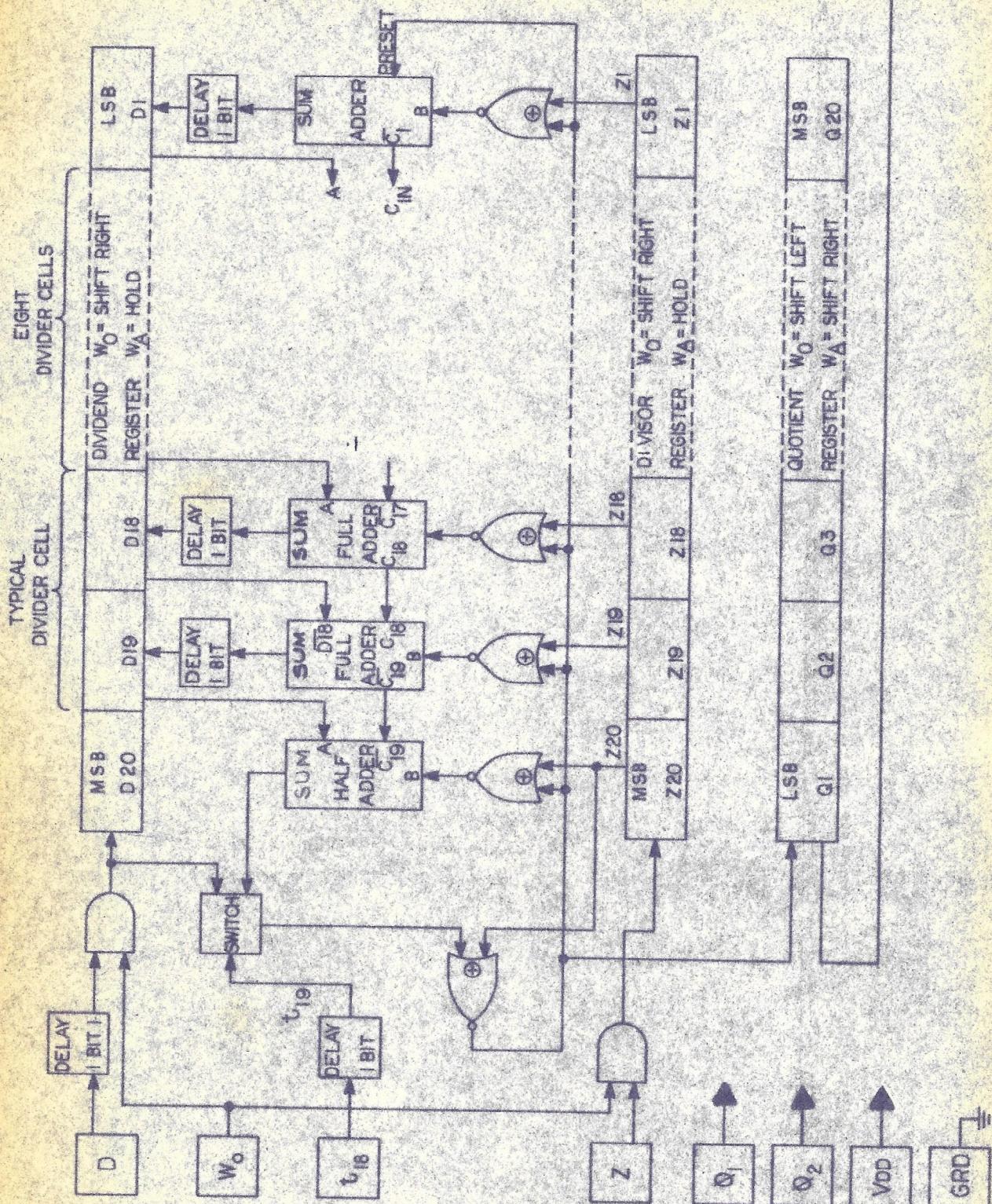


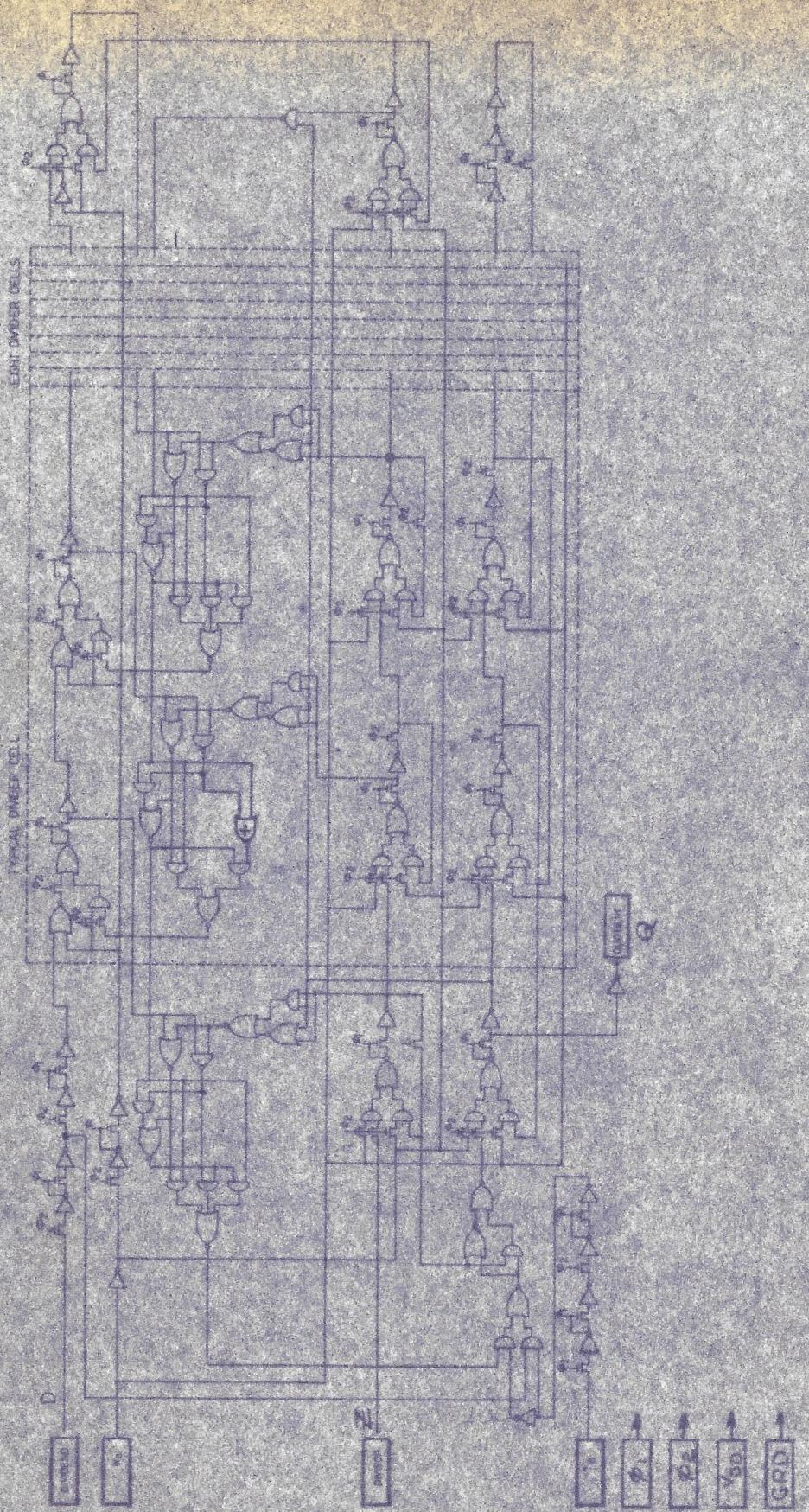
FIGURE 3 POU - BLOCK DIAGRAM



**AIRESEARCH MANUFACTURING COMPANY**  
A DIVISION OF THE GARRETT CORPORATION  
LOS ANGELES, CALIFORNIA

SIZE <b>A</b>	CODE NO. <b>70210</b>	DWG NO. <b>944112</b>
SCALE	REV	SHEET <b>22</b>

FIGURE 4 PDU - LOGIC DIAGRAM



SIZE	CODE NO.	DWG NO.	A	70210	944112
			SCALE	REV	SHEET 23



AIRSEARCH MANUFACTURING COMPANY  
A Division of Learjet Corporation  
1000 Park Lane, Fort Worth, Texas

## PARALLEL DIVIDE P/N 944112-1

PIN NAME	PIN NUMBER	INPUT CAP. MAX		INPUT RES. MIN	
		-55°C	+125°C	-55°C	+125°C
IN {	9	5 pf	5 pf	5 M <sub>Ω</sub>	5 M <sub>Ω</sub>
	17	5 pf	5 pf	5 M <sub>Ω</sub>	5 M <sub>Ω</sub>
	18	5 pf	5 pf	5 M <sub>Ω</sub>	5 M <sub>Ω</sub>
	8	13 pf	13 pf	1 M <sub>Ω</sub>	1 M <sub>Ω</sub>
	23	35 pf	35 pf	6.3 mA	3.2 mA
	21	45 pf	45 pf	0	0
	6				
GROUND	22				
OUT { Q	20				

Chip Size: 141 x 151 mils

Number Devices: 1241

Package Type: 24-pin dual in-line package

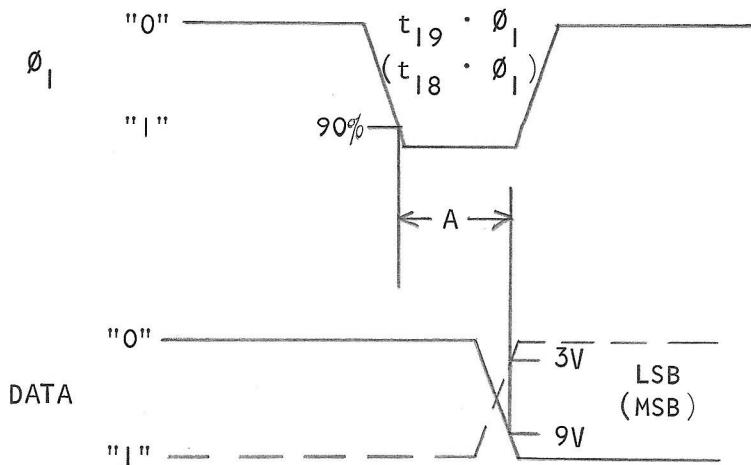
DC Power Dissipation -55°C 1.3W +125°C 475 mW

DC Power Dissipation (measured) -55°C \_\_\_\_\_ +125°C \_\_\_\_\_

Output Drive Capability Res. -55°C 75K<sub>Ω</sub> +125°C 75K<sub>Ω</sub>  
Cap. -55°C 50pf +125°C 50pfR. M. Holt  
Dept. 93-9  
July 24, 1970

PROPAGATION DELAYS -  $\emptyset_1$  OUTPUT INITIATIONS

CIRCUIT PDU 944112-1

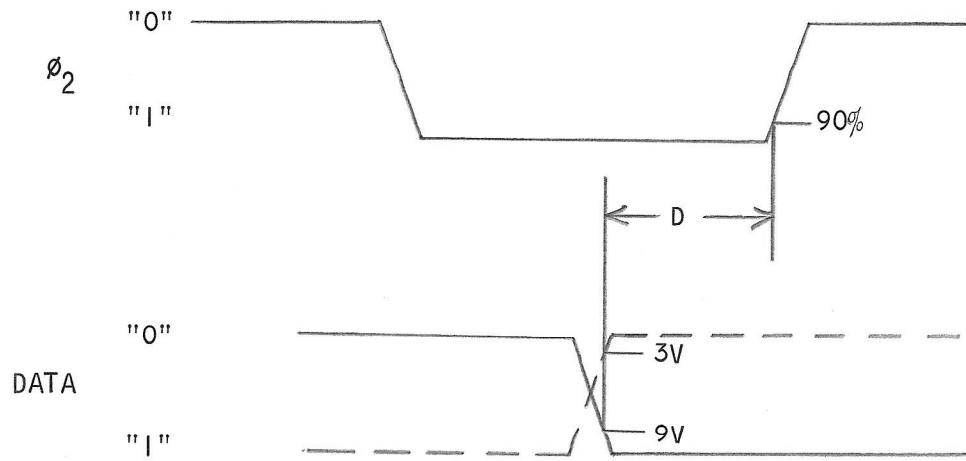


TERMINAL NAME	PACKAGE TERMINAL	PROPAGATION DELAY (A) MAX
Q	20	300 nS

R. M. Holt  
Dept. 93-9  
July 24, 1970

PROPAGATION DELAYS -  $\phi_2$  INPUT TERMINATIONS

CIRCUIT PDU 944112-1



TERMINAL NAME	PACKAGE TERMINAL	DATA SET-UP TIME (D) MIN
$w_0$	8	1000 nS 2000

R. M. Holt  
Dept. 93-9  
July 24, 1970

DIVIDER TEST SEQUENCE  
P/N 944112

PAGE 1  
PDU

DIVIDER TEST SEQUENCE

P/N 944112

## DIVIDER TEST SEQUENCE

PAGE 2  
PDU

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A vertical column of 20 empty rectangular boxes, likely a template for a survey or form.

A vertical column of 20 empty rectangular boxes, arranged one above the other. The boxes are evenly spaced and have thin black borders. This grid is positioned on the right side of the page, serving as a template for a survey or form.

Table 1. The effect of the number of columns on the performance of the proposed method.

Table 1. The effect of the number of columns on the performance of the proposed method.

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A vertical column of 20 empty rectangular boxes, likely for taking notes or drawing diagrams.

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A vertical column of 20 empty rectangular boxes, intended for handwritten notes or observations.

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## AIRESARCH MFG. CO.

DATE \_\_\_\_\_

CALC. NO. \_\_\_\_\_

PREPARED BY \_\_\_\_\_

MODEL \_\_\_\_\_

CHECKED BY \_\_\_\_\_

PART NO. \_\_\_\_\_

#1

PDU

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D 01000001001010101110  
 Z 11001101010100100011  
 $Q_1$  100101111111100001

#2

M

D 01000001001010101110  
 Z 00110010101011011100  
 $Q_2$  0110100000000111100

#3

D 10100010010000110011  
 Z 10011101110001111101  
 $Q_3$  011110100110001011

#4

D 11000100001111010111  
 Z 10000011000000000010  
 $Q_4$  00111101001100011100

#5

D 100000000000000000001  
 Z 100010010000000000100  
 $Q_5$  0000000000000000001110