F-14 CADC MODULE SPECIFICATION

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This document provides detailed specifications for all reconstructed modules of the F-14 Central Air Data Computer (CADC), suitable for VHDL implementation.

MODULES INCLUDED

- PMU – Parallel Multiplier Unit

- PDU – Parallel Divider Unit

- SLF – Special Logic Function / ALU Core

- RAS – Random Access Storage

- SL – Steering Logic

- Control ROM + Sequencer

- I/O Bridge

SECTION 1 — PMU SPECIFICATION

Purpose:

20×20-bit signed multiply using Booth-style algorithm. Produces 20-bit result.

Interfaces:

clk – system clock

rst – reset

start – start multiplication

busy – multiplication in progress

done – result valid

operand_a – 20-bit signed

operand_b – 20-bit signed

result – 20-bit signed result

...

SECTION 2 — PDU SPECIFICATION

Purpose:

20-bit signed division using non-restoring division. Provides quotient & remainder.

Interfaces:

clk, rst, start, busy, done, dividend, divisor, quotient, remainder

...

SECTION 3 — SLF SPECIFICATION

Purpose:

Main ALU: ADD, SUB, LOGIC, SHIFT, NEG, ABS, GRAY/BINARY conversion.

Interfaces:

clk, rst, acc_in, alu_op, acc_write_enable, tmp_write_enable, flags_write_enable,

acc_out, tmp_out, flags (Z,N,C)

...

SECTION 4 — RAS SPECIFICATION

Purpose:

Local scratchpad RAM for intermediate values.

Interfaces:

clk, rst, read_address, read_data, write_address, write_data, write_enable

...

SECTION 5 — STEERING LOGIC (SL)

Purpose:

Combinational routing fabric selecting sources for ACC input, RAS write data, IO output.

Interfaces:

src_ras, src_acc, src_tmp, src_pmu, src_pdu_q, src_pdu_r, src_io_in, src_const,

sel_acc_src, sel_ras_src, sel_io_src, acc_in, ras_wr_data, io_out

...

SECTION 6 — CONTROL ROM + SEQUENCER

Purpose:

Fetch-decode-execute microinstructions; handle branching, waits, micro-PC updates.

Interfaces:

clk, rst

Inputs: flag_z, flag_n, flag_c, pmu_busy, pdu_busy

Outputs: micro_addr, micro_word and decoded control signals

Microinstruction fields (48-bit reconstructed):

NEXTCTL (47–40)

NEXTADR (39–32)

ALU_OP (31–28)

ACCCTL (27–24)

RASCTL (23–20)

SL_ACC (19–16)

SL_RAS (15–12)

PMUCTL (11–8)

PDUCTL (7–4)

IOCTL (3–0)

...

SECTION 7 — I/O BRIDGE

Purpose:

Adapt CADC core signals to/from real sensors, displays, actuators.

Interfaces:

clk, rst, io_in, io_out, io_ctrl, external sensor lines, actuator outputs

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