The F14A Central Air Data Computer
and the
LSI Technology State-of-the-Art in 1968

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This paper is designed to be a supplement to the paper "Architecture Of A Microprocessor" written in 1971 by Ray M. Holt. This paper is written because of the recent declassification of the 1968 F14A Central Air Data Computer (CADC) microprocessor design.

Introduction

With 30 years of computer architecture design, MOS/CMOS process technology, and computer history written in stone, it is difficult, at best, for the current readers to critically examine the architecture and technology decisions made in the time frame of 1968-69. I will attempt to set the stage with what we faced in 1968 for technology choices and I will attempt to present some of the design trade-off's that were made that time. The architecture and logic of the F14A MOS-LSI chips were designed my Mr. Steve Geller and myself.

Of course, it is normal and natural for the current computer designer to compare all designs with the current Intel series of microprocessors. Intel has accomplished a tremendous feat in producing commercial microprocessors that have been able to meet or exceed the expectation of the computing world. However, the current accepted microprocessor definition, (i.e. the single-chip CPU) is a by-product of, mostly, Intel's marketing needs and commercial motives and, not necessarily, the best integration of computing architecture and technology. The commercial and consumer world uses what is available at a cost-effective price.

What Did The CADC do?

The CADC performed the function of controlling the moving surfaces of the aircraft and the displaying of pilot information. The CADC received input from five main sources, 1) static pressure sensor, dynamic pressure sensor, temperature sensor, analog pilot information, and digital switch pilot information. The output of the CADC controlled the moving surfaces of the aircraft. These were the wings, maneuver flaps, and the glove vane controls. The CADC also controlled four cockpit displays for, Mach Speed, Altitude, Air Speed, and Vertical Speed. The CADC was a redundant system with real-time self-testing built-in. Any single failure from one system would switch over to the other. Two state-of-the-art quartz sensors, a 20-bit high precision analog-to-digital converter, a 20-bit high precision digital-to-analog converter, the MOS-LSI chip set, and a very efficient power unit made up the complete CADC. A team of over 25 managers, engineers, programmers, and technicians from AiResearch and American Microsystems labored for three years to accomplish a design feat never before attempted, a complete state-of-the-art, highly integrated, digital air data computer. This paper will discuss the MOS-LSI microprocessor chip set only.

The Problem

Previous Central Air Data Computers were mechanical designs. Gears, cams, potentiometers, etc were designed to implement the algorithms for the mathematical functions necessary to control the aircraft. With the F14A, a newer, lighter, faster, and higher performance aircraft was needed. Mechanical computer were not only too heavy, but they required extensive design changes to implement any changes in operational function.

The challenge presented to the F14A CADC design team was to develop a small, lightweight, reliable, low power, rugged, high performance, and flexible computer that could be shipped within two years. Extensive monetary penalties were placed on not meeting the design and delivery goals.

The F14A CADC computer had the following design requirements:

- Must fit onto one 4" x 10" printed circuit card, 40 square inches
- It's power must not exceed 10 watts at room temperature
- Must be flexible enough to handle computing capacity changes during the development cycle
- Must be programmable to accomplish eventual functional changes
- Must be able to self-test and report any failure
- Must operate at high-G forces and at Mach 1 speeds

Design Considerations

The choices for technology in 1968 was either TTL bipolar, MOS chip modules (and, or gates and flip-flops), or large-scale integrated (LSI) circuitry.

TTL bi-polar technology was eliminated because of the high package count required and for the high power consumption required. MOS gate modules were eliminated because of the high package count and the space required to implement the computing requirement.

If we were to meet the necessary requirements we were forced to consider, and eventually use, the new state-of-the-art P-Channel MOS technology. This technology being only a year or so old was attractive because of its high density capability, its low power requirements, and hopefully its low, or reasonable, cost. Eventually, American Microsystems Inc of Santa Clara, CA was our selected as our preferred vendor because they had custom chip design experience, was willing to work with us, was able to provide extremely capable design engineers, and had proven capability in the P-MOS process technology. Even so, this project proved to be very aggressive considering its time schedule, its mil spec temperature requirements which greatly reduced the chip densities, and the computing architecture styles which had never been integrated at such a large scale.

Large Scale Integration – 1967-69

I will present the state-of-the-art at the time of the F14A CADC microprocessor development by referring to several papers, articles, and documents I used during the design trade-off's and one's I have obtained in recent months.

Joseph, Earl C. Impact of Large Scale Integration on Aerospace Computers IEEE Transactions on Electronic Computers, Vol EC-16, No. 5, October 1967

Abstract
"The continued development of Large Scale Integration (LSI) presages the advent of a fourth generation of computers, and is causing an upheaval at all levels of computer technology – both technical and managerial. Today's computers use integrated circuit components containing at most ten gates per component; however, LSI is introducing hundreds of gates per component and will eventually evolve into thousands of gates per component. To the aerospace planner, this technological breakthrough of LSI means tremendous reductions in cost, size, weight, and power consumption of logic components, together with increased speed and reliability. However, for the aerospace planner to successfully implement aerospace computers with LSI, the computer designer and manager must reorient their methodology and goals. A multitude of new design and cost considerations must be carefully scrutinized, and out of this must come the new techniques that will permit effective incorporation of LSI in aerospace computers."

Higher speed, a smaller system, greater reliability, and lower cost stem from the physical structure (more gates per component with no increase in component size) and the LSI component. These inherent features of LSI, together with multiprocessor system organization, point to future aerospace computers with capabilities equal to today's best ground base systems."

"Today, we build our computers using integrated circuits components with two or four and at most ten gates per component."

Pin Minimization
"The designer will be forced to organize the logic per component in a fashion that will minimize the number of pins required to connect the LSI into the system."

Reliability
"It is of great importance to the aerospace system designer that the LSI features of higher speed and smaller systems can be obtained with greater reliability, lower power, and at a reduced cost over present day systems."

Parity (error) checking
"In an LSI component, where many logic nodes exist, multiple logic node failures are likely, such as, when a crack propagates through a chip."

"Most likely, in the future the designer will resort to forms of multiple checking (various coding techniques) with LSI."

Survival of Industry in the LSI Era
"LSI protends the computer on a chip – would you believe a single wafer or perhaps two wafers? This certainly will occur; the only question is when."

Conclusion
"We are only at the threshold of LSI. Its large-scale implementation lies ahead of us."

Levy, Saul Y. System Utilization of Large-Scale Integration IEEE Transactions on Electronic Computers, Vol EC-16, No. 5, October 1967

"The system architectural problem is one of maximizing the benefits of reliability and speed to be derived from utilizing the LSI technology, benefits obtained by minimizing connections external to the arrays and encompassing all functionally related logic in one tightly packed array."

Feth, G.C. & Smith, M.G. "Large-Scale Integration Perspectives" Computer Group News, November 1968

Introduction
"LSI is a physical reality, yet it has a long way to go to reach the impact so often forecast."

"How large is large-scale is not fully agreed upon. Is it 50, 100, or 200 circuits on a chip; is it a computer on a wafer; or is it simply a level of integration just a little beyond what is attainable today?"

LSI is Packaging
"An important point which should be emphasized here is that the economic impact of LSI is not only on the basic circuit costs, but also in the displacement of packaging costs. In a real sense LSI is packaging."

MOS Technology
"Consequently, the simple geometry of MOS circuitry leads to very high packing density, which is particularly appropriate to LSI."
Larger and Cheaper
"Table II presents a representative projection of MOS integrated circuitry."

TABLE II.
PROJECTED MOS INTEGRATED CIRCUITRY

MEMORIES	1968	1969	1970	1972
R/W				
BITS/CHIPS	64	256	512	1024
COST/BIT (1000 LOTS)	25¢	10¢	2¢	0.5¢
SPEED FOR 1024 WORDS (μSEC)	1.0	0.3	0.25	0.15
CHIP SIZE MILS²	9K	10K	12K	15K
ROM				
BITS	1024	2048	2048	4096
COST/BIT (1000 LOTS)	4¢	1¢	0.3¢	0.1¢
SPEED 1024 WORDS (μSEC)	1.0	1.0	1.0	0.5
TOOLING COST	$750	$500	$400	$400
SHIFT REGISTERS				
BITS/CHIPS	256	256	1024	2048
COST/BIT (1000 LOTS)	10¢	4¢	1¢	0.3¢
SPEED	5MC	5MC	20MC	20MC
LOGIC-BUILDING BLOCK				
FUNCTIONS/CHIP	100	180	250	500
COST/FUNCTION (100 LOTS)	40¢	25¢	15¢	7¢
CHIP SIZE MILS²	10K	15K	15K	17K
DELAY PER STAGE, F/O = 2 (NSEC)	80	60	40	30

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Packaging
"Of all the claim made of LSI, few have promised the complete system-packaging efficiency representative of an advanced technology. While concentrated efforts are being made to produce more complex chips (with high device densities and higher yields), the industry patiently awaits the time when it can specify and purchase a packaged computer on a slice. This goal may indeed be desirable, but major problems still intervene. In the meantime, most companies are attempting to optimize parts as well as the user-designer interface at the chip level."

LSI for Memory
"A major LSI interest today is in memory. Obviously, it would be a significant boon to LSI if it could compete for the memory market, and particularly the main memory market."

Conclusion
"LSI is a natural and fundamental extension of technology. There are variations, but ultimately the direction is inescapable.

"LSI imposes some additional conditions in its implementation and application. We will have to be a little more clever."

Fischel, Jack & Gee, Shu W. Aeronautical Flight-Control Systems Research Aerospace Electronic Systems Technology: A Briefing for Industry, May 3-4, 1967, p 259

"The primary flight-control system configuration now being used, an electrical-mechanical-hydraulic combination, has proved to be fairly reliable… However, the rate of advancement of the fly-by-wire system rest entirely with the electronics industry in providing completely reliable, low-cost, easily maintained systems for the more exacting flight control of future aircraft."

Boyce, Jefferson C. Microprocessor and Microcomputer Basics Prentice-Hall 1979 p. 3

"Continued development and new techniques finally resulted in capabilities to pack hundreds of components into extremely small spaces, and in about 1967 the first practical LSI assembly emerged. It was this high-density packaging that has allowed the microprocessor to become a reality and to usher in the era of low-cost computing."

Computing Architecture

Alt, Franz L. & Rubinoff, Morris Advances in Computers Academic Press, Vol 9, 1968, p.17

New Systems
"Most computing systems of the last two decades have had a fundamental structure proposed by von Neumann, i.e. they consist of a certain number of registers connected to a memory on one hand and to an arithmetic unit on the other with appropriate shuffling of numbers dictated by a control unit. It is a tribute to von Neumann's genius that this arrangement should have become completely standard. The time has come, however, for compute designers to reassess the situation and to think in terms of arrangements in which either the memory and processing functions are more intimately connected or in which there is a very strong parallelism even to the extent of having hundreds of arithmetic units."

Selecting a computer design architecture is like selecting the best house for a given piece of property. There are many parameters to consider when deciding upon the optimal configuration. For computers these parameters are usually based upon speed, size, power consumption, and cost.

When designing without size and power consumption constraints computing architecture designs are centered around speed. How fast can we make this machine go? How can we optimize our instruction set to pick up speed? When small space and low power are included into the design constraints then the overall problems is complicated ten-fold, at best.

Some of the issues we were faced with in determining the final F14A CADC microprocessor architecture are:

- PC board space – will it all fit on one PC card of 40 square inches?
- Computational speed – can we perform all functions in the required time, including the single-failure built-in self-test?
- Reliability (based on pin count) & technology stability
- Project schedule & the likelihood of finishing on time
- Power consumption – can we keep it at 10 watts at room temperature
- Temperature range – will it operate over mil spec temperature ranges
- Will it withstand the acceleration and mechanical shock?

Given these constraints we ended up with the following design guidelines:

- P-MOS technology would be used because of its high density capability
- Unique chip designs would be kept to a minimum
- Package size would be kept to a minimum
- Package quantity would be kept to a minimum
- Package pin counts would be minimized overall
- Data transfer between any chips or computing modules would be serial

Working within these guidelines we had to come up with a computer architecture that would meet the performance requirements.

Our first approach was the classical single arithmetic unit, instructions stored in ROM, temporary values and results stored in random-access memory and some form of input/output. This well know design which could have been implemented easily with the current MOS technology did not have enough computational power. In other words, we could not drive the chips fast enough, at the required temperature spec's, to perform all of the necessary functions. If we were implementing a consumer application, such as a calculator, at consumer spec's, it would have been accomplished with ease.

Our second approach was to come up with a way to perform computations in parallel. In order to accomplish this we had to analyze the functions of the aircraft to see if and how much of the operations can be performed at the same time without causing any dynamic or stability problems to the aircraft control surfaces. An exhaustive review of the mathematical functions and the dynamics of the aircraft allowed us to come up with a parallel, multi-processor implementation whereas we could have 2 or more CPU units running at the same time. In order to accomplish this we had to synchronize the CPU's and to provide an instruction command set that allowed data transfers between each.

Additionally, it was decided to increase the throughput of each CPU by providing an additional register, whereas, we could "pipeline" the instruction and data transfers. This meant that while new data was being calculated, old data was being shifted to another CPU or into random-access storage. This "pipelining" provided a tremendous speed increase without adding much to the chip space. The final configuration was determined after many weeks of design and consultation with the engineering team at American Microsystems. The final architecture was a 20-bit, multi-purpose, microprogrammed, pipelined, multi-processor, using MOS P-channel technology. Only six unique chips were required. The total number of devices (or transistors) in the system was 74,442 of which 62,092 was the stored program instructions in read-only memory.

Pushing the limits of the technology and the complexity of the architecture put an additional risk factor on the project schedule. We had less than one year to implement the chips, program the ROM's, fabricate the chips, and test the system. In order to reduce this risk factor as much as possible we used a team of programmers to entirely simulate the chip design (transistor by transistor), the timing between the chips, and the stored program instructions. Before we committed to final silicon with the chips we had a 99% confidence level that everything would work. We were not so brave as to expect 100%, even though we would have not been surprised had we accomplished it.

In addition, we had the requirement to completely self-test all the chips in the system and report any single failure. In order to do this we used our program simulation and generated an exhaustive set of test patterns and results that would continuously run through all of the chips along with the normal flight requirements. Our simulation showed us we accomplished this goal.

The completed F14A CADC was prototyped with off-the-shelf MOS devices and demonstrated to operate as designed. After extensive software simulations, test patterns, prototyping, we committed our instruction set to ROM. Turn around on ROM was several months. We anxiously waited the arrival of the first ROM set and plugged them into our actual first CADC system. The first day of testing was 100% successful. Every function performed flawlessly. The second day we discovered a slight, but critical, glitch in moving one of the surfaces. Our investigation resulted in one ROM bit was incorrectly programmed. One out of 62,092 is a great percentage, especially for hand programming, however, it required us to wait another month or so for the new ROM. The second set was perfect.

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Did It Work?

First CADC's were delivered to Grumman in early 1970. The first flight of the No. 1 prototype F14A took place on December 21, 1970. The fully proven F14A was introduced to the fleet only 51 months after contract award. A total of 557 F14A's were produced of which 32 are still scheduled for upgrades to F14A+. The Tomcat's size, speed, and range, outstanding cockpit visibility, coupled with its unparalleled radar and missile systems makes it the premier fighter in Western service according to many observers. Grumman succeeded in delivering the F14A on time, on cost and as an even better fighter than they contracted for!

Moore's Law

Gordon Moore's observation, in 1965, of semiconductor growth and performance led to what is now called Moore's Law. Each new chip contained roughly twice as much capacity as it predecessor, and each chip was released within 18-24 months of the previous chip.

Applying Moore's Law to the F14A microprocessor chips which were produced approximately 18 months prior to the Intel 4004 meant that we should have only been able to put 1,000-1,500 devices (or transistors), or less, on a chip when, in fact, we were able to get as much as 3,268 and at mil spec temperature ranges. A testimony to the engineers and the P-channel process at American Microsystems Inc.

Micro Is The Name

In the '67-'69 timeframe, as technology was advancing towards 100's and even 1000's of devices (transistors) per chip several terms starting appearing describing this new breed of technology.

Integrated Circuits

LSI – large-scale integration

MOS-LSI large-scale integration made from the MOS technology

Microelectronics – small electronics or more specifically logic gates in one package.

Microminature – small circuit boards containing complete functions normally on several large circuit boards. Mostly accomplished using LSI circuits.

Computer-on-a-chip (or slice) – intended to mean the entire computer on a chip, however, nobody really considered the I/O as part of the computer which even to this day would not make a computer-on-a chip. Later, the arithmetic unit on a chip. Even later, the central processing unit, or CPU, on a chip.

Microcomputer – Initially, in 1968, a computer implemented on several circuit boards. Later, on one circuit board. Even later, on several chips.

Microprocessor – Initially, in 1969, the processing unit of a computer on a single-card. Later, an arithmetic unit on a chip. Even later, the ALU with instruction decoding and a few registers on a chip. This later definition was marketed by Intel and became a "standard" definition around the 1973-74 timeframe.

What is A Microprocessor?

Prior to the commercialization of the LSI computer chips this question was not of too much concern to most people except chip designers.

However, this is 1998 and many are interested in whether the F14 CADC microprocessor was, in fact, of similar definition to the 4004 built 1-2 years later.

- **1973 from Hank Smith, Microprocessor Marketing Manager, Intel Corp**. IEEE 1973 WESCON Professional Program Session 11 Proceedings

    "A CPU uses P-channel MOS and is contained in 1, 2, 3 or 4 LSI standard dual-in-line packages from 16 - 42 pins per package".

- **Intel's definition off its web site at:**

    http://www.intel.com/intel/museum/25anniv/Hof/whatis.htm

    says, *"A microprocessor is an integrated circuit built on a tiny piece of silicon. It contains thousands, or even millions, of transistors, which are interconnected via superfine traces of aluminum. The transistors work together to store and manipulate data so that the microprocessor can perform a wide variety of useful functions. The particular functions a microprocessor performs are dictated by software."*

- **Boyce, Jefferson C. Microprocessor and Microcomputer Basics Prentice-Hall 1979**

    "A microprocessor is, by generally accepted definiiton, a large-scale integrated circuit assembly that contains about 70% of the computing capability of a very small digital computer."

Certainly the F14A microprocessor met these definitions. However, to apply a definition to a design before the definition was even in existence is slightly short-sighted and certainly takes away from the accomplishments of the F14A microprocessor architecture and chip design.

My Opinion

The fine line between a small minicomputer, a microcomputer, or a microprocessor was quite a mute point for many years as the quantity of units that would qualify under these definitions was very small and the number of people who cared was even smaller. As the commercial market for small computing devices began to explode the definition marketed by Intel dominated.

Consequently, the perception today is that small computers, the MOS-LSI computers, and other highly integrated devices did not exist prior to 1971 i.e. the introduction of the 4004. When in fact, 1971 was almost two years after the initial design of the first MOS-LSI microminature, microprogrammed, parallel processing, pipelined computer, which I will take the liberty, as designer, to call it the very first microprocessor, because that is, in fact, what we called it. A significant achievement, under very tight constraints, by a tremendous team, for a world class aircraft.

My Claims for the F14A Microprocessor and Related Chip Set

1st microprocessor and microcomputer
1st aerospace microprocessor and microcomputer
1st "fly-by-wire" flight computer
1st military microprocessor and microcomputer
1st production microprocessor and microcomputer
1st fully integrated chip set microprocessor and microcomputer
1st 20-bit microprocessor and microcomputer
1st microprocessor and microcomputer with built-in programmed self-test and redundancy
1st microprocessor and microcomputer in a digital signal processor (DSP) application
1st microprocessor and microcomputer with execution pipelining
1st microprocessor and microcomputer with parallel processing
1st integrated math co-processors (PDU and PMU)
1st Read-Only Memory (ROM) with a built-in program counter

Respectfully submitted,

Ray Holt