

944125
ROM

4.0 LOGICAL SPECIFICATION

4.1 DEFINITION OF SYSTEM TERMS

BIT TIME: ONE COMPLETE CLOCK PERIOD, 2.66 SEC AT 375 KHZ.

SEE FIGURE 2.

WORD TIME: 20 CONSECUTIVE BIT TIMES (t_0 THROUGH t_{19}). THERE ARE TWO TYPES OF "WORDS".

IN w_A , THE PARALLEL ARITHMETICAL ALGORITHMS OPERATE AND CONTROL WORDS ARE SHIFTED INTO THE UNITS (SERIALLY).

IN w_O , COMPUTATIONAL INPUTS AND OUTPUTS ARE SHIFTED SERIALLY AMONG THE UNITS.

THESE WORDS ALTERNATE AND ARE OF EQUAL DURATION,
i.e., THEY ARE COMPLEMENTARY.

WORD MARK: A SIGNAL COINCIDENT WITH t_{18} OF EVERY WORD TIME.

OPERATION ("Op") TIME: TWO CONSECUTIVE WORD TIMES (w_A AND w_O).

FRAME MARK: t_{18} OF THE FINAL Op.

WORD LENGTH IS 20 BITS. FOR DATA WORDS, THIS IS NORMALLY SIGN AND 19 BITS. DATA IS SHIFTED LSB FIRST. TWO'S COMPLEMENT REPRESENTATION IS USED FOR NEGATIVE NUMBERS. DURING BIT TIME t_0 , INFORMATION IN THE COMPUTER REGISTERS IS "PROPERLY ORIENTED"; i.e., ALL THE BITS OF A DATA WORD ARE CONTAINED IN PROPERLY CORRESPONDING REGISTER POSITIONS. CONTROL WORDS ARE SHIFTED INTO THE LOGIC CHIPS FROM READ-ONLY MEMORIES (ROM's) SERIALLY DURING w_A OF EVERY OP, AND THEREBY SPECIFY VARIOUS DETAILS OF THE PRESENT AND SUBSEQUENT OPERATIONS. MEANINGFUL DATA TRANSFERS INTO AND OUT OF THE LOGIC CHIPS AND REGISTERS OCCUR DURING w_O OF EVERY OP.

4.2 FUNCTIONAL DESCRIPTION

THE ROM SHALL OPERATE AS A 2560 BIT RANDOM ACCESS/SEQUENTIAL ACCESS DEVICE.

THE DEVICE SHALL STORE FIXED PATTERNS OF 128 WORDS OF 20-BIT LENGTH FOR SERIAL

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	SCALE	REV	SHEET 9

READOUT, THE PATTERNS TO BE SPECIFIED BY THE PURCHASER. THE ADDRESS PROVIDED THE ROM WILL BE A 20 BIT SERIAL BINARY WORD; THE FIRST SEVEN BITS INDICATING WHICH OF THE 128 WORDS IS TO BE ACCESSED, AND THE NEXT 3 BITS SPECIFYING, BY MASK DECODING, WHICH ROM OUT OF A POSSIBLE 8 ROM GROUP SHOULD HAVE ITS OUTPUT ENABLED. THE ADDRESS MANAGEMENT IS TO BE ACCOMPLISHED BY A COUNTER CONTAINED WITHIN THE ROM WHICH (1) IS RESETTABLE, (2) IS STEPPABLE SUCH THAT THE MEMORY CAN BE SEQUENCED THROUGH THE 128 WORD FIELD AND UP INTO THE ROM SELECT FIELD, (3) ACCEPTS "RETAIN ADDRESS" COMMAND, (4) ACCEPTS A NUMERICAL INPUT FOR INDEPENDENT ADDRESS MODIFYING OR LOADING. THE ROM OUTPUTS ARE (1) DATA OUTPUT, AND (2) PARITY ERROR.

4.3 INPUTS AND OUTPUTS

PROVISIONS SHALL BE MADE FOR ACCEPTING ELECTRICAL AND LOGICAL INPUTS AS FOLLOWS PHASE 1 AND PHASE 2 CLOCKS, V_{DD} , GROUND, A t_{18} SIGNAL, 6 LOGIC INPUTS AND ONE NUMERICAL ADDRESS INPUT. TWO OUTPUTS SHALL BE PROVIDED, THESE SHALL BE REFERRED TO AS "DATA OUT", AND "PARITY ERROR".

4.4 LOGICAL OPERATION

4.4.1 INPUTS

THE SIX LOGIC INPUTS ARE "RESET" (R), "RETAIN", "INCREMENT", "LOAD", "ADD", AND "SUB".

4.4.1.1 THE "R" INPUT SHALL, ON ITS NEGATIVE TRANSITION, RESET THE BITS OF THE ADDRESS REGISTER TO ALL ZEROS. IF THE "R" SIGNAL OCCURS DURING t_{ACC} , IT SHALL NOT AFFECT THAT DATA. THE NEXT STATE OF THE ADDRESS COUNTER SHALL BE ALL ZEROS. THE "R" INPUT WILL BE COINCIDENT WITH t_{18} . The "R" input shall override "Retain", "Increment", "Load", "Add", and "Sub" inputs.

4.4.1.2 THE "RETAIN" INPUT SHALL HOLD THE CURRENT ADDRESS OF THE COUNTER. THE NATURE OF THIS SIGNAL WILL BE SUCH THAT IT WILL BE A LOGICAL "1" DURING THE COUNT INTERVAL (t_{ACC}).



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	SIZE	CODE NO.	DWG NO.
	A	70210	944125
SCALE		REV	
			SHEET 10

- 4.4.1.3 THE "INCREMENT" INPUT WILL BE A 20-BIT LOGIC LEVEL. IF THIS IS A LOGICAL "1", THE ADDRESS COUNTER SHALL BE INCREASED BY ONE AND THE NEWLY ADDRESSED DATA SHALL BE SHIFTED OUT DURING THE NEXT W_{ACC}.
- 4.4.1.4 THE "LOAD" INPUT WILL BE A LOGICAL "1" WHEN A NEW ADDRESS IS TO BE LOADED INTO THE ADDRESS REGISTER.
- THE NEW ADDRESS WILL APPEAR ON THE "ADDRESS INPUT" COINCIDENTALLY WITH THE "LOAD" SIGNAL.
- 4.4.1.5 WHEN THE "ADD" INPUT IS A LOGICAL "1", THE ADDRESS INPUT SHALL BE ADDED TO THE CONTENTS OF THE PREVIOUS ADDRESS.
- 4.4.1.6 WHEN THE "SUB" INPUT IS A LOGICAL "1", THE ADDRESS INPUT SHALL BE SUBTRACTED FROM THE CONTENTS OF THE PREVIOUS ADDRESS.
- 4.4.1.7 THE "ADDRESS INPUT" WILL CONTAIN DATA TO BE USED AS COMMANDED BY THE LOGICAL INPUTS. VALID INPUTS WILL APPEAR DURING THE NON-ACCESS (W_{ACC}) PERIOD.
- 4.4.1.8 THE "ADDRESS FIELD" SHALL BE AS FOLLOWS: THE FIRST SEVEN LSB'S SHALL SELECT ONE OF 128 20-BIT WORDS. THE NEXT THREE SHALL BE USED TO SELECT ONE OF EIGHT ROM'S, THE REMAINING TEN SHALL BE ZERO. THE THREE-BIT SELECT FIELD WILL DETERMINE, BY MASK DECODING, WHICH CHIP'S (ROM) OUTPUT IS TO BE ENABLED. ROM'S WHICH ARE NOT ENABLED BY THE CHIP SELECT FIELD SHALL DISABLE THEIR OUTPUTS.
- 4.4.1.9 THE "ACCESS" PERIOD (W_{ACC}) SHALL BE DEFINED AS THE PERIOD DURING WHICH NONE OF THE FOLLOWING IS AT A LOGICAL "1": RETAIN, INCREMENT, LOAD, ADD, SUBTRACT.
- 4.4.1.10 THE "RESET", "INCREMENT", "LOAD", AND "RETAIN" INPUTS ARE MUTUALLY EXCLUSIVE.
- 4.4.1.11 THE "ADD" AND "SUBTRACT" INPUTS ARE MUTUALLY EXCLUSIVE.
- 4.4.1.12 THE "RESET", "INCREMENT", "LOAD", OR "RETAIN" INPUTS SHALL OVERRIDE THE "ADD" AND "SUBTRACT" INPUTS.



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SIZE	CODE NO.	DWG NO.
A	70210	944125
SCALE	REV	SHEET

4.4.2 OUTPUTS

TWO OUTPUTS SHALL BE PROVIDED, "DATA OUTPUT", AND "PARITY ERROR".

4.4.2.1 THE "DATA OUTPUT" SHALL CONTAIN THE 20-BIT SERIAL DATA WORD ADDRESSED BY THE ADDRESS REGISTER. THE OUTPUT DEVICE SHALL BE CONSTRUCTED SUCH THAT IT MAY BE WIRE OR'ED WITH THE OUTPUTS OF ASSOCIATED ROM'S, THERE BEING NORMALLY ONLY ONE OUT OF A GROUP OF WIRE OR'ED ROM'S WHICH IS ENABLED.

4.4.2.2 THE "PARITY ERROR" OUTPUT IS FROM A DEVICE THAT CHANGES STATE FOR EVERY OCCURRENCE OF STATE CHANGE IN THE ENABLED "DATA OUTPUT" OF AN ROM. DURING t_0 OF EVERY 20-BIT PERIOD, THE PARITY DEVICE SHALL BE SET FOR A "ONE" OUTPUT AND, IF THERE IS AN ODD NUMBER OF STATE CHANGES ON THE DATA LINE, THE STATE OF THE PARITY DEVICE DURING PHASE ONE (NEGATIVE TRANSITION) OF t_1 SHOULD GO TO "ZERO" (NEGATIVE TRANSITION) AND SHALL LAST UNTIL PHASE ONE OF t_0 .

ALL PARITY DEVICES IN AN ASSOCIATED GROUP OF ROM'S ARE READING THE SAME SIGNAL, i.e., THE WIRE OR'ED DATA OUTPUT SIGNAL, AS THE POINT OF TAKE-OFF FOR PARITY ON A CHIP IS THE OUTPUT PAD. THE "PARITY ERROR" OUTPUTS IN AN ASSOCIATED GROUP OF ROM'S WILL BE WIRE OR'ED TOGETHER. IF THE "RETAIN", "INCREMENT", "LOAD", "ADD", OR "SUBTRACT" INPUTS IS A LOGICAL "1", THE "PARITY ERROR" OUTPUT SHALL BE RESET TO "0" DURING W_{ACC} AT ϕ_1 OF t_0 AND SHALL LAST TO THE NEXT ϕ_1 OF t_0 .

4.5 THE LOGIC DIAGRAM IN FIGURE 4 IS INCLUDED AS A SUPPLEMENT TO THE WRITTEN SPECIFICATION.

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	A	70210	944125
SCALE	REV	SHEET	12

4.6 SYSTEM CONSIDERATIONS

THE ROM WILL TYPICALLY BE CONNECTED IN THE SYSTEM AS SHOWN IN FIGURE 6.

4.6.1 PROPAGATION DELAYS

TO INSURE PROPER INTERFACE OF THIS CIRCUIT WITH OTHERS IN THE SYSTEM,

THE FOLLOWING PROPAGATION DELAY TIMES MUST BE MET. ALL TIMES ARE MAXIMUM
AND ARE MEASURED FROM THE 90% LEVEL OF THE CLOCK TO THE 90% LEVEL OF THE
SIGNAL.

FROM	TO	TIME (NS)
ADDRESS INPUT	ADDRESS REGISTER	800
MEMORY CORE	DATA OUTPUT	250 (UNDER CONDITIONS OF PARA. 4.7.5)

ALL DATA OUTPUTS SHALL BE ON THE NEGATIVE TRANSITION OF THE PHASE ONE CLOCK.

4.6.2 THE ABOVE CALCULATED WORST CASE PROPAGATION DELAYS SHALL BE SUBMITTED TO
AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF
CONTRACT.



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SIZE	CODE NO.	DWG NO.
A	70210	944125
SCALE	REV.	SHEET
		13

4.7 ELECTRICAL CHARACTERISTICS

THE ELECTRICAL CHARACTERISTICS SHALL APPLY AT ROOM AMBIENT TEMPERATURE.

4.7.1 POWER SUPPLIES: THE INPUT POWER SUPPLY CHARACTERISTICS ARE DEFINED BELOW:

$$V_{SS} = 0 \text{ V}$$

0.0 VDC (GROUND POTENTIAL ABOUT WHICH V_{SS} AND V_{DD} ARE REFERENCED)

$$V_{DD} = +14.0 \pm 1.0 \text{ V}$$

$$V_G = -28.5 \pm 1.5 \text{ VDC}$$

4.7.2 POWER DISSIPATION:

4.7.2.1 CALCULATED POWER: THE DC POWER DISSIPATION SHALL AT -55°C AND $+125^{\circ}\text{C}$ BE CALCULATED FOR THE DEVICE COVERED BY THIS SPECIFICATION. THE CALCULATED VALUE SHALL BE SUBMITTED TO AIRSEARCH WITHIN 45 DAYS AFTER AWARD OF CONTRACT.

4.7.2.2 MEASURED POWER: THE DC POWER DISSIPATION AT -55°C AND $+125^{\circ}\text{C}$ OF THIS DEVICE SHALL NOT EXCEED THE CALCULATED VALUE BY MORE THAN 15 PERCENT.

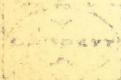
4.7.3 CLOCK CHARACTERISTICS: THE CLOCK CHARACTERISTICS ARE DEFINED IN FIGURE 2 OF THIS SPECIFICATION.

4.7.4 LOGIC LEVELS: THE MOS INPUT AND OUTPUT LOGIC LEVELS ARE DEFINED IN THE MATRIX BELOW:

	(MIN)	(MAX)
INPUT LOGIC "0"	-3.0 V	0.0 V
INPUT LOGIC "1"	V_{DD}	-9.0 V
OUTPUT LOGIC "0"	-2.0 V	0.0 V
OUTPUT LOGIC "1"	V_{DD}	-10.0 V

W_0 , t_{18} , FRAME MARK AND DISCRETE INPUT LOGIC LEVELS ARE DEFINED IN THE MATRIX BELOW:

	(MIN)	(MAX)
INPUT LOGIC "0"	-0.6 V	0.0 V
INPUT LOGIC "1"	-15.4 V	-12.6 V



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SIZE	CONT. NO.	DATE REC'D.	944125
A	70210		
SCALE	REV	MFG	14

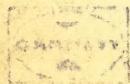
4.7.5 OUTPUT DRIVE CAPABILITY: EACH OUTPUT SHALL BE CAPABLE OF DRIVING A LOAD TO GROUND OF 25.0 KOMS RESISTIVE IN PARALLEL WITH A 10 pF CAPACITOR PLUS A CAPACITOR EQUAL TO FOUR TIMES THE MAXIMUM INPUT CAPACITANCE ON ANY SINGLE INPUT (EXCEPT POWER, CLOCK AND TIMING INPUTS) FOR ANY OF THE FOLLOWING CIRCUITS (P/N 944125, T/AI 944111, P/R 944112, P/N 944113, P/N 944114, P/N 944118). THE CALCULATED CAPACITANCE LOAD AT -55°C AND +125°C PER ABOVE SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.7.6 INPUT LOADING

4.7.6.1 TIMING AND LOGIC INPUTS: THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL TIMING AND LOGIC INPUTS (EXCEPTCLOCKS φ_1 AND φ_2) SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.7.6.2 THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL CLOCK INPUTS (φ_1 AND φ_2) SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.

4.7.6.3 DATA INPUTS: THE INPUT LOADING (RESISTIVE AND CAPACITIVE) ON ALL DATA INPUTS SHALL BE CALCULATED AT -55°C AND +125°C AND SHALL BE SUBMITTED TO AIRESEARCH FOR APPROVAL NO LATER THAN 45 CALENDAR DAYS AFTER AWARD OF CONTRACT.



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SIZE	CODE NO.	DWG NO.
A	70210	944125
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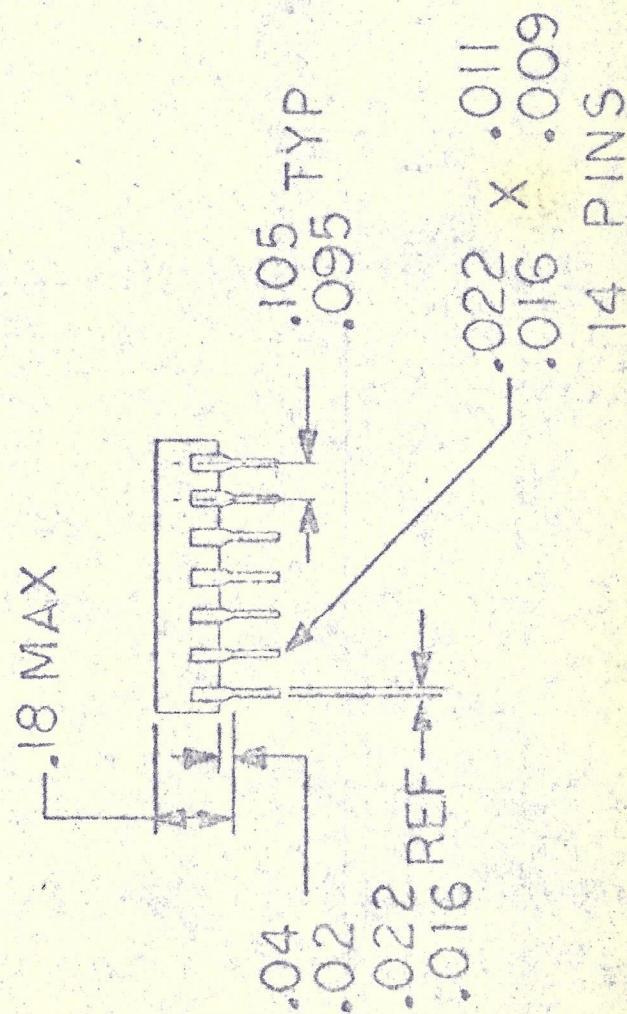
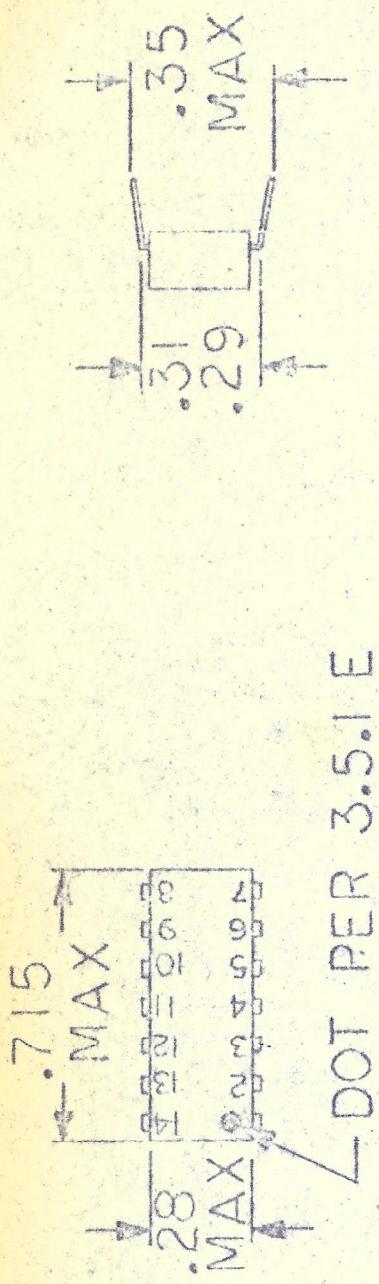


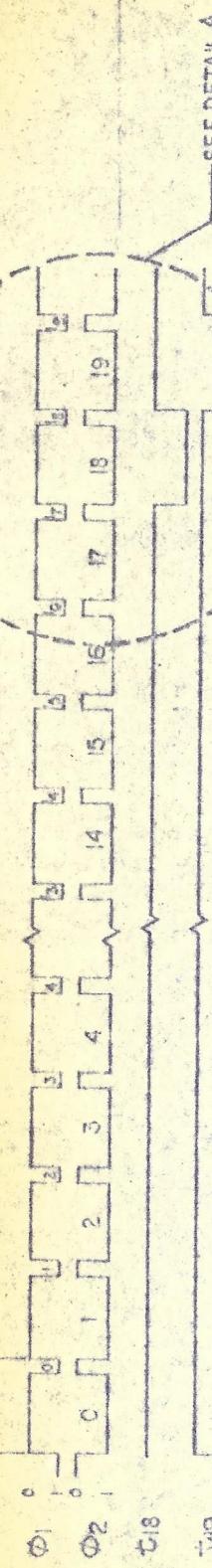
FIGURE 1 PACKAGE DRAWING

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FOR AIRCRAFT EQUIPMENT

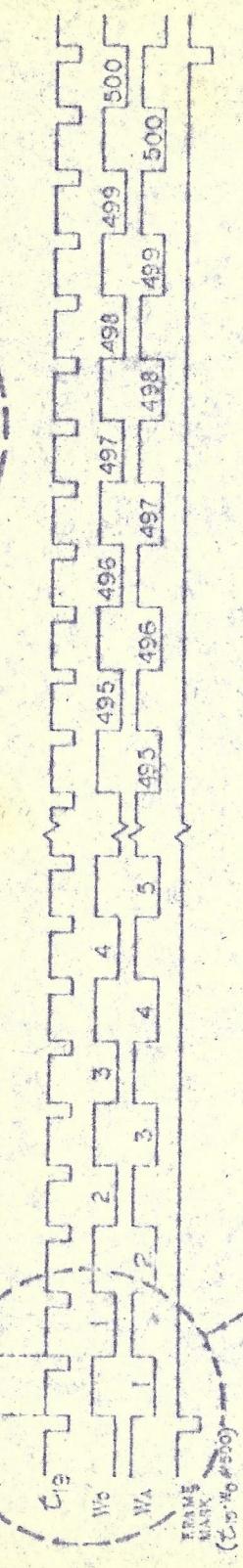
SIZE	CODE NO.	DWG NO.
A	70210	944125
SCALE	REV	SHEET
		23

18T

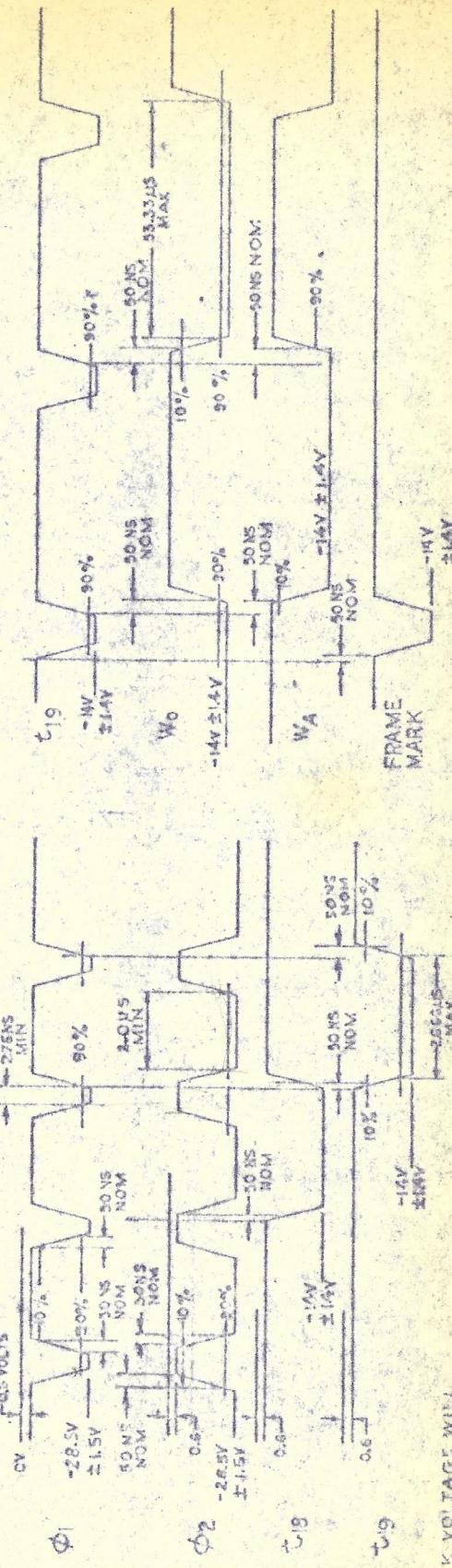
TIME



SEE DETAIL A



SEE DETAIL B



DETAIL B

FIGURE 2a TIMING DIAGRAM

DETAIL A

- CLOCK VOLTAGE WILL NOT BE POSITIVE
- MAX OVERLAP φ₁ AND φ₂
- VOLTAGE IS 30 VOLTS

NOTES:



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SIZE	CODE NO.	DWG NO.
A	70210	944125
SCALE	REV.	SHEET
1	1	24

ROM P/N 944125

PIN NAME	PIN NUMBER	INPUT CAP.		INPUT RES.	
		MAX -55°C	+125°C	MIN -55°C	+125°C
IN {	ADD	6	5 pf	5 pf	10 M _Ω
	SUB.	7	5 pf	5 pf	10 M _Ω
	LOAD	10	5 pf	5 pf	10 M _Ω
	RETAIN	2	5 pf	5 pf	10 M _Ω
	RESET(FM)	9	5 pf	5 pf	10 M _Ω
	INCREMENT	5	5 pf	5 pf	10 M _Ω
	Ø ₁	13	10 pf	10 pf	1.5 mA
	Ø ₂	12	35 pf	35 pf	0.1 mA
	t ₁₈	11	5 pf	5 pf	10 M _Ω
	DATA IN	1	5 pf	5 pf	10 M _Ω
OUT {	V _{DD}	14			
	GROUND	8			
	DATA OUT	3	6 pf	6 pf	
	PARITY OUT	4			

Chip Size: 143 x 150 mils

Number Devices: 3268 2580 memory

Package Type: 14-pin dual in-line package

DC Power Dissipation -55°C 680 mW +125°C 300 mW

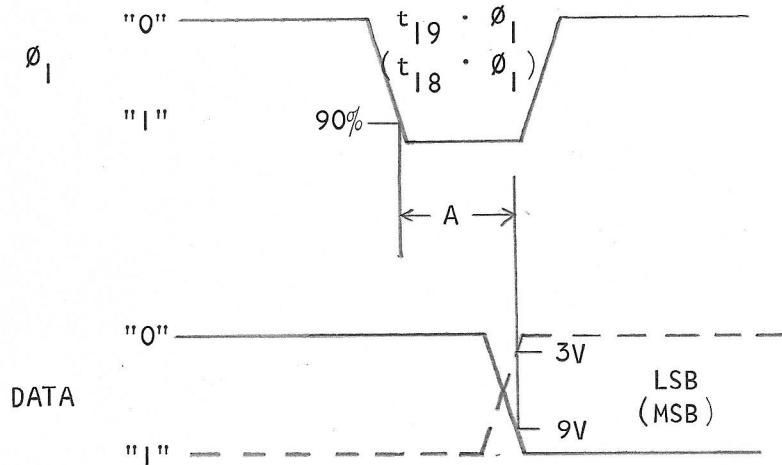
DC Power Dissipation (measured) -55°C _____ +125°C _____

Output Drive Capability Res. -55°C 75K_Ω +125°C 75K_Ω
Cap. -55°C 75pf +125°C 75pf

R. M. Holt
Dept. 93-9
July 24, 1970

PROPAGATION DELAYS - \emptyset , OUTPUT INITIATIONS

CICCUIT ROM 944125



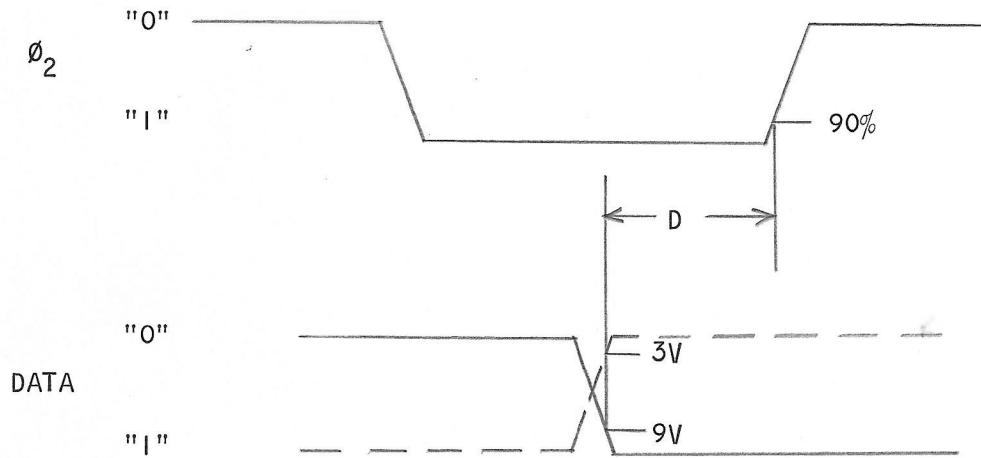
*NOTES: THIS SPEED REQUIREMENT APPLIES TO 4 OR FEWER ROM'S
TIED TOGETHER.

TERMINAL NAME	PACKAGE TERMINAL	PROPAGATION DELAY (A) MAX
DATA OUT	3	275 nS *
PARITY	4	275 nS *

R. M. Holt
Dept. 93-9
July 24, 1970

PROPAGATION DELAYS - ϕ_2 INPUT TERMINATIONS

CIRCUIT ROM 944125



TERMINAL NAME	PACKAGE TERMINAL	DATA SET-UP TIME (D) MIN
LOAD	10	1000 nS
INCREMENT	5	1000 nS $(w_0 \text{ or } w_A) \cdot t_0 \cdot \phi_2$
ADD	6	1000 nS
SUBTRACT	7	1000 nS
RETAIN	2	1000 nS
RESET (FM)	9	1000 nS
t_{18}	11	600 nS 2000
DATA IN	1	1000 nS

DATA BITS ARE FOR
ROM-4 (TEST PATTERN)

944125-4

2

101

t₈

LOAD

DATA IN

INCREMENT

ADD

SUB

RTN

FM

DATA OUT

Mod 13

PARITY

0 1 0 0 1 0 0 0 0 0 0 0 1 0 0 0 1 0 0

X

t₈

LOAD

DATA IN

INCREMENT

SUBTRACT

INCREMENT

ADD

SUB

RETAIN

FM

DATA OUT

read 13

PARITY

X

llevel =

read 10

0 0 0 1 0 0 0 1 0 0

0 1 1 1 0 0 0 0 0 1 1 0 0 1 0 1 1

DATA BITS ARE FOR

ROM - 4 (TEST PATTERN)

t8

LOAD

DATA IN

INCREMENT

ADD

SUB

RTN

FM

DATA OUT

PARITY

X

X

00010000000011100

X

00000000000000000000

X

t8

LOAD

DATA IN

INCREMENT

ADD

SUB

RETAIN

FM

DATA OUT

PARITY

X

1010100010001001110

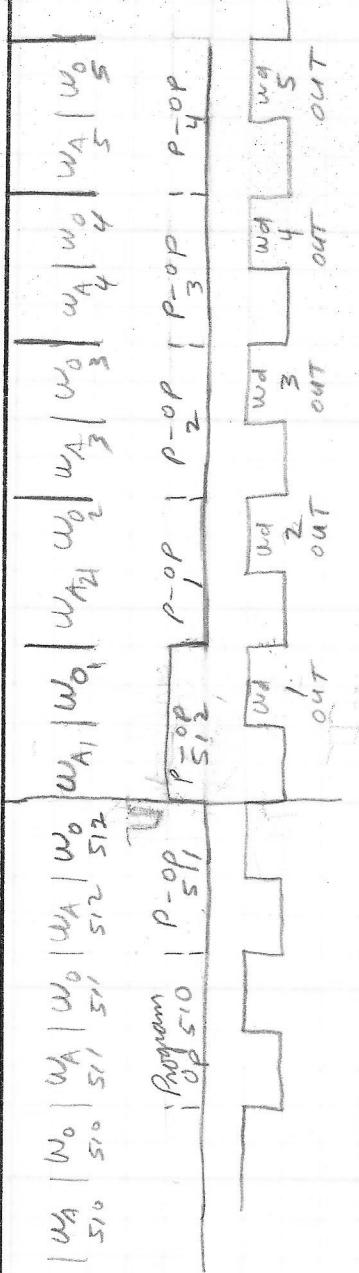
X

X

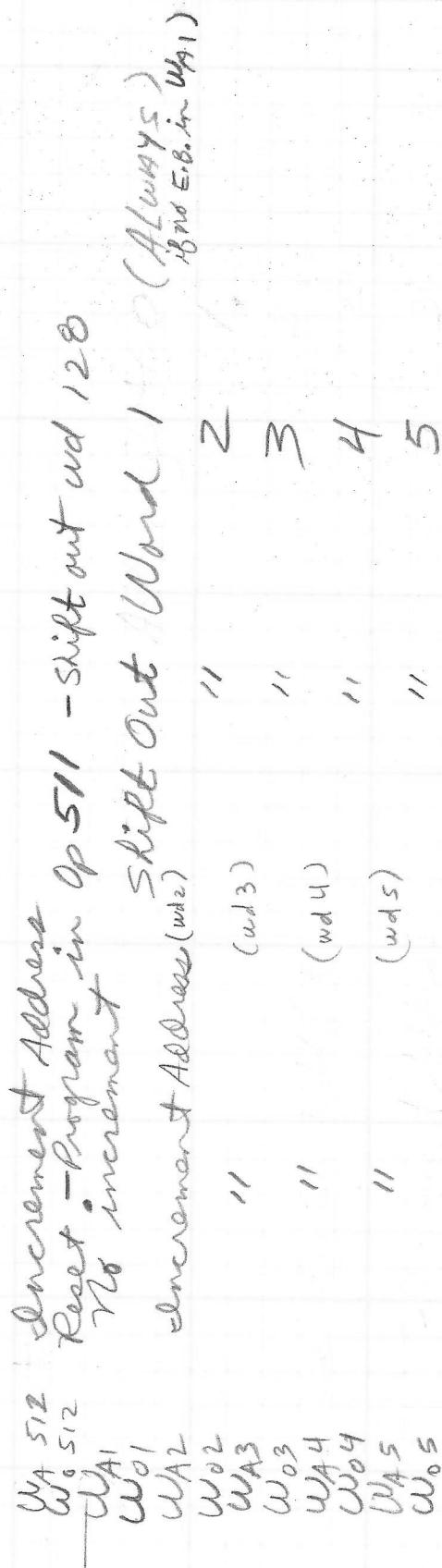
AI RESEARCH MFG. CO.

DATE 4-7-70PREPARED BY Holt

CHECKED BY _____

CALC. NO. _____
MODEL _____
PART NO. _____Data Rom w/o accessed
w/o addressed

Exe Bit :
 Exe Bit - WA¹
 (non-access and)
 increment



The executive bit should be programmed
 the operation proceeding the active one.
 To inhibit increment, do not program the
 executive bit.

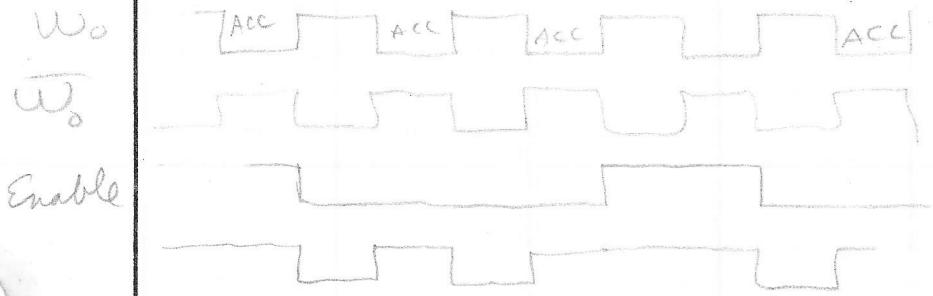
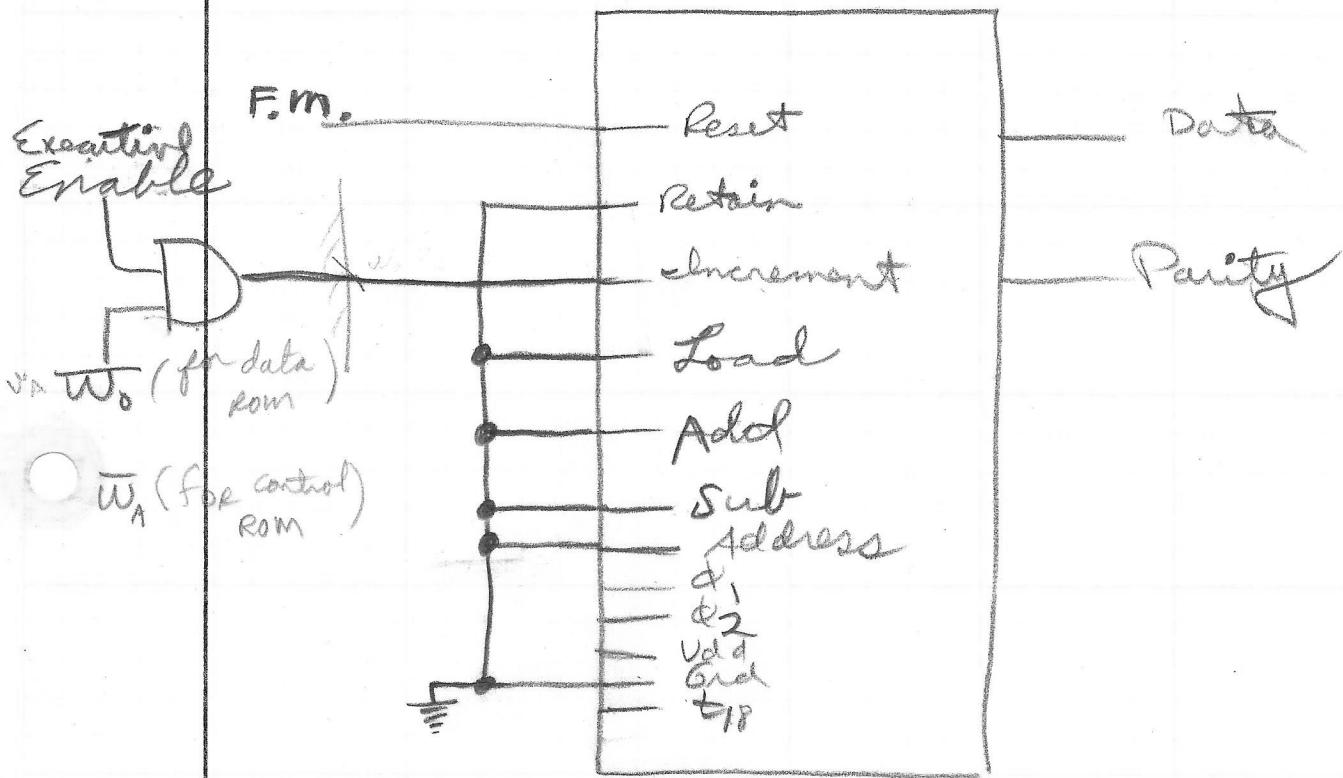
AIRESARCH MFG. CO.

DATE 4-7-70
 PREPARED BY R. Holt
 CHECKED BY _____

CALC. NO. _____
 MODEL _____
 PART NO. _____

ROM Connections

Data R.O.M.
 Control R.O.M.



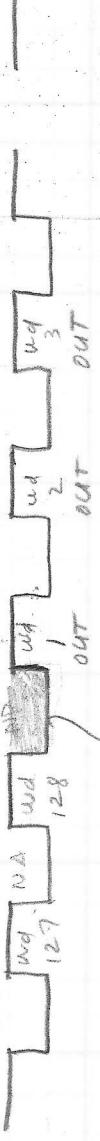
AIRSEARCH MFG. CO.

DATE 4-7-70PREPARED BY Holt

CHECKED BY _____

CALC. NO. _____
MODEL _____
PART NO. _____Control Row WA accessed
Wo addressed

| WA |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| 509 | 509 | 510 | 510 | 511 | 511 | 512 | 512 | W ₀ | W ₁ | W ₂ | W ₃ | W ₄ | W ₅ | |
| W ₁ | W ₂ | W ₃ | W ₄ | W ₅ | W ₀ | W ₁ | W ₂ | W ₃ | W ₄ | W ₅ | W ₀ | W ₁ | W ₂ | W ₃ |

EXE. BIT 0EXE. BIT. Wo 0
(non-access period)
incrementProgram: Op 509 P 120510 P 00511 P 00512 P 00513

WA510
WA511
WA512
WA512
WA1
WA2
WA2
WA3
WA3
WA4
WA4
WA5

Reset and/or increment will
address word 2.

Reset - Increment Address
Shift Out Word 1 (Always)

Increment Address (ad.)

11 2 3 4
 " " " etc.

(wd4)

etc.

REPORT

PAGE OF

To inhibit increment, do not
program the executive bit.