Exercise 1

A swapping system eliminates holes by compaction. Assuming a random distribution of many holes and many data segments and a time to read or write a 32-bit memory word of 4 nsec, about how long does it take to compact 4 GiB? For simplicity, assume that word 0 is part of a hole and that the highest word in memory contains valid data.

Exercise 2

Consider a swapping system in which memory consists of the following hole sizes in memory order: 10 MB, 4 MB, 20 MB, 18 MB, 7 MB, 9 MB, 12 MB, and 15 MB. Which hole is taken for successive segment requests of

(a) 12 MB

(b) 10 MB

(c) 9 MB

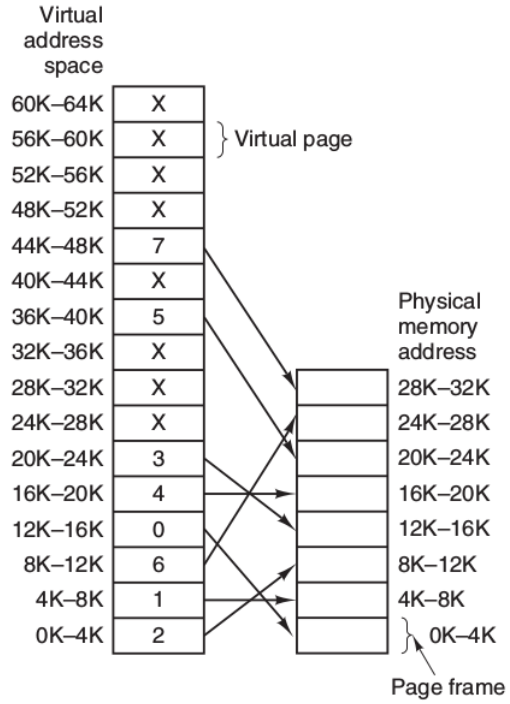
for *first fit*? Now repeat the question for *best fit*, *worst fit*, and *next fit*.

Exercise 3

For each of the following decimal virtual addresses, compute the virtual page number and offset for a 4 KiB page and for an 8 KiB page: 20000, 32768, 60000.

Exercise 4

Using the following page table (page size is 4 KiB):



give the physical address corresponding to each of the following virtual addresses:

(a) 20

(b) 4100

(c) 8300

Exercise 5

Consider the following C program:

```
int X[N];
int step = M; /* M is some predefined constant */

for (int i = 0; i < N; i += step) {
    X[i] = X[i] + 1;
}
```

(a) If this program is run on a machine with a 4 KiB page size and 64-entry TLB, what values of M and N will cause a TLB miss for every execution of the inner loop?

(b) Would your answer in part (a) be different if the loop were repeated many times? Explain.

Exercise 6

A machine has a 32-bit address space and an 8 KiB page. The page table is entirely in hardware, with one 32-bit word per entry. When a process starts, the page table is copied to the hardware from memory, at one word every 100 nsec. If each process runs for 100 msec (including the time to load the page table), what fraction of the CPU time is devoted to loading the page tables?

Exercise 7

You are given the following data about a virtual memory system:

(a) The TLB can hold 1024 entries and can be accessed in 1 clock cycle (1 nsec).

(b) A page table entry can be found in 100 clock cycles or 100 nsec.

(c) The average page replacement time is 6 msec.

If page references are handled by the TLB 99% of the time, and only 0.01% lead to a page fault, what is the effective address-translation time?