PRODUCT BRIEF

GPL32611B

Multimedia Processor

Nov 18, 2013

Version 1.0

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MULTIMEDIA PROCESSOR

1. GENERAL DESCRIPTION

The Generalplus GPL32611B, a highly integrated SoC (System-On a Chip), embedded 8Mx16 Bits SDRAM, offers a great cost-effective and high performance ratio solution for Multimedia, Virtual 3D and interactive game applications. It is embedded the ARM7TDMI with 8K-byte unified ID-cache and many tremendous features such as JPEG CODEC engine, MPEG4 decoder with de-blocking engine, MP3 decoder accelerator, face detection engine, binarization function for GPID application, TFT-LCD interface, CMOS sensor interface, scalar engine, picture process unit (PPU), TV encoder with de-flicker engine, 16-channel sound process unit (SPU), SDRAM controller, ROM/SRAM/NOR FLASH/ NAND FLASH with BCH/ECC Memory controller, UART/IrDA interface, 4-channel DMA controller, 6-channel 16-bit timers, RTC, 2 sets of SD/ MMC card interface, MS/ MS pro card interface, xD card interface, USB 2.0 mini-host/device, mono STN-LCD, interrupt controller, 2 sets of SPI (master/slave) controller, key scan controller, programmable I/O ports, stereo 16-bit DAC for audio playback, 2-channel DC-DC Boost control circuit, 1 data lane MIPI ,6-channel 12-bit ADC, MIC, PLL, and 38K-byte embedded SRAM.

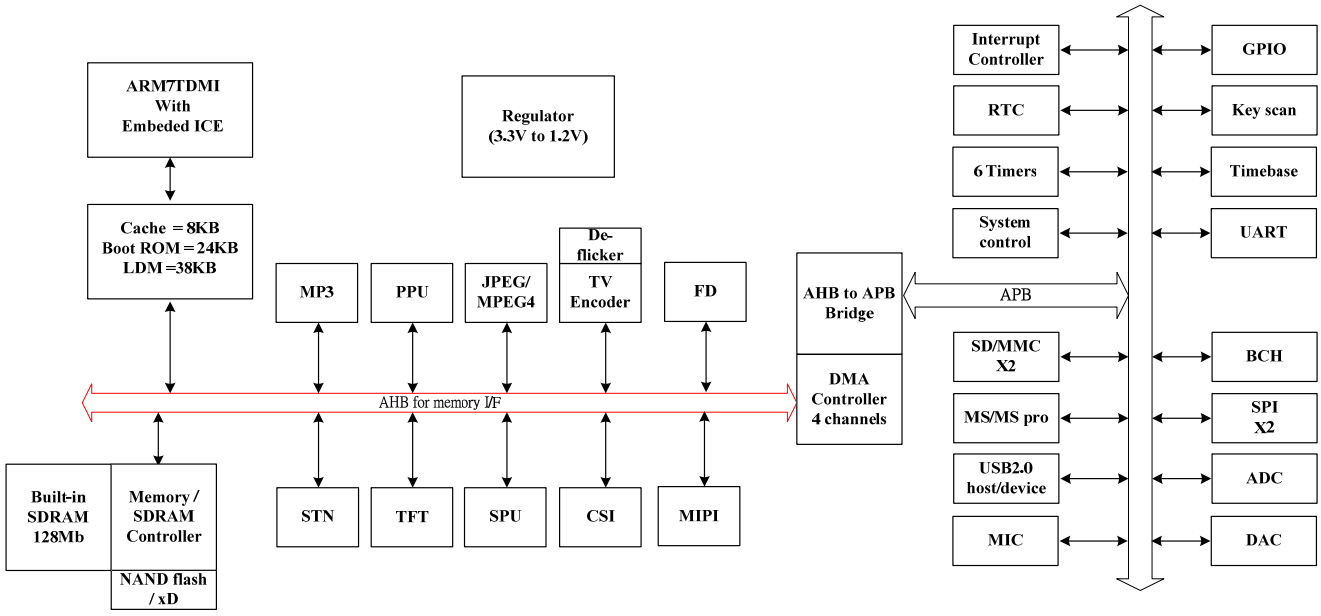
With a complete set of common system peripherals, the GPL32611B chip minimizes overall system cost and no additional component needs to be added. Not only does GPL32611B feature the high-speed performance, but it is also a cost-effective system and the most importantly - compatible with all ARM based programs.

2. FEATURES

- ARM7TDMI CPU with 8KB unified ID-cache, write buffer, embedded JTAG ICE, and working frequency up to 96MHz.
- 38KB SRAM for local data buffer.
- Picture Process Unit. (PPU)
  - Four Text layers
  - 1024 internal and 4096 extend Sprites.
  - Virtual 3D effect for text and sprite.
  - QVGA/ VGA/ D1 output.
  - Line base or Frame base operation.
  - Max. 1024x768 LCD Resolution output.
  - Texture mapping with anti-aliasing and bilinear interpolation.
- Sound Process Unit. (SPU)
  - 16 hardware PCM/ADPCM channels.
  - Built-in dynamic volume compressor.
  - MP3/WMA decoder.
- JPEG CODEC.
  - ISO/IEC 10918-1 baseline JPEG.
  - High-speed Decoding and Encoding with resolution up to 64MPixel.
  - Hardware Motion JPEG Decoding and Encoding (up to VGA@30fps) for real-time video record and playback application.
- MPEG4 decoder.
  - H.263 baseline profile level30, MPEG4 simple profile level3 Decoder (up to 30 fps @ 640 x 480 resolution).
  - Build-in de-blocking filter.
- Face Detection function
  - Supports 320x240, 5fps
  - Detection multiple faces in a photo
- OID Binary Function
- MIPI Function
  - Up to 450M bit rate
- Video-in & CMOS sensor interface and CCIR601/CCIR656 standard supported.
- Embedded 8Mx16 Bits SDRAM
- Static memory controller. (NAND FLASH with ECC and 4/8/12/16/24/40/60 -bit BCH)
- Four-channel DMA controller.
- Mono and 16 gray levels STN-LCD controller.
- TFT-LCD controller.
  - UPS051. (serial RGB)
  - UPS052. (serial RGB dummy)
  - Parallel RGB (6-6-6/8-8-8).
  - I80 (8-bit/16-bit/18-bit system bus) I/F type.
  - CCIR601/CCIR656.
  - Scalar engine inside with programmable up-scaling and down-scaling factor.
- Image Processing Unit.
  - Histogram statistics for auto brightness and contrast.
  - Programmable RGB gamma correction.
  - Color convert matrix for various post-image processing.
- 2-channel DC-DC Boost control circuit for LED Backlight and VGH/VGL voltage generator of TFT-LCD drivers.
- Interrupt Controller.
- Universal Serial Bus (USB) 2.0 high/full speed compliance device and USB mini-host with built-in transceiver.
- Watchdog timer.
- Six 16-bit timers/counters.
- 2 sets of SD/SDHC/SDIO/MMC card interface.
- MS/MS pro card interface.

- xD card interface.
- 2 sets of SPI (master/slave) interface with data rate up to 24Mbps.
- UART (asynchronous serial I/O) or IrDA interface with baud rate up to 1.8432Mbps and 115.2Kbps.
- 81 Programmable general I/O ports (GPIO) with pull-high/low control.
- 64/88 keys scan controller.
- Power manager.
- Built-in 3.3V to 1.2V Regulator.
- Low voltage reset.
- 1 data lane MIPI
- Real-time clock (RTC) with independent power supply.
- 96MHz, 27MHz and 12MHz PLL.
- 16-bit stereo DAC (2-channel) for audio playback.
- 12-bit ADC with 6 line-in channels.
- MIC with PGAC. (program gain control)
- TV encoder supporting NTSC/PAL and de-flicker and scalar function.

3. BLOCK DIAGRAM



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5. REVISION HISTORY

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