DATA SHEET

GPL162004A

Advanced 16-Bit SoC with *μ'nSP*®

2.0

Preliminary

Jun. 27, 2008

Version 0.5

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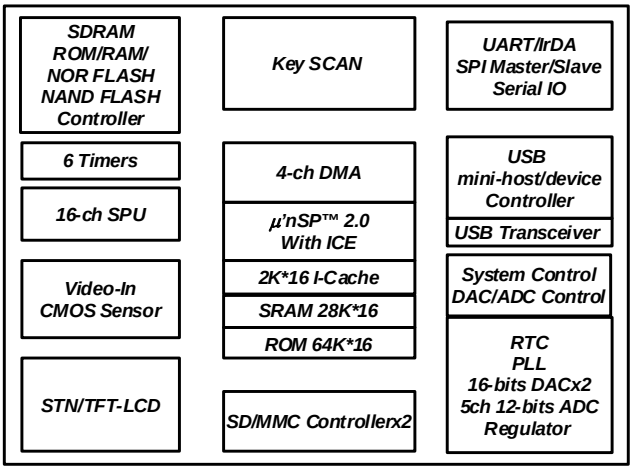
Advanced 16-Bit SoC with μ'nSP® 2.0

1. GENERAL DESCRIPTION

The Generalplus GPL162004A is highly integrated system-on-a chip and targets a cost-effective, high performance micro-controller solution for electronic dictionary, education and learning applications. It embedded μ'nSP® 2.0 (16-bit CPU developed by Sunplus Technology) with 4KB I-cache, 16 channels sound process unit (SPU), SDRAM controller, ROM/SRAM/NOR FLASH/NAND FLASH with ECC Memory controller, UART/IrDA interface, four channel DMA controller, six-channel 16-bit timers, SD/MMC memory interface, USB mini-host/device, mono STN-LCD and TFT-LCD interface, interrupt controller, SPI master/slave controller, Key scan controller, programmable I/O ports, 16-bit DAC for audio playback, 12 bits ADC, PLL, and embedded 28K*16 bits SRAM and 64K*16 ROM.

By providing a complete set of common system peripherals, the Generalplus GPL162004A chip minimizes overall system costs and eliminates the need to configure additional components. The GPL162004A provides not only the high-speed performance and low cost for a system, but it also integrates several powerful tools into the development system, such as development system with C language, assembly compiler, linker, source debugger functions and project management tools.

2. BLOCK DIAGRAM



3. FEATURES

- μ'nSP® 2.0 16-bit CPU with frequency up to 96MHz.
- 4K bytes I-cache.
- 28k*16 bits SRAM for programming or LCD frame buffers.
- 64K*16 bits ROM for embedded algorithm.
- Sound Process Unit (SPU)
  - 16 hardware PCM/ADPCM channels.
  - Built-in sound compressor.
  - MP3 decoder.
- Video-in/CMOS sensor interface supports CCIR601/CCIR656 standard.
- 96 MHz SDRAM with maximum size 64M bytes for single chip select.
- Static memory controller. (ROM/SRAM/NOR FLASH/Page Memory/NAND FLASH with ECC)
- Four-channel DMA controller.
- Mono and 16 gray STN-LCD controller.
- TFT-LCD controller which can be UPS051(serial RGB), UPS052(serial RGB dummy), parallel RGB, i80(8-bit/16-bit system bus) I/F type, and CCIR601/CCIR656.
- Twenty-eight sources Interrupt Controller.
- Universal Serial Bus (USB) 2.0 full speed compliant device and USB mini-host with built-in transceiver.
- Watch-dog timer.
- Real-time clock.
- Six 16-bit timers.
- 2 sets SD/MMC memory interface.
- SPI master/slave interface.
- UART (asynchronous serial I/O) or IrDA interface.
- 72 Programmable general I/O ports (GPIO) with pull-high/low control.
- 64/88 keys scan controller with velocity detection.
- Power manager.
- Built-in 3.0V to 1.8V Regulator.
- Low voltage reset.
- 96MHz, 27MHz and 12MHz PLL.
- 16-bit stereo DAC(2ch) for audio playback.
- 12-bit ADC with 4 line-in and 1 microphone input.

4. SIGNAL DESCRIPTIONS

Left Side

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
1	7	BKCSB0	Memory I/F	I/O	External memory chip select 0	IOD0
2	8	XA3	Memory I/F	I/O	External memory address pin 3	
3	9	XA2	Memory I/F	I/O	External memory address pin 2	
4	10	XA1	Memory I/F	I/O	External memory address pin 1	
5	11	DVSS	Digital GND	P	Digital ground	
6	12	BKCSB1	Memory I/F	I/O	External memory chip select 1	IOD1
7	13	XA0	Memory I/F	I/O	External memory address pin 0	
8	14	XA10	Memory I/F	I/O	External memory address pin 10	
9	15	XA11	Memory I/F	I/O	External memory address pin 11	
10	16	DVCC33	Digital PWR	P	3.3V digital power	
11	17	BKCSB2	Memory I/F	I/O	External memory chip select 2	IOD2
12	18	XA12	Memory I/F	I/O	External memory address pin 12	
13	19	XA13	Memory I/F	I/O	External memory address pin 13	
14	20	XA14	Memory I/F	I/O	External memory address pin 14	
15	21	DVSS	Digital GND	P	Digital ground	
16	22	IOC3	SDRAM	I/O	General-purposed I/O C3	IOC3
17	23	IOC4	SDRAM	I/O	General-purposed I/O C4	IOC4
18	24	IOC2	SDRAM	I/O	General-purposed I/O C2	IOC2
19	25	DVCC33	Digital PWR	P	3.3V digital power	
20	26	DVSS	Digital GND	P	Digital ground	
21	27	DVCC18	Digital PWR	P	1.8V digital power	
22	28	BKWEB	Memory I/F	I/O	External memory write enable pin	
23	29	BKOEB	Memory I/F	I/O	External memory output enable pin	
24	30	XA15	Memory I/F	I/O	External memory address pin 15	IOD7
25	31	XA16	Memory I/F	I/O	External memory address pin 16	IOD8
26	32	XA17	Memory I/F	I/O	External memory address pin 17	IOD9
27	33	XA18	Memory I/F	I/O	External memory address pin 18	IOD10
28	34	XA19	Memory I/F	I/O	External memory address pin 19	IOD11
29	35	XA20	Memory I/F	I/O	External memory address pin 20	IOD12
30	36	XA21	Memory I/F	I/O	External memory address pin 21	IOD13
31	37	XA22	Memory I/F	I/O	External memory address pin 22	IOD14
32	38	XA23	Memory I/F	I/O	External memory address pin 23	IOD15
33	39	DVSS	Digital GND	P	Digital ground	
34	40	AGC	ADC	A/O	For AGC circuit	IOE11
35	41	OPI	ADC	A/I	For MIC circuit	IOE10
36	42	MICOUT	ADC	A/O	For MIC circuit	IOE9
37	43	MICN	ADC	A/I	Microphone differential input	IOE8
38	44	MICP	ADC	A/I	Microphone differential input	IOE7
39	45	VMIC	ADC	A/I/O	For MIC circuit	IOE6
40	46	AVDD	ADC	P	3.3V Power for 12-bit ADC	
41	47	LINEIN1	ADC	A/I	LINEIN1 of 12-bit ADC	IOE12
42	48	LINEIN2	ADC	A/I	LINEIN2 of 12-bit ADC	IOE13

Bottom Side

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
43	61	LINEIN3	ADC	A/I	LINEIN3 of 12-bit ADC	IOE14
44	62	LINEIN4	ADC	A/I	LINEIN4 of 12-bit ADC	IOE15
45	63	AVSS	ADC	A/I/O	Ground for 12-bit ADC	
46	64	TEST	MODE	I	Test mode control signal. Input floating; it must be tied with ground under normal operation.	
47	65	RESETB	SYSTEM	I/O	Reset input pin. (Low active)	
48	66	IOB2	MODE	I/O	BM2: Boot mode selection pin 2. (0: use 6MHz crystal, usually for USB application, 1: use internal PLL, usually for other application w/o USB)	IOB2
49	67	IOB1	MODE	I/O	BM1: Boot mode selection pin 1. 1 : Internal ROM Boot (SPI boot, NAND boot) 0 : Chip Select 0 Memory Boot	IOB1
50	68	IOB0	MODE	I/O	BM0: Boot mode selection pin 0. (This pin must be pull low with a resistor)	IOB0
51	69	ICEDA	ICE	I/O	Embedded ICE data pin	
52	70	ICECK	ICE	O	Embedded ICE clock pin	
53	71	IOA7	Key/LCD	I/O	Key-scan's output 7; TFT-LCD's D7	IOA7
54	72	IOA6	Key/LCD	I/O	Key-scan's output 6; TFT-LCD's D6	IOA6
55	73	IOA5	Key/LCD	I/O	Key-scan's output 5; TFT-LCD's D5	IOA5
56	74	IOA4	Key/LCD	I/O	Key-scan's output 4; TFT-LCD's D4	IOA4
57	75	IOA3	Key/LCD	I/O	Key-scan's output 3; TFT-LCD's D3	IOA3
58	76	IOA2	Key/LCD	I/O	Key-scan's output 2; TFT-LCD's D2	IOA2
59	77	IOA1	Key/LCD	I/O	Key-scan's output 1; TFT-LCD's D1	IOA1
60	78	IOA0	Key/LCD	I/O	Key-scan's output 0; TFT-LCD's D0	IOA0
61	79	IOA8	Key/LCD	I/O	Key-scan's input 0; TFT-LCD's D8	IOA8
62	80	DVCC33	Digital PWR	PWR	3.3V digital power	
63	81	DVSS	Digital GND	PWR	Digital ground	
64	82	DVSS	Digital GND	PWR	Digital ground	
65	83	DVCC18	Digital PWR	PWR	1.8V digital power	
66	84	IOA9	Key/LCD	I/O	Key-scan's input 1; TFT-LCD's D9	IOA9
67	85	IOA10	Key/LCD	I/O	Key-scan's input 2; TFT-LCD's D10	IOA10
68	86	IOA11	Key/LCD	I/O	Key-scan's input 3; TFT-LCD's D11	IOA11
69	87	IOA12	Key/LCD	I/O	Key-scan's input 4; TFT-LCD's D12	IOA12
70	88	IOA13	Key/LCD	I/O	Key-scan's input 5; TFT-LCD's D13	IOA13
71	89	IOA14	Key/LCD	I/O	Key-scan's input 6; TFT-LCD's D14	IOA14
72	90	IOA15	Key/LCD	I/O	Key-scan's input 7; TFT-LCD's D15	IOA15
73	91	IOC8	SD2	I/O	SD2 data0	IOC8
74	92	IOC7	SD2	I/O	SD2 clock	IOC7
75	93	IOC6	SD2	I/O	SD2 command	IOC6
76	94	IOC10	SD2	I/O	SD2 data2	IOC10
77	95	IOC9	SD2	I/O	SD2 data1	IOC9
78	96	IOC5	SD2	I/O	SD2 data3	IOC5
79	97	IOC11	UART	I/O	UART/IrDA receive data pin	IOC11
80	98	IOC12	UART	I/O	UART/IrDA transmit data pin	IOC12
81	99	PLLV33	PLL	PWR	3.3V PLL power	
82	100	X32KO	PLL	O	32768 Hz crystal output pin	
83	101	X32KI	PLL	I	32768 Hz crystal input pin	

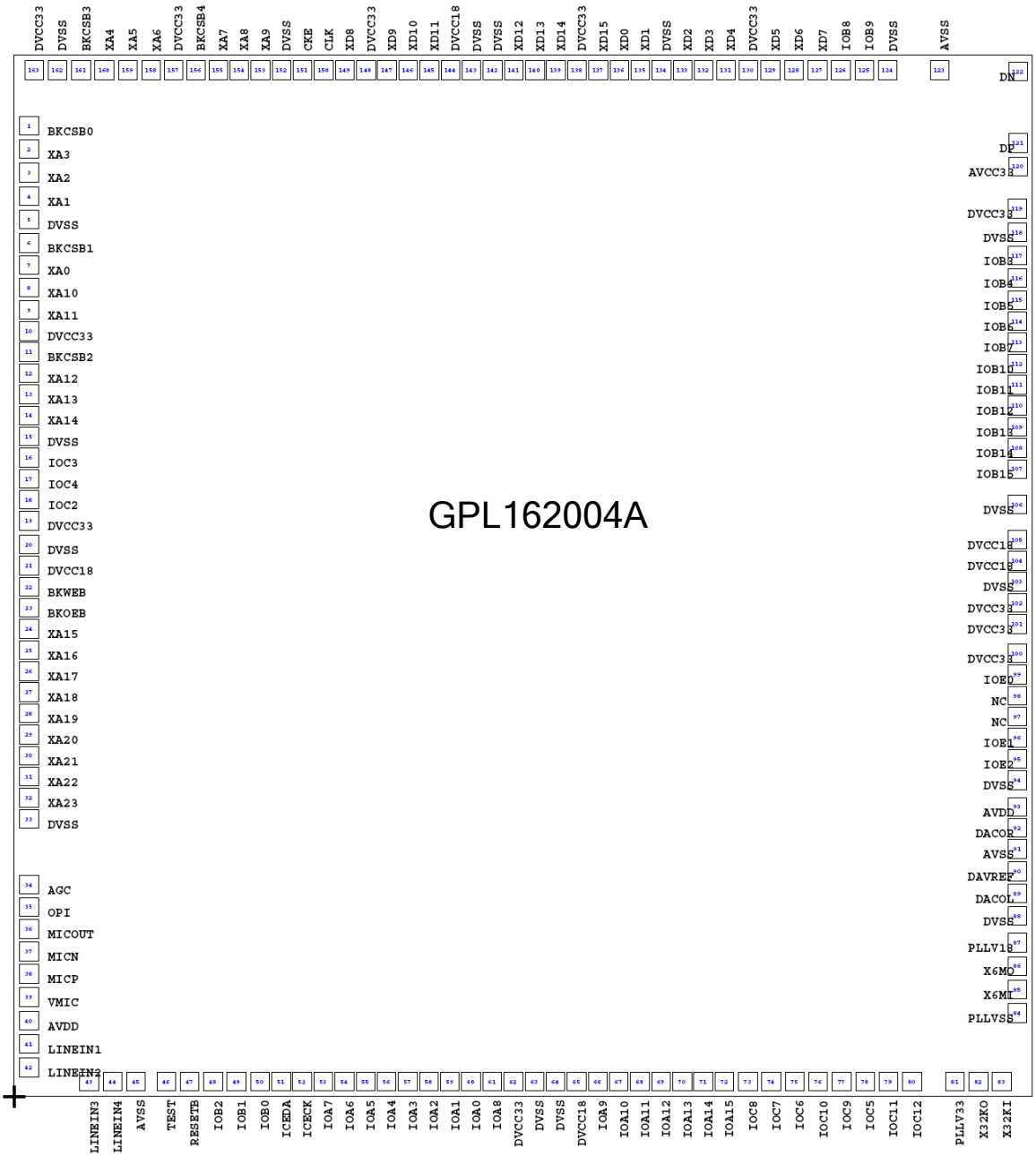
Right Side

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
84	115	PLLVSS	PLL	PWR	PLL ground	
85	116	X6MI	PLL	A/I	6MHz crystal input pin or 12M PLL filter pin	
86	117	X6MO	PLL	O	6MHz crystal output pin	
87	118	PLLV18	PLL	P	1.8V power for PLL	
88	119	DVSS	Digital GND	PWR	Digital ground	
89	120	DACOL	DAC	A/O	Left channel audio output	
90	121	DAVREF	DAC	A/O	DAC reference voltage pin	
91	122	AVSS	DAC	PWR	DAC ground	
92	123	DACOR	DAC	A/O	Right channel audio output	
93	124	AVDD	DAC	PWR	3.3V DAC power	
94	125	DVSS	Digital GND	PWR	VDAC ground	
95	126	IOE2	GPIO	I/O	General-purposed I/O E2	IOE2
96	127	IOE1	GPIO	I/O	General-purposed I/O E1	IOE1
97	128	NC				
98	129	NC				
99	130	IOE0	GPIO	I/O	General-purposed I/O E0	IOE0
100	131	DVCC33	Digital PWR	PWR	3.3V digital power	
101	132	DVCC33	Regulator	PWR	3.3V Regulator power	
102	133	DVCC33	Regulator	PWR	3.3V Regulator power	
103	134	DVSS	Regulator	PWR	Regulator ground	
104	135	DVCC18	Regulator	A/O	Regulator 1.8V output	
105	136	DVCC18	Digital PWR	PWR	1.8V digital power	
106	137	DVSS	Digital GND	PWR	Digital ground	
107	138	IOB15	SD1	I/O	SD1 data2	IOB15
108	139	IOB14	SD1	I/O	SD1 data1	IOB14
109	140	IOB13	SD1	I/O	SD1 data0	IOB13
110	141	IOB12	SD1	I/O	SD1 clock	IOB12
111	142	IOB11	SD1	I/O	SD1 command	IOB11
112	143	IOB10	SD1	I/O	SD1 data3	IOB10
113	144	IOB7	SPI	I/O	SPIRX: SPI data input	IOB7
114	145	IOB6	SPI	I/O	SPITXD: SPI data output	IOB6
115	146	IOB5	SPI	I/O	SPICLK: SPI clock	IOB5
116	147	IOB4	SPI	I/O	SPICS: SPI CS(Slave)	IOB4
117	148	IOB3	LCD	I/O	TFT DCLK	IOB3
118	149	DVSS	Digital GND	PWR	Digital ground	
119	150	DVCC33	Digital PWR	PWR	3.3V digital power	
120	151	AVCC33	USB	PWR	3.3V USB power	
121	152	DP	USB	I/O	DP pin of USB PHY	
122	153	DN	USB	I/O	DN pin of USB PHY	

Top Side

No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
123	169	AVSS	USB	PWR	USB ground	
124	170	DVSS	Digital GND	PWR	Digital ground	
125	171	IOB9	EINT	I/O	External INT1; AD bus free	IOB9
126	172	IOB8	EINT	I/O	External INT0	IOB8
127	173	XD7	Memory I/F	I/O	External memory data pin 7	
128	174	XD6	Memory I/F	I/O	External memory data pin 6	
129	175	XD5	Memory I/F	I/O	External memory data pin 5	
130	176	DVCC33	Digital PWR	PWR	3.3V digital power	
131	177	XD4	Memory I/F	I/O	External memory data pin 4	
132	178	XD3	Memory I/F	I/O	External memory data pin 3	
133	179	XD2	Memory I/F	I/O	External memory data pin 2	
134	180	DVSS	Digital GND	PWR	Digital ground	
135	181	XD1	Memory I/F	I/O	External memory data pin 1	
136	182	XD0	Memory I/F	I/O	External memory data pin 0	
137	183	XD15	Memory I/F	I/O	External memory data pin 15	
138	184	DVCC33	Digital PWR	PWR	3.3V digital power	
139	185	XD14	Memory I/F	I/O	External memory data pin 14	
140	186	XD13	Memory I/F	I/O	External memory data pin 13	
141	187	XD12	Memory I/F	I/O	External memory data pin 12	
142	188	DVSS	Digital GND	PWR	Digital ground	
143	189	DVSS	Digital GND	PWR	Digital ground	
144	190	DVCC18	Digital PWR	PWR	1.8V digital power	
145	191	XD11	Memory I/F	I/O	External memory data pin 11	
146	192	XD10	Memory I/F	I/O	External memory data pin 10	
147	193	XD9	Memory I/F	I/O	External memory data pin 9	
148	194	DVCC33	Digital PWR	PWR	3.3V digital power	
149	195	XD8	Memory I/F	I/O	External memory data pin 8	
150	196	CLK	SDRAM	I/O	SDRAM clock	IOC0
151	197	CKE	SDRAM	I/O	SDRAM clock enable	IOC1
152	198	DVSS	Digital GND	PWR	Digital ground	
153	199	XA9	Memory I/F	I/O	External memory address pin 9	
154	200	XA8	Memory I/F	I/O	External memory address pin 8	
155	201	XA7	Memory I/F	I/O	External memory address pin 7	
156	202	BKCSB4	Memory I/F	I/O	External memory chip select 4	IOD4
157	203	DVCC33	Digital PWR	PWR	3.3V digital power	
158	204	XA6	Memory I/F	I/O	External memory address pin 6	
159	205	XA5	Memory I/F	I/O	External memory address pin 5	
160	206	XA4	Memory I/F	I/O	External memory address pin 4	
161	207	BKCSB3	Memory I/F	I/O	External memory chip select 3	IOD3
162	208	DVSS	Digital GND	PWR	Digital ground	
163	209	DVCC33	Digital PWR	PWR	3.3V digital power	

4.1. PAD Assignment



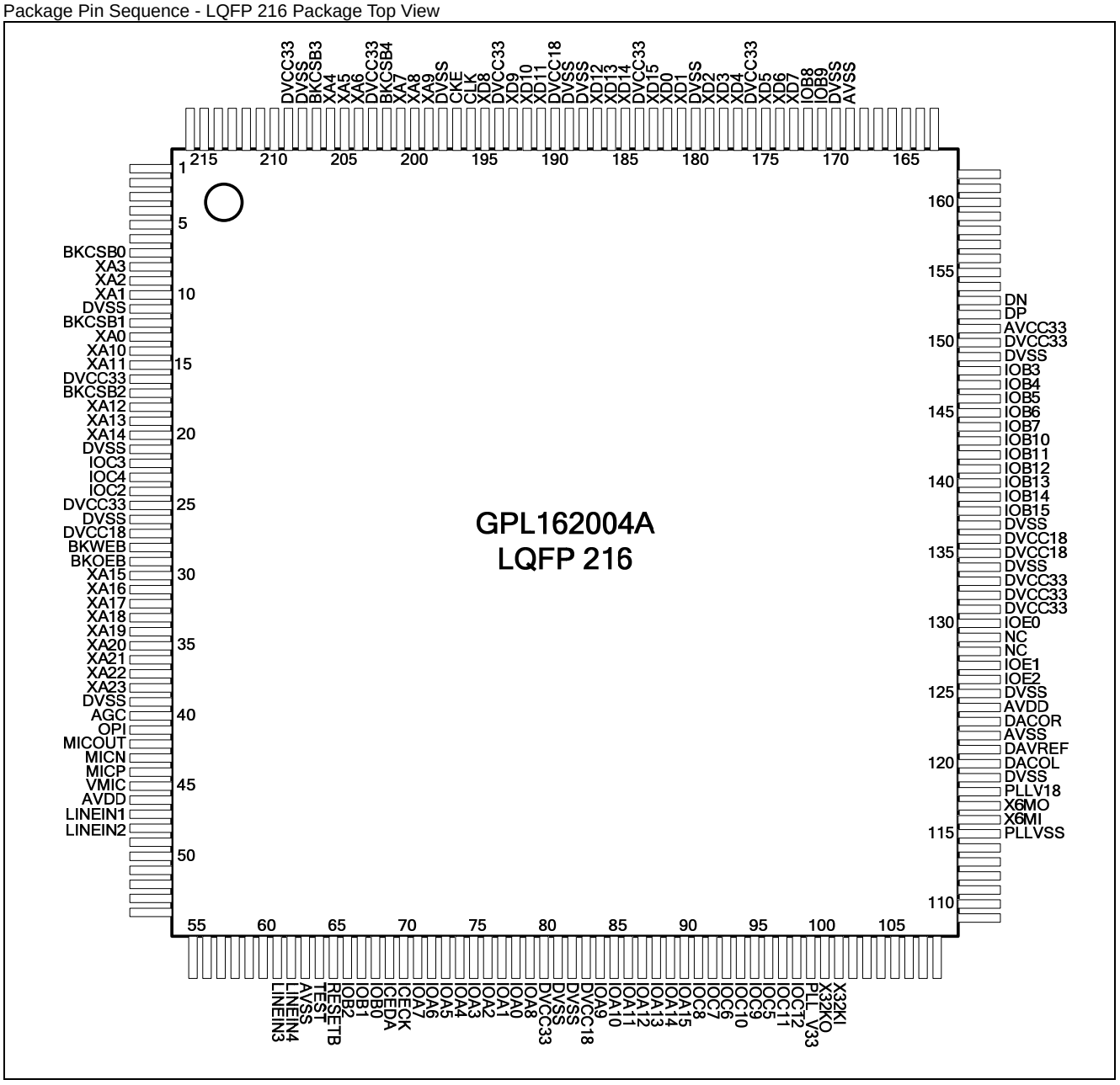
This IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as closed as possible.

4.2. PIN Map

Package Pin Sequence - LQFP 216 Package Top View



5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The GPL162004A is equipped with a 16-bit *μ'nSP*™ 2.0, the newest 16-bit microprocessor by SUNPLUS and pronounced as *micro-n-SP*. Sixteen registers are involved in *μ'nSP*™ 2.0: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP), SR (Segment Register) and R8 - R15 (General-purpose register). The interrupt include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK. GPL162004A is also built-in a 4K bytes I-cache which can increase the performance significantly.

5.2. Memory

5.2.1. Internal SRAM

The amount of SRAM is 28K-word (including Stack), ranged from 0x0000 through 0x6FFF with access speed of one CPU clock. Since this SRAM is located in CPU's locale bus, the system bus will not be occupied when this SRAM is access by CPU. This SRAM can be access freely by CPU/DMA /LCD.

5.2.2. External memory

The memory space is separate into 5 banks and each bank can be up to 256 pages, and each page is 64K words, the controller can support up to 80M words NOR type flash memories. Each bank can be programmed as SDRAM/ROM/SRAM/NOR Flash/NAND Flash. GPL162004A can support up-to 64M bytes (512Mb) SDRAM with single chip-select. 8-bit NAND flash are supported with an embedded 1/4/8 bits ECC calculation circuit which can realize the error correction mechanism on SLC/MLC NAND flash.

5.3. PLL, Clock, Power Mode

5.3.1. PLL (Phase Lock Loop)

There are three PLLs embedded in GPL162004A. 1st PLL can pump up to 96MHz, 2nd PLL can generate 27MHz, and 3rd PLL can pump 12MHz. The output frequency of fast PLL is programmable and has range from 15MHz ~ 96MHz (3MHz per step).

5.3.2. System clock

The system clock can be selected from 32768 or 12M or 96M (determined by fast PLL's output frequency) by register setting. Furthermore, a clock divider which can divide clock up to 1/128 is provided to reduce the power consumption.

5.4. Power Savings Mode

The GPL162004A provide 4 power modes, Normal, Wait, Halt and Sleep.

Mode	CPU	System	RTC	POWEREN	After wakeup
Normal	ON	ON	ON	ON	-
Wait	OFF	ON	ON	ON	Next Instruction
Halt	OFF	OFF	ON	OFF	Reset CPU
Halt2	OFF	OFF	ON	OFF	Next Instruction
Sleep	OFF	OFF	OFF	OFF	Reset System

Enter the Wait/Halt/Halt2/Sleep mode, is done by write designated value to designated port. The wake-up source can be interrupt or timer or key-change.

5.5. Video Input Interface

GPL162004A supports video input from sensor or TV decoder. The maximum input resolution is 4095x4095. A built-in scaler can be used to scale input data from arbitrary resolution to VGA or QVGA mode. A motion detect engine is also built-in GPL162004A which can realize the interactive game with sensor input. The video-in interface support CCIR601/CCIR656 format with YUV or RGB format. The output format is frame-based and the input frame rate need not to synchronous with GPL162004A's system clock.

5.6. Sound Process Unit

GPL162004A equips a 16-channel SPU. Each channel of SPU can support PCM8/PCM16/ADPCM. A dynamic volume compressor is also embedded to enlarge the overall volume. For software application, GPL162004A is also capable for MP3 decode and other wide-band(sample rate >= 16kHz) low bit rate algorithm.

5.7. Video Output Interface

5.7.1. STN-LCD Interface

The STN-LCD driver interface built-in GPL162004A supports up-to 320X240 LCD panel and supports 1/4 bits data bus for monochrome/gray-scale STN. Memory interface type CSTN is also supported.

5.7.2. TFT-LCD Interface

The GPL162004A supports TFT-LCD controller. The LCM interface including parallel RGB(5-6-5), serial delta RGB, serial stripe RGB, CPU (MPU) type, and CCIR601/CCIR656. The horizontal resolution of TFT controller maximum reaches 320

pixels, and the vertical resolution of TFT controller maximum reaches 240 pixels. The TFT controller mainly provides four timing control pins and 8 or 16 data pins to control external TFT panel. Those are VSYNC, HSYNC, DE, DCLK, and DATA.

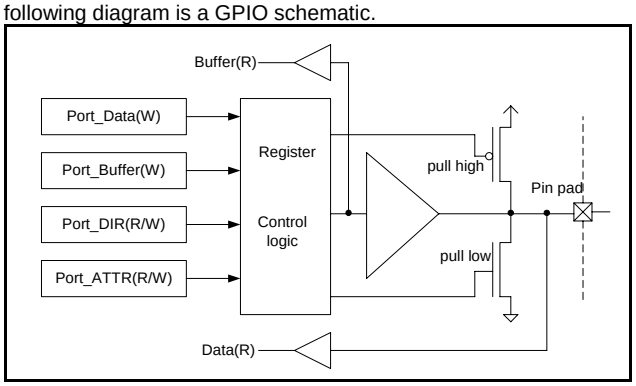
5.8. Interrupt

The GPL162004A has 28 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources. Some of the interrupt source can be programmed as FIQ or IRQ by register setting.

5.9. I/O

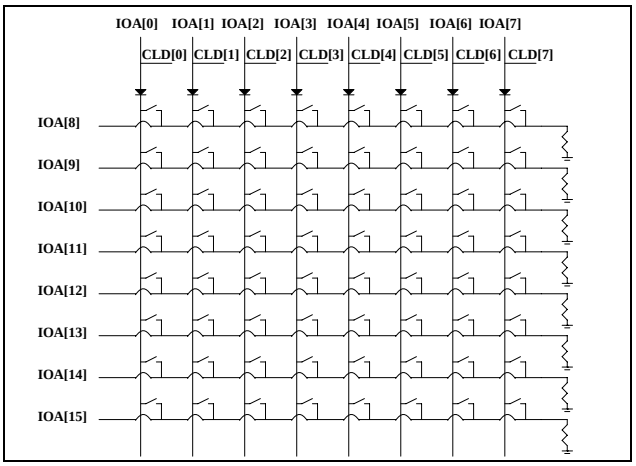
5.9.1. GPIO

Five I/O ports are built in GPL162004A, IOA, IOB, IOC, IOD and IOE. Each I/O pin has its normal function and is described in the signal description section. When the normal function of the I/O is disabled, it will switch to GPIO function automatically. The following diagram is a GPIO schematic.



5.9.2. Key Scan Function

The key scan function built-in GPL162004A is output at IOA[7:0] and input with IOA[15:8] under 64 keys mode. Additional 3 outputs IOC[2:0] are required under 88 keys mode. The keyscan controller also supports velocity detection when additional 8 inputs IOC[10:3] are used. The IOA[7:0] are shared with LCD data[7:0], which means the key scan function can still work even when LCD is on. But when 16-bit-data-bus TFT-LCD panel is connected, the key scan function can't work. It should be noted that when key scan function shared IOA with LCD panel, each output must connect a diode serially to the key pad to prevent the LCD glitch caused by contention when more than one keys are pressed at the same time. The following diagram shows an example of the connection.



5.10. Timer / Counter

The GPL162004A provides six 16-bit timers/counters, TimerA to TimerF. The clock source of each timer can be set individually. For Timer A to TimerD, an INT will be sent to CPU when timer overflow. Besides, Capture, Comparison and PWM functions are also provided by TimerA/TimerB/TimerC.

Clock Source A	Clock Source B
Fosc/2	2048Hz
Fosc/256	1024Hz
32768Hz	256Hz
8192Hz	Time Base B
4096Hz	Time Base A
1	0
Another Timer	1
INT1	INT2

The GPL162004A is embedded with a time base controller which is used to generate the slow and precisely interrupt form 32768Hz crystal. The following table shows the available time base.

TimeBase A	TimeBase B	TimeBase C
--	8Hz	128Hz
1Hz	16Hz	256Hz
2Hz	32Hz	512Hz
4Hz	64Hz	1024Hz

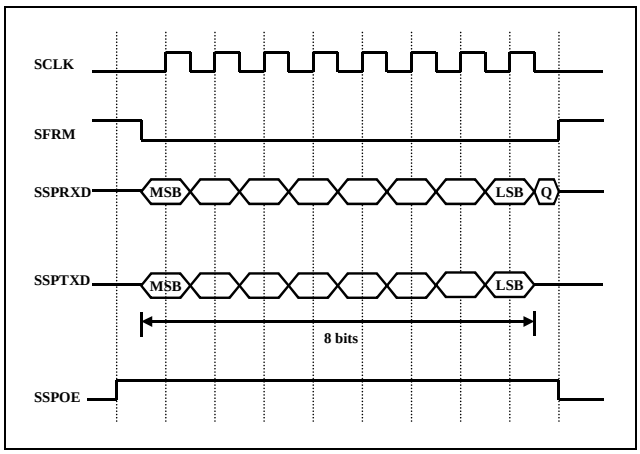
5.11. Watchdog

The purpose of watchdog is to monitor if the system operates normally. Within a certain period, watchdog must be cleared. If watchdog is not cleared, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again. In GPL162004A, the clear period is software programmable. If watchdog is cleared before expired, the system will not be reset.

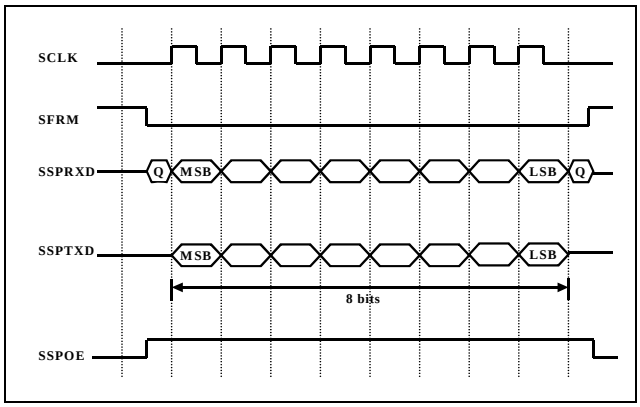
5.12. Serial Interface

5.12.1. Serial Peripheral Interface (SPI)

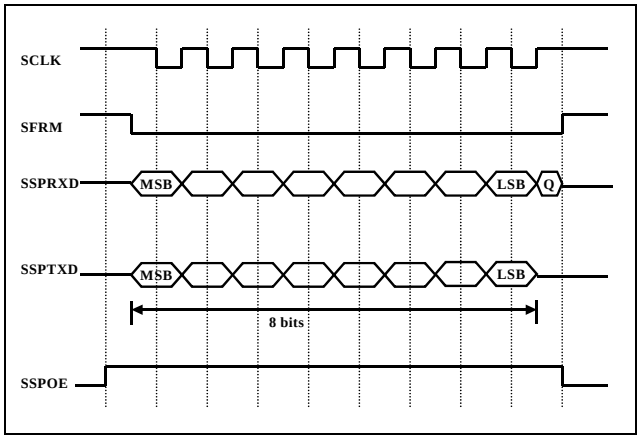
The SPI interface is a master/slave interface that enables synchronous serial communication with slave/master peripherals. Two 8 bytes FIFO are used for transmit and receive. Four types of timing are supported and showing in the following diagram.



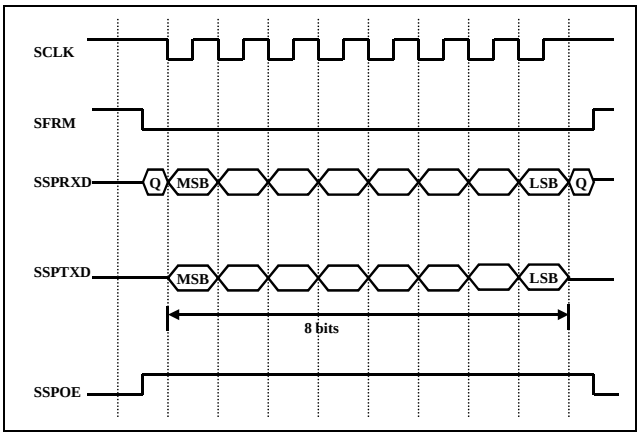
SPO = 0, SPH = 0, only this mode is supported in SPI slave mode.



SPO = 0, SPH = 1



SPO = 1, SPH = 0



SPO = 1, SPH = 1

5.12.2. UART/IrDA Function

GPL162004A provides a UART/IrDA controller with supported baud-rate up to 1.8432MHz(UART) when system running at 48MHz. When receive data, a 16-byte FIFO is used to prevent the data loss. When transmit data, a 16-byte FIFO is used. DMA transfer is available for both transmit and receive.

5.12.3. USB Mini-host/Device Function

GPL162004A provides both USB mini-host and device function which is compatible with USB 1.1 and USB 2.0 full speed standard. The mini-host and device function is not allowed to active at the same time. An USB transceiver is built-in for both host and devices function. A FIFO with size of 128x8 is used for bulk-in and bulk-out transfer and an 8-bytes FIFO is used for control pipe transfer. Interrupt IN/OUT and Isochronous IN/OUT pipes are also supported. The DMA transfer is enabled for bulk-in/out and ISO-in/out to maximize the transfer performance.

5.13. IDE Tools Function

The functions of IDE include the follows:
1). C compiler, Assembly and Linker
2). Single step trace
3). Break point (break point for debugging)
4). Run (execute)

5.14. SD/MMC Controller

GPL162004A provides two individual SD/MMC controllers which are compatible with MMC system specification version 2.3 and SD Memory Card specification 1.1. The controller supports automatically CRC generation and check, 1-bit and 4-bit transfer, interrupt generation when buffer empty/full, DMA transfer for page read/write.

5.15. Real Time Clock (RTC)

The RTC block provides the alarm function, schedule function, and hour/minute/second/half-second interrupt function.

5.16. Analog Control

5.16.1. DAC control

A 16-bit stereo DAC(2ch) is embedded in GPL162004A. For both left and right channel, a 16x16 FIFO is used to prevent the sound glitch when CPU is busy. The left and right channel does not need to have the same sample rate. A single DMA channel can utilize the stereo playback.

5.16.2. ADC control

A 12-bit ADC is embedded in GPL162004A for general purpose application. The ADC has five inputs which can be selected by software programming with maximum 100kHz sample rate for 5ch totally. The ADC also provides the microphone input function with hardware AGC supported.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	DVCC33 PLL_V33	-0.3 to 4.0	V
Supply Voltage 2	AVDD	-0.3 to 4.0	V
Supply Voltage 3	DVCC18 PLL_V18	-0.3 to 2.16	V
Input Voltage	V_{IN}	-0.3 to 4.0	V
Operating Temperature	T_A	0 to 70	℃
Storage Temperature	T_{STG}	-40 to +150	℃

6.2. DC Characteristics

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage 1	DVCC33 PLL_V33	2.7 3.0[1]	3.0	3.6	V	-
Operating Voltage 2	AVDD	2.7	3.0	3.3	V	-
Operating Voltage 3	DVCC18 PLL_V18	1.62	1.8	1.98	V	-
Operating Current	I_{OP}	-	60[2]	-	mA	@96MHz, 3.3V, all clocks on
Power Down Current	I_{PD}	-	40[3]	80[3]	μA	Sleep Mode@1.5V
High Input Voltage	V_{IH}	0.7DVDD33	-	DVDD33	V	-
Low Input Voltage	V_{IL}	VSS	-	0.8	V	-
Crystal Frequency 1	-	-	32768	-	Hz	-
Crystal Frequency 2	$F_{CRYSTAL}$	-	6.0[4]	-	MHz	-
System Clock	F_{SYS}	256Hz[5]	48	96	MHz	-

Note1: When USB function is enabled, the minimum voltage of DVCC33 is 3.0V.

Note2: Operating current depends on software code. In this test case, the following macro is turned on: Audio DAC, 96MHz PLL and 27MHz PLL.

Note3: Regulator is in sleep mode.

Note4: 6M Crystal is needed when USB function is enabled.

Note5: By setting clock divider and changing system clock to 32768 mode.

6.3. Audio DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	16	-	Bit	-
Full Scale Output Voltage	-	0.6*VDDDA	-	Vp-p	-
THD+N (f = 1kHz)	-	0.1	-	%	-
Noise at No Signal	-85	90	-	dBv	-
Frequency Response	20	-	19200	Hz	-

6.4. 12 Bits ADC Characteristics (VDD = 3.3V, T_A = 25℃)

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
ADC Power Dissipation	IADC	-	1.8	-	mA

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
ADC Input Voltage Range	VINL (Note1)	VSS - 0.3	-	VDD + 0.3	V
Resolution of ADC	RESO	-	-	12	bits
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note3)	-	56	-	dB
Effective Number of Bit	ENOB (Note4)	9.0	10	-	bits
Integral Non-Linearity of ADC	INL	-	±1.0	-	LSB (Note2)
Differential Non-Linearity of ADC	DNL (Note5)	-	±1.0	-	LSB
AD Conversion Rate	F_{CONV}	F_{CPU} / 2048	-	F_{CPU} / 256	Hz

Note1: Internal protection diodes clamp the analog input to VDD and VSS. These diodes allow the analog input to swing from (VSS - 0.3V) to (VDD + 0.3V) without causing damage to the devices.

Note2: LSB means Least Significant Bit (at 10 bits resolution). With VINL = 2.0V, 1LSB = 2.0V / 2^10 = 1.953mV.

Note3: The SINAD testing condition at VINLp-p = 0.8 * VDD, F_{CONV} = 100KHz, Fin = 1.0KHz Sine waves at VDD = 3.0V from the ADC input.

Note4: ENOB = (SINAD - 1.76) / 6.02.

Note5: This ADC can guarantee no missing code at 10 bits resolution.

6.5. Regulator Characteristics

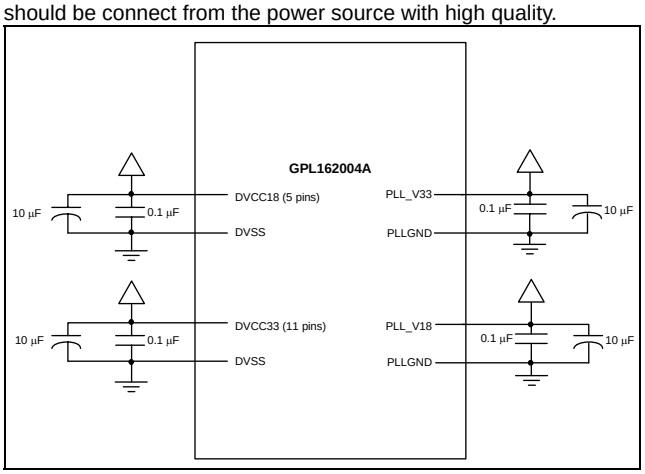
Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.7	3.0	3.6	V
Maximum Current Output	IREGO	-	70	100	mA
Output Voltage	VREGO	1.5[1]	1.8	1.89	V
Standby Current	IREGS	-	10	-	-

Note1: To save more power, it is recommended switching to 1.5V before entering the halt/sleep mode and switching to 1.8V in normal operation mode.

7. RECOMMENDED BOARD LAYOUT

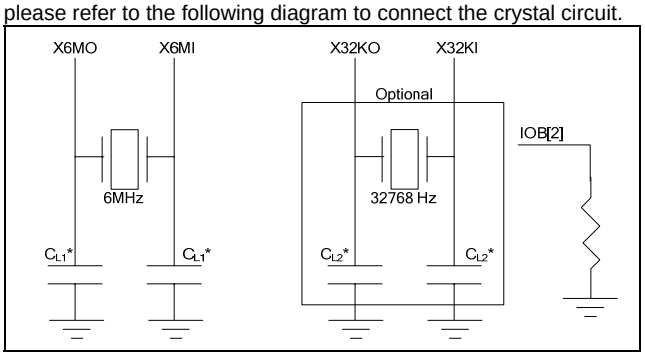
7.1. Power and Ground

All digital power and ground should be connected. The decoupling capacitor of 0.1μF and 10μF should be connected to each power pin of the IC as the following diagram. The power of analog parts should be connect from the power source with high quality.



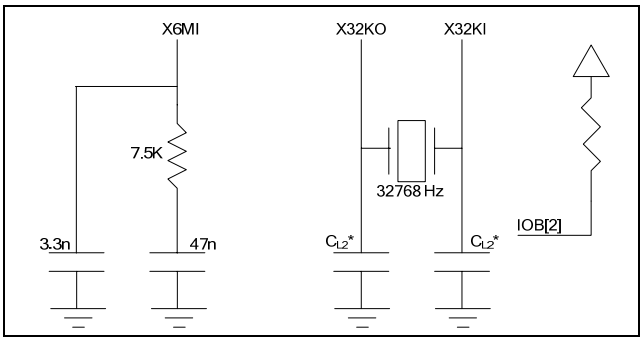
7.2. Crystal and PLL

When the 32768Hz crystal is disabled, usually for USB application, please refer to the following diagram to connect the crystal circuit.



Note*: Please refer to the crystal's application circuit.

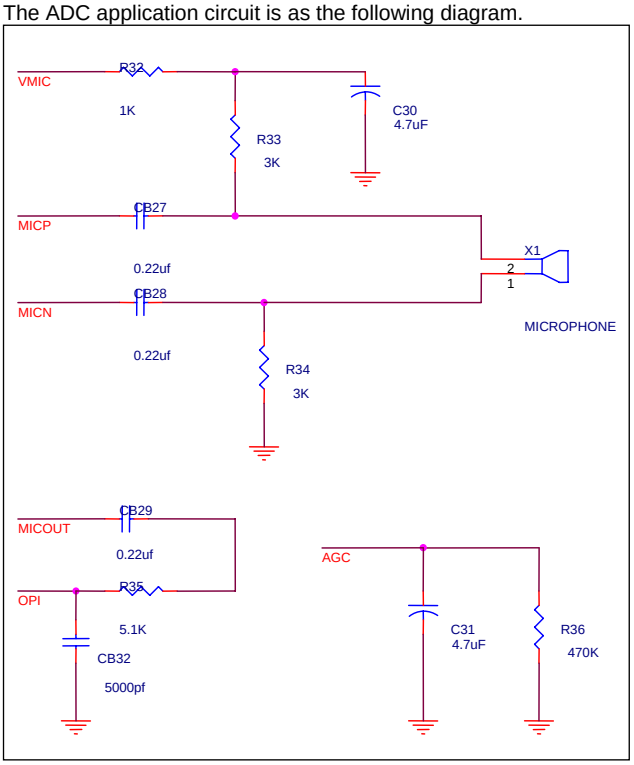
When the 6MHz crystal is disabled, please refer to the following diagram to connect the crystal circuit.



7.3. Analog Section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. DAVREF should be connected to a 1μF capacitor to ground.

The ADC application circuit is as the following diagram.



8. PACKAGE / ORDERING INFORMATION

8.1. Ordering Information

Product Number	Package Type
GPL162004A - NnnV - C	Chip Form
GPL162004A - NnnV - QL17x	Halogen Free Package

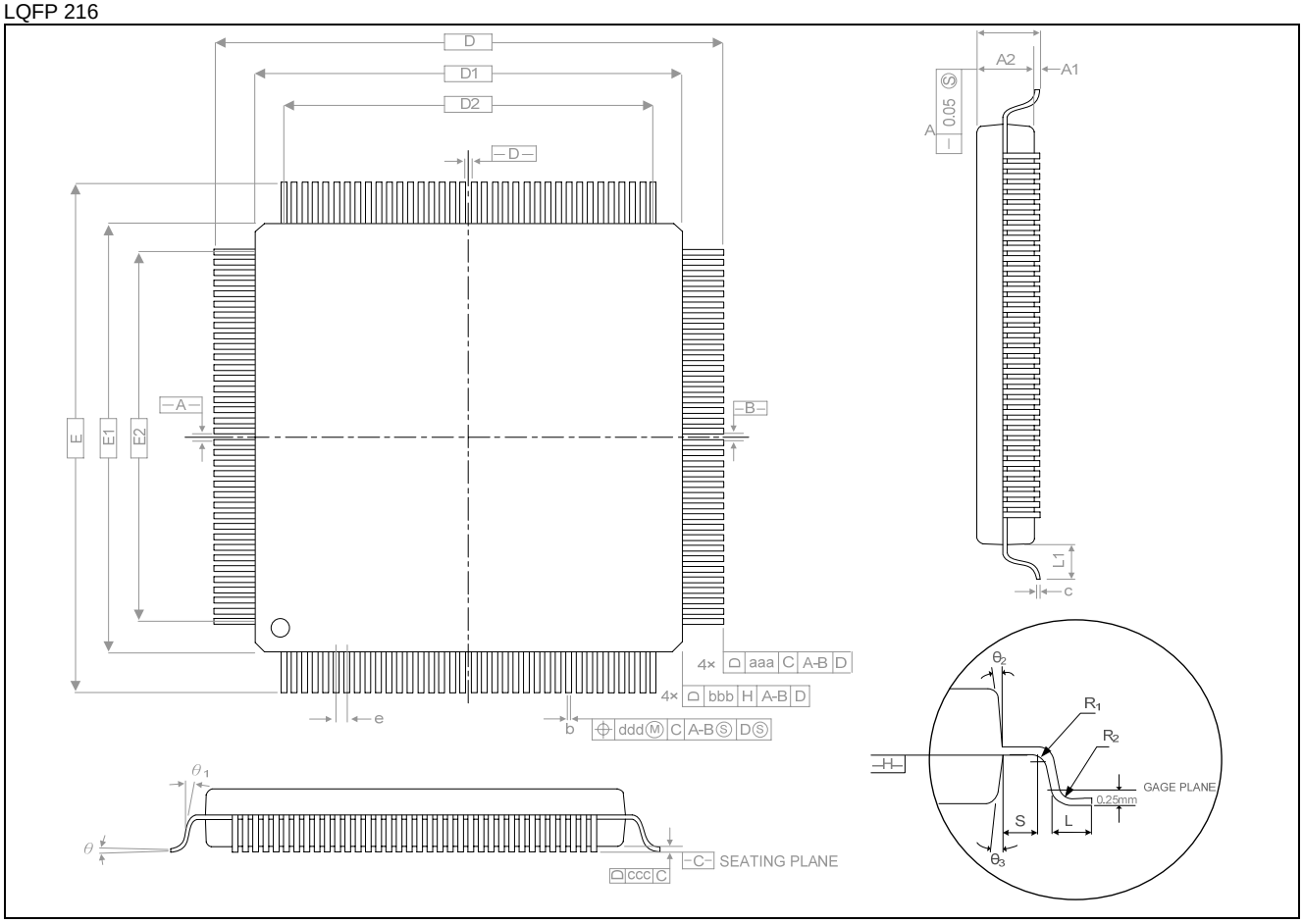
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

8.2. Package Information

LQFP 216



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	26.00 BCS.			1.024 BSC.		
D1	24.00 BCS.			0.945 BSC.		
E	26.00 BCS.			1.024 BSC.		
E1	24.00 BCS.			0.945 BSC.		
R2	0.08	-	0.20	0.003	-	0.008
R1	0.08	-	-	0.003	-	-

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
θ	0°	3.5°	7°	0°	3.5°	7°
$\theta 1$	0°	-	-	0°	-	-
$\theta 2$	11°	12°	13°	11°	12°	13°
$\theta 3$	11°	12°	13°	11°	12°	13°
c	0.09	-	0.20	0.004	-	0.008
L	0.45	0.80	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	-	-	0.008	-	-
b	0.13	0.16	0.23	0.005	0.006	0.009
E	0.40 BSC.			0.016 BSC.		
D2	21.20			0.835		
E2	21.2			0.835		
Tolerances of form and position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.07			0.003		
ddd	0.07			0.003		

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
Jun. 27, 2008	0.5	Modify test pin description.	6
Jun. 02, 2008	0.4	1. Modify regulator characteristic	16
		2. Modify ADC C30 to 4.7uF	17
Mar. 06, 2008	0.3	1. Modify standby current to 40uA(typ.) and 80uA(max.).	15
		2. Modify operating current to 60mA.	
		3. Modify ADC resolution to 12-bit.	
Oct. 22, 2007	0.2	1. Modify the “GENERAL DESCRIPTION” in section 1.	4
		2. Modify the “BLOCK DIAGRAM” in section 2.	4
		3. Modify the “FEATURES” in section 3.	4
		4. Modify the “SIGNAL DESCRIPTIONS” in section 4.	8
		5. Modify the “Analog Section” in section 7.3.	17
Sep. 27, 2007	0.1	Preliminary version.	21