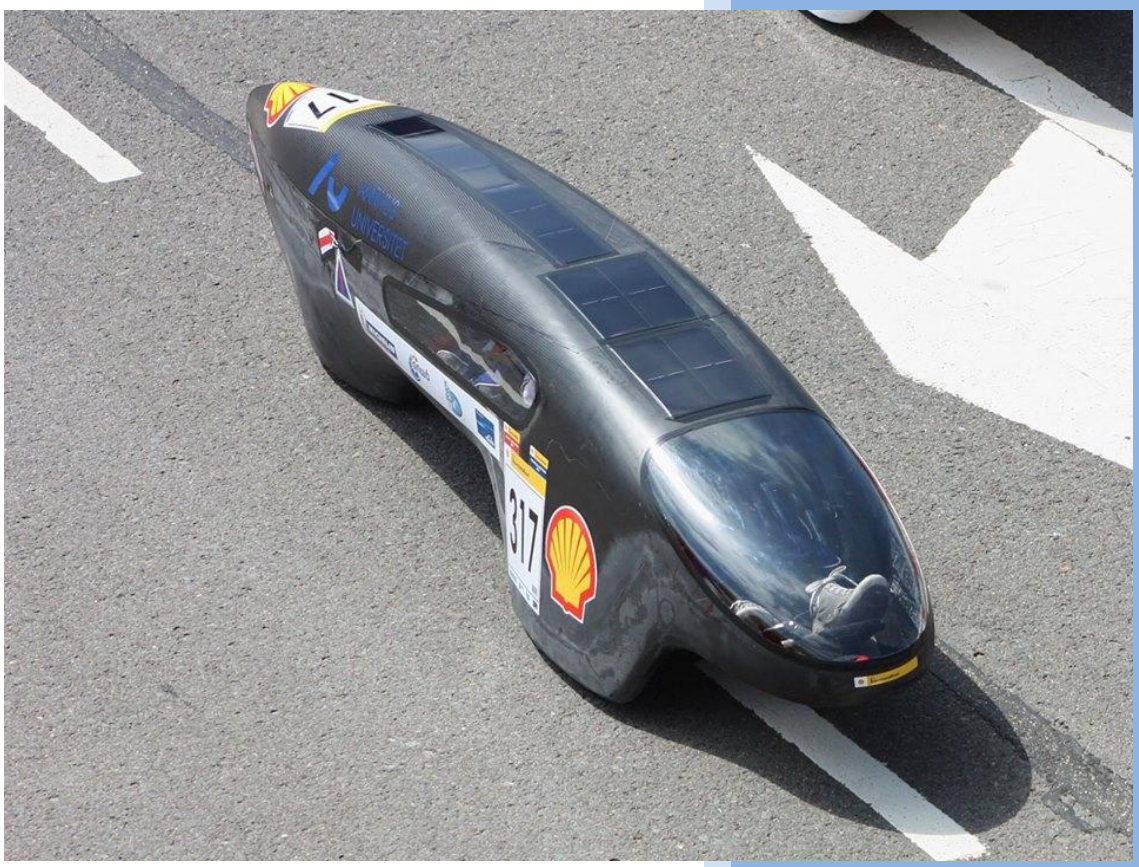
Project Documentation

2013

# Propulsion Battery and Battery Management System

*- for Shell Eco-marathon 2013*

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# FOREWORD

This document contains documentation of a propulsion battery and Battery Management System tailored for Shell Eco-marathon 2013. These are specified in a sequential manner, starting at Specification Requirements, elaborated by a System Architecture, and subsequently implemented with description of design and chosen solutions. In addition, system tests are included in this document.

# CONTENTS

# 1. SPECIFICATION REQUIREMENTS

## 1.1. Version History

**Version 1, date: 09-02-2013**

**Version 2, date: 16-02-2013**
System Description modified, figure 1 modified, battery voltage changed to 24V on request from AU Herning, Communication protocols added.
**Version 3, date: 03-03-2013**
System Description improved after advice from external review. Requirements: PB_F.2, PB_F.3, BMS_F.6, PB_NF.3 and BMS_NF.7 clarified.
**Version 4, date: 21-05-2013**
Mechanical and documentation requirements, added to System Description. Requirements: PB_NF.5, PB_NF.6, BMS_NF.8, BMS_NF.9, BMS_NF.10 added.

## 1.2. Introduction

This document outlines the system to be designed, and associated specification requirements. Basic system requirements have been driven by Shell Eco-marathon official rules 2013 and interfacing agreements with other parties involved[1]. In addition, some extended battery cell surveillance features, described later in this document, has been included to increase safety and to impose the possibility of performance analysis.

[1] AU Herning (project groups working on related Shell Eco-marathon projects)

# 1.3. System Description

This project emanates from the participation in Shell Eco-marathon, a competition on energy efficiency of a small vehicle carrying one person. The vehicle to be constructed, will be a light electric vehicle, with photovoltaic cells and an off track charger as power source. An onboard Lithium-Ion battery pack with high energy density will serve as energy storage, which imposes the need of a Battery Management System (BMS), to ensure that the battery is kept within its Safe Operation Area (SOA), and to ensure optimum lifespan.

A project description outlining general electric drive train requirements[2] was framed by Aarhus college of engineering, and is underlying basis for the project specified in this specification requirement.

A simple BMS comparing cell voltage, temperature and current to allowable upper and lower threshold levels would fulfill the requirements given by the Shell Eco-marathon committee. However, a more sophisticated digital BMS performing measurements at cell level, and presenting these, will allow detailed analysis of battery performance, and point out cells with unsatisfying performance. Therefore, the sophisticated digital approach has been selected for this project.

As a number of cells will be connected in series, the battery pack performance will be limited by the performance of the weakest cell. Therefore the system to be designed must present individual cell parameters, along with battery parameters. Real time data must be accessible through a CAN interface, while logged data shall be available via USB.

While most features of the BMS to be designed are supported by some off-the-shelf battery management systems, designed for electric vehicles with large cell count, such systems are often large in size, heavy and unnecessarily power consuming for small systems. Designing a small but full featured centralized BMS for a moderate number of cells, will not only be beneficial for Shell Eco-marathon. It can potentially lead to more sustainable battery systems for electric bicycles, mowers etc. as a defective cell can be discovered and replaced as an alternative to disposal of the entire battery pack.

Besides advanced features, like estimation of State Of Charge (SOC), State Of Health (SOH) and interfacing to external vehicle units. The BMS must perform primary and redundant protection, by monitoring cell voltages, cell temperatures and battery current and autonomously isolate the battery from its load, in case any parameter exceeds SOA.

The Battery Pack to be designed must be as light as possible, certain high energy density battery chemistries do however pose a higher fire hazard. Therefore a balance between density and safety must be found.

As the BMS and battery are to be used for Shell Eco-marathon 2013, a functional system must be prepared before participation, this includes fabrication of all PCB's, mechanical assembly of the system and mounting within the vehicle. Furthermore, to ensure the possibility of on-site repairs, back-up replacement modules, including extra PCB's, batteries, plugs etc., must be made. To ensure approval of the system, technical documentation, fulfilling Shell Eco-marathon requirements must be prepared.

[2] See "12105 Shell eco marathon" in appendices

### 1.3.1. System Outline

The system to be designed, including external units with relevance to the specification requirements, has been outlined in Figure 1. The cell count is for illustration only. Furthermore, only main functionalities have been included.

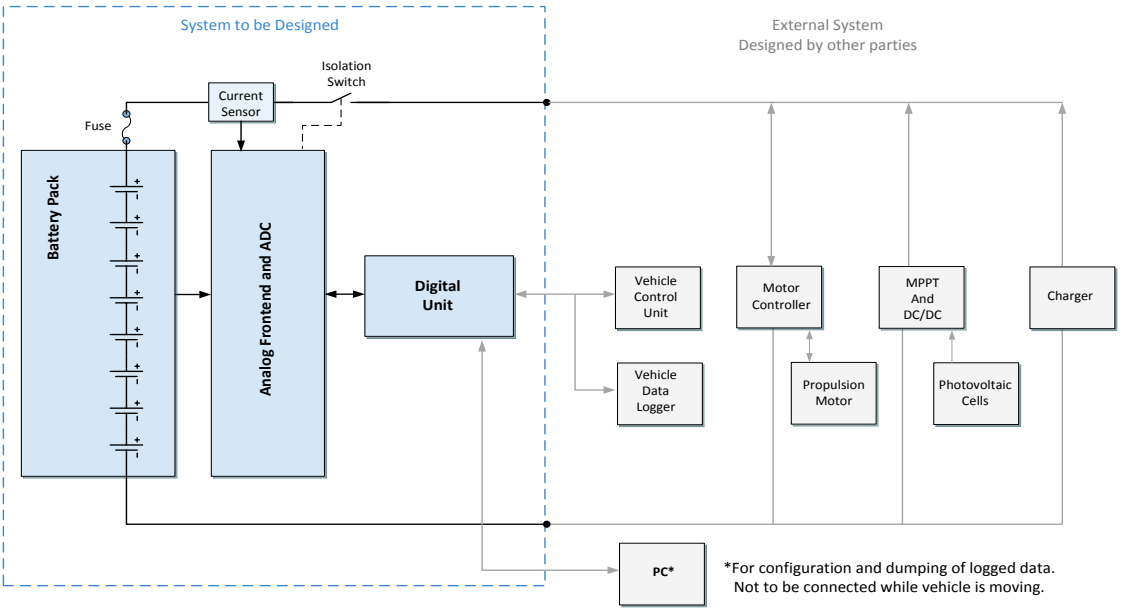



*Figure 1 - Draft of Battery Pack and BMS*

## 1.4. System Delimitation

As the duration of this project does not allow comprehensive research and design optimizing of all involved hardware units and software, the system will be delimited to certain main focus points, while other system parts will be briefly described. Below a list of delimitations:

- Off track charger will not be implemented, as a CC-CV (Constant Current - Constant Voltage) charging profile can be accomplished using a laboratory power supply.
- Analog Front End will be based on a number of ASIC's in order to reduce power consumption and time to market. As achieving lower power consumption with a custom designed Front End, within the given timeframe, is predicted to be unrealistic.
- PC software for analysis of data readout from the BMS may be briefly described, but not fully implemented.

# 1.5. Requirements

As described in the pre-project[3] the system has to fulfill certain mandatory requirements to qualify for participation in Shell Eco-marathon. Furthermore the Interfacing to external units and the desire to design a system with extended battery cell surveillance, entails certain requirement.

The tentative list of requirements, specified in the pre-project, has been summed up and refined, resulting in the functional and non-functional requirement, described in section 1.5.1 and 1.5.2

To ease the use of references to specific requirements, these are given a specific requirement number.

## 1.5.1. Functional requirements

### 1.5.1.1. Propulsion Battery

| Req. # | Requirement description |
|---|---|
| PB_F.1 | The propulsion battery must be short circuit protected by a fuse located on the positive conductor, as close to the battery as possible. Furthermore the fuse must be rated so that the battery is able to deliver enough short circuit current to open the fuse at all times. |
| PB_F.2 | The propulsion battery must safely be able to withstand a continuous discharge current of 25A and a temporary max. current of 50A for 10 seconds. |
| PB_F.3 | The propulsion battery must accept a constant charging current of max. 15A. |

*Table 1 - Functional requirements for Propulsion Battery*

### 1.5.1.2. Battery Management System

| Req. # | Requirement description |
|---|---|
| BMS_F.1 | The BMS must, at all times, be able to isolate the battery from all external circuitry except the BMS, if any of the limits listed below is exceeded:<br>• Undervoltage limit (monitored at cell level)<br>• Overvoltage limit (monitored at cell level)<br>• Overcurrent limit (load and charge current)<br>• Overtemperature limit (monitored at battery level) |
| BMS_F.2 | The BMS must be able to monitor from 6 to at least 16 cells. Changes in number of connected cells may require connection of extension modules and minor SW and HW adjustments. SW values that are cell count dependant must be implemented using definitions assembled in one location, to allow easy modification. |
| BMS_F.3 | In case of microcontroller failure or loss of communication with Analog Front End, the Analog Front End must perform autonomous protection of cells against under- and overvoltage, and perform isolation of battery if limits are exceeded. |
| BMS_F.4 | Maintenance cell balancing[4] must be performed by the BMS doing charge, to equalize SOC, and thereby compensate for (cell to cell) differences in self discharge currents. As cells SOC will be in |

[3] See "Pre-Project BMS and Propulsion Battery" in appendices

| | |
|---|---|
| | balance at initial connection to the BMS, gross balancing capability is not needed. |
| BMS_F.5 | Following data must be stored in internal memory, once per minute, for later readout via USB port or SD card:<br>• Individual cell voltages (averaged over a period of 1 minute)<br>• battery current (averaged over a period of 1 minute)<br>• battery temperature(s) (averaged over a period of 1 minute)<br>• battery SOC (at time of saving)<br>• battery SOH (at time of saving)<br>• Error information<br>Capacity of internal memory must hold data history of min. 10 hours |
| BMS_F.6 | The BMS must be able to estimate SOC and internal resistance. |
| BMS_F.7 | If the internal resistance of any cell exceeds (averaged internal resistance x 2) an error message* must be transmitted on the CAN bus, to reveal poor cell performance.<br>* See CAN protocol DTC (5) for further details. |
| BMS_F.8 | The actual battery and cell status must be transmitted on the CAN bus according to CAN protocol. See CAN protocol for further details. |
| BMS_F.9 | The BMS must be able to enter a low power mode consuming less than 100mW if a undervoltage failure occurs. Low power mode will be entered after isolating the battery, so all protection functionalities may be deactivated. A pushbutton (or similar) must be available to resume normal BMS activity. |
| BMS_F.10 | After the occurrence of an undervoltage error, the BMS must sense the connection of a charger and re-close the isolation switch, and thereby enable charging. |

*Table 2 - Functional requirements for BMS*

## 1.5.2. Non-functional requirements

### 1.5.2.1. Propulsion Battery

| Req. # | Requirement description |
|---|---|
| PB_NF.1 | The propulsion battery must consist of a number of Lithium-Ion cells, leading to a nominal battery voltage within the range of 22 - 26 Volts. |
| PB_NF.2 | All battery cells must be contained in one battery unit, as only one propulsion battery per vehicle is allowed. |
| PB_NF.3 | The effective capacity* must be greater than or equal to 70Wh.<br>*Capacity available at 100W load and ambient temperature of 8°C[5]. |
| PB_NF.4 | The propulsion battery must be electrically isolated from the vehicle frame and the accessory battery circuit. |
| PB_NF.5 | Technical documentation fulfilling Article 58 of Shell Eco-marathon official rules[6] must be prepared before participation. |

[4] For details see: http://liionbms.com/php/wp_balance_current.php (date: 07-02-2013)
[5] Based on average low temperature for Rotterdam in May, See: http://weatherspark.com/averages/28810/5/Rotterdam-Zuid-Holland-The-Netherlands (date: 02-02-2013)
[6] See " sem_rules_chapter01_2013" in appendices

| | |
|---|---|
| PB_NF.6 | Min. 2 batteries must be available, to ensure the possibility of battery replacement between races. |

*Table 3 - Non-functional requirements for Propulsion Battery*

## 1.5.2.2. Battery Management System

| Req. # | Requirement description |
|---|---|
| BMS_NF.1 | Limits listed in BMS_F.1 must be kept within specifications of chosen cell type. |
| BMS_NF.2 | Types of measurements performed by the BMS, including measurement ranges and accuracy:<br>Cell voltage: 2V to 4.5V (accuracy +/- 4mV @ 24°C)<br>Battery temperature: -20°C to 100°C (accuracy +/- 3°C)<br>Battery current: -15A to 60A (accuracy +/- 100mA) |
| BMS_NF.3 | Cell balancing current min. 75mA[7] |
| BMS_NF.4 | Operational within Industrial Temperature range -40°C to 85°C |
| BMS_NF.5 | COM port communication must be implemented according to RS-232 (ISO IS2110) standard, or as virtual COM port with female Mini USB plug. |
| BMS_NF.6 | Average power consumption must be kept below 1.5W while all BMS functionalities are active. (consumption of isolation switch not included) |
| BMS_NF.7 | Isolation switch must safely carry a continues current of 25A. And a max. current of 50A for 10 seconds. Furthermore it must be able to interrupt a current of 75A. |
| BMS_NF.8 | Technical documentation fulfilling Article 58 of Shell Eco-marathon official rules[8] must be prepared before participation. |
| BMS_NF.9 | The system must be mounted in a cabinet fulfilling Article 57-m of Shell Eco-marathon official rules[7]. |
| BMS_NF.10 | All PCBs, plugs, fuses etc. must be backed-up by replacement units to allow on-site repair. |

*Table 4 - Non-functional requirements for BMS*

[7] Derived from rules specified in: http://liionbms.com/php/wp_balance_current.php (date: 07-02-2013)
[8] See " sem_rules_chapter01_2013" in appendices

## 1.5.3. Communication Protocols

### 1.5.3.1. CAN communication protocol

While a CAN protocol based on CANopen CiA 301 and CiA 418 standards, might be the best choice for a commercial product, as it will allow communication with chargers featuring CiA 419 communication protocol, which most likely will be the de facto standard of the future. A more simple protocol will be sufficient for this project, and ease the implementation. Therefore the Standard Traction Pack Messages has been chosen, this protocol is being used by elithion and claimed to be supported by a number of chargers.

The Original Standard Traction Pack messages can be found at:
http://liionbms.com/php/standards.php

The protocol tailored for this project can be seen below:

- CAN communication bit rate: 125 Kbit/s
- Standard addressing (CAN 2.0 A) (not extended)
- Period between data transmission: 1 second
- Multi-byte values are big-endian

| ID | Bytes | Byte 0 | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Byte 7 |
|---|---|---|---|---|---|---|---|---|---|
| 620h | 8 | Company name (1) | | | | | | | |
| 621h | 8 | Product name / rev level (1) | | | | | | | |
| 622h | 6 | State (2) | Timer (3) | | Flags (4) | DTC (5) | DTC (5) | - | |
| 623h | 6 | Voltage (6) | | Min Vtg (7) | Min Vtg # (8) | Max vtg (7) | Max Vtg # (8) | - | |
| 624h | 6 | Current (9) | | Charge limit (10) | | Discharge limit (10) | | - | |
| 625h | 8 | Batt. energy in (11) | | | | Batt. energy out (11) | | | |
| 626h | 7 | SOC (12) | DOD (13) | | Capacity (14) | | SOC2 (15) | SOH (16) | - |
| 627h | 6 | Temperature (17) | Air temper. (17) | Min tmp (18) | Min tmp # (8) | Max tmp (18) | Max tmp # (8) | - | |
| 628h | 6 | Resistance (19) | | Min res (20) | Min res# (8) | Max res (20) | Max res# (8) | - | |

*Table 5 - CAN protocol*

1. 8 ASCII characters ID620h = "IHA BMS1" and ID621h = "SW: X.XX" (X.XX = numbers indicating SW version)
2. State of Propulsion battery system
    0. Fault

    1. Charger connected, Isolation Switch closed
    2. Vehicle ON, Isolation Switch closed
    3. Vehicle OFF, Isolation Switch closed
    4. Vehicle OFF, Isolation Switch open
3. Power up time [s]; after 65535 s, it overflows back to 0
4. Byte of flags (0,3-7 for future use)
    1. Battery is being charged
    2. Battery is being discharged
5. Error codes
    1. Sign of poor cell performance
    2. Sign of poor battery performance
    3. Battery temperature too low for charging
6. Total voltage of pack [V], unsigned, 0 to 65 kV
7. Voltages [100 mV] of least charged and most charged cells or blocks of cells, 0 to 25.5 V
8. ID of the cell that has the lowest / highest voltage / temperature / resistance. 0 or 1 to 254
9. Pack current [A], signed, positive out of pack, -32kA to + 32kA
10. Maximum current acceptable (charge) or available (discharge), unsigned, 0 to + 32kA
11. Total energy in or out of battery, since manufacture. Unsigned, overflows back to 0 [WH]
12. State Of Charge [%], unsigned, 0 to 100. When deeply discharged, its value does not go below 0
13. Depth Of Discharge [AH], unsigned, 0 to 65 kAH. When deeply discharged, its value may exceed the actual capacity's value
14. Actual capacity of pack [AH], unsigned, 0 to 65 kAH
15. State Of Charge of 2nd pack (such as the vehicle's original pack) [%], unsigned, 0 to 100. When deeply discharged, its value does not go below 0 (FFh will be send as no secondary battery is connected)
16. State Of Health [%], unsigned, 0 to 100. 100 % = all OK. Actual operation defined by the manufacturer.
17. Average pack temperature, and Air intake temperature [°C], signed, -127 °C to +127 °C
18. Temperatures [°C] of coldest and hottest sensors, signed, -127 °C to +127 °C
19. Resistance of pack [mohm], unsigned, 0 to 65 ohm
20. Resistances [100 micro-ohm] of lowest and highest resistance cells (or block of cells), unsigned, 0 to 25.5 milliohm

Note:

- If a value is not available, set to an invalid number:
    - 80h for 1-byte, signed variables
    - FFh for 1-byte, unsigned variables
    - 8000h for 2-byte, signed variables
    - FFFFh for 2-byte, unsigned variables

### 1.5.3.2. RS232 communication protocol

The COM port or virtual COM port(USB) shall allow the system administrator to dump logged data on a PC using a simple RS232 terminal program.

- RS232 baudrate: 38400 Kbit/s

| Operation | ASCII string to be send from PC | Confirmation send to PC |
|---|---|---|
| Set cell count | CellC:xx (xx = number of connected cells)<br>Ex.: if 12 cells are connected following string should be send: CellC:12 | ASCII string: New Cell Count:xx |
| Request logged data | LogReq | Logged data is being sent. If log is empty, following ASCII string will be send: Log is empty |

*Table 6 - RS232 protocol*

# 2. SYSTEM ARCHITECTURE

## 2.1. Version History

**Version 1, date: 11-03-2013**

**Version 2, date: 10-03-2013**

Software flow chart simplified.

## 2.2. Introduction

This document describes the System Architecture of the project "Battery Management System and Propulsion Battery". The purpose of the System Architecture is to elaborate system blocks, of the system described and specified in the "Specification Requirements", to a level allowing subsequent implementation.

As the specifications of the selected ASIC for the Analog Front End to be designed, will influence considerably on interfaces towards other system units, the selection of an appropriate ASIC has been made prior to the definition of interfaces. This has allowed a more thorough elaboration of all system units with Analog Front End dependencies.

The system outlined in the specification requirements will be described at system block level, and following be grouped in battery, hardware(HW) and software(SW) units for which internal interfaces, functionalities and requirements will be clarified.

## 2.3. Overview of System Blocks

Figure 2 shows the general block diagram, extracted from the system outline in Figure 1. The function of each unit is briefly described below.

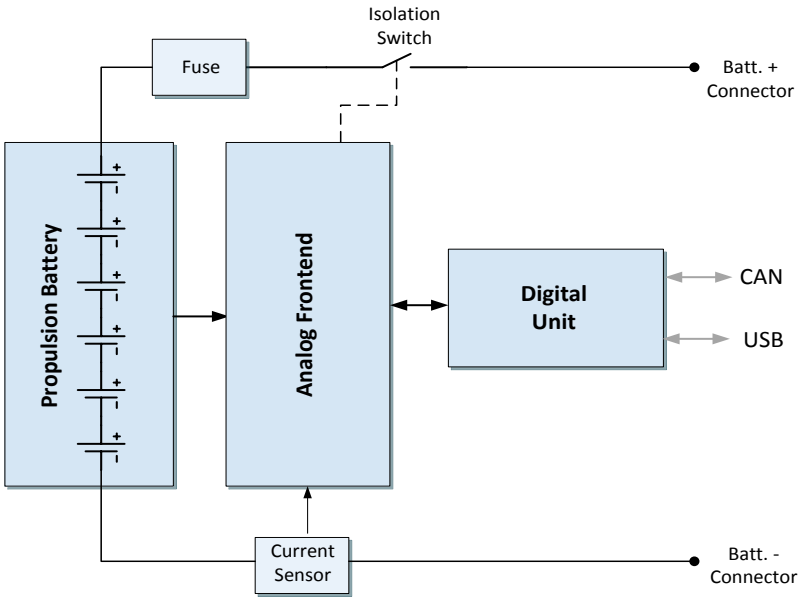



*Figure 2 - General Block Diagram*

**Propulsion Battery:** This unit, consisting of a number of battery cells, is responsible for storage of electrical energy. It must be able to capture energy from an external charger, solar panels and regenerative braking. And capable of delivering the current needed to propel the propulsion motor.

**Analog Front End:** This unit performs measurements and analog to digital conversion of cell voltages, battery temperatures and signal from current sensor. Furthermore, it handles cell balancing on request from the digital unit, and redundant battery protection independent of the digital unit.

**Current Sensor:** Senses value and direction of battery current, and present this for the Analog Front End.

**Isolation Switch:** This unit enables the BMS to interrupt the battery current (when the Safe Operation Area(SOA) is exceeded).

**Digital Unit:** Collects measured values from the Analog Front End and perform calculations and estimations of cell and battery parameters specified in the specification requirements. Furthermore it handles communication with external units.

# 2.4. Elaborated System Block Descriptions and Interfacing

System Blocks to be implemented are visualized in Figure 3. Sub blocks (written in Italic), outlines functionalities within the block. Functionality descriptions and design requirements for illustrated blocks are described below.

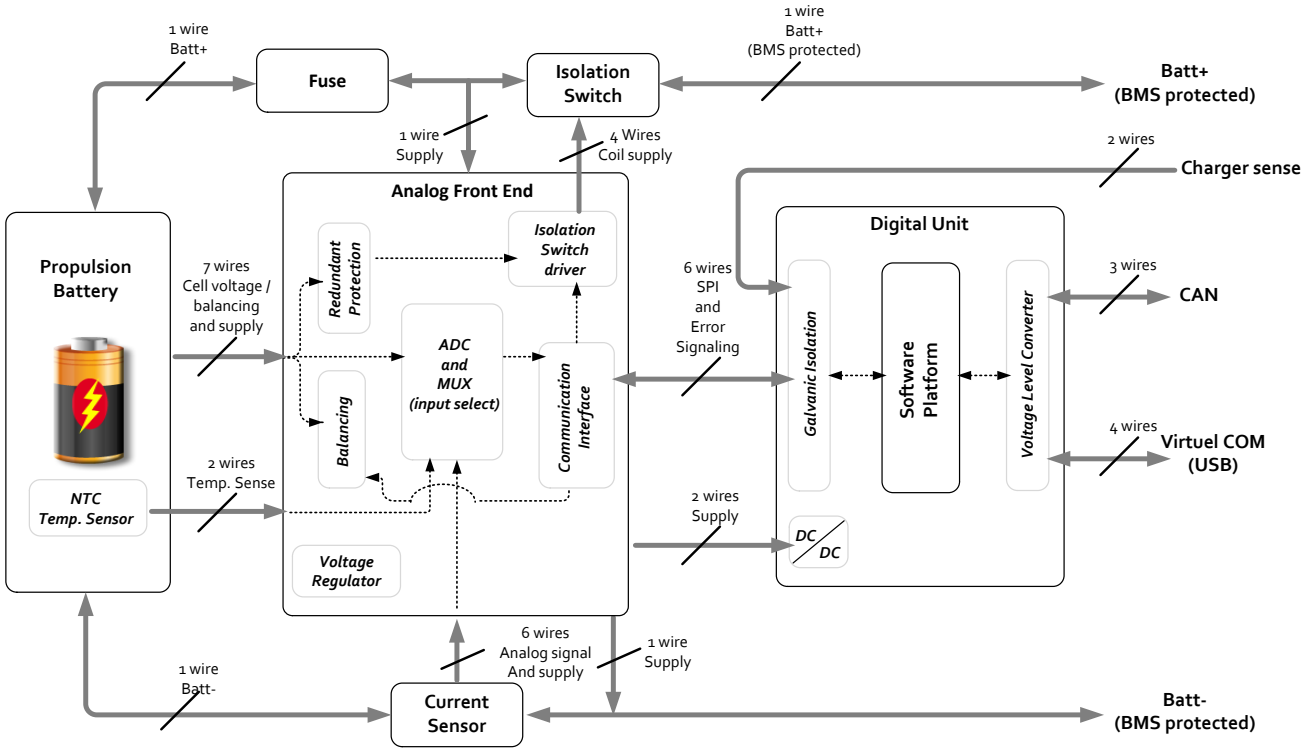



*Figure 3 - Elaborated system and interfacing Diagram*

## 2.4.1. Elaborated Battery Block Details

### 2.4.1.1. Propulsion Battery

**IPO(Input, Process, Output)**

Table below describes Input, process and output for Propulsion Battery.

| Input | Process | Output |
|---|---|---|
| Charging Current ,<br>Charging profile: CC-CV | Storage of electrical energy. | Propulsion Current |

*Table 7 – IPO for Propulsion Battery*

**Design requirements:** The Battery Pack is to be build from 6 to 8 Lithium-ion cells leading to a nominal battery voltage of 22 to 24V.

A fuse of suitable rated current and high(>2KA) breaking capacity[9] is to be inserted in the positive conductor.

To allow battery temperature monitoring a NTC of type, 10KΩ at 25°C (1%), Panasonic ERT-J1VG103FA or equivalent, must be mounted on the battery.

Connections and devices to be contained in the propulsion battery has been illustrated in Figure 4.

**Note:** A choice of one particular Lithium Iron Phosphate (LFP)[10] cell and one Li-ion polymer[11] cell has been pointed out based on their high power density. However thermal performance, energy density and safety is to be compared, to find most appropriate cell chemistry.

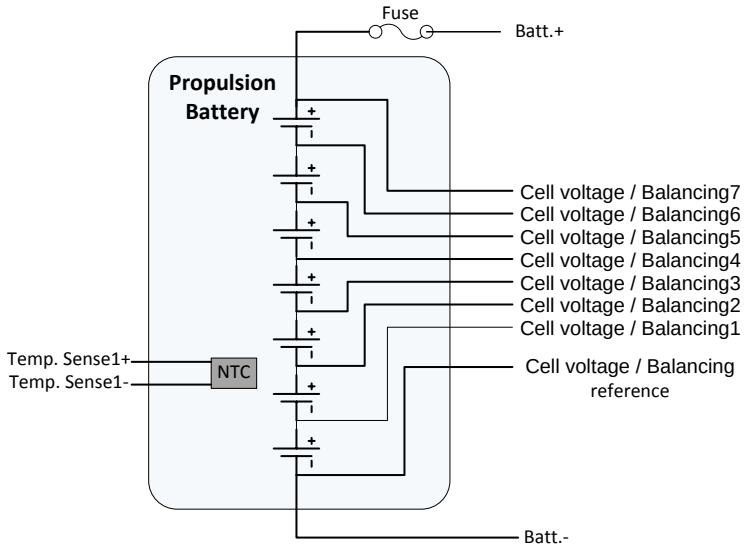



*Figure 4 - Propulsion Battery Connections*

[9] As the internal resistance of the battery is low, and the battery is able to deliver a very high peak current
[10] Turnigy nano-tech 3000mAh 2S1P 20~40C LiFePo4
[11] Turnigy nano-tech 3000mAh 2S2P 20~40C Lipo

**Table of In-/Output Requirements**

Table below specifies requirements for input and output connections of Propulsion Battery.

| Connector Name | Direction | Voltage | Current | Remarks |
|---|---|---|---|---|
| **Battery Pack Terminals** | | | | |
| Batt+ | IN / OUT | 17.5 to 30V | -15 to 50A | Fuse protected |
| Batt- | IN / OUT | 0V | -15 to 50A | |
| **Connections to Analog Front End and ADC** | | | | |
| Cell voltage / Balancing (#1 to 7 or 8) | OUT | 0 to 4.8V[3] | 0 to 150mA (Balancing current) | Same wires used for cell surveillance, balancing and Front End ASIC supply # of wires = cell count |
| Cell voltage / Balancing reference | OUT | 0V | | Negative terminal of lowest cell in stack |
| Temp. Sense+ (#1 to 5) | OUT | | | NTC's of type: 10KΩ at 25°C (1%), Panasonic ERT-J1VG103FA or equivalent |
| Temp. Sense- (#1 to 5) | OUT | | | |

*Table 8 - Connections and Signal Levels for Propulsion Battery*

## 2.4.2. Elaborated Hardware Block Details

### 2.4.2.1. Analog Front End

**IPO(Input, Process, Output)**

Table below describes Input, process and output for Analog Front End.

| Input | Process | Output |
|---|---|---|
| Data requests from Digital Unit. | Acquire and convert cell voltages, battery temperatures and current sensor signal to digital form. And send values to Digital Unit on request. Performs Balancing on request from Digital Unit. Survey cell voltages and autonomously isolate battery if SOA is exceeded. Drive Isolation Switch. | Measured and digitalized measurement data |
| Cell voltage / Balancing current | | |
| Current sensor signal | | |
| Cell temperature signal | | Isolation Switch open/close signal |
| Balancing requests from Digital Unit | | |
| Isolation Switch command from Digital Unit | | |

*Table 9 – IPO for Analog Front End*

**Design requirements:** As described in The Specification Requirements an ASIC with lowest possible power consumption must be selected. The bq76PL536A, from Texas Instruments, has been selected as it offers the possibility to stack a number of ICs, to achieve support of a scalable number of cells. Furthermore its quiescent current is low and it offers secondary protection and high precision voltage measurements. The Analog Front End and ADC to be designed must therefore be based on the bq76PL536A, and contain inputs and outputs as specified in the table below. Furthermore, the communication with the Digital Unit must fulfill the protocol defined in the bq76PL536A datasheet[12].

Functionalities to be implemented, not contained in bq76PL536A:

**Balancing:** External switches and dissipative elements (bleeder resistors), must be interfaced with bq76PL536A.

**Isolation Switch driver:** Open collector output for Isolation Switch to be driven from GPIO of bq76PL536A.

**Sensor interfacing:** All circuitry necessary for interfacing between bq76PL536A and sensor in-/outputs specified in Table 10, is to be implemented.

**Table of In-/Output Requirements**

Table below specifies requirements for input and output connections of Analog Front End.

| Connector Name | Direction | Voltage | Current sink | Current source | Input resistance | Remarks |
|---|---|---|---|---|---|---|
| **Connections to Digital Unit** | | | | | | |
| SCLK | IN | 5V logic[1] | | | 5KΩ min. | SPI interface |
| MOSI | IN | 5V logic[1] | | | 5KΩ min. | |
| MISO | OUT | 5V logic[2] | 1mA min. | 1mA min. | | |
| SS | IN | 5V logic[1] | | | 5KΩ min. | |
| Convert | IN | 5V logic[1] | | | 5KΩ min. | Starts ADC conversion |
| Fault | OUT | 5V logic[2] | 1mA min. | 1mA min. | | Reports errors |
| $DGND_{Batt}$ | | 0V | | | | Digital battery ground |
| Aux Vdd out | OUT | 17.5 to 60V | | 50mA min. | | Supply for Digital Unit. |
| Aux Vss out | | 0V | | | | Voltage depends on number of connected cells |
| **Connections to Isolation Switch** | | | | | | |
| Coil + | OUT | 17.5 to 60V | | 200mA min. | | Voltage depends on |

[12] See "bq76PL536A - Battery monitor and secondary protection" in appendices

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | | | number of connected cells |
| Coil - | OUT | 0 to 60V | 200mA min. | | | Open collector output |
| **Connections to Propulsion Battery** | | | | | | |
| Cell voltage / Balancing (#1 to 16) | IN | 0 to 4.8V[3] | 75mA min. (Balancing current) | | 1MΩ min. (balancing off) | Same wires used for cell surveillance, balancing and Front End ASIC supply # of wires = cell count |
| Cell voltage / Balancing reference | IN | 0 V | | | | Negative terminal of lowest cell in stack, is connected to this input. |
| Temp. Sense+ (#1 to 6) | IN | | | | | To be configured for use with NTC's of type: 10KΩ at 25°C (1%), Panasonic ERT-J1VG103FA or similar |
| Temp. Sense- (#1 to 6) | IN | | | | | |
| AUX Vdd in | IN | 17.5 to 60V | | | 480Ω min. | Directly feed to AUX out connector |
| AUX Vss in | | 0V | | | | |
| **Connections to Current Sensor** | | | | | | |
| Current Sensor Vdd | OUT | 5V +/-0.1V | | 1mA min. | | Sensor supply |
| Discharge current signal | IN | 0 to 2.5V | | | 25KΩ min. | Sensor signal |
| Charge current signal | IN | 0 to 2.5V | | | 25KΩ min. | Sensor signal |
| $AGND_{Batt}$ | | 0V | | | | Analog battery ground |

*Table 10 - Connections and Signal Levels for Analog Front End*

[1] Input Logic low: 0 to 0.8V Input Logic high: 2 to 5.2V
[2] Output Logic low: 0 to 0.5V, Output Logic high: 4 to 5.1V
[3] Not referenced to GND. As cells are stacked in series connection.

## 2.4.2.2. Current Sensor

**IPO(Input, Process, Output)**

Table below describes Input, process and output for Current Sensor .

| Input | Process | Output |
|---|---|---|
| Battery current | Bidirectional monitoring of battery current, outputs analog voltages proportional to current. | Battery current |
| | | Analog voltages proportional to battery current |

*Table 11 – IPO for Current Sensor*

**Design requirements:** Gain and offset is to be determined in cooperation with Analog Front End designer. Offset drift must be as low as possible.

**Table of In-/Output Requirements**

Table below specifies requirements for input and output connections of Current Sensor.

| Connector Name | Direction | Voltage | Current | Input resistance | Remarks |
|---|---|---|---|---|---|
| **Connections to Propulsion Battery and Isolation Switch** | | | | | |
| Batt- | IN | 0V | -15 to 50A | | Voltage depends on number of connected cells |
| Batt- | OUT | 0V | -15 to 50A | | |
| **Connections to Analog Front End** | | | | | |
| Current Sensor Vdd | IN | 5V +/-0.2V | | 5KΩ min. | Sensor supply |
| Discharge current signal | OUT | 0 to 2.5V | Source 0.1mA min. | | Sensor output |
| Charge current signal | OUT | 0 to 2.5V | Source 0.1mA min. | | Sensor output |
| $AGND_{Batt}$ | | 0V | | | Analog battery ground |

*Table 12 - Connections and Signal Levels for Current Sensor*

## 2.4.2.3. Isolation Switch

**IPO(Input, Process, Output)**

Table below describes Input, process and output for Isolation Switch .

| Input | Process | Output |
|---|---|---|
| Battery current | Conduct battery current when closed.<br>Interrupt battery current and perform galvanic isolation of battery when open. | Battery current when switch closed<br>No current when switch open |
| Relay Coil+ | | |
| Relay Coil- | | |

*Table 13 – IPO for Isolation Switch*

**Design requirements:** Isolation switch must be a mechanical switch(contactor or relay) to meet Shell Eco-marathon requirements. And must be of normally open (NO) type to ensure that the switch will open if connection is lost or if BMS power is interrupted.

Resistance of closed switch must be as low as possible to limit dissipative loses.

As the load (motor controller) contains large capacitors, the inrush current can potentially damage the contacts of the isolation switch. The inrush current shall therefore be limited, to limit contact wear and risk of welding.

**Table of Connections and In-/Output Requirements**

Table below specifies requirements for input and output connections of Isolation Switch.

| Connector Name | Direction | Voltage | Current | Input resistance | Remarks |
|---|---|---|---|---|---|
| **Connections to Current Sensor and External Load** | | | | | |
| Batt+ | IN | 17.5 to 60V | -15 to 50A | | Voltage depends on number of connected cells |
| Batt+ (BMS protected) | OUT | 0 to 60V | -15 to 50A | | |
| **Connections to Analog Front End** | | | | | |
| Coil + | IN | 0 to 30V* | | 150Ω min. | *Switch Closed when Coil voltage > 17.5V<br>Switch Open when Coil voltage < 10V |
| Coil - | IN | 0V | | | |

*Table 14 - Connections and Signal Levels for Isolation Switch*

## 2.4.2.4. Digital Unit (HW)

**IPO(Input, Process, Output)**

Table below describes Input, process and output for Digital Unit.

| Input | Process | Output |
|---|---|---|
| SPI and parallel signals from Analog Front End | Interfacing inputs and outputs of Software Platform to CAN and USB voltage levels.<br><br>Establish galvanic isolation between Analog Front End and Software Platform. | SPI and parallel signals from Analog Front End (Isolated) |
| CAN<br>Physical layer as specified in ISO 11898. | | CAN level converted to be Software Platform compliant |
| USB<br>USB 2.0 Compliant | | UART<br>Software Platform compliant |
| Charger sense | | Charger sense (isolated) |

*Table 15 – IPO for Digital Unit*

**Design requirements:** A Charger sense input must be included to allow the BMS to resume normal operation after an undervoltage error. This enables the BMS to reclose the isolation switch at the connection of a charger.

All external devices communicating with the BMS must be galvanic isolated from the propulsion battery. This means that opto-isolators or similar and an isolated DC/DC converter must be included as part of the Digital Unit(HW).

Physical interfaces towards system blocks connected to the Digital Unit, is described in Table 16. However, physical interface between Digital Unit (HW) and Digital Unit Software platform is left for the Digital Unit designer to decide.

**Note:** Certain In-/Outputs requires routing to special functionalities of the Digital Unit Software Platform, such as interrupt functionality etc. This will be stated in remarks of Table 16.

**Table of Connections and In-/Output Requirements**

Table below specifies requirements for input and output connections of Digital Unit.

| Connector Name | Direction | Voltage | Current sink | Current source | Input resistance | Remarks |
|---|---|---|---|---|---|---|
| **Connections to Analog Front End** | | | | | | |
| SCLK | OUT | 5V logic[1] | 1mA min. | 1mA min. | | SPI interface |
| MOSI | OUT | 5V logic[1] | 1mA min. | 1mA min. | | |
| MISO | IN | 5V logic[2] | | | 10KΩ min. | |
| SS | OUT | 5V logic[1] | 1mA min. | 1mA min. | | |
| Convert | OUT | 5V logic[1] | 1mA min. | 1mA min. | | Starts ADC conversion |

| | | | | | | |
|---|---|---|---|---|---|---|
| Fault | IN | 5V logic[2] | | | 10KΩ min. | Reports errors. Must generate interrupt |
| $DGND_{Batt}$ | | 0V | | | | Digital battery ground |
| **Connections to CAN (external devices)** | | | | | | |
| CAN high | IN/OUT | 2.5 to 3.5V | | | 120Ω | Physical layer as specified in ISO 11898. Must be routed to CAN controller in Digital Unit Software Platform |
| CAN low | IN/OUT | 1.5 to 2.5V | | | | |
| CAN Gnd | | 0V | | | | |
| **Connections to USB (virtual COM for external device)** | | | | | | |
| USB 5V+ | IN | 5V +/- 0.25V | | | 50Ω min. | Must generate interrupt |
| Data - | IN/OUT | | | | | Must be converted to UART and routed to UART of Digital Unit Software Platform |
| Data + | IN/OUT | | | | | |
| USB Gnd | | 0V | | | | |
| **Connections to Charger (external device)** | | | | | | |
| Charger Sense+ | IN | 17.5 to 60V | | | | Charger Sense+ will be 0V when charger is off or disconnected. |
| Charger Sense- | | 0V | | | | |
| **Connections to Supply** | | | | | | |
| Aux Vdd | OUT | 17.5 to 60V | | 50mA min. | | Supply for Digital Unit. Voltage depends on number of connected cells |
| Aux Vss | | 0V | | | | |

*Table 16 - Connections and Signal Levels for Digital Unit*

[1] Output Logic low: 0 to 0.5V, Output Logic high: 4 to 5.1V
[2] Input Logic low: 0 to 0.8V Input Logic high: 2 to 5.2V

## 2.4.3. Elaborated Software Block Details

### 2.4.3.1. Digital Unit Software Platform

**IPO(Input, Process, Output)**
table below describes Input, process and output for Digital Unit Software Platform.

| Input | Process | Output |
|---|---|---|
| Battery data Acquired by Analog Front End.<br>bq76PL536A protocol | Calculation and estimation of SOC and Internal resistance etc. from data acquired by Analog Front End.<br>Performing communication with Analog Front End and external units.<br>Log data as specified in Specification Requirements, in non-volatile memory | Data log (via virtual COM)<br>See protocol in Specification Requirements |
| Log request and parameter change requests<br>See protocol in Specification Requirements. | | Actual battery information<br>(via CAN)<br>See protocol in Specification Requirements |
| Charger information<br>(connected or not) | | Start Analog Front End conversion request.<br>bq76PL536A protocol |
| Fault Interrupt<br>(Indicating errors) | | Request data from Analog Front End.<br>bq76PL536A protocol |

*Table 17 – IPO for Digital Unit Software Platform*

**Design requirements:** As power consumption is of great importance, sleep modes must be used where possible and safety or time critical functions must then be interrupt driven.

Physical Interfaces towards system blocks connected to the Digital Unit, is described in Table 16. However, physical interface between Digital Unit (HW) and Digital Unit Software platform is left for the Digital Unit designer to decide.

**Note:** As part of the software development process. The most appropriate methods for SOC, SOH and Internal resistance are to be found.

### Flowchart Diagram

To describe software execution flowcharts has been visualized in Figure 5.

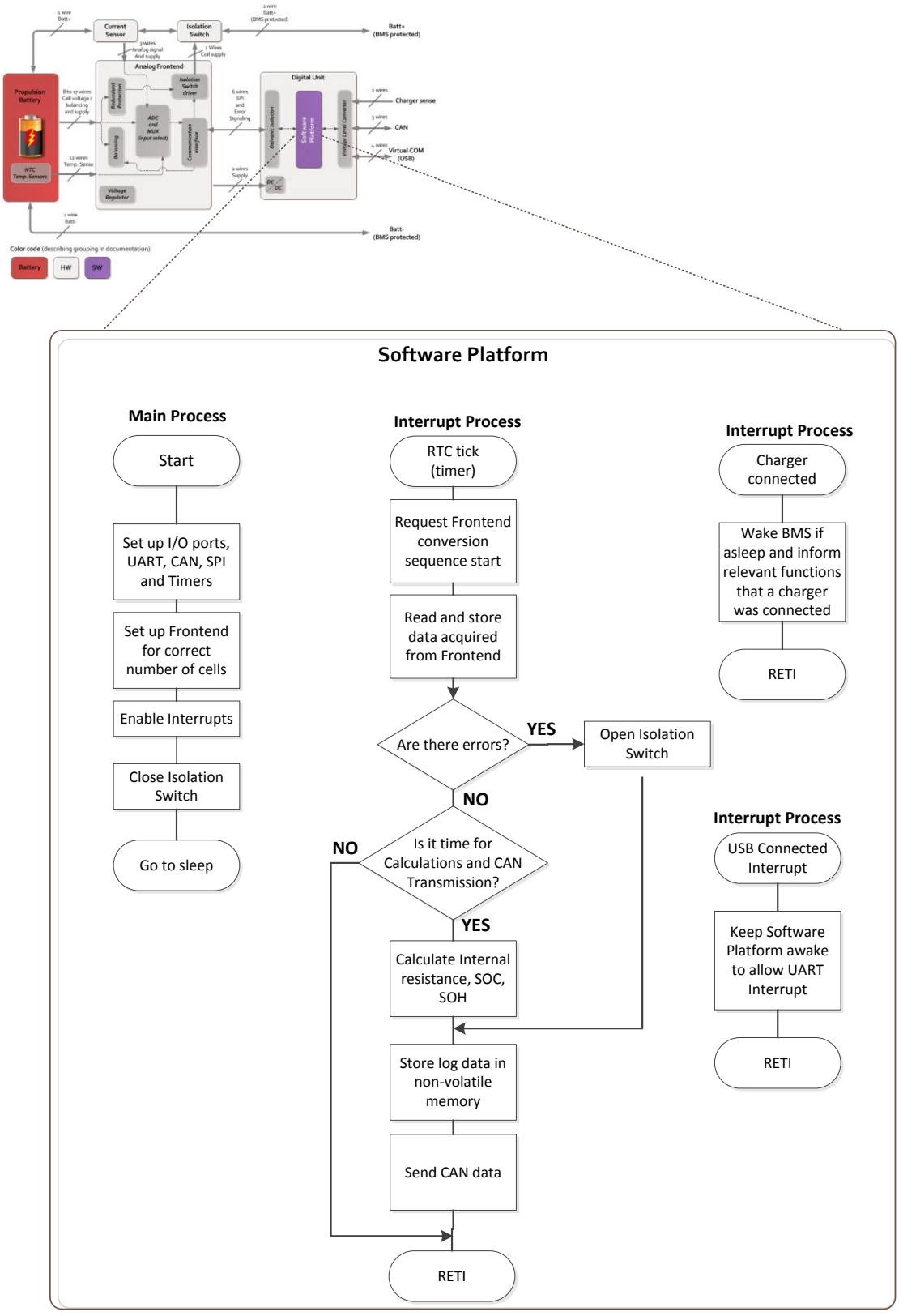



*Figure 5 - Flowchart draft*

# 3. DESIGN AND IMPLEMENTATION

In this chapter HW system blocks outlined in the system architecture will be elaborated to a level allowing implementation at component level. Furthermore, SW elements will be further detailed and subsequently implemented. Calculations and chosen technical solutions will be described and measurement results will be presented where considered relevant.

## 3.1. Hardware

This paragraph documents the HW design and implementation, unit by unit, in the same order as in the system architecture. For HW units including multiple circuits, a graphical overview of implemented circuits will be given. The schematics of each unit are presented and described individually. Full schematics will be presented in 0

Physical System Realization.

## 3.1.1. Propulsion Battery

Based on the performed battery test,[13] Lithium-ion polymer(Li-PO) is found to be the most appropriate choice, as it offers satisfying capacity at simulated worst case Eco-marathon conditions, as well as low internal resistance and weight. The cycle life is expected to be shorter compared to LiFePO4[14], but for this application cycle life is of little concern. Only 2/3 of the stated capacity was available from the tested LiFePO4 battery at 1.33C discharge rate and 8°C ambient. In comparison the stated capacity was achieved from the Li-PO battery. The different behavior during discharge can be seen in Figure 6 and Figure 7.

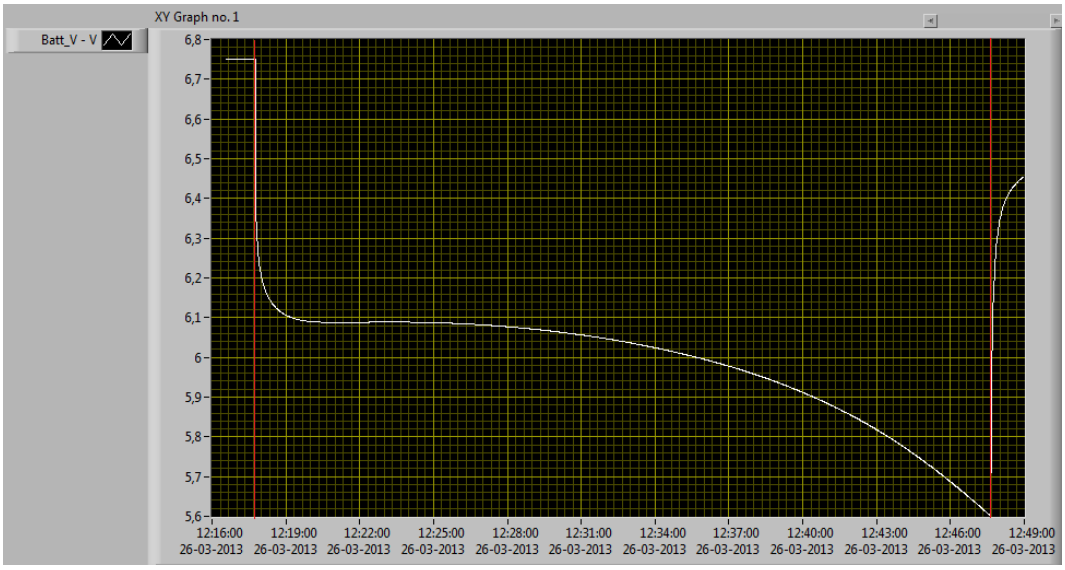



*Figure 6 - Discharge of LiFePO4 under worst case Eco-marathon conditions*

[13] See "Battery cell type test" in appendices
[14] http://batteryuniversity.com/learn/article/types_of_lithium_ion (date: 11-06-2013)

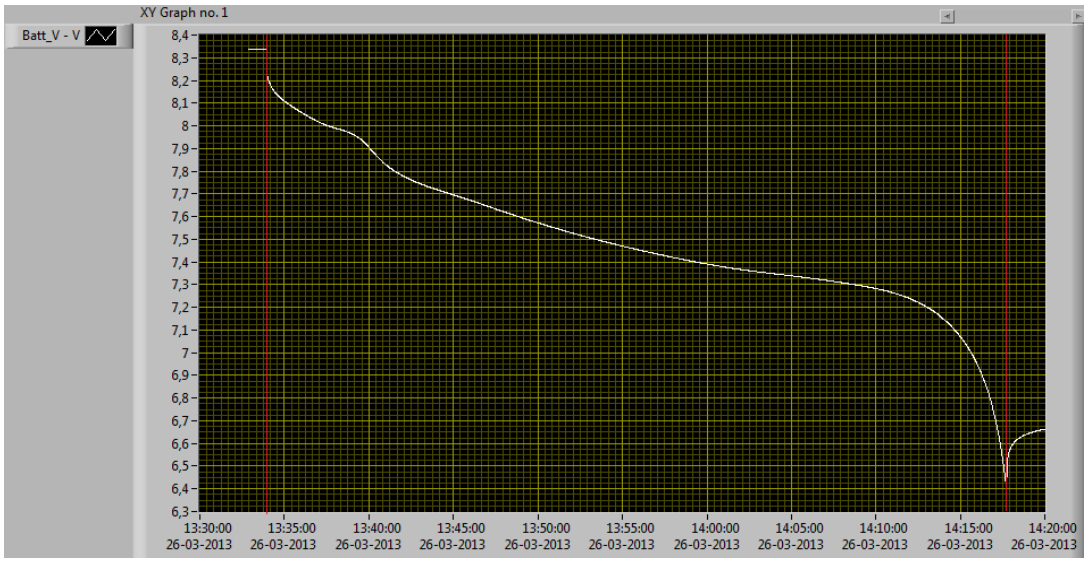



*Figure 7 - Discharge of Li-PO under worst case Eco-marathon conditions*

### Battery dimensioning and calculations

To meet the system voltage as described in requirement PB_NF.1, and to avoid the need of Front End Extension Modules(which will be described later) 6 series connected cells has been chosen. Based on cell count and voltage the required capacity has been found:

$$Required\ capacity[Ah] = \frac{Required\ capacity\ at\ load[Wh] + BMS\ consumption[Wh]}{Nominal\ Battery\ Voltage[V]} = \frac{70Wh + 2Wh}{22.2V}$$
$$= 3.24Ah$$

This results in the selection of the, Turnigy nano-tech 3.3 Li-PO pack, with specifications as stated below.


| | |
|---|---|
| Capacity [Ah] | 3.3 |
| Number of cells | 6 |
| Continues discharge [C] | 45 |
| Weight[g] | 565 |
| Max Charge Rate [C] | 10 |
| Length-A [mm] | 135 |
| Height-B [mm] | 45 |
| Width-C [mm] | 44 |

*Figure 8 - Picture of battery*[15]

*Table 18 - Battery specifications*[15]

### Battery test and measurements

The effective capacity available at the output of the BMS/Battery Unit. At a discharge current of 4A and a ambient temperature of 8°C is 75Wh (measured after 5 charge cycles, Start condition 4.2V per cell, End condition 3V per cell). See accept test for further test results.

[15] http://www.hobbyking.com/hobbyking/store/uh_viewItem.asp?idProduct=27121 (date: 22-05-2013)

## 3.1.2. Analog Front End

As described in the system architecture the core of the Analog Front End, will be the bq76PL536A. To achieve all required functionalities external circuitry and interfacing has been implemented. Overview of Front End circuit blocks can be seen in Figure 9. Elaborated circuit descriptions will be given below.

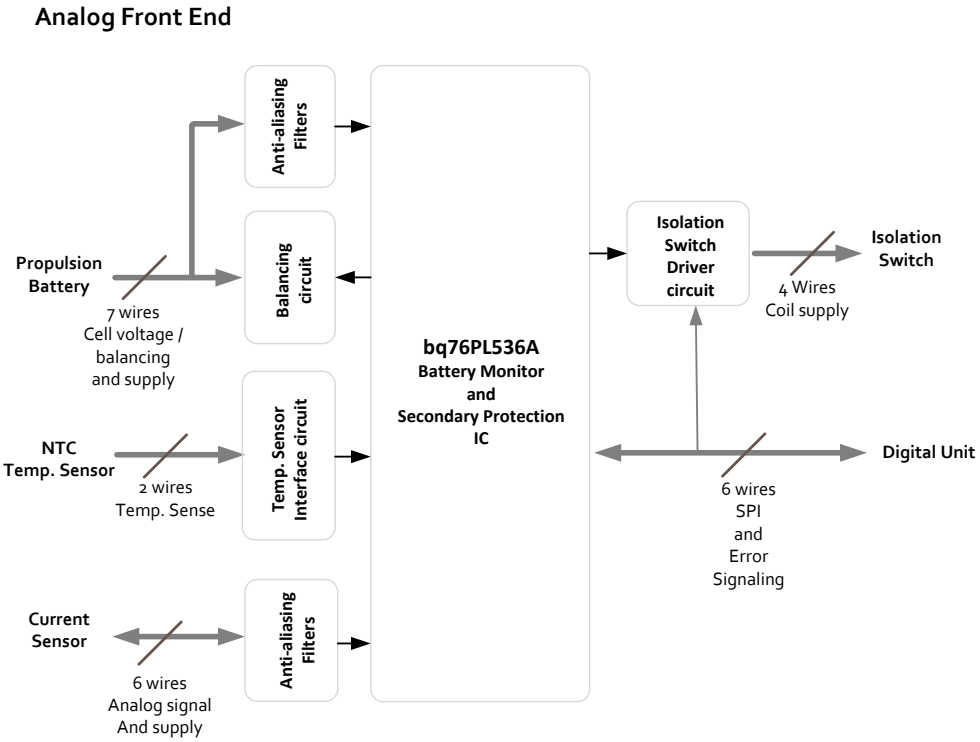



*Figure 9 - Front End circuit blocks*

### 3.1.2.1. Anti-aliasing Filters

To decrease unwanted ac noise, all signals are filtered very close to their respective ADC inputs. Cell voltages are filtered by a traditional 1.order RC low-pass filter, designed according to datasheet guidelines. 1kΩ is used as the bq76PL536A is calibrated to compensate for the voltage division created by this resistance and the input impedance. To filter the charge current signal from the Current Sensor a similar low-pass filter is applied, while the discharge current signal is filtered by a differential RC low-pass filter, filtering both common mode and differential mode noise. Schematic can be seen in Figure 10, component functionality descriptions and calculations are found below.

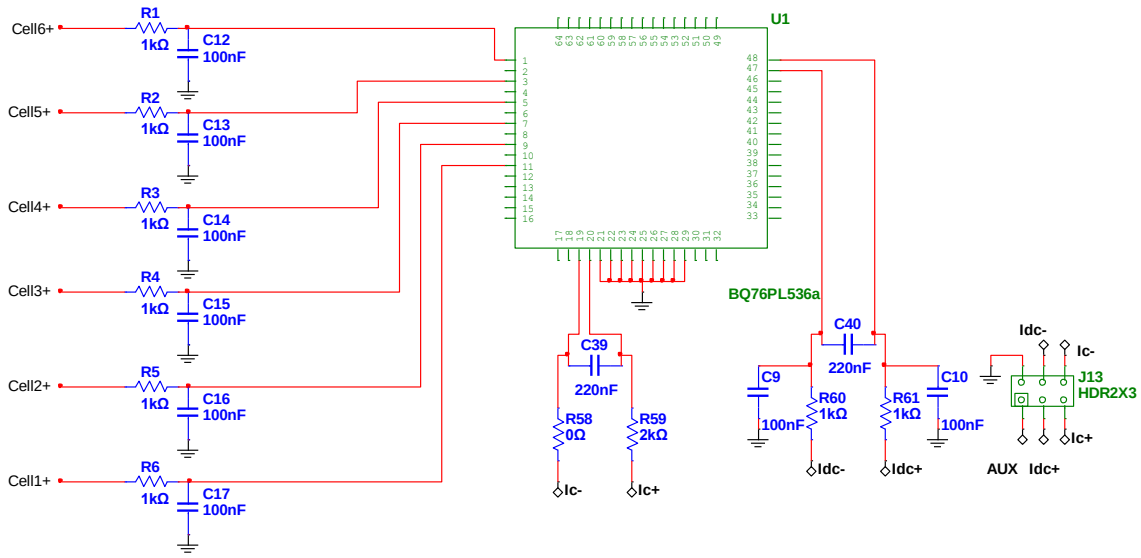



*Figure 10 - Anti-aliasing filters, all filter components are placed very close to the IC*

**Anti-aliasing Filters component description and calculations**

**Resistors R1 to R6 and Capacitors C12 to C17:** Low-pass filters, filtering cell voltages. Designed according to datasheet guidelines.

**Resistors R58, R59 and Capacitor C39:** Low-pass filter. R59 is large enough to isolate the capacity from the current sensor amplifier, and sufficient phase margin is thereby maintained.

$$f_{-3dB} = \frac{1}{2\pi * R59 * C39} = 362Hz$$

**Resistors R60, R61 and Capacitors C9, C10 and C40:** Common mode and differential mode filtering of discharge signal referenced to 0.1V ref. voltage.

$$f_{-3dB\ CM} = \frac{1}{2\pi * (R60//R61) * (C9//C10)} = 1.6KHz$$

$$f_{-3dB\ DM} = \frac{1}{2\pi * (R60 + R61) * (C40 + C9/2)} = 295Hz$$

## 3.1.2.2. Balancing circuit

The bq76PL536A offers outputs to control balancing on request from the Digital Unit. Therefore, dissipative balancing can be easily implemented, using an N-channel MOSFET as switch and a power resistor as dissipative element. Thereby a part of the charging current can be bypassed, which allows reduction of charging current feed to cells with highest SOC. The schematic is shown in Figure 11,component functionality descriptions and calculations are found below.

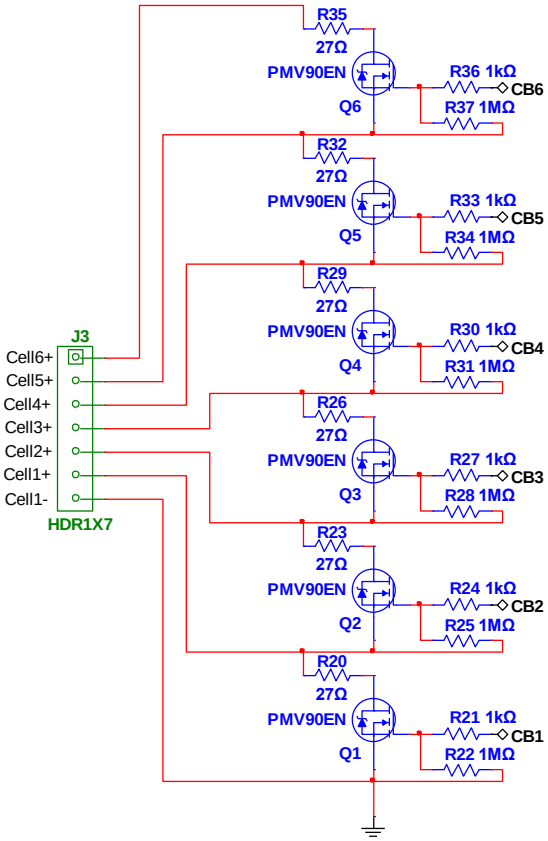



*Figure 11 - Balancing circuit*

**Balancing component description and calculations**

**MOSFETS Q1 to Q6:** While in saturation mode cell is partly bypassed, reducing the charging of the particular cell. PMV90EN is selected based on its low subthreshold leakage and low RDS. $I_{Drain}$ has been over dimensioned to allow upgrade to larger balancing current.

**Power resistors R20, R23, R26, R29, R32 and R35:** Bleeder resistors, converting bypassed charging current to heat while its respective MOSFET is in saturation mode. To allow a proper heat transfer to PCB traces, power resistors with wide terminals has been selected. To decrease the time required for balancing a balancing current of two times the min. requirement(BMS_NF.3) has been selected.

$$dissipation\ resistance[\Omega] = \frac{Vcell[V]}{required\ balancing\ current[A]} = \frac{4\text{V(approx.)}}{150\text{mA}} = 26{,}66\Omega$$

Nearest standard value(27Ω) has been selected.

**Resistors R21, R24, R27, R30, R33 and R36:** Limits $I_{Gate}$ and thereby the sink / source current required by the bq76PL536A balancing outputs at state shift(ON to OFF and OFF to ON). In theory these resistors could be excluded as $Z_{out}$ of the balancing outputs is high.

**Resistors R22, R25, R28, R31, R34 and 37:** Pull-down resistors, ensures MOSFETS are off when bq76PL536A is shut down(balancing outputs are floating).

**Balancing Test and Measurements**
Test of this unit will be performed as part of the accept test. See accept test chapter.

### 3.1.2.3. Temp. Sensor Interface circuit

To allow battery temperature surveillance, a voltage divider including a Thermistor(NTC) has been used to convert temperature to a proportional voltage. As the ADC reference voltage used for the temperature sensor is divided from the sensor supply voltage(REG50), the ADC result will be ratiometric, which eliminates the need of further supply voltage regulation. The bandwidth of the sensor has been limited to reduce noise. The circuit can be seen in Figure 12. The circuit design is based on application note recommendations[16].

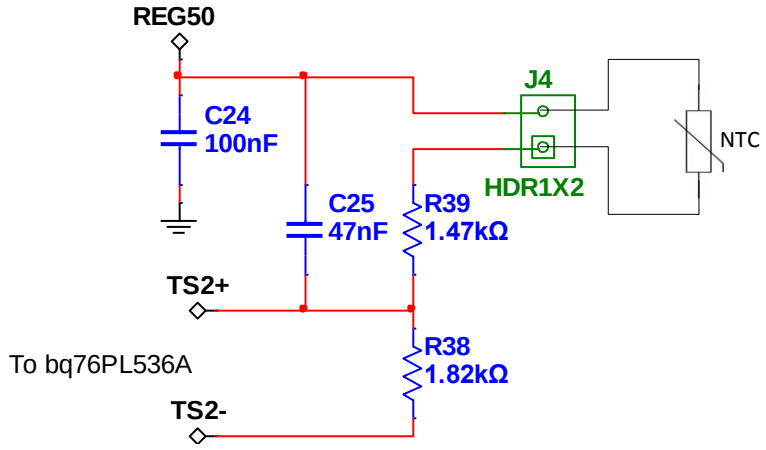



*Figure 12 - Temp. sensor Interface circuit (NTC is mounted on the battery)*

**Temp. Sensor component description and calculations**

**Capacitor C24:** Decoupling capacitor.

**Resistors R38, R39 and NTC:** Creates a temperature dependent voltage divider. Increased temperature will result in increased current through R38, which increases the voltage across it.

**Capacitor C25:** reduces the bandwidth and thus the noise.

$$f_{-3dB} = \frac{1}{2\pi * R_{eq} * C} = \frac{1}{2\pi * (R38^{-1} + (R39 + NTC\_resistance)^{-1})^{-1} * C25}$$
$$= \frac{1}{2\pi * (1820^{-1} + (1470 + 10000)^{-1})^{-1} * 47 * 10^{-9}} = 2.16\text{KHz}$$

[16] See "bq76PL536A - Battery monitor and secondary protection" in appendices

**Temp. Sensor Test and Measurements**

Temperature measurements has been performed using AMETEK ITC-155 A temperature calibrator. See Figure 13.

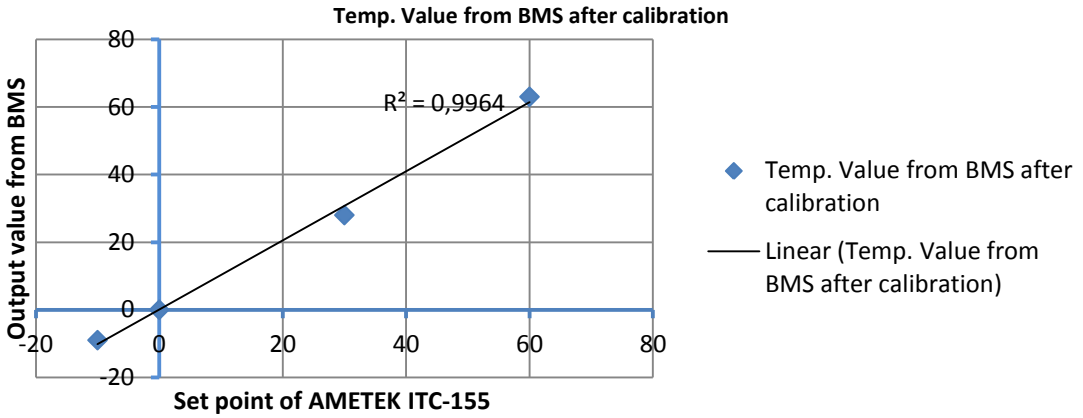



*Figure 13 - Temperature measurement results compared with trend line*

## 3.1.2.4. Isolation Switch Driver circuit

The purpose of this circuit is to allow the Digital Unit and the bq76PL536A to drive the Isolation Switch relay. To ensure the flexibility of connecting relays with any coil voltage rating, open drain topology has been chosen.

As subthreshold leakage is proportional to $V_{DS}$ (which is equal to the battery voltage) extra attention has been paid to decrease subthreshold leakage of this driver. Therefore stacked MOSFETS[17], a technique commonly used in IC design, has been implemented to decrease leakage, this also adds a logic AND functionality, which ensures that errors detected in either the bq76PL536A or the Digital Unit will result in interruption of battery current flow, as both units must output a logic high to close the Isolation Switch.

To reduce contact wear and the risk of relay welding, a pre-charge relay driver circuit has been included. The pre-charge circuit ensures that any capacitive load will be pre-charged by a limited current to avoid an inrush current peak.

The Isolation Switch and Pre-charge relay will be discussed later.

The Isolation Switch Driver circuit can be seen in Figure 14.

[17] http://ambienthardware.com/courses/tfe01/pdfs/Roy1.pdf (date: 11-06-2013)

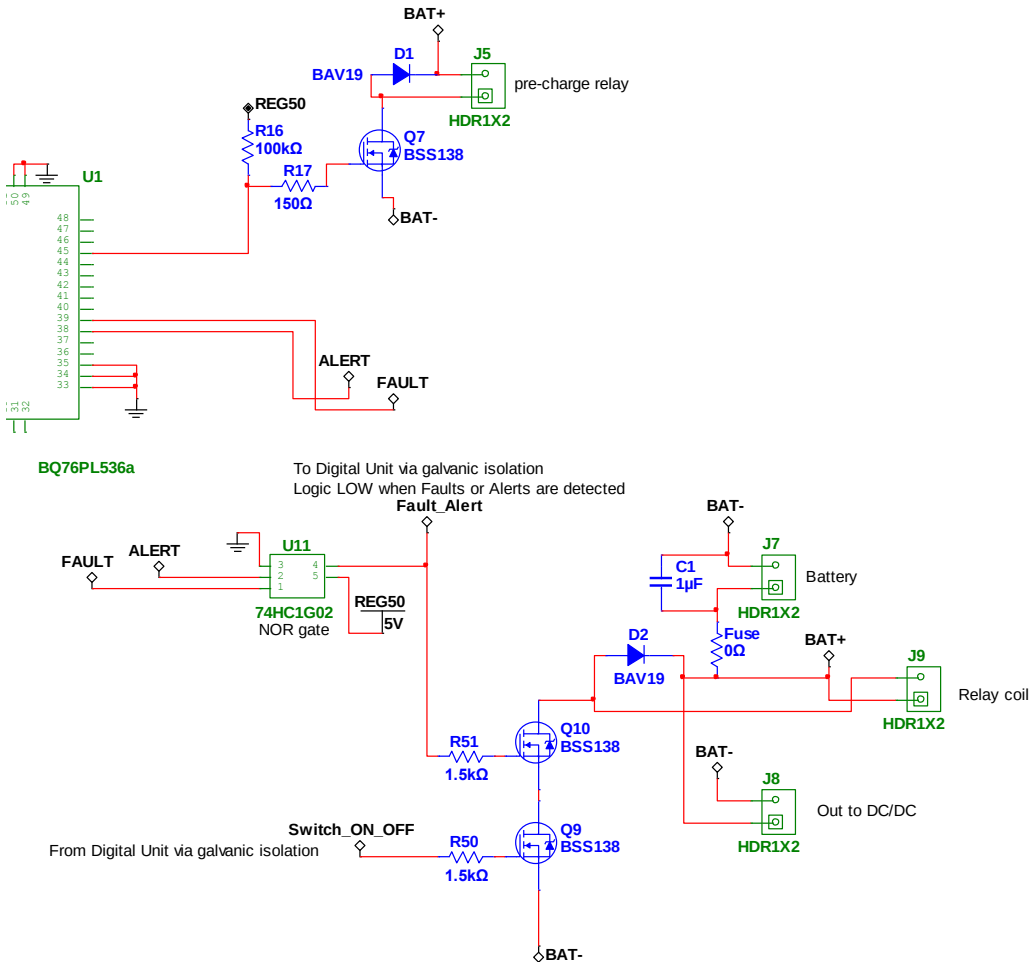



*Figure 14 - Isolation Switch Driver circuit*

**Isolation Switch component description and calculations**

**Pre-charge Driver (Q7, D1, R16 and R17):**

**MOSFET Q7:** A switching device configured for open-drain output, while in saturation mode, the pre-charge relay is active.
**Diode D1**: Transient protection, clamps voltage transient that would otherwise appear when Q7 is switched OFF.
**Resistor R16:** Pull-up resistor(output of bq76PL536A is open drain).
**Resistor R17:** Limits $I_{Gate}$ to a level accepted by the bq76PL536A output.

**Isolation Switch Driver circuit (Q9, Q10, D2, C1, R50, R51 and U11):**

**MOSFETS Q9 and Q10:** Stacked MOSFETS which ensures logic AND operation with open drain output and reduces leakage while in OFF mode, as leakage current passing through Q10 will charge the capacity present at the drain of Q9 thus increase $V_{S\text{-}Q10}$ which results in a negative $V_{GS\text{-}Q10}$(leakage is dramatically reduced when $V_{GS} < 0$).
**Diode D2:** Transient protection, clamps voltage transient that would otherwise appear when Q9 and Q10 are switched OFF.
**Capacitor C1**: Decoupling capacitor.
**Resistors R50 and R51:** Limits $I_{Gate}$ to a level tolerated by the gate driving devices.

**NOR gate U11:** Ensures that any Fault or Alert detected by bq76PL536A will turn OFF Q10 and thereby open the Isolation Switch. Furthermore the gate output is send to the Digital Unit(via the galvanic isolation) to warn this unit that errors has been detected.

**Isolation Switch Driver Test and Measurements**

Test of this unit will be performed as part of the accept test. See accept test chapter.

## 3.1.3. Analog Front End Extension Module

The Analog Front End support up to 6 cells, if a larger cell count is required an extension module can be connected. This system supports up to 2 extension modules which allows connection of up to 18 cells. The extension module is similar to the Analog Front End with the exception that there is no SPI interface for connection to the Digital Unit, no Isolation Switch driver, and no input for current sensor. Furthermore the host select pin of bq76PL536A (pin 44) is pulled high to disable the SPI host interface. A draft of extension module connection can be seen in Figure 15.

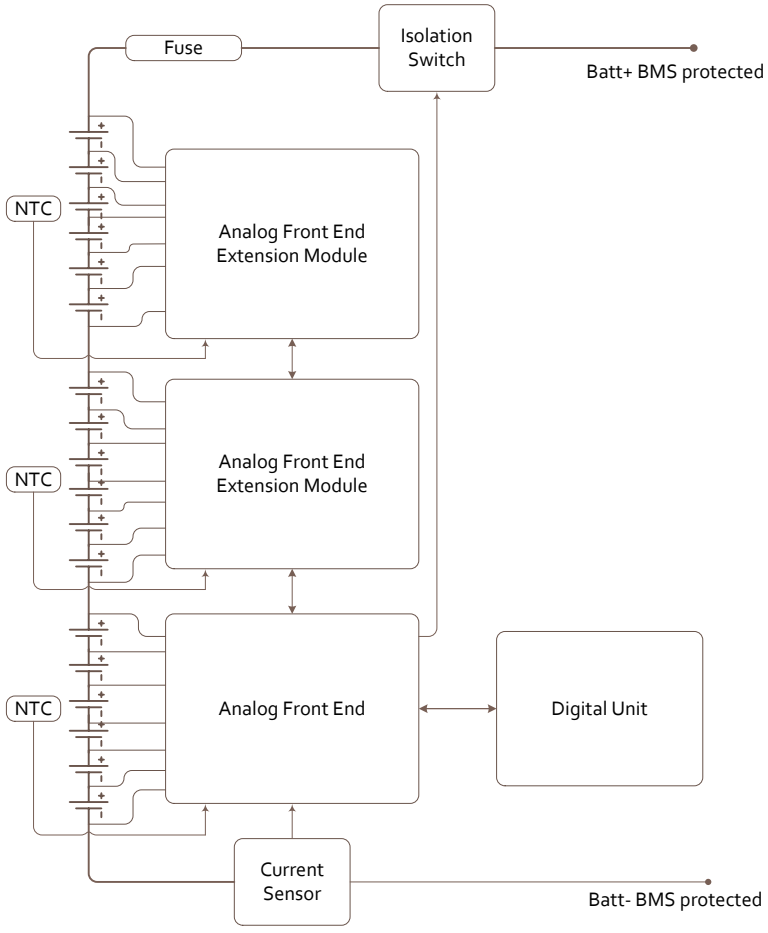



*Figure 15 - Connection of Extension Modules*

### 3.1.4. Current Sensor

Two types of sensors has been considered suitable, hall current sensors and shunt based current measurement. The benefit of the hall sensor is that no resistance is inserted in the conductor carrying the current to be measured, as opposed to the shunt sensor where power loses are proportional to the measured current. The static supply current is however higher for the hall current sensor, than what can be achieved with a low power shunt amplifier.

**Sensor type power consumption comparison:**

The current to be measured is estimated to be within a range of -10 to 10A at least 90% of the time. And the average current is estimated to be well below 4A, therefore a current of 4A has been used for comparison.

| Parameter to be compared | Hall current sensor ACS756 | Shunt current sensor based on OPA333 |
|---|---|---|
| Supply voltage | 5V | 5V |
| Supply current | 10mA(typ.) | < 100uA(estimated) |
| Resistive loses at 4A | 2mW | 16mW |
| Total power consumption at 4A | 52mW | 16.5mW |

*Table 19 - sensor comparison*

From the comparison, it can be concluded that a shunt current sensor will offer the lowest overall consumption, and requires a supply current within the capability of the LDO integrated in the bq76PL536A, as oppose to the Hall current sensor which requires a dedicated voltage regulator.

As a wide measuring range is required and a high accuracy is desirable, the current sensor has been designed with separate amplifiers for charge and discharge measurement, connected to individual ADCs, thereby the measurement resolution is improved as the dynamic range of each ADC covers a smaller measurement range.

The Current Sensor circuit can be seen in Figure 16, component description is given below.

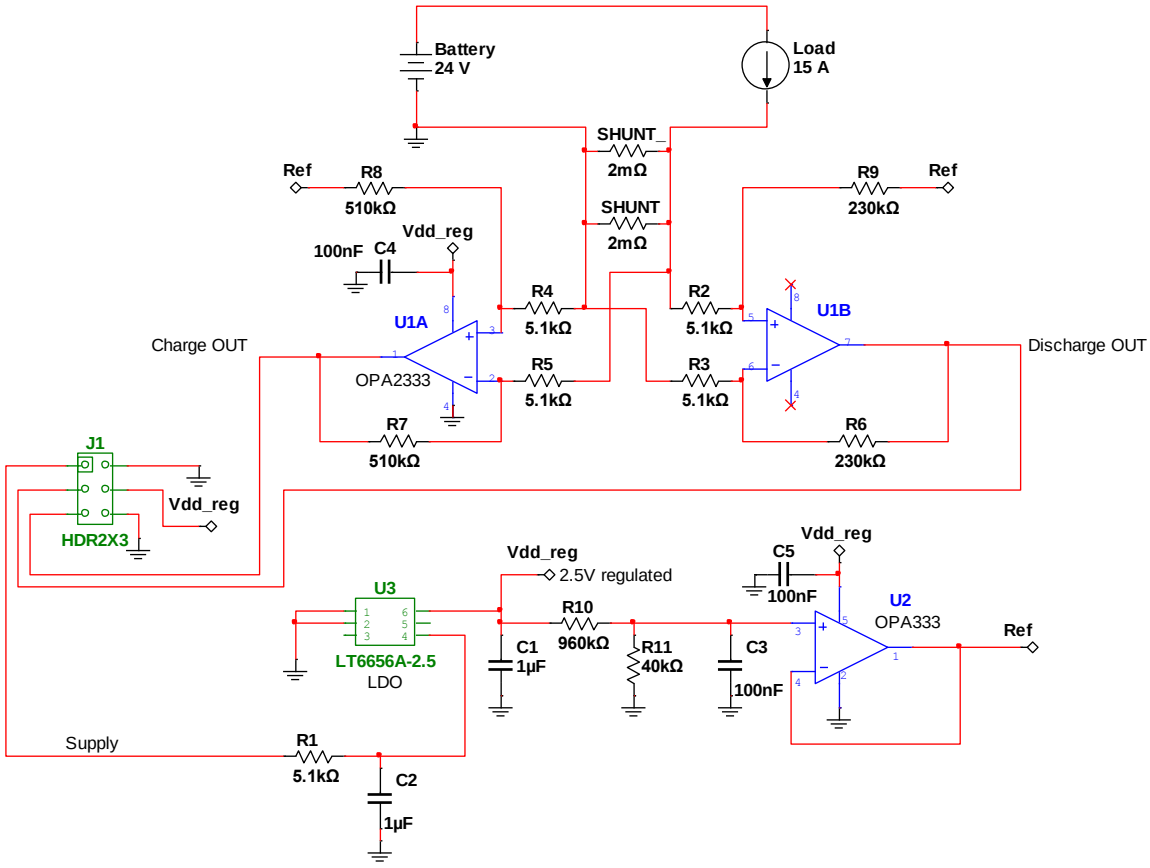



*Figure 16 - Current Sensor circuit*

### Current Sensor component description and calculations

#### Voltage regulator (U3, R1, C2 and C1):

**Regulator U3:** A series regulator with ultra low power consumption reduces input voltage from 5V to 2.5V and significantly reduces ripple. The regulator is needed to ensure a stable reference voltage(described below). Furthermore, reducing the Op Amp supply voltage to 2.5V ensures that the ADCs won't be overdriven, even if the current to be sensed exceeds the specified maximum value. In addition, the lowered Op Amp supply voltage reduces the supply current.
**Resistor R1:** limits the inrush current, which must be kept below 1mA to allow direct connection to the AUX output of bq76PL536A, by using this output to supply the sensor, the sensor can be switched OFF when system is put to sleep.
**Capacitors C1 and C2:** Ensures stable operation of U3, and noise reduction. low ESR/ESL types has been chosen for good HF noise suppression

#### Reference circuit (U2, C5, C3, R10, R11):

Creates a low impedance voltage source. This reference voltage of 0.1V is needed as neither the output of U1 nor the ADC input(except the GPAI ADC input) are able to operate down to 0V.
**Resistors R10 and R11:** Creates a voltage divider.
**Capacitors C3 and C5:** Ensures decoupling.
**Op Amp U2:** Buffer ensuring low $Z_{Out}$.

**Charge current sense amp. (U1A, C4, R4, R5, R7, R8):**

Difference amplifier, which amplifies the voltage across the shunt while current flows into the battery. The output voltage is referenced to ground which means that a offset voltage of 0.1V is applied to the ADC while charging current is zero, this is necessary as the TS1 ADC input range of the bq76PL536A do not cover voltages near 0V.

The gain must be high enough to ensure that the full scale current value results in a output voltage of 2.5V(the max. input value of the ADC). However, as the TS ADC input used for charge current monitoring, supports programmable over temperature limit, which in this case is used as a redundant charge current limit, the gain of the charge current sense amplifier must be set lower, as the max. programmable value is 2V(0.4*REG50)[18].

A redundant charge current protection limit of 19A has been selected, this limit will only be reached if the primary protection implemented in the Digital Unit fails.

$$Required\ gain = \frac{Required\ V_{Out} - V_{Offset}}{V_{In\_full-scale}} = \frac{2V - 0.1V}{19mV^*} = 100\ V/V$$

$$Gain = \frac{R7}{R6} \Rightarrow R7 = Gain * R6 = 100 * 5.1K\Omega = 510K\Omega$$

*As the shunt resistance is 1mΩ, the input will be 1mV per Ampere.

**Discharge current sense amp. (U1B, R2, R3, R8, R9):** Difference amplifier, which amplifies the voltage across the shunt while current flows out of the battery. The output voltage is referenced to Ref(0.1V) which is possible, as the input range of the GPAI ADC input range of the bq76PL536A includes 0V. By measuring the voltage difference between Vout and Ref, reference drift will be cancelled out.

The full-scale value is set higher than the specification requirement demands, to allow detection of overcurrent situations. A value of 55A is chosen.

$$Required\ gain = \frac{Required\ V_{Out} - V_{Offset}}{V_{In_{full}-scale}} = \frac{2.5V - 0.1V}{55mV^*} = 43.6\ V/V$$

$$Gain = \frac{R8}{R3} \Rightarrow R8 = Gain * R3 = 43.6 * 5.1K\Omega \approx 220K\Omega$$

*As the shunt resistance is 1mΩ, the input will be 1mV per Ampere.

[18] See "bq76PL536A - Battery monitor and secondary protection" in appendices

**Current Sensor Simulations**

Simulations has been performed to verify functionality and gain calculations. Furthermore, the bandwidth and phase margin of the amplifiers has been found. See simulations below:

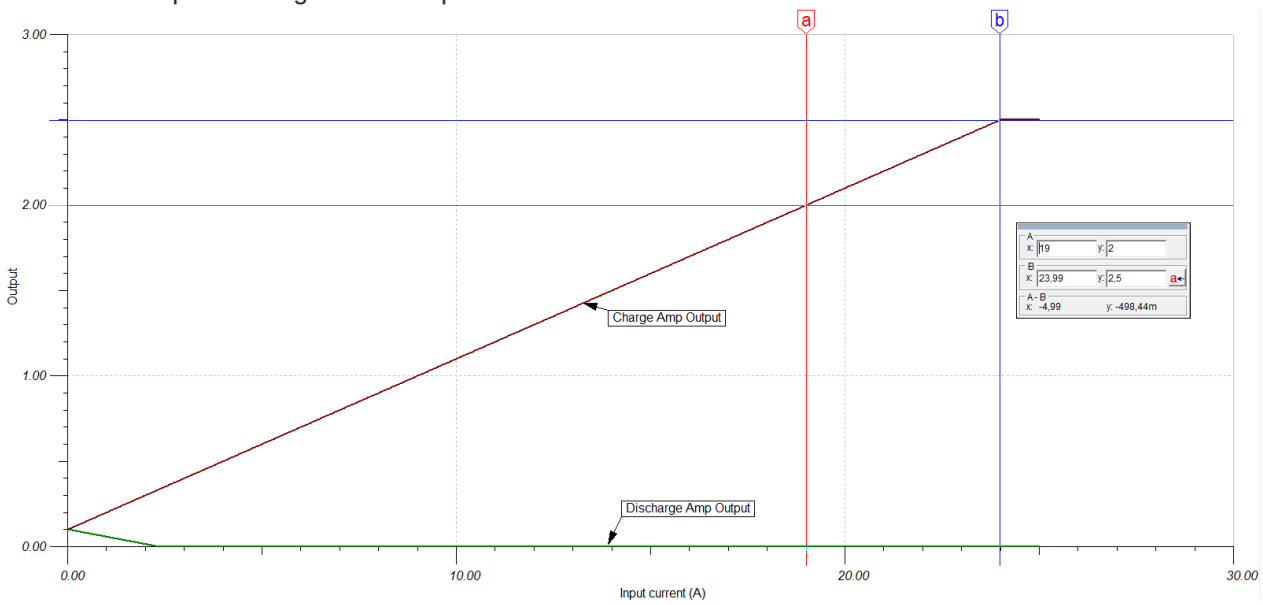



*Figure 17 - DC transfer characteristics (charging)*

Comment on Figure 17: Functionality is confirmed. Output voltage is 2V at a charging current of 19A as expected.

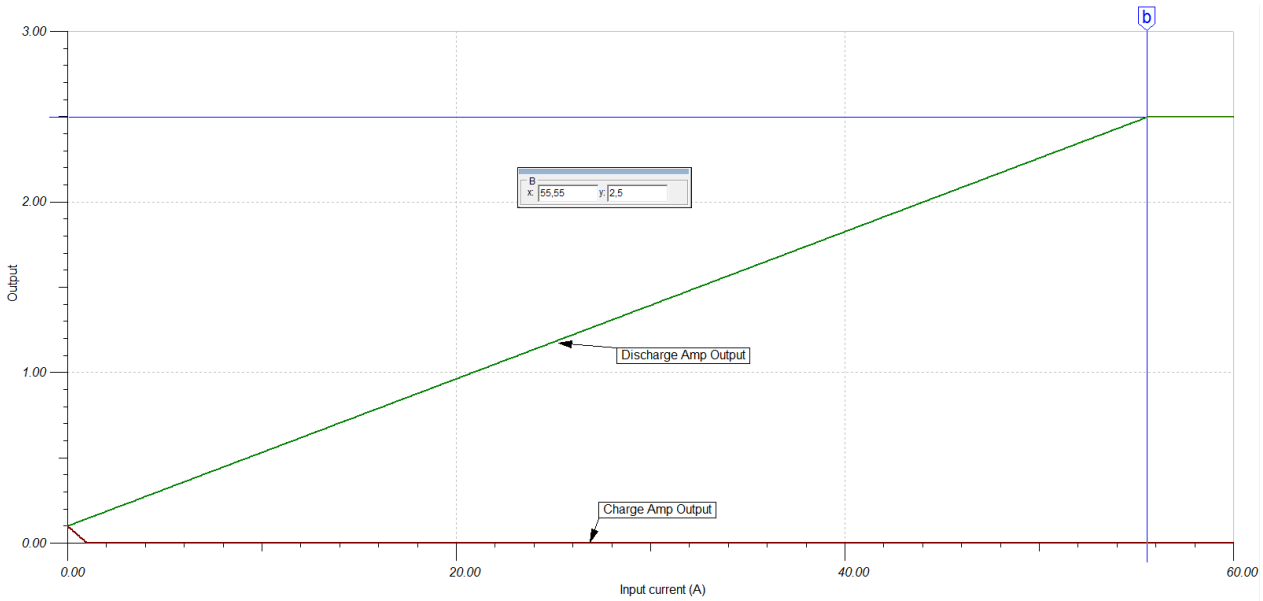



*Figure 18 - DC transfer characteristics (discharging)*

Comment on Figure 18: Functionality is confirmed. Output is limited by the positive rail when discharge current exceeds 55.55A, as expected.

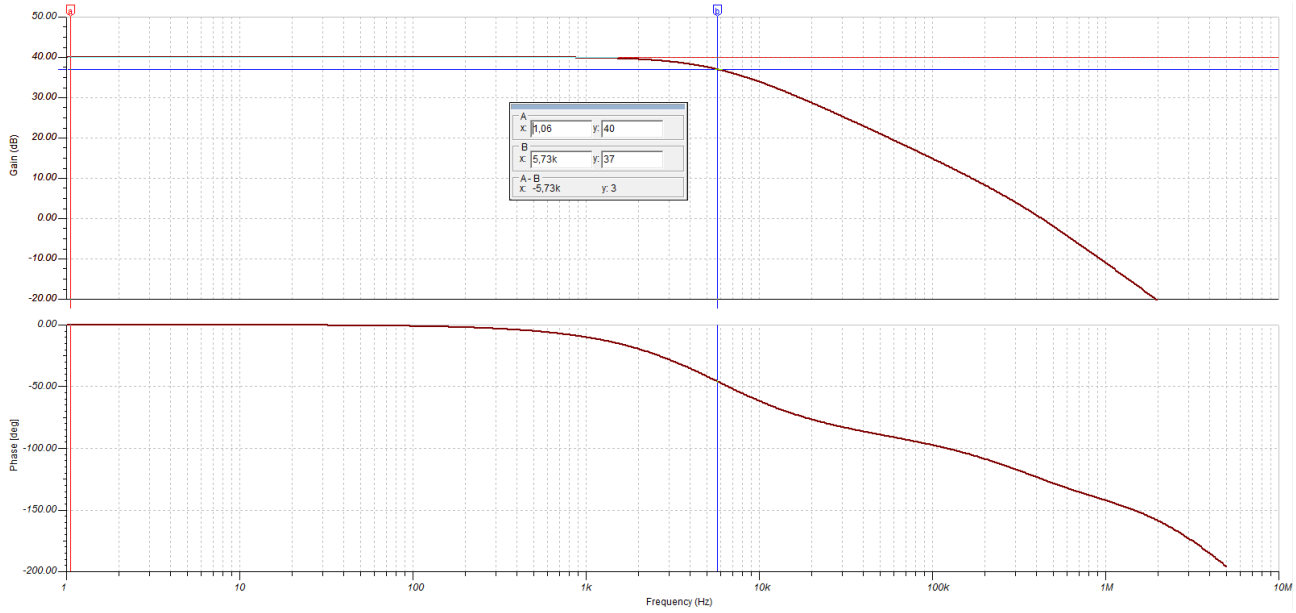



*Figure 19 - Simulation of bandwidth and gain verification(Charge current amplifier)*

Comment on Figure 19: It can be concluded that the expected gain is achieved. Furthermore, it can be seen that the closed loop bandwidth is 5,73KHz. The noise could be decreased by reducing the bandwidth of the amplifier, this is however considered unnecessary as the signal is subsequently filtered by the anti-aliasing filter placed at the ADC input.

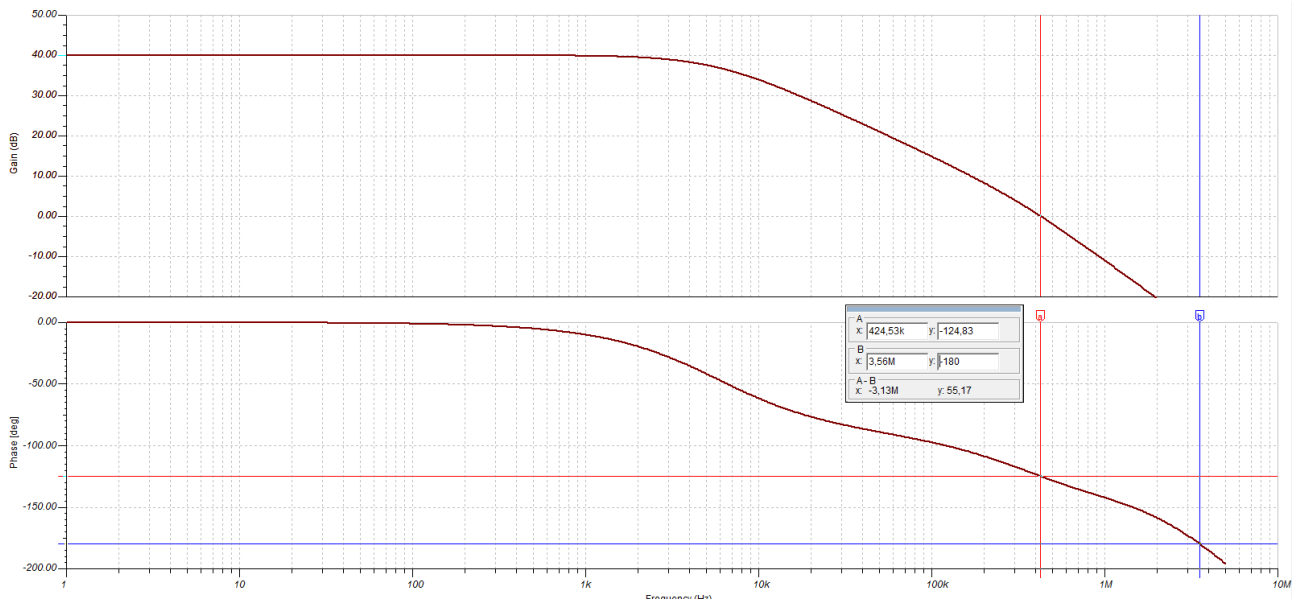



*Figure 20 - Phase margin(Charge current amplifier)*

Comment on Figure 20: The phase margin is 55° for the unloaded amplifier. The phase margin must be taken into consideration if a capacitive load is applied.

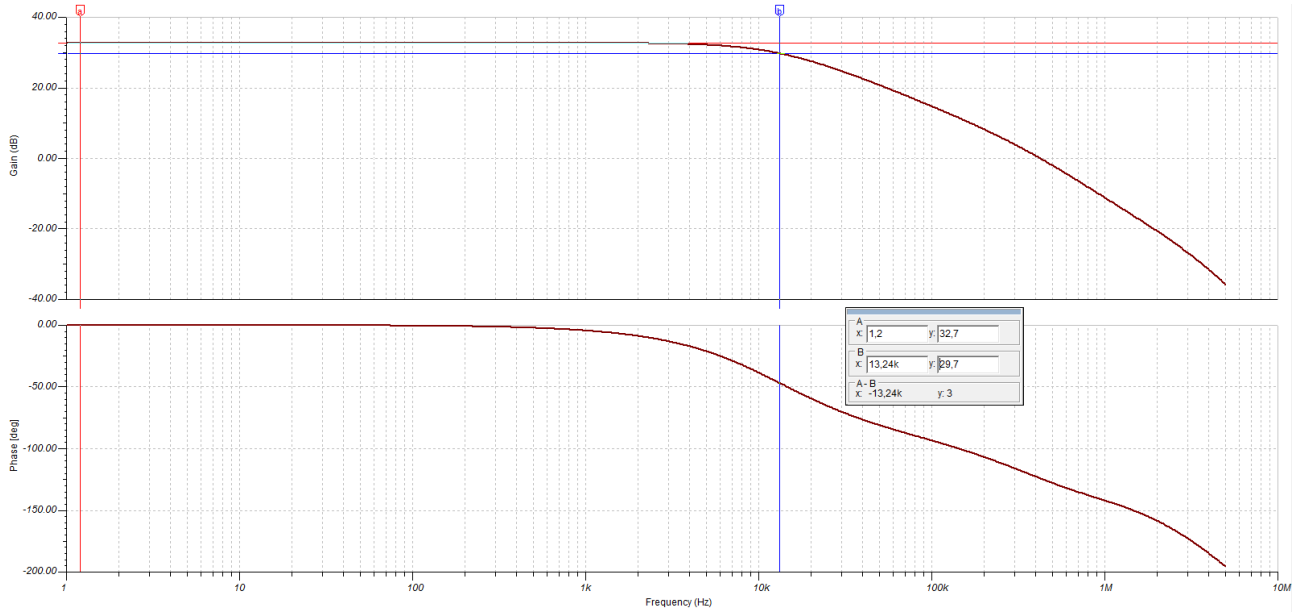



*Figure 21 - Simulation of bandwidth and gain verification(Discharge current amplifier)*

Comment on Figure 21: It can be concluded that the expected gain is achieved. Furthermore, it can be seen that the closed loop bandwidth is 13.24KHz.

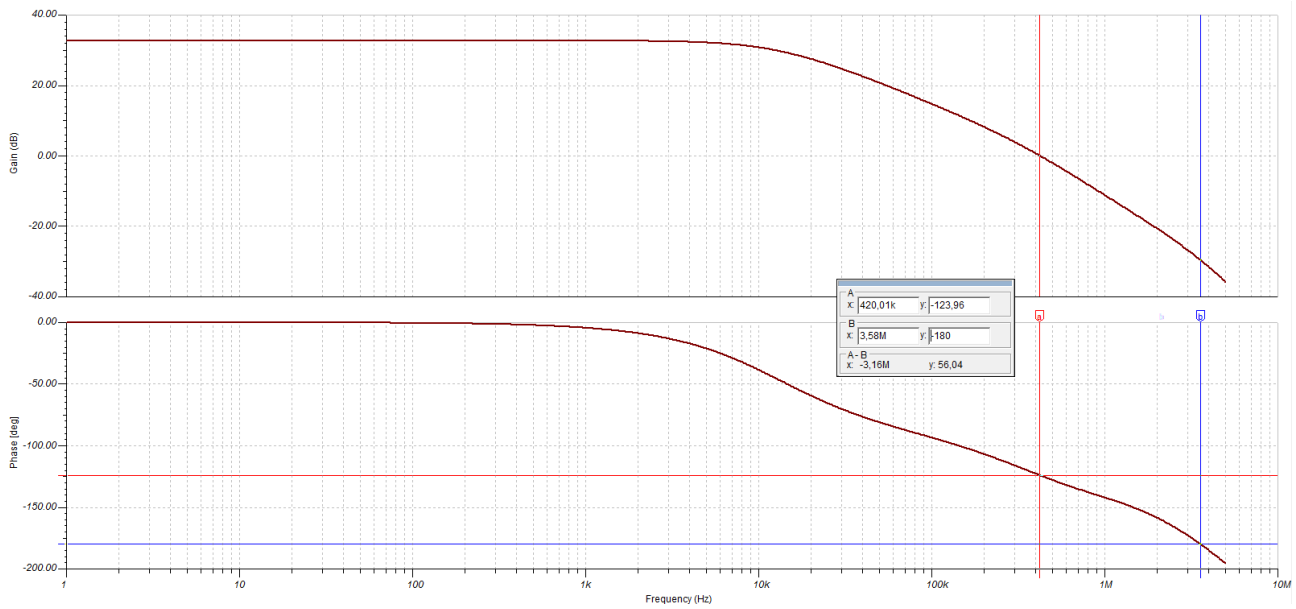



*Figure 22 - Phase margin(Discharge current amplifier)*

Comment on Figure 22: The phase margin is 56° for the unloaded amplifier. The phase margin must be taken into consideration if a capacitive load is applied.

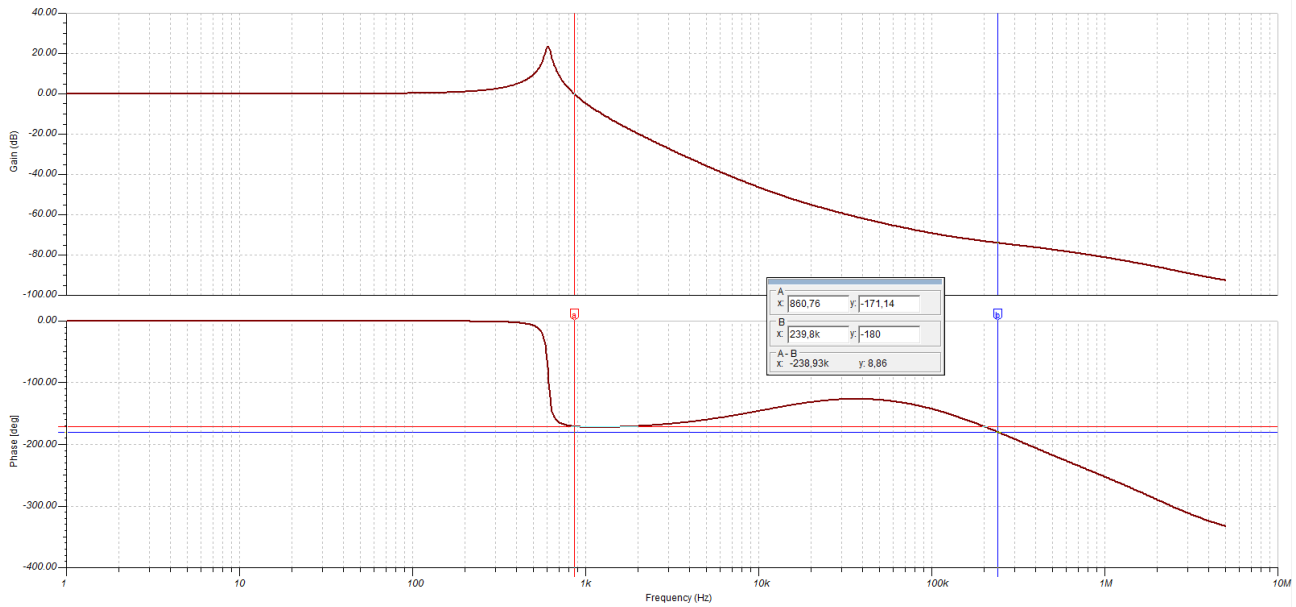



*Figure 23 - AC transfer characteristics of Buffer(U2)*

Comment on Figure 23: Even though the OPA333 is internally compensated and stated to be unity gain stable, the phase margin of the buffer(U2) is only 9° while unloaded. However, as no stability issues has been detected, no further compensation has been considered necessary.

**Current Sensor Test and Measurements**

**Supply current: 44.4uA** (Vsupply = 5V, output unloaded)

To ensure correct functionality and linear operation, the Current Sensor has been tested. The output has been measured after the ADC to include ADC gain and offset errors in the calculation of calibration constants.

**Charge current sense Amp.**

| Measurement No: | Input [mA] | Output [raw ADC value] |
|---|---|---|
| 1 | 0 | 691 |
| 2 | 500 | 1033 |
| 3 | 1000 | 1350 |
| 4 | 1500 | 1672 |
| 5 | 2000 | 2012 |

*Figure 24 - Measurements performed to acquire calibration information(Charge)*

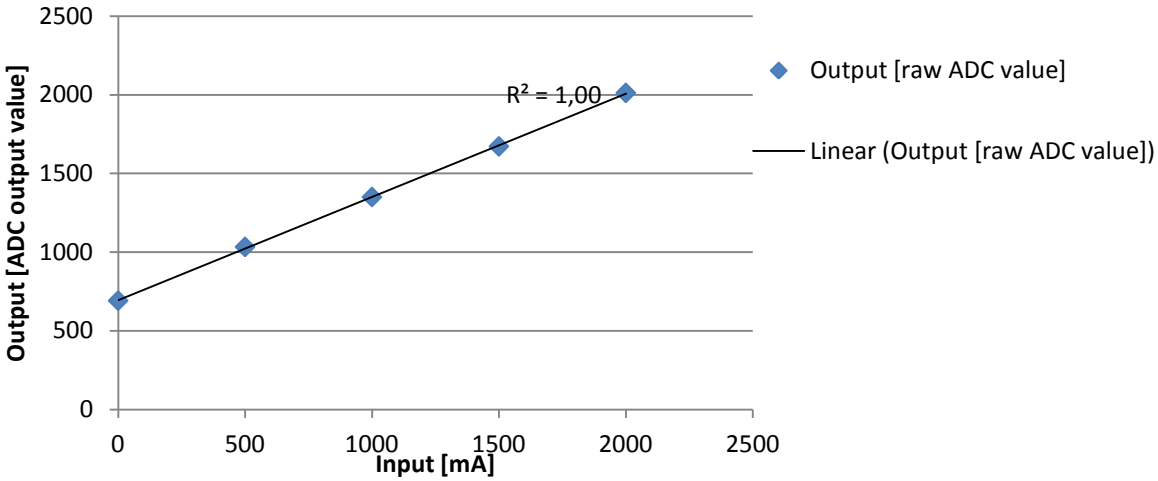



*Figure 25 - Graphical presentation of measurements and trend line(Charge)*

Calibration constants for the charge current sense amplifier has been found based on the trend line slope and interception point. The binary to mA conversion, implemented in the source code can be seen below:

```
if(Icharge < Ich_offset)
{
    Icharge = 0;
}
else
{
    Icharge = (unsigned long)(Icharge - Ich_offset)*1480/1000;
}
```

**Discharge current sense Amp.**

| Measurement No: | Input [mA] | Output [raw ADC value] |
|---|---|---|
| 1 | 0 | 10 |
| 2 | 500 | 150 |
| 3 | 1000 | 291 |
| 4 | 1500 | 436 |
| 5 | 2000 | 579 |

*Table 20 - Measurements performed to acquire calibration information(Discharge)*

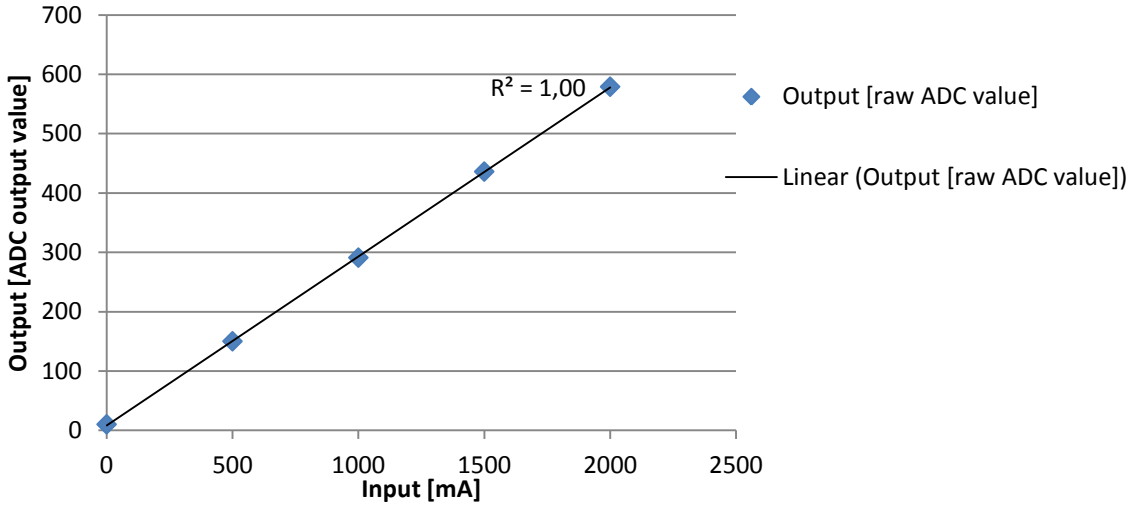



*Figure 26 - Graphical presentation of measurements and trend line(Discharge)*

Calibration constants for the discharge current sense amplifier has been found based on the trend line slope and interception point. The binary to mA conversion, implemented in the source code can be seen below:

```
//GPAI ADC input raw value converted to mA
Idischarge = (Rec_buffer[1]<<8) + Rec_buffer[2];

if(Idischarge < Idis_offset)
{
    Idischarge = 0;
}
else
{
    Idischarge = (unsigned long)(Idischarge - Idis_offset)*35/10;
}
```

## 3.1.5. Isolation Switch

This unit consist of a isolation switch relay and a pre-charge circuit. While relays are a bad solution in an low power application, they have been considered the only solution as real physical isolation of the battery, in the event of errors, has been required by the Shell Eco-marathon committee. If this BMS is to be used in commercial applications, the Isolation Switch should be redesigned and implemented using low RDS MOSFETS, as this will dramatically decrease the supply current.

As the driver and transient protection is implemented as part of the Analog Front End, the Isolation Switch circuit is very simple and can be seen in Figure 27

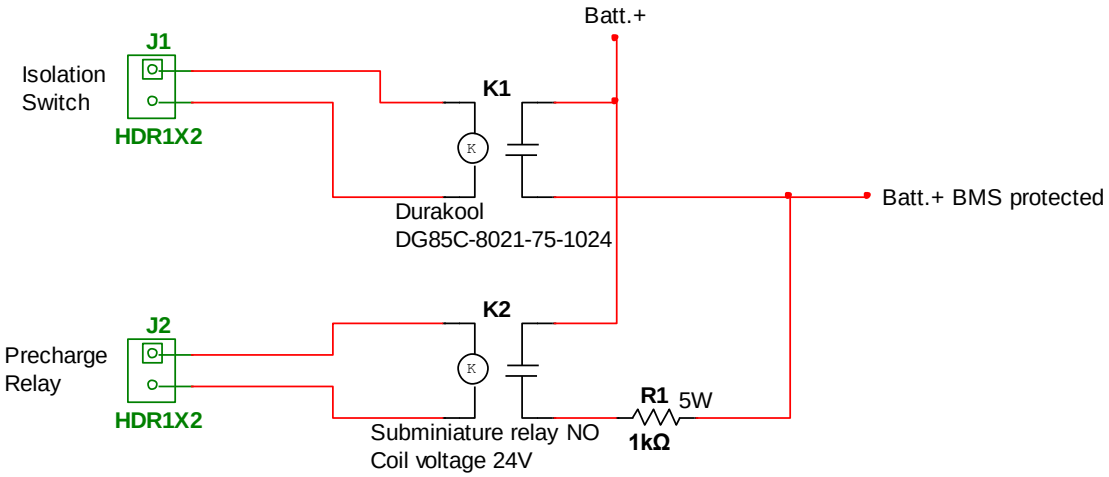



*Figure 27 - Isolation Switch circuit*

**Isolation Switch component description and calculations**

**Relay K1:** Isolation relay performing interruption of battery current flow. Coil voltage: 24V, Max. break current 80A.

**Relay K2:** Pre-charge relay, when closed the load capacity will be charged through R1.

**Resistor R1:** Pre-charge resistor. Limits pre-charge current to $V_{Battery}$/R1.

**Isolation Switch Test and Measurements**

Test of this unit will be performed as part of the accept test. See accept test chapter.

## 3.1.6. Digital Unit (HW)

This Unit consist of a number of circuits, an overview of designed circuits can be seen in Figure 28.

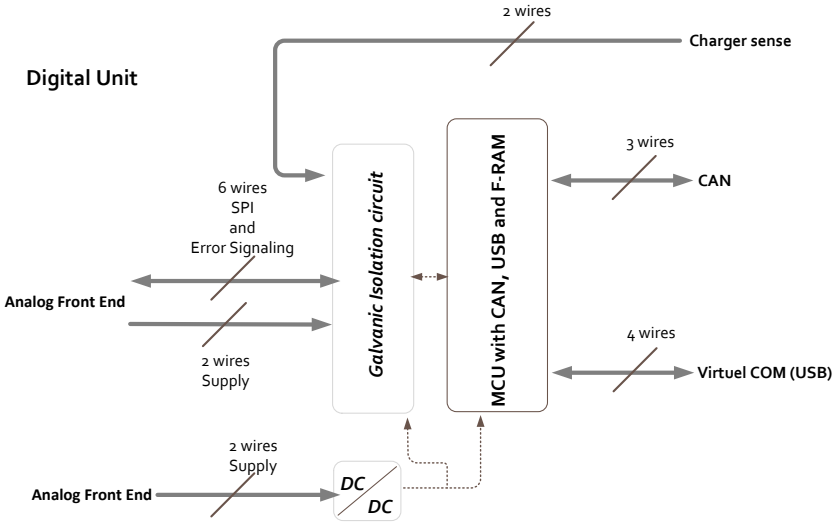



*Figure 28 - Digital Unit circuit blocks*

### 3.1.6.1. Galvanic Isolation circuit

This circuit performs the galvanic isolation between the battery side and the communication side, connected to auxiliary units. A number of techniques can be used to accomplish isolation, these includes the use of digital isolators based on optocouplers, and iCouplers a technology patented by Analog Devices.

The digital isolator ISO7141CC from Texas Instruments and The iCoupler ADuM1401 from Analog Devices has been used to compare technologies.

Digital Isolator(ISO7141CC) pros and cons: High speed can be achieved, however both the dynamic and static supply current at both sides of the isolator are unacceptably high[19].

iCoupler(ADuM1401) pros and cons: Very high speed, low dynamic supply current. Unacceptably high static supply current at both sides of the isolator when not in use[20].

As none of above solutions offers satisfying low power consumption, another approach based on dual optocouplers has been implemented. This allows a design which consumes very little power while in use and next to no power while quiescent.

As it is desirable to be able to drive the light source of the optocouplers directly from the pins of bq76PL536A and the MCU unit, and as low power consumption is required optocouplers with high Current Transfer Ratio(CTR) has been chosen. The optocoupler offers open collector outputs for which the pull-up has been selected based on specific data speed requirements, so that data with less level shifts(e.g. Slave Select) is equipped with a weaker pull-up for reduced consumption. As the SPI bus is shared, an enable functionality is implemented and connected to Slave Select for the Analog Front End, this ensures that the galvanic isolation do not consume power when the SPI bus is used for non-isolated devices.

[19] See " iso7141cc - digital isolator" in appendices
[20] See " ADuM1400_1401_1402 - iCoupler" in appendices

The Galvanic Isolation circuit can be seen in Figure 29.

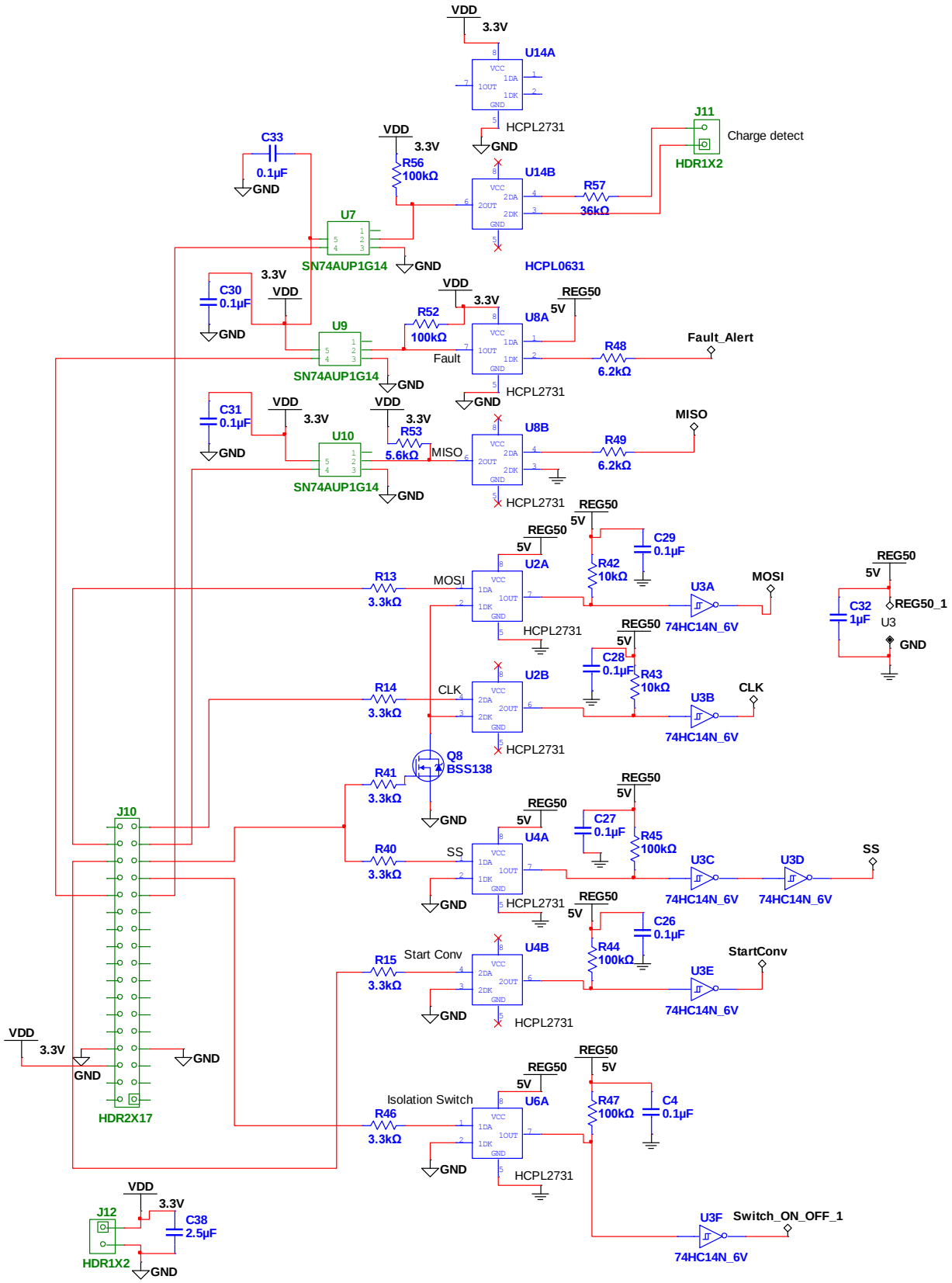



*Figure 29 - Galvanic Isolation circuit*

**Galvanic Isolation component description and calculations**

**Optocouplers U2, U4, U6, U8, U14:** Performs the galvanic isolation, chosen based on low input current requirement, high CTR, relatively high speed and SMD package.

**Resistors R13, R14, R15, R40, R41 and R46:** Determines the forward current of optocoupler LEDs at the MCU side of the galvanic isolation.

$$R = \frac{V_{In_{high}} - V_{forward}}{Required\ I_{forward}} = \frac{3.3V - 1.25V}{0.6mA} \approx 3.3K\Omega\ (rounded\ to\ E24\ value)$$

Where $V_{In_{high}}$ is the voltage of a logic high applied from the MCU, and $V_{forward}$ is the voltage across the LED.

**Resistors R52, 53 and 56:** Pull-up resistors dimensioned so that charge sense and fault, which do not require fast state shift, has weaker pull-up resistors and thereby consumes less power while optocoupler is in saturation mode, compared to the pull-up for the MISO(R53) data signal which has shorter rise and fall times but consumes more power. R53 has been trimmed to match speed of MOSI and CLK isolation stages.

**MOSFET Q8:** Enable/Disable switch which is controlled by SS and ensures that the galvanic isolation is only active when required.

**Resistor R41:** Limits $I_{Gate}$.

**Inverters U7, U9, U10:** Reshapes data(edges are sharpened). And ensures that logic levels are clearly defined.

**Resistors R48, R49 and R57:** Determines the forward current of optocoupler LEDs at the Battery side of the galvanic isolation.

$$R = \frac{V_{In_{high}} - V_{forward}}{Required\ I_{forward}} = \frac{5V - 1.25V}{0.6mA} \approx 6.2K\Omega\ (rounded\ to\ E24\ value)$$

Where $V_{In_{high}}$ is the voltage of a logic high applied from the MCU, and $V_{forward}$ is voltage across the LED.

**Resistors R42, R43, R44, R45 and R47:** Pull-up resistors, for dimensioning see: Resistors R52, 53 and 56

**Inverter U3:** Reshapes data(edges are sharpened). And ensures that logic levels are clearly defined.

**All capacitors:** Decoupling of supply.

**Galvanic Isolation Test and Measurements**

Measurement Figure 30 confirms the expected functionality. Initial tests has been performed with weaker pull-up resistors and thereby faster fall and rise times. However, the performance was then limited by the narrowing of first bit in the first byte to be send, as can be seen in Figure 31 (As the voltage must fall from a higher level when the first bit is transferred, the output rising edge is delayed and thereby the pulse is narrowed). This issue can be solved by decreasing the SPI speed of the first byte, which was successfully implemented. However, the propagation delay then becomes a limitation. The solution has been low data transfer speed, with weak pull-up resistors and thereby low power consumption.

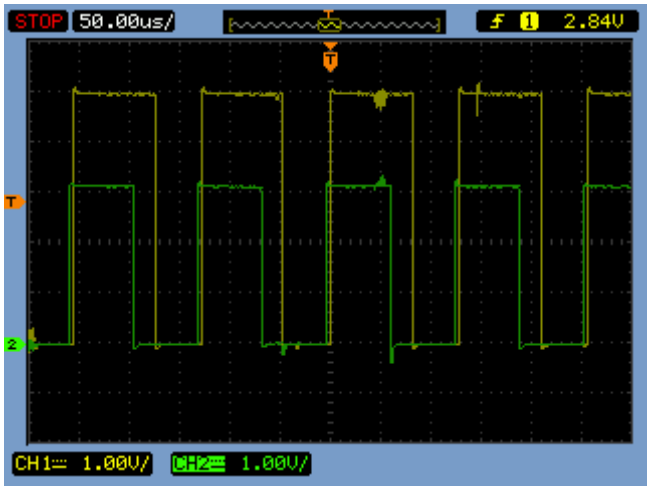



*Figure 30 - Input and output of galvanic isolation (SCLK) (Green = Input)*

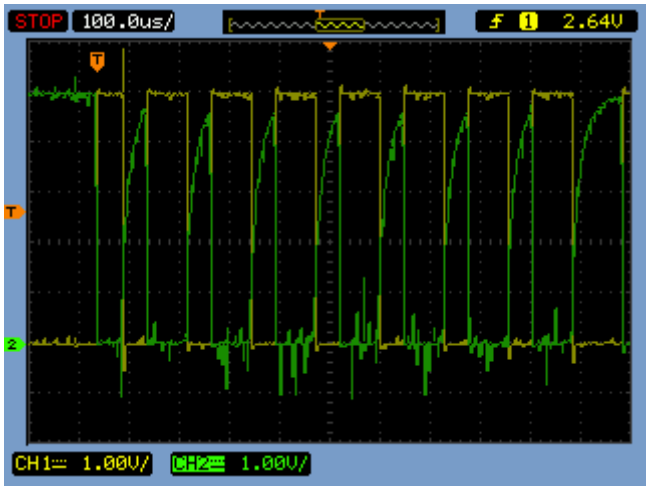



*Figure 31 - Output before and after inverter*

### 3.1.6.2. DC / DC converter

The consumption of this unit is critical, as it must be active at all times(except from low voltage lock-out described later). All prefabricated commercial DC/DC converters has been found to have a high no-load supply current and a too high minimum load requirement for this application. Commercial dc/dc converter comparison can be seen in Table 21($V_{In}$ = 12V for compared converters. However, no 24V version with significantly better performance has been found).

CHARACTERISTICS OF COMMERCIAL DC-DC CONVERTERS

| Manufacturer | Model | Vi (V) | Vo (V) | Io (A) | Ii (Io=0) (mA) | η (%) | Isol. |
|---|---|---|---|---|---|---|---|
| TRACO POWER | TEN 5-1210 | 12 | 3.3 | 1.2 | 20 | 77 | yes |
| XP Power | JCA0412S03 | 12 | 3.3 | 1.2 | 38 | 83 | yes |
| RECOM | RW-123.3S | 12 | 3.3 | 0.7 | 21 | 65 | yes |
| C&D Technologies | HL02R12S05 | 12 | 5 | 0.4 | 40 | 60 | yes |
| BOURNS | MX3A-12SA | 12 | 3.3 | 3.0 | 11 | 93 | no |
| RECOM | R-78A3.3-1 | 12 | 3.3 | 1.0 | 7 | 81 | no |

*Table 21 - Comparison of commercial converters*[21]

To meet the required power consumption an ultra low power DC/DC converter has been designed. As the required output current is below 20mA at all times and only 1/10 of this value most of the time, the no-load quiescent current is of great importance. Two techniques has been used to dramatically decrease the power demand, Pulse Frequency Modulation(PFM) switching(as oppose to more traditional PWM), and regulation without feedback from the secondary side, to eliminate the power consumption associated with the use of optocoupler or transformer feedback. Furthermore the converter is designed to eliminate the need of preloading. The converter has been based on the LT8300, a controller featuring PFM switching(actually it uses a combination of different switching schemes to be exact) , integrated switch and output voltage regulation based on sampling of the primary-side flyback pulse waveform[22]. To keep the size and weight low, and to improve EMC performance, a shielded dual inductor has been used as alternative to a traditional transformer. Low voltage lock-out is implemented and disables the converter, to prevent further discharge of a deeply discharged battery. The implemented circuit can be seen in Figure 32.

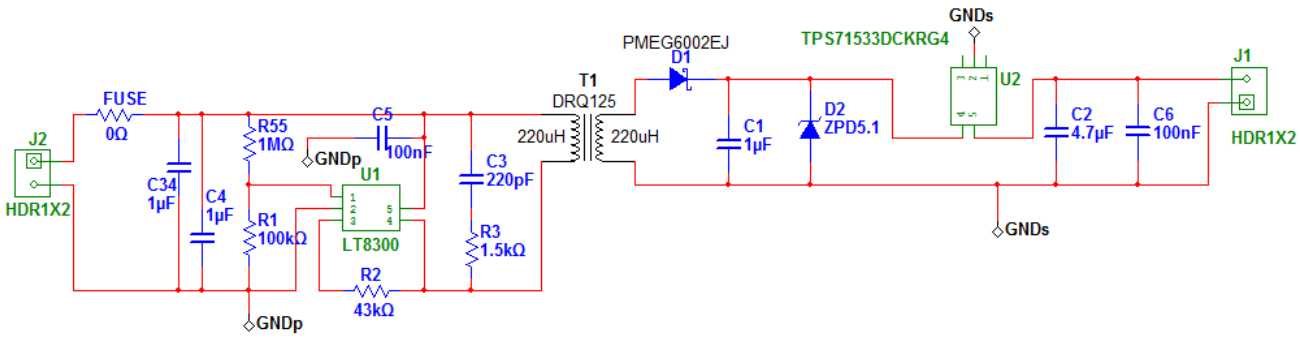



*Figure 32 - DC/DC converter circuit*

[21] Rodrigo et al. date unknown. http://www.icrepq.com/icrepq-08/434-de-diego.pdf (date:14-04-13)

[22] See "LT8300 - flyback converter IC" in appendices

**DC/DC converter component description and calculations**

**Flyback converter controller and switch U1:** Performs and regulates the switching based on primary-side flyback pulse waveforms measured across the switch while OFF.

**Capacitors C34, C4 and C5:** Serves as charge reservoir, to ensure a steady input current flow. And decouples noise present at the supply rail.

**Resistors R1 and R55:** This voltage divider sets the low voltage lock-out threshold and hysteresis. Values has been calculated according to application note:

$$V_{UpperThreshold} = \frac{1.239V*(R55+R1)}{R1} + 2.5uA * R55 = 16.13V$$

$$V_{LowerThreshold} = \frac{1.223V*(R55+R1)}{R1} = 13.45V$$

**RC snubber R3 and C3:** Reduces ringing to improve EMI performance and to avoid false triggering of the boundary mode detector which is a part of the regulation scheme. The capacity has been found empirically by measuring the period of the ringing and subsequently add capacity till the period is doubled[23]. Then the appropriate series resistance has been calculated, using Equation 1.

$$C_{PAR} = \frac{C_{SNUBBER}}{\left(\frac{t_{PERIOD(SNUBBED)}}{t_{PERIOD}}\right)^2 - 1}$$

$$L_{PAR} = \frac{t_{PERIOD}^2}{C_{PAR} \bullet 4\pi^2}$$

$$R_{SNUBBER} = \sqrt{\frac{L_{PAR}}{C_{PAR}}}$$

*Equation 1 - Extracted from LT8300 datasheet page 15*

**Resistor R2:** Feedback resistor, which determines the voltage across C1(output before LDO). Calculated based on datasheet guidelines, subsequently empirically trimmed to $V_{C1}$ = 4V.

**Shielded dual inductor/transformer T1:** Used as 1:1 transformer, lighter smaller and cheaper compared to traditional transformers, the drawback is reduced coil to coil isolation(200Vac).

**Schottky rectifier PMEG6002EJ:** A rectifier with low forward voltage has been selected to decrease loses. Required reverse voltage and forward current has been calculated based on datasheet[24] guidelines.

**Capacitor C1:** Filter capacitor, a low ESR type has been selected to decrease output ripple.

**Zener diode D2:** When the converter is unloaded, the output starts to climb, in this situation D2 will start conduct and thereby act as a light load, which prevent further climbing. This ensures a lower no-load quiescent current compared to a resistive preloading. It does however impose the need of a low drop out regulator at the output.

**LDO U2:** Low dropout regulator, required as technique mentioned above allows some voltage climbing which is not tolerable at the converter output. The dropout is kept low to decrease the negative impact on the efficiency.

**Capacitors C2 and C6:** Required for stable operation of U2 and noise reduction, low ESR/ESL types has been chosen for good HF noise suppression.

[23] Method extracted from LT8300 datasheet.
[24] See "LT8300 - flyback converter IC" in appendices

### DC/DC converter Test and Measurements

For all performed tests $V_{In}$=24V unless otherwise stated.

| Output current | Input current (with snubber) | Input current (without snubber) | Output voltage | Efficiency (with snubber) | Efficiency (without snubber) |
|---|---|---|---|---|---|
| **0 (no-load)** | **0.24 mA** | **0.23 mA** | 3.32V | | |
| 3.3 mA | 1.26 mA | 0.92 mA | 3.32V | 36% | 49% |
| 9.8 mA | 3.42 mA | 2.52 mA | 3.32V | 40% | 54% |

*Table 22 - DC / DC converter results*

**Max. output current:** 50mA

**Min. output current:** 0 (no loading required)

**Voltage lockout:** Upper threshold 16.1V, Lower threshold 13.4V(Converter will shut down when $V_{In}$ drops below 13.4V and assume normal operation when $V_{In}$ raises above 16.1V)

**Max. input voltage:** 55V (calculated value, operation subsequently confirmed by test)

**Measurements to determine necessity of snubber and noise filtering**

RC snubber measurements has been performed during construction, see measurement results below.
All measurements below has been performed with a 1KΩ load at the output.

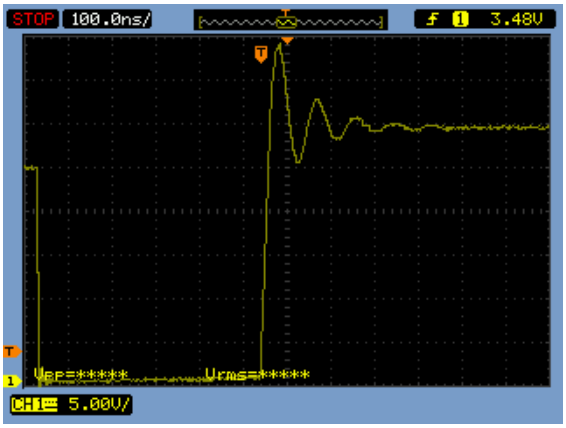



*Figure 33 - Ringing at drain without snubber*

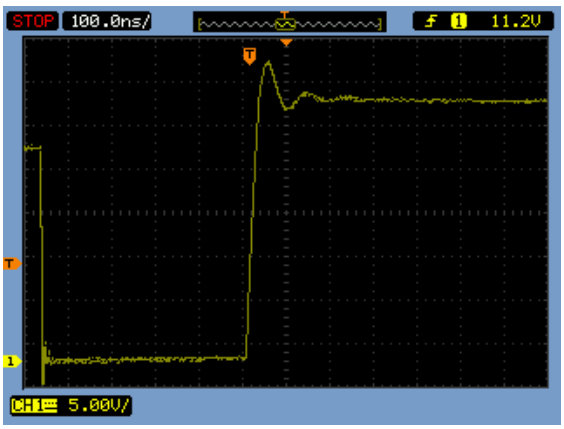



*Figure 34 - Ringing at drain with RC snubber*

To ensure compatibility with connected system units and to test the necessity of snubber the noise performance has been tested. As seen in Figure 35 the switch turn ON(falling edge of Vdrain) at primary side results in ringing at the output. The amplitude of this ringing is not decreased with the presence of a snubber and is dominant compared to the ringing present at switch OFF. Therefore, and because the snubber appeared to only slightly improving the load regulation, the snubber has been removed to improve efficiency.

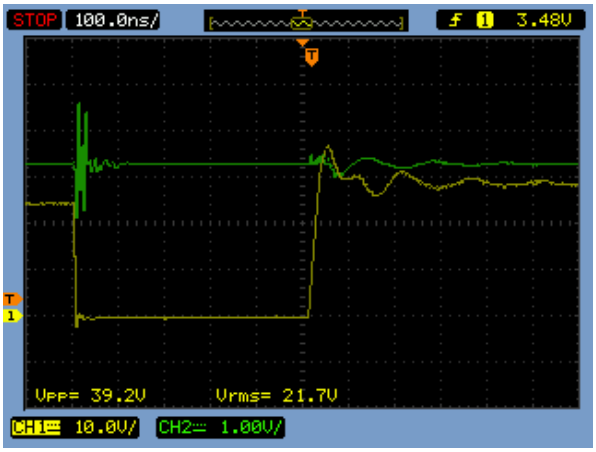



*Figure 35 - Switching noise (yellow = Vdrain, green = Vout)*

The ringing created at switch ON results in a $Vout_{Peak}$ which exceeds the maximum voltage tolerated by the digital circuits which are to be supplied by this dc/dc converter. Therefore filtering has been implemented in terms of a ferrite bead. The output wires are wound two turns around this ferrite bead resulting in a significant reduction as seen in Figure 36 (A 15nF capacitor was mounted across load resistor, to simulate decoupling capacitors present at digital circuits to be supplied).

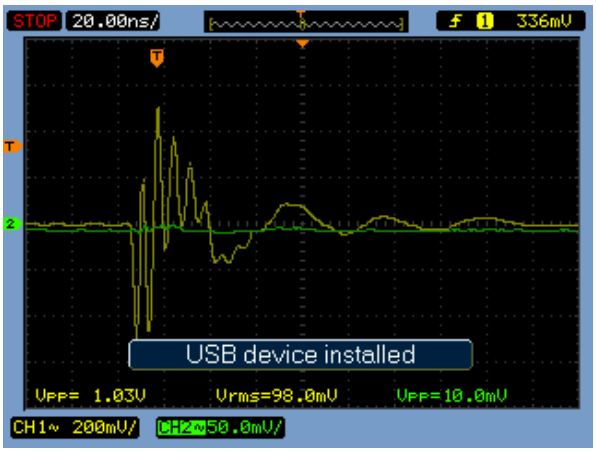



*Figure 36 - Output ringing before and after ferrite bead filtering*

## 3.1.6.3. MCU with CAN, USB and F-RAM

This unit contains a Microcontroller with CAN controller, non-volatile memory and a USB interface. The CAN functionalities of the BMS are rather limited, therefore a mainstream microcontroller like the AVR Mega32 could have been used, as an emulated CAN interface would have been sufficient. However, by using a microcontroller with integrated CAN controller, a platform prepared for future improvements has been created. This is considered useful as implementation of a de facto CAN protocol is considered a necessity if this BMS is to be a commercial success.

As data logging is required, the memory included in the microcontroller is not sufficient, a number of solutions have been considered; SD cards which are cheap but too power consuming and not made for operation in a harsh environment, EEPROM which is non-volatile but have limited write cycles, battery backed-up RAM a reasonable solution but more consuming than the implemented solution which is based on F-RAM. Ferroelectric RAM(F-RAM) offers $10^{14}$ write cycles, very low power consumption between writes and is non-volatile[25]. It is therefore considered the obvious choice in an application where cost is of less concern.

The MCU has been implemented by modifying a OLIMEX AVR-CAN development board[26], The CAN Transceiver has been replaces and a number of unused components has been removed, USB and F-RAM has been added, but is physically located at another PCB. The implemented circuit can be seen in Figure 37 and Figure 38.

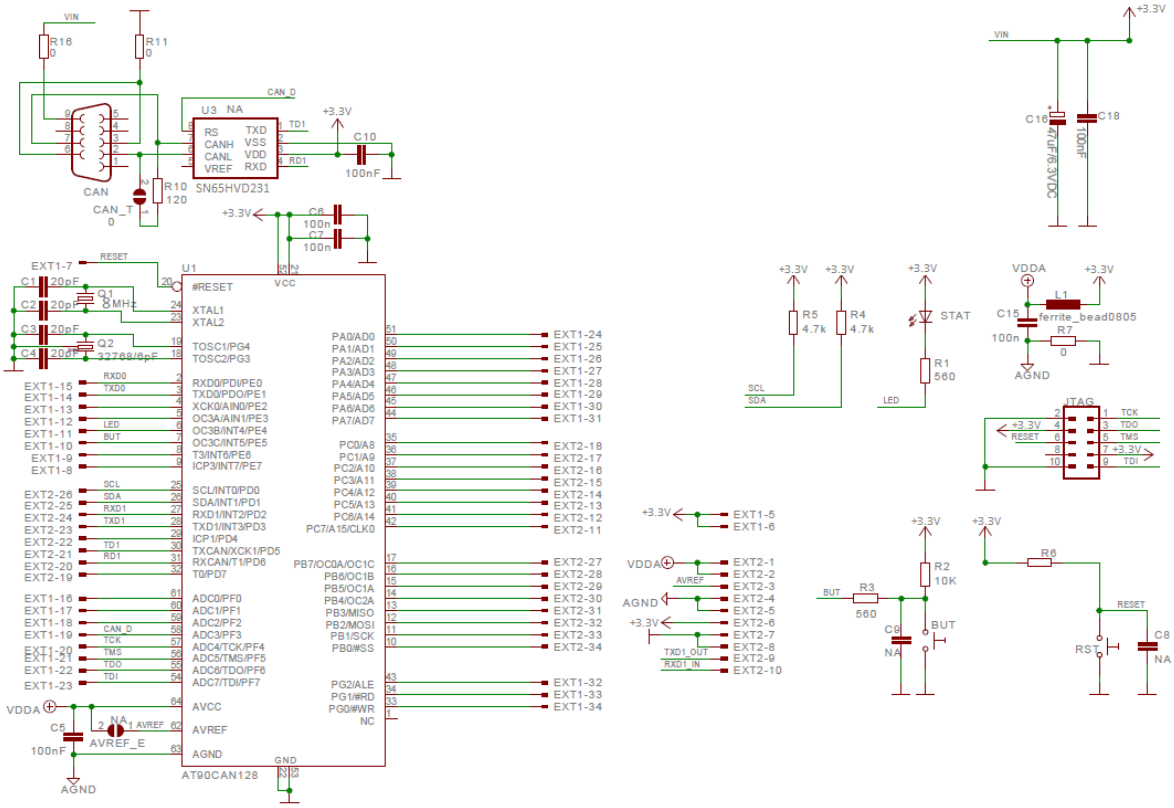



*Figure 37 - MCU and CAN transceiver circuit*

[25] See "FM25V20 - F-RAM memory IC" in appendices
[26] See "AVR-CAN" in appendices

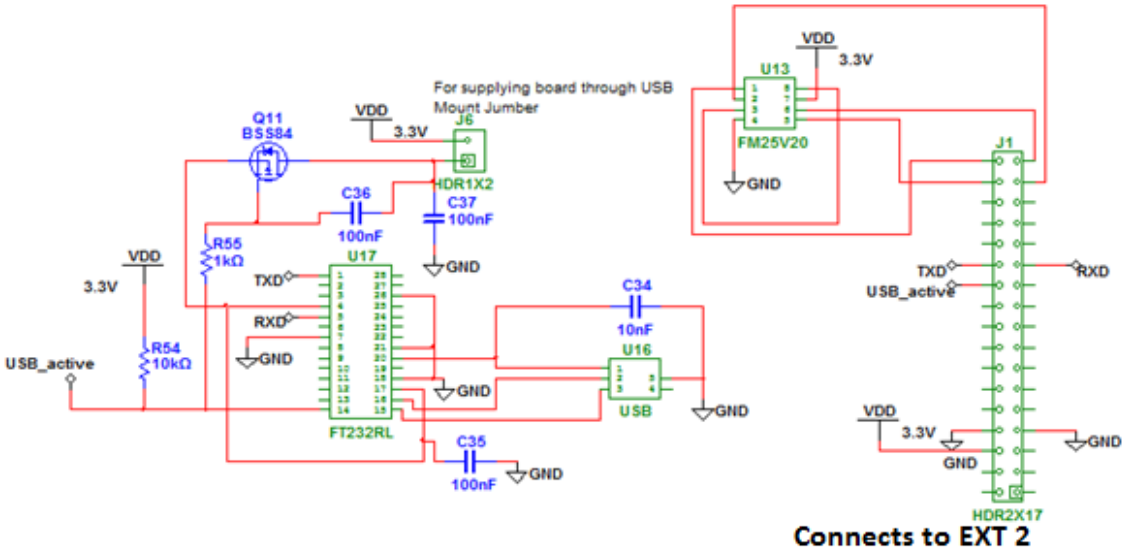
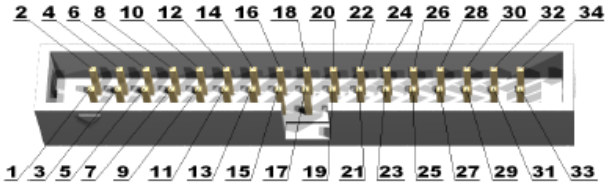



*Figure 38 - USB Interface and F-RAM circuit*




| Pin # | Signal Name | Pin # | Signal Name |
|---|---|---|---|
| 1 | VDDA | 2 | VDDA |
| 3 | AVREF | 4 | AGND |
| 5 | AGND | 6 | +5V |
| 7 | GND | 8 | GND |
| 9 | TXD1_OUT | 10 | RXD1_IN |
| 11 | PC7/A15/CLK0 | 12 | PC6/A14 |
| 13 | PC5/A13 | 14 | PC4/A12 |
| 15 | PC3/A11 | 16 | PC2/A10 |
| 17 | PC1/A9 | 18 | PC0/A8 |
| 19 | T0/PD7 | 20 | RXCAN/T1/PD6 |
| 21 | TXCAN/XCK1/P5 | 22 | ICP1/PD4 |
| 23 | TXD1/INT3/PD3 | 24 | RXD1/INT2/PD2 |
| 25 | SDA/INT1/PD1 | 26 | SCL/INT0/PD0 |
| 27 | PB7/OC0A/OC1C | 28 | PB6/OC1B |
| 29 | PB5/OC1A | 30 | PB4/OC2A |
| 31 | PB3/MISO | 32 | PB2/MOSI |
| 33 | PB1/SCK | 34 | PB0/#SS |

*Figure 39 - MCU EXT2 connector PINOUT*

**MCU with CAN and USB component description and calculations**

**MCU and CAN transceiver:**

**Microcontroller U1:** Microcontroller with CAN controller. An Atmel AVR microcontroller designed for automotive environment.

**CAN Transceiver U3:** Transceiver featuring a ultra low power sleep mode.

**Crystal Q1:** Determines system clock frequency. 8MHz has been selected as it is the lowest frequency still offering high speed CAN communication of 1Mbit/s.

**Crystal Q2:** Determines the frequency of RTC oscillator. 32.768KHz as this value, when applied to the 8bit asynchronous counter, allows real time counting.

**USB interface and F-RAM:**

**USB to UART IC U17:** USB to UART converter, creates a virtual COM port, and converts data voltage levels. In addition, it includes a low dropout regulator($V_{Out}$=3.3V), which allows supply of the entire Digital Unit through USB, this is practical for test and firmware update(Jumper J6 must be mounted for USB supply).

**MOSFET Q11:** Functions as switch which disconnects the regulator of U17 from external circuitry when USB suspend mode is entered, to meet USB specifications(low supply current is mandatory in suspend mode). **Capacitor C36:** In cooperation with R55 it creates a gradual turn ON of Q11. Recommended by the supplier of U17 to avoid Reset of the IC as a result of voltage sag created by inrush current peak.

**USB socket U16:** Mini USB socket.

**F-RAM U13:** F-RAM IC with SPI interface and sleep mode feature.

## 3.2. Software

This paragraph documents the implemented SW, including descriptions of methods used to accomplish the functionalities outlined in the system architecture. Firstly a brief description of considerations behind the implemented SW will be presented, followed by a presentation of Classes and Methods. Last the source code implementation will be described, including a description of which approach has been used to accomplish the required functionalities. Source code snippets will be presented where considered relevant, but for a full overview the reader is advised to study the source code, included in appendices.

### 3.2.1. General SW Considerations

As specified in the System Architecture, power consumptions must be taken into consideration, meaning code must be efficient, so that it can be quickly executed, and thereby allow the Microcontroller maximum sleep time. Furthermore dynamic system clock prescaling has been used, to reduce power consumption, while waiting for SPI communication to be executed. In addition, to further reduce consumption, the measurement rate will dynamically change based on necessity to acquire new data, if current is changing rapidly or if any parameter is near its limit, the speed of which new data is collected will be increased.

As time is a limited resource and to allow increased focus on implementation of safety critical functions, standard libraries available from Atmel, has been used where considered beneficial. To ensure that a functional system was available before the Eco-marathon(13.May), all functionalities needed to meet Shell Eco-marathon driven requirements, where implemented first, and features with no direct influence on the performance, such as data logging was implemented after the Eco-marathon participation.

## 3.2.2. Class Diagram

The class diagram can be seen in Figure 40.

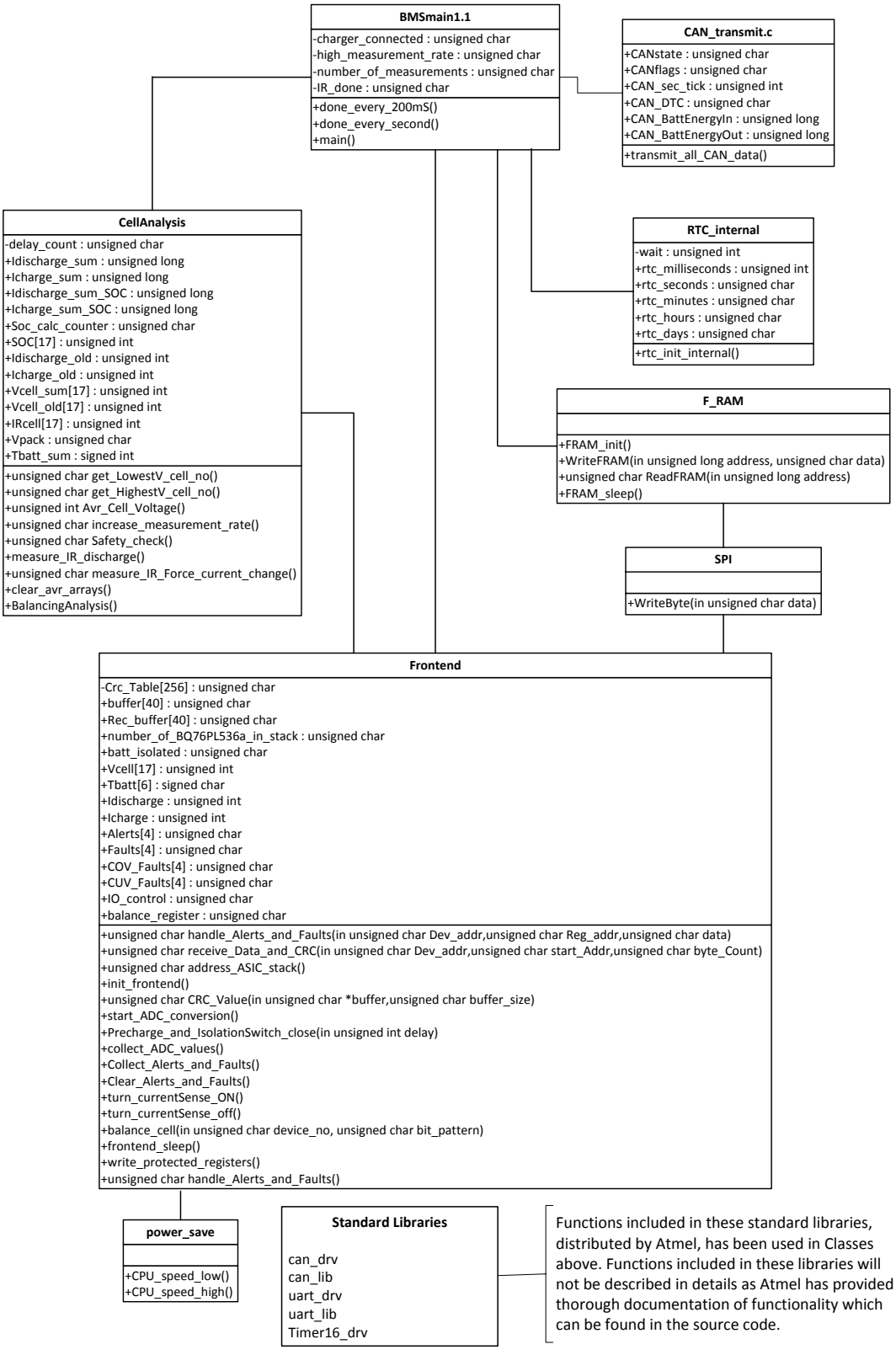



*Figure 40 - Class Diagram for software embedded in BMS*

## 3.2.3. Class and Functions Descriptions

In this paragraph functionalities of each Class has been described, followed by descriptions of functions included in the class.

### BMSmain1.1.c

Includes the Main function from which all initialization is done by calling relevant functions. In addition, it includes a number of interrupt routines executed with fixed time intervals.

**Function Description**

| Function: | void main (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Main function of the program. Performs initializing, sets sleep mode and goes to sleep, as other functions are interrupt driven. |

**Function Description**

| Function: | ISR (Timer2_COMP_vect) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Timer interrupt routine executed every 200ms. Increments RTC ticks and calls done_every_mS() and done_every_second() with correct time intervals. |

**Function Description**

| Function: | void done_every_200mS (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Function is called from RTC timer interrupt and executes every 200ms. If high measurement rate is active, measurements and safety check will be performed. |

**Function Description**

| Function: | void done_every_second (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Function is called from RTC timer interrupt and executes every second. It is responsible of calling functions performing data collection and calculations. If charger is connected a balancing algorithm is applied when needed. Subsequently CAN function is called. |

**Function Description**

| Function: | ISR (INT0_vect) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | External interrupt triggered by Fault or Alert output from Analog Front End. handle_Alerts_and _Faults() is called from this interrupt routine. |

**Function Description**

| Function: | ISR (INT1_vect) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | External interrupt triggered by charger connection, used to wake device from sleep. A charger flag is set to inform other functions that charger is connected. |

## Frontend.c

Includes functions to setup and perform communication with Analog Front End, including more sophisticated functions to perform addressing of devices(bq76PL536A IC) and autonomous handling of faults and alerts reported to the Digital Unit.

**Function Description**

| Function: | void Send_Data_and_CRC (unsigned char Dev_addr, unsigned char Reg_addr, unsigned char data) |
|---|---|
| Parameters | Address of device(bq76PL536A IC)<br>Address of register to be written<br>Data to be written |
| Return Value | None |
| Description of function | Sends data to specified address, followed by calculated checksum. |

**Function Description**

| Function: | Unsigned char Receive_Data_and_CRC (unsigned char Dev_addr, unsigned char start_Addr, unsigned char byte_Count) |
|---|---|
| Parameters | Address of device(bq76PL536A IC)<br>Address of first register to be read<br>Number of registers to be read |
| Return Value | CRC error(0 if successfully received) |
| Description of function | Receives specified number of data bytes from specified start register. CRC check is performed and result presented by return value. |

**Function Description**

| Function: | unsigned char Address_ASIC_stack (void) |
|---|---|
| Parameters | None |
| Return Value | Number of present devices(bq76PL536A ICs) (depends on number of connected extension modules) |
| Description of function | Assign addresses to connected devices, and clear address error flag. Warn user via UART if errors detected. |

**Function Description**

| Function: | void init_frontend (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Initializes ports, calls Adress_ASIC_stack(), and setups a number of registers in Analog Front End to configure ADC, balancing, protection limits etc. |

**Function Description**

| Function: | unsigned char CRC_Value (unsigned char *buffer, unsigned char buffer_size) |
|---|---|
| Parameters | Pointer to array to be calculated<br>Size of array to be calculated |
| Return Value | Calculated CRC value. |
| Description of function | Performs CRC calculation. Look-up table is used to improve speed. |

**Function Description**

| Function: | void start_ADC_conversion (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Enables temperature sensor and starts a new ADC conversion. |

**Function Description**

| Function: | void Precharge_and_IsolationSwitch_close (unsigned int delay) |
|---|---|
| Parameters | Delay[ms] from pre-charge relay is closed to Isolation Switch closes |
| Return Value | None |
| Description of function | Enables pre-charge circuit, waits specified time and closes Isolation Switch. |

**Function Description**

| Function: | void collect_ADC_values (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Collects all measured values and places these in dedicated arrays. |

**Function Description**

| Function: | void Collect_Alerts_and_Faults (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Collects alert and fault register values from all devices(bq76PL536A ICs). Values are placed in dedicated arrays. |

**Function Description**

| Function: | void Clear_Alerts_and_Faults (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Clear all alerts and faults in Analog Front End. |

**Function Description**

| Function: | void turn_currentSense_ON (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Turns current sensor supply voltage ON. |

**Function Description**

| Function: | void turn_currentSense_off (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Turns current sensor supply voltage OFF. |

**Function Description**

| Function: | void balance_cell(unsigned char device_no, unsigned char bit_pattern) |
|---|---|
| Parameters | Address of device(bq76PL536A IC), value indicating which balancing outputs to enable. |
| Return Value | None |
| Description of function | Controls balancing outputs, and thereby balancing MOSFETs. |

**Function Description**

| Function: | void frontend_sleep(void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Puts all devices(bq76PL536A ICs), to sleep. And opens Isolation Switch, as all protection features are disabled in sleep mode. |

**Function Description**

| Function: | void write_protected_registers (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Overwrites values in protected registers. These values specifies threshold values of redundant protection and ADC configuration. |

**Function Description**

| Function: | unsigned char handle_Alerts_and_Faults (void) |
|---|---|
| Parameters | None |
| Return Value | For future use |
| Description of function | Handles error condition, when possible the error is automatically removed. |

## CellAnalysis.c

Includes functions to analyze cell and battery conditions.

**Function Description**

| Function: | unsigned char get_LowestV_cell_no (void) |
|---|---|
| Parameters | None |
| Return Value | Number indicating which cell has the lowest voltage(range: 1 to highest cell number in stack of cells) |
| Description of function | Find out which of the connected cells has the lowest voltage. |

**Function Description**

| Function: | unsigned char get_HighestV_cell_no (void) |
|---|---|
| Parameters | None |
| Return Value | Number indicating which cell has the highest voltage(range: 1 to highest cell number in stack of cells) |
| Description of function | Find out which of the connected cells has the highest voltage. |

**Function Description**

| Function: | unsigned int Avr_Cell_Voltage (void) |
|---|---|
| Parameters | None |
| Return Value | The average cell voltage [mV] |
| Description of function | Returns the average voltage of cells. As the sum of cell voltages is found as part of the calculation, the battery pack voltage is also found and placed in a global variable. |

**Function Description**

| Function: | unsigned char increase_measurement_rate (void) |
|---|---|
| Parameters | None |
| Return Value | Number indicating which condition imposes the need of increased measurement rate (0 if no warnings) |
| Description of function | Analyses if any value(e.g. cell voltage) is close to its threshold or if current is rapidly changing. |

**Function Description**

| Function: | unsigned char Safety_check (void) |
|---|---|
| Parameters | None |
| Return Value | Number indicating which condition exceeded its safe level(0 if none) |
| Description of function | Analyses if any value(e.g. cell voltage) exceeded the allowed level, and Isolates battery, by opening the Isolation Switch, if level exceeded. |

**Function Description**

| Function: | void measure_IR_discharge (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Measures Internal Resistance(IR) during discharge. This function is only called when a large change in current has been detected. The calculated IR values are placed in a dedicated array (IR of cell 1 is placed at index 1 etc.) |

**Function Description**

| Function: | unsigned char measure_IR_Force_current_change (void) |
|---|---|
| Parameters | None |
| Return Value | Returns 1 when IR measurement has been performed. |
| Description of function | Measures Internal Resistance(IR) during charge. A large current change is achieved by interrupting the charging current for a short period. This function is called at a fixed SOC, so that conditions are similar each time to allow comparison. The calculated IR values are placed in a dedicated array (IR of cell 1 is placed at index 1 etc.) |

**Function Description**

| Function: | void clear_avr_arrays (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Clears arrays used during analysis. |

**Function Description**

| Function: | void BalancingAnalysis (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Analyses which cells has the highest SOC based on IR compensated voltage(OCV). And performs required balancing by turning ON bleeder resistors for cells with highest SOC. |

## RTC_internal.c

Includes a function to enable use of Timer2 as Real Time Counter.

**Function Description**

| Function: | void rtc_init_internal(void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Initializes Timer2 for use as RTC, including configuration of oscillator(32.768kHz), and required interrupt enabling. |

## F_RAM.c

Includes functions to communicate with external memory, and perform initialization of memory IC.

**Function Description**

| Function: | void FRAM_init (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Initializes F-RAM IC and port used for communication. |

**Function Description**

| Function: | void WriteFRAM (unsigned long address, unsigned char data) |
|---|---|
| Parameters | Address of register to be written<br>Data to be written |
| Return Value | None |
| Description of function | Writes a data byte to specified address. |

**Function Description**

| Function: | unsigned char ReadFRAM (unsigned long address) |
|---|---|
| Parameters | Address of register to be read |
| Return Value | Data |
| Description of function | Returns data located at address specified by parameter. |

**Function Description**

| Function: | void FRAM_sleep (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Puts F-RAM IC to sleep(ultra low power consumption). |

## power_save.c

Includes functions to scale system frequency. Used to reduce power consumption when high speed is not required.

**Function Description**

| Function: | void CPU_speed_low (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Scales system oscillator frequency down to 1MHz. Decreases speed of program execution but also power consumption. Used when CPU waits for slow SPI communication with Analog Front End. |

**Function Description**

| Function: | void CPU_speed_high (void) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Sets system frequency prescaler to 1, resulting in frequency of 8MHz. |

## SPI.c

Includes a function to write data byte via SPI, this function is shared by F_RAM.c and Frontend.c. A read function is not included here as reads are performed by doing a dummy write(sending 0's) and reading the SPI data register(SPDR).

**Function Description**

| Function: | void WriteByte(unsigned char data) |
|---|---|
| Parameters | Data |
| Return Value | None |
| Description of function | Sends data via SPI interface. Low level function which places data in SPI data register(SPDR), function does not perform Slave Select or SPI speed configuration. |

## CAN_transmit.c

Includes a function which prepares and send data via CAN interface.

**Function Description**

| Function: | void WriteByte(unsigned char data) |
|---|---|
| Parameters | None |
| Return Value | None |
| Description of function | Data is placed in the Message Object buffers(MObs) of the can controller and send via CAN bus interface. |

## Standard Drivers

To ease the implementation of UART and CAN communication a number of standard libraries distributed by Atmel has been used. The functionalities performed by these libraries are briefly described below, see the source code included in appendices for details.

**uart_lib.c:** Used for UART initialization. And transmission of data via UART.

**uart_drv.h:** Includes driver functions used by uart_lib.c.

**timer16_drv.c:** Used by uart_drv.h.

**can_lib.c:** Used for transmission of data via CAN.

**can_drv.c:** Includes functions used by can_lib.c, and functions used for enabling/disabling CAN and perform initialization.

## 3.2.4. Implementation of Software

In this paragraph the implementation of classes, which functionalities is defined in paragraph 3.2.3, is described. Considerations behind chosen solutions, elaborated flow charts and snippets of source code will be presented.

### BMSmain1.1.c

As execution of functions is interrupt driven to save power, the main program only needs to perform the initialization of interfaces and functionalities and then put the Microcontroller into sleep mode. After ended execution of interrupts the Microcontroller is put back to sleep. The execution flow can be seen in Figure 41.

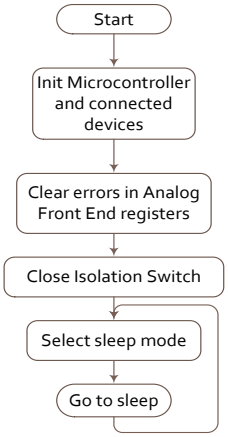



*Figure 41 - Flow description of: void main (void)*

Furthermore, the BMSmain1.1c file includes interrupt driven functions. which performs operations with fixed time intervals and detection of charger, as well as detection of Fault/Alert signal from Analog Front End. The execution flow of these has been described below.

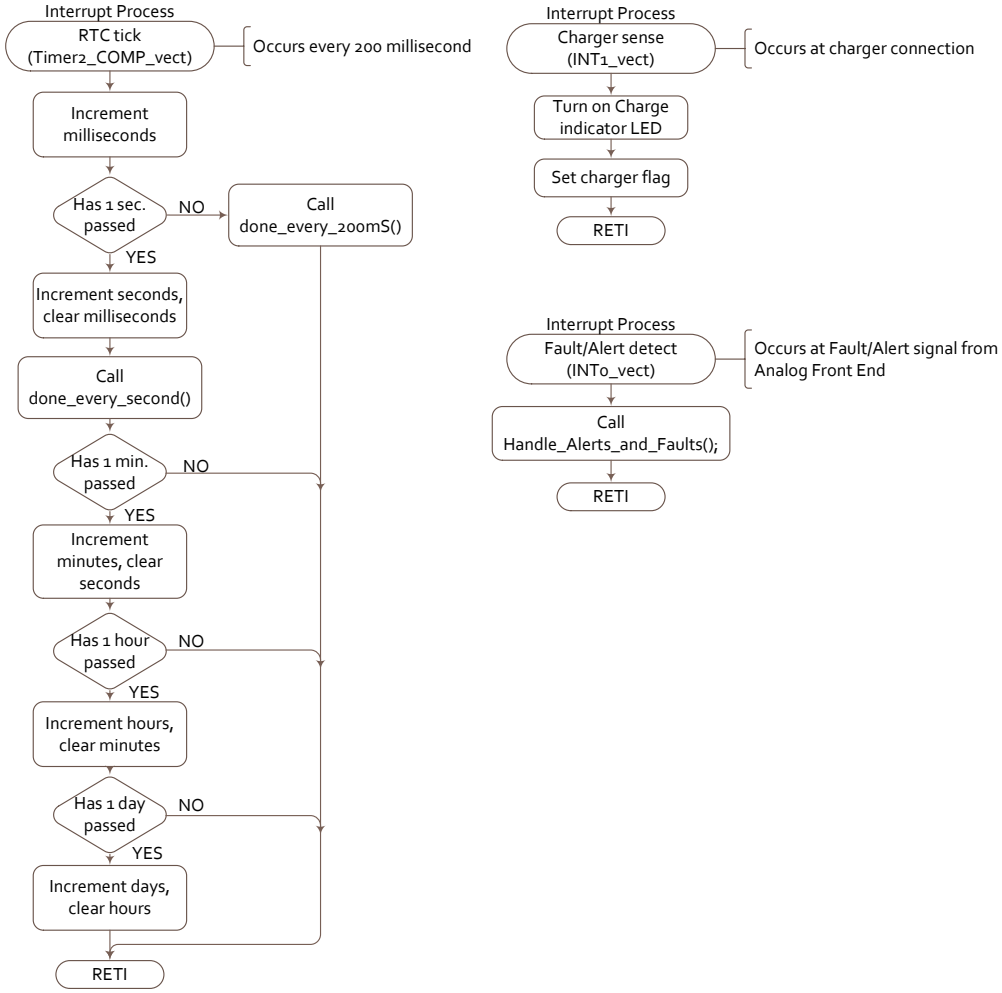



*Figure 42 - Interrupt routines included in BMSmain1.1.c*

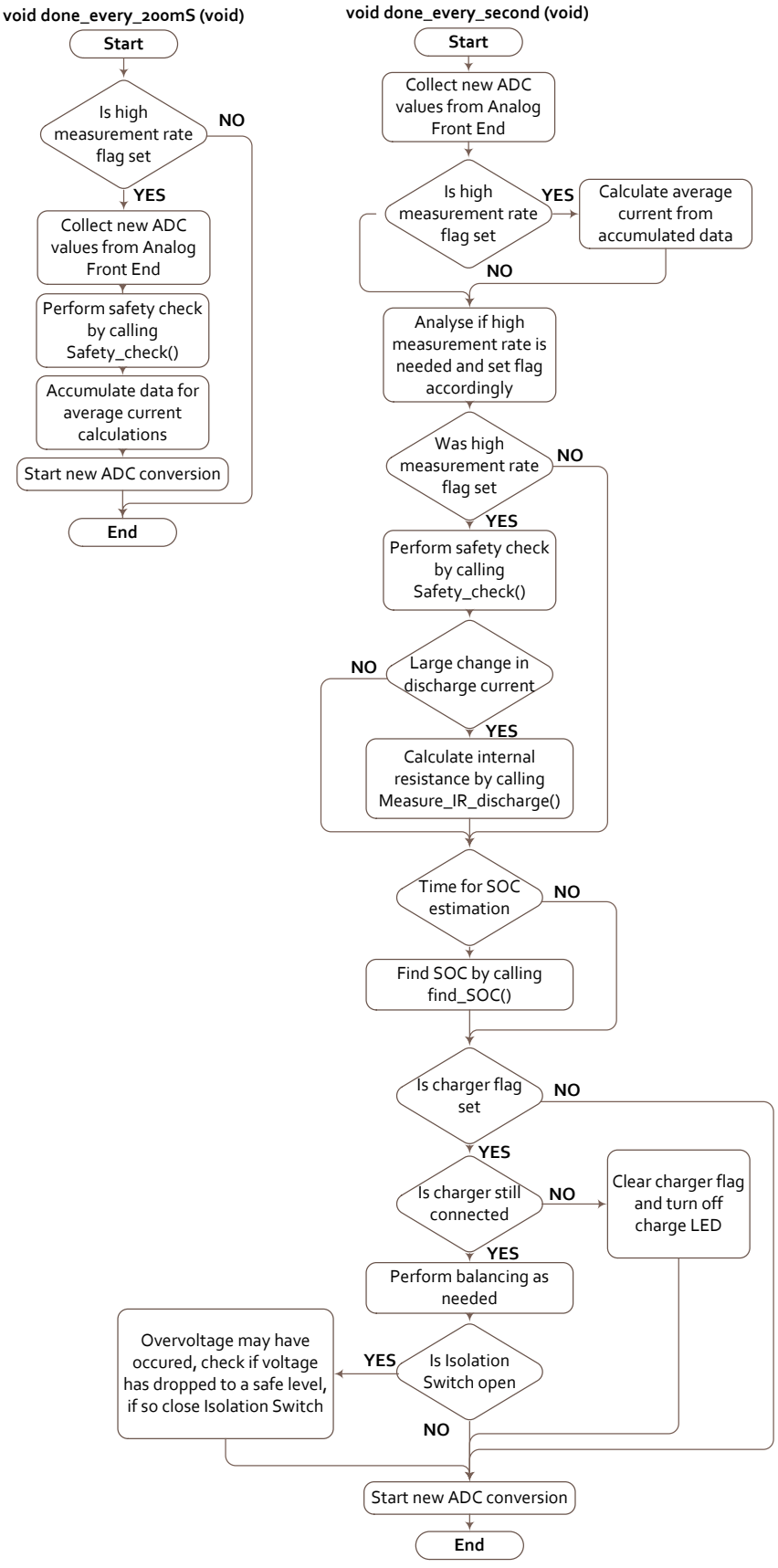



*Figure 43 - Functions called from RTC interrupt, included in BMSmain1.1.c*

## Frontend.c

A stable connection between the Analog Front End and the Digital Unit is vital to ensure proper operation of the BMS, therefore error checking and automatic handling of certain errors has been implemented. As an example the source code for the bq76PL536A addressing process has been shown in Figure 44, firstly the program checks the SPI connection and warn the user via USB interface if no Analog Front End is found, secondly all connected bq76PL536As are addressed if the address register returns a zero and no CRC errors are detected. The addressing is subsequently checked by reading a specific register of the bq76PL536A. If any errors occurs during addressing, the user is informed for which bq76PL536A the assignment of address has failed. After successful addressing the user is informed how many cells are expected by the BMS.

```
//Check ASIC SPI connection by reading address register
CRC_error = receive_Data_and_CRC(0x00,0x3b,1);
//if error, try again
if(CRC_error)
{
    _delay_ms(1);
    CRC_error = receive_Data_and_CRC(0x00,0x3b,1);
    uart_mini_printf ("\rCRC ERROR. Please check connection to analog frontend\r\n");
}

//Assign addresses until all assigned
while(Rec_buffer[0] == 0x00 && CRC_error == 0 && ASIC_count <= ASIC_max)
{
    ASIC_count++;
    send_Data_and_CRC(0x00,0x3b,ASIC_count);
    //Check that assignment has been performed
    receive_Data_and_CRC(ASIC_count,0x3b,1);
    if (Rec_buffer[0] == (ASIC_count|0b10000000))
    {
        uart_mini_printf ("\rAddress successfully assigned to BQ76PL536a no.: %u\r\n",ASIC_count);
    }
    else
    {
        //Error in assigning address, warn user through UART
        uart_mini_printf ("\rError occurred while assigning address to BQ76PL536a no.: %u ==\r\n",ASIC_count);
        //return 0 and exit
        return (0);
    }

    //Check for next unaddressed ASIC
    CRC_error = 1;
    CRC_error = receive_Data_and_CRC(0x00,0x3b,1);
}
uart_mini_printf ("\r  %u Front End module(s) has been detected, connect up to %u battery cells\r\n",ASIC_count,(ASIC_count*6));

// Clear Address error flag, as address has now been assigned
send_Data_and_CRC(0x3f,0x20,0b10000000);
send_Data_and_CRC(0x3f,0x20,0b00000000);
```

*Figure 44 - Addressing of bq76PL536As  contained in the Analog Front End*

## CellAnalysis.c

Contains function to analyze cell and battery parameters, such as SOC, lowest and highest cell voltage, as well as a balancing function, performing balancing when needed.

**SOC estimation**

As described in the project report, a number of techniques can be used. A combination of coulomb counting and voltage based estimation has been implemented, as this combination reduces the drift issues imposed by coulomb counting and the issues related to the rather flat voltage plateau around

SOC=50%. When the SOC is high a piecewise linear relation[27] between calculated Open Circuit Voltage(OCV) and SOC is used to determine SOC, while coulomb counting is used for the flat region of the voltage curve. At SOC = 0 the voltage based method is applied to reset the coulomb counting. The applied technique has been illustrated in Figure 45 and Figure 46.

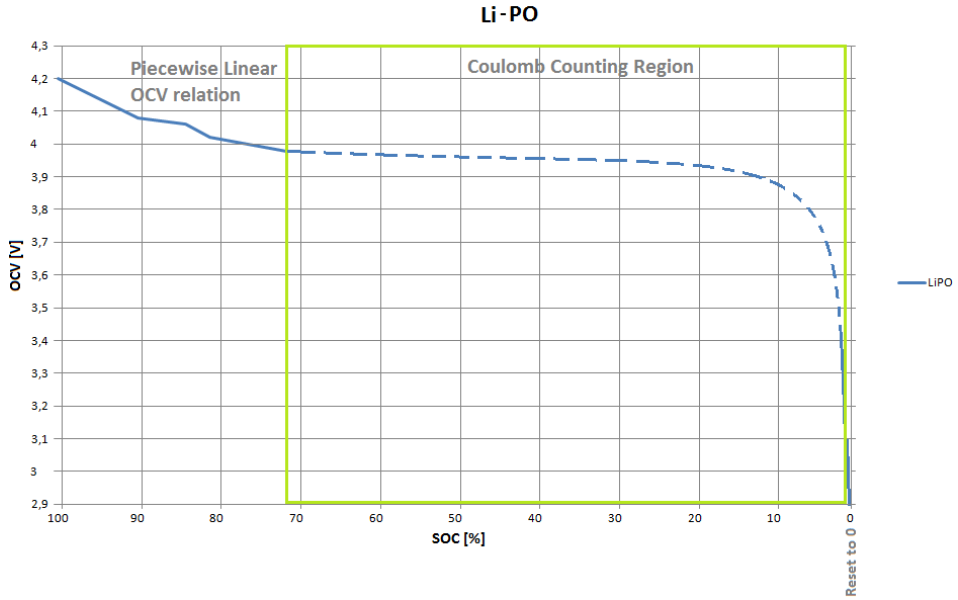



*Figure 45 - Illustration of applied mixed SOC estimation methods*

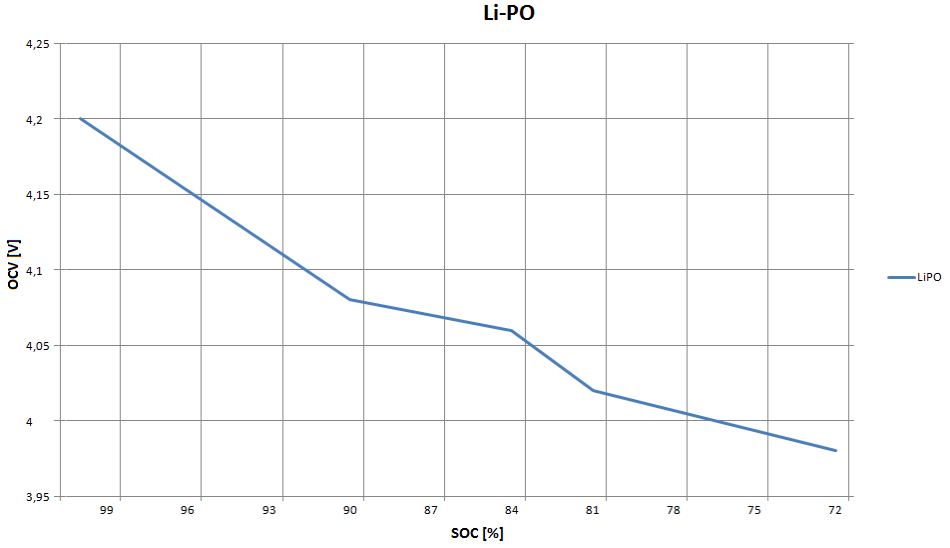



*Figure 46 - Piecewise Linear OCV/SOC relation (zoomed)*

[27] Derived from: Valer Pop et al. " Battery Management Systems: Accurate State-Of-Charge Indication for Battery Powered Applications" Page29

**Internal Resistance**

From the voltage change imposed by a change in current the resistance can be found as $IR_{Cell} = \frac{|\Delta V_{Cell}|}{|\Delta I|}$, this calculation is performed when a significant change in current is detected. A threshold has been introduced, so that large changes at a small current draw are ignored. The performed operation can be seen in Figure 47 and Figure 48.

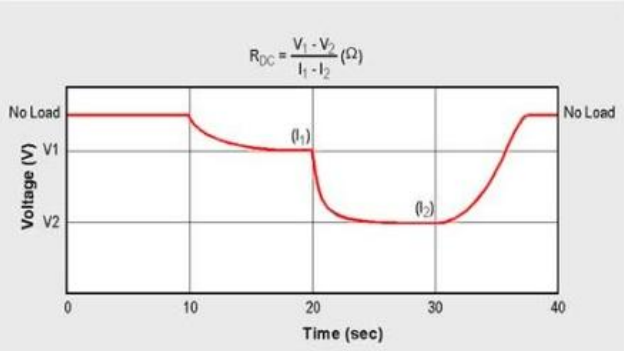



*Figure 47 - Illustration of method*[28]

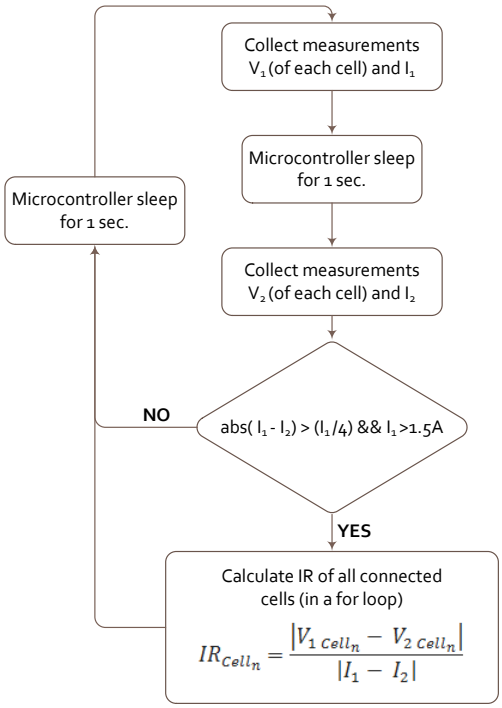



*Figure 48 - implemented IR calculation*

[28] http://largebattery2012.fotopages.com/?&page=15 (Date:08-06-2013)

**Balancing**

Pros and cons of available balancing methods has been discussed in the project report. The implemented method is based on a voltage based method. When a charger is applied the voltage increase created by the charging current is proportional to the internal resistance, therefore direct comparison of cell voltages would lead to balancing based on internal resistance and not SOC. To avoid this the OCV is calculated from the measured cell voltage, charging current and internal resistance as; $OCV_{Cell_n} = V_{Cell_n} - IR_{Cell_n} * I_{Charge}$.

To allow longer time for balancing than achieved with a final voltage algorithm[29] the method shown in Figure 49 has been applied. The system has been prepared for SOC history based balancing, as individual SOC of each cell is calculated. An upgrade to SOC history based balancing will be beneficial if the BMS is to be used with cells of larger capacity, as this allows balancing at all times not only at high SOC.

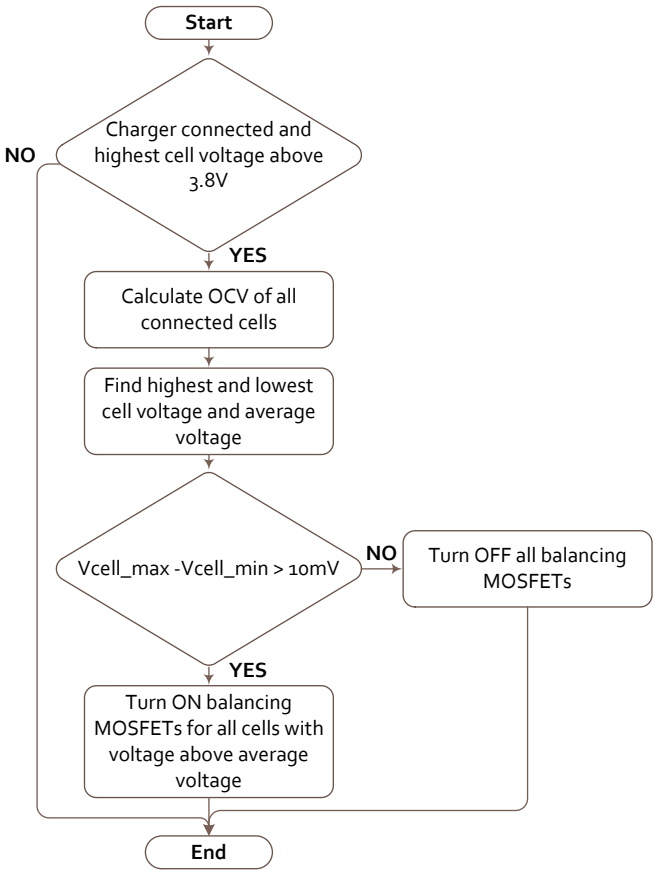



*Figure 49 - applied balancing method*

[29] See "Battery Management Systems for Large Lithium Ion Battery Packs" (page 66)

## RTC_internal.c

A special procedure following Atmels guidelines[30] has been used during oscillator shift to prevent register corruption. See code snippet in Figure 50.

```
void rtc_init_internal(void)
{

    unsigned int wait;

    //init procedure following AT90CAN128 guidelines to avoid register corruption at oscillator shift
    for (wait=0;wait<0xFFFF;wait++);//-- Waiting to let the Xtal stabilize after a power-on
    TIMSK2 &= ~0b00000011;          //disable timer interrupts
    ASSR  =  (ASSR & ~(1<<EXCLK)) | (1<<AS2); //-- Init RTC clock for 32.768 KHZ external XTAL
    TCCR2A=0; TCNT2=0; OCR2A=0;     //-- Timer 2 cleared & "OFF"
    TCCR2A |= (1<<WGM21);           //-- CTC mode
    OCR2A = 50;                     //--compare register set for match every 200 msec.
    TCCR2A |= 0x05;                 //--prescaler 64, start count
    while ( ASSR & ( (1<<TCN2UB) | (1<<OCR2UB) | (1<<TCR2UB) ) )//--wait while busy
    {}
    TIFR2 |=  (1<<OCF2A);           //-- Clear Output_Compare Interrupt-flags

      //-- Time setting
      rtc_milliseconds = 0;
      rtc_seconds      = 0;
      rtc_minutes      = 0;
      rtc_hours        = 0;
      rtc_days         = 0;

    TIMSK2 |= (1<<OCIE2A);          //-- Enable Compare interrupt
}
```

*Figure 50 - Initializing counter for RTC use*

[30] See, bq76PL536A - Battery monitor and secondary protection, in appendices

## F_RAM.c

The memory IC supports a high data rate. Therefore the implemented functions increments SPI speed when communication with the F-RAM IC is being performed. As the address is to be send as 3 bytes, bit shifting is performed as part of the send and receive functions. See example in Figure 51.

```
unsigned char ReadFRAM(unsigned long address)
{
    unsigned char addressMSB;
    unsigned char addressMLSB;
    unsigned char addressLSB;

    // Change to high SPI speed
    FRAM_SPI_speed

    // Enable F-RAM (SS low)
    FRAM_enable

    // Convert address to 3 bytes
    addressLSB = address;
    addressMLSB = address>>8;
    addressMSB = address>>16;

    // Send read command
    WriteByte(0b00000011);

    // Send address to be read
    WriteByte(addressMSB);
    WriteByte(addressMLSB);
    WriteByte(addressLSB);

    // Send "dummy byte" (to generate 8 clock periods)
    WriteByte(0x00);

    // Disable F-RAM (SS high)
    FRAM_disable

    // Read and return the received data byte
    return(SPDR);
}
```

*Figure 51 - Read a specified byte from the F-RAM memory*

## power_save.c

The CLKPR register of the AT90CAN128 is used to perform scaling of system clock speed, see Figure 52.

```
void CPU_speed_low(void)
{
    //enable change of Clk prescaler
    CLKPR = 0b10000000;
    //Set prescaling to  (resulting in cpu speed 1MHz)
    CLKPR = 0b00000011;
    _delay_ms(1);
}
```

*Figure 52 - Down scaling of system clock speed*

## SPI.c

The SPI communication function, contained in this class, is implemented so that it makes use of the dedicated SPI register of the AT90CAN128.

## CAN_transmit.c

This function has been implemented so that it makes use of the integrated CAN controller and drivers from Atmel to place data in Message Object buffers(MObs) and send this data. All data is first prepared and placed in arrays named after their CAN address location. Subsequently MObs are cleared and new data is placed and send.

# 3.3. Physical System Realization

As the system is operating in a harsh automotive environment, effort has been put into ensuring robustness in both the design phases and the physical realization phase. This paragraph will document the physical realization including PCB layout, BMS and battery cabinet, vehicle integration, as well as presenting complete system schematics.

## 3.3.1. PCB Layout

A four layer PCB with full ground plane layer has been designed, as this ensures the lowest possible impedance of the return path, and gives a shielding effect. Below the ground layer a full power plane ensures a clean and low impedance supply, shielded from high frequency traces at the top layer. The top layer can be seen in Figure 53, see all layers in appendices.

Heat from balancing resistors is transferred, via thermal vias, to wide traces at the bottom layer.

A thermal pad below the bq76PL536A ensure heat transfer and proper grounding.

All decoupling and filter components have been located very near to their respective ICs.

A SPI test connector has been inserted to ease fault finding procedures(Compatible with Aardvark SPI/USB converter).

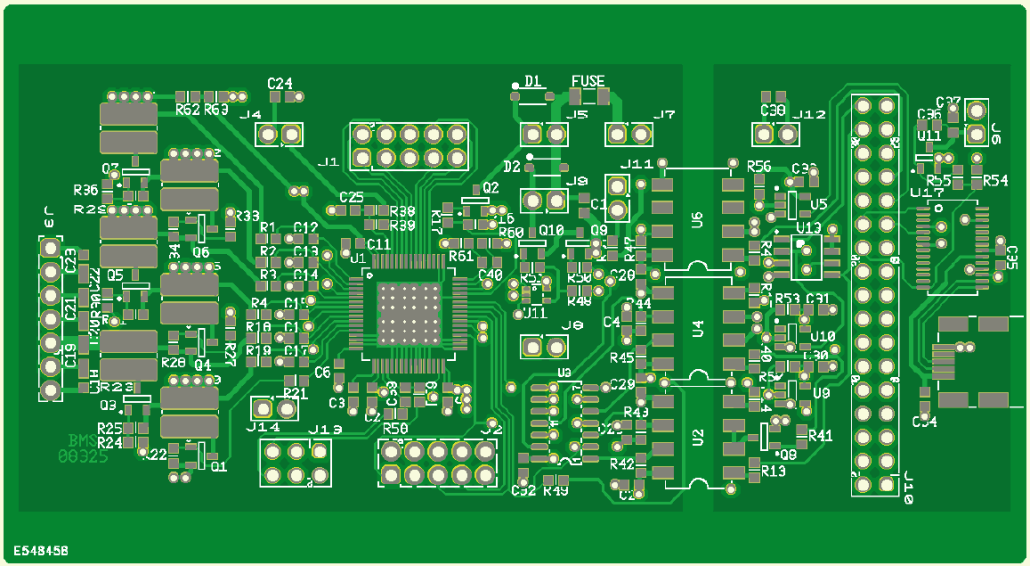



*Figure 53 - PCB top layer*

## 3.3.2. BMS / Battery Cabinet

The system is located in a transparent cabinet fulfilling the requirements. Connectors featuring lock mechanism are used to ensure proper connection under harsh conditions. The battery is fixated by a rubber material to allow expansion. See cabinet in Figure 54 and Figure 55.


*Figure 54 - Side view showing battery inside BMS cabinet*

*Figure 55 - Top view showing placement of system units*

## 3.3.3. Vehicle Integration

The BMS / battery unit is located outside the cockpit to increase safety. An emergency switch has been added to the BMS to allow interruption of battery current from outside the vehicle as well as from the cockpit. The electrical system integration as well as the mechanical fixation is showed in figure Figure 56 and Figure 57.

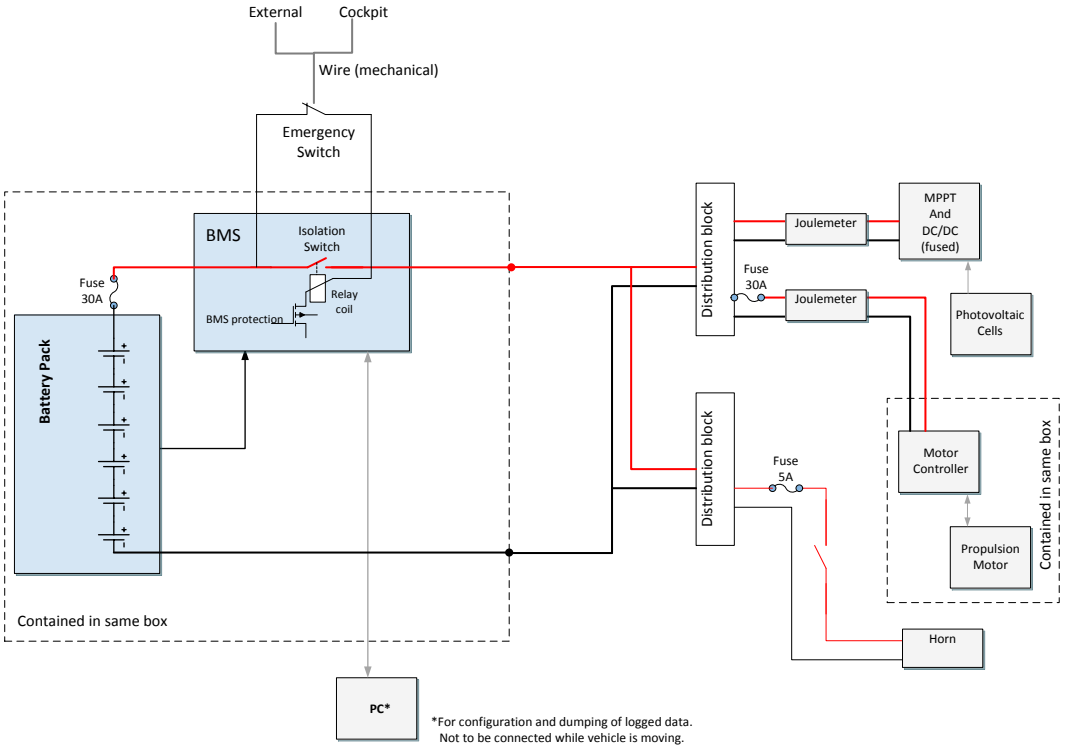



*Figure 56 - Vehicle schematic*

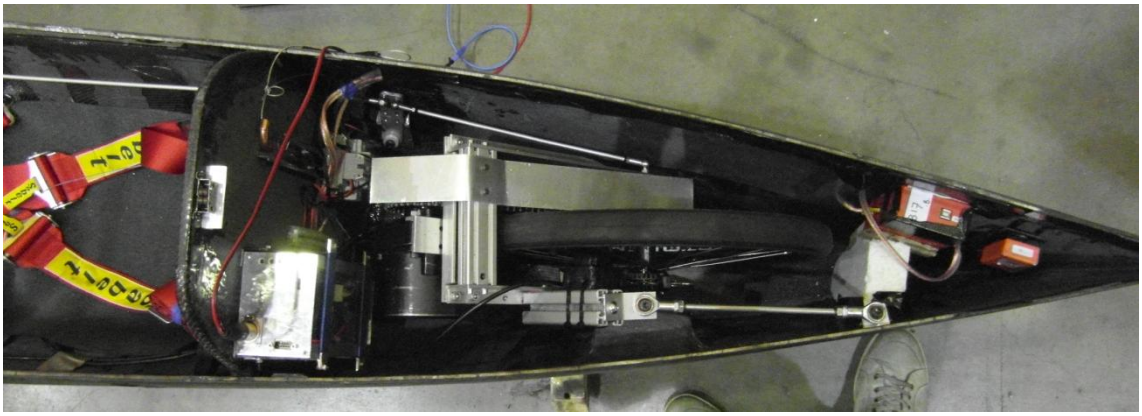


*Figure 57 - Location in vehicle*

### 3.3.4. Schematics

Full schematics of implemented system can be seen on following pages.

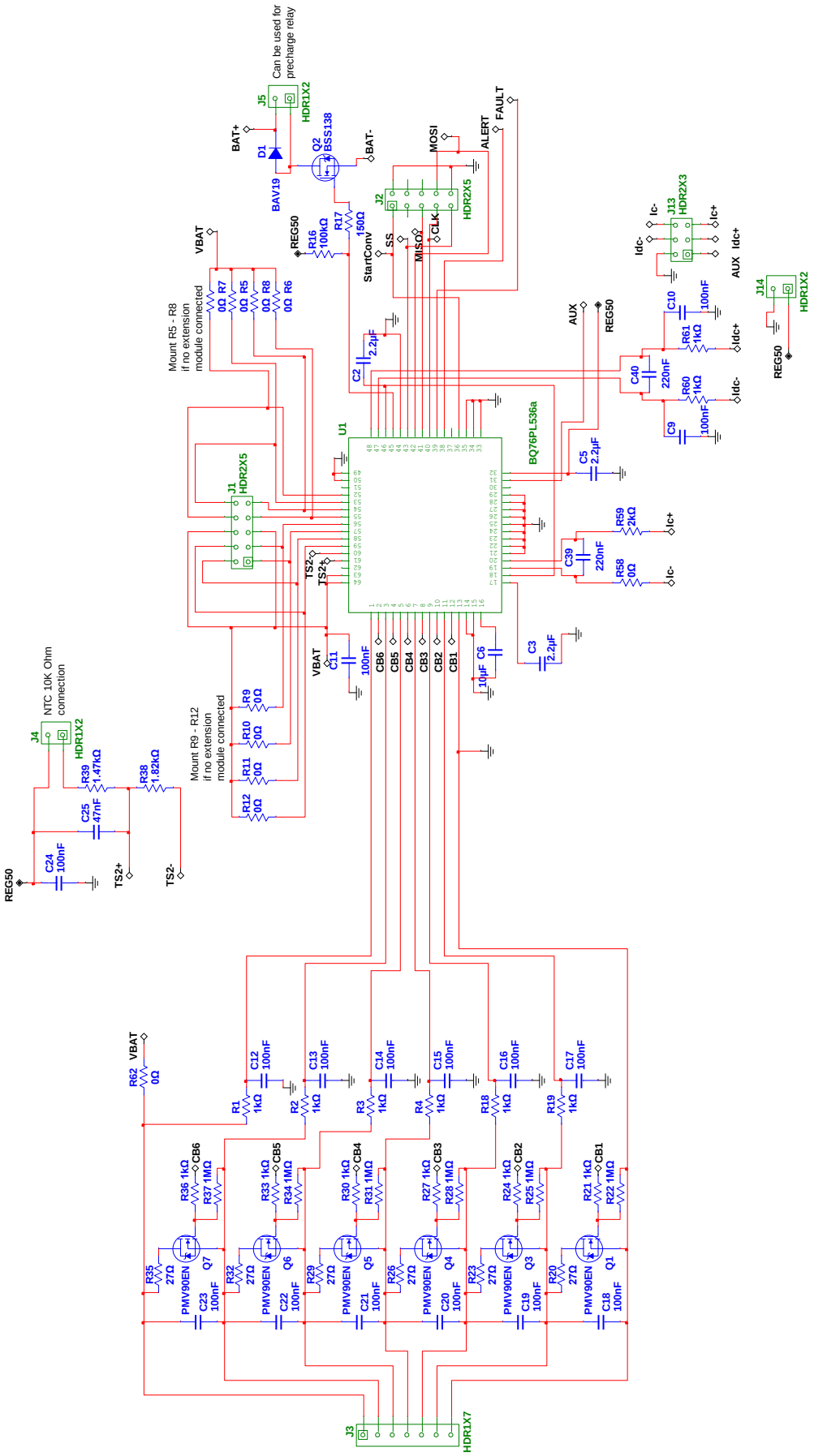



Figure 58 - Analog Front End

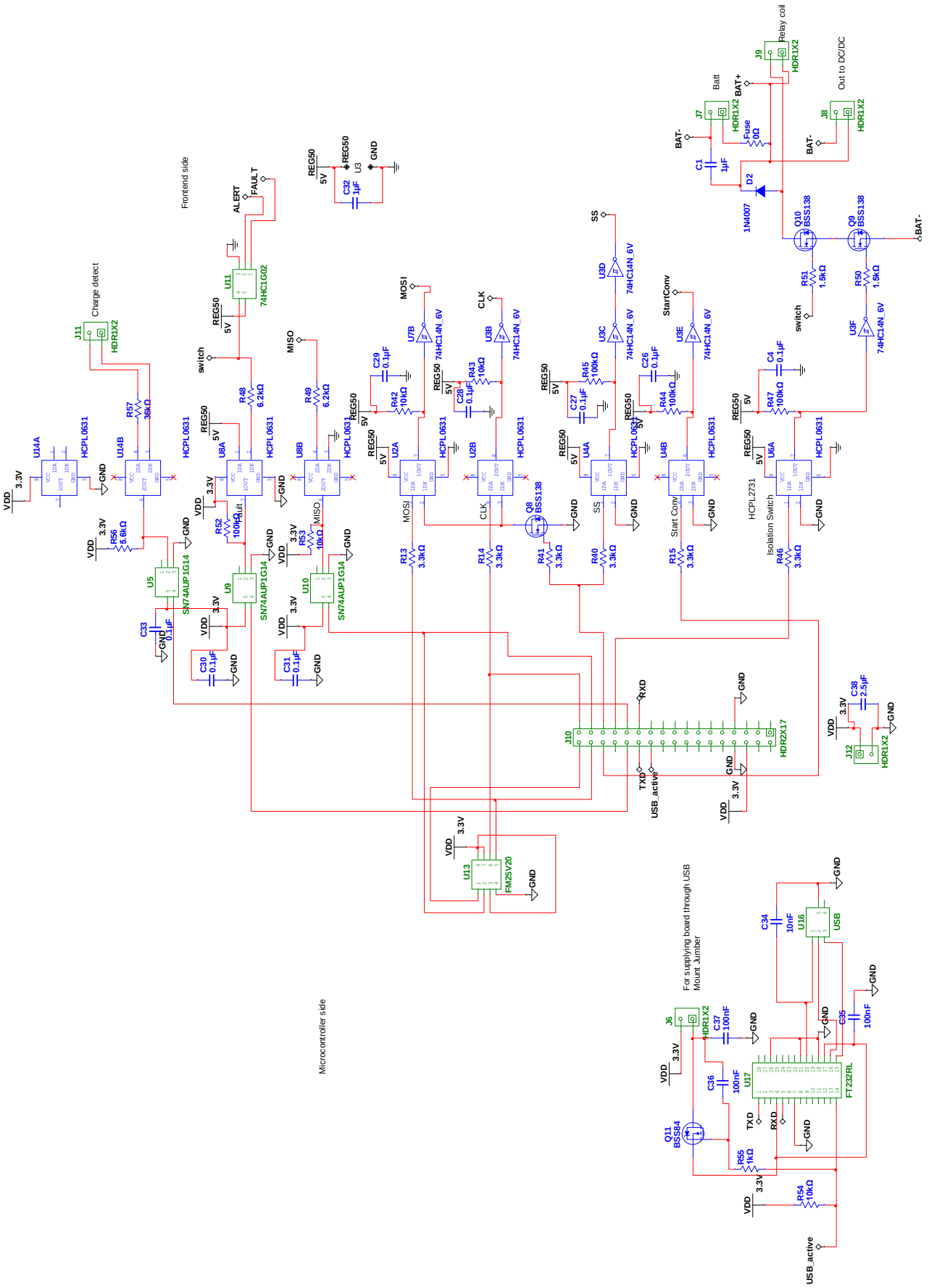



Figure 59 - Galvanic Isolation, USB interface and F-RAM

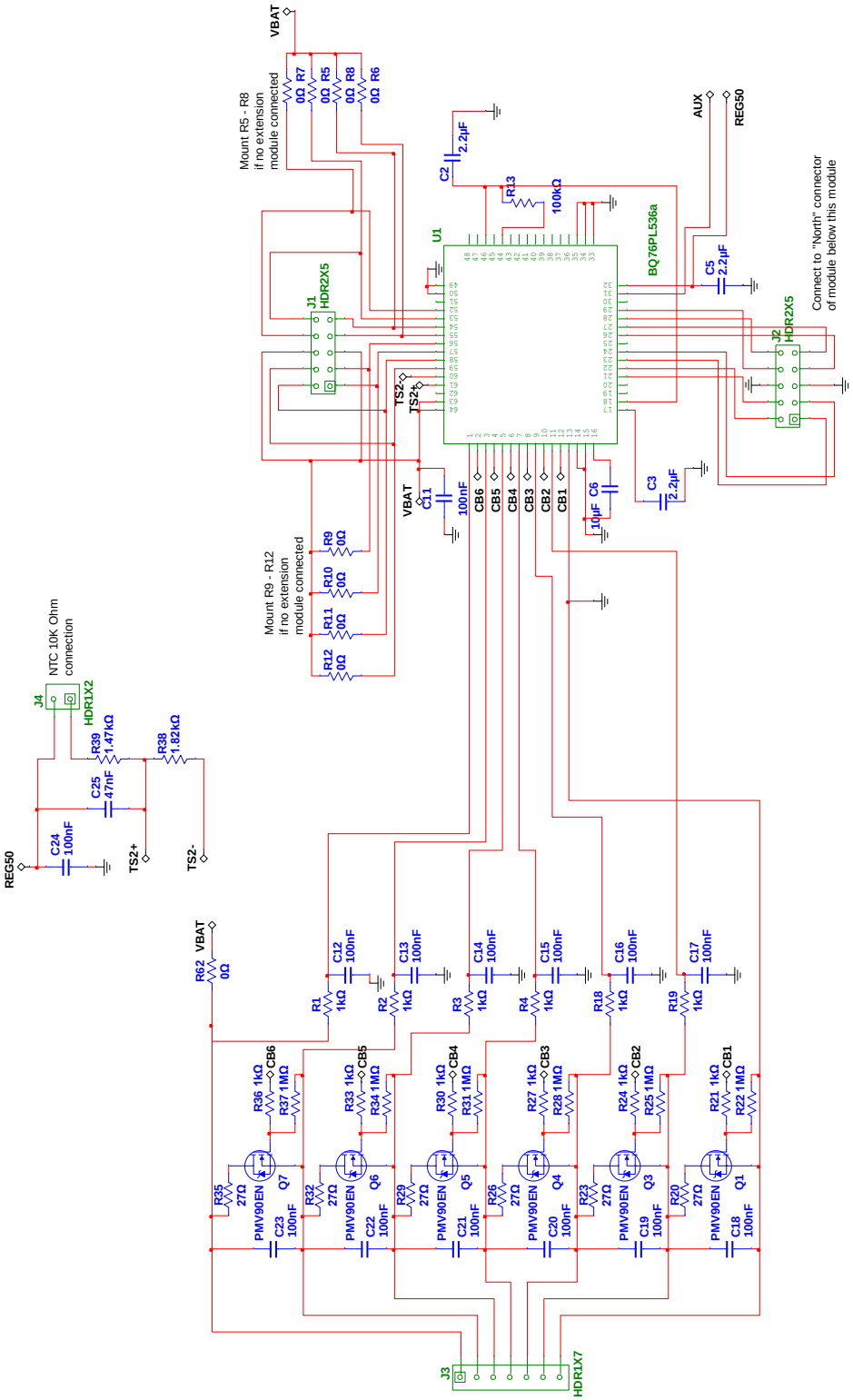



Figure 60 - Analog Front End Extension Module

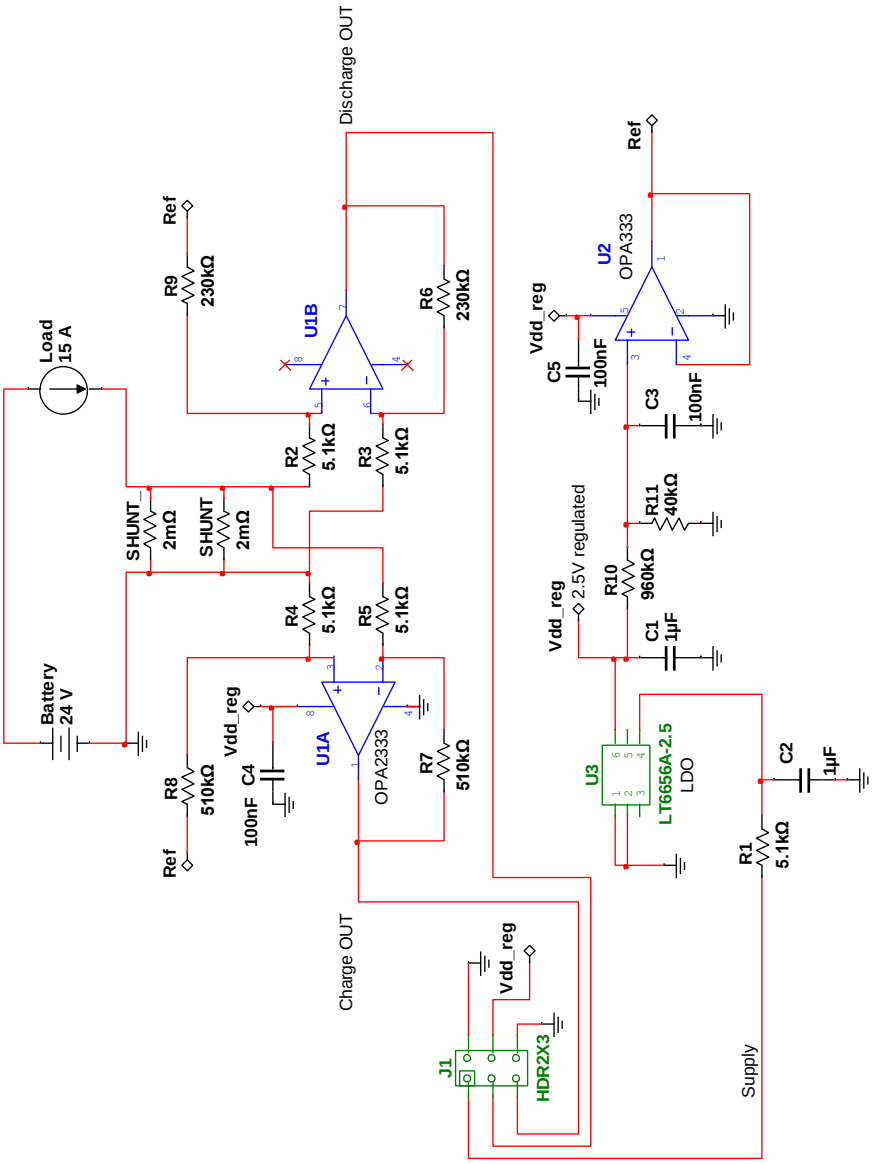



Figure 61 - Current Sensor

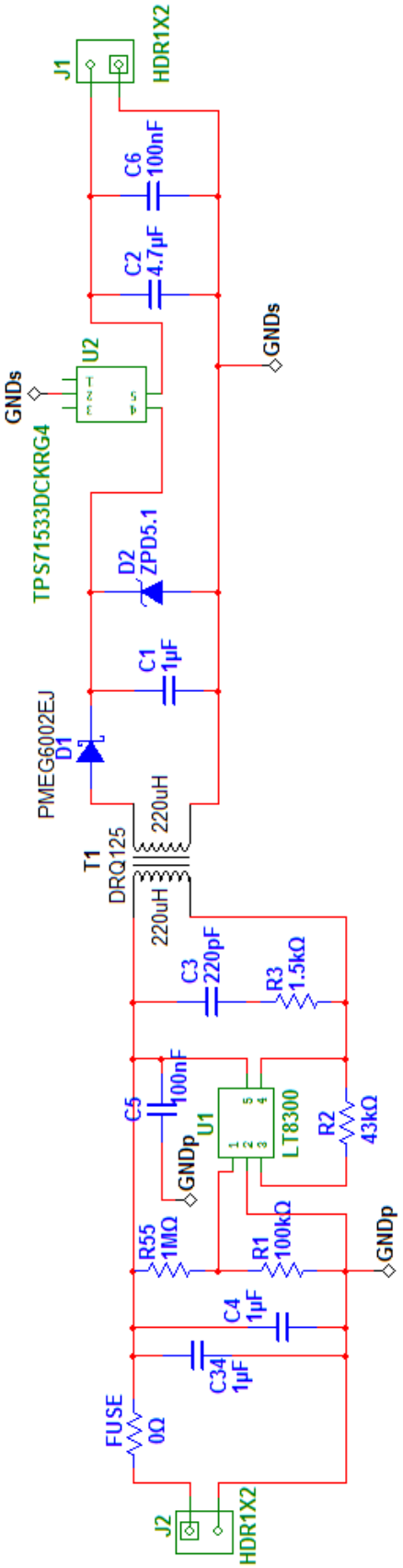



Figure 62 - DC/DC converter

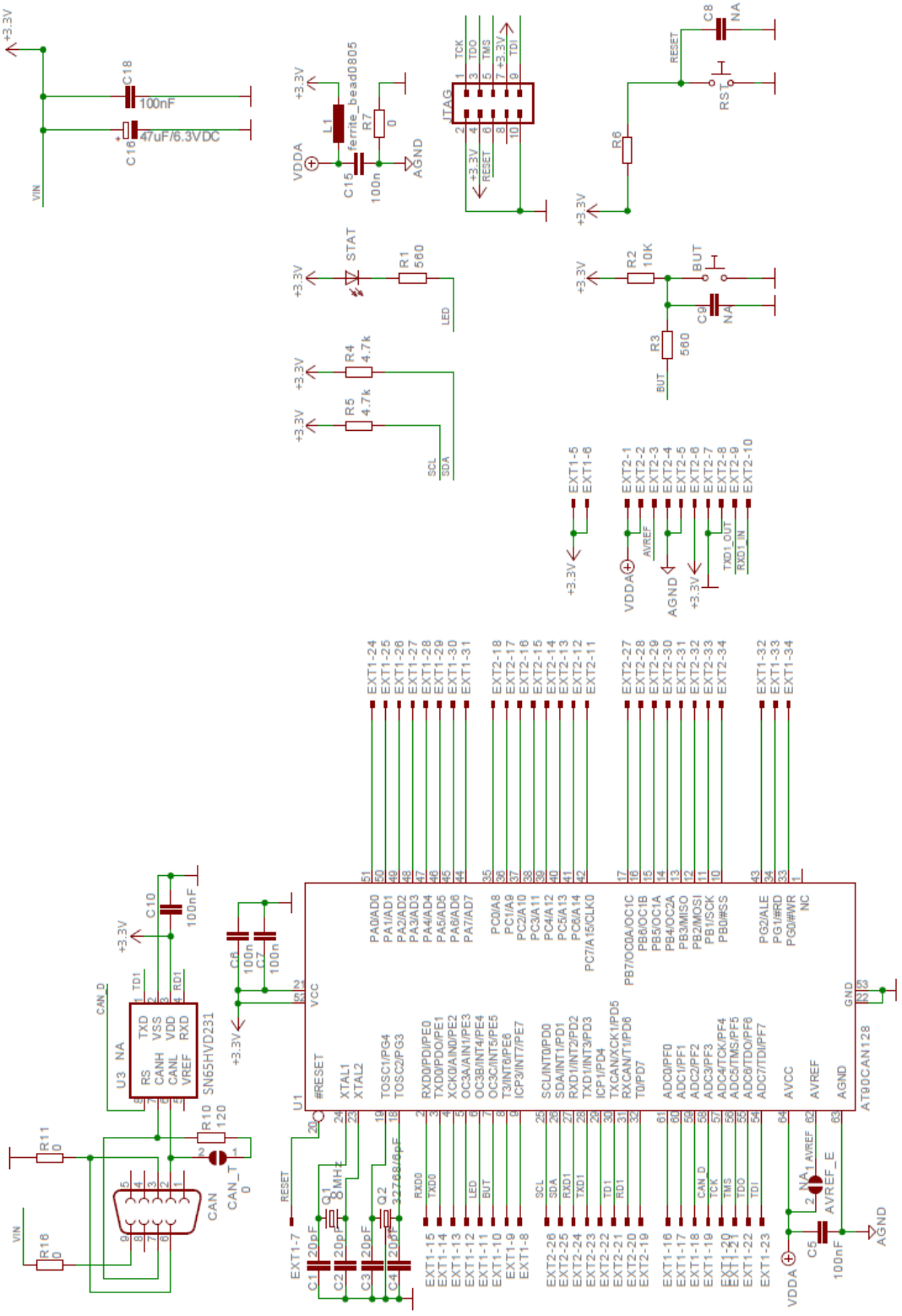


Figure 63 - Modified Olimex CAN-AVR (part of Digital Unit)

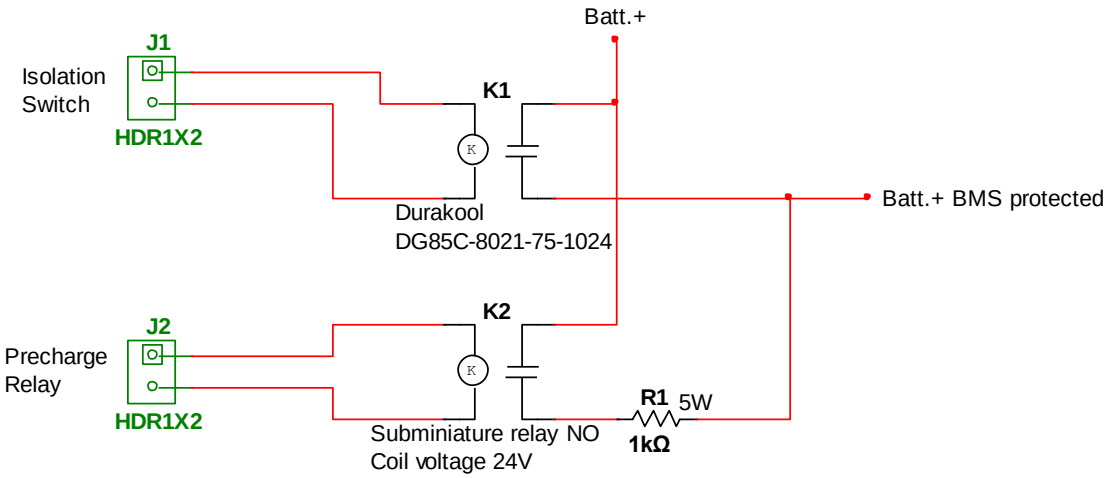



Figure 64 - Isolation Switch

# 4. ACCEPT TEST

## Version History

**Version 1, date: 31-05-2013**

## 4.1. Introduction

This document describes test procedures and results for the implemented Battery Management System and Propulsion Battery. The purpose of this accept test is to ensure that the system meets the specification requirements. For each specified requirement a test procedure will be given, subsequently the result will be presented and if needed, be commented on.

List of test equipment can be seen in Table 23.

| Type of equipment | Manufacture/Model/SW version | Serial No. |
|---|---|---|
| Constant current load | TDI / RBL 488 50-150-800 / unknown | 0706-0185 |
| Multimeter | Fluke / 289 / unknown | 12100169 |
| Power Supply | TTi / CPX400DP / unknown | 368469 |
| Temp. calibrator | AMETEK / ITC-155 A / unknown | unknown |
| Climate chamber | Feutron / KPK800 / unknown | unknown |
| CAN / USB converter | PEAK / unknown / unknown | unknown |
| CAN terminal SW | PEAK / PCAN view / unknown | unknown |

*Table 23 - List of test equipment*

# 4.2. Functional Requirements

## 4.2.1. Propulsion Battery

**Test of requirement PB_F.1 and PB_F.2** must be performed without active BMS protection. However the BMS is used for monitoring cell voltages and battery temperature and test mode must be enabled in the source code to transfer these measurements to the PC. Load is applied across fuse holder terminal(marked load) and negative battery terminal. See test setup in Figure 65.

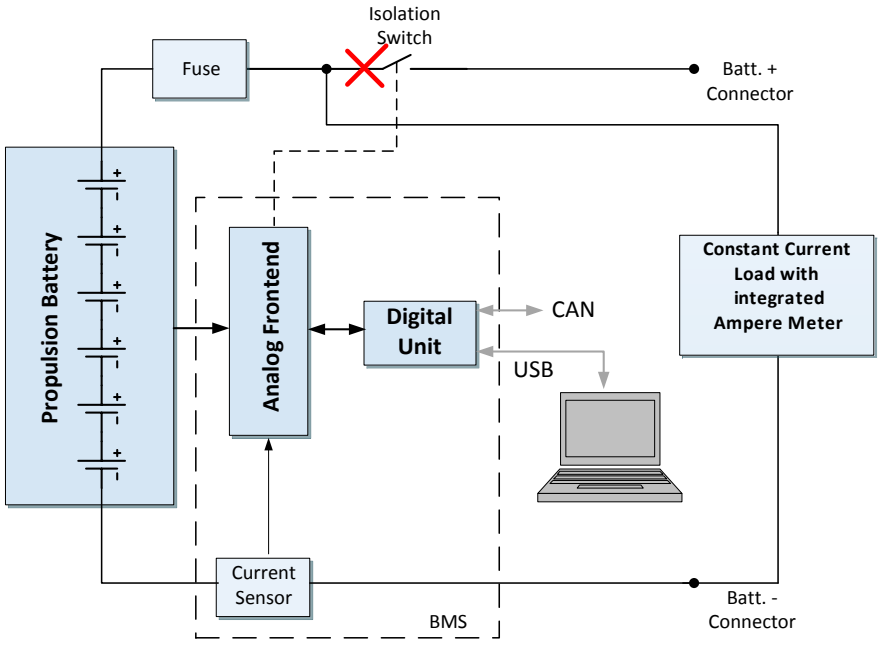



*Figure 65 - Test setup for battery and fuse test (PB_F.1 and PB_F.2)*

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| PB_F.1 | The propulsion battery must be short circuit protected by a fuse located on the positive conductor, as close to the battery as possible. Furthermore the fuse must be rated so that the battery is able to deliver enough short circuit current to open the fuse at all times. | | |
| | **Test Procedure** | | |
| | Inspect that distance between battery positive terminal and fuse is less than 15cm. Apply a load of 0Ω at SOC=5%. The fuse must blow and interrupt current flow. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| PB_F.2 | The propulsion battery must safely be able to withstand a continuous discharge current of 25A and a temporary max. current of 50A for 10 seconds. | | |
| | **Test Procedure** | | |
| | Charge battery to SOC>50%. Apply a constant current load of 25A for 1min. Increase current to 50A for 10sec. Battery temperature and cell voltages must be monitored during test, and must not exceed safe operation area. | **Yes** | cell voltage drops approximately 0.1V at 50A, temperature raises from 17 to 22°C |

**Test of requirement PB_F.3** must be performed with active BMS protection. Connect charger as shown in Figure 66.

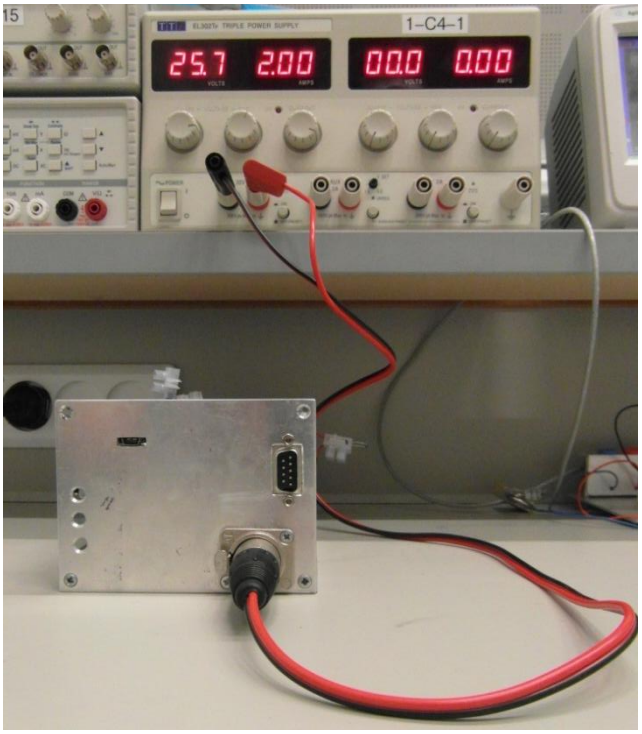



*Figure 66 - Connection of charger, for illustration only different PSU type*

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| PB_F.3 | The propulsion battery must accept a constant charging current of max. 15A. | | |
| | **Test Procedure** | | |
| | This test must be performed with active BMS monitoring!<br>Fully discharge battery. Set current limit of power supply to 15A and voltage to 25.7V. Connect to charging input of BMS and charge till current falls below 10% of initial value. | **Yes** | |

## 4.2.2. Battery Management System

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_F.1 | The BMS must, at all times, be able to isolate the battery from all external circuitry except the BMS, if any of the limits listed below is exceeded:<br>• Undervoltage limit (monitored at cell level)<br>• Overvoltage limit (monitored at cell level)<br>• Overcurrent limit (load and charge current)<br>• Overtemperature limit (monitored at battery level) | | |
| | **Test Procedure** | | |
| | Connect a load, and discharge till any cell voltage drops to undervoltage limit, ensure that load current is interrupted. Connect charger and charge till overvoltage limit is reached and ensure that charge current is interrupted. Apply a constant current load larger than overcurrent limit value, ensure that load current is interrupted. Mount temperature sensor in temperature calibration tool and adjust to a value above overtemperature limit, ensure that current flow is interrupted. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_F.2 | The BMS must be able to monitor from 6 to at least 16 cells. Changes in number of connected cells may require connection of extension modules and minor SW and HW adjustments. SW values that are cell count dependant must be implemented using definitions assembled in one location, to allow easy modification. | | |
| | **Test Procedure** | | |
| | Inspect HW and SW design and ensure that scalability has been taken into consideration. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_F.3 | In case of microcontroller failure or loss of communication with Analog Front End, the Analog Front End must perform autonomous protection of cells against under- and overvoltage, and perform isolation of battery if limits are exceeded. | | |
| | **Test Procedure** | | |
| | Disconnect SPI connection between Digital Unit and Front End. Perform over-/undervoltage test as specified in BMS_F.1 | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_F.4 | Maintenance cell balancing[31] must be performed by the BMS doing charge, to equalize SOC, and thereby compensate for (cell to cell) differences in self discharge currents. As cells SOC will be in balance at initial connection to the BMS, gross balancing capability is not needed. | | |
| | **Test Procedure** | | |
| | Discharge a single cell to a voltage 100mV below average of remaining cells. Complete a charge cycle and ensure that all cells are within a range of 20mV. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_F.5 | Following data must be stored in internal memory, once per minute, for later readout via USB port or SD card:<br>• Individual cell voltages<br>• battery current<br>• battery temperature(s)<br>• battery SOC<br>• battery SOH<br>• Error information<br>Capacity of internal memory must hold data history of min. 10 hours | | |
| | **Test Procedure** | | |
| | Charge battery to SOC=100%. Disconnect from charger and leave BMS unused for min. 10 hours. Read out data log and confirm that required values are present. | **No** | **Functionality not fully implemented** |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_F.6 | The BMS must be able to estimate SOC (at battery level), and internal resistance (at cell level). | | |
| | **Test Procedure** | | |
| | Connect USB while the BMS is in service mode and confirm presence. | **Yes** | |

[31] For details see: http://liionbms.com/php/wp_balance_current.php (date: 07-02-2013)

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_F.7 | If the internal resistance of any cell exceeds (averaged internal resistance x 2) an error message* must be transmitted on the CAN bus, to reveal poor cell performance.<br>* See CAN protocol DTC (5) for further details. | | |
| | **Test Procedure** | | |
| | Mount a battery with a cell known to have higher internal resistance. And ensure a warning is transmitted after a load has been applied. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_F.8 | The actual battery and cell status must be transmitted on the CAN bus according to CAN protocol. See CAN protocol for further details. | | |
| | **Test Procedure** | | |
| | Connect CAN/USB converter to BMS and PC. Use CAN terminal SW to confirm that values are transmitted according to CAN protocol. | **Yes** | |

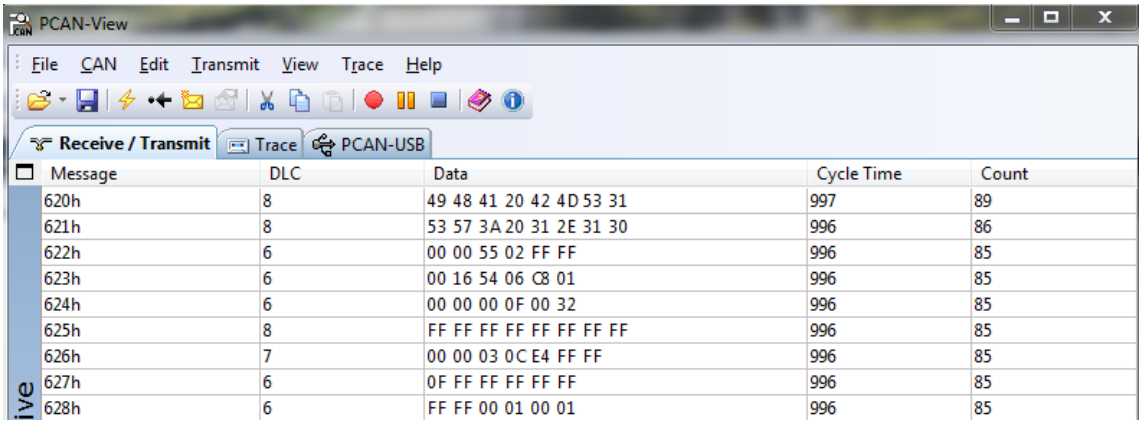



*Figure 67 - CAN output monitored using PCAN-view*

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_F.9 | The BMS must be able to enter a low power mode consuming less than 100mW if a undervoltage failure occurs. Low power mode will be entered after isolating the battery, so all protection functionalities may be deactivated. A pushbutton (or similar) must be available to resume normal BMS activity. | | |
| | **Test Procedure** | | |
| | Discharge till low power mode is entered. Insert ampere meter in cell 6+ wire and supply wire running from fuse holder to Analog Front End. Calculate the total power consumption as Vbatt * Itotal. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_F.10 | After the occurrence of an undervoltage error, the BMS must sense the connection of a charger and re-close the isolation switch, and thereby enable charging. | | |
| | **Test Procedure** | | |
| | Connect load and discharge till an undervoltage error occur. Confirm that load current is interrupted. Connect charger and inspect charge current to confirm that battery is being charged. | **Yes** | |

## 4.3. Non-functional requirements

### 4.3.1. Propulsion Battery

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| PB_NF.1 | The propulsion battery must consist of a number of Lithium-Ion cells, leading to a nominal battery voltage within the range of 22 - 26 Volts. | | |
| | **Test Procedure** | | |
| | Inspect battery label, which is visible through transparent side of BMS cabinet, and confirm that labeled value is within specified range. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| PB_NF.2 | All battery cells must be contained in one battery unit, as only one propulsion battery per vehicle is allowed. | | |
| | **Test Procedure** | | |
| | Visually inspect BMS to confirm that only one battery is contained in the BMS/battery cabinet. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| PB_NF.3 | The effective capacity* must be greater than or equal to 70Wh.<br>*Capacity available at 100W load and ambient temperature of 8°C[32]. | | |
| | **Test Procedure** | | |
| | Charge battery to SOC=100%. Place BMS/battery unit in climatic chamber. Set temperature to 8°C and wait for battery temperature to stabilize at this level. Discharge battery at constant current of 4A and measure time from discharge start to BMS interrupts discharge current. Calculate Capacity as 4A*discharge time[h]*nominal voltage and confirm that value exceeds 70Wh. | **Yes** | **0.85h*4A*22.2V = 75.5Wh** |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| PB_NF.4 | The propulsion battery must be electrically isolated from the vehicle frame and the accessory battery circuit. | | |
| | **Test Procedure** | | |
| | Inspect schematics to confirm galvanic isolation and visually inspect implemented system to confirm that no electric connection is established with the cabinet surrounding the system. | **Yes** | |

[32] Based on average low temperature for Rotterdam in May, See: http://weatherspark.com/averages/28810/5/Rotterdam-Zuid-Holland-The-Netherlands (date: 02-02-2013)

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| PB_NF.5 | Technical documentation fulfilling Article 58 of Shell Eco-marathon official rules[33] must be prepared before participation. | | |
| | **Test Procedure** | | |
| | Ensure that technical documentation is approved at technical inspection performed at the Eco-marathon event. See technical documentation in appendices. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| PB_NF.6 | Min. 2 batteries must be available, to ensure the possibility of battery replacement between races. | | |
| | **Test Procedure** | | |
| | Count number of available batteries. | **Yes** | |

### 4.3.2. Battery Management System

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_NF.1 | Limits listed in BMS_F.1 must be kept within specifications of chosen cell type. | | |
| | **Test Procedure** | | |
| | Compare thresholds defined in source code with Li-PO safety guidelines[34]. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_NF.2 | Types of measurements performed by the BMS, including measurement ranges and accuracy:<br>Cell voltage: 2V to 4.5V (accuracy +/- 4mV @ 24°C)<br>Battery temperature: -20°C to 100°C (accuracy +/- 3°C)<br>Battery current: -15A to 60A (accuracy +/- 100mA) | | |
| | **Test Procedure** | | |
| | Replace cell 6 with a power supply, and adjust values as stated in table below. Ensure BMS test mode is enabled. Compare voltmeter and BMS output value, by using a terminal software(Code vision terminal has been used). | **Yes** | |

[33] See " sem_rules_chapter01_2013" in appendices
[34] See "Li-ion_Li-Poly_Precautions-1" in appendices

| | | | | |
|---|---|---|---|---|
| | Place temperature sensor in temp. calibration tool. Adjust to values stated in table below and compare with BMS output.<br>Connect a constant current load and adjust to values specified in table below. Note the initial value (approx 70mA) which is consumed by the isolation switch (and a fragmental part by the BMS) and subtract this value when currents are compared. Connect charger(power supply) and adjust constant current limit to values as stated in table below. | | | |
| | **Voltage test** | | | |
| | PSU (simulates cell 6) [mV] | BMS cell 6 voltage [mV] | **Yes** | Will not be tested down to 2V as the BMS goes into sleep when voltage falls below 3V |
| | 4500 | 4498 | | |
| | 3500 | 3499 | | |
| | 3000 | 2999 | | |
| | **Temperature test** | | | |
| | Temp. calibration tool set point [°C] | BMS temperature [°C] | | |
| | -10 | -9 | **Yes** | |
| | 0 | 0 | | |
| | 30 | 28 | | |
| | 60 | 60 | | |
| | **Current test** | | | |
| | Constant current load [mA] | BMS Idischarge value [mA] | | |
| | 1000 | 1074 (-70) | **YES** | |
| | 5000 | 5107 (-70) | | |
| | 20000 | 20093 (-70) | | |
| | 50000 | 50156 (-70) | | |
| | Charging current [A] | BMS Icharge value [A] | | |
| | 1000 | 929(+70) | **YES** | |
| | 5000 | 4937 (+70) | | |
| | 14500 | 14456 (+70) | | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_NF.3 | Cell balancing current min. 75mA[35] | | |
| | **Test Procedure** | | |
| | Inspect design(check power resistor for dissipative balancing) to confirm that requirement is meet. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_NF.4 | Operational within Industrial Temperature range -40°C to 85°C | | |
| | **Test Procedure** | | |
| | Check the ratings of components. As full test in climatic chamber will be too time consuming. | **Yes** | **See table below** |
| **IC type** | **IC ID** | **Temp. range** | |
| Battery monitor and secondary protection | Bq76PL536A | -40 to 85 | |
| NOR gate | 74HC1G02 | -40 to 125 | |
| Op Amp | OPA333/2333 | -40 to 150 | |
| Voltage reference | LT6656A | -55 to 125 | |
| Optocoupler | HCPL2731 | -40 to 85 | |
| Inverter | 74HC14 | -40 to 125 | |
| Inverter | SN74AUP1G14 | -40 to 85 | |
| Flyback converter IC | LT8300 | -40 to 125 | |
| Voltage regulator | TPS71533 | -40 to 150 | |
| Microcontroller | AT90CAN128 | -40 to 85 | |
| USB to UART converter | FT232RL | -40 to 85 | |
| CAN transceiver | SN65HVD231 | -40 to 85 | |
| F-RAM | FM25V20 | -40 to 85 | |

[35] Derived from rules specified in: http://liionbms.com/php/wp_balance_current.php (date: 07-02-2013)

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_NF.5 | COM port communication must be implemented according to RS-232 (ISO IS2110) standard, or as virtual COM port with female Mini USB plug. | | |
| | **Test Procedure** | | |
| | Visually inspect BMS/battery unit to confirm type of connector and connect to PC to confirm that unit is recognized as COM port device. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_NF.6 | Average power consumption must be kept below 1.5W while all BMS functionalities are active. (consumption of isolation switch not included) | | |
| | **Test Procedure** | | |
| | Insert ampere meter in cell 6+ wire and supply wire running from fuse holder to Analog Front End. Calculate the total power consumption as Vbatt * Itotal. | **Yes** | **(0.9mA+1.95mA)* 23.4V**<br>**= 67mW** |

**Note regarding power consumption measurement**

To get a overview of dynamic changes in supply current an Aim I-prober current probe has been used, a wire has been wounded through the probe loop 10 times and Oscilloscope has been set to 0.1x probe, this results in a I to V ratio of 1 (1mV equals 1mA).

Analog Front End, Current Sensor and galvanic isolation is supplied through Cell 6+ wire. Measurement can be seen in Figure 68. A DC ampere meter was connected in series with the current probe to validate measurement. DC ampere meter value read to 0.88mA.

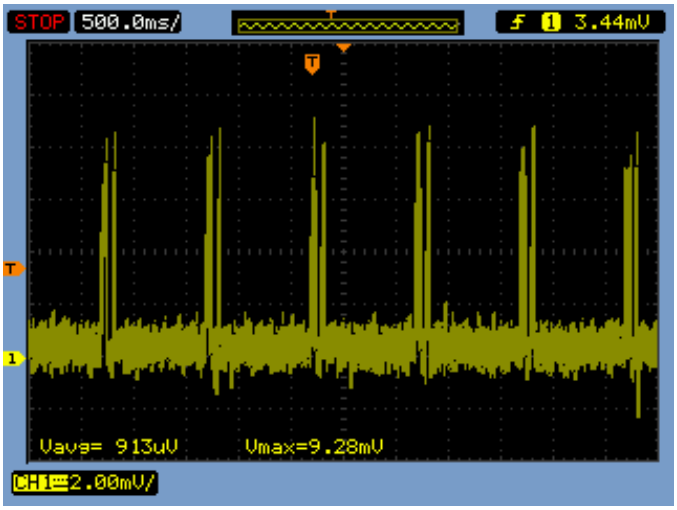



*Figure 68 - Supply current for Analog Front End, current sensor and battery side of galvanic isolation*

Power consumption of the remaining system must be performed using the voltage drop across a 100Ω resistor, as the current probe picks up too much noise from the DC/DC converter to achieve a satisfying result. Measurements can be seen below 1mV = 1mA.

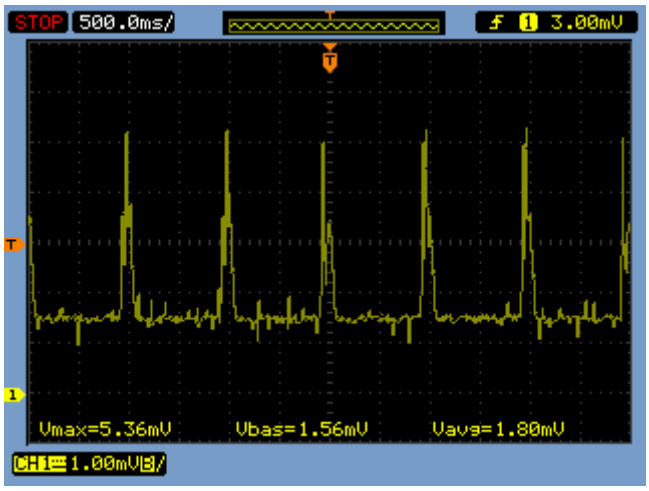



*Figure 69 - Supply current for all remaining circuitry except the Isolation Switch (CAN deactivated)*


*Figure 70 - Supply current of all remaining circuitry except Isolation Switch (CAN active)*

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_NF.7 | Isolation switch must safely carry a continues current of 25A. And a max. current of 50A for 10 seconds. Furthermore it must be able to interrupt a current of 75A. | | |
| | **Test Procedure** | | |
| | Connect BMS/battery unit to constant current load set to 75A and confirm that current is interrupted. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_NF.8 | Technical documentation fulfilling Article 58 of Shell Eco-marathon official rules[36] must be prepared before participation. | | |
| | **Test Procedure** | | |
| | Ensure that technical documentation is approved at technical inspection performed at the Eco-marathon event. See technical documentation in appendices. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_NF.9 | The system must be mounted in a cabinet fulfilling Article 57-m of Shell Eco-marathon official rules. | | |
| | **Test Procedure** | | |
| | Ensure that cabinet is approved at the Eco-marathon technical inspection. | **Yes** | |

| Req. # | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| BMS_NF.10 | All PCBs, plugs, fuses etc. must be backed-up by replacement units to allow on-site repair. | | |
| | **Test Procedure** | | |
| | Inspect availability of required parts. | **Yes** | |

## 4.4. Communication Protocols

### 4.4.1. CAN communication protocol

To confirm that the implemented system meets the CAN protocol requirements, a CAN/USB converter and a terminal PC software must be used. Confirm that received data is of correct format and located at addresses stated in the Specification Requirements.

**Result:** See BMS_F.8 (requirements met).

### 4.4.2. RS232 communication protocol

As the system log function has not been fully implemented, this test could not be conducted.

[36] See " sem_rules_chapter01_2013" in appendices

## 4.5. Summary of Tests

| Req. type | Requirement description | Meets requirement? | Comment |
|---|---|---|---|
| PB_F | Propulsion battery functional requirements. | **Yes** | |
| BMS_F | BMS functional requirements | **(Yes)**<br>Except BMS_F.5 | BMS_F.5 does not meet the requirement as the functionality has not been fully implemented. |
| PB_NF | Propulsion battery non-functional requirements. | **Yes** | |
| BMS_NF | BMS non-functional requirements | **Yes** | |

*Table 24 - Test summary*

Test performed by: Jonas Nyborg

Date of test: 10-05-2013 and 12-06-2013

# LITERATURE

## Articles/Papers

Rodrigo et al., date unknown, http://www.icrepq.com/icrepq-08/434-de-diego.pdf (date:14-04-13)

Kaushik Roy et al., 02/2003, http://ambienthardware.com/courses/tfe01/pdfs/Roy1.pdf (date: 11-06-2013)

Davide Andrea, 08/11/2009 http://liionbms.com/php/standards.php (date: 02-03-2013)

Davide Andrea, 13/03/2013 http://liionbms.com/php/wp_balance_current.php (date: 07-02-2013)

## General Links

http://weatherspark.com/averages/28810/5/Rotterdam-Zuid-Holland-The-Netherlands (date: 02-02-2013)

http://batteryuniversity.com/learn/article/types_of_lithium_ion (date: 11-06-2013)

http://www.hobbyking.com/hobbyking/store/uh_viewItem.asp?idProduct=27121 (date: 22-05-2013)

http://largebattery2012.fotopages.com/?&page=15 (Date:08-06-2013)

## Books

Valer Pop et al. 21/05/2008 "Battery Management Systems: Accurate State-Of-Charge Indication for Battery Powered Applications"

Davide Andrea, 30/09/2010 "Battery Management Systems for Large Lithium Ion Battery Packs"

## Other

sem_rules_chapter01_2013, Official Shell Eco-marathon rules, see appendices

Referenced Datasheets are included in appendices