Description of Electric System [for Technical Inspection SEM 2014]

System Description

The system consist of a Lithium-ion polymer propulsion battery, and a Battery Management System (BMS) tailored to survey this battery chemistry. The system features a Digital Unit able to analyze safety relevant parameters and interrupt the current if any parameter exceeds allowable threshold. Furthermore, to ensure maximum safety, redundant protection, independent of the Digital Unit, has been implemented as part of the analog frontend, which handles the measurements at cell level, and like the Digital Unit is able to interrupt the battery current. protection thresholds, battery data, etc. can be seen below, in the chapter: Safety related Information.

Block Diagram and Block Description

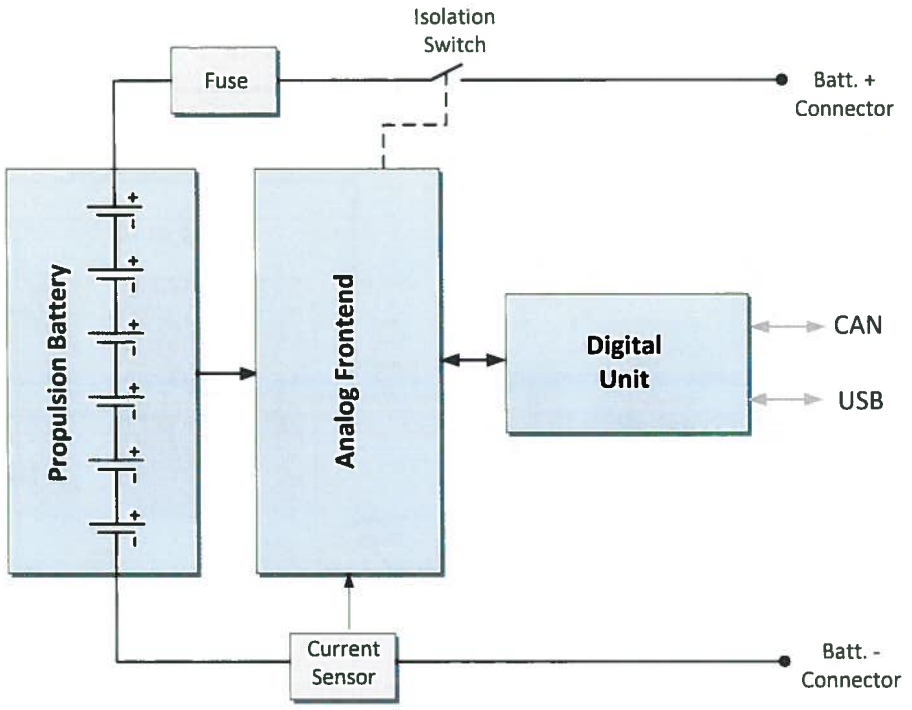


Figure 1 - general block diagram

Propulsion Battery

This unit, consisting of 6 Lithium-ion polymer battery cells, is responsible for storage of electrical energy. It captures energy from an external charger, solar panels and regenerative braking. And is capable of delivering the current needed to propel the propulsion motor.

Max. charging voltage: 50.4V
Min. voltage: 36V
Capcity: 1300 / 2200mAh (depends on weather and achieved efficiency)
Max. continues discharge: 25 / 35C
Max. charge rate: 5 / 8C

Fuse Data:

Type: KLK 20 fast-acting fuse
Nominal current: 20 A
Interrupt Rating: 50KA

Isolation Switch(relay) Data:

Manufacture: Panasonic
Type: HE1ANS48
Contact type: Normally Open
Max. continues current: 30A
Max. Break current: 30A
Nom. coil voltage: 48V

Parameters under surveillance, and action at out of range

Parameter	Action at out of range	Action required to reset
Cell voltage	Undervoltage: Battery is isolated from load, BMS goes to deep sleep to reduce consumption. Overvoltage: Battery is isolated from charger, bleeder resistor is applied across cells exceeding threshold, to force voltage down.	Undervoltage error is reset at connection of charger. Overvoltage error requires press at reset button.
Battery Temperature	Isolates battery from load/charger	Requires removal of error condition and press at reset button.
Charge current	Isolates battery from load/charger	Requires removal of error condition and press at reset button.
Discharge current	Isolates battery from load/charger	Requires removal of error condition and press at reset button.

BMS Threshold levels, primary protection levels

Parameter	Upper threshold / delay	Lower threshold / delay
Cell voltage	4.19V / 201ms(max.)	3V / 201ms(max.)
Temperature (charge)	45°C / 201ms(max.)	0°C / 201ms(max.)
Temperature (discharge)	60°C / 201ms(max.)	-20°C / 201ms(max.)
Discharge current	20A / 10sec (25A / 201ms(max.))	-
Charge current	8A / 201ms(max.)	-

Motor Controller

Shell ECO Marathon Team AU 2014

Simon Møiniche Skov

Anders Fiilsøe Ramsing

Christoffer Graversen

Contents

Preliminary work 1

This chapter describes the work performed to get to grips with the functionality of the complete system. The chapter will cover system diagrams, requirements specifications and use case models.

1.1 Requirements

1.1.1 Description

The motor drive system has to fulfill the requirements to qualify for participation in Shell Eco-marathon. Functional requirements are derived from SEM[1], OOD[2] and the BMS[3]. The internal structure of the motor drive system is depicted in Figure 1.1.

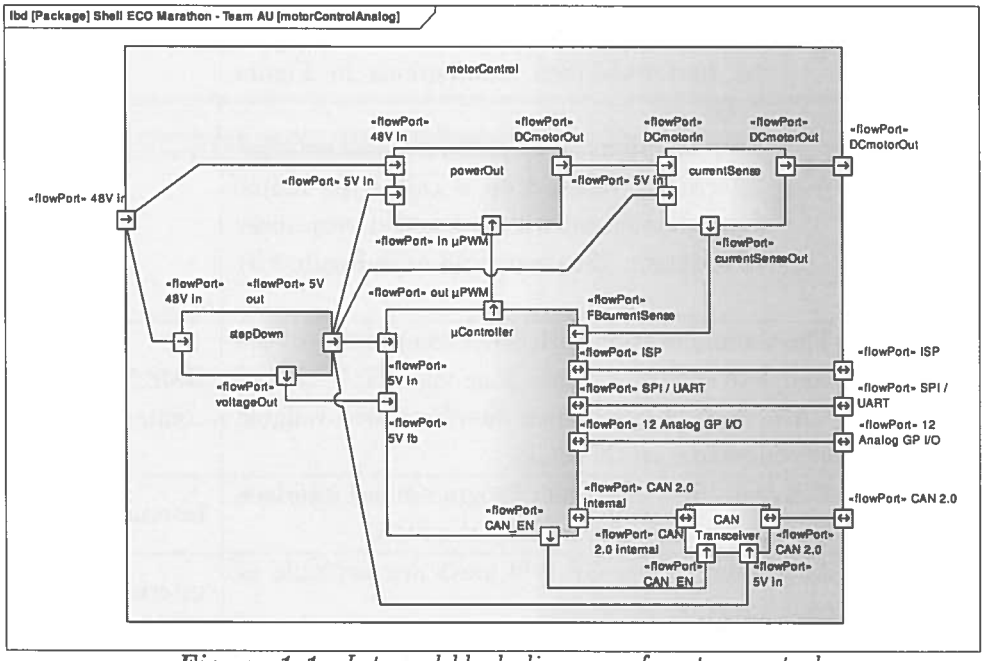


Figure 1.1: Internal block diagram of motor control

To ease the use of the individual requirements, each requirement is given a specific number in the form of mC.x-x.

[1]SEM global official rules 2014.
[2]Reports and conclusions on optimization of the drivetrain.
[3]Documentation of the battery management system.

Internal Boundaries		
Req.#	***Requirement description***	***Reference***
mC.1-6	To supply the control circuit an internal supply of 100 mA@5 V is needed. *Tolerance:* V_{CC}: 4,8 V - 5,2 V	Internal Requirements
mC.1-7	A step down converter with a voltage input range of 12 V-75 V, and an output of max. 380 mA@5 V is implemented in the system.	Internal Requirements
mC.1-8	The internal current sense has a resolution of approximately 330 mV/A through a buffered low pass filter.	Internal Requirements
mC.1-9	The output is controlled by adjusting the duty cycle of the internal PWM signal. • Voltage: 0 V-5 V *Tolerance:* Low_{max}: 0,7 V $High_{min}$: 4,2 V • Current: Max. 40 mA • Frequency: Adjustable from 15 kHz - 100 kHz	ATmega64M1 datasheet section 28.2(DC characteristics)
Power output		
Req.#	***Requirement description***	***Reference***
mC.1-10	The components of the power output has to be able to handle a continuous max current of 15 A@75 V	OOD-section 14.3(Delkonklusion) (200 W DC motor)
mC.1-11	The motor drive is only able to operate DC motor in 1^{st} quadrant of the I_A-N_{rpm} plane, Figure 1.2	Internal Requirements
mC.1-12	The output control is based on the burn and coast principle, Figure 1.3	OOD-section 16.2(Simuleringscyklus)
mC.1-13	Launch procedure is implemented as a ramp acceleration derived from a torque curve available from the test bench group. An array of ten integers is made in the software to define the current output according to rpm in the acceleration ramp.	OOD-section 16(Accelerations Principper)
mC.1-14	The output control is maintained via feedback from both output current and drivetrain speed.	Internal Requirements

Table 1.1: Functional requirements table

1.1.4 Functionality

The use of the system is simplified to the use om two buttons "Go" and "Stop". The functionality is described in the state machine in Figure 1.4.

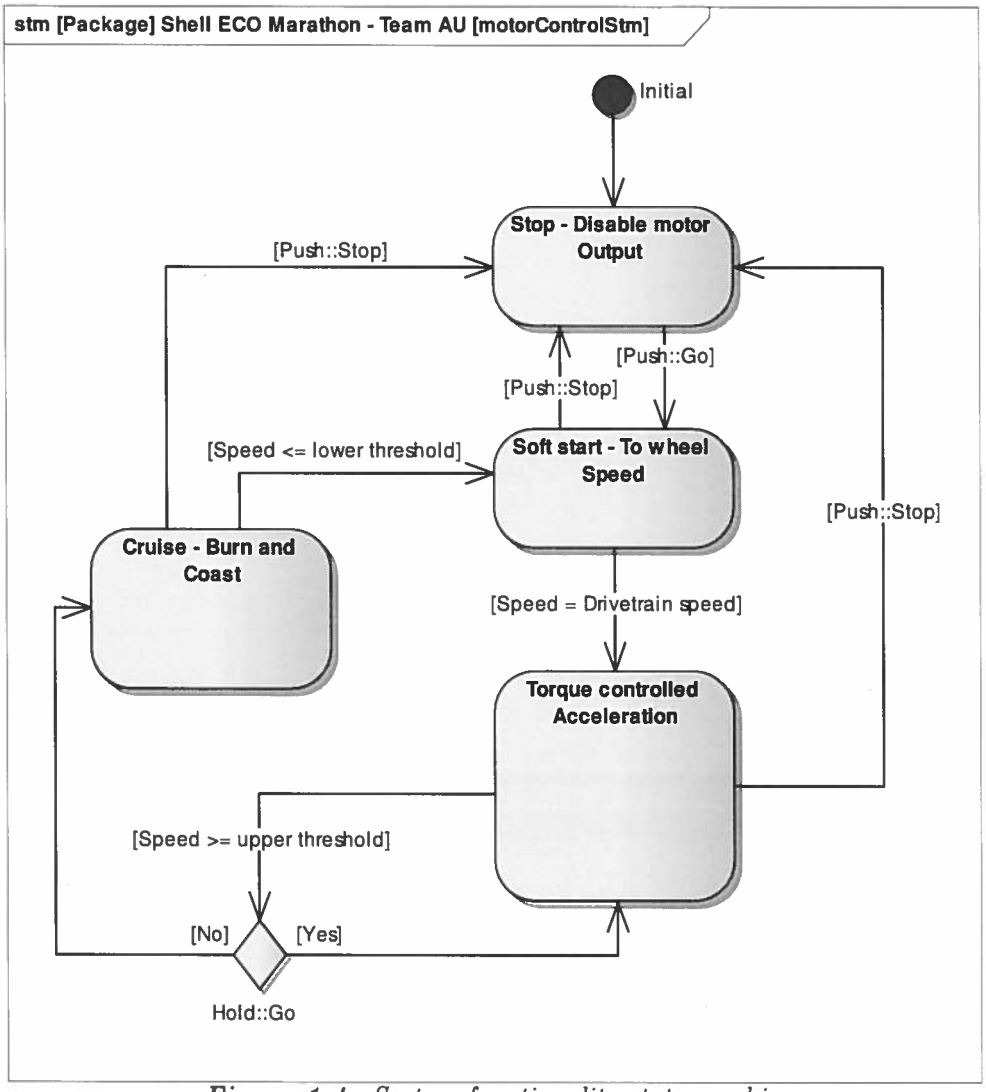


Figure 1.4: System functionality state machine

Design and Implementation 2

The purpose of this chapter is to describe the design of the motor controller in details, both for the hardware and the software. For the hardware a graphical schematic will be given and the purpose of each element will be described with its considerations and equations. The software will be described by graphical UML diagrams and element functionality for each section.

2.1 System Description

The system description summarizes the considerations and design choices of the system.

2.1.1 Hardware

The complete Hardware circuit is designed as shown in the schematic in Figure 2.1, and implemented on a printed circuit board. Considerations about spacing, EMC and high frequency noise has been made prior to the physical implementation. In this section the functionality of each subcircuit of the hardware is described in details.

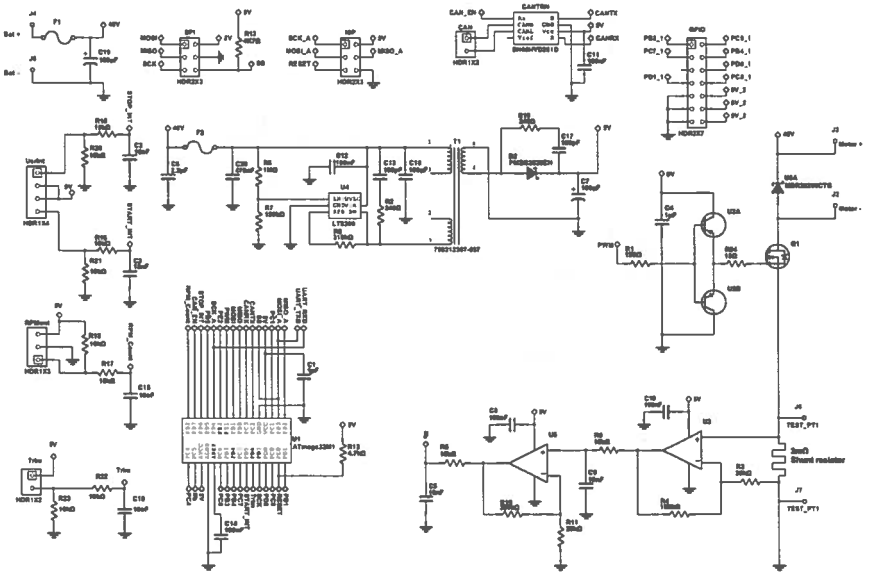


Figure 2.1: Complete motor controller circuit

For better noise performance the AREF pin is connected to GND via a noise reduction capacitor as described in ATmega32M1 datasheet section 21.

2.1.1.3 Switch Mode Step Down Converter

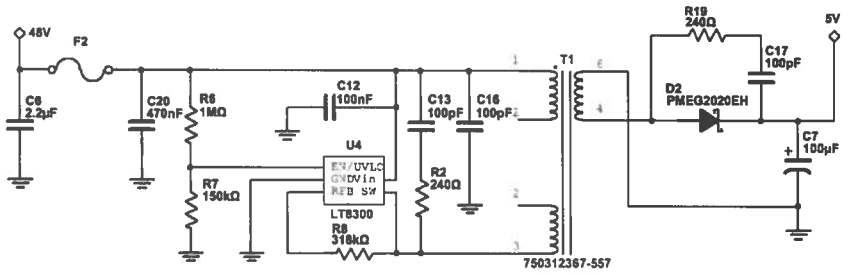


Figure 2.4: Switch Mode Step Down Converter

The voltage step down from the system supply voltage to the control circuit voltage is achieved with at switching mode step down converter. The switching converter provides a significant improvement in efficiency compared to a LDO. The circuit is adapted from the datasheet of the LT8300 controller, and is customized to meet the system specifications. All design details are chosen according to the applications section in the LT8300 datasheet.

To meet the specifications of the dynamic input voltage from 12 V - 75 V the input resistors of the step down converter is chosen as shown in Equation 2.1.

$$R_7 = \frac{V_{Pin} \cdot R_6}{I_{Pin} \cdot R_6 + V_{in} + V_{Pin}} \tag{2.1}$$

Where:
$R_6 = 1\,\text{M}\Omega$
$V_{Pin} = 1{,}239\,\text{V}$
$I_{Pin} = 2{,}5\,\mu\text{A}$
$V_{in} = 12\,\text{V}$
$\Rightarrow R_7 \approx 150\,\text{k}\Omega$

The control circuit is specified to operate at 5 V. This is achieved by calculating the correct value of R_8 as in Equation 2.2.

$$R_8 = \frac{N \cdot (V_{out} + V_f)}{I_{fb}} \tag{2.2}$$

Where:
$N = 6$
$V_{out} = 5\,\text{V}$
$V_f = 0{,}3\,\text{V}$

2.1.1.4 Power Output and Feedback Circuit

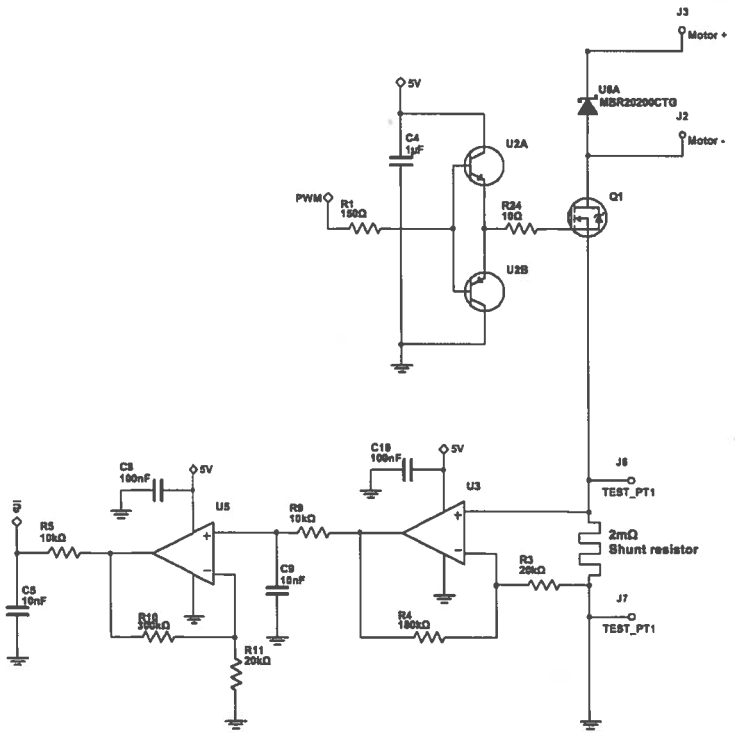


Figure 2.5: Power output stage at current feedback circuit

The power output for the DC motor is made as a simple on switch chopper PWM control. The motor controller is thereby only able to control the DC motor in the first quadrant. To minimize switch losses a two transistor gate driver is implemented. These two Bipolar junction transistors is able to charge the gate of the MOSFET with a current of approximately 500 mA. The gate current is limited by R_{24} to minimize high frequency ringing on the gate. A flyback diode is coupled parallel to the DC motor terminals to ensure at current path when the MOSFET is turned of.

The main current feedback is maintained via a 2 mΩ shunt resistor in the main power line. The shunt is realized as a specific piece of PBC wire and calculated as shown in Equation 2.7.

$$R_{Shunt} = \frac{\rho \cdot length}{Area} \tag{2.7}$$

Where:
$\rho = 17{,}5\,\text{n}\Omega\,\text{m}$
$length = 4\,\text{cm}$
$Area = 35\,\mu\text{m} \cdot 1\,\text{cm}$
$\Rightarrow R_{Shunt} \approx 2\,\text{m}\Omega$

A the voltage across the shunt resistor is measured via a second order buffered low pass filter with sufficient gain. The voltage is proportional to the DC motor current. The filter

Drivetrain Speed Feedback

The drivetrain speed feedback is implemented as a Hall effect sensor in the drivetrain. This sensor triggers an interrupt on the micro controller.

Additional Analog Interfaces

A number of general purpose In/Out ports is connected to accessible solder pads for additional and "on the fly" extensions.

CAN Interface

The system and the PCB layout is prepared for CAN interfacing.

SPI Interface

The SPI interface is used to log data form the motor controller on an SD card placed on a breakout board with a level converter.

UART Interface

The UART is used for accessing and monitoring internal software parameters.

USER Interface

The User interface consists of a number of buttons in the user controls. The user is able to control the system functions via these buttons.

Each interface includes protocol specific hardware such as pull-up resistors, decoupling capacitors and analog low pass filters.

A seven point turn switch is placed in the cabin to make the driver able to adjust parameters in the cruise control while driving. The turn switch in implemented as a simple voltage divider, shown in Figure 2.7 and connected to an analog to digital converter in the micro controller.

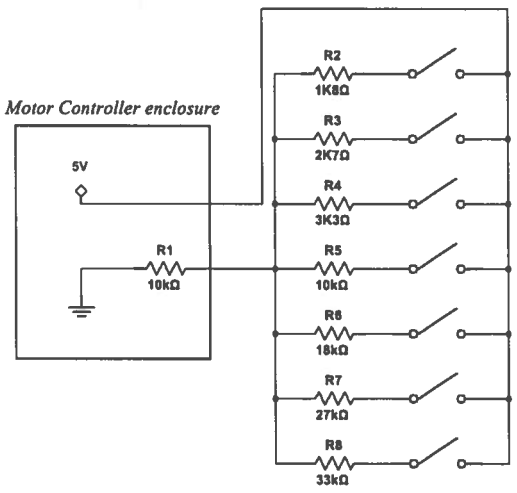


Figure 2.7: Turn switch circuit for adjusting cruise parameters.

2.1.2 Software

The software in implemented to match the state machine shown in Figure 2.8. The input parameters for the software is the speed of the drivetrain, the current through the DC

Appendices 3

3.1 Appendix A

System Block diagram

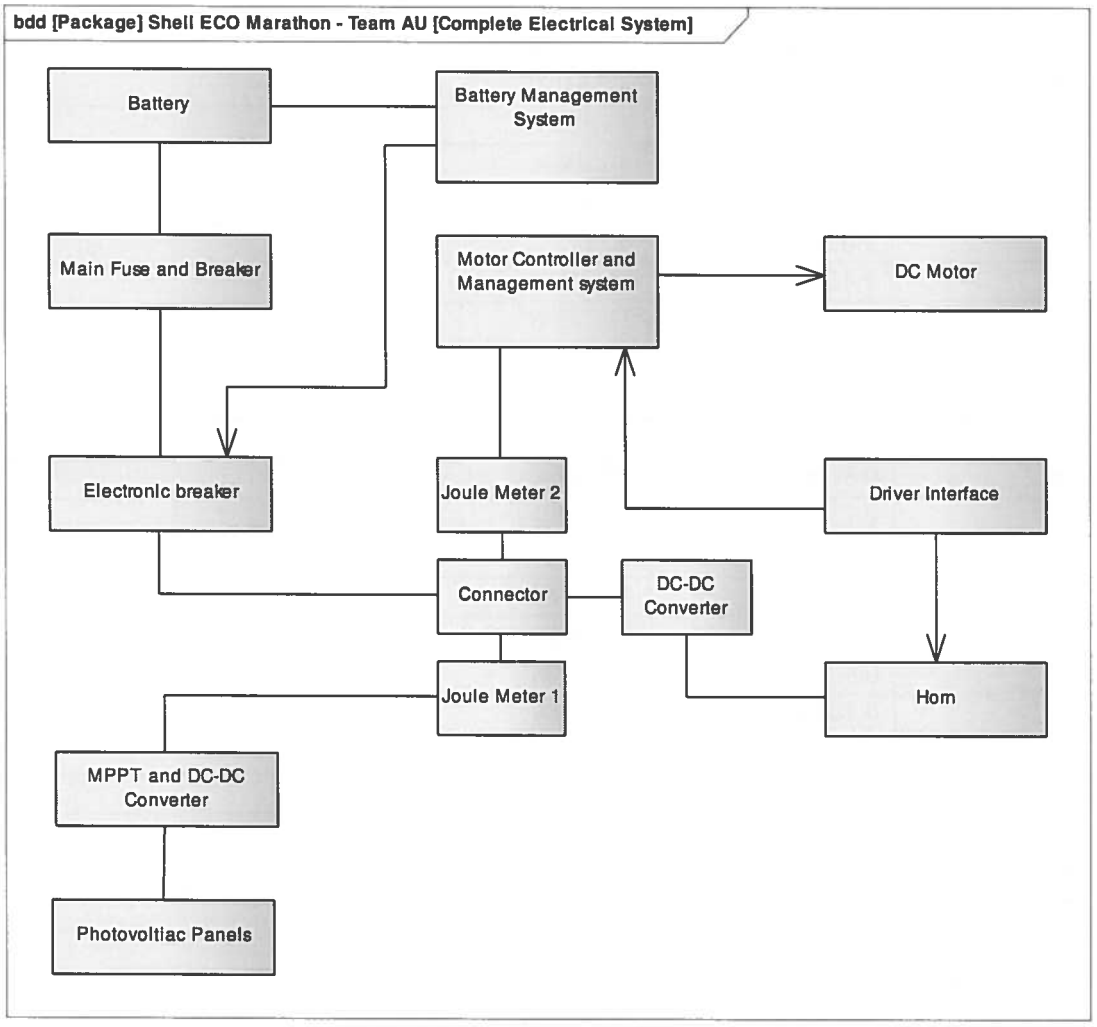


Figure 3.1: System Block Definition Diagram

3.3 Appendix C

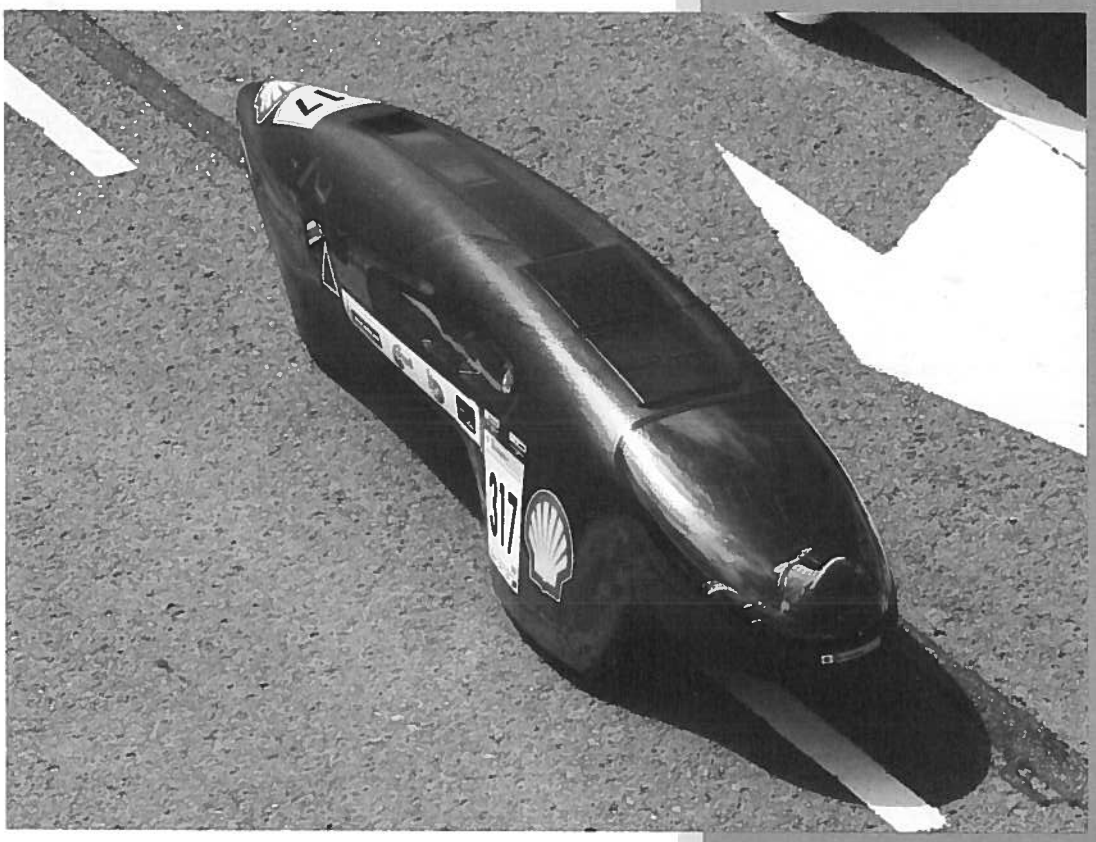
Position of system elements in vehicle

Project Documentation

2013

Propulsion Battery and Battery Management System

- for Shell Eco-marathon 2013



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Submission date: 14-06-2013

Project Manager:

Jonas Nyborg- 08325

Project number:

12105

CONTENTS

1. SPECIFICATION REQUIREMENTS

1.1. Version History

Version 1, date: 09-02-2013

Version 2, date: 16-02-2013
System Description modified, figure 1 modified, battery voltage changed to 24V on request from AU Herning, Communication protocols added.
Version 3, date: 03-03-2013
System Description improved after advice from external review. Requirements: PB_F.2, PB_F.3, BMS_F.6, PB_NF.3 and BMS_NF.7 clarified.
Version 4, date: 21-05-2013
Mechanical and documentation requirements, added to System Description. Requirements: PB_NF.5, PB_NF.6, BMS_NF.8, BMS_NF.9, BMS_NF.10 added.

1.2. Introduction

This document outlines the system to be designed, and associated specification requirements. Basic system requirements have been driven by Shell Eco-marathon official rules 2013 and interfacing agreements with other parties involved[1]. In addition, some extended battery cell surveillance features, described later in this document, has been included to increase safety and to impose the possibility of performance analysis.

[1] AU Herning (project groups working on related Shell Eco-marathon projects)

1.3.1. System Outline

The system to be designed, including external units with relevance to the specification requirements, has been outlined in Figure 1. The cell count is for illustration only. Furthermore, only main functionalities have been included.

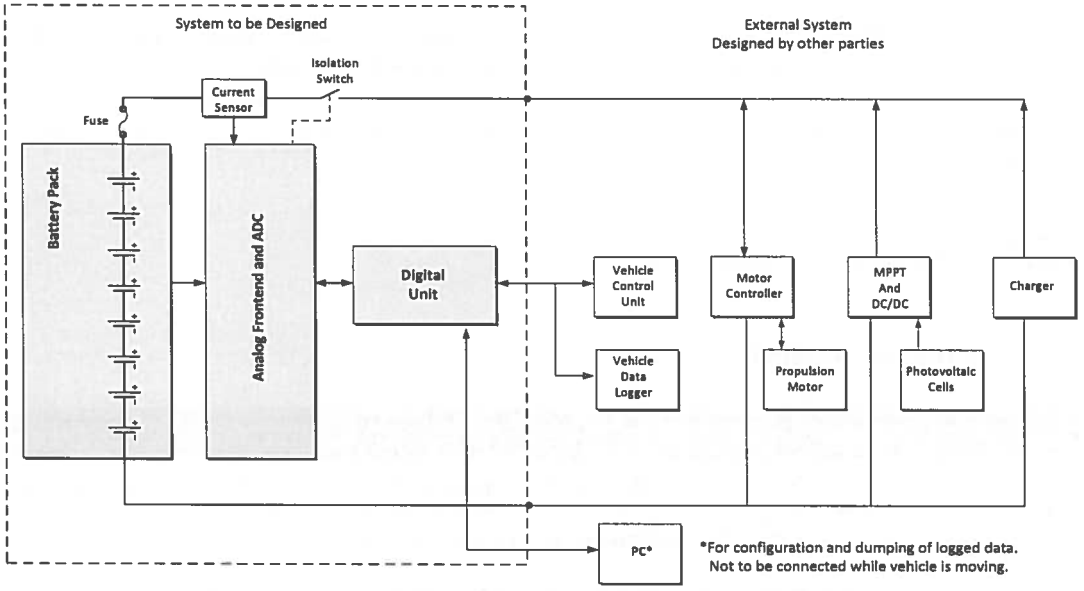

Figure 1 - Draft of Battery Pack and BMS

1.4. System Delimitation

As the duration of this project does not allow comprehensive research and design optimizing of all involved hardware units and software, the system will be delimited to certain main focus points, while other system parts will be briefly described. Below a list of delimitations:

- Off track charger will not be implemented, as a CC-CV (Constant Current - Constant Voltage) charging profile can be accomplished using a laboratory power supply.
- Analog Front End will be based on a number of ASIC's in order to reduce power consumption and time to market. As achieving lower power consumption with a custom designed Front End, within the given timeframe, is predicted to be unrealistic.
- PC software for analysis of data readout from the BMS may be briefly described, but not fully implemented.

	balance at initial connection to the BMS, gross balancing capability is not needed.
BMS_F.5	Following data must be stored in internal memory, once per minute, for later readout via USB port or SD card: • Individual cell voltages (averaged over a period of 1 minute) • battery current (averaged over a period of 1 minute) • battery temperature(s) (averaged over a period of 1 minute) • battery SOC (at time of saving) • battery SOH (at time of saving) • Error information Capacity of internal memory must hold data history of min. 10 hours
BMS_F.6	The BMS must be able to estimate SOC and internal resistance.
BMS_F.7	If the internal resistance of any cell exceeds (averaged internal resistance x 2) an error message* must be transmitted on the CAN bus, to reveal poor cell performance. * See CAN protocol DTC (5) for further details.
BMS_F.8	The actual battery and cell status must be transmitted on the CAN bus according to CAN protocol. See CAN protocol for further details.
BMS_F.9	The BMS must be able to enter a low power mode consuming less than 100mW if a undervoltage failure occurs. Low power mode will be entered after isolating the battery, so all protection functionalities may be deactivated. A pushbutton (or similar) must be available to resume normal BMS activity.
BMS_F.10	After the occurrence of an undervoltage error, the BMS must sense the connection of a charger and re-close the isolation switch, and thereby enable charging.

Table 2 - Functional requirements for BMS

1.5.2. Non-functional requirements

1.5.2.1. Propulsion Battery

Req. #	Requirement description
PB_NF.1	The propulsion battery must consist of a number of Lithium-Ion cells, leading to a nominal battery voltage within the range of 22 - 26 Volts.
PB_NF.2	All battery cells must be contained in one battery unit, as only one propulsion battery per vehicle is allowed.
PB_NF.3	The effective capacity* must be greater than or equal to 70Wh. *Capacity available at 100W load and ambient temperature of 8°C[5].
PB_NF.4	The propulsion battery must be electrically isolated from the vehicle frame and the accessory battery circuit.
PB_NF.5	Technical documentation fulfilling Article 58 of Shell Eco-marathon official rules[6] must be prepared before participation.

[4] For details see: http://liionbms.com/php/wp_balance_current.php (date: 07-02-2013)
[5] Based on average low temperature for Rotterdam in May, See: http://weatherspark.com/averages/28810/5/Rotterdam-Zuid-Holland-The-Netherlands (date: 02-02-2013)
[6] See " sem_rules_chapter01_2013" in appendices

1.5.3. Communication Protocols

1.5.3.1. CAN communication protocol

While a CAN protocol based on CANopen CiA 301 and CiA 418 standards, might be the best choice for a commercial product, as it will allow communication with chargers featuring CiA 419 communication protocol, which most likely will be the de facto standard of the future. A more simple protocol will be sufficient for this project, and ease the implementation. Therefore the Standard Traction Pack Messages has been chosen, this protocol is being used by elithion and claimed to be supported by a number of chargers.

The Original Standard Traction Pack messages can be found at:
http://liionbms.com/php/standards.php

The protocol tailored for this project can be seen below:

- CAN communication bit rate: 125 Kbit/s
- Standard addressing (CAN 2.0 A) (not extended)
- Period between data transmission: 1 second
- Multi-byte values are big-endian

ID	Bytes	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
620h	8	Company name (1)							
621h	8	Product name / rev level (1)							
622h	6	State (2)	Timer (3)		Flags (4)	DTC (5)	DTC (5)	-	
623h	6	Voltage (6)		Min Vtg (7)	Min Vtg # (8)	Max vtg (7)	Max Vtg # (8)	-	
624h	6	Current (9)		Charge limit (10)		Discharge limit (10)		-	
625h	8	Batt. energy in (11)				Batt. energy out (11)			
626h	7	SOC (12)	DOD (13)		Capacity (14)		SOC2 (15)	SOH (16)	-
627h	6	Temperature (17)	Air temper. (17)	Min tmp (18)	Min tmp # (8)	Max tmp (18)	Max tmp # (8)	-	
628h	6	Resistance (19)		Min res (20)	Min res# (8)	Max res (20)	Max res# (8)	-	

Table 5 - CAN protocol

1. 8 ASCII characters ID620h = "IHA BMS1" and ID621h = "SW: X.XX" (X.XX = numbers indicating SW version)
2. State of Propulsion battery system
    0. Fault

2. SYSTEM ARCHITECTURE

2.1. Version History

Version 1, date: 11-03-2013

Version 2, date: 10-03-2013

Software flow chart simplified.

2.2. Introduction

This document describes the System Architecture of the project "Battery Management System and Propulsion Battery". The purpose of the System Architecture is to elaborate system blocks, of the system described and specified in the "Specification Requirements", to a level allowing subsequent implementation.

As the specifications of the selected ASIC for the Analog Front End to be designed, will influence considerably on interfaces towards other system units, the selection of an appropriate ASIC has been made prior to the definition of interfaces. This has allowed a more thorough elaboration of all system units with Analog Front End dependencies.

The system outlined in the specification requirements will be described at system block level, and following be grouped in battery, hardware(HW) and software(SW) units for which internal interfaces, functionalities and requirements will be clarified.

2.4. Elaborated System Block Descriptions and Interfacing

System Blocks to be implemented are visualized in Figure 3. Sub blocks (written in Italic), outlines functionalities within the block. Functionality descriptions and design requirements for illustrated blocks are described below.

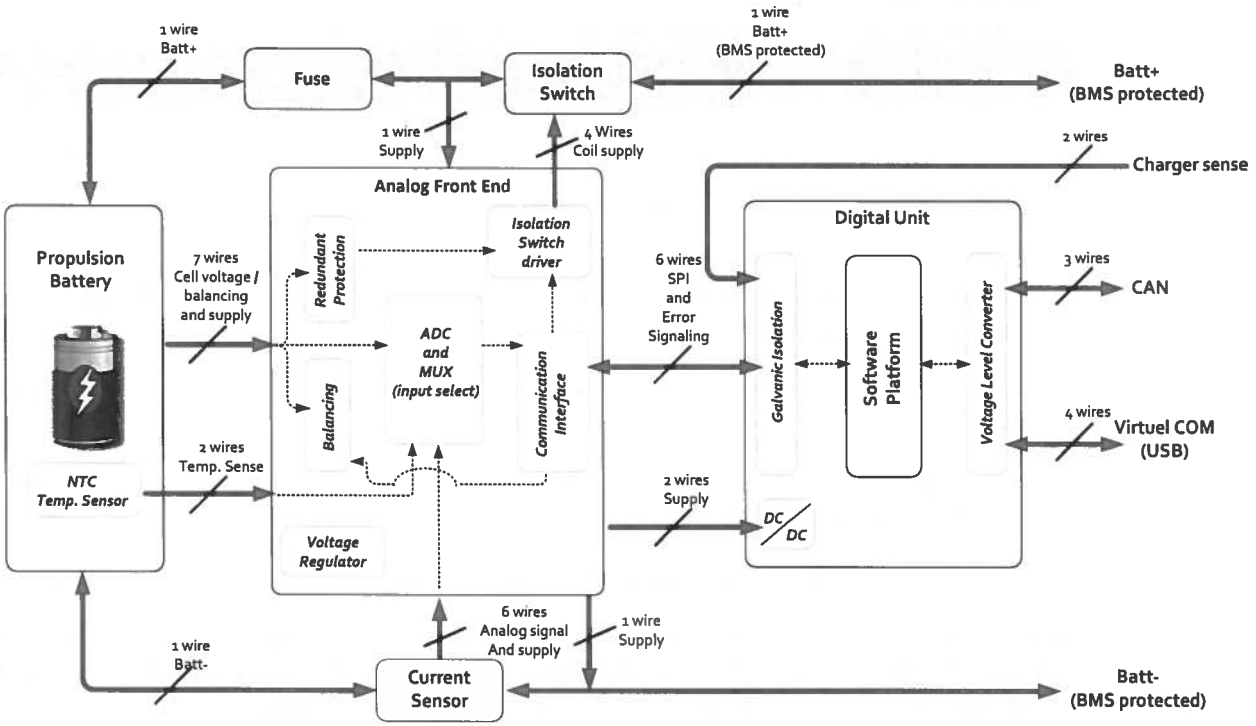

Figure 3 - Elaborated system and interfacing Diagram

Table of In-/Output Requirements

Table below specifies requirements for input and output connections of Propulsion Battery.

Connector Name	Direction	Voltage	Current	Remarks
Battery Pack Terminals				
Batt+	IN / OUT	17.5 to 30V	-15 to 50A	Fuse protected
Batt-	IN / OUT	0V	-15 to 50A	
Connections to Analog Front End and ADC				
Cell voltage / Balancing (#1 to 7 or 8)	OUT	0 to 4.8V[3]	0 to 150mA (Balancing current)	Same wires used for cell surveillance, balancing and Front End ASIC supply # of wires = cell count
Cell voltage / Balancing reference	OUT	0V		Negative terminal of lowest cell in stack
Temp. Sense+ (#1 to 5)	OUT			NTC's of type: 10KΩ at 25°C (1%), Panasonic ERT-J1VG103FA or equivalent
Temp. Sense- (#1 to 5)	OUT			

Table 8 - Connections and Signal Levels for Propulsion Battery

2.4.2. Elaborated Hardware Block Details

2.4.2.1. Analog Front End

IPO(Input, Process, Output)

Table below describes Input, process and output for Analog Front End.

Input	Process	Output
Data requests from Digital Unit.	Acquire and convert cell voltages, battery temperatures and current sensor signal to digital form. And send values to Digital Unit on request.	Measured and digitalized measurement data
Cell voltage / Balancing current		
Current sensor signal		
Cell temperature signal	Performs Balancing on request from Digital Unit.	Isolation Switch open/close signal
Balancing requests from Digital Unit	Survey cell voltages and autonomously isolate battery if SOA is exceeded.	
Isolation Switch command from Digital Unit	Drive Isolation Switch.	

Table 9 – IPO for Analog Front End

						number of connected cells
Coil -	OUT	0 to 60V	200mA min.			Open collector output
Connections to Propulsion Battery						
Cell voltage / Balancing (#1 to 16)	IN	0 to 4.8V[3]	75mA min. (Balancing current)		1MΩ min. (balancing off)	Same wires used for cell surveillance, balancing and Front End ASIC supply # of wires = cell count
Cell voltage / Balancing reference	IN	0 V				Negative terminal of lowest cell in stack, is connected to this input.
Temp. Sense+ (#1 to 6)	IN					To be configured for use with NTC's of type: 10KΩ at 25°C (1%), Panasonic ERT-J1VG103FA or similar
Temp. Sense- (#1 to 6)	IN					
AUX Vdd in	IN	17.5 to 60V			480Ω min.	Directly feed to AUX out connector
AUX Vss in		0V				
Connections to Current Sensor						
Current Sensor Vdd	OUT	5V +/-0.1V		1mA min.		Sensor supply
Discharge current signal	IN	0 to 2.5V			25KΩ min.	Sensor signal
Charge current signal	IN	0 to 2.5V			25KΩ min.	Sensor signal
$AGND_{Batt}$		0V				Analog battery ground

Table 10 - Connections and Signal Levels for Analog Front End

[1] Input Logic low: 0 to 0.8V Input Logic high: 2 to 5.2V
[2] Output Logic low: 0 to 0.5V, Output Logic high: 4 to 5.1V
[3] Not referenced to GND. As cells are stacked in series connection.

2.4.2.3. Isolation Switch

IPO(Input, Process, Output)

Table below describes Input, process and output for Isolation Switch .

Input	Process	Output
Battery current	Conduct battery current when closed. Interrupt battery current and perform galvanic isolation of battery when open.	Battery current when switch closed No current when switch open
Relay Coil+		
Relay Coil-		

Table 13 – IPO for Isolation Switch

Design requirements: Isolation switch must be a mechanical switch(contactor or relay) to meet Shell Eco-marathon requirements. And must be of normally open (NO) type to ensure that the switch will open if connection is lost or if BMS power is interrupted.

Resistance of closed switch must be as low as possible to limit dissipative loses.

As the load (motor controller) contains large capacitors, the inrush current can potentially damage the contacts of the isolation switch. The inrush current shall therefore be limited, to limit contact wear and risk of welding.

Table of Connections and In-/Output Requirements

Table below specifies requirements for input and output connections of Isolation Switch.

Connector Name	Direction	Voltage	Current	Input resistance	Remarks
Connections to Current Sensor and External Load					
Batt+	IN	17.5 to 60V	-15 to 50A		Voltage depends on number of connected cells
Batt+ (BMS protected)	OUT	0 to 60V	-15 to 50A		
Connections to Analog Front End					
Coil +	IN	0 to 30V*		150Ω min.	*Switch Closed when Coil voltage > 17.5V Switch Open when Coil voltage < 10V
Coil -	IN	0V			

Table 14 - Connections and Signal Levels for Isolation Switch

Fault	IN	5V logic[2]			10KΩ min.	Reports errors. Must generate interrupt
$DGND_{Batt}$		0V				Digital battery ground
Connections to CAN (external devices)						
CAN high	IN/OUT	2.5 to 3.5V			120Ω	Physical layer as specified in ISO 11898. Must be routed to CAN controller in Digital Unit Software Platform
CAN low	IN/OUT	1.5 to 2.5V				
CAN Gnd		0V				
Connections to USB (virtual COM for external device)						
USB 5V+	IN	5V +/- 0.25V			50Ω min.	Must generate interrupt
Data -	IN/OUT					Must be converted to UART and routed to UART of Digital Unit Software Platform
Data +	IN/OUT					
USB Gnd		0V				
Connections to Charger (external device)						
Charger Sense+	IN	17.5 to 60V				Charger Sense+ will be 0V when charger is off or disconnected.
Charger Sense-		0V				
Connections to Supply						
Aux Vdd	OUT	17.5 to 60V		50mA min.		Supply for Digital Unit.
Aux Vss		0V				Voltage depends on number of connected cells

Table 16 - Connections and Signal Levels for Digital Unit

[1] Output Logic low: 0 to 0.5V, Output Logic high: 4 to 5.1V
[2] Input Logic low: 0 to 0.8V Input Logic high: 2 to 5.2V

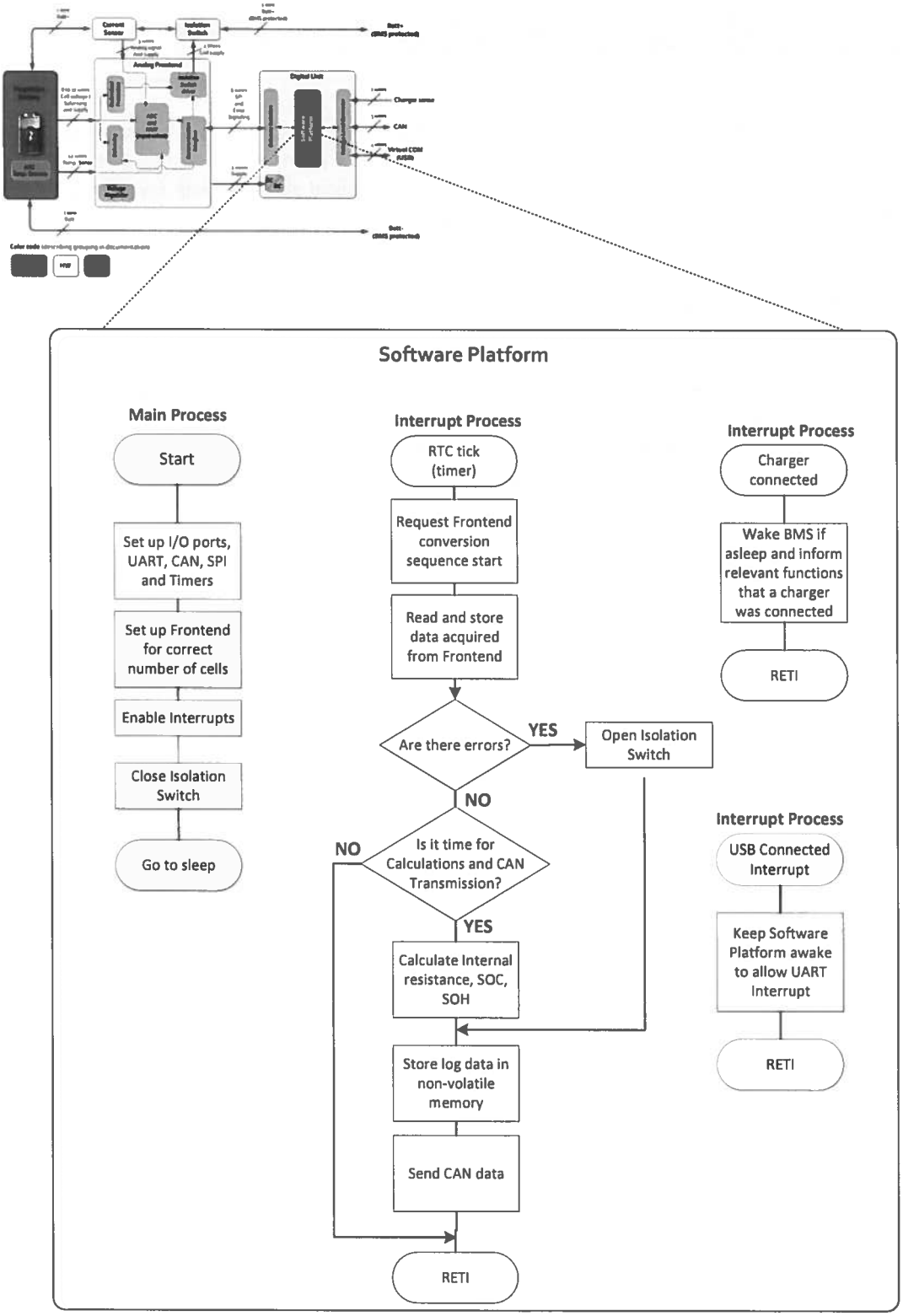

Figure 5 - Flowchart draft

3.1.1. Propulsion Battery

Based on the performed battery test,[13] Lithium-ion polymer(Li-PO) is found to be the most appropriate choice, as it offers satisfying capacity at simulated worst case Eco-marathon conditions, as well as low internal resistance and weight. The cycle life is expected to be shorter compared to LiFePO4[14], but for this application cycle life is of little concern. Only 2/3 of the stated capacity was available from the tested LiFePO4 battery at 1.33C discharge rate and 8°C ambient. In comparison the stated capacity was achieved from the Li-PO battery. The different behavior during discharge can be seen in Figure 6 and Figure 7.

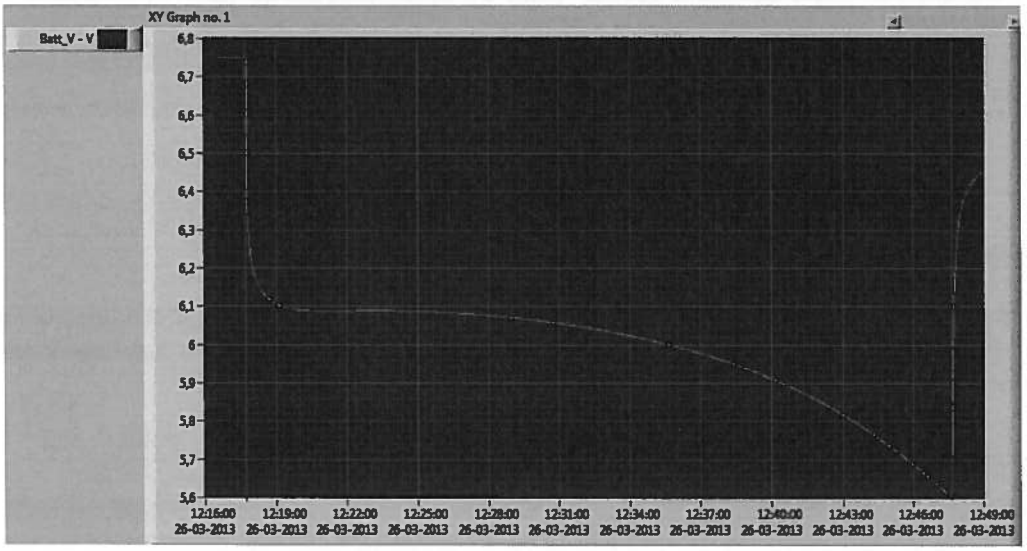

Figure 6 - Discharge of LiFePO4 under worst case Eco-marathon conditions

[13] See "Battery cell type test" in appendices
[14] http://batteryuniversity.com/learn/article/types_of_lithium_ion (date: 11-06-2013)

3.1.2. Analog Front End

As described in the system architecture the core of the Analog Front End, will be the bq76PL536A. To achieve all required functionalities external circuitry and interfacing has been implemented. Overview of Front End circuit blocks can be seen in Figure 9. Elaborated circuit descriptions will be given below.

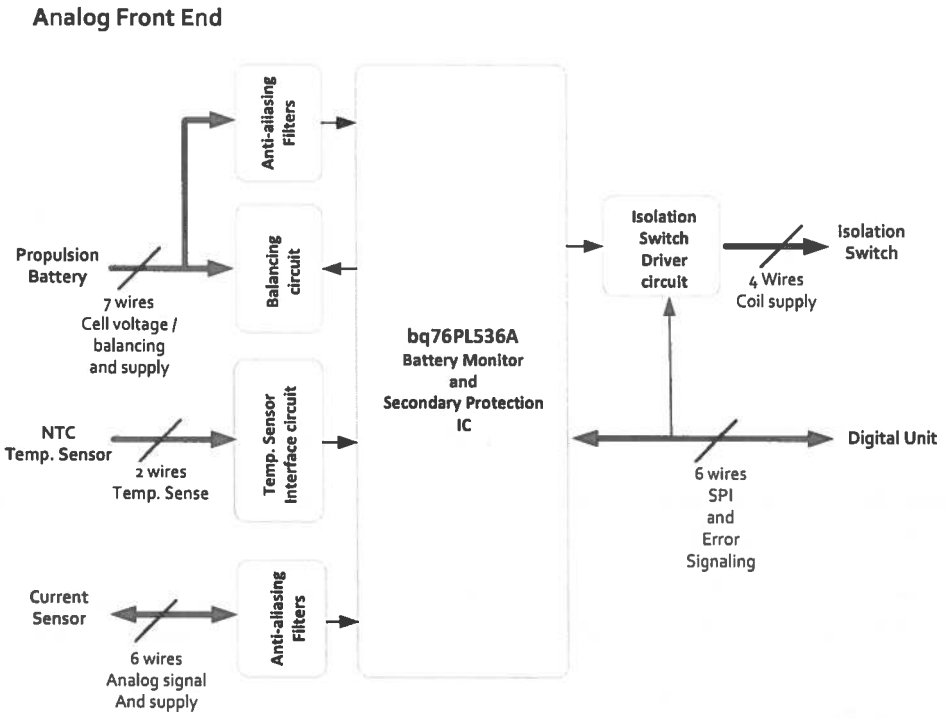

Figure 9 - Front End circuit blocks

3.1.2.1. Anti-aliasing Filters

To decrease unwanted ac noise, all signals are filtered very close to their respective ADC inputs. Cell voltages are filtered by a traditional 1.order RC low-pass filter, designed according to datasheet guidelines. 1kΩ is used as the bq76PL536A is calibrated to compensate for the voltage division created by this resistance and the input impedance. To filter the charge current signal from the Current Sensor a similar low-pass filter is applied, while the discharge current signal is filtered by a differential RC low-pass filter, filtering both common mode and differential mode noise. Schematic can be seen in Figure 10, component functionality descriptions and calculations are found below.

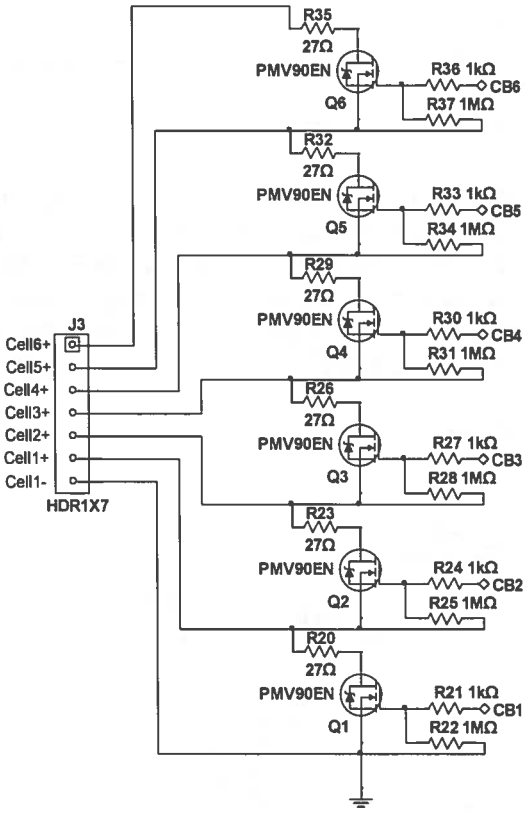

Figure 11 - Balancing circuit

Balancing component description and calculations

MOSFETS Q1 to Q6: While in saturation mode cell is partly bypassed, reducing the charging of the particular cell. PMV90EN is selected based on its low subthreshold leakage and low RDS. I_{Drain} has been over dimensioned to allow upgrade to larger balancing current.

Power resistors R20, R23, R26, R29, R32 and R35: Bleeder resistors, converting bypassed charging current to heat while its respective MOSFET is in saturation mode. To allow a proper heat transfer to PCB traces, power resistors with wide terminals has been selected. To decrease the time required for balancing a balancing current of two times the min. requirement(BMS_NF.3) has been selected.

$$dissipation\ resistance[\Omega] = \frac{Vcell[V]}{required\ balancing\ current[A]} = \frac{4\text{V(approx.)}}{150\text{mA}} = 26{,}66\Omega$$

Nearest standard value(27Ω) has been selected.

Resistors R21, R24, R27, R30, R33 and R36: Limits I_{Gate} and thereby the sink / source current required by the bq76PL536A balancing outputs at state shift(ON to OFF and OFF to ON). In theory these resistors could be excluded as Z_{out} of the balancing outputs is high.

Resistors R22, R25, R28, R31, R34 and 37: Pull-down resistors, ensures MOSFETS are off when bq76PL536A is shut down(balancing outputs are floating).

Temp. Sensor Test and Measurements

Temperature measurements has been performed using AMETEK ITC-155 A temperature calibrator. See Figure 13.

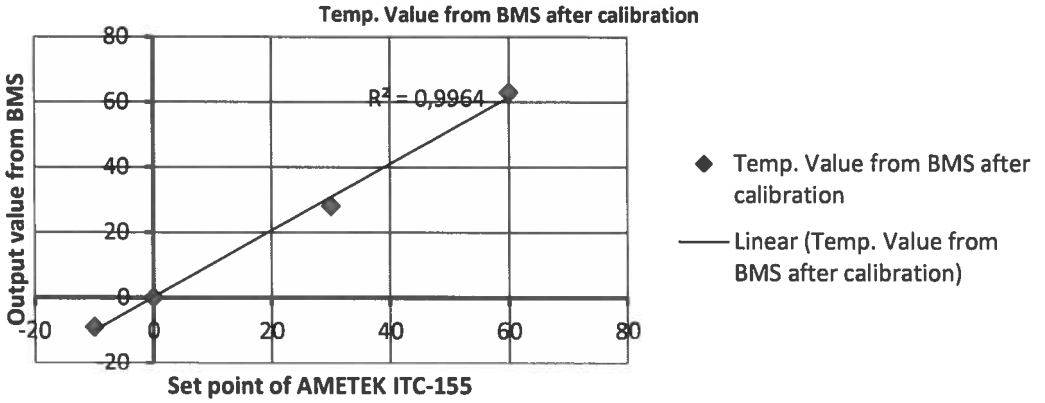

Figure 13 - Temperature measurement results compared with trend line

3.1.2.4. Isolation Switch Driver circuit

The purpose of this circuit is to allow the Digital Unit and the bq76PL536A to drive the Isolation Switch relay. To ensure the flexibility of connecting relays with any coil voltage rating, open drain topology has been chosen.

As subthreshold leakage is proportional to V_{DS} (which is equal to the battery voltage) extra attention has been paid to decrease subthreshold leakage of this driver. Therefore stacked MOSFETS[17], a technique commonly used in IC design, has been implemented to decrease leakage, this also adds a logic AND functionality, which ensures that errors detected in either the bq76PL536A or the Digital Unit will result in interruption of battery current flow, as both units must output a logic high to close the Isolation Switch.

To reduce contact wear and the risk of relay welding, a pre-charge relay driver circuit has been included. The pre-charge circuit ensures that any capacitive load will be pre-charged by a limited current to avoid an inrush current peak.

The Isolation Switch and Pre-charge relay will be discussed later.

The Isolation Switch Driver circuit can be seen in Figure 14.

[17] http://ambienthardware.com/courses/tfe01/pdfs/Roy1.pdf (date: 11-06-2013)

NOR gate U11: Ensures that any Fault or Alert detected by bq76PL536A will turn OFF Q10 and thereby open the Isolation Switch. Furthermore the gate output is send to the Digital Unit(via the galvanic isolation) to warn this unit that errors has been detected.

Isolation Switch Driver Test and Measurements

Test of this unit will be performed as part of the accept test. See accept test chapter.

3.1.3. Analog Front End Extension Module

The Analog Front End support up to 6 cells, if a larger cell count is required an extension module can be connected. This system supports up to 2 extension modules which allows connection of up to 18 cells. The extension module is similar to the Analog Front End with the exception that there is no SPI interface for connection to the Digital Unit, no Isolation Switch driver, and no input for current sensor. Furthermore the host select pin of bq76PL536A (pin 44) is pulled high to disable the SPI host interface. A draft of extension module connection can be seen in Figure 15.

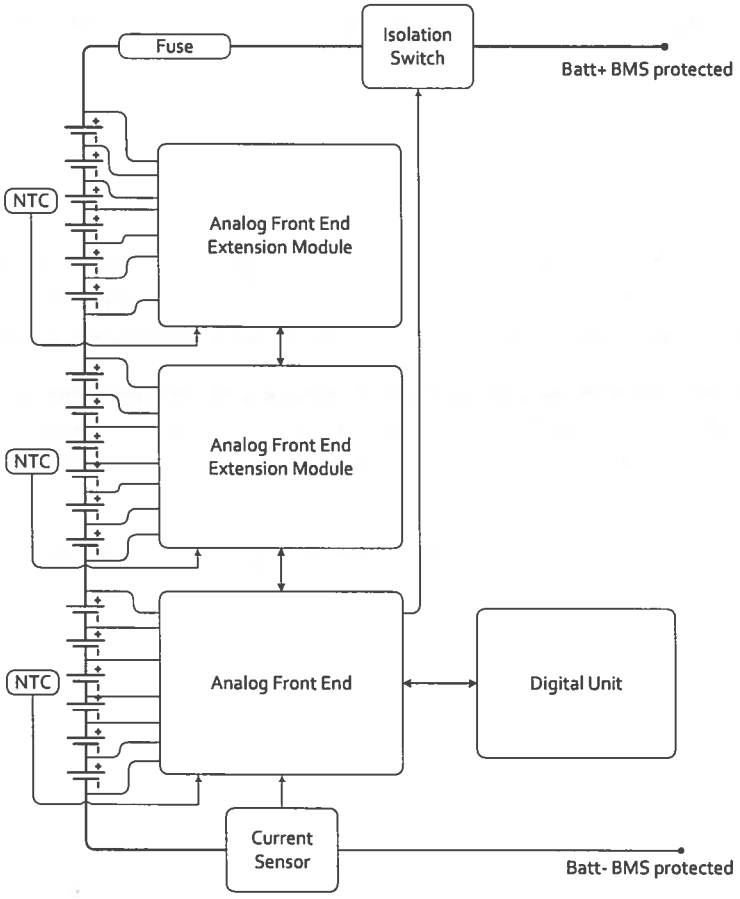

Figure 15 - Connection of Extension Modules

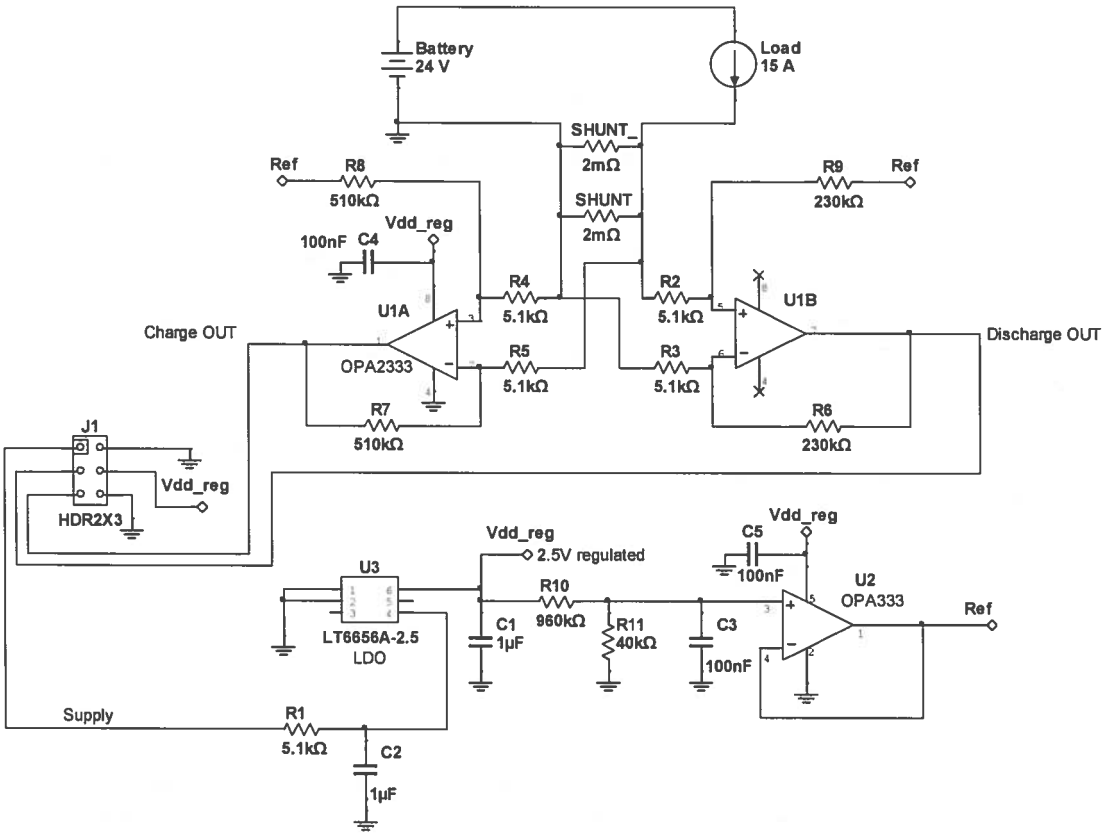

Figure 16 - Current Sensor circuit

Current Sensor component description and calculations

Voltage regulator (U3, R1, C2 and C1):

Regulator U3: A series regulator with ultra low power consumption reduces input voltage from 5V to 2.5V and significantly reduces ripple. The regulator is needed to ensure a stable reference voltage(described below). Furthermore, reducing the Op Amp supply voltage to 2.5V ensures that the ADCs won't be overdriven, even if the current to be sensed exceeds the specified maximum value. In addition, the lowered Op Amp supply voltage reduces the supply current.
Resistor R1: limits the inrush current, which must be kept below 1mA to allow direct connection to the AUX output of bq76PL536A, by using this output to supply the sensor, the sensor can be switched OFF when system is put to sleep.
Capacitors C1 and C2: Ensures stable operation of U3, and noise reduction. low ESR/ESL types has been chosen for good HF noise suppression

Reference circuit (U2, C5, C3, R10, R11):

Creates a low impedance voltage source. This reference voltage of 0.1V is needed as neither the output of U1 nor the ADC input(except the GPAI ADC input) are able to operate down to 0V.
Resistors R10 and R11: Creates a voltage divider.
Capacitors C3 and C5: Ensures decoupling.
Op Amp U2: Buffer ensuring low Z_{Out}.

Current Sensor Simulations

Simulations has been performed to verify functionality and gain calculations. Furthermore, the bandwidth and phase margin of the amplifiers has been found. See simulations below:

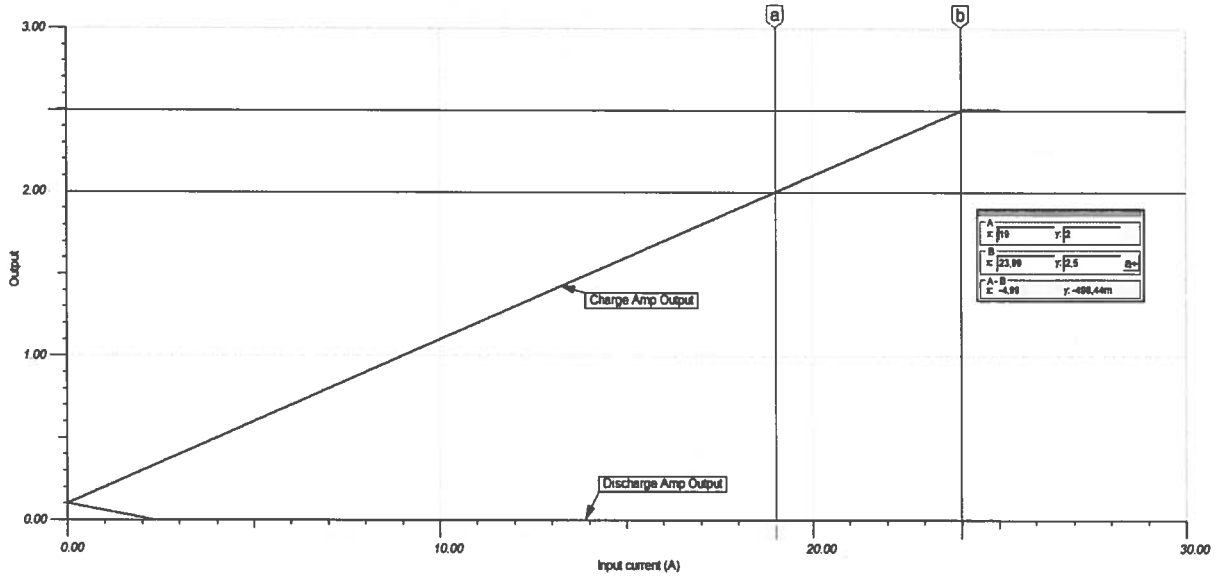

Figure 17 - DC transfer characteristics (charging)

Comment on Figure 17: Functionality is confirmed. Output voltage is 2V at a charging current of 19A as expected.

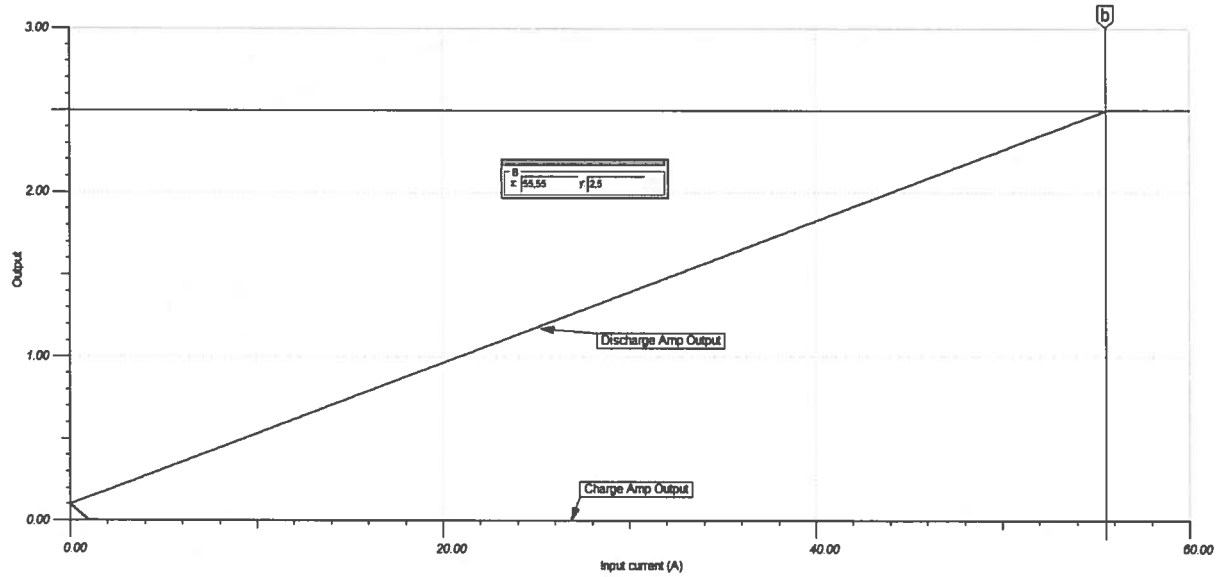

Figure 18 - DC transfer characteristics (discharging)

Comment on Figure 18: Functionality is confirmed. Output is limited by the positive rail when discharge current exceeds 55.55A, as expected.

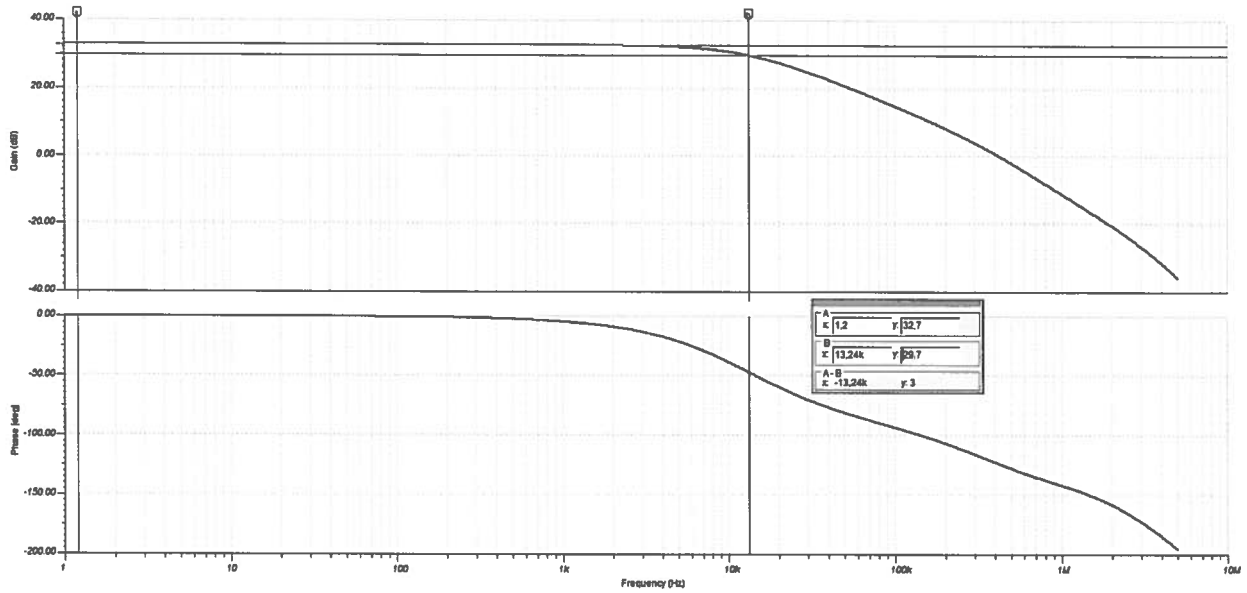

Figure 21 - Simulation of bandwidth and gain verification(Discharge current amplifier)

Comment on Figure 21: It can be concluded that the expected gain is achieved. Furthermore, it can be seen that the closed loop bandwidth is 13.24KHz.

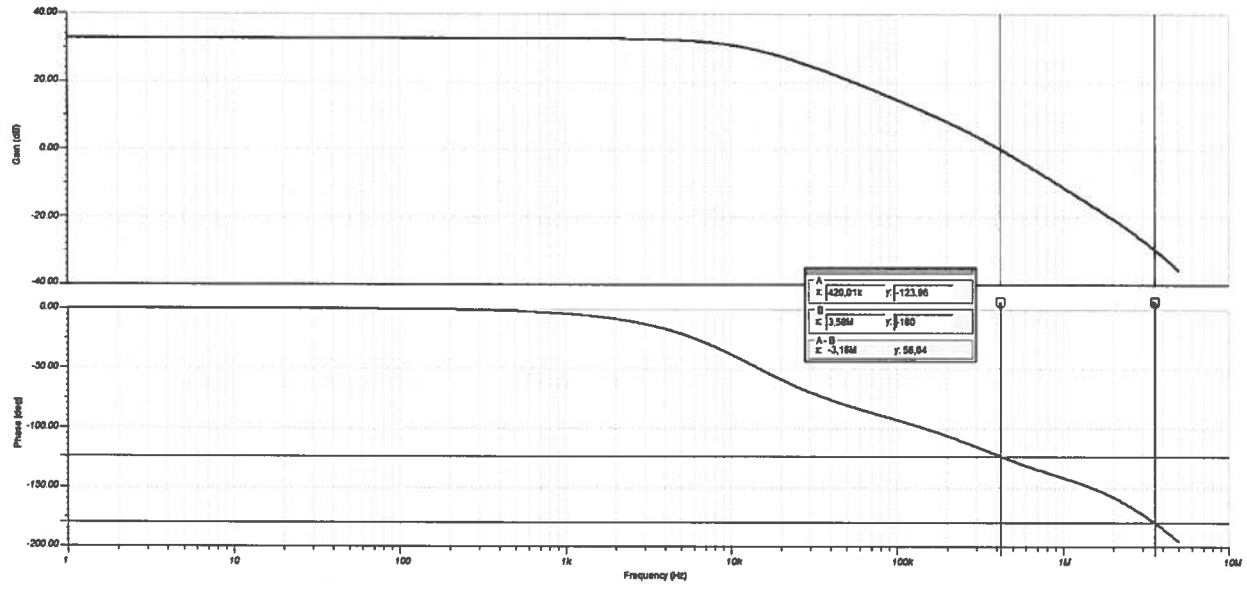

Figure 22 - Phase margin(Discharge current amplifier)

Comment on Figure 22: The phase margin is 56° for the unloaded amplifier. The phase margin must be taken into consideration if a capacitive load is applied.

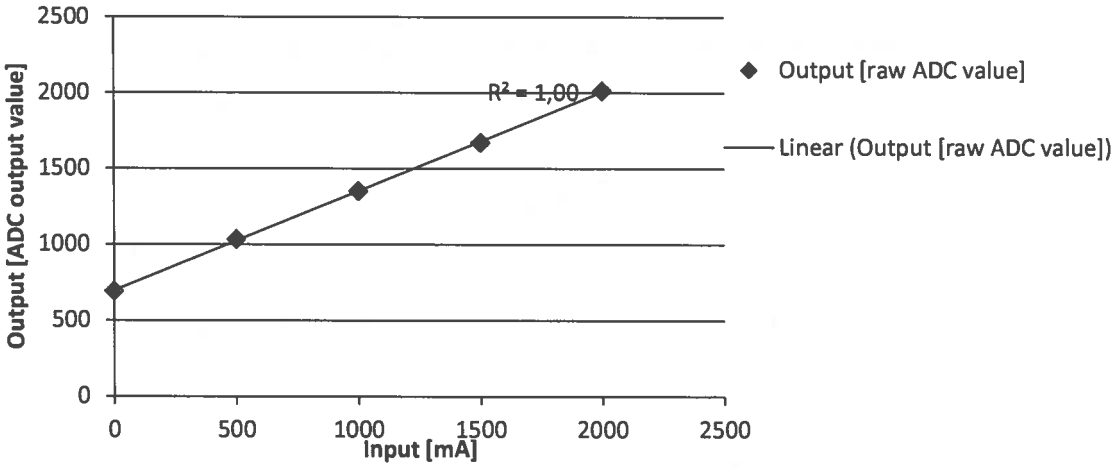

Figure 25 - Graphical presentation of measurements and trend line(Charge)

Calibration constants for the charge current sense amplifier has been found based on the trend line slope and interception point. The binary to mA conversion, implemented in the source code can be seen below:

```
if(Icharge < Ich_offset)
{
    Icharge = 0;
}
else
{
    Icharge = (unsigned long)(Icharge - Ich_offset)*1480/1000;
}
```

3.1.5. Isolation Switch

This unit consist of a isolation switch relay and a pre-charge circuit. While relays are a bad solution in an low power application, they have been considered the only solution as real physical isolation of the battery, in the event of errors, has been required by the Shell Eco-marathon committee. If this BMS is to be used in commercial applications, the Isolation Switch should be redesigned and implemented using low RDS MOSFETS, as this will dramatically decrease the supply current.

As the driver and transient protection is implemented as part of the Analog Front End, the Isolation Switch circuit is very simple and can be seen in Figure 27

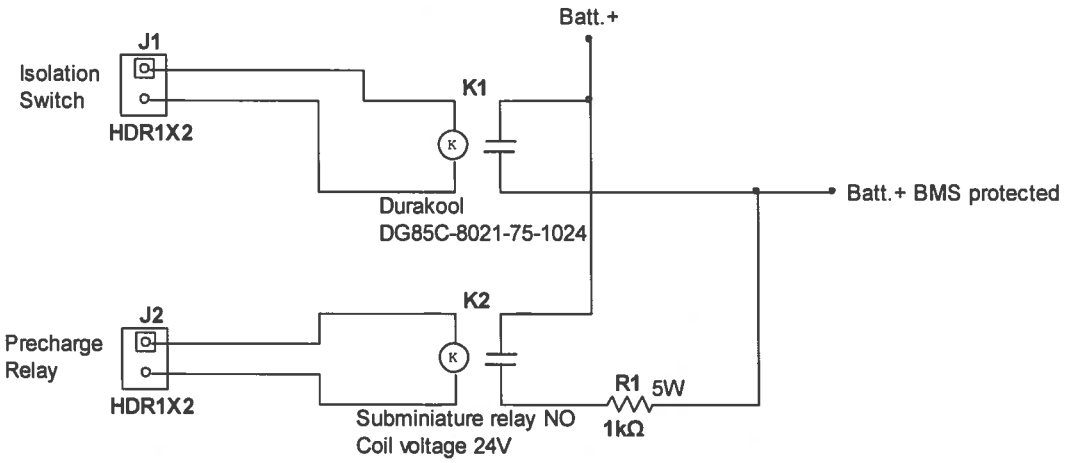

Figure 27 - Isolation Switch circuit

Isolation Switch component description and calculations

Relay K1: Isolation relay performing interruption of battery current flow. Coil voltage: 24V, Max. break current 80A.

Relay K2: Pre-charge relay, when closed the load capacity will be charged through R1.

Resistor R1: Pre-charge resistor. Limits pre-charge current to $V_{Battery}$/R1.

Isolation Switch Test and Measurements

Test of this unit will be performed as part of the accept test. See accept test chapter.

The Galvanic Isolation circuit can be seen in Figure 29.

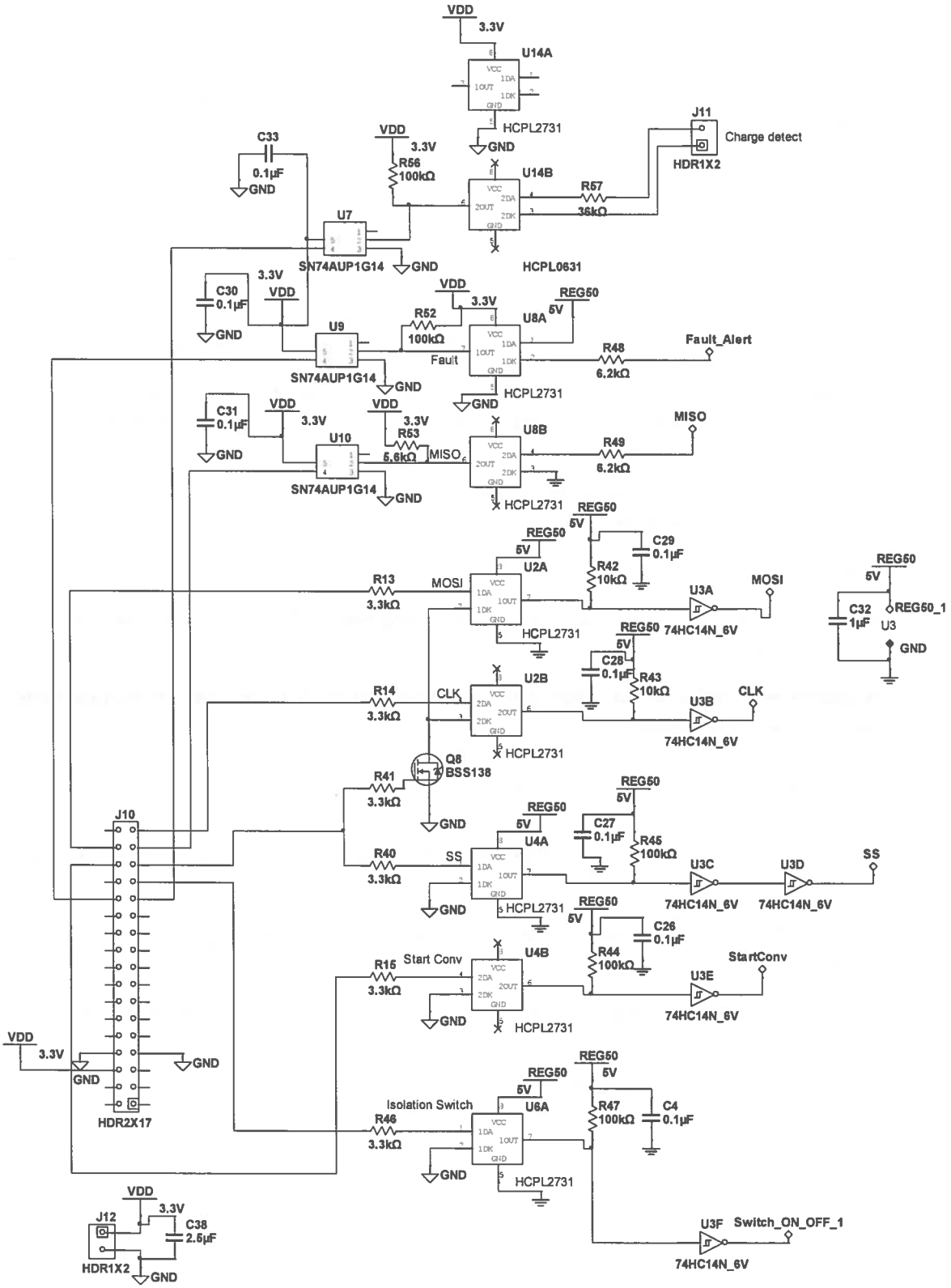

Figure 29 - Galvanic Isolation circuit

Galvanic Isolation Test and Measurements

Measurement Figure 30 confirms the expected functionality. Initial tests has been performed with weaker pull-up resistors and thereby faster fall and rise times. However, the performance was then limited by the narrowing of first bit in the first byte to be send, as can be seen in Figure 31 (As the voltage must fall from a higher level when the first bit is transferred, the output rising edge is delayed and thereby the pulse is narrowed). This issue can be solved by decreasing the SPI speed of the first byte, which was successfully implemented. However, the propagation delay then becomes a limitation. The solution has been low data transfer speed, with weak pull-up resistors and thereby low power consumption.

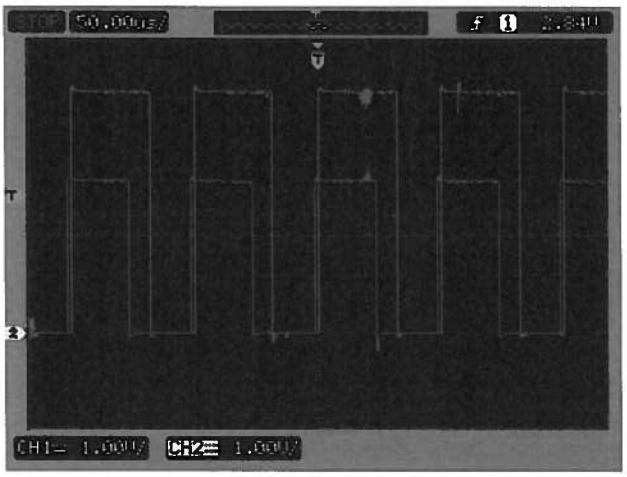

Figure 30 - Input and output of galvanic isolation (SCLK) (Green = Input)

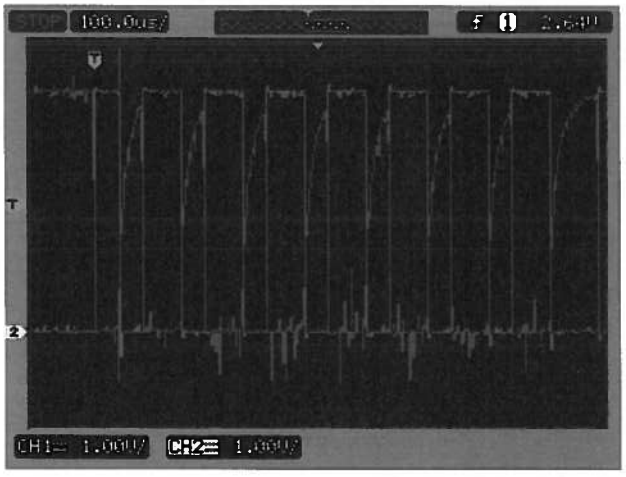

Figure 31 - Output before and after inverter

DC/DC converter component description and calculations

Flyback converter controller and switch U1: Performs and regulates the switching based on primary-side flyback pulse waveforms measured across the switch while OFF.

Capacitors C34, C4 and C5: Serves as charge reservoir, to ensure a steady input current flow. And decouples noise present at the supply rail.

Resistors R1 and R55: This voltage divider sets the low voltage lock-out threshold and hysteresis. Values has been calculated according to application note:

$$V_{UpperThreshold} = \frac{1.239V*(R55+R1)}{R1} + 2.5uA * R55 = 16.13V$$

$$V_{LowerThreshold} = \frac{1.223V*(R55+R1)}{R1} = 13.45V$$

RC snubber R3 and C3: Reduces ringing to improve EMI performance and to avoid false triggering of the boundary mode detector which is a part of the regulation scheme. The capacity has been found empirically by measuring the period of the ringing and subsequently add capacity till the period is doubled[23]. Then the appropriate series resistance has been calculated, using Equation 1.

$$C_{PAR} = \frac{C_{SNUBBER}}{\left(\frac{t_{PERIOD(SNUBBED)}}{t_{PERIOD}}\right)^2 - 1}$$

$$L_{PAR} = \frac{t_{PERIOD}^2}{C_{PAR} * 4\pi^2}$$

$$R_{SNUBBER} = \sqrt{\frac{L_{PAR}}{C_{PAR}}}$$

Equation 1 - Extracted from LT8300 datasheet page 15

Resistor R2: Feedback resistor, which determines the voltage across C1(output before LDO). Calculated based on datasheet guidelines, subsequently empirically trimmed to V_{C1} = 4V.

Shielded dual inductor/transformer T1: Used as 1:1 transformer, lighter smaller and cheaper compared to traditional transformers, the drawback is reduced coil to coil isolation(200Vac).

Schottky rectifier PMEG6002EJ: A rectifier with low forward voltage has been selected to decrease loses. Required reverse voltage and forward current has been calculated based on datasheet[24] guidelines.

Capacitor C1: Filter capacitor, a low ESR type has been selected to decrease output ripple.

Zener diode D2: When the converter is unloaded, the output starts to climb, in this situation D2 will start conduct and thereby act as a light load, which prevent further climbing. This ensures a lower no-load quiescent current compared to a resistive preloading. It does however impose the need of a low drop out regulator at the output.

LDO U2: Low dropout regulator, required as technique mentioned above allows some voltage climbing which is not tolerable at the converter output. The dropout is kept low to decrease the negative impact on the efficiency.

Capacitors C2 and C6: Required for stable operation of U2 and noise reduction, low ESR/ESL types has been chosen for good HF noise suppression.

[23] Method extracted from LT8300 datasheet.
[24] See "LT8300 - flyback converter IC" in appendices

Figure 35 - Switching noise (yellow = Vdrain, green = Vout)

The ringing created at switch ON results in a $Vout_{Peak}$ which exceeds the maximum voltage tolerated by the digital circuits which are to be supplied by this dc/dc converter. Therefore filtering has been implemented in terms of a ferrite bead. The output wires are wound two turns around this ferrite bead resulting in a significant reduction as seen in Figure 36 (A 15nF capacitor was mounted across load resistor, to simulate decoupling capacitors present at digital circuits to be supplied).

Figure 36 - Output ringing before and after ferrite bead filtering