Description of Electric System [for Technical Inspection SEM 2014]

System Description

The system consist of a Lithium-ion polymer propulsion battery, and a Battery Management System (BMS) tailored to survey this battery chemistry. The system features a Digital Unit able to analyze safety relevant parameters and interrupt the current if any parameter exceeds allowable threshold. Furthermore, to ensure maximum safety, redundant protection, independent of the Digital Unit, has been implemented as part of the analog frontend, which handles the measurements at cell level, and like the Digital Unit is able to interrupt the battery current. protection thresholds, battery data, etc. can be seen below, in the chapter: Safety related Information.

Block Diagram and Block Description

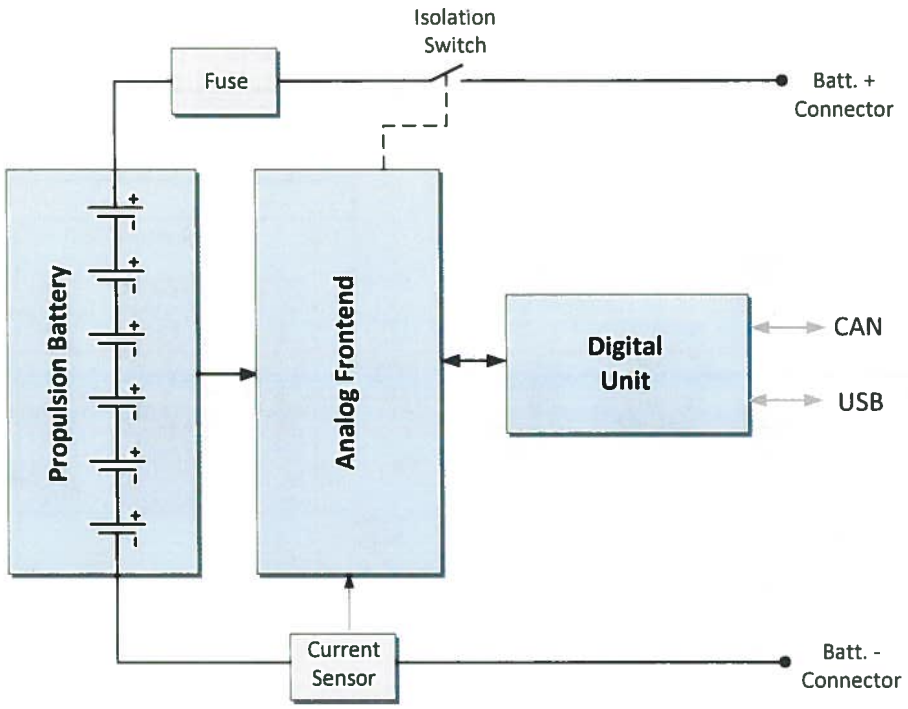


Figure 1 - general block diagram

Propulsion Battery

This unit, consisting of 6 Lithium-ion polymer battery cells, is responsible for storage of electrical energy. It captures energy from an external charger, solar panels and regenerative braking. And is capable of delivering the current needed to propel the propulsion motor.

Analog Frontend

This unit performs measurements and analog to digital conversion of cell voltages, battery temperatures and signal from current sensor. Furthermore it handles cell balancing on request from the digital unit, and redundant battery protection independent of the digital unit.

Current Sensor

Senses value and direction of battery current, and present this to the Analog Frontend.

Isolation Switch

This unit enables the BMS to interrupt the battery current.

Digital Unit

Collects measured values from the analog frontend and perform calculations and estimations of cell and battery parameters. Furthermore it handles communication with external units.

Elaborated Block Diagram

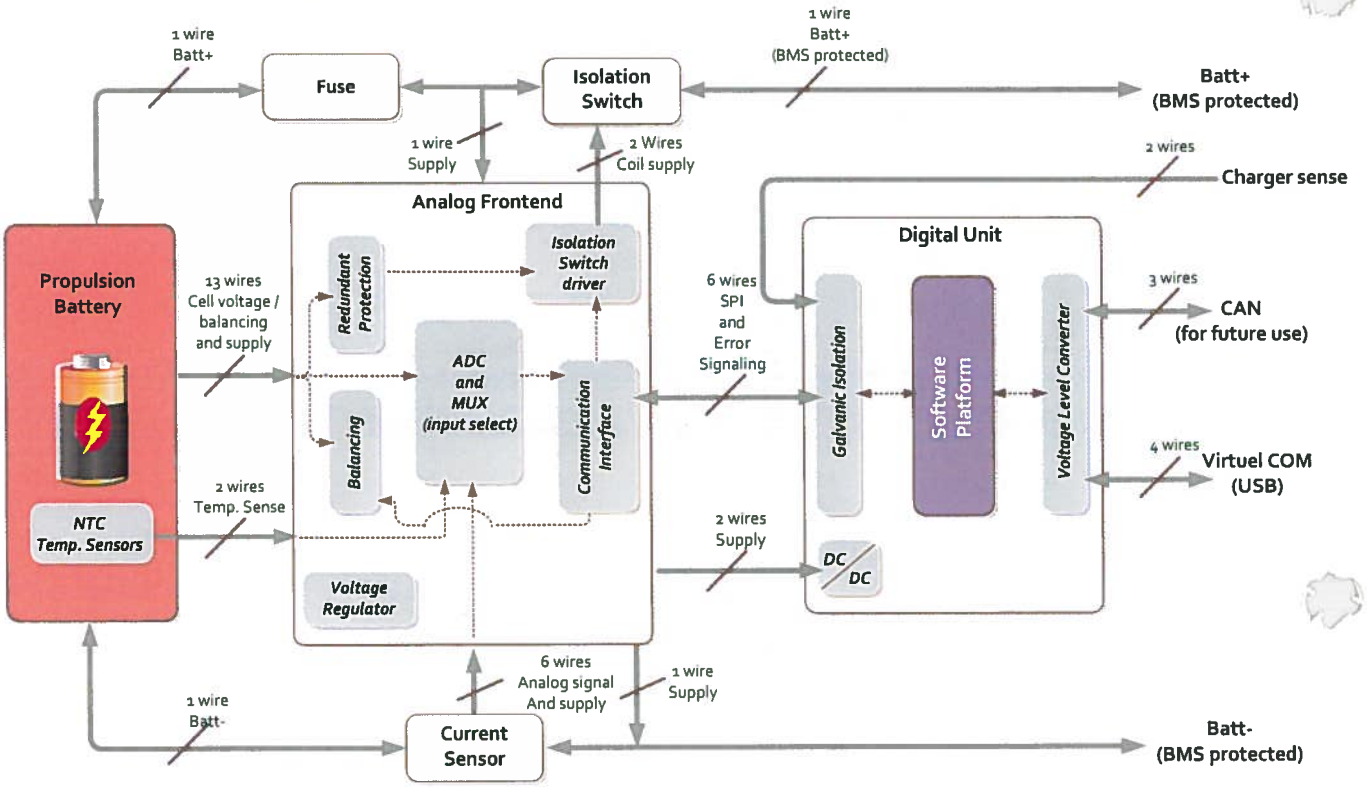


Figure 2 - elaborated block diagram

Safety related Information

Battery Data:

Chemistry: Lithium-ion polymer(Li-cobalt)
Manufacture: Turnigy
type: nano-tech
Nominal voltage: 44.4V

Max. charging voltage: 50.4V
Min. voltage: 36V
Capcity: 1300 / 2200mAh (depends on weather and achieved efficiency)
Max. continues discharge: 25 / 35C
Max. charge rate: 5 / 8C

Fuse Data:

Type: KLK 20 fast-acting fuse
Nominal current: 20 A
Interrupt Rating: 50KA

Isolation Switch(relay) Data:

Manufacture: Panasonic
Type: HE1ANS48
Contact type: Normally Open
Max. continues current: 30A
Max. Break current: 30A
Nom. coil voltage: 48V

Parameters under surveillance, and action at out of range

Parameter	Action at out of range	Action required to reset
Cell voltage	Undervoltage: Battery is isolated from load, BMS goes to deep sleep to reduce consumption. Overvoltage: Battery is isolated from charger, bleeder resistor is applied across cells exceeding threshold, to force voltage down.	Undervoltage error is reset at connection of charger. Overvoltage error requires press at reset button.
Battery Temperature	Isolates battery from load/charger	Requires removal of error condition and press at reset button.
Charge current	Isolates battery from load/charger	Requires removal of error condition and press at reset button.
Discharge current	Isolates battery from load/charger	Requires removal of error condition and press at reset button.

BMS Threshold levels, primary protection levels

Parameter	Upper threshold / delay	Lower threshold / delay
Cell voltage	4.19V / 201ms(max.)	3V / 201ms(max.)
Temperature (charge)	45°C / 201ms(max.)	0°C / 201ms(max.)
Temperature (discharge)	60°C / 201ms(max.)	-20°C / 201ms(max.)
Discharge current	20A / 10sec (25A / 201ms(max.))	-
Charge current	8A / 201ms(max.)	-

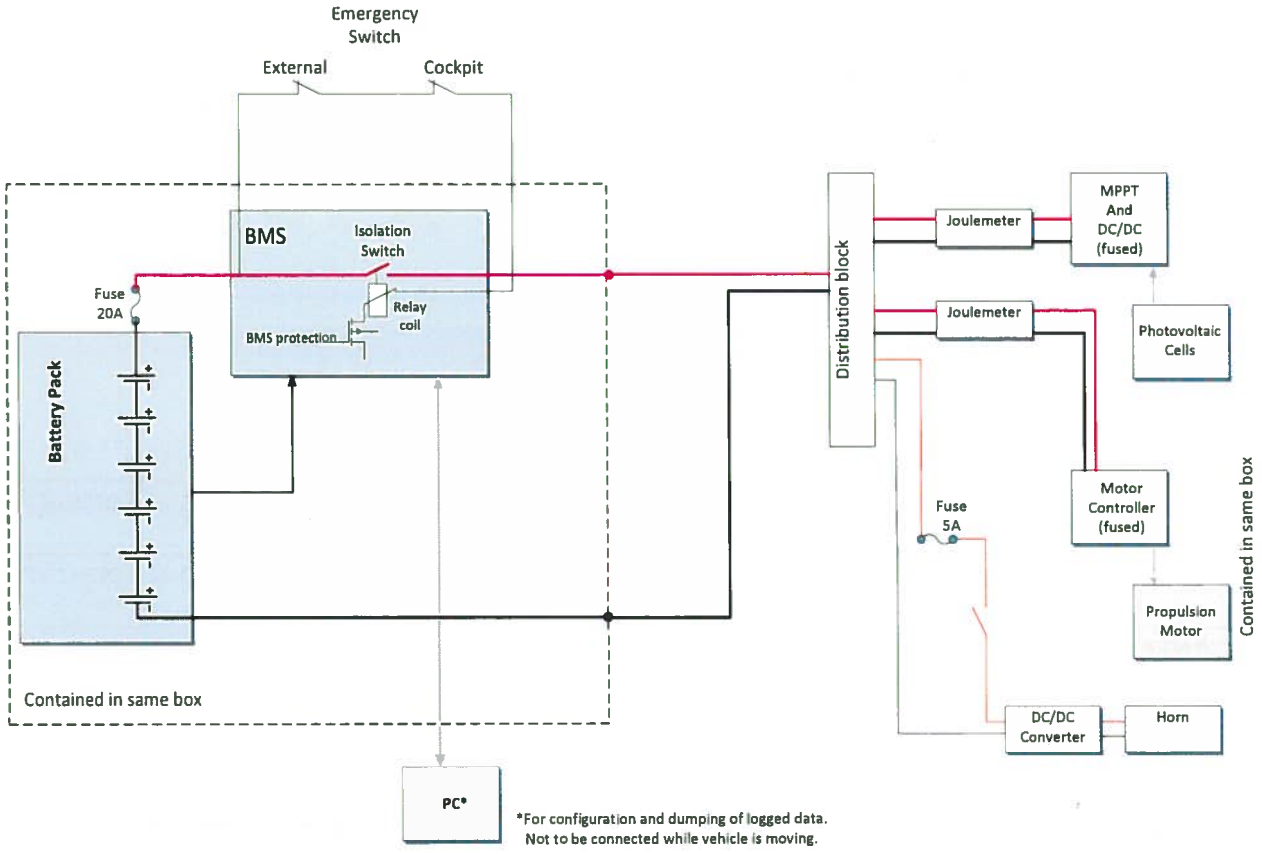
BMS Threshold levels, redundant protection levels

Parameter	Upper threshold / delay	Lower threshold / delay
Cell voltage	4.2V / 500ms	2.9V / 100ms
Temperature	60°C / 20ms	-
Charge current	19A / 20ms	-

Cell Balancing

Dissipative balancing is performed based on final-voltage algorithm. When charger is connected and any cell exceeds 3.8V, the internal resistance is measured for all cells, to allow calculation of OCV's. Based on OCV's, cells with highest SOC is being partly bypassed by a resistor, to reduce the charging current to these cells. This procedure is being performed until all calculated OCV's are within a 30mV range. Balancing current is approximately 150mA.

Connection Diagram



Motor Controller

Shell ECO Marathon Team AU 2014

Simon Møiniche Skov

Anders Fiilsøe Ramsing

Christoffer Graversen

Contents

Preliminary work 1

This chapter describes the work performed to get to grips with the functionality of the complete system. The chapter will cover system diagrams, requirements specifications and use case models.

1.1 Requirements

1.1.1 Description

The motor drive system has to fulfill the requirements to qualify for participation in Shell Eco-marathon. Functional requirements are derived from SEM[1], OOD[2] and the BMS[3]. The internal structure of the motor drive system is depicted in Figure 1.1.

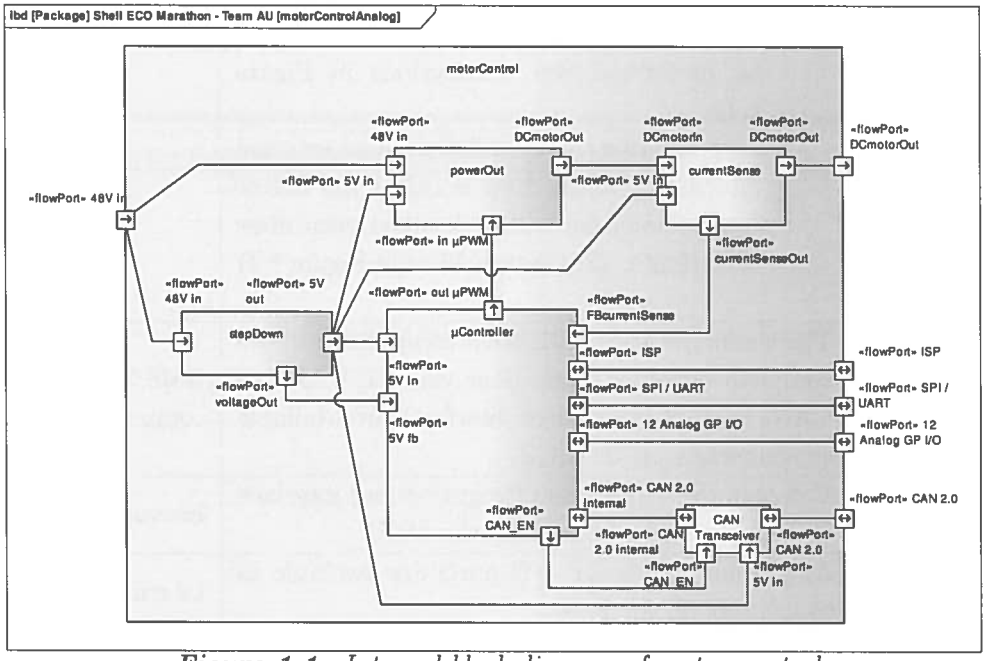


Figure 1.1: Internal block diagram of motor control

To ease the use of the individual requirements, each requirement is given a specific number in the form of mC.x-x.

[1]SEM global official rules 2014.
[2]Reports and conclusions on optimization of the drivetrain.
[3]Documentation of the battery management system.

1.1.2 Functional requirements

Motor control Functional requirements

Interfacing		
Req.#	*Requirement description*	*Reference*
mC.1-1	Accessing and setting of internal functions and parameters in the system while driving is done via the analog GP I/O interface. Listed beneath is all the functions and parameters controlled and accessed via the analog interface. • A drivetrain speed feedback is available in the form of pulses from a sensor mounted in the drivetrain. • Lower and upper speed limits for the burn and coast, see Figure 1.3, can be adjusted from zero to max speed in steps of 1 km/h. Upper limit will always be at least 1 km/h higher than the lower limit. • Go function can be called from an external interrupt. When Go is called and the speed is equal to zero, the launch procedure will be performed. If Go is called and speed is different from zero, the cruise procedure will be performed.(See transactions in Figure 1.4) • Stop function can be called from an external interrupt. When Stop is called the motor controller output will be disabled, regardless of the state. (See transactions in Figure 1.4)	Internal Requirements and OOD-Section 23.5(Montering af hastighedssensor)
mC.1-2	The communication with other components of the complete system is either done via SPI, UART or CAN. Each of these three interfaces are available as connectors on the PCB.	BMS Section 1.5.3.1.(CAN communication protocol)
mC.1-3	A six pin ISP (In-System Programming) interface is available for programming the MCU.	Internal Requirements
mC.1-4	Additional analog GP I/O ports are available as connectors on the PCB.	Internal Requirements
mC.1-5	The power input is rated to 15 A@12 V - 75 V	Internal Requirements

Internal Boundaries		
Req.#	***Requirement description***	***Reference***
mC.1-6	To supply the control circuit an internal supply of 100 mA@5 V is needed. *Tolerance:* V_{CC}: 4,8 V - 5,2 V	Internal Requirements
mC.1-7	A step down converter with a voltage input range of 12 V-75 V, and an output of max. 380 mA@5 V is implemented in the system.	Internal Requirements
mC.1-8	The internal current sense has a resolution of approximately 330 mV/A through a buffered low pass filter.	Internal Requirements
mC.1-9	The output is controlled by adjusting the duty cycle of the internal PWM signal. • Voltage: 0 V-5 V *Tolerance:* Low_{max}: 0,7 V $High_{min}$: 4,2 V • Current: Max. 40 mA • Frequency: Adjustable from 15 kHz - 100 kHz	ATmega64M1 datasheet section 28.2(DC characteristics)
Power output		
Req.#	***Requirement description***	***Reference***
mC.1-10	The components of the power output has to be able to handle a continuous max current of 15 A@75 V	OOD-section 14.3(Delkonklusion) (200 W DC motor)
mC.1-11	The motor drive is only able to operate DC motor in 1^{st} quadrant of the I_A-N_{rpm} plane, Figure 1.2	Internal Requirements
mC.1-12	The output control is based on the burn and coast principle, Figure 1.3	OOD-section 16.2(Simuleringscyklus)
mC.1-13	Launch procedure is implemented as a ramp acceleration derived from a torque curve available from the test bench group. An array of ten integers is made in the software to define the current output according to rpm in the acceleration ramp.	OOD-section 16(Accelerations Principper)
mC.1-14	The output control is maintained via feedback from both output current and drivetrain speed.	Internal Requirements

Table 1.1: Functional requirements table

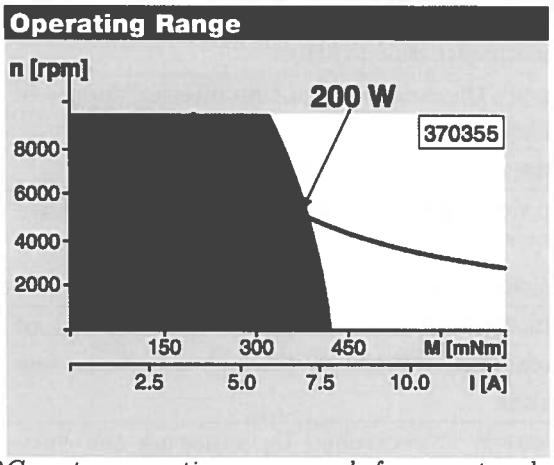


Figure 1.2: DC motor operating area graph from motor datasheet, available area in this system is 1^{st} quadrant.

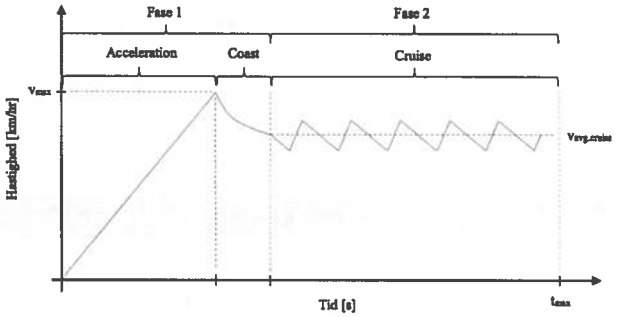


Figure 1.3: Graph on burn and coast principle from OOD-section 16.2(Simuleringscyklus). Higher and lower speed limits are at to top and the bottom of the sawtooth respectively

1.1.3 Non-functional requirements

Motor control Non-functional requirements

Rules and Regulations		
Req.#	***Requirement description***	***Reference***
mC.2-1	Sufficient overload protection has to be incorporated in the electrical cucuits. Fuses are incorporated to accommodate various current ratings in the system. Output current is furthermore limited by the control system.	SEM-Article 57:e
mC.2-2	The system is incorporated in a transparent enclosure/ the enclosure has to have a transparent lid.	SEM-Article 57:l
mC.2-3	Text "SEM" has to be incorporated in the mask of all PCB's.	SEM-Article 67:a

Table 1.2: Non-functional requirements table

1.1.4 Functionality

The use of the system is simplified to the use om two buttons "Go" and "Stop". The functionality is described in the state machine in Figure 1.4.

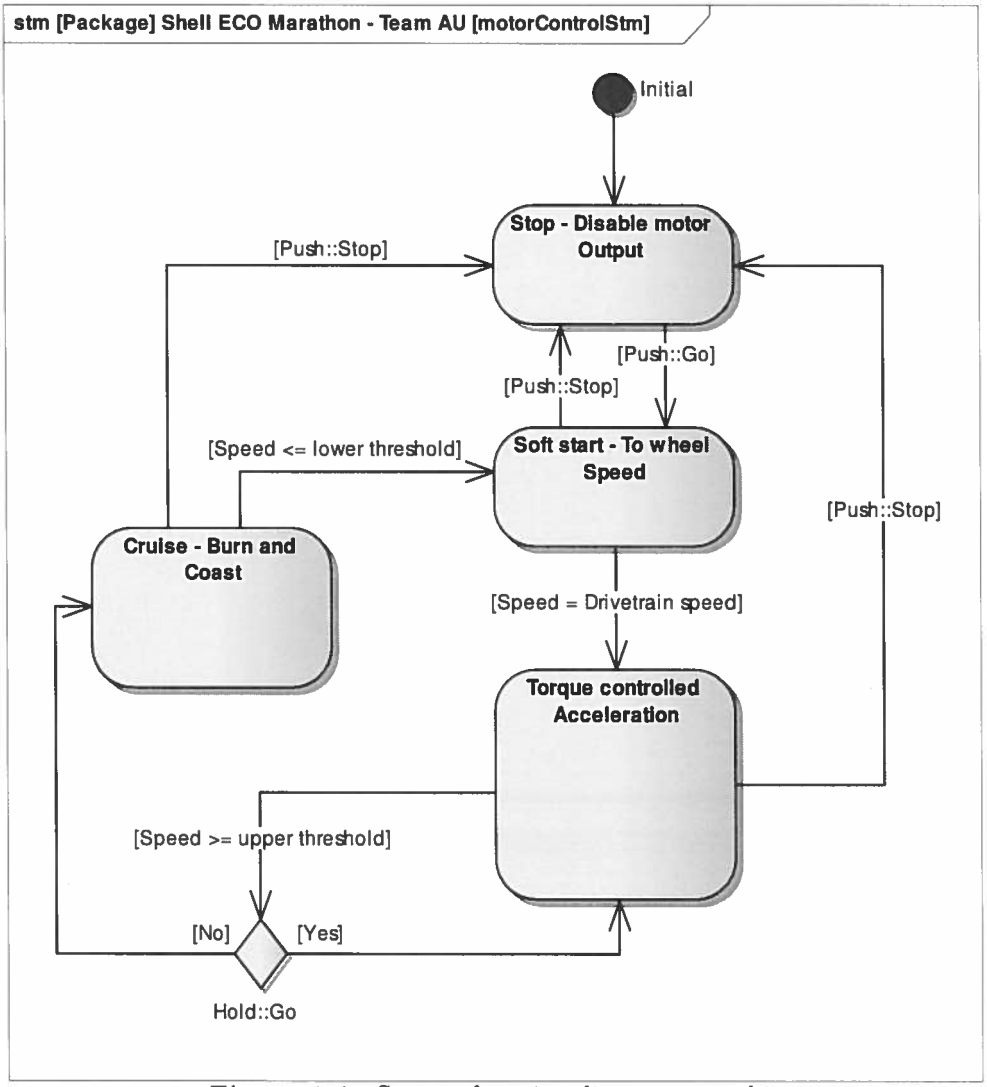


Figure 1.4: System functionality state machine

Design and Implementation 2

The purpose of this chapter is to describe the design of the motor controller in details, both for the hardware and the software. For the hardware a graphical schematic will be given and the purpose of each element will be described with its considerations and equations. The software will be described by graphical UML diagrams and element functionality for each section.

2.1 System Description

The system description summarizes the considerations and design choices of the system.

2.1.1 Hardware

The complete Hardware circuit is designed as shown in the schematic in Figure 2.1, and implemented on a printed circuit board. Considerations about spacing, EMC and high frequency noise has been made prior to the physical implementation. In this section the functionality of each subcircuit of the hardware is described in details.

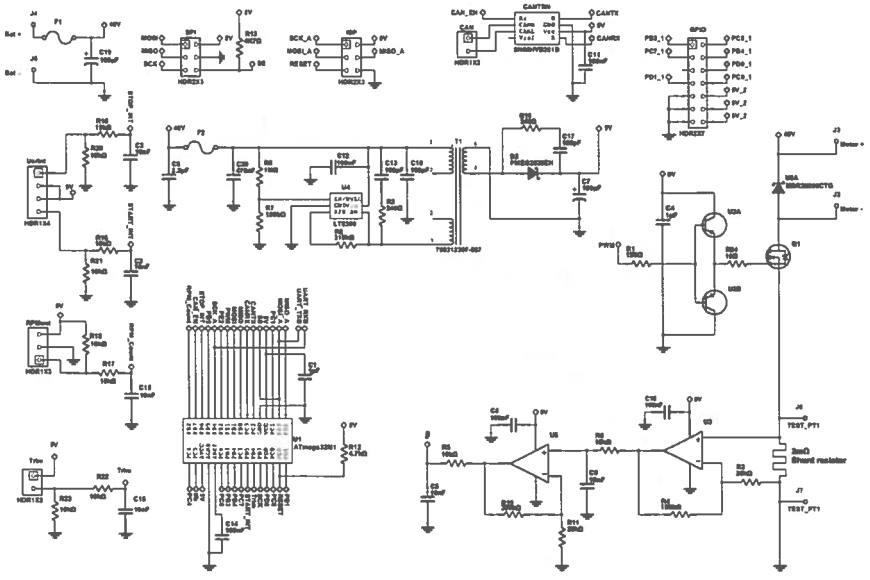


Figure 2.1: Complete motor controller circuit

2.1.1.1 Input and Main Protection

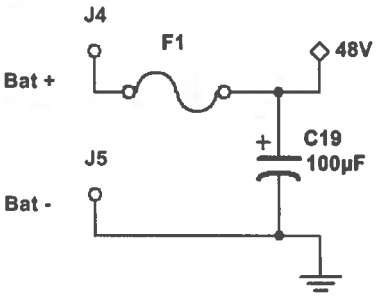


Figure 2.2: Input circuit including protection an voltage stabilization

The main protection of the motor controller is dona via a sand filled fuse rated 250 V@16 A. The fuse acts as both overcurrent and short circuit protection. Cables protected by this fuse is sized to 2,5 mm^2, cable size is chosen according to the table in Appendix B, Section 3.2. Furthermore the input voltage is stabilized by a 100 µF electrolytic capacitor.

2.1.1.2 Micro Controller Circuitry

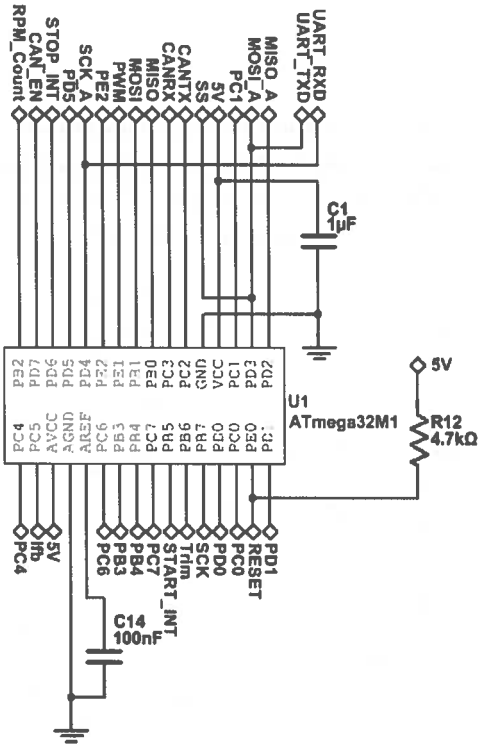


Figure 2.3: Micro controller circuit

The circuitry around the AVR micro controller is made accordingly to the AVR042 application note on Hardware design considerations. The decoupling capacitors are placed physically close to the micro controller to provide sufficient decoupling of all signals.

For better noise performance the AREF pin is connected to GND via a noise reduction capacitor as described in ATmega32M1 datasheet section 21.

2.1.1.3 Switch Mode Step Down Converter

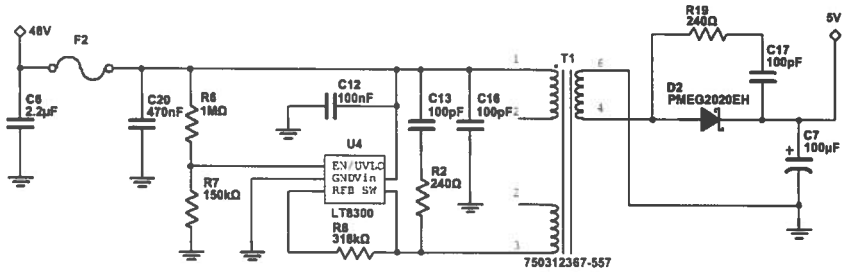


Figure 2.4: Switch Mode Step Down Converter

The voltage step down from the system supply voltage to the control circuit voltage is achieved with at switching mode step down converter. The switching converter provides a significant improvement in efficiency compared to a LDO. The circuit is adapted from the datasheet of the LT8300 controller, and is customized to meet the system specifications. All design details are chosen according to the applications section in the LT8300 datasheet.

To meet the specifications of the dynamic input voltage from 12 V - 75 V the input resistors of the step down converter is chosen as shown in Equation 2.1.

$$R_7 = \frac{V_{Pin} \cdot R_6}{I_{Pin} \cdot R_6 + V_{in} + V_{Pin}} \tag{2.1}$$

Where:
$R_6 = 1\,\text{M}\Omega$
$V_{Pin} = 1{,}239\,\text{V}$
$I_{Pin} = 2{,}5\,\mu\text{A}$
$V_{in} = 12\,\text{V}$
$\Rightarrow R_7 \approx 150\,\text{k}\Omega$

The control circuit is specified to operate at 5 V. This is achieved by calculating the correct value of R_8 as in Equation 2.2.

$$R_8 = \frac{N \cdot (V_{out} + V_f)}{I_{fb}} \tag{2.2}$$

Where:
$N = 6$
$V_{out} = 5\,\text{V}$
$V_f = 0{,}3\,\text{V}$

$I_{fb} = 100\,\mu A$
$\Rightarrow R_8 \approx 318\,k\Omega$

This design yields a minimum load current at any given time. The minimum load current is calculated as in Equation 2.3.

$$I_{Loadmin} = \frac{L_{Pri} \cdot I_{sw} \cdot f_{min}}{2 \cdot V_{out}} \tag{2.3}$$

Where:
$L_{Pri} = 300\,\mu H$
$V_{out} = 5\,V$
$I_{sw} = 52\,mA$
$f_{min} = 7{,}5\,kHz$
$\Rightarrow I_{Loadmin} \approx 610\,\mu A$

In order to reduce the ringing on the output diode an RC snubber is implemented on the primary side of the transformer. An additional snubber is designed on the secondary side so that the PCB is ready for implementation, this one is not implemented. The calculations is done as in Equations 2.4, 2.5 and 2.6. The timing parameters are measured on the actual circuit to provide the most optimum snubbing.

$$C_{parasitic} = \frac{C_{17}}{(\frac{T_{periodsnub}}{T_{period}})^2 - 1} \tag{2.4}$$

$$L_{parasitic} = \frac{T_{period}^2}{C_{parasitic} \cdot 4 \cdot \pi^2} \tag{2.5}$$

$$R_{19} = \sqrt{\frac{L_{parasitic}}{C_{parasitic}}} \tag{2.6}$$

Where:
$T_{period} = 60\,ns$
$T_{periodsnub} = 112\,ns$
$C_{17} = 100\,pF$
$\Rightarrow R_{19} \approx 240\,\Omega$

The switch mode step down converter has an additional overcurrent and short circuit protection via a fuse rated 250 V@200 mA.

2.1.1.4 Power Output and Feedback Circuit

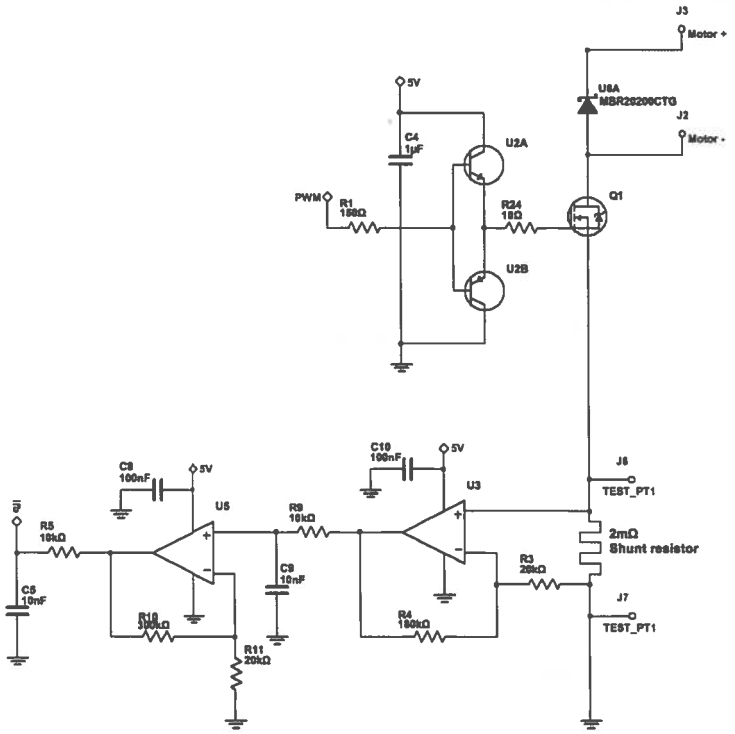


Figure 2.5: Power output stage at current feedback circuit

The power output for the DC motor is made as a simple on switch chopper PWM control. The motor controller is thereby only able to control the DC motor in the first quadrant. To minimize switch losses a two transistor gate driver is implemented. These two Bipolar junction transistors is able to charge the gate of the MOSFET with a current of approximately 500 mA. The gate current is limited by R_{24} to minimize high frequency ringing on the gate. A flyback diode is coupled parallel to the DC motor terminals to ensure at current path when the MOSFET is turned of.

The main current feedback is maintained via a 2 mΩ shunt resistor in the main power line. The shunt is realized as a specific piece of PBC wire and calculated as shown in Equation 2.7.

$$R_{Shunt} = \frac{\rho \cdot length}{Area} \tag{2.7}$$

Where:
$\rho = 17{,}5\,\text{n}\Omega\,\text{m}$
$length = 4\,\text{cm}$
$Area = 35\,\mu\text{m} \cdot 1\,\text{cm}$
$\Rightarrow R_{Shunt} \approx 2\,\text{m}\Omega$

A the voltage across the shunt resistor is measured via a second order buffered low pass filter with sufficient gain. The voltage is proportional to the DC motor current. The filter

gain is calculated to fit the control voltage range when the current is lower or equal to the maximum rating for the system. The gain is calculated for each filter as in Equations 2.8. The cut off frequency for each of the filters is calculated as in Equation 2.9.

$$A = \frac{R_4}{R_3} + 1 \tag{2.8}$$

Where:
A = Gain
R_3 = Ground Resistor (Will be R_{11} for the second filter in Figure 2.5)
R_4 = Feedback Resistor (Will be R_{10} for the second filter in Figure 2.5)

$$f_c = \frac{1}{2 \cdot pi \cdot R \cdot C} \tag{2.9}$$

Where:
f_c = Cut Off Frequency
R = Resistor in RC low pass filter
C = Capacitor in RC low pass filter

2.1.1.5 Analog and Digital Interfacing

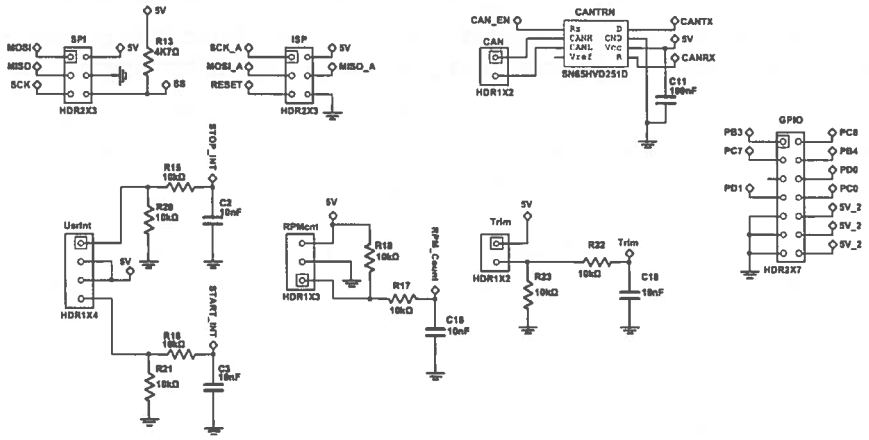


Figure 2.6: Interfacing circuits

The system interfaces includes the following types.

- Drivetrain Speed Feedback
- Additional Analog Interfaces
- CAN Interface
- SPI Interface
- UART Interface
- User Interface

Drivetrain Speed Feedback
The drivetrain speed feedback is implemented as a Hall effect sensor in the drivetrain. This sensor triggers an interrupt on the micro controller.

Additional Analog Interfaces
A number of general purpose In/Out ports is connected to accessible solder pads for additional and "on the fly" extensions.

CAN Interface
The system and the PCB layout is prepared for CAN interfacing.

SPI Interface
The SPI interface is used to log data form the motor controller on an SD card placed on a breakout board with a level converter.

UART Interface
The UART is used for accessing and monitoring internal software parameters.

USER Interface
The User interface consists of a number of buttons in the user controls. The user is able to control the system functions via these buttons.

Each interface includes protocol specific hardware such as pull-up resistors, decoupling capacitors and analog low pass filters.

A seven point turn switch is placed in the cabin to make the driver able to adjust parameters in the cruise control while driving. The turn switch in implemented as a simple voltage divider, shown in Figure 2.7 and connected to an analog to digital converter in the micro controller.

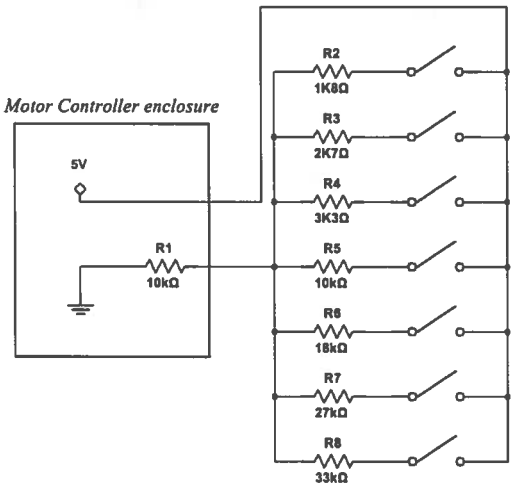


Figure 2.7: Turn switch circuit for adjusting cruise parameters.

2.1.2 Software

The software in implemented to match the state machine shown in Figure 2.8. The input parameters for the software is the speed of the drivetrain, the current through the DC

motor and driver inputs from the controls in the steering rods. Furthermore the driver is able to adjust the setpoint for the driving style via a turn switch in the cabin.

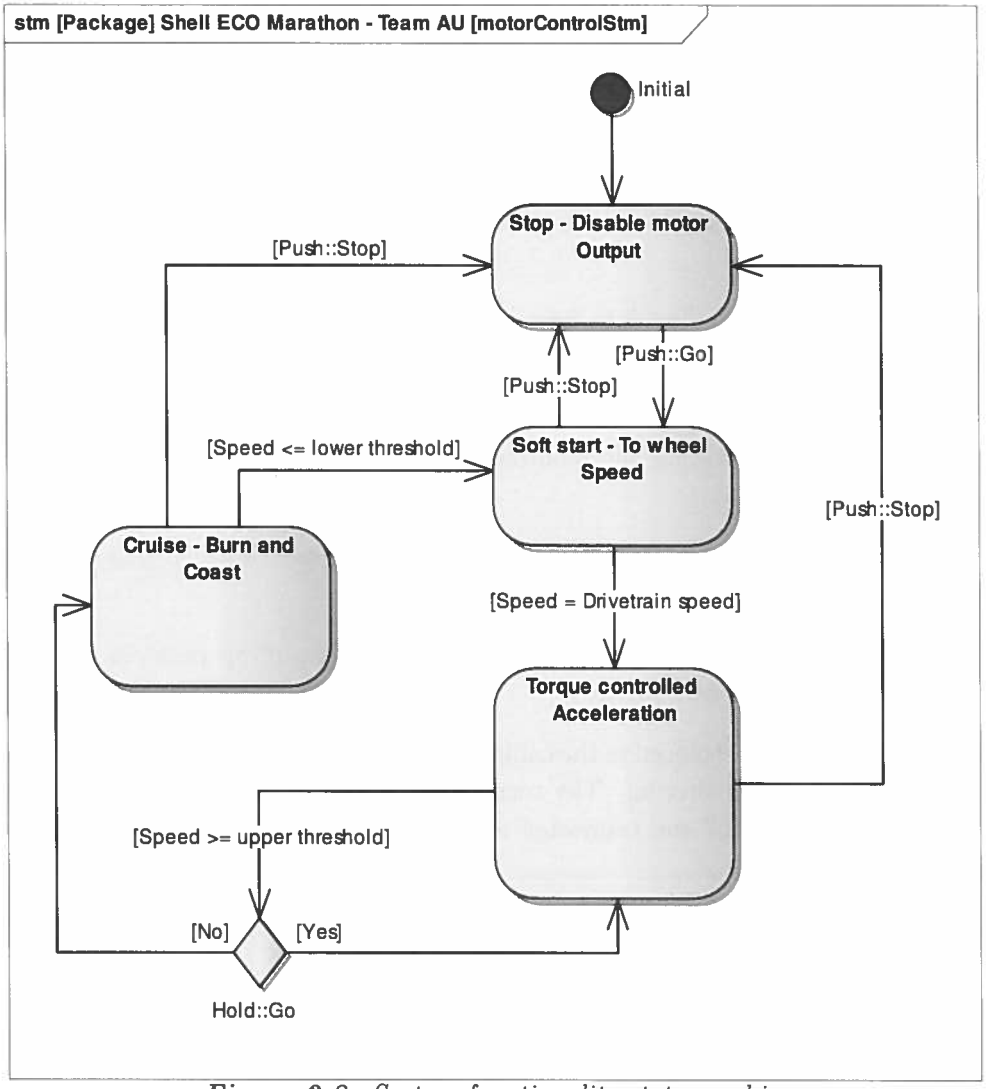


Figure 2.8: System functionality state machine

Appendices 3

3.1 Appendix A

System Block diagram

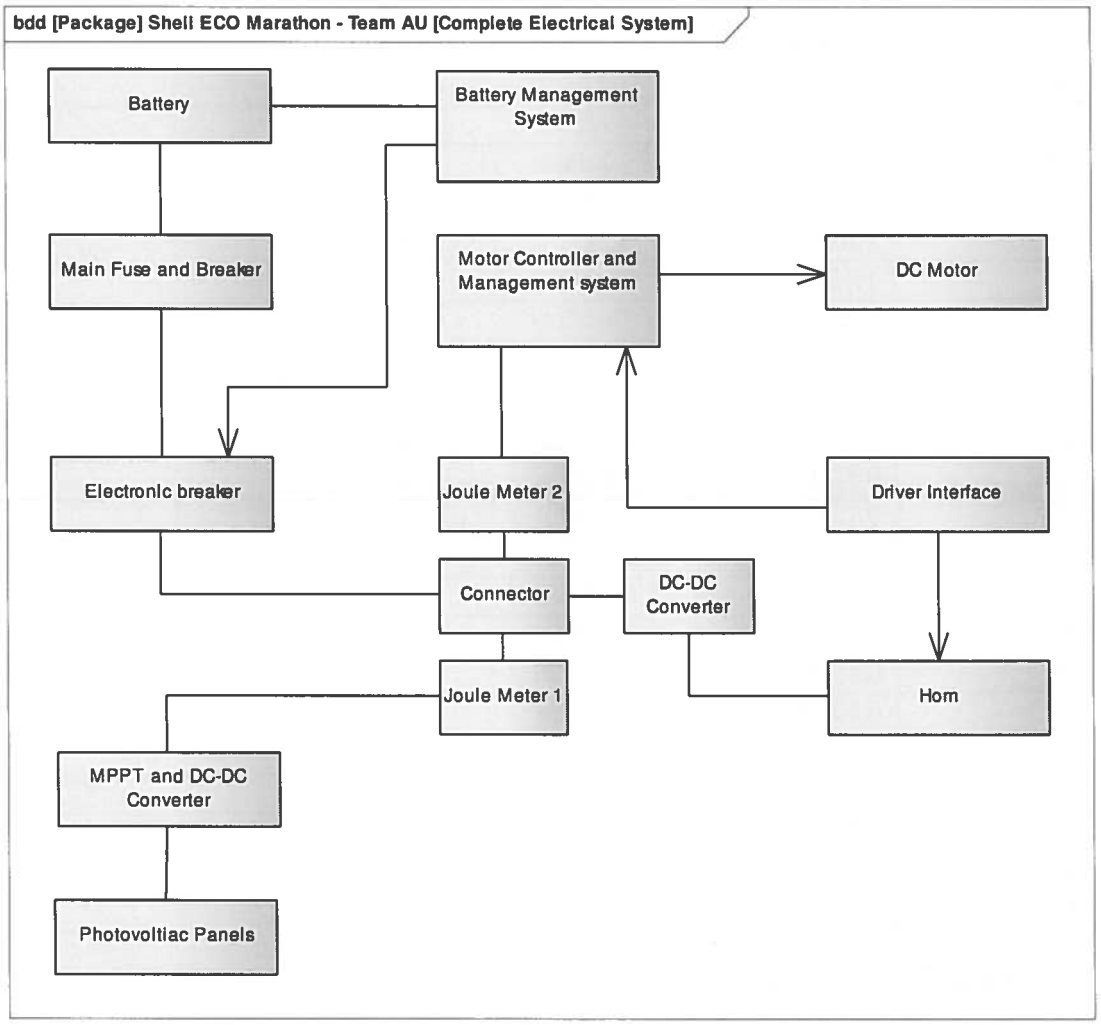


Figure 3.1: System Block Definition Diagram

3.2 Appendix B

Maximum Ampere according to wire size

AWG gauge	Diameter [mm]	Ohms per km	Maximum amps for chassis wiring
0	8.25246	0.322424	245
1	7.34822	0.406392	211
2	6.54304	0.512664	181
3	5.82676	0.64616	158
4	5.18922	0.81508	135
5	4.62026	1.027624	118
6	4.1148	1.295928	101
7	3.66522	1.634096	89
8	3.2639	2.060496	73
9	2.90576	2.598088	64
10	2.58826	3.276392	55
11	2.30378	4.1328	47
12	2.05232	5.20864	41
13	1.8288	6.56984	35
14	1.62814	8.282	32
15	1.45034	10.44352	28
16	1.29032	13.17248	22
17	1.15062	16.60992	19
18	1.02362	20.9428	16
19	0.91186	26.40728	14
20	0.8128	33.292	11
21	0.7239	41.984	9
22	0.64516	52.9392	7
23	0.57404	66.7808	4.7
24	0.51054	84.1976	3.5
25	0.45466	106.1736	2.7
26	0.40386	133.8568	2.2
27	0.36068	168.8216	1.7
28	0.32004	212.872	1.4
29	0.28702	268.4024	1.2
30	0.254	338.496	0.86
31	0.22606	426.728	0.7
32	0.2032	538.248	0.53

Table 3.1: Part selection of AWG gauge current table
Source: `https://www.eol.ucar.edu/rtf/facilities/isff/LOCAL_access_only/Wire_Size.htm`

3.3 Appendix C

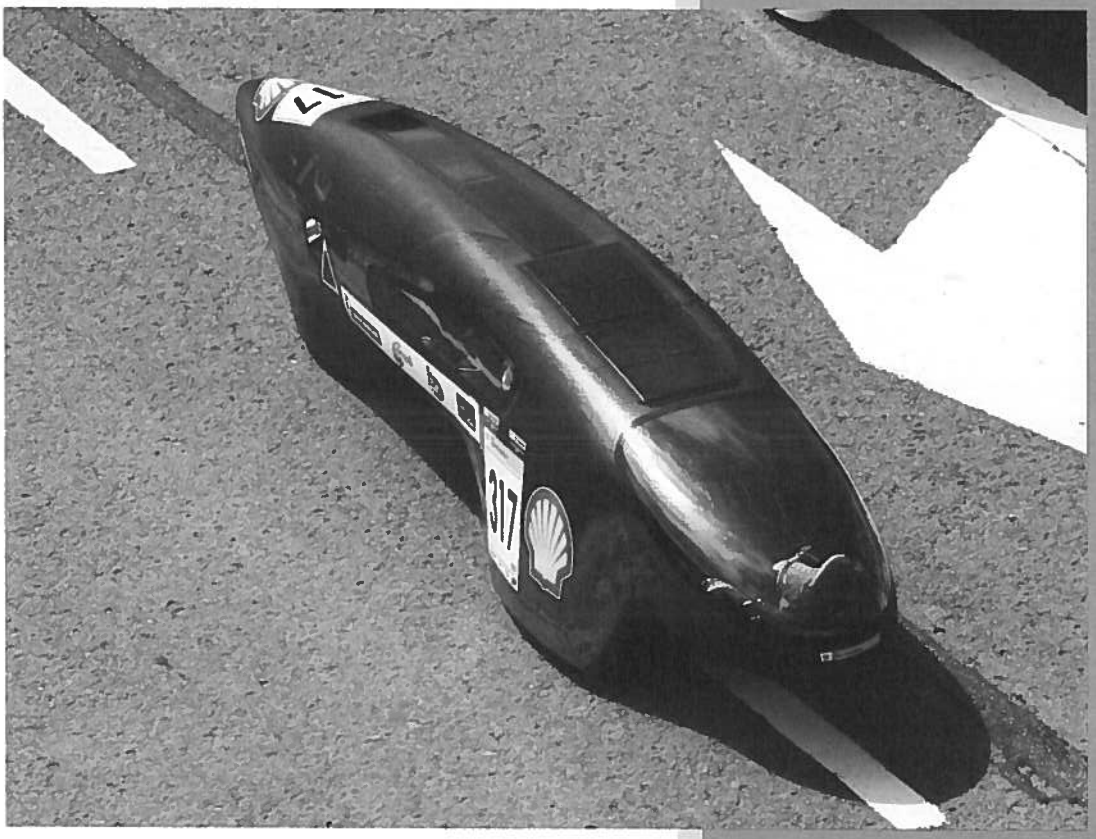
Position of system elements in vehicle

Project Documentation

2013

Propulsion Battery and Battery Management System

- for Shell Eco-marathon 2013



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Submission date: 14-06-2013

Project Manager:

Jonas Nyborg- 08325

Project number:

12105

FOREWORD

This document contains documentation of a propulsion battery and Battery Management System tailored for Shell Eco-marathon 2013. These are specified in a sequential manner, starting at Specification Requirements, elaborated by a System Architecture, and subsequently implemented with description of design and chosen solutions. In addition, system tests are included in this document.

CONTENTS

1. SPECIFICATION REQUIREMENTS

1.1. Version History

Version 1, date: 09-02-2013

Version 2, date: 16-02-2013
System Description modified, figure 1 modified, battery voltage changed to 24V on request from AU Herning, Communication protocols added.
Version 3, date: 03-03-2013
System Description improved after advice from external review. Requirements: PB_F.2, PB_F.3, BMS_F.6, PB_NF.3 and BMS_NF.7 clarified.
Version 4, date: 21-05-2013
Mechanical and documentation requirements, added to System Description. Requirements: PB_NF.5, PB_NF.6, BMS_NF.8, BMS_NF.9, BMS_NF.10 added.

1.2. Introduction

This document outlines the system to be designed, and associated specification requirements. Basic system requirements have been driven by Shell Eco-marathon official rules 2013 and interfacing agreements with other parties involved[1]. In addition, some extended battery cell surveillance features, described later in this document, has been included to increase safety and to impose the possibility of performance analysis.

[1] AU Herning (project groups working on related Shell Eco-marathon projects)

1.3. System Description

This project emanates from the participation in Shell Eco-marathon, a competition on energy efficiency of a small vehicle carrying one person. The vehicle to be constructed, will be a light electric vehicle, with photovoltaic cells and an off track charger as power source. An onboard Lithium-Ion battery pack with high energy density will serve as energy storage, which imposes the need of a Battery Management System (BMS), to ensure that the battery is kept within its Safe Operation Area (SOA), and to ensure optimum lifespan.

A project description outlining general electric drive train requirements[2] was framed by Aarhus college of engineering, and is underlying basis for the project specified in this specification requirement.

A simple BMS comparing cell voltage, temperature and current to allowable upper and lower threshold levels would fulfill the requirements given by the Shell Eco-marathon committee. However, a more sophisticated digital BMS performing measurements at cell level, and presenting these, will allow detailed analysis of battery performance, and point out cells with unsatisfying performance. Therefore, the sophisticated digital approach has been selected for this project.

As a number of cells will be connected in series, the battery pack performance will be limited by the performance of the weakest cell. Therefore the system to be designed must present individual cell parameters, along with battery parameters. Real time data must be accessible through a CAN interface, while logged data shall be available via USB.

While most features of the BMS to be designed are supported by some off-the-shelf battery management systems, designed for electric vehicles with large cell count, such systems are often large in size, heavy and unnecessarily power consuming for small systems. Designing a small but full featured centralized BMS for a moderate number of cells, will not only be beneficial for Shell Eco-marathon. It can potentially lead to more sustainable battery systems for electric bicycles, mowers etc. as a defective cell can be discovered and replaced as an alternative to disposal of the entire battery pack.

Besides advanced features, like estimation of State Of Charge (SOC), State Of Health (SOH) and interfacing to external vehicle units. The BMS must perform primary and redundant protection, by monitoring cell voltages, cell temperatures and battery current and autonomously isolate the battery from its load, in case any parameter exceeds SOA.

The Battery Pack to be designed must be as light as possible, certain high energy density battery chemistries do however pose a higher fire hazard. Therefore a balance between density and safety must be found.

As the BMS and battery are to be used for Shell Eco-marathon 2013, a functional system must be prepared before participation, this includes fabrication of all PCB's, mechanical assembly of the system and mounting within the vehicle. Furthermore, to ensure the possibility of on-site repairs, back-up replacement modules, including extra PCB's, batteries, plugs etc., must be made. To ensure approval of the system, technical documentation, fulfilling Shell Eco-marathon requirements must be prepared.

[2] See "12105 Shell eco marathon" in appendices

1.3.1. System Outline

The system to be designed, including external units with relevance to the specification requirements, has been outlined in Figure 1. The cell count is for illustration only. Furthermore, only main functionalities have been included.

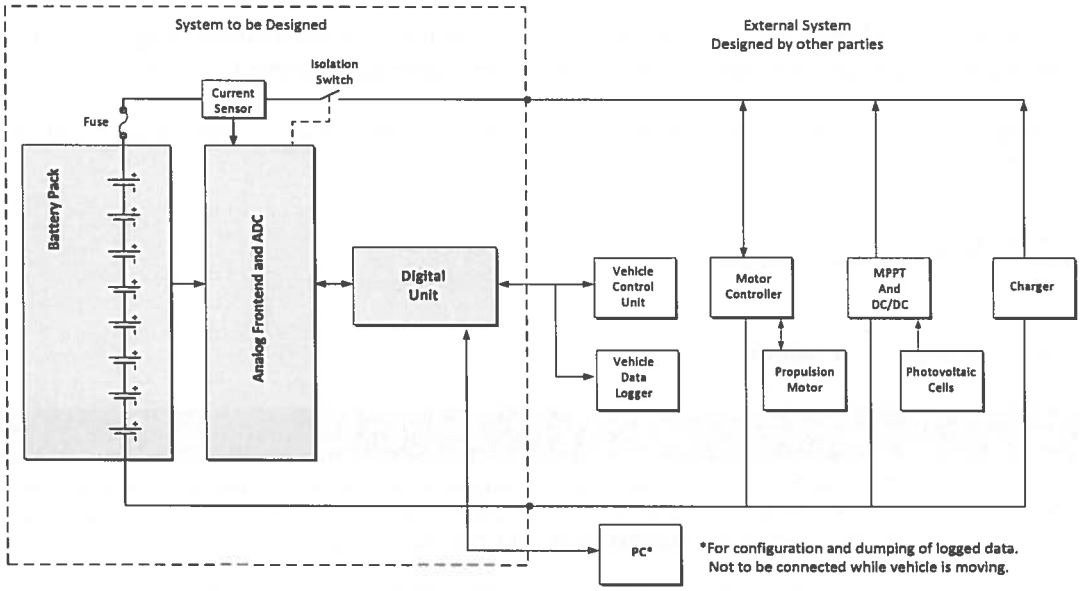

Figure 1 - Draft of Battery Pack and BMS

1.4. System Delimitation

As the duration of this project does not allow comprehensive research and design optimizing of all involved hardware units and software, the system will be delimited to certain main focus points, while other system parts will be briefly described. Below a list of delimitations:

- Off track charger will not be implemented, as a CC-CV (Constant Current - Constant Voltage) charging profile can be accomplished using a laboratory power supply.
- Analog Front End will be based on a number of ASIC's in order to reduce power consumption and time to market. As achieving lower power consumption with a custom designed Front End, within the given timeframe, is predicted to be unrealistic.
- PC software for analysis of data readout from the BMS may be briefly described, but not fully implemented.

1.5. Requirements

As described in the pre-project[3] the system has to fulfill certain mandatory requirements to qualify for participation in Shell Eco-marathon. Furthermore the Interfacing to external units and the desire to design a system with extended battery cell surveillance, entails certain requirement.

The tentative list of requirements, specified in the pre-project, has been summed up and refined, resulting in the functional and non-functional requirement, described in section 1.5.1 and 1.5.2

To ease the use of references to specific requirements, these are given a specific requirement number.

1.5.1. Functional requirements

1.5.1.1. Propulsion Battery

Req. #	Requirement description
PB_F.1	The propulsion battery must be short circuit protected by a fuse located on the positive conductor, as close to the battery as possible. Furthermore the fuse must be rated so that the battery is able to deliver enough short circuit current to open the fuse at all times.
PB_F.2	The propulsion battery must safely be able to withstand a continuous discharge current of 25A and a temporary max. current of 50A for 10 seconds.
PB_F.3	The propulsion battery must accept a constant charging current of max. 15A.

Table 1 - Functional requirements for Propulsion Battery

1.5.1.2. Battery Management System

Req. #	Requirement description
BMS_F.1	The BMS must, at all times, be able to isolate the battery from all external circuitry except the BMS, if any of the limits listed below is exceeded: • Undervoltage limit (monitored at cell level) • Overvoltage limit (monitored at cell level) • Overcurrent limit (load and charge current) • Overtemperature limit (monitored at battery level)
BMS_F.2	The BMS must be able to monitor from 6 to at least 16 cells. Changes in number of connected cells may require connection of extension modules and minor SW and HW adjustments. SW values that are cell count dependant must be implemented using definitions assembled in one location, to allow easy modification.
BMS_F.3	In case of microcontroller failure or loss of communication with Analog Front End, the Analog Front End must perform autonomous protection of cells against under- and overvoltage, and perform isolation of battery if limits are exceeded.
BMS_F.4	Maintenance cell balancing[4] must be performed by the BMS doing charge, to equalize SOC, and thereby compensate for (cell to cell) differences in self discharge currents. As cells SOC will be in

[3] See "Pre-Project BMS and Propulsion Battery" in appendices

	balance at initial connection to the BMS, gross balancing capability is not needed.
BMS_F.5	Following data must be stored in internal memory, once per minute, for later readout via USB port or SD card: • Individual cell voltages (averaged over a period of 1 minute) • battery current (averaged over a period of 1 minute) • battery temperature(s) (averaged over a period of 1 minute) • battery SOC (at time of saving) • battery SOH (at time of saving) • Error information Capacity of internal memory must hold data history of min. 10 hours
BMS_F.6	The BMS must be able to estimate SOC and internal resistance.
BMS_F.7	If the internal resistance of any cell exceeds (averaged internal resistance x 2) an error message* must be transmitted on the CAN bus, to reveal poor cell performance. * See CAN protocol DTC (5) for further details.
BMS_F.8	The actual battery and cell status must be transmitted on the CAN bus according to CAN protocol. See CAN protocol for further details.
BMS_F.9	The BMS must be able to enter a low power mode consuming less than 100mW if a undervoltage failure occurs. Low power mode will be entered after isolating the battery, so all protection functionalities may be deactivated. A pushbutton (or similar) must be available to resume normal BMS activity.
BMS_F.10	After the occurrence of an undervoltage error, the BMS must sense the connection of a charger and re-close the isolation switch, and thereby enable charging.

Table 2 - Functional requirements for BMS

1.5.2. Non-functional requirements

1.5.2.1. Propulsion Battery

Req. #	Requirement description
PB_NF.1	The propulsion battery must consist of a number of Lithium-Ion cells, leading to a nominal battery voltage within the range of 22 - 26 Volts.
PB_NF.2	All battery cells must be contained in one battery unit, as only one propulsion battery per vehicle is allowed.
PB_NF.3	The effective capacity* must be greater than or equal to 70Wh. *Capacity available at 100W load and ambient temperature of 8°C[5].
PB_NF.4	The propulsion battery must be electrically isolated from the vehicle frame and the accessory battery circuit.
PB_NF.5	Technical documentation fulfilling Article 58 of Shell Eco-marathon official rules[6] must be prepared before participation.

[4] For details see: http://liionbms.com/php/wp_balance_current.php (date: 07-02-2013)
[5] Based on average low temperature for Rotterdam in May, See: http://weatherspark.com/averages/28810/5/Rotterdam-Zuid-Holland-The-Netherlands (date: 02-02-2013)
[6] See " sem_rules_chapter01_2013" in appendices

PB_NF.6	Min. 2 batteries must be available, to ensure the possibility of battery replacement between races.

Table 3 - Non-functional requirements for Propulsion Battery

1.5.2.2. Battery Management System

Req. #	Requirement description
BMS_NF.1	Limits listed in BMS_F.1 must be kept within specifications of chosen cell type.
BMS_NF.2	Types of measurements performed by the BMS, including measurement ranges and accuracy: Cell voltage: 2V to 4.5V (accuracy +/- 4mV @ 24°C) Battery temperature: -20°C to 100°C (accuracy +/- 3°C) Battery current: -15A to 60A (accuracy +/- 100mA)
BMS_NF.3	Cell balancing current min. 75mA[7]
BMS_NF.4	Operational within Industrial Temperature range -40°C to 85°C
BMS_NF.5	COM port communication must be implemented according to RS-232 (ISO IS2110) standard, or as virtual COM port with female Mini USB plug.
BMS_NF.6	Average power consumption must be kept below 1.5W while all BMS functionalities are active. (consumption of isolation switch not included)
BMS_NF.7	Isolation switch must safely carry a continues current of 25A. And a max. current of 50A for 10 seconds. Furthermore it must be able to interrupt a current of 75A.
BMS_NF.8	Technical documentation fulfilling Article 58 of Shell Eco-marathon official rules[8] must be prepared before participation.
BMS_NF.9	The system must be mounted in a cabinet fulfilling Article 57-m of Shell Eco-marathon official rules[7].
BMS_NF.10	All PCBs, plugs, fuses etc. must be backed-up by replacement units to allow on-site repair.

Table 4 - Non-functional requirements for BMS

[7] Derived from rules specified in: http://liionbms.com/php/wp_balance_current.php (date: 07-02-2013)
[8] See " sem_rules_chapter01_2013" in appendices

1.5.3. Communication Protocols

1.5.3.1. CAN communication protocol

While a CAN protocol based on CANopen CiA 301 and CiA 418 standards, might be the best choice for a commercial product, as it will allow communication with chargers featuring CiA 419 communication protocol, which most likely will be the de facto standard of the future. A more simple protocol will be sufficient for this project, and ease the implementation. Therefore the Standard Traction Pack Messages has been chosen, this protocol is being used by elithion and claimed to be supported by a number of chargers.

The Original Standard Traction Pack messages can be found at:
http://liionbms.com/php/standards.php

The protocol tailored for this project can be seen below:

- CAN communication bit rate: 125 Kbit/s
- Standard addressing (CAN 2.0 A) (not extended)
- Period between data transmission: 1 second
- Multi-byte values are big-endian

ID	Bytes	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
620h	8	Company name (1)							
621h	8	Product name / rev level (1)							
622h	6	State (2)	Timer (3)		Flags (4)	DTC (5)	DTC (5)	-	
623h	6	Voltage (6)		Min Vtg (7)	Min Vtg # (8)	Max vtg (7)	Max Vtg # (8)	-	
624h	6	Current (9)		Charge limit (10)		Discharge limit (10)		-	
625h	8	Batt. energy in (11)				Batt. energy out (11)			
626h	7	SOC (12)	DOD (13)		Capacity (14)		SOC2 (15)	SOH (16)	-
627h	6	Temperature (17)	Air temper. (17)	Min tmp (18)	Min tmp # (8)	Max tmp (18)	Max tmp # (8)	-	
628h	6	Resistance (19)		Min res (20)	Min res# (8)	Max res (20)	Max res# (8)	-	

Table 5 - CAN protocol

1. 8 ASCII characters ID620h = "IHA BMS1" and ID621h = "SW: X.XX" (X.XX = numbers indicating SW version)
2. State of Propulsion battery system
    0. Fault

    1. Charger connected, Isolation Switch closed
    2. Vehicle ON, Isolation Switch closed
    3. Vehicle OFF, Isolation Switch closed
    4. Vehicle OFF, Isolation Switch open
3. Power up time [s]; after 65535 s, it overflows back to 0
4. Byte of flags (0,3-7 for future use)
    1. Battery is being charged
    2. Battery is being discharged
5. Error codes
    1. Sign of poor cell performance
    2. Sign of poor battery performance
    3. Battery temperature too low for charging
6. Total voltage of pack [V], unsigned, 0 to 65 kV
7. Voltages [100 mV] of least charged and most charged cells or blocks of cells, 0 to 25.5 V
8. ID of the cell that has the lowest / highest voltage / temperature / resistance. 0 or 1 to 254
9. Pack current [A], signed, positive out of pack, -32kA to + 32kA
10. Maximum current acceptable (charge) or available (discharge), unsigned, 0 to + 32kA
11. Total energy in or out of battery, since manufacture. Unsigned, overflows back to 0 [WH]
12. State Of Charge [%], unsigned, 0 to 100. When deeply discharged, its value does not go below 0
13. Depth Of Discharge [AH], unsigned, 0 to 65 kAH. When deeply discharged, its value may exceed the actual capacity's value
14. Actual capacity of pack [AH], unsigned, 0 to 65 kAH
15. State Of Charge of 2nd pack (such as the vehicle's original pack) [%], unsigned, 0 to 100. When deeply discharged, its value does not go below 0 (FFh will be send as no secondary battery is connected)
16. State Of Health [%], unsigned, 0 to 100. 100 % = all OK. Actual operation defined by the manufacturer.
17. Average pack temperature, and Air intake temperature [°C], signed, -127 °C to +127 °C
18. Temperatures [°C] of coldest and hottest sensors, signed, -127 °C to +127 °C
19. Resistance of pack [mohm], unsigned, 0 to 65 ohm
20. Resistances [100 micro-ohm] of lowest and highest resistance cells (or block of cells), unsigned, 0 to 25.5 milliohm

Note:

- If a value is not available, set to an invalid number:
    - 80h for 1-byte, signed variables
    - FFh for 1-byte, unsigned variables
    - 8000h for 2-byte, signed variables
    - FFFFh for 2-byte, unsigned variables

1.5.3.2. RS232 communication protocol

The COM port or virtual COM port(USB) shall allow the system administrator to dump logged data on a PC using a simple RS232 terminal program.

- RS232 baudrate: 38400 Kbit/s

Operation	ASCII string to be send from PC	Confirmation send to PC
Set cell count	CellC:xx (xx = number of connected cells) Ex.: if 12 cells are connected following string should be send: CellC:12	ASCII string: New Cell Count:xx
Request logged data	LogReq	Logged data is being sent. If log is empty, following ASCII string will be send: Log is empty

Table 6 - RS232 protocol

2. SYSTEM ARCHITECTURE

2.1. Version History

Version 1, date: 11-03-2013

Version 2, date: 10-03-2013

Software flow chart simplified.

2.2. Introduction

This document describes the System Architecture of the project "Battery Management System and Propulsion Battery". The purpose of the System Architecture is to elaborate system blocks, of the system described and specified in the "Specification Requirements", to a level allowing subsequent implementation.

As the specifications of the selected ASIC for the Analog Front End to be designed, will influence considerably on interfaces towards other system units, the selection of an appropriate ASIC has been made prior to the definition of interfaces. This has allowed a more thorough elaboration of all system units with Analog Front End dependencies.

The system outlined in the specification requirements will be described at system block level, and following be grouped in battery, hardware(HW) and software(SW) units for which internal interfaces, functionalities and requirements will be clarified.

2.3. Overview of System Blocks

Figure 2 shows the general block diagram, extracted from the system outline in Figure 1. The function of each unit is briefly described below.

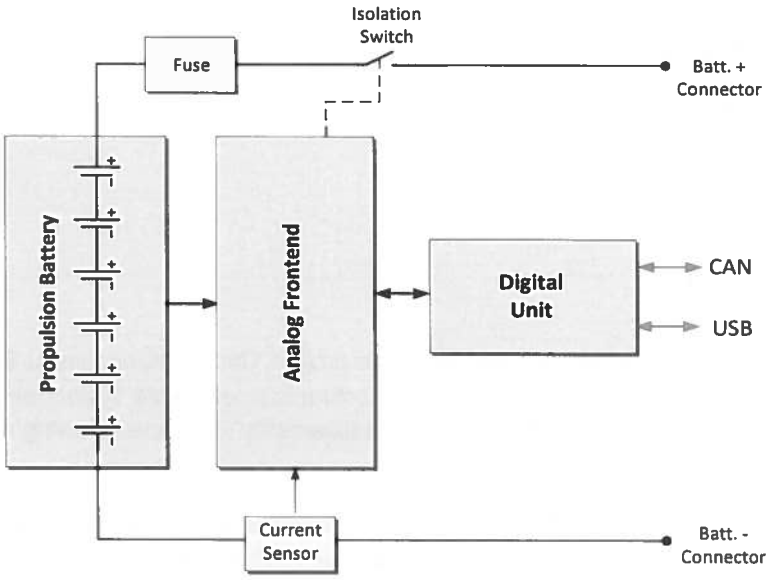

Figure 2 - General Block Diagram

Propulsion Battery: This unit, consisting of a number of battery cells, is responsible for storage of electrical energy. It must be able to capture energy from an external charger, solar panels and regenerative braking. And capable of delivering the current needed to propel the propulsion motor.

Analog Front End: This unit performs measurements and analog to digital conversion of cell voltages, battery temperatures and signal from current sensor. Furthermore, it handles cell balancing on request from the digital unit, and redundant battery protection independent of the digital unit.

Current Sensor: Senses value and direction of battery current, and present this for the Analog Front End.

Isolation Switch: This unit enables the BMS to interrupt the battery current (when the Safe Operation Area(SOA) is exceeded).

Digital Unit: Collects measured values from the Analog Front End and perform calculations and estimations of cell and battery parameters specified in the specification requirements. Furthermore it handles communication with external units.

2.4. Elaborated System Block Descriptions and Interfacing

System Blocks to be implemented are visualized in Figure 3. Sub blocks (written in Italic), outlines functionalities within the block. Functionality descriptions and design requirements for illustrated blocks are described below.

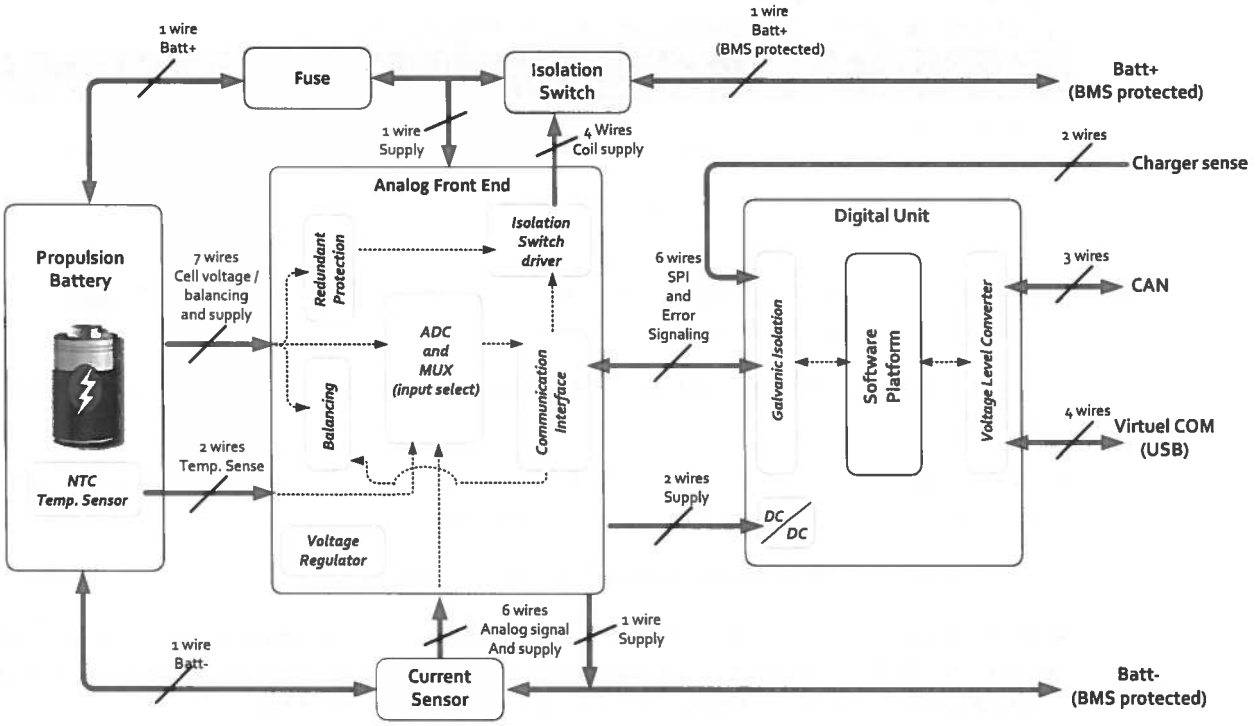

Figure 3 - Elaborated system and interfacing Diagram

2.4.1. Elaborated Battery Block Details

2.4.1.1. Propulsion Battery

IPO(Input, Process, Output)

Table below describes Input, process and output for Propulsion Battery.

Input	Process	Output
Charging Current , Charging profile: CC-CV	Storage of electrical energy.	Propulsion Current

Table 7 – IPO for Propulsion Battery

Design requirements: The Battery Pack is to be build from 6 to 8 Lithium-ion cells leading to a nominal battery voltage of 22 to 24V.

A fuse of suitable rated current and high(>2KA) breaking capacity[9] is to be inserted in the positive conductor.

To allow battery temperature monitoring a NTC of type, 10KΩ at 25°C (1%), Panasonic ERT-J1VG103FA or equivalent, must be mounted on the battery.

Connections and devices to be contained in the propulsion battery has been illustrated in Figure 4.

Note: A choice of one particular Lithium Iron Phosphate (LFP)[10] cell and one Li-ion polymer[11] cell has been pointed out based on their high power density. However thermal performance, energy density and safety is to be compared, to find most appropriate cell chemistry.

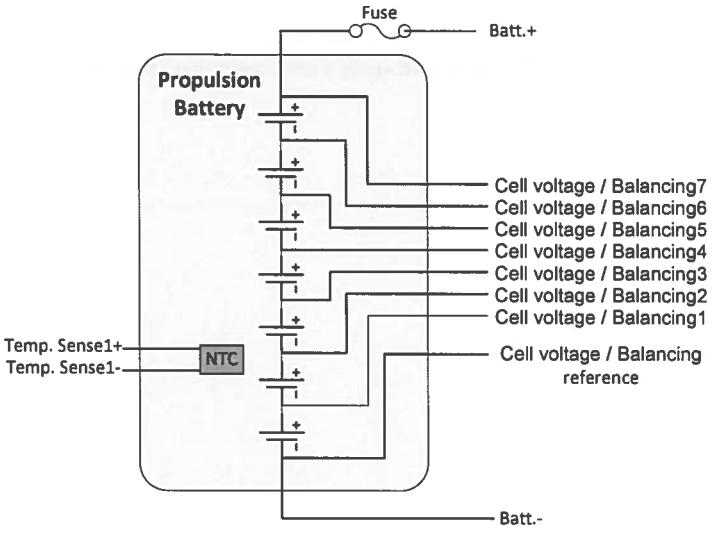

Figure 4 - Propulsion Battery Connections

[9] As the internal resistance of the battery is low, and the battery is able to deliver a very high peak current
[10] Turnigy nano-tech 3000mAh 2S1P 20~40C LiFePo4
[11] Turnigy nano-tech 3000mAh 2S2P 20~40C Lipo

Table of In-/Output Requirements

Table below specifies requirements for input and output connections of Propulsion Battery.

Connector Name	Direction	Voltage	Current	Remarks
Battery Pack Terminals				
Batt+	IN / OUT	17.5 to 30V	-15 to 50A	Fuse protected
Batt-	IN / OUT	0V	-15 to 50A	
Connections to Analog Front End and ADC				
Cell voltage / Balancing (#1 to 7 or 8)	OUT	0 to 4.8V[3]	0 to 150mA (Balancing current)	Same wires used for cell surveillance, balancing and Front End ASIC supply # of wires = cell count
Cell voltage / Balancing reference	OUT	0V		Negative terminal of lowest cell in stack
Temp. Sense+ (#1 to 5)	OUT			NTC's of type: 10KΩ at 25°C (1%), Panasonic ERT-J1VG103FA or equivalent
Temp. Sense- (#1 to 5)	OUT			

Table 8 - Connections and Signal Levels for Propulsion Battery

2.4.2. Elaborated Hardware Block Details

2.4.2.1. Analog Front End

IPO(Input, Process, Output)

Table below describes Input, process and output for Analog Front End.

Input	Process	Output
Data requests from Digital Unit.	Acquire and convert cell voltages, battery temperatures and current sensor signal to digital form. And send values to Digital Unit on request.	Measured and digitalized measurement data
Cell voltage / Balancing current		
Current sensor signal		
Cell temperature signal	Performs Balancing on request from Digital Unit.	Isolation Switch open/close signal
Balancing requests from Digital Unit	Survey cell voltages and autonomously isolate battery if SOA is exceeded.	
Isolation Switch command from Digital Unit	Drive Isolation Switch.	

Table 9 – IPO for Analog Front End

Design requirements: As described in The Specification Requirements an ASIC with lowest possible power consumption must be selected. The bq76PL536A, from Texas Instruments, has been selected as it offers the possibility to stack a number of ICs, to achieve support of a scalable number of cells. Furthermore its quiescent current is low and it offers secondary protection and high precision voltage measurements. The Analog Front End and ADC to be designed must therefore be based on the bq76PL536A, and contain inputs and outputs as specified in the table below. Furthermore, the communication with the Digital Unit must fulfill the protocol defined in the bq76PL536A datasheet[12].

Functionalities to be implemented, not contained in bq76PL536A:

Balancing: External switches and dissipative elements (bleeder resistors), must be interfaced with bq76PL536A.

Isolation Switch driver: Open collector output for Isolation Switch to be driven from GPIO of bq76PL536A.

Sensor interfacing: All circuitry necessary for interfacing between bq76PL536A and sensor in-/outputs specified in Table 10, is to be implemented.

Table of In-/Output Requirements

Table below specifies requirements for input and output connections of Analog Front End.

Connector Name	Direction	Voltage	Current sink	Current source	Input resistance	Remarks
Connections to Digital Unit						
SCLK	IN	5V logic[1]			5KΩ min.	SPI interface
MOSI	IN	5V logic[1]			5KΩ min.	
MISO	OUT	5V logic[2]	1mA min.	1mA min.		
SS	IN	5V logic[1]			5KΩ min.	
Convert	IN	5V logic[1]			5KΩ min.	Starts ADC conversion
Fault	OUT	5V logic[2]	1mA min.	1mA min.		Reports errors
$DGND_{Batt}$		0V				Digital battery ground
Aux Vdd out	OUT	17.5 to 60V		50mA min.		Supply for Digital Unit.
Aux Vss out		0V				Voltage depends on number of connected cells
Connections to Isolation Switch						
Coil +	OUT	17.5 to 60V		200mA min.		Voltage depends on

[12] See "bq76PL536A - Battery monitor and secondary protection" in appendices

						number of connected cells
Coil -	OUT	0 to 60V	200mA min.			Open collector output
Connections to Propulsion Battery						
Cell voltage / Balancing (#1 to 16)	IN	0 to 4.8V[3]	75mA min. (Balancing current)		1MΩ min. (balancing off)	Same wires used for cell surveillance, balancing and Front End ASIC supply # of wires = cell count
Cell voltage / Balancing reference	IN	0 V				Negative terminal of lowest cell in stack, is connected to this input.
Temp. Sense+ (#1 to 6)	IN					To be configured for use with NTC's of type: 10KΩ at 25°C (1%), Panasonic ERT-J1VG103FA or similar
Temp. Sense- (#1 to 6)	IN					
AUX Vdd in	IN	17.5 to 60V			480Ω min.	Directly feed to AUX out connector
AUX Vss in		0V				
Connections to Current Sensor						
Current Sensor Vdd	OUT	5V +/-0.1V		1mA min.		Sensor supply
Discharge current signal	IN	0 to 2.5V			25KΩ min.	Sensor signal
Charge current signal	IN	0 to 2.5V			25KΩ min.	Sensor signal
$AGND_{Batt}$		0V				Analog battery ground

Table 10 - Connections and Signal Levels for Analog Front End

[1] Input Logic low: 0 to 0.8V Input Logic high: 2 to 5.2V
[2] Output Logic low: 0 to 0.5V, Output Logic high: 4 to 5.1V
[3] Not referenced to GND. As cells are stacked in series connection.

2.4.2.2. Current Sensor

IPO(Input, Process, Output)

Table below describes Input, process and output for Current Sensor .

Input	Process	Output
Battery current	Bidirectional monitoring of battery current, outputs analog voltages proportional to current.	Battery current
		Analog voltages proportional to battery current

Table 11 – IPO for Current Sensor

Design requirements: Gain and offset is to be determined in cooperation with Analog Front End designer. Offset drift must be as low as possible.

Table of In-/Output Requirements

Table below specifies requirements for input and output connections of Current Sensor.

Connector Name	Direction	Voltage	Current	Input resistance	Remarks
Connections to Propulsion Battery and Isolation Switch					
Batt-	IN	0V	-15 to 50A		Voltage depends on number of connected cells
Batt-	OUT	0V	-15 to 50A		
Connections to Analog Front End					
Current Sensor Vdd	IN	5V +/-0.2V		5KΩ min.	Sensor supply
Discharge current signal	OUT	0 to 2.5V	Source 0.1mA min.		Sensor output
Charge current signal	OUT	0 to 2.5V	Source 0.1mA min.		Sensor output
$AGND_{Batt}$		0V			Analog battery ground

Table 12 - Connections and Signal Levels for Current Sensor

2.4.2.3. Isolation Switch

IPO(Input, Process, Output)

Table below describes Input, process and output for Isolation Switch .

Input	Process	Output
Battery current	Conduct battery current when closed. Interrupt battery current and perform galvanic isolation of battery when open.	Battery current when switch closed No current when switch open
Relay Coil+		
Relay Coil-		

Table 13 – IPO for Isolation Switch

Design requirements: Isolation switch must be a mechanical switch(contactor or relay) to meet Shell Eco-marathon requirements. And must be of normally open (NO) type to ensure that the switch will open if connection is lost or if BMS power is interrupted.

Resistance of closed switch must be as low as possible to limit dissipative loses.

As the load (motor controller) contains large capacitors, the inrush current can potentially damage the contacts of the isolation switch. The inrush current shall therefore be limited, to limit contact wear and risk of welding.

Table of Connections and In-/Output Requirements

Table below specifies requirements for input and output connections of Isolation Switch.

Connector Name	Direction	Voltage	Current	Input resistance	Remarks
Connections to Current Sensor and External Load					
Batt+	IN	17.5 to 60V	-15 to 50A		Voltage depends on number of connected cells
Batt+ (BMS protected)	OUT	0 to 60V	-15 to 50A		
Connections to Analog Front End					
Coil +	IN	0 to 30V*		150Ω min.	*Switch Closed when Coil voltage > 17.5V Switch Open when Coil voltage < 10V
Coil -	IN	0V			

Table 14 - Connections and Signal Levels for Isolation Switch

2.4.2.4. Digital Unit (HW)

IPO(Input, Process, Output)

Table below describes Input, process and output for Digital Unit.

Input	Process	Output
SPI and parallel signals from Analog Front End	Interfacing inputs and outputs of Software Platform to CAN and USB voltage levels. Establish galvanic isolation between Analog Front End and Software Platform.	SPI and parallel signals from Analog Front End (Isolated)
CAN Physical layer as specified in ISO 11898.		CAN level converted to be Software Platform compliant
USB USB 2.0 Compliant		UART Software Platform compliant
Charger sense		Charger sense (isolated)

Table 15 – IPO for Digital Unit

Design requirements: A Charger sense input must be included to allow the BMS to resume normal operation after an undervoltage error. This enables the BMS to reclose the isolation switch at the connection of a charger.

All external devices communicating with the BMS must be galvanic isolated from the propulsion battery. This means that opto-isolators or similar and an isolated DC/DC converter must be included as part of the Digital Unit(HW).

Physical interfaces towards system blocks connected to the Digital Unit, is described in Table 16. However, physical interface between Digital Unit (HW) and Digital Unit Software platform is left for the Digital Unit designer to decide.

Note: Certain In-/Outputs requires routing to special functionalities of the Digital Unit Software Platform, such as interrupt functionality etc. This will be stated in remarks of Table 16.

Table of Connections and In-/Output Requirements

Table below specifies requirements for input and output connections of Digital Unit.

Connector Name	Direction	Voltage	Current sink	Current source	Input resistance	Remarks
Connections to Analog Front End						
SCLK	OUT	5V logic[1]	1mA min.	1mA min.		SPI interface
MOSI	OUT	5V logic[1]	1mA min.	1mA min.		
MISO	IN	5V logic[2]			10KΩ min.	
SS	OUT	5V logic[1]	1mA min.	1mA min.		
Convert	OUT	5V logic[1]	1mA min.	1mA min.		Starts ADC conversion

Fault	IN	5V logic[2]			10KΩ min.	Reports errors. Must generate interrupt
$DGND_{Batt}$		0V				Digital battery ground
Connections to CAN (external devices)						
CAN high	IN/OUT	2.5 to 3.5V			120Ω	Physical layer as specified in ISO 11898. Must be routed to CAN controller in Digital Unit Software Platform
CAN low	IN/OUT	1.5 to 2.5V				
CAN Gnd		0V				
Connections to USB (virtual COM for external device)						
USB 5V+	IN	5V +/- 0.25V			50Ω min.	Must generate interrupt
Data -	IN/OUT					Must be converted to UART and routed to UART of Digital Unit Software Platform
Data +	IN/OUT					
USB Gnd		0V				
Connections to Charger (external device)						
Charger Sense+	IN	17.5 to 60V				Charger Sense+ will be 0V when charger is off or disconnected.
Charger Sense-		0V				
Connections to Supply						
Aux Vdd	OUT	17.5 to 60V		50mA min.		Supply for Digital Unit.
Aux Vss		0V				Voltage depends on number of connected cells

Table 16 - Connections and Signal Levels for Digital Unit

[1] Output Logic low: 0 to 0.5V, Output Logic high: 4 to 5.1V
[2] Input Logic low: 0 to 0.8V Input Logic high: 2 to 5.2V

2.4.3. Elaborated Software Block Details

2.4.3.1. Digital Unit Software Platform

IPO(Input, Process, Output)
table below describes Input, process and output for Digital Unit Software Platform.

Input	Process	Output
Battery data Acquired by Analog Front End. bq76PL536A protocol	Calculation and estimation of SOC and Internal resistance etc. from data acquired by Analog Front End. Performing communication with Analog Front End and external units. Log data as specified in Specification Requirements, in non-volatile memory	Data log (via virtual COM) See protocol in Specification Requirements
Log request and parameter change requests See protocol in Specification Requirements.		Actual battery information (via CAN) See protocol in Specification Requirements
Charger information (connected or not)		Start Analog Front End conversion request. bq76PL536A protocol
Fault Interrupt (Indicating errors)		Request data from Analog Front End. bq76PL536A protocol

Table 17 – IPO for Digital Unit Software Platform

Design requirements: As power consumption is of great importance, sleep modes must be used where possible and safety or time critical functions must then be interrupt driven.

Physical Interfaces towards system blocks connected to the Digital Unit, is described in Table 16. However, physical interface between Digital Unit (HW) and Digital Unit Software platform is left for the Digital Unit designer to decide.

Note: As part of the software development process. The most appropriate methods for SOC, SOH and Internal resistance are to be found.

Flowchart Diagram

To describe software execution flowcharts has been visualized in Figure 5.

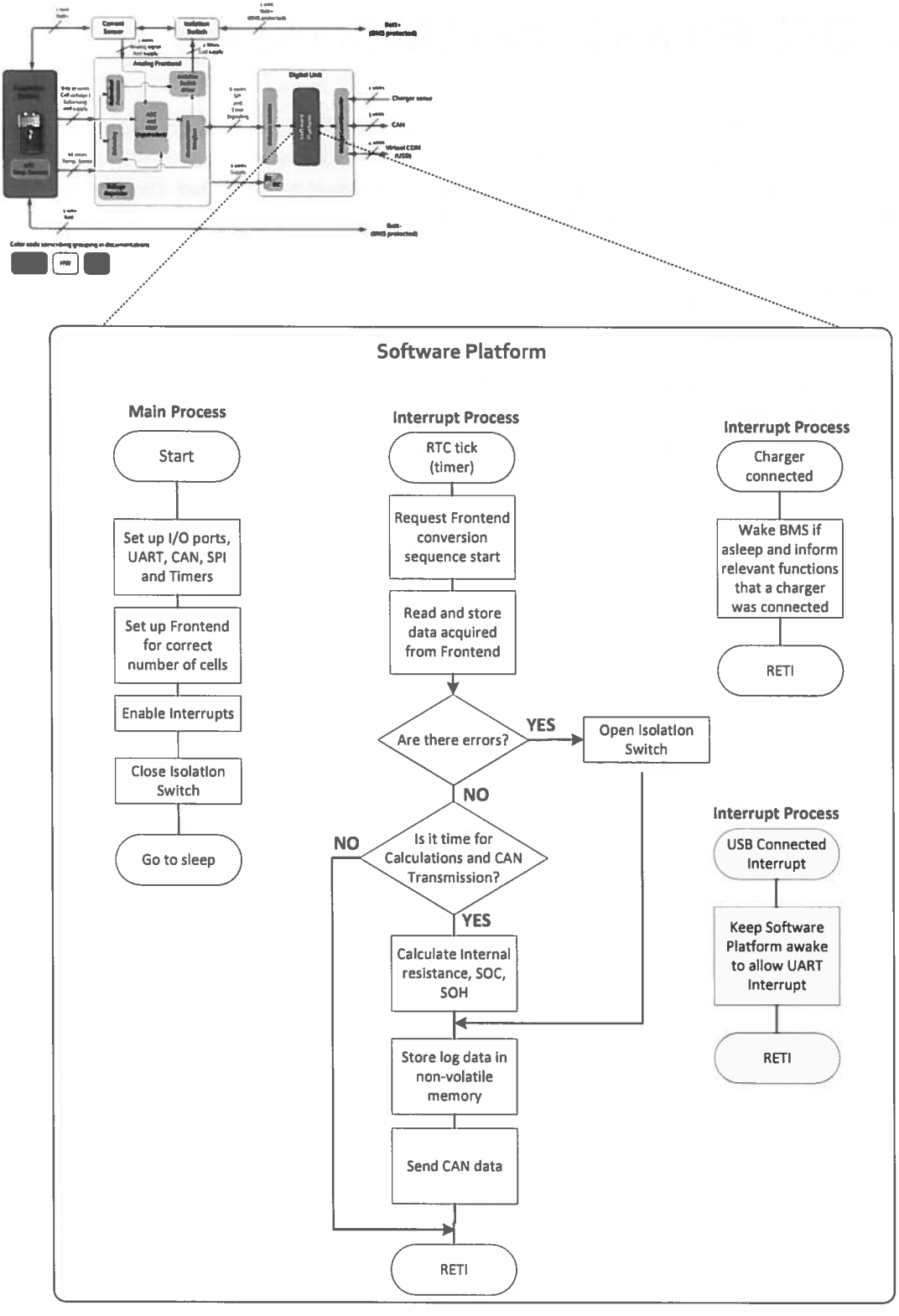

Figure 5 - Flowchart draft

3. DESIGN AND IMPLEMENTATION

In this chapter HW system blocks outlined in the system architecture will be elaborated to a level allowing implementation at component level. Furthermore, SW elements will be further detailed and subsequently implemented. Calculations and chosen technical solutions will be described and measurement results will be presented where considered relevant.

3.1. Hardware

This paragraph documents the HW design and implementation, unit by unit, in the same order as in the system architecture. For HW units including multiple circuits, a graphical overview of implemented circuits will be given. The schematics of each unit are presented and described individually. Full schematics will be presented in 0

3.1.1. Propulsion Battery

Based on the performed battery test,[13] Lithium-ion polymer(Li-PO) is found to be the most appropriate choice, as it offers satisfying capacity at simulated worst case Eco-marathon conditions, as well as low internal resistance and weight. The cycle life is expected to be shorter compared to LiFePO4[14], but for this application cycle life is of little concern. Only 2/3 of the stated capacity was available from the tested LiFePO4 battery at 1.33C discharge rate and 8°C ambient. In comparison the stated capacity was achieved from the Li-PO battery. The different behavior during discharge can be seen in Figure 6 and Figure 7.

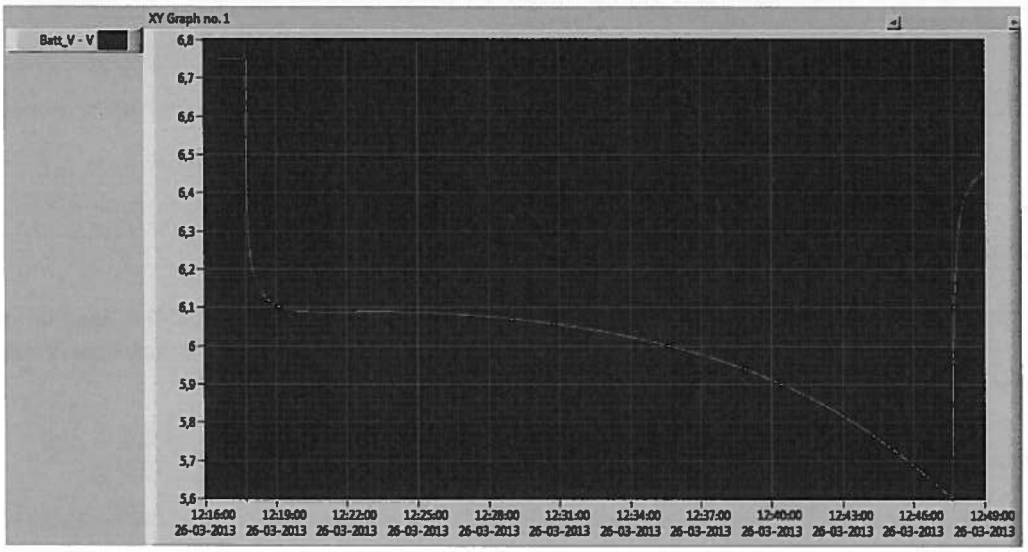

Figure 6 - Discharge of LiFePO4 under worst case Eco-marathon conditions

[13] See "Battery cell type test" in appendices
[14] http://batteryuniversity.com/learn/article/types_of_lithium_ion (date: 11-06-2013)

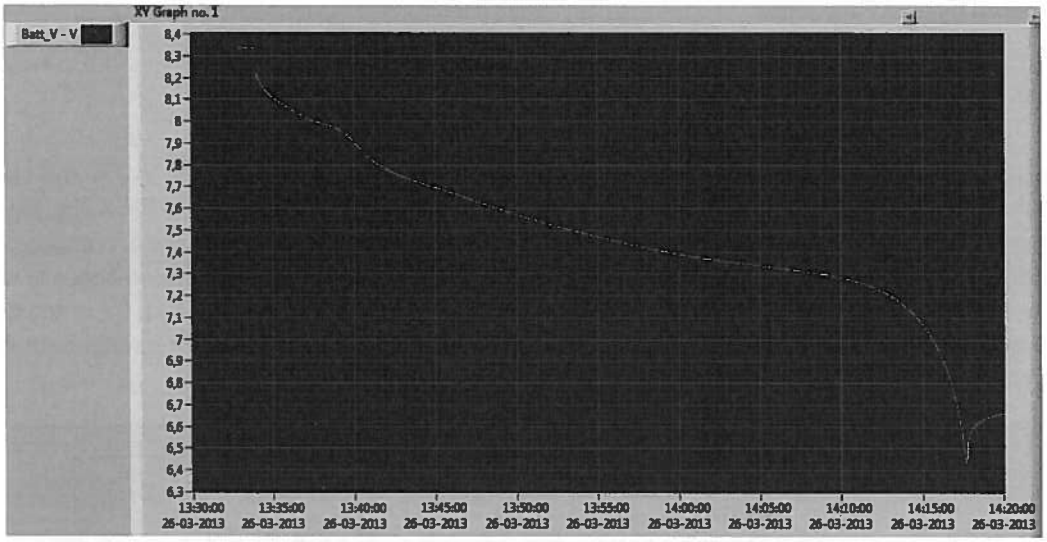

Figure 7 - Discharge of Li-PO under worst case Eco-marathon conditions

Battery dimensioning and calculations

To meet the system voltage as described in requirement PB_NF.1, and to avoid the need of Front End Extension Modules(which will be described later) 6 series connected cells has been chosen. Based on cell count and voltage the required capacity has been found:

$$Required\ capacity[Ah] = \frac{Required\ capacity\ at\ load[Wh] + BMS\ consumption[Wh]}{Nominal\ Battery\ Voltage[V]} = \frac{70Wh + 2Wh}{22.2V}$$
$$= 3.24Ah$$

This results in the selection of the, Turnigy nano-tech 3.3 Li-PO pack, with specifications as stated below.

Figure 8 - Picture of battery[15]

Capacity [Ah]	3.3
Number of cells	6
Continues discharge [C]	45
Weight[g]	565
Max Charge Rate [C]	10
Length-A [mm]	135
Height-B [mm]	45
Width-C [mm]	44

Table 18 - Battery specifications[15]

Battery test and measurements

The effective capacity available at the output of the BMS/Battery Unit. At a discharge current of 4A and a ambient temperature of 8°C is 75Wh (measured after 5 charge cycles, Start condition 4.2V per cell, End condition 3V per cell). See accept test for further test results.

[15] http://www.hobbyking.com/hobbyking/store/uh_viewItem.asp?idProduct=27121 (date: 22-05-2013)

3.1.2. Analog Front End

As described in the system architecture the core of the Analog Front End, will be the bq76PL536A. To achieve all required functionalities external circuitry and interfacing has been implemented. Overview of Front End circuit blocks can be seen in Figure 9. Elaborated circuit descriptions will be given below.

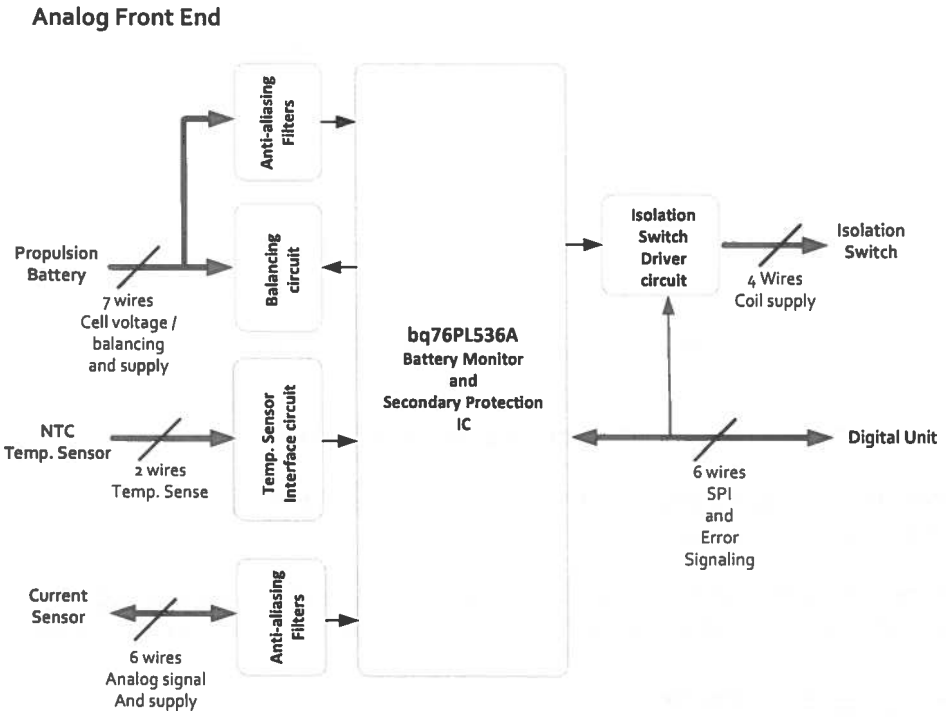

Figure 9 - Front End circuit blocks

3.1.2.1. Anti-aliasing Filters

To decrease unwanted ac noise, all signals are filtered very close to their respective ADC inputs. Cell voltages are filtered by a traditional 1.order RC low-pass filter, designed according to datasheet guidelines. 1kΩ is used as the bq76PL536A is calibrated to compensate for the voltage division created by this resistance and the input impedance. To filter the charge current signal from the Current Sensor a similar low-pass filter is applied, while the discharge current signal is filtered by a differential RC low-pass filter, filtering both common mode and differential mode noise. Schematic can be seen in Figure 10, component functionality descriptions and calculations are found below.

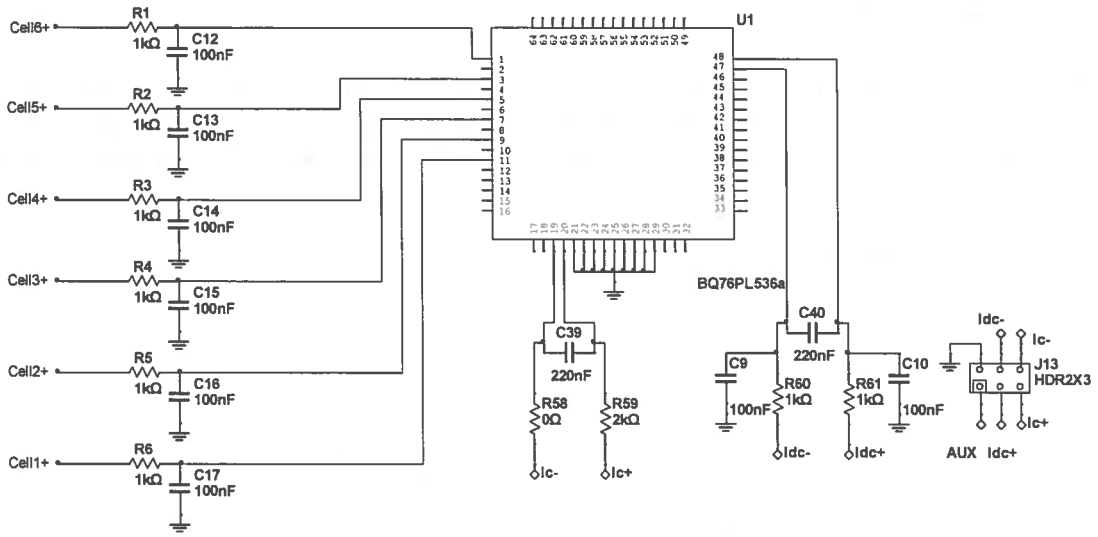

Figure 10 - Anti-aliasing filters, all filter components are placed very close to the IC

Anti-aliasing Filters component description and calculations

Resistors R1 to R6 and Capacitors C12 to C17: Low-pass filters, filtering cell voltages. Designed according to datasheet guidelines.

Resistors R58, R59 and Capacitor C39: Low-pass filter. R59 is large enough to isolate the capacity from the current sensor amplifier, and sufficient phase margin is thereby maintained.

$$f_{-3dB} = \frac{1}{2\pi * R59 * C39} = 362Hz$$

Resistors R60, R61 and Capacitors C9, C10 and C40: Common mode and differential mode filtering of discharge signal referenced to 0.1V ref. voltage.

$$f_{-3dB\ CM} = \frac{1}{2\pi * (R60//R61) * (C9//C10)} = 1.6KHz$$

$$f_{-3dB\ DM} = \frac{1}{2\pi * (R60 + R61) * (C40 + C9/2)} = 295Hz$$

3.1.2.2. Balancing circuit

The bq76PL536A offers outputs to control balancing on request from the Digital Unit. Therefore, dissipative balancing can be easily implemented, using an N-channel MOSFET as switch and a power resistor as dissipative element. Thereby a part of the charging current can be bypassed, which allows reduction of charging current feed to cells with highest SOC. The schematic is shown in Figure 11,component functionality descriptions and calculations are found below.

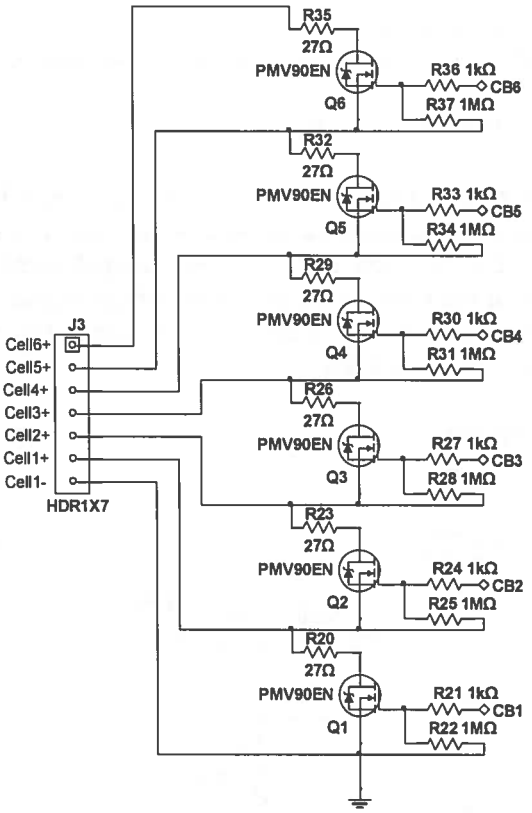

Figure 11 - Balancing circuit

Balancing component description and calculations

MOSFETS Q1 to Q6: While in saturation mode cell is partly bypassed, reducing the charging of the particular cell. PMV90EN is selected based on its low subthreshold leakage and low RDS. I_{Drain} has been over dimensioned to allow upgrade to larger balancing current.

Power resistors R20, R23, R26, R29, R32 and R35: Bleeder resistors, converting bypassed charging current to heat while its respective MOSFET is in saturation mode. To allow a proper heat transfer to PCB traces, power resistors with wide terminals has been selected. To decrease the time required for balancing a balancing current of two times the min. requirement(BMS_NF.3) has been selected.

$$dissipation\ resistance[\Omega] = \frac{Vcell[V]}{required\ balancing\ current[A]} = \frac{4\text{V(approx.)}}{150\text{mA}} = 26{,}66\Omega$$

Nearest standard value(27Ω) has been selected.

Resistors R21, R24, R27, R30, R33 and R36: Limits I_{Gate} and thereby the sink / source current required by the bq76PL536A balancing outputs at state shift(ON to OFF and OFF to ON). In theory these resistors could be excluded as Z_{out} of the balancing outputs is high.

Resistors R22, R25, R28, R31, R34 and 37: Pull-down resistors, ensures MOSFETS are off when bq76PL536A is shut down(balancing outputs are floating).

Balancing Test and Measurements
Test of this unit will be performed as part of the accept test. See accept test chapter.

3.1.2.3. Temp. Sensor Interface circuit

To allow battery temperature surveillance, a voltage divider including a Thermistor(NTC) has been used to convert temperature to a proportional voltage. As the ADC reference voltage used for the temperature sensor is divided from the sensor supply voltage(REG50), the ADC result will be ratiometric, which eliminates the need of further supply voltage regulation. The bandwidth of the sensor has been limited to reduce noise. The circuit can be seen in Figure 12. The circuit design is based on application note recommendations[16].

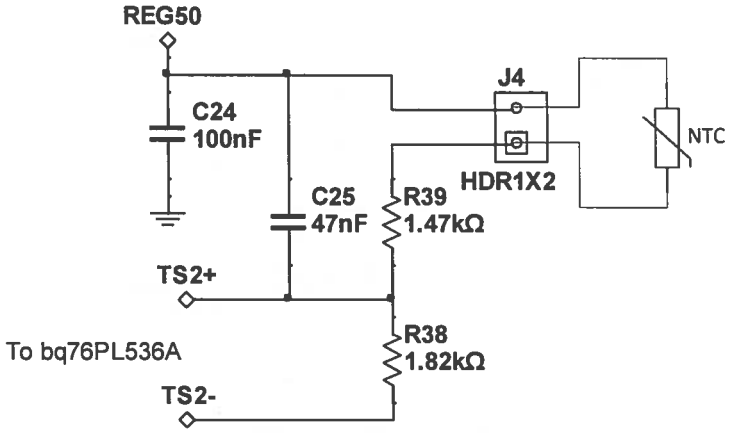

Figure 12 - Temp. sensor Interface circuit (NTC is mounted on the battery)

Temp. Sensor component description and calculations

Capacitor C24: Decoupling capacitor.

Resistors R38, R39 and NTC: Creates a temperature dependent voltage divider. Increased temperature will result in increased current through R38, which increases the voltage across it.

Capacitor C25: reduces the bandwidth and thus the noise.

$$f_{-3dB} = \frac{1}{2\pi * R_{eq} * C} = \frac{1}{2\pi * (R38^{-1} + (R39 + NTC\_resistance)^{-1})^{-1} * C25}$$
$$= \frac{1}{2\pi * (1820^{-1} + (1470 + 10000)^{-1})^{-1} * 47 * 10^{-9}} = 2.16\text{KHz}$$

[16] See "bq76PL536A - Battery monitor and secondary protection" in appendices

Temp. Sensor Test and Measurements

Temperature measurements has been performed using AMETEK ITC-155 A temperature calibrator. See Figure 13.

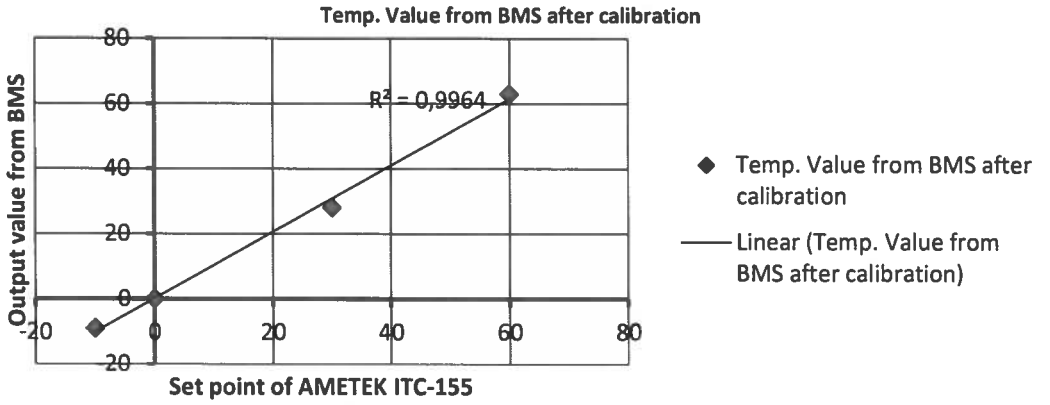

Figure 13 - Temperature measurement results compared with trend line

3.1.2.4. Isolation Switch Driver circuit

The purpose of this circuit is to allow the Digital Unit and the bq76PL536A to drive the Isolation Switch relay. To ensure the flexibility of connecting relays with any coil voltage rating, open drain topology has been chosen.

As subthreshold leakage is proportional to V_{DS} (which is equal to the battery voltage) extra attention has been paid to decrease subthreshold leakage of this driver. Therefore stacked MOSFETS[17], a technique commonly used in IC design, has been implemented to decrease leakage, this also adds a logic AND functionality, which ensures that errors detected in either the bq76PL536A or the Digital Unit will result in interruption of battery current flow, as both units must output a logic high to close the Isolation Switch.

To reduce contact wear and the risk of relay welding, a pre-charge relay driver circuit has been included. The pre-charge circuit ensures that any capacitive load will be pre-charged by a limited current to avoid an inrush current peak.

The Isolation Switch and Pre-charge relay will be discussed later.

The Isolation Switch Driver circuit can be seen in Figure 14.

[17] http://ambienthardware.com/courses/tfe01/pdfs/Roy1.pdf (date: 11-06-2013)

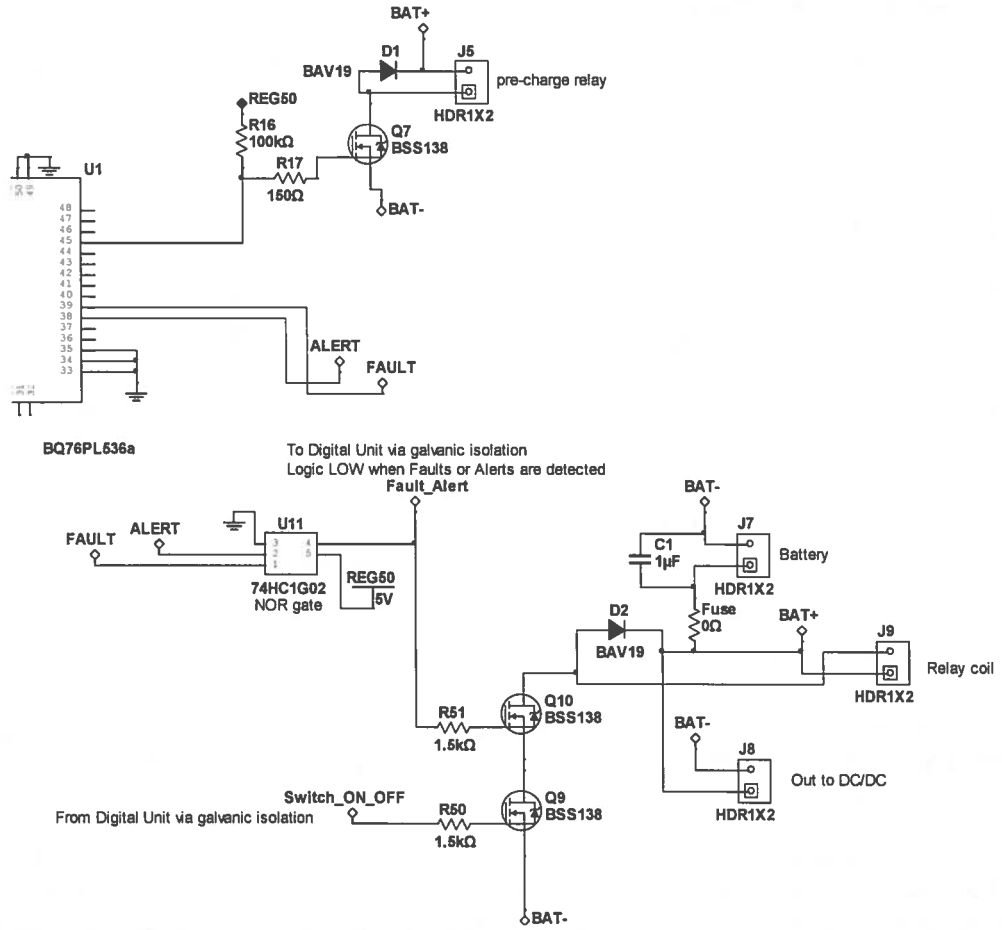

Figure 14 - Isolation Switch Driver circuit

Isolation Switch component description and calculations

Pre-charge Driver (Q7, D1, R16 and R17):

MOSFET Q7: A switching device configured for open-drain output, while in saturation mode, the pre-charge relay is active.
Diode D1: Transient protection, clamps voltage transient that would otherwise appear when Q7 is switched OFF.
Resistor R16: Pull-up resistor(output of bq76PL536A is open drain).
Resistor R17: Limits I_{Gate} to a level accepted by the bq76PL536A output.

Isolation Switch Driver circuit (Q9, Q10, D2, C1, R50, R51 and U11):

MOSFETS Q9 and Q10: Stacked MOSFETS which ensures logic AND operation with open drain output and reduces leakage while in OFF mode, as leakage current passing through Q10 will charge the capacity present at the drain of Q9 thus increase $V_{S\text{-}Q10}$ which results in a negative $V_{GS\text{-}Q10}$(leakage is dramatically reduced when $V_{GS} < 0$).
Diode D2: Transient protection, clamps voltage transient that would otherwise appear when Q9 and Q10 are switched OFF.
Capacitor C1: Decoupling capacitor.
Resistors R50 and R51: Limits I_{Gate} to a level tolerated by the gate driving devices.

NOR gate U11: Ensures that any Fault or Alert detected by bq76PL536A will turn OFF Q10 and thereby open the Isolation Switch. Furthermore the gate output is send to the Digital Unit(via the galvanic isolation) to warn this unit that errors has been detected.

Isolation Switch Driver Test and Measurements

Test of this unit will be performed as part of the accept test. See accept test chapter.

3.1.3. Analog Front End Extension Module

The Analog Front End support up to 6 cells, if a larger cell count is required an extension module can be connected. This system supports up to 2 extension modules which allows connection of up to 18 cells. The extension module is similar to the Analog Front End with the exception that there is no SPI interface for connection to the Digital Unit, no Isolation Switch driver, and no input for current sensor. Furthermore the host select pin of bq76PL536A (pin 44) is pulled high to disable the SPI host interface. A draft of extension module connection can be seen in Figure 15.

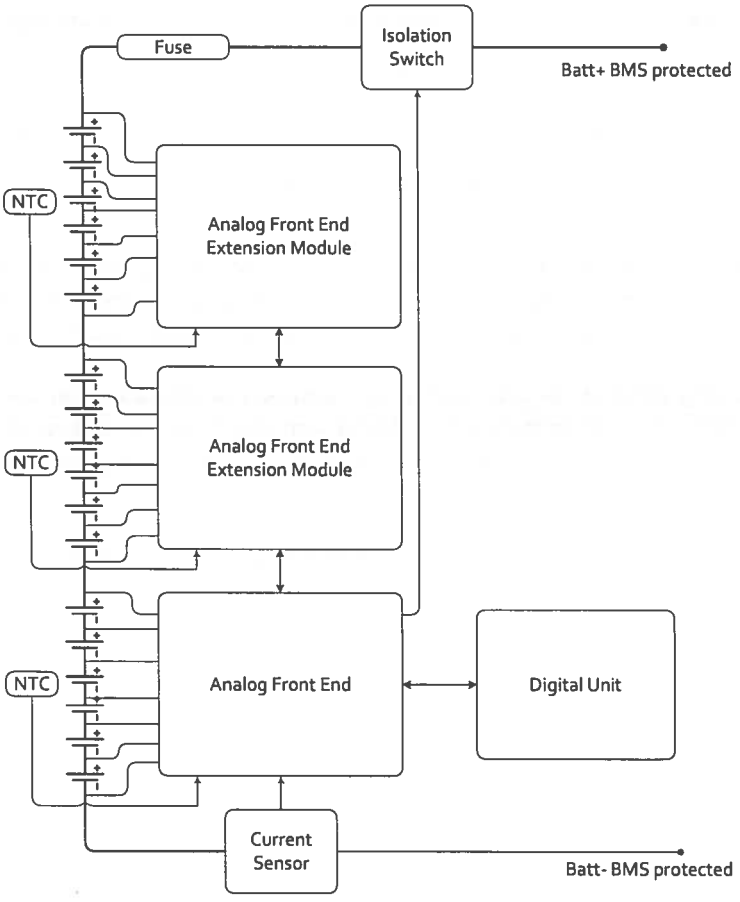

Figure 15 - Connection of Extension Modules

3.1.4. Current Sensor

Two types of sensors has been considered suitable, hall current sensors and shunt based current measurement. The benefit of the hall sensor is that no resistance is inserted in the conductor carrying the current to be measured, as opposed to the shunt sensor where power loses are proportional to the measured current. The static supply current is however higher for the hall current sensor, than what can be achieved with a low power shunt amplifier.

Sensor type power consumption comparison:

The current to be measured is estimated to be within a range of -10 to 10A at least 90% of the time. And the average current is estimated to be well below 4A, therefore a current of 4A has been used for comparison.

Parameter to be compared	Hall current sensor ACS756	Shunt current sensor based on OPA333
Supply voltage	5V	5V
Supply current	10mA(typ.)	< 100uA(estimated)
Resistive loses at 4A	2mW	16mW
Total power consumption at 4A	52mW	16.5mW

Table 19 - sensor comparison

From the comparison, it can be concluded that a shunt current sensor will offer the lowest overall consumption, and requires a supply current within the capability of the LDO integrated in the bq76PL536A, as oppose to the Hall current sensor which requires a dedicated voltage regulator.

As a wide measuring range is required and a high accuracy is desirable, the current sensor has been designed with separate amplifiers for charge and discharge measurement, connected to individual ADCs, thereby the measurement resolution is improved as the dynamic range of each ADC covers a smaller measurement range.

The Current Sensor circuit can be seen in Figure 16, component description is given below.

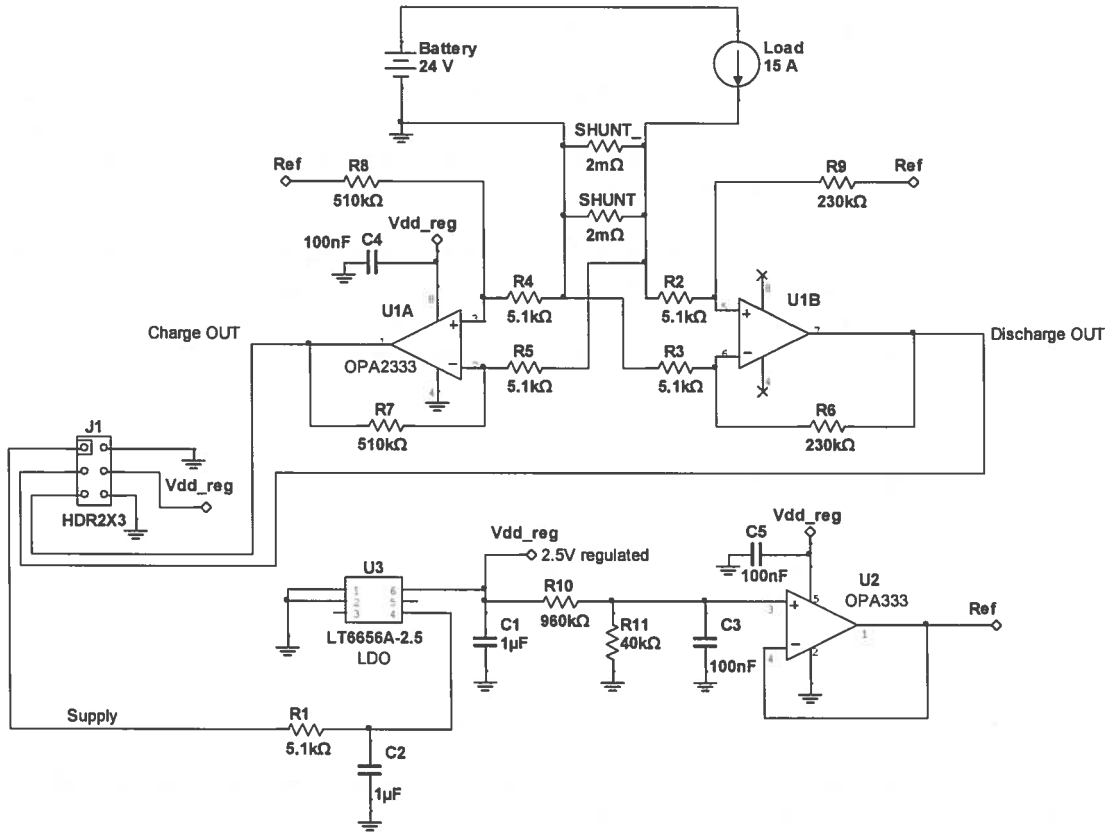

Figure 16 - Current Sensor circuit

Current Sensor component description and calculations

Voltage regulator (U3, R1, C2 and C1):

Regulator U3: A series regulator with ultra low power consumption reduces input voltage from 5V to 2.5V and significantly reduces ripple. The regulator is needed to ensure a stable reference voltage(described below). Furthermore, reducing the Op Amp supply voltage to 2.5V ensures that the ADCs won't be overdriven, even if the current to be sensed exceeds the specified maximum value. In addition, the lowered Op Amp supply voltage reduces the supply current.
Resistor R1: limits the inrush current, which must be kept below 1mA to allow direct connection to the AUX output of bq76PL536A, by using this output to supply the sensor, the sensor can be switched OFF when system is put to sleep.
Capacitors C1 and C2: Ensures stable operation of U3, and noise reduction. low ESR/ESL types has been chosen for good HF noise suppression

Reference circuit (U2, C5, C3, R10, R11):

Creates a low impedance voltage source. This reference voltage of 0.1V is needed as neither the output of U1 nor the ADC input(except the GPAI ADC input) are able to operate down to 0V.
Resistors R10 and R11: Creates a voltage divider.
Capacitors C3 and C5: Ensures decoupling.
Op Amp U2: Buffer ensuring low Z_{Out}.

Charge current sense amp. (U1A, C4, R4, R5, R7, R8):

Difference amplifier, which amplifies the voltage across the shunt while current flows into the battery. The output voltage is referenced to ground which means that a offset voltage of 0.1V is applied to the ADC while charging current is zero, this is necessary as the TS1 ADC input range of the bq76PL536A do not cover voltages near 0V.

The gain must be high enough to ensure that the full scale current value results in a output voltage of 2.5V(the max. input value of the ADC). However, as the TS ADC input used for charge current monitoring, supports programmable over temperature limit, which in this case is used as a redundant charge current limit, the gain of the charge current sense amplifier must be set lower, as the max. programmable value is 2V(0.4*REG50)[18].

A redundant charge current protection limit of 19A has been selected, this limit will only be reached if the primary protection implemented in the Digital Unit fails.

$$Required\ gain = \frac{Required\ V_{Out} - V_{Offset}}{V_{In\_full-scale}} = \frac{2V - 0.1V}{19mV^*} = 100\ V/V$$

$$Gain = \frac{R7}{R6} \Rightarrow R7 = Gain * R6 = 100 * 5.1K\Omega = 510K\Omega$$

*As the shunt resistance is 1mΩ, the input will be 1mV per Ampere.

Discharge current sense amp. (U1B, R2, R3, R8, R9): Difference amplifier, which amplifies the voltage across the shunt while current flows out of the battery. The output voltage is referenced to Ref(0.1V) which is possible, as the input range of the GPAI ADC input range of the bq76PL536A includes 0V. By measuring the voltage difference between Vout and Ref, reference drift will be cancelled out.

The full-scale value is set higher than the specification requirement demands, to allow detection of overcurrent situations. A value of 55A is chosen.

$$Required\ gain = \frac{Required\ V_{Out} - V_{Offset}}{V_{In_{full-scale}}} = \frac{2.5V - 0.1V}{55mV^*} = 43.6\ V/V$$

$$Gain = \frac{R8}{R3} \Rightarrow R8 = Gain * R3 = 43.6 * 5.1K\Omega \approx 220K\Omega$$

*As the shunt resistance is 1mΩ, the input will be 1mV per Ampere.

[18] See "bq76PL536A - Battery monitor and secondary protection" in appendices

Current Sensor Simulations

Simulations has been performed to verify functionality and gain calculations. Furthermore, the bandwidth and phase margin of the amplifiers has been found. See simulations below:

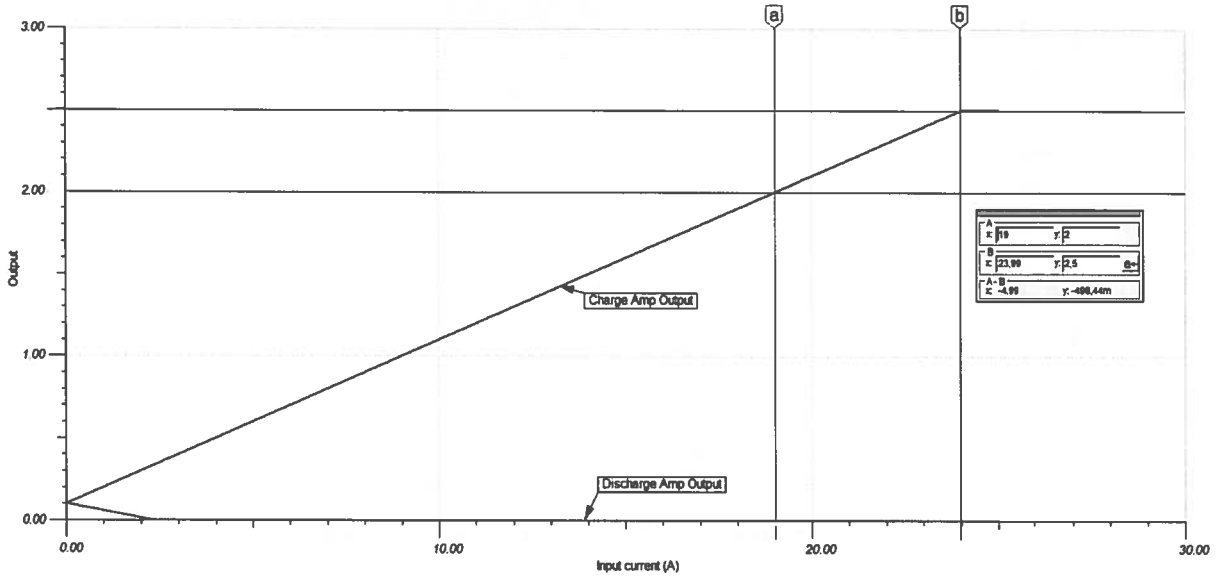

Figure 17 - DC transfer characteristics (charging)

Comment on Figure 17: Functionality is confirmed. Output voltage is 2V at a charging current of 19A as expected.

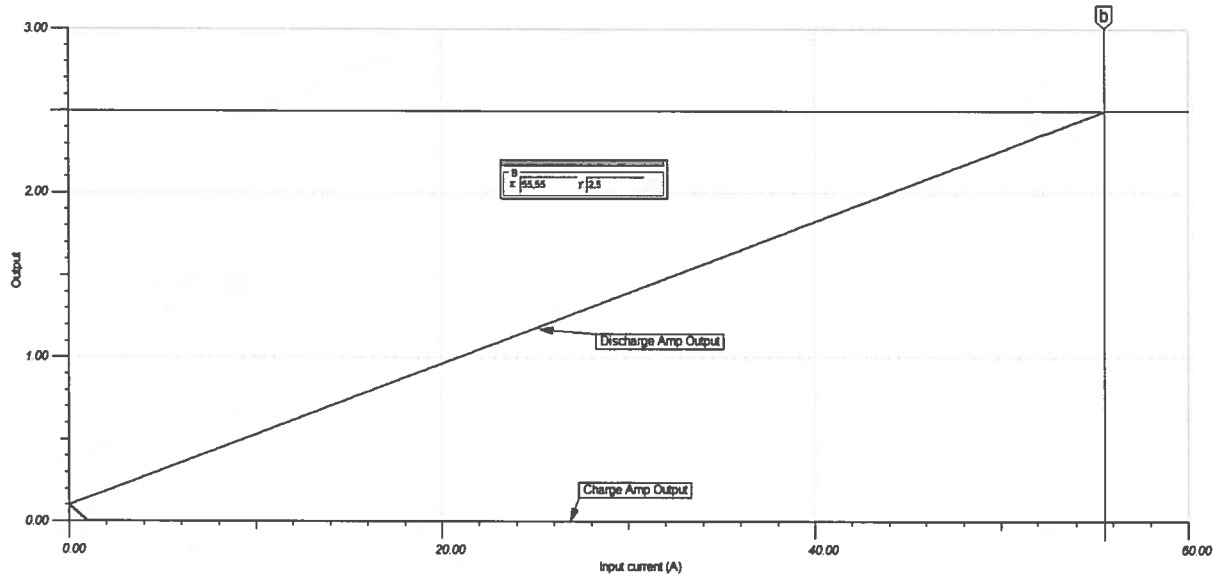

Figure 18 - DC transfer characteristics (discharging)

Comment on Figure 18: Functionality is confirmed. Output is limited by the positive rail when discharge current exceeds 55.55A, as expected.

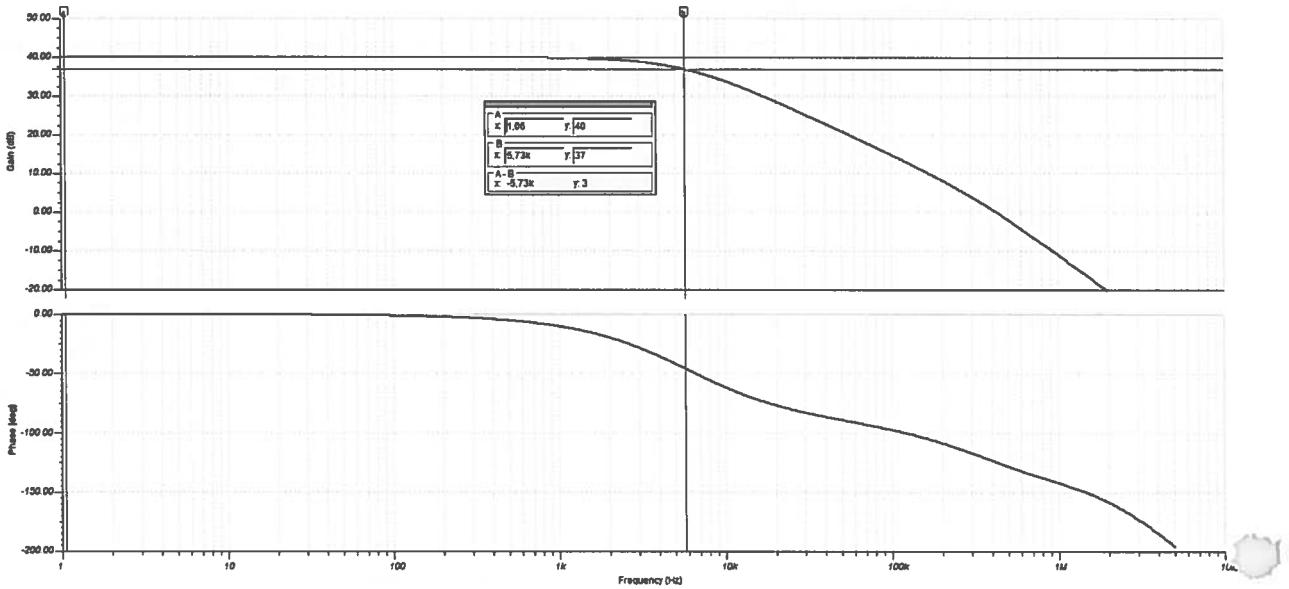

Figure 19 - Simulation of bandwidth and gain verification(Charge current amplifier)

Comment on Figure 19: It can be concluded that the expected gain is achieved. Furthermore, it can be seen that the closed loop bandwidth is 5,73KHz. The noise could be decreased by reducing the bandwidth of the amplifier, this is however considered unnecessary as the signal is subsequently filtered by the anti-aliasing filter placed at the ADC input.

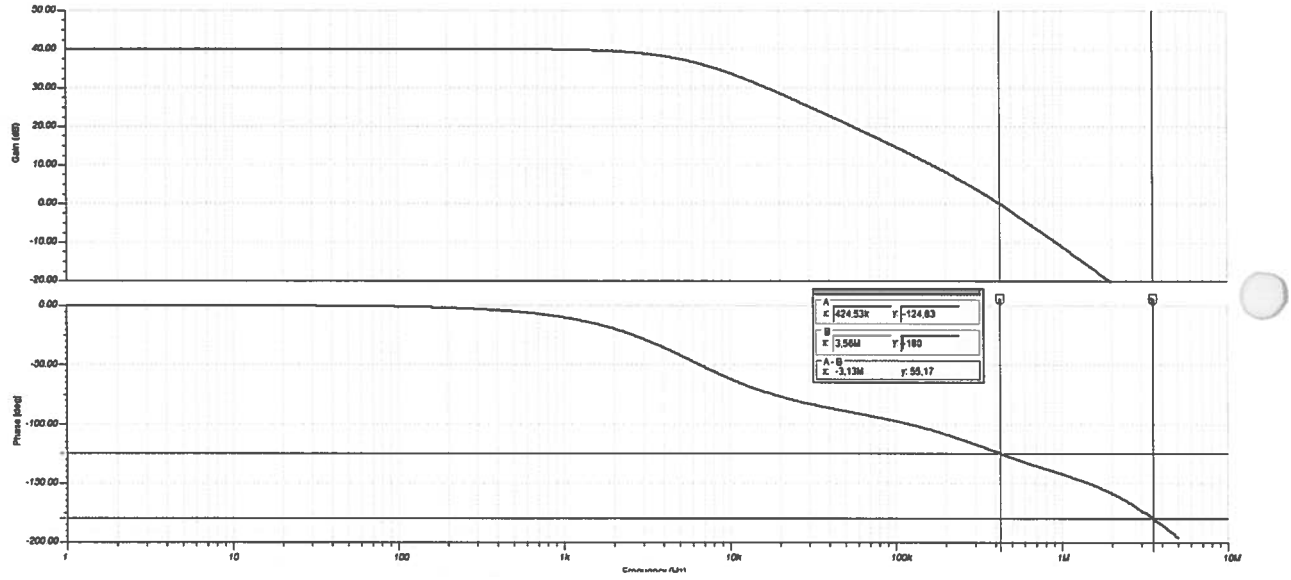

Figure 20 - Phase margin(Charge current amplifier)

Comment on Figure 20: The phase margin is 55° for the unloaded amplifier. The phase margin must be taken into consideration if a capacitive load is applied.

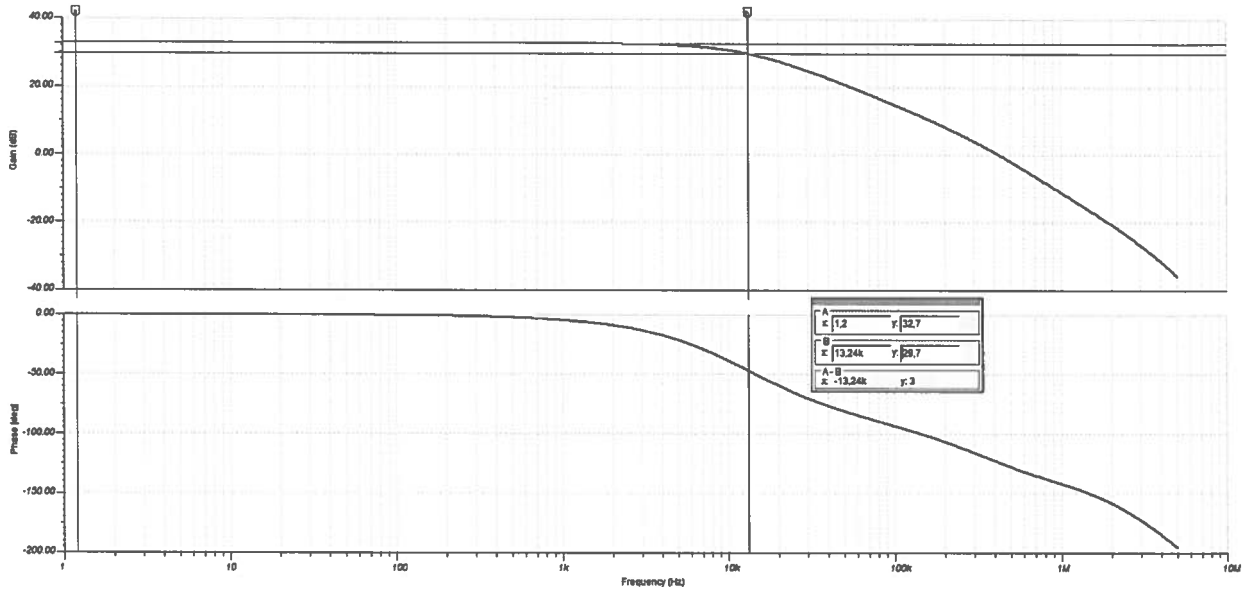

Figure 21 - Simulation of bandwidth and gain verification(Discharge current amplifier)

Comment on Figure 21: It can be concluded that the expected gain is achieved. Furthermore, it can be seen that the closed loop bandwidth is 13.24KHz.

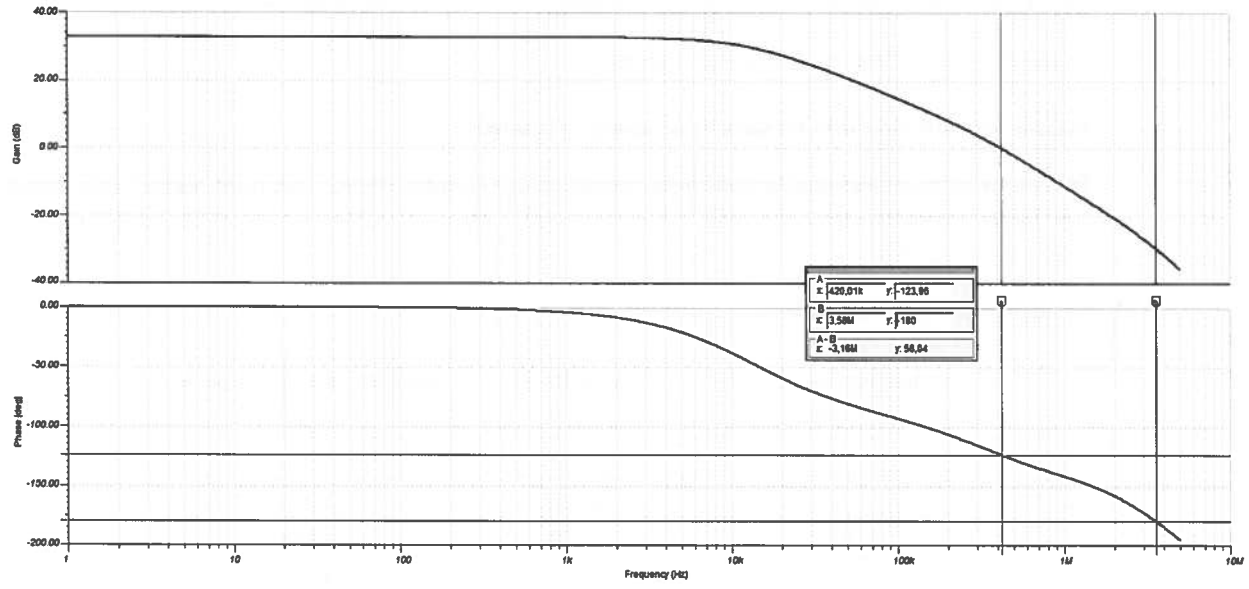

Figure 22 - Phase margin(Discharge current amplifier)

Comment on Figure 22: The phase margin is 56° for the unloaded amplifier. The phase margin must be taken into consideration if a capacitive load is applied.

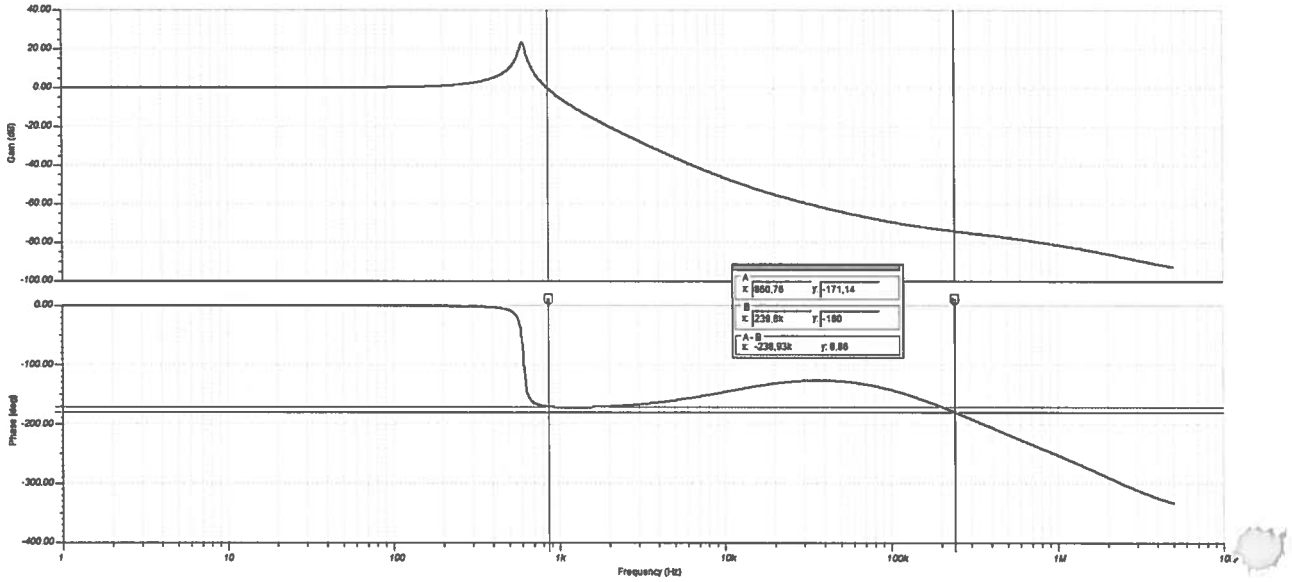

Figure 23 - AC transfer characteristics of Buffer(U2)

Comment on Figure 23: Even though the OPA333 is internally compensated and stated to be unity gain stable, the phase margin of the buffer(U2) is only 9° while unloaded. However, as no stability issues has been detected, no further compensation has been considered necessary.

Current Sensor Test and Measurements

Supply current: 44.4uA (Vsupply = 5V, output unloaded)

To ensure correct functionality and linear operation, the Current Sensor has been tested. The output has been measured after the ADC to include ADC gain and offset errors in the calculation of calibration constants.

Charge current sense Amp.

Measurement No:	Input [mA]	Output [raw ADC value]
1	0	691
2	500	1033
3	1000	1350
4	1500	1672
5	2000	2012

Figure 24 - Measurements performed to acquire calibration information(Charge)

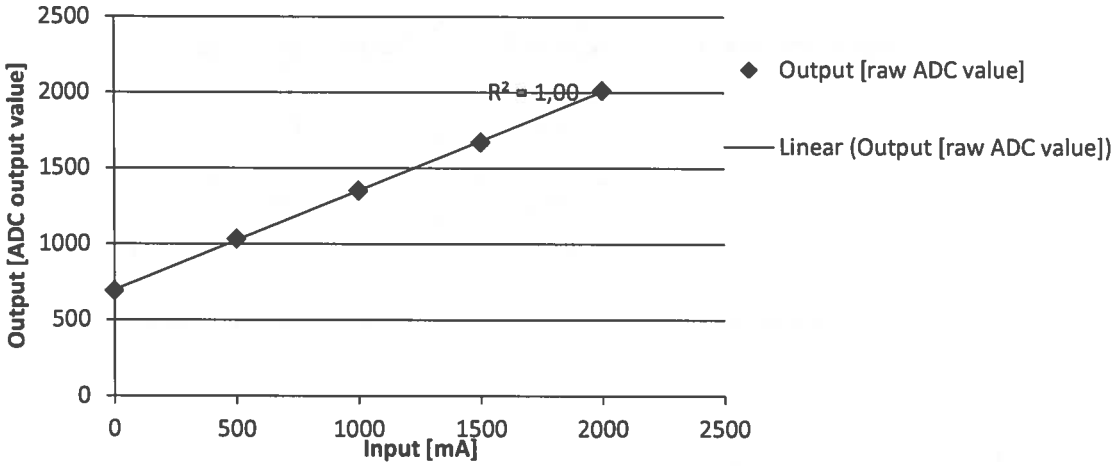

Figure 25 - Graphical presentation of measurements and trend line(Charge)

Calibration constants for the charge current sense amplifier has been found based on the trend line slope and interception point. The binary to mA conversion, implemented in the source code can be seen below:

```
if(Icharge < Ich_offset)
{
    Icharge = 0;
}
else
{
    Icharge = (unsigned long)(Icharge - Ich_offset)*1480/1000;
}
```

Discharge current sense Amp.

Measurement No:	Input [mA]	Output [raw ADC value]
1	0	10
2	500	150
3	1000	291
4	1500	436
5	2000	579

Table 20 - Measurements performed to acquire calibration information(Discharge)

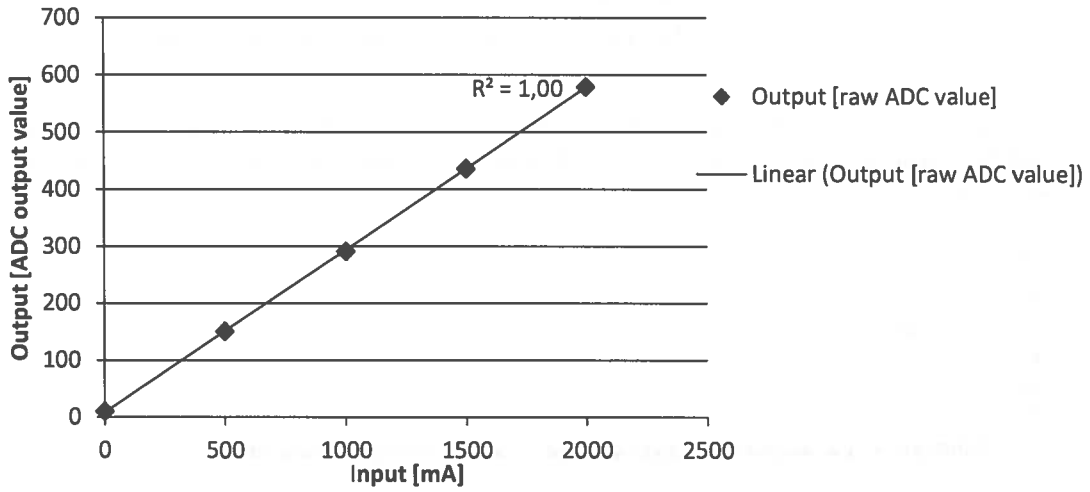

Figure 26 - Graphical presentation of measurements and trend line(Discharge)

Calibration constants for the discharge current sense amplifier has been found based on the trend line slope and interception point. The binary to mA conversion, implemented in the source code can be seen below:

```
//GPAI ADC input raw value converted to mA
Idischarge = (Rec_buffer[1]<<8) + Rec_buffer[2];

if(Idischarge < Idis_offset)
{
    Idischarge = 0;
}
else
{
    Idischarge = (unsigned long)(Idischarge - Idis_offset)*35/10;
}
```

3.1.5. Isolation Switch

This unit consist of a isolation switch relay and a pre-charge circuit. While relays are a bad solution in an low power application, they have been considered the only solution as real physical isolation of the battery, in the event of errors, has been required by the Shell Eco-marathon committee. If this BMS is to be used in commercial applications, the Isolation Switch should be redesigned and implemented using low RDS MOSFETS, as this will dramatically decrease the supply current.

As the driver and transient protection is implemented as part of the Analog Front End, the Isolation Switch circuit is very simple and can be seen in Figure 27

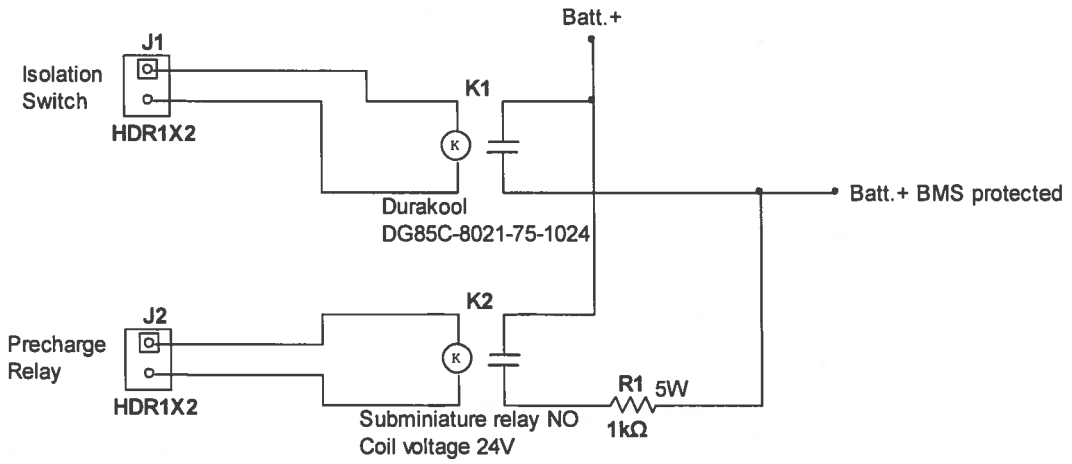

Figure 27 - Isolation Switch circuit

Isolation Switch component description and calculations

Relay K1: Isolation relay performing interruption of battery current flow. Coil voltage: 24V, Max. break current 80A.

Relay K2: Pre-charge relay, when closed the load capacity will be charged through R1.

Resistor R1: Pre-charge resistor. Limits pre-charge current to $V_{Battery}$/R1.

Isolation Switch Test and Measurements

Test of this unit will be performed as part of the accept test. See accept test chapter.

3.1.6. Digital Unit (HW)

This Unit consist of a number of circuits, an overview of designed circuits can be seen in Figure 28.

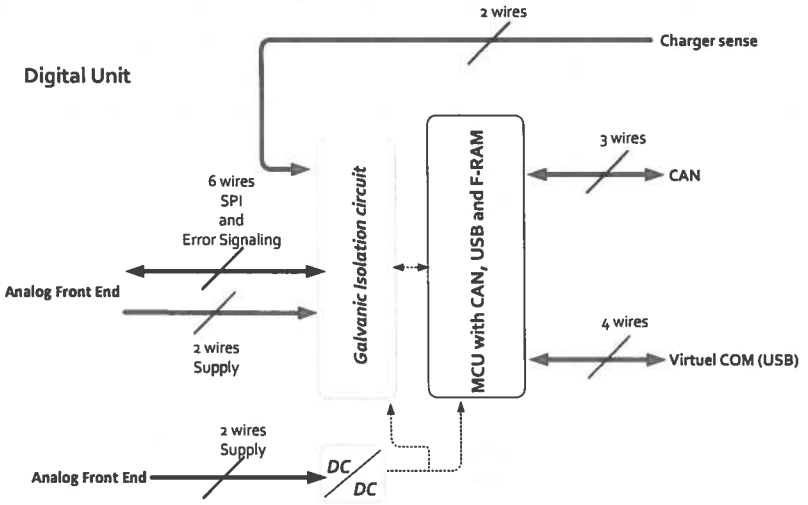

Figure 28 - Digital Unit circuit blocks

3.1.6.1. Galvanic Isolation circuit

This circuit performs the galvanic isolation between the battery side and the communication side, connected to auxiliary units. A number of techniques can be used to accomplish isolation, these includes the use of digital isolators based on optocouplers, and iCouplers a technology patented by Analog Devices.

The digital isolator ISO7141CC from Texas Instruments and The iCoupler ADuM1401 from Analog Devices has been used to compare technologies.

Digital Isolator(ISO7141CC) pros and cons: High speed can be achieved, however both the dynamic and static supply current at both sides of the isolator are unacceptably high[19].

iCoupler(ADuM1401) pros and cons: Very high speed, low dynamic supply current. Unacceptably high static supply current at both sides of the isolator when not in use[20].

As none of above solutions offers satisfying low power consumption, another approach based on dual optocouplers has been implemented. This allows a design which consumes very little power while in use and next to no power while quiescent.

As it is desirable to be able to drive the light source of the optocouplers directly from the pins of bq76PL536A and the MCU unit, and as low power consumption is required optocouplers with high Current Transfer Ratio(CTR) has been chosen. The optocoupler offers open collector outputs for which the pull-up has been selected based on specific data speed requirements, so that data with less level shifts(e.g. Slave Select) is equipped with a weaker pull-up for reduced consumption. As the SPI bus is shared, an enable functionality is implemented and connected to Slave Select for the Analog Front End, this ensures that the galvanic isolation do not consume power when the SPI bus is used for non-isolated devices.

[19] See " iso7141cc - digital isolator" in appendices
[20] See " ADuM1400_1401_1402 - iCoupler" in appendices

The Galvanic Isolation circuit can be seen in Figure 29.

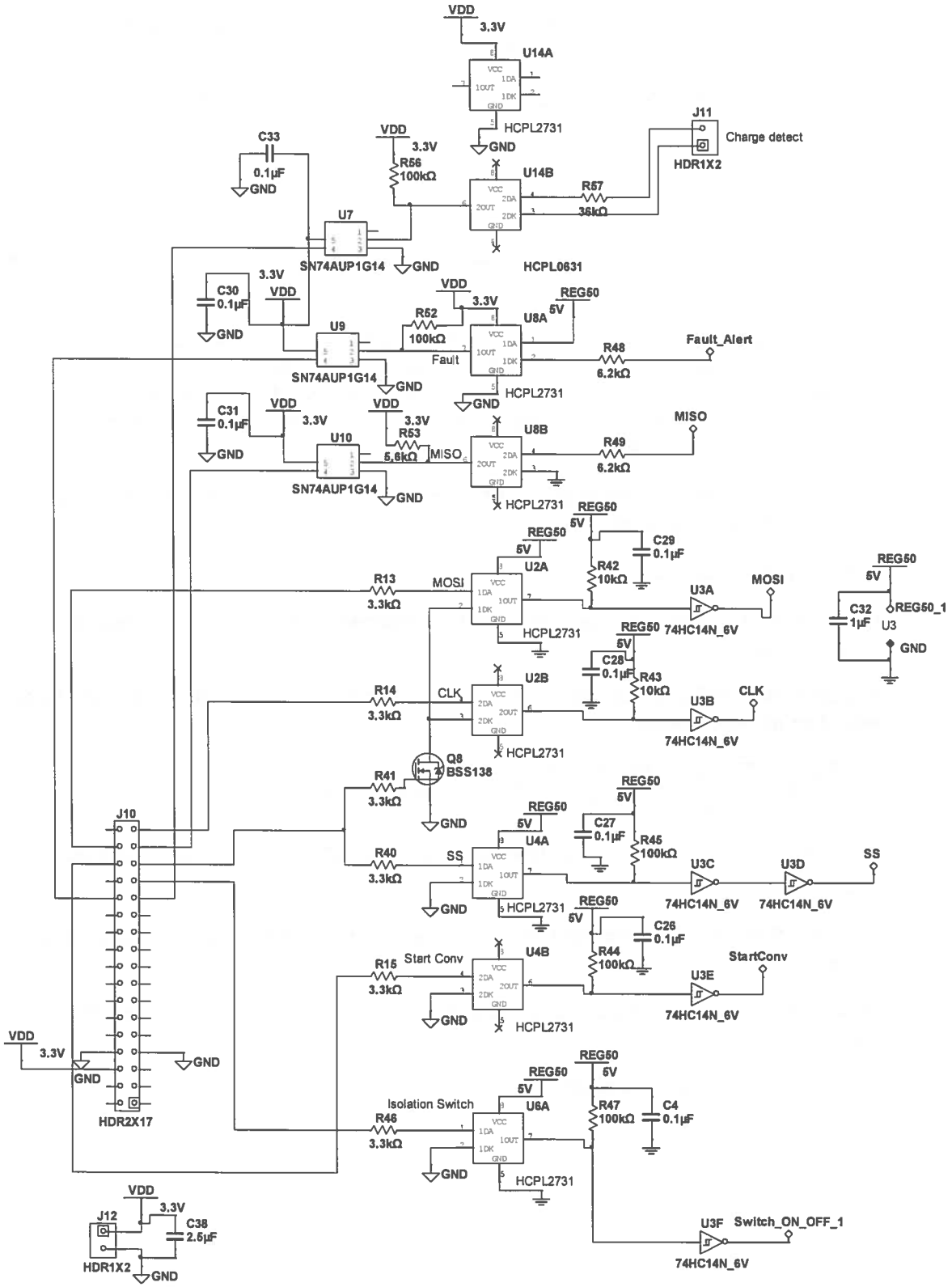

Figure 29 - Galvanic Isolation circuit

Galvanic Isolation component description and calculations

Optocouplers U2, U4, U6, U8, U14: Performs the galvanic isolation, chosen based on low input current requirement, high CTR, relatively high speed and SMD package.

Resistors R13, R14, R15, R40, R41 and R46: Determines the forward current of optocoupler LEDs at the MCU side of the galvanic isolation.

$$R = \frac{V_{In_{high}} - V_{forward}}{Required\ I_{forward}} = \frac{3.3V - 1.25V}{0.6mA} \approx 3.3K\Omega\ (rounded\ to\ E24\ value)$$

Where $V_{In_{high}}$ is the voltage of a logic high applied from the MCU, and $V_{forward}$ is the voltage across the LED.

Resistors R52, 53 and 56: Pull-up resistors dimensioned so that charge sense and fault, which do not require fast state shift, has weaker pull-up resistors and thereby consumes less power while optocoupler is in saturation mode, compared to the pull-up for the MISO(R53) data signal which has shorter rise and fall times but consumes more power. R53 has been trimmed to match speed of MOSI and CLK isolation stages.

MOSFET Q8: Enable/Disable switch which is controlled by SS and ensures that the galvanic isolation is only active when required.

Resistor R41: Limits I_{Gate}.

Inverters U7, U9, U10: Reshapes data(edges are sharpened). And ensures that logic levels are clearly defined.

Resistors R48, R49 and R57: Determines the forward current of optocoupler LEDs at the Battery side of the galvanic isolation.

$$R = \frac{V_{In_{high}} - V_{forward}}{Required\ I_{forward}} = \frac{5V - 1.25V}{0.6mA} \approx 6.2K\Omega\ (rounded\ to\ E24\ value)$$

Where $V_{In_{high}}$ is the voltage of a logic high applied from the MCU, and $V_{forward}$ is voltage across the LED.

Resistors R42, R43, R44, R45 and R47: Pull-up resistors, for dimensioning see: Resistors R52, 53 and 56

Inverter U3: Reshapes data(edges are sharpened). And ensures that logic levels are clearly defined.

All capacitors: Decoupling of supply.

Galvanic Isolation Test and Measurements

Measurement Figure 30 confirms the expected functionality. Initial tests has been performed with weaker pull-up resistors and thereby faster fall and rise times. However, the performance was then limited by the narrowing of first bit in the first byte to be send, as can be seen in Figure 31 (As the voltage must fall from a higher level when the first bit is transferred, the output rising edge is delayed and thereby the pulse is narrowed). This issue can be solved by decreasing the SPI speed of the first byte, which was successfully implemented. However, the propagation delay then becomes a limitation. The solution has been low data transfer speed, with weak pull-up resistors and thereby low power consumption.

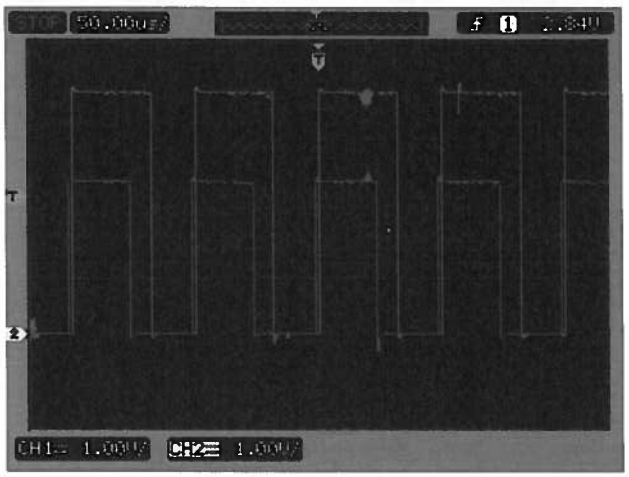

Figure 30 - Input and output of galvanic isolation (SCLK) (Green = Input)

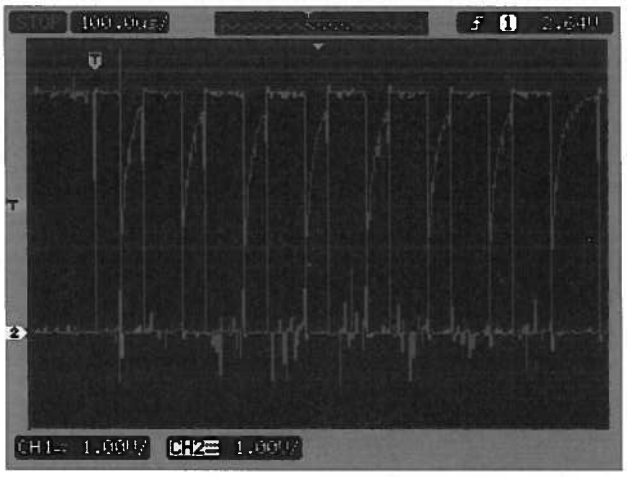

Figure 31 - Output before and after inverter

3.1.6.2. DC / DC converter

The consumption of this unit is critical, as it must be active at all times(except from low voltage lock-out described later). All prefabricated commercial DC/DC converters has been found to have a high no-load supply current and a too high minimum load requirement for this application. Commercial dc/dc converter comparison can be seen in Table 21(V_{In} = 12V for compared converters. However, no 24V version with significantly better performance has been found).

CHARACTERISTICS OF COMMERCIAL DC-DC CONVERTERS

Manufacturer	Model	Vi (V)	Vo (V)	Io (A)	Ii (Io=0) (mA)	η (%)	Isol.
TRACO POWER	TEN 5-1210	12	3.3	1.2	20	77	yes
XP Power	JCA0412S03	12	3.3	1.2	38	83	yes
RECOM	RW-123.3S	12	3.3	0.7	21	65	yes
C&D Technologies	HL02R12S05	12	5	0.4	40	60	yes
BOURNS	MX3A-12SA	12	3.3	3.0	11	93	no
RECOM	R-78A3.3-1	12	3.3	1.0	7	81	no

Table 21 - Comparison of commercial converters[21]

To meet the required power consumption an ultra low power DC/DC converter has been designed. As the required output current is below 20mA at all times and only 1/10 of this value most of the time, the no-load quiescent current is of great importance. Two techniques has been used to dramatically decrease the power demand, Pulse Frequency Modulation(PFM) switching(as oppose to more traditional PWM), and regulation without feedback from the secondary side, to eliminate the power consumption associated with the use of optocoupler or transformer feedback. Furthermore the converter is designed to eliminate the need of preloading. The converter has been based on the LT8300, a controller featuring PFM switching(actually it uses a combination of different switching schemes to be exact) , integrated switch and output voltage regulation based on sampling of the primary-side flyback pulse waveform[22]. To keep the size and weight low, and to improve EMC performance, a shielded dual inductor has been used as alternative to a traditional transformer. Low voltage lock-out is implemented and disables the converter, to prevent further discharge of a deeply discharged battery. The implemented circuit can be seen in Figure 32.

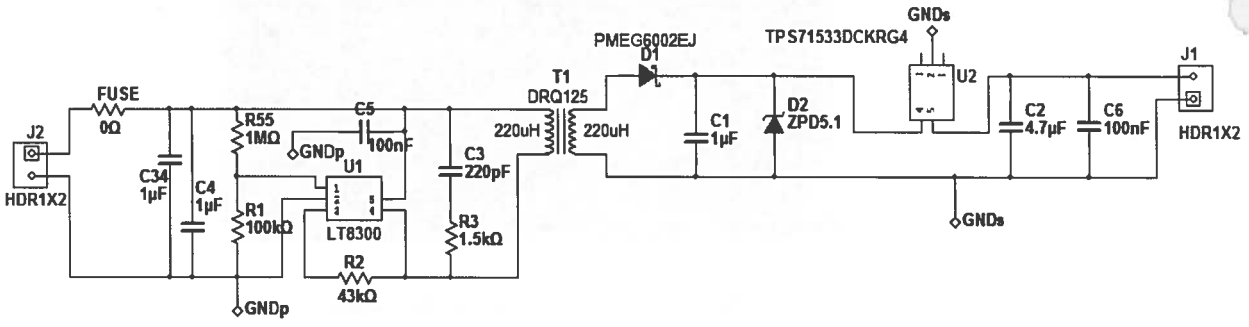

Figure 32 - DC/DC converter circuit

[21] Rodrigo et al. date unknown. http://www.icrepq.com/icrepq-08/434-de-diego.pdf (date:14-04-13)
[22] See "LT8300 - flyback converter IC" in appendices

DC/DC converter component description and calculations

Flyback converter controller and switch U1: Performs and regulates the switching based on primary-side flyback pulse waveforms measured across the switch while OFF.

Capacitors C34, C4 and C5: Serves as charge reservoir, to ensure a steady input current flow. And decouples noise present at the supply rail.

Resistors R1 and R55: This voltage divider sets the low voltage lock-out threshold and hysteresis. Values has been calculated according to application note:

$$V_{UpperThreshold} = \frac{1.239V*(R55+R1)}{R1} + 2.5uA * R55 = 16.13V$$

$$V_{LowerThreshold} = \frac{1.223V*(R55+R1)}{R1} = 13.45V$$

RC snubber R3 and C3: Reduces ringing to improve EMI performance and to avoid false triggering of the boundary mode detector which is a part of the regulation scheme. The capacity has been found empirically by measuring the period of the ringing and subsequently add capacity till the period is doubled[23]. Then the appropriate series resistance has been calculated, using Equation 1.

$$C_{PAR} = \frac{C_{SNUBBER}}{\left(\frac{t_{PERIOD(SNUBBED)}}{t_{PERIOD}}\right)^2 - 1}$$

$$L_{PAR} = \frac{t_{PERIOD}^2}{C_{PAR} * 4\pi^2}$$

$$R_{SNUBBER} = \sqrt{\frac{L_{PAR}}{C_{PAR}}}$$

Equation 1 - Extracted from LT8300 datasheet page 15

Resistor R2: Feedback resistor, which determines the voltage across C1(output before LDO). Calculated based on datasheet guidelines, subsequently empirically trimmed to V_{C1} = 4V.

Shielded dual inductor/transformer T1: Used as 1:1 transformer, lighter smaller and cheaper compared to traditional transformers, the drawback is reduced coil to coil isolation(200Vac).

Schottky rectifier PMEG6002EJ: A rectifier with low forward voltage has been selected to decrease loses. Required reverse voltage and forward current has been calculated based on datasheet[24] guidelines.

Capacitor C1: Filter capacitor, a low ESR type has been selected to decrease output ripple.

Zener diode D2: When the converter is unloaded, the output starts to climb, in this situation D2 will start conduct and thereby act as a light load, which prevent further climbing. This ensures a lower no-load quiescent current compared to a resistive preloading. It does however impose the need of a low drop out regulator at the output.

LDO U2: Low dropout regulator, required as technique mentioned above allows some voltage climbing which is not tolerable at the converter output. The dropout is kept low to decrease the negative impact on the efficiency.

Capacitors C2 and C6: Required for stable operation of U2 and noise reduction, low ESR/ESL types has been chosen for good HF noise suppression.

---

[23] Method extracted from LT8300 datasheet.

[24] See "LT8300 - flyback converter IC" in appendices

DC/DC converter Test and Measurements

For all performed tests V_{in}=24V unless otherwise stated.

Output current	Input current (with snubber)	Input current (without snubber)	Output voltage	Efficiency (with snubber)	Efficiency (without snubber)
0 (no-load)	**0.24 mA**	**0.23 mA**	3.32V		
3.3 mA	1.26 mA	0.92 mA	3.32V	36%	49%
9.8 mA	3.42 mA	2.52 mA	3.32V	40%	54%

Table 22 - DC / DC converter results

Max. output current: 50mA

Min. output current: 0 (no loading required)

Voltage lockout: Upper threshold 16.1V, Lower threshold 13.4V(Converter will shut down when V_{in} drops below 13.4V and assume normal operation when V_{in} raises above 16.1V)

Max. input voltage: 55V (calculated value, operation subsequently confirmed by test)

Measurements to determine necessity of snubber and noise filtering

RC snubber measurements has been performed during construction, see measurement results below.
All measurements below has been performed with a 1KΩ load at the output.

Figure 33 - Ringing at drain without snubber

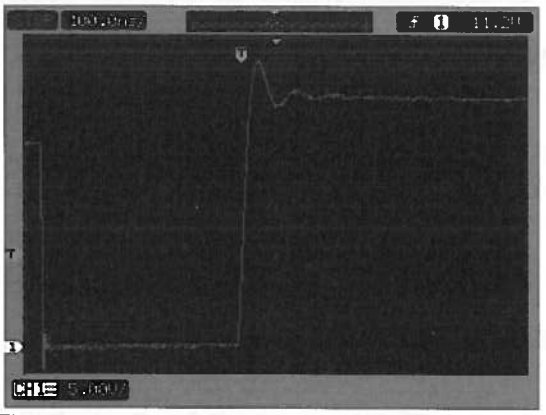

Figure 34 - Ringing at drain with RC snubber

To ensure compatibility with connected system units and to test the necessity of snubber the noise performance has been tested. As seen in Figure 35 the switch turn ON(falling edge of Vdrain) at primary side results in ringing at the output. The amplitude of this ringing is not decreased with the presence of a snubber and is dominant compared to the ringing present at switch OFF. Therefore, and because the snubber appeared to only slightly improving the load regulation, the snubber has been removed to improve efficiency.

Figure 35 - Switching noise (yellow = Vdrain, green = Vout)

The ringing created at switch ON results in a $Vout_{Peak}$ which exceeds the maximum voltage tolerated by the digital circuits which are to be supplied by this dc/dc converter. Therefore filtering has been implemented in terms of a ferrite bead. The output wires are wound two turns around this ferrite bead resulting in a significant reduction as seen in Figure 36 (A 15nF capacitor was mounted across load resistor, to simulate decoupling capacitors present at digital circuits to be supplied).

Figure 36 - Output ringing before and after ferrite bead filtering

3.1.6.3. MCU with CAN, USB and F-RAM

This unit contains a Microcontroller with CAN controller, non-volatile memory and a USB interface. The CAN functionalities of the BMS are rather limited, therefore a mainstream microcontroller like the AVR Mega32 could have been used, as an emulated CAN interface would have been sufficient. However, by using a microcontroller with integrated CAN controller, a platform prepared for future improvements has been created. This is considered useful as implementation of a de facto CAN protocol is considered a necessity if this BMS is to be a commercial success.

As data logging is required, the memory included in the microcontroller is not sufficient, a number of solutions have been considered; SD cards which are cheap but too power consuming and not made for operation in a harsh environment, EEPROM which is non-volatile but have limited write cycles, battery backed-up RAM a reasonable solution but more consuming than the implemented solution which is based on F-RAM. Ferroelectric RAM(F-RAM) offers 10^{14} write cycles, very low power consumption between writes and is non-volatile[25]. It is therefore considered the obvious choice in an application where cost is of less concern.

The MCU has been implemented by modifying a OLIMEX AVR-CAN development board[26], The CAN Transceiver has been replaces and a number of unused components has been removed, USB and F-RAM has been added, but is physically located at another PCB. The implemented circuit can be seen in Figure 37 and Figure 38.

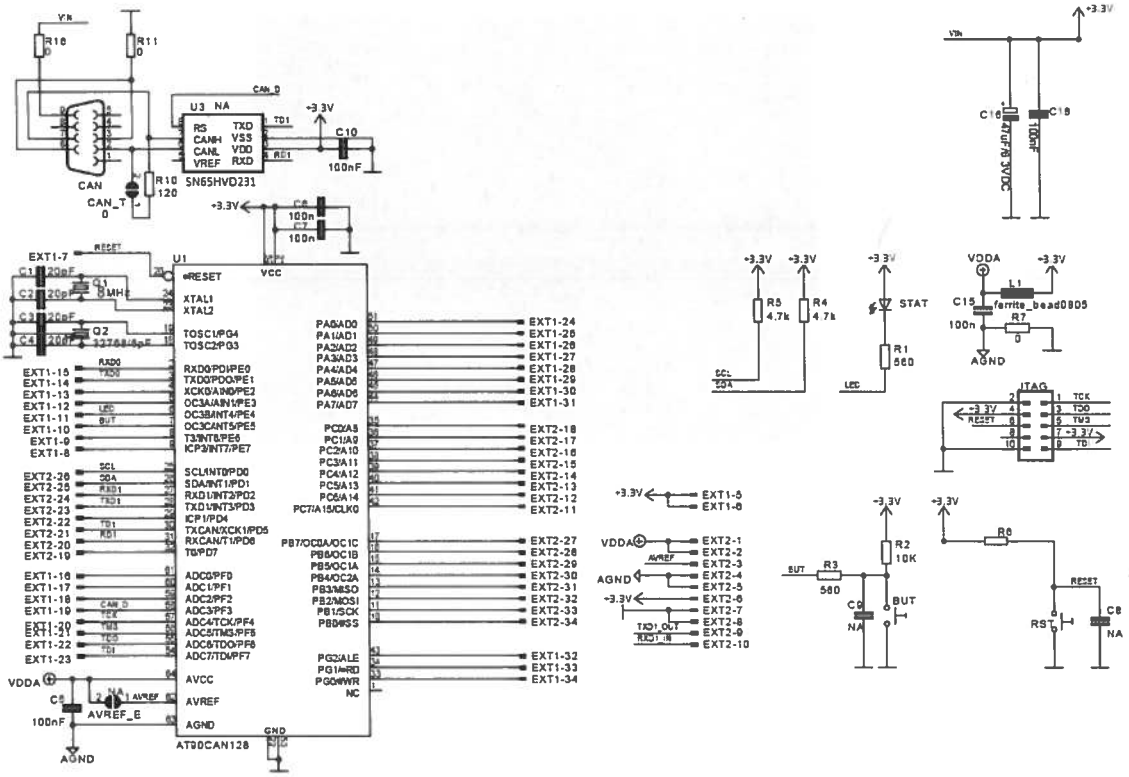

Figure 37 - MCU and CAN transceiver circuit

[25] See "FM25V20 - F-RAM memory IC" in appendices
[26] See "AVR-CAN" in appendices