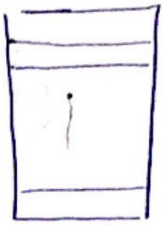
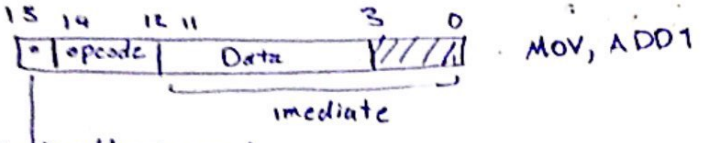
ISA → 6 members → opcode; 3bits

CPU Registers → AX, BX, CX, DX → 2 bit address



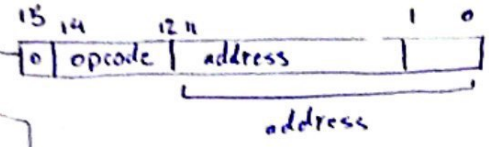


1024 * 16

2^{10}

addressing → 10 bits

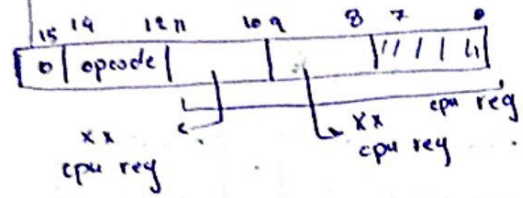
addressing mode



Functional Instructions

ADD1 SUB

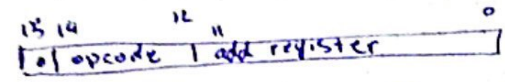
ADD2



Transfer Instruction

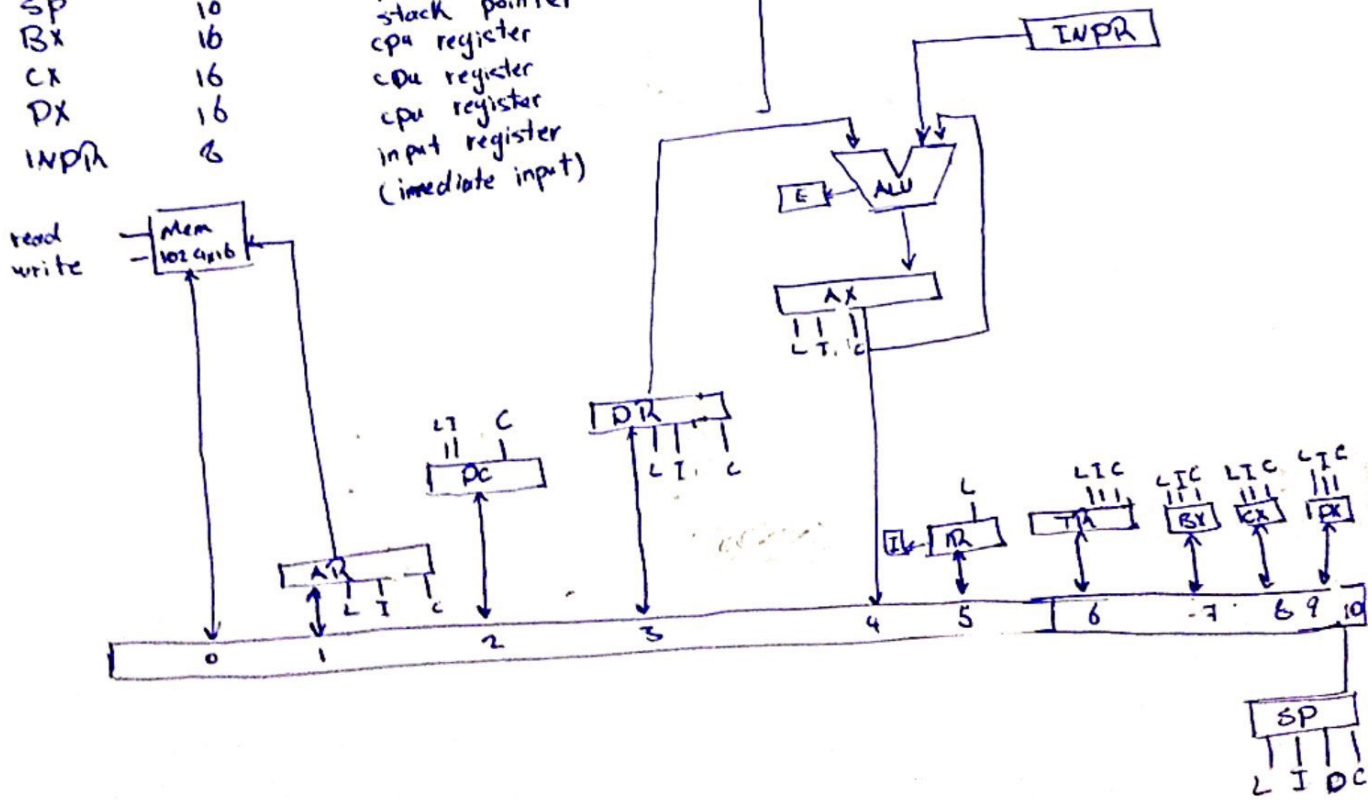
Mov PUSH

POP



TR	16	Temporary Register
DR	16	Data Register
AR	10	Address Register
AX	16	Accumulator
IR	16	Instruction Register
I	1	address model
PC	10	program counter
SP	10	stack pointer
BX	16	cpu register
CX	16	cpu register
DX	16	cpu register
INPR	8	input register (immediate input)

4 bit select



MOV AC ← INPR

ADD1 AC ← AC + INPR

ADD2 AC ← AC + M[address]

SUB AC ← R[add1] − R[add2]

نباید طوری CPU Register

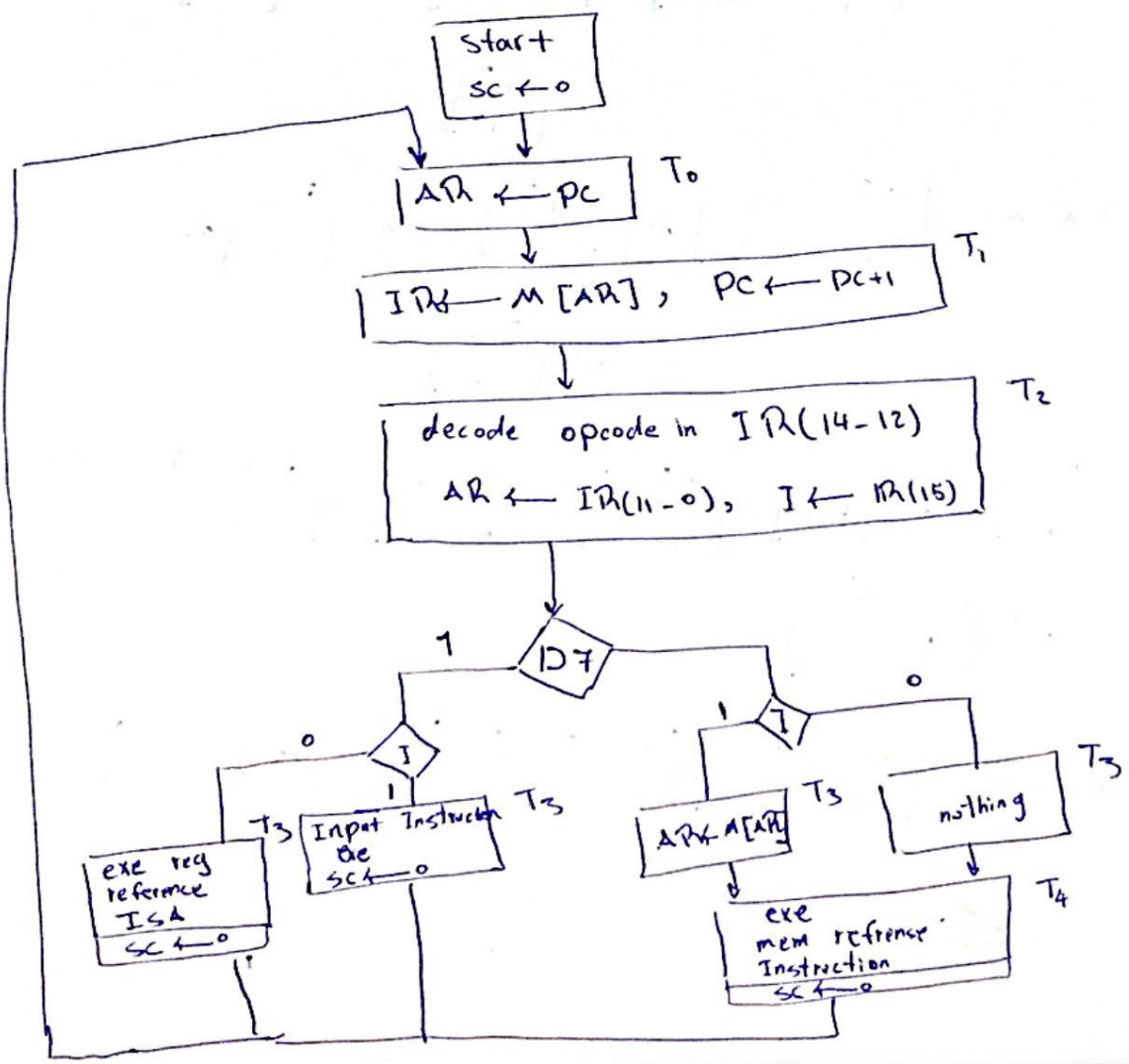
PUSH M[SP] ← R[address] , SP ← SP+1

POP R[address] ← M[SP] , SP ← SP−1

کوتاه ترین ← MOV

طولانی ترین ← POP

چون هم میتوی Reg و هم خواندن از decrement هم Mem



SP	Stack pointer	load, clear, Increment (Push), Decrement (Pop)
I : IR	Instruction Register	load
PC	load, clear, Increment	

2) Total = $100 \times 50 = 5000$ number of Instructions

$f = 1$ BHz

clock per instruction = 1.25

CPI

exe time $= n \times \overline{CPI} \times \frac{1}{f} = 5000 \times 1.25 \times \frac{1}{10^9} = 6.25 \times 10^{-6}$

$MIPS = \overline{IPC} \times f \times 10^{-6} = \frac{1}{\overline{CPI}} \times f \times 10^{-6} = \frac{1}{1.25} \times 10^9 \times 10^{-6} = \frac{10^3 \times 10^2}{125} = \underline{300}$

3)

$f = 60 \times 10^6$ Hz

$$\overline{CPI} = \frac{\overbrace{40\times1 + 20\times3}^{100} + \overbrace{30\times1 + 10\times2}^{40}}{100} = 1.4$$

$$MIPS = \frac{1}{\overline{CPI}} \times f \times 10^{-6} = \frac{10}{14} \times 60 \times 10^6 \times 10^{-6} = \frac{600}{14} = 42.85714429$$