

Verification Phase Gate

Revision

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SME

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Abstract

This document describes the process used to confirm that all work products specified within the verification phase are complete and sufficient to generate the work products required by applicable certification standards.

Group / Owner

Security / Secure Assessor

Motivation

This document is motivated by the need to have formal processes in place for the verification and sign-off of phase products necessary for the creation of certification work products required for the certification safety-critical, cyber-physical systems, such as **ISO 21434** and **ISO 26262**.

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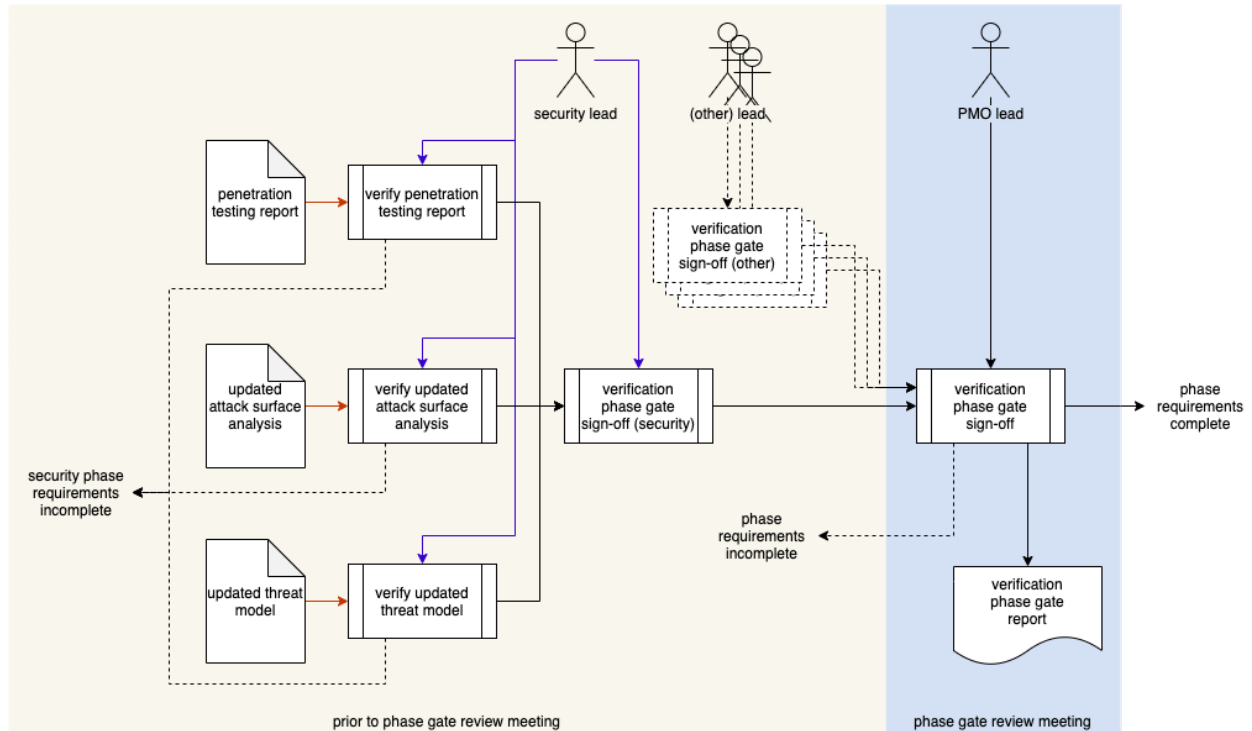
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Overview

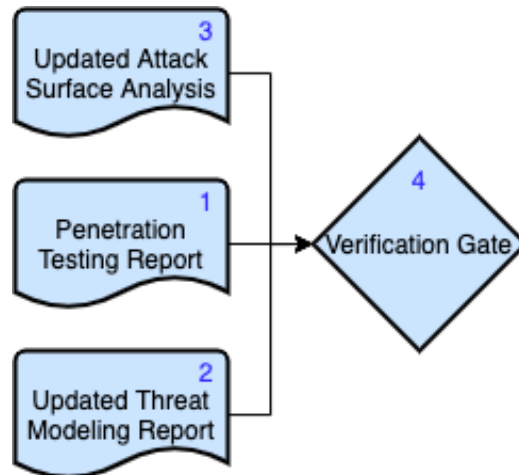
The implementation phase gate provides a point of process synchronization for all organizational groups to confirm that their process requirements have been fulfilled. The outcome is either a passing of the gate (transition to the design phase) or failure to pass (required products are incomplete).

The following diagram illustrates the process to be used:



Process

The following diagram is taken from the implementation phase section of the **AVCDL** product dependencies graph.



As shown by the blue numbers in the upper right corner of each element, we can see that the requirements phase gate has three gated phase requirements with three products.

Note: Activities stemming from non-dependent phase requirements may be undertaken in parallel.

The following phase requirement products need to be verified as completed for the gate to be signed off:

1. **Penetration Testing Report**
2. **Updated Attack Surface Analysis**
3. **Updated Threat Model Report**

The process is broadly divided into two parts: prior to the phase gate review meeting and the meeting itself. Activities taking place prior to the meeting are conducted separately by each group with a dependency on the gate. Failure during these activities precludes the meeting taking place, as any such failure would cause the gate to be failed.

Penetration Testing Report Verification

Inputs	Penetration Testing Report
Outputs	none
Participants	Security Lead

The security lead verifies that the **Penetration Testing Report** phase requirements product for the element under consideration are complete. If they are not complete, the gate should not be entered and the PMO should be informed.

Updated Attack Surface Analysis Verification

Inputs	Updated Attack Surface Analysis
Outputs	none
Participants	Security Lead

The security lead verifies that the **Updated Attack Surface Analysis** phase requirements product for the element under consideration are complete. If they are not complete, the gate should not be entered and the PMO should be informed.

Updated Threat Model Report Verification

Inputs	Updated Threat Model Report
Outputs	none
Participants	Security Lead

The security lead verifies that the **Updated Threat Model Report** phase requirements product for the element under consideration are complete. If they are not complete, the gate should not be entered and the PMO should be informed.

Verification Phase Gate Signoff (Security)

Inputs	none
Outputs	none
Participants	Security Lead

The security lead signs off that all security-related products for this phase are complete and in good order. The PMO is informed of this.

Verification Phase Gate Signoff

Inputs	none
Outputs	Verification Phase Gate Report
Participants	PMO Lead

If all participating groups provide signoffs the phase gate review meeting takes place. During this meeting all parties satisfy themselves that all their dependencies upon other groups are met. If there are no issues raised, the PMO lead signs off that all products for this phase are complete and in good order. Otherwise, the gate is not passed. The PMO produces the **Verification Phase Gate Report** to document the gate outcome.

At a minimum, the report contains formal sign-off from each group's lead with a list of the phase products verified.

References

1. **AVCDL Product Dependencies** (in **AVCDL** main document)
2. **Verification Phase Gate Report**
3. **Penetration Testing Report** (**AVCDL** secondary document)
4. **Updated Attack Surface Analysis** (**AVCDL** secondary document)
5. **Updated Threat Model Report** (**AVCDL** secondary document)