

# Updated Attack Surface Analysis

## Revision

Version 5  
2/8/24 2:00 PM

## SME

Charles Wilson

## Abstract

This document describes the process used to update the attack surface analysis report.

## Group / Owner

Security / Security Architect

## Motivation

This document is motivated by the need to determine whether the security deficiencies identified during the design phase have been appropriately disposed. This is necessary given the nature of safety-critical, cyber-physical systems, subject to certifications such as **ISO/SAE 21434** and **ISO 26262**.

## License

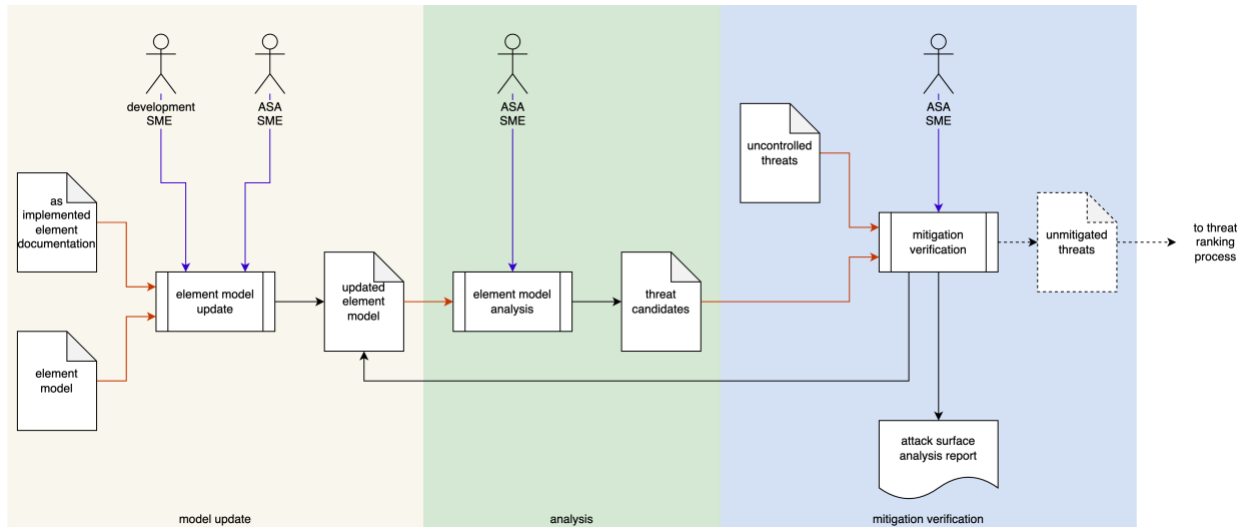
This work was created by **Motional** and is licensed under the **Creative Commons Attribution-Share Alike (CC BY-SA-4.0)** License.

<https://creativecommons.org/licenses/by/4.0/legalcode>

# Overview

Many changes can occur between the creation/update of an element model during the design phase and the verification phase. Reviewing the model allows for the verification that issues identified for mitigation have been appropriately dealt with and that no new issues have arisen.

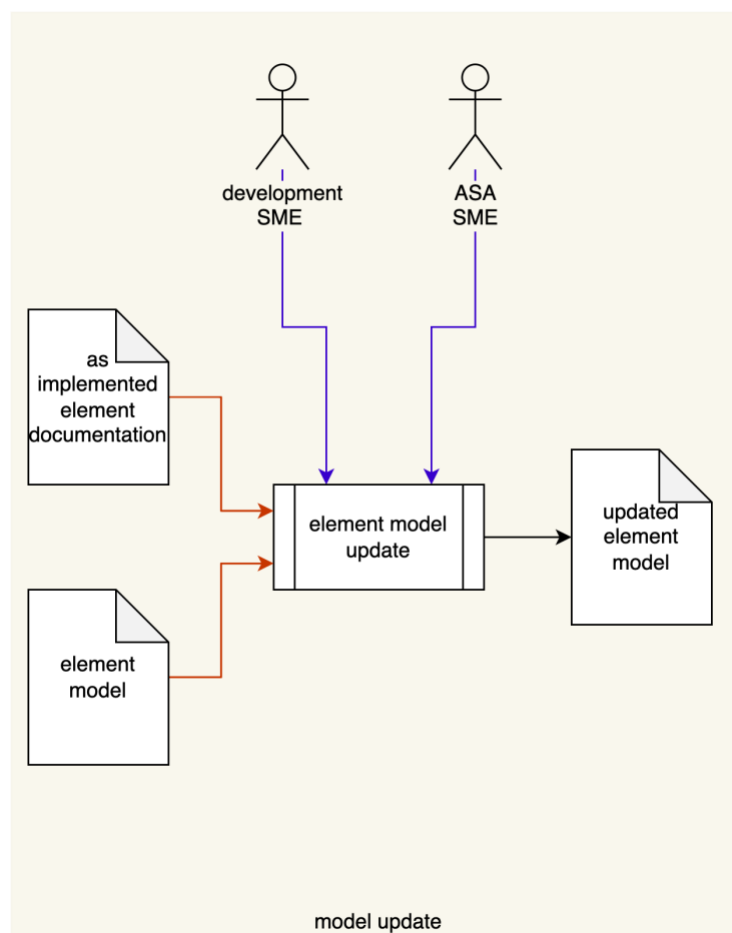
The following diagram illustrates the process to be used:



# Process

## Model Update

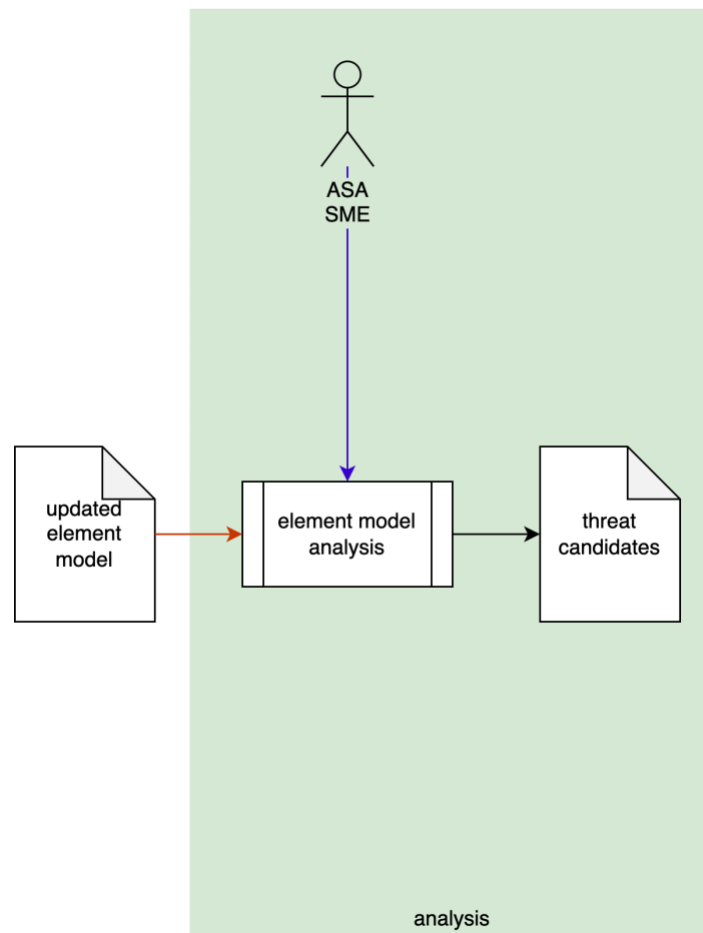
<b>Inputs</b>	As-implemented element documentation Element model
<b>Outputs</b>	Updated element model
<b>Participants</b>	Development SME ASA SME



The attack surface analysis (**ASA**) SME works with the development SME(s) to create an **updated element model** of the system. The **as-implemented element documentation** is used to update the model created in the design phase.

## Analysis

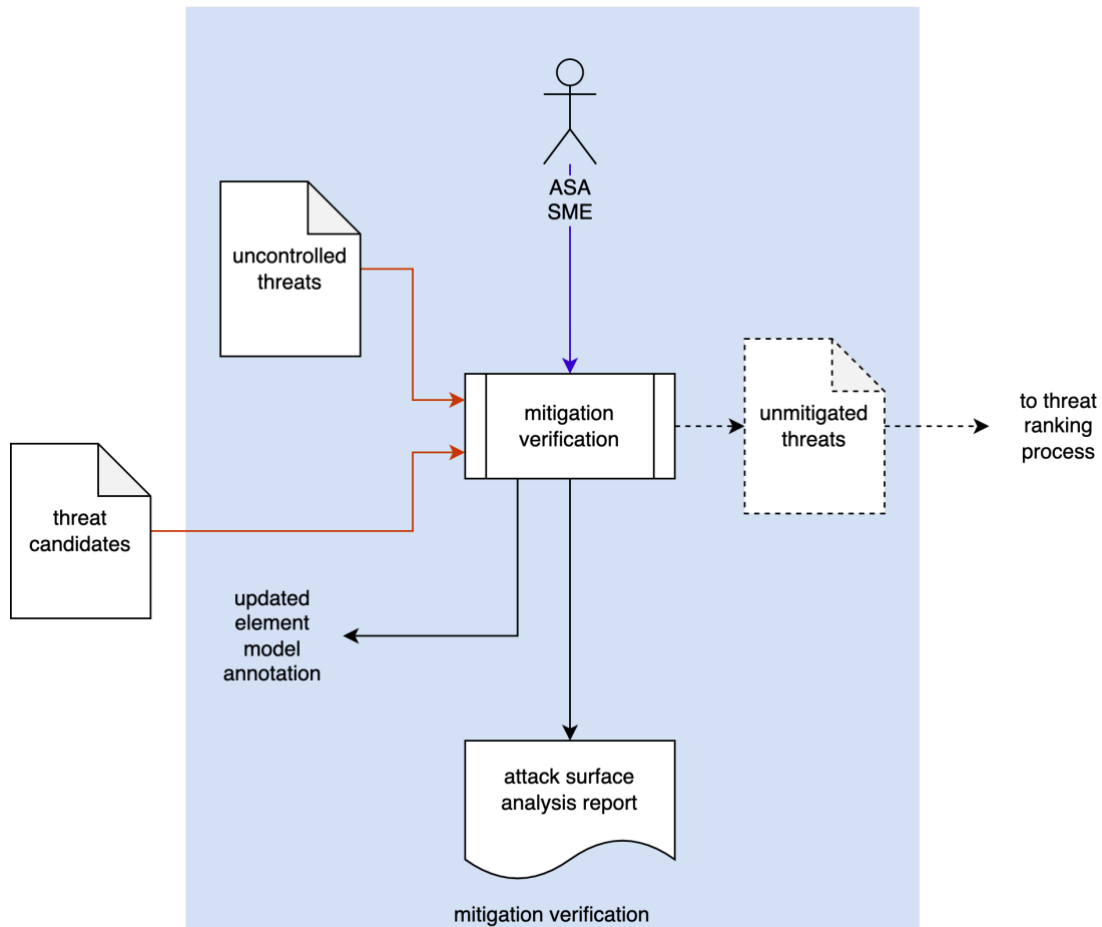
<b>Inputs</b>	Updated element model
<b>Outputs</b>	Threat candidates
<b>Participants</b>	ASA SME



The ASA SME takes the **updated element model** and performs a new analysis. This results in the creation of a list of **threat candidates**.

## Mitigation Verification

<b>Inputs</b>	Threat candidates Uncontrolled threats
<b>Outputs</b>	Unmitigated threats
<b>Participants</b>	ASA SME



The ASA SME takes the **threat candidates** and the previously established **uncontrolled threats** generated in the design phase and verifies that all uncontrolled threats have been mitigated. An **attack surface analysis report** is generated. The **updated element model** is annotated with the findings of the verification. If any uncontrolled threats remain, a list of **unmitigated threats** is generated and passed along to the threat ranking process (specified in the **Threat Prioritization Plan**).

# References

1. **Threat Prioritization Plan** (AVCDL secondary document)
2. **Attack Surface Analysis Report** (AVCDL secondary document)