APPENDIX B

Theory of Hardware Circuit

A. System Clock

U3a, U3b, and 3.58M Hz crystal produce 3.58MHz signal. This signal is sent to U2a pin 3 to produce 3.58MHz÷2 = 1.79MHz system clock.

B. Reset Signal

U2b is used to trim the Reset signal produced by power on or pressing [..] key. The trimmed $\overline{RST}$ is sent to CPU and CTC. RST is sent to the 8255.

C. Memory Addressing

MREQ	A15	A14	A13	A12	A11	A10 --- A0	Selected Chip	Address
0	0	0	0	0	X	X --- X	U6	0000-0FFF
0	0	0	1	0	X	X --- X	U7	2000-2FFF
0	0	0	0	1	1	X --- X	U8	1800-1FFF

U6 is the monitor for MPF-I, it may be a TMS2516, or an Intel 2716. U7 is a spare socket for future expansion usage, it may be a RAM or a ROM, Circuit design is default for 2716, 2516, 2532(EPROM) when user intends to plug in Intel 2732, or HM 6116(RAM), he should consult the note on Sheet 4 of the schematic. U8 is a system RAM, the memory size is 2K bytes.

D. Input/Output port addressing

U96 (74LS139) is an I/O port decoder.

IORQ	A7	A6	Selected I/O	Port Address
0	0	0	8255	00 - 03
0	0	1	CTC	40 - 43
0	1	0	PIO	80 - 83

Note; I/O port is not fully decoded, e.g. the 16 combinations 00 - 03, 04 - 07, 08 - 0B,.....3C - 3F, all select the s 8255. The CTC & PIO are also selected by 16 different combinations.

E. Matrix Keyboard and Display

U14 (8255) has 3 I/O ports, PB0-PB7 control individual segments in a display, U15 and U12 are segment drivers, PC0-PC5 select which display is to be activated, U13 (75492) is a 6-digit digit driver.

The LED display uses a Multiplexing method, only one is selected at a time, from right to left. Due to its rapid multiplexing rate. The displays appear to be on continuously.

Whenever the diaplays are accesed keyboard activity is also checked via U14 (8255) PA0-PA5. If no key is pressed, PA0-PA5 are high, when there is one key pressed, via keyboard scan routine the CPU will detect which key id pressed. In MPF-I there are 6 x 6 = 36 keys, but only 32 keys are checked through the key board matrix.

F. User-Key

The user-key is not assigned a function and is reserved for user's future use. The state of this key is detected via PA6 of 8255. via PA6 of 8255.

G. Audio Tape Interface.

The program or data to be stored in Magnetic Tape is serially sent out via PC7 of 8255. The filtering & decaying circuit are composed of C13, R11, C12, R12 and R13. This decayed signal is to MIC ("Microphone") inlet of Tape-recorder, Q2 drives an LED and speaker. PC7 is also used as the port for audio output.

A recorded file may be read back to the RAM from the ("Earphone") EAR outlet of Tape recorder. The input interface circuit is composed of R14, CR2, CR1 and C11. This circuit converts EAR inputed signal to TTL level signal and detected by CPU via PA7 of 8255.

H. Step, Break point and Monitor Break

PC6 is normally high. This signal send to R0 input of U4 (7490) will preset U4 output to 0000, and make NMI of Z-80 high. When PC reach Breakpoint or MPF-I execute single step, PC6 will output low, U4 starts counting, after 5th OP code fetch, NMI becomes low. This will interrupt program execution and jump back to monitor program.

Logic State of U4 (74LS90)

	R9	R0	Qa	Qd	Qc	Qb	NMI	Comment
Normal State	0	1	0	0	0	0	1	U4 preset to 0000
BREAK becomes low	0	0	0	0	0	0	1	R0=$\overline{\text{BREAK}}$=0
1St MI	0	0	0	0	0	1	1	7490 Start commting
2nd MI	0	0	0	0	1	0	1	Qd,Qc,Qb is Mod, 5
3rd MI	0	0	0	0	1	1	1	Counter
4th MI	0	0	0	1	0	0	1	
5th MI	0	0	1	0	0	0	0	Qa from 0-1 when Qd from 1-0
Pressing Key [MON]	1	0	1	1	0	0	0	U4 Preset to 1001

After [MON] key is pressed, R9 of U4 is high, Qa becomes high and NMI becomes Low. So CPU jump back to monitor program execution due to nonmaskable interrupt.

I. PIO and CTC

U11 (CTC) and U10 (PIO) are daisy-chained, CTC has the higher interrupt priority, CTC IEI, PIO IEO, CTC channel signals and PIO I/O port are reserved on P2 edge connector for user future expansion.