Design, Analysis and Experimental Validation of a CLLC Resonant Converter for Electric Vehicle (EV) battery charging applications

Submitted in partial fulfillment of the requirements for the degree of

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in

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by

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DECLARATION

I here by declare that the thesis entitled "**Design, Analysis and Experimental Validation of a CLLC resonant converter for Electric Vehicle (EV) battery charging applications**" submitted by me, for the award of the degree of *Bachelor of Technology in Electrical and Electronics Engineering* to VIT University is a record of bonafide work carried out by me under the supervision of **Dr. Arunkumar G**, Associate Professor Sr, School of Electrical Engineering, VIT University, Vellore.

I further declare that the work reported in this thesis has not been submitted and will not be submitted, either in part or in full, for the award of any other degree or diploma in this institute or any other institute or university.

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CERTIFICATE

This is to certify that the thesis entitled "**Design, Analysis and Experimental Validation of a CLLC resonant converter for Electric Vehicle (EV) battery charging applications**" submitted by **Kuldip Bag(21BEE0013)**, School of Electrical Engineering (SELECT), VIT, Vellore, for the award of the degree of *Bachelor of Technology in Electrical and Electronics Engineering* , is a record of bonafide work carried out by him under my supervision during the period 15/07/2027 to 11/05/2024 as per the VIT code of academic and research ethics.

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Head of the Department
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Place: Vellore

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Executive Summary

This project implements a CLLC resonant converter for Electric Vehicle (EV) battery charging applications. It addresses the absence of detailed hardware analysis by implementing a working, low-power hardware prototype with detailed operational analysis and parameter documentation. The input to the converter was provided by the Chroma Programmable DC Power Supply 62050H-600S, and the results were captured using the Keysight IntegraVision Power Analyzer PA2203A. The gate pulses for the MOSFET switches was provided using the WAVECT WCU300 controller. The simulation of the proposed converter was carried out on the PLECS software, and it is designed in the buck mode, with an input of $65V$ and an output of $48V$ to $60V$. The detailed design steps and considerations have also been duly mentioned in the concerned chapters. The measured efficiency during hardware validation has also been provided for better insights into the different types of losses that can occur during the prototyping stage. The project, thus, aims to further advance the EV battery charging infrastructure through the unexplored, but powerful potential of the CLLC resonant converters, and as a result lead to sustainability and reduction in the carbon footprints.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

In the transportation industry, electric vehicles (EVs) are becoming the market leader on a global scale. EVs are the driving force behind the transportation industry's transformation into the twenty-first century, countering the damaging effects of traditional internal combustion engine vehicles' (ICEVs) pollution. In addition to trying to clean up the environment, this transportation revolution has also sought to create jobs in a number of fields, such as EV and charger manufacturing, assembly, testing, quality assurance, validation, installation, and maintenance (Rajagopal 2023).
Globally, there is a swift shift from internal combustion engines (ICEVs) to electric vehicles (EVs) (Soman et al. 2020, King et al. 2024, Todorovic and Simic 2019, Tan et al. 2023). As a result, infrastructure for EV charging needs to be developed. While many electric vehicle (EV) users charge their vehicles at home, public charging stations should be established in order to lessen range anxiety, especially for long-distance driving (Funke et al. 2019). The main obstacle to EV adoption in India, according to some reports, is infrastructure (Gulzar et al. 2024). Public charging station installation serves as the infrastructure for EV charging.

1.1 Background

In recent years, we have witnessed the detrimental effects of fossil fuel emissions and carbon footprints, which are direct byproducts of internal combustion engines. A depletion of fossil fuel reserves has also been witnessed at an alarming rate. The severity of the effects has very well transcended the threshold and has metamorphosed into an earth-shattering phenomenon.
In light of this, major automobile manufacturers around the world are initiating a shift towards electric vehicles (EVs). The manufacturing of an EV demands the presence of dependable power converters, be it AC-to-DC converters or DC-to-DC converters, with enhanced efficiency. In accordance with the state-of-the art technologies, resonant converters turn out to be the optimal choice of most automobile manufacturers.
Resonant converters have received appreciation in several applications, especially in those cases where stringent requirements are present in terms of efficiency, electro-

magnetic compatibility (EMC), and power density. Among various different resonant converter topologies, CLLC converters have received a large amount of fame and appreciation for their unidirectional and bidirectional applicability. The reduced switching stress due to the incorporation of soft switching techniques is the key highlight of this converter.
This project addresses this pressing issue of pollution due to fossil fuel emissions by designing and experimentally validating a CLLC resonant converter, which can become an aid in forwarding Net-Zero and Carbon Neutrality initiatives.

1.2 Motivation

Dr. Yaron Ogen's research at Martin Luther University Halle-Wittenberg, Germany has found (Ogen 2020) that as of March 19, 2020, 4443 deaths in Italy, Spain, France, and Germany were due to COVID-19. The regions with a maximum NO_2 concentration above $100\mu mol/m^2$ had 83% (3701 cases), those with a maximum concentration between 50 and $100\mu mol/m^2$ had 15.5% (691 cases), and those with a maximum NO_2 concentration below $50\mu mol/m^2$ had only 1.5% (51 cases). One of the primary components of ICEV exhaust is NO_2 (US EPA 2016).
It can be inferred from this research, that the magnitude of COVID-19 pandemic aggravated the effects of pollution manifold times. Thus a faster transition from internal combustion engines to EVs is the need of the day. However, the transition is viable, if and only if the efficiency of the power converters that power the EVs is significantly high, and the longevity of the converters should be long enough to sustain the market competitions.
Thus, in the light of these parameters, the design and detailed analysis of such converters are imperative. CLLC resonant converters provides a sustainable solution to this, through its following inherent properties :

- High power efficiency due to soft switching techniques.
- Lower Electromagnetic Interference and higher Electromagnetic Compatibility.
- Higher converter reliability due to reduced switch stress.

However, in accordance with the literature review, it can be concluded that the popular research has been centered around the theoretical modelling and simulation of CLLC converters, and the hardware implementation of such converters has not been explored that much. A sincere hardware prototype provides enlightening insights into the real world operation of such converters, and can also be used to assess and mitigate the operational faults and issues faced during converter operation. The motivation of this work is to provide a detailed design and analysis of the operational modes, and to finally develop a working hardware prototype for experimental validation.

1.3 Objective

This work aims to provide a comprehensive design and detailed analysis of a CLLC resonant converter, and to develop a working hardware prototype to validate the simulation results.

1.4 Methodology

The design workflow of resonant converters demands detailed and precise calculations, as the attainment of resonance, which is the necessary requirement for soft switching, is completely dependent on the component values. As a precursor to numerical calculations, an in-depth literature review was conducted and an effort was made to understand the modes of operation for a CLLC resonant converter through the various thesis papers and research articles available on the internet.

Further, a rigorous effort was made to numerically calculate the component values through the use of the dynamic volt-sec balance equations. The calculated parameters were utilized to create a simulation model of the topology on PLECS software, wherein the soft switching of the switches and the necessary output and input parameters were checked and compared against the theoretical values.

With the attainment of satisfactory simulation results, a hardware prototype was planned. The component parameters used for the hardware implementation were at least 1.25times the simulation values. The components were carefully selected based on those available on the laboratory test bench. The connections were made in accordance with the circuit diagram of the proposed converter, and upon its completion, the hardware results were documented.

CHAPTER 2

LITERATURE REVIEW

2.1 Literature Review

Khalid et al. (2022) have reviewed the various charging topologies and methodologies for EV battery charging. Non-isolated and isolated DC-DC converter topologies, along with AC-DC converter topologies have been reviewed. In addition, several charging methods and algorithms have been detailed with their advantages and limitations. Specific to simultaneous charging, multi-port converters have been described. The authors have touched on the possibility of integrating multiple sources as a part of a multi-input multi-output (MIMO) converter to charge multiple batteries simultaneously using multi-winding transformer isolation. The merits of MIMO converters have been described to be low ripples, high voltage gain, and V2G and G2V capabilities, while its disadvantages are mentioned to be on synchronization of converters and high sensitivity to changes in duty cycle.

Deshmukh et al. (2022) have reviewed the various resonant converter topologies and control strategies for EV applications. Numerous topologies of resonant converters with the different combination of the resonant elements are described in detail with the advantages and limitations. Specifically, the LLC converter and its equivalent circuit have been described, along with the modulation strategies of various resonant topologies. An exhaustive comparison of the existing topologies is provided and the future of EV charging with resonant converters is described.

Shankar and Arunkumar (2024) have proposed a solar PV-fed H6 topology-based CLLC resonant converter for charging multiple EV batteries of equal and unequal voltage ratings as applicable to battery swapping station. The authors have described the modes of operation of the proposed converter for charging two batteries using two separate high-frequency transformers, so that both the batteries have isolated grounds. The characteristics of the resonance system and the detailed design and modeling of the converter are provided in the work. Simulation and $100W$ hardware prototype results to charge two equal ($36V$) and unequal ($24V$ and $36V$) batteries have been provided

to validate the topology for the EV battery application. An efficiency of 80% has been obtained with the implementation with discrete components in the hardware prototype.

Qayamuddin et al. (2023) have have proposed a logic circuit-based new control strategy for controlling DAB converter for EV battery charging applications. The proposed DAB-based converter employs twelve MOSFETs, two capacitors, and one high-frequency transformer (HFT) to charge one battery. The authors have clearly identified the charging algorithm for grid-to-vehicle (G2V) and vehicle-to-grid (V2G) modes, and is given below:

- In both G2V and V2G modes, if the battery state of charge (SOC) is less than 20%, the battery is charged.
- In G2V mode, if the battery SOC is between 20% and 80%, the battery is charged.
- In V2G mode, if the battery SOC is between 20% and 80%, the battery is allowed to discharge.
- In both G2V and V2G modes, if the battery state of charge (SOC) is greater than 80%, the battery is allowed to discharge.

The authors have provided design calculations and the simulation results, considering the Indian standard AC supply as the input to charge a $50V$, $100Ah$, $5kW$peak, Li-ion battery. The highlights of the work include simple control that can be easily implemented, detailed analysis of charging and discharging control during V2G and G2V modes, and focus on charging at homes. On the other hand, it is seen that the capacitance of both DC-link capacitors is very high, which increases the size and weight of the system. In addition, hardware implementation could involve several challenges which is beyond the scope of the work. Furthermore, any hard-switching will result in higher losses, since resonance has not been introduced in the topology considered in the work.

Krishnan Nair et al. (2021) have proposed a bidirectional soft-switched DC-DC converter for battery charging application. The proposed converter uses nine switches, two diodes, one inductor, and four capacitors. The uniqueness of the work is the inclusion of active and passive snubbers at LV and HV sides, respectively. While the converter is a buck-boost converter, it can perform boost action in the forward mode and buck action in the reverse mode. Another advantage of the work is the soft-switching of several switches, leading to reduced losses. The proposed system also incorporates solar photovoltaic (SPV) array, which makes it much suitable even for grid-independent systems. The authors have modeled the various components of the circuit, and have also included the EV load demand model. Three scenarios have been simulated considering

various states of SOC and SPV system voltage. The switch stress is seen to reduce due to the inclusion of snubber, resulting in an increased efficiency. While the proposed system has several of the aforementioned advantages, its validation in hardware is beyond the scope of the work. Several limitations in hardware implementation needs to be considered during prototyping and implementation, and these issues need special focus.

Shi et al. (2024) have proposed a new control strategy for on-board chargers which use CLLC converter. The authors have considered a single-phase power factor correction (PFC) circuit which is supplied from a $220V$ AC grid. The input voltage to the CLLC (output of PFC) has a range of 340 to $430V$, considering a 10% variation in the AC supply. The battery voltage varies between 225 and $450V$, implying the possibility of both buck and boost modes. The details of the various operational modes have been provided with the corresponding equations. The analysis of voltage gain, soft-switching, and design has been provided. The control strategy has been experimentally validated with silicon MOSFETs at a resonant frequency of $102kHz$. The advantages of the system include ease of implementation, simple control, and ability to work in both buck and boost modes. On the other hand, only one battery is considered by the authors, and the control complexity might increase with multi-battery charging.

Alatai et al. (2024) have focused on modeling of the proposed five-level LLC converter to charge one EV battery. The design considerations and the PI-controller-based control strategy are detailed to suit the CC-CV charging algorithm. A $200V$ supply is used to charge a $48V$ lead-acid battery. Experimental validation of zero voltage switching (ZVS) and zero current switching (ZCS) have been provided, along with the waveforms related to transition from constant current (CC) to constant voltage (CV) modes. A thorough comparison of the proposed work with several existing works has been provided to highlight the novelty of the proposed system. The control is simple and easy to implement. However, the implementation in the work is limited to charging one battery.

Zanatta et al. (2023) have proposed a two-stage DC-DC converter employing a CLLC converter with a two-secondary HFTs. The two outputs are interleaved and connected to a synchronous buck converter to charge the EV battery load. An exhaustive comparison of various literature has been provided to clarify the research gap. The research paper presents a two-stage CLLC converter: the first stage ensures isolation and fixed conversion ratios, while the second stage effectively regulates the output voltage across a wide range of battery voltages. The authors have provided the results for a $10kW$ prototype supplied from an $800V$ input and an output range of $250V$ to $500V$. The prototype uses Silicon Carbide (SiC) and Gallium-Nitride (GaN) devices. The experimental results highlight exceptional performance, with the efficiency over 98% at

an input of $500V$ while transferring a power of $7kW$. However, a notable shortcoming is the lack of consideration for boost operation in the paper. Despite this limitation, the converter module demonstrates promising results in terms of both simulation and experimental validation.

Zhang et al. (2023) have proposed a CLLC converter designed for the three-stage charging of lithium-ion batteries in electric vehicles (EVs). The fully symmetrical converter demonstrates increased efficiency during charging, validated by a $1.2kW$ experimental prototype. The paper provides a comprehensive review of the converter's relevance to bidirectional on-board chargers in the context of global carbon goals. Notable features include detailed design, small-signal models, closed-loop pulse-frequency modulation (PFM) control, and a novel planar transformer design with an integrated resonant inductor. The proposed approach involves charging of a battery with a $250-450V$ range from a $400V$ input at a power of $1.2kW$ with the tank resonant frequency of $500kHz$. Experimental results confirm the converter's 96% efficiency, making a significant contribution to the field of bidirectional on-board chargers for EVs. On the other hand, the limitation is its application being limited to buck mode operation.

A wireless power transfer (WPT) system that integrates a bidirectional DC-DC CLLC converter using an innovative sandwiched coil set, with enhanced coupling factor, misalignment tolerance, and overall compact size has been proposed by Liao et al. (2020). The WPT system used Litz wires, the simulation of which has been provided considering a frequency of $110kHz$. The digitally controlled CLLC converter showcases efficient bidirectional power flow, achieving 96% efficiency during charging and 93.8% efficiency during discharging at the three-fourth of the rated load. Its versatile functionality includes the capability to provide $200V$ to $48V$, $500W$ charging and discharging functions, incorporating CC-CV modes and fast-response current control. Similar to the other works discussed in this section, this work also focuses only on buck operation of the CLLC converter.

Min and Ordonez (2020) have proposed bidirectional CLLC resonant converter with an innovative tank design for efficient power transfer. Asymmetrical adjustments in secondary components cater to charging and discharging modes, enhancing operational efficiency. The paper discusses control techniques like time-domain models and synchronous rectification for optimization. Performance analysis shows improved efficiency and reduced switching frequency variations across a wide battery voltage range. However, challenges are acknowledged in implementing complex asymmetric designs practically. The tested prototype operates successfully in battery voltage ranges of $250-450V$, stabilizing the DC bus voltage at $400V$. This research provides insights

into advanced bidirectional resonant converter designs, noting practical challenges associated with asymmetry.

Zhang et al. (2020) have proposed a two-transformer interleaved CLLC converter. The design capitalizes on wide band gap (WBG) technology and incorporates a planar transformer with low stray capacitance. By introducing a matrix transformer, the configuration further minimizes inter-winding capacitance, achieving an impressive 75% reduction in stray capacitance. The proposed design attains a peak efficiency of 97.85% and a remarkable power density of $114W/in^3$ in a $6.6 - kW$ prototype in which the power devices are switching at $500kHz$. However, the use of advanced technologies and specialized components may contribute to a higher overall cost for implementing this converter, especially in the automotive industry where cost-effectiveness and affordability are crucial factors. In addition, the work focuses on charging a single battery, for which 12 switches are employed. It is also important to note that the efficiency gains heavily rely on the strategic utilization of WBG semiconductors.

Jo et al. (2024) have focused the work on wide output voltage application and have provided the detailed design Methodology for CLLC bidirectional converter with dual resonant frequencies. The structure incorporates dual resonant frequencies for constant current and constant voltage, ensuring load-independent output characteristics. Validation through a $3.6kW$ experimental prototype reveals a 3.13% efficiency improvement under light load conditions. In CC charging, CV charging, and discharging modes, the highest efficiencies of the proposed design were 98.04%, 97.84%, and 98.05%, respectively. However, the dual resonant frequency approach may introduce complexity in implementation and prove sensitive to component variations, potentially impacting consistent efficiency. The proposed structure, while novel and efficient, is only limited to single load in buck mode ($400V$ input to $250 - 450V$ output).

Zhao et al. (2022) have introduced a novel methodology grounded in parameter equivalence and a time-domain model, by implementing various control techniques such as variable frequency control, sensor-less synchronous rectification algorithm with combined phase shift modulation, among other techniques. Utilizing parameter optimization, the design achieves bidirectional voltage gain and zero-voltage switching within a predetermined frequency range. Experimental validation using a $1kW$ prototype highlights the converter's efficiency and feasibility in accommodating wide voltage ranges. The shortcoming of this literature is that it offers limited insights into specific control techniques employed in similar designs.

Chen, Sun, Shi, Ha and Lee (2021) have implemented a novel synchronous rectifi-

cation (SR) battery charging principle for CLLC converters. The conduction losses on the secondary side are reduced by this method, leading to higher efficiencies. Its applications include uninterrupted power supply (UPS) systems, DC distribution systems, V2G systems, battery energy storage (BES) systems, electric aircrafts, and reversible solid oxide fuel cell systems. The proposed control provides robust and flexible control, and is well suited for battery charging. However, SR has limitations such as current-based SR methods are not suitable for high-frequency applications, and voltage-based SR methods are limited by the withstand voltage of sensor chip. This work also considers one battery load.

Chen, Sun, Lu, Wang and Ouyang (2021) have proposed a PI-based novel current control method for battery charging circuit that uses a CLLC converter. State trajectory model is employed to analyze the transients in the resonant tank, and the corresponding design is provided. Phase shift control was applied, and combined hybrid control was proposed to improve the dynamic performance of the converter with a tight output voltage regulation. Hardware implementation has been used to validate the proposed control. The dynamic performance analysis details are limited in the work, and only considers single battery load.

Mungekar and Mallik (2024) have proposed a C3L3 converter with a single primary bridge and two isolated outputs. The work details a novel improved generalized harmonic approximation (iGHA) model of the proposed C3L3 converter. The authors have described the conventional first harmonic approximation model and its disadvantages, and derived a GHA and iGHA based model. The model has been simulated to verify the proposed model. Further, calculation of losses is detailed with the proposed modeling approach, and the loss optimization methodology has been provided. The control strategy is detailed and the corresponding experimental results are discussed in the work. The work is an excellent reference on multiple aspects of CLLC converters, with specific focus on modeling and control. Since MOSFETs are used on both primary and secondary, all the 12 MOSFETs are to be controlled precisely. Although this gives better control, the control is very complex. If diodes are used on the secondary side, a single primary bridge will not be sufficient to provide different outputs. In such a case, two MOSFET bridges will be required on the primary side (as proposed in this work), where only 8 MOSFETs need to be controlled. Although the control will not be as flexible as that in Mungekar and Mallik (2024), the control of 8 MOSFETs will be relatively less complex.

Other works that use resonant converters include the research by Tran et al. (2015) where multi-secondary transformer based CLLC converter is proposed, by Okon et al.

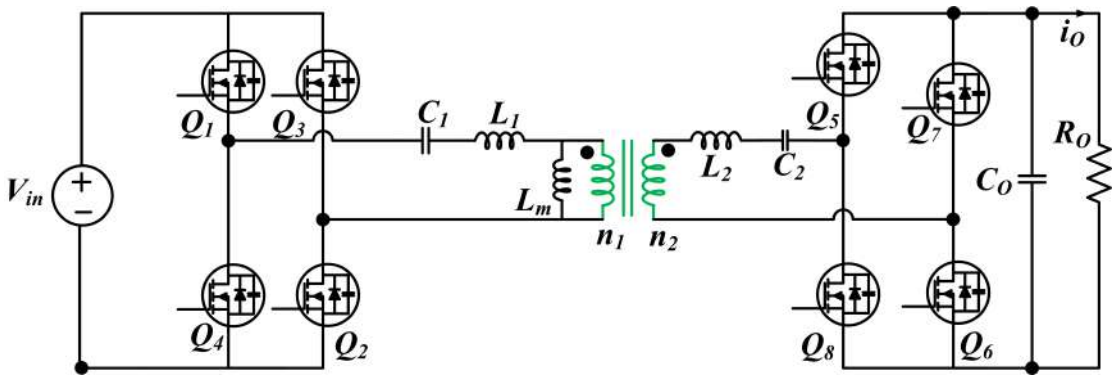


Fig. 2.1 Circuit of the Proposed Converter

(2021), Li et al. (2018) and Mishra et al. (2021), where CLLC and DAB-CLLC combination topology is proposed for battery charging. Okon et al. have proposed a CLLC based charging circuit to charge one battery, while Li et al. have proposed voltage divider with two DABs to charge three batteries, two of which have a common node. Mishra et al. have proposed a DAB-CLLC combination circuit to charge two batteries, where CLLC is proposed for fast charging and DAB is proposed for slow charging.

2.2 Research Gap

In accordance with the literature review, it can be inferred that the state-of-the-art researches that have been conducted provided deeper insights into the theoretical simulation, while keeping the dimension of hardware prototyping relatively unexplored. An absence of significant insights into the operational modes and the efficiency under real-world working conditions was also observed. Hence, this research work aims to navigate this relatively unexplored spectrum of CLLC resonant converter design, and as a result, provide deeper insights into its hardware prototyping and efficiency.

2.3 Proposed Solution

The scope of this research work is to provide a detailed design, topological analysis and hardware validation of a CLLC resonant converter in the Buck mode of operation. The proposed topology has been represented in the Figure2.1. The input voltage rating of the proposed converter is $65V$, while the output provided is $48V$, which is meant for charging Electric vehicle (EV) batteries.

CHAPTER 3

OPERATION OF THE PROPOSED CONVERTER

The CLLC resonant converter operation can be described in eight modes of operation. Based on the power flow direction and current direction, each of the eight modes can be classified under one of the following sub-modes for the proposed converter: the forward power transfer mode (FPTM), the parasitic power flow mode (PPFM), and the zero power transfer mode (ZPTM). In the FPTMs, power is transferred from the source to the load. On the other hand, no power is transferred from the source to load in the ZPTMs. However, the load is supplied from the output capacitors during ZPTMs. The PPFMs indicate that power flows between the four the primary parasitic capacitors of the primary switches. The eight operational modes are explained in detail in this chapter.

3.1 Mode 1 : Forward Power Transfer Mode-A (FPTM-A)

During mode 1 (or) FPTM-A as presented in the Figure 3.1, the switches Q_1 and Q_2 are turned on, by calibrating their gating signals to the high state. The resonant current, i_1, has a sinusoidal increase while the magnetising current (i_m) through the magnetising inductance (L_m) increases linearly. The polarities across the transformer windings on

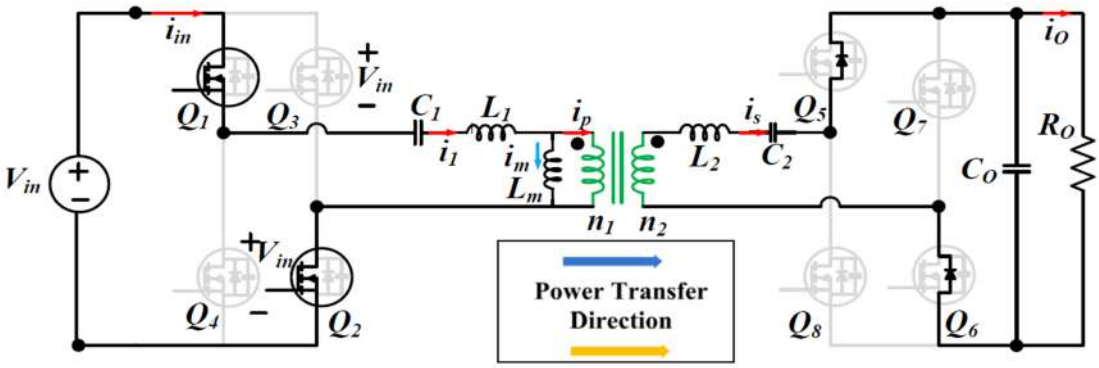


Fig. 3.1 Mode 1 : Forward Power Transfer Mode - A (FPTM-A)

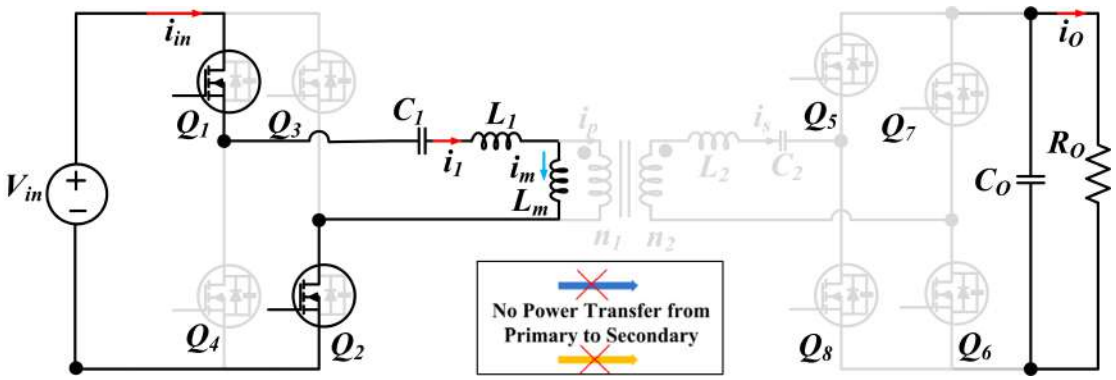


Fig. 3.2 Mode 2 : Zero Power Transfer Mode-A (ZPTM-A)

both the primary and the secondary sides are same since the alternating current on the two sides of the transformer, are in-phase. Consequently, the voltage across the transformer secondary winding forward biases the anti-parallel diodes of the switches Q_5 and Q_6. The AC power transferred through the transformer is rectified through the rectifier bridge, and the DC power thus obtained is transferred to the battery for charging it. In this case, power is transferred from the primary to the secondary side. Current i_m is less then i_1 in this mode of operation, and this mode ends when i_m becomes equal to i_1.

3.2 Mode 2 : Zero Power Transfer Mode-A (ZPTM-A)

During the Mode 2 (or) ZPTM-A mode of operation, as portrayed in Figure 3.2, i_m reaches the value of i_1, and hence no power is transferred from the primary to the secondary side of the resonant bridge. The entirety of i_1 flows through the magnetising inductance L_m. In this stage, the magnetising inductance L_m also participates in the resonance. The secondary diodes are turned off, as no current flows through them. The output capacitor C_0 discharges and supplies the output current i_0.

3.3 Mode 3 : Parasitic Power Flow Mode-A (PPFM-A)

During the Mode 3 (or) PPFM-A mode of operation, as shown in Figure 3.3, all the switches on the primary side (Q_1 to Q_4) are in the off state. This time period is also known as the dead time interval. The direction of the resonant current i_1 through the primary side of the circuit, is synonymous to that in ZPTM-A. As a result, i_1 charges the parasitic capacitance of switches Q_1 and Q_2, while discharging the parasitic capacitance of Q_3 and Q_4, so that those switches can be turned on during the next cycle in the ZVS condition. During this stage, no power is transferred from the primary to the secondary side, and the output capacitor C_0 discharges to provide the output current i_0.

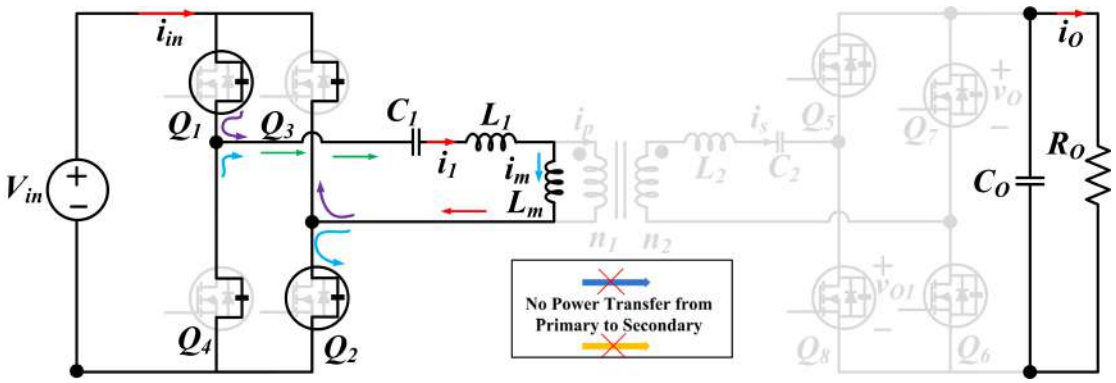


Fig. 3.3 Mode 3 : Parasitic Power Flow Mode-A (PPFM-A)

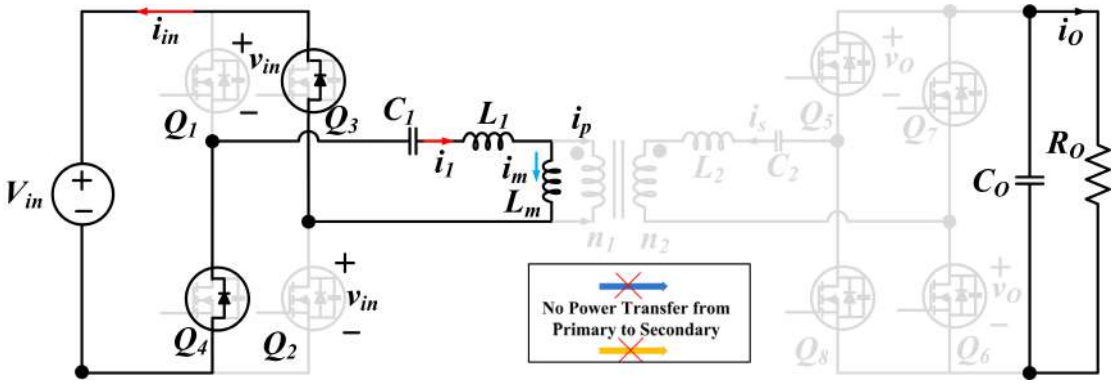


Fig. 3.4 Mode 4 : Zero Power Transfer Mode-B (ZPTM-B)

3.4 Mode 4 : Zero Power Transfer Mode-B (ZPTM-B)

During the Mode 4 (or) ZPTM-B mode of operation of the proposed converter, as showcased in Figure 3.4, the parasitic capacitance of switches Q_3 and Q_4 have completely been discharged. The resonant current, i_1 still circulates through the primary side of the circuit, and thus requires a path to flow, however in the opposite direction or the negative direction. Hence, the resonant current flows through the anti-parallel diode of switches Q_3 and Q_4, since only those diodes become forward biased under the influence of i_1 which flows in the negative direction. As a result of this, the switches, Q_3 and Q_4, can be turned on under the ZVS condition, during the next mode of operation. Similar to the last two modes, there is no power transfer from the primary to the secondary side, and the output capacitor, C_0 discharges to provide the output current, i_0.

3.5 Mode 5 : Forward Power Transfer Mode-B (FPTM-B)

During the Mode 5 (or) FPTM-B mode of operation, as portrayed in Figure 3.5, the gating signals of the switches Q_3 and Q_4 are high, and hence, these switches are turned on. The anti-parallel diodes of the secondary side switches, Q_3 and Q_4 becomes forward biased, and thus are involved in the conduction of the output current, i_0, through the

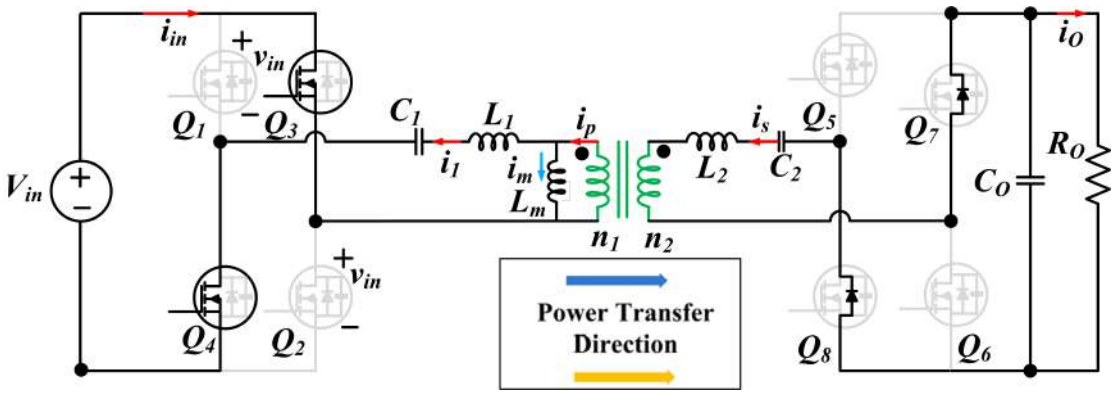


Fig. 3.5 Mode 5 : Forward Power Transfer Mode-B (FPTM-B)

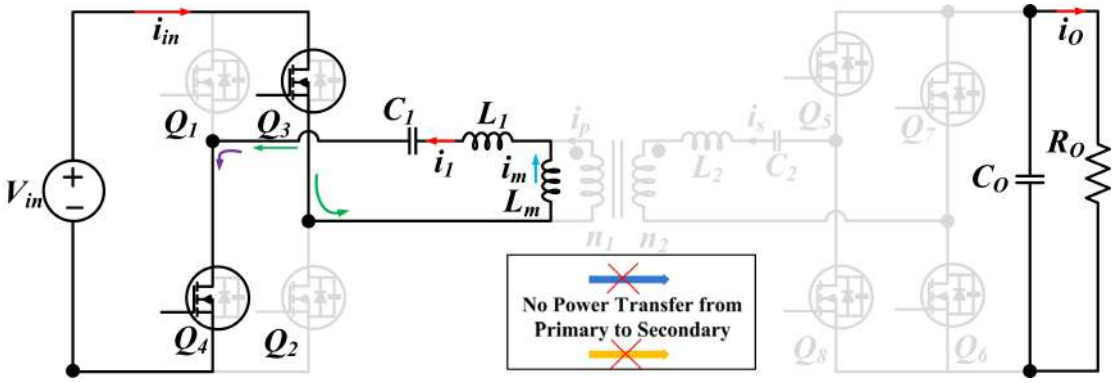


Fig. 3.6 Mode 6 : Zero Power Transfer Mode-C (ZPTM-C)

battery. The resonant current, i_1, increases sinusoidally, in a direction which is opposite to that of the resonant current in FPTM-A. In this mode, power is transferred from the primary to the secondary side of the converter circuit.

3.6 Mode 6 : Zero Power Transfer Mode-C (ZPTM-C)

During the Mode 6 (or) ZPTM-C mode of operation of the proposed converter, as presented in the Figure 3.6, the switches, Q_3 and Q_4 are on, whereas the switches Q_1 and Q_2 are turned off. The magnetising current, i_m becomes equal in magnitude to that of the resonant current, i_1. As a result, all of i_1 flows through the magnetising inductance, and therefore, no power is transferred from the primary to the secondary side. The output capacitor, C_0 discharges, and the current, i_0 flows through the load, R_0, thereby charging the battery.

3.7 Mode 7 : Parasitic Power Flow Mode-B (PPFM-B)

During the Mode 7 (or) PPFM-B mode of operation, as shown in the Figure 3.7, the switches Q_3 and Q_4 are turned off. This operation is similar to the operation of the converter in mode 3, the only difference is that, the direction of resonant current, i_1

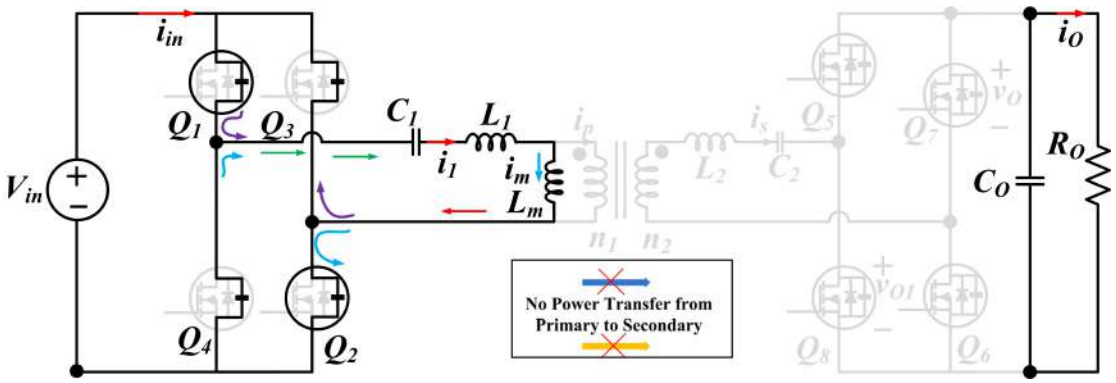


Fig. 3.7 Mode 7 : Parasitic Power Flow Mode-B (PPFM-B)

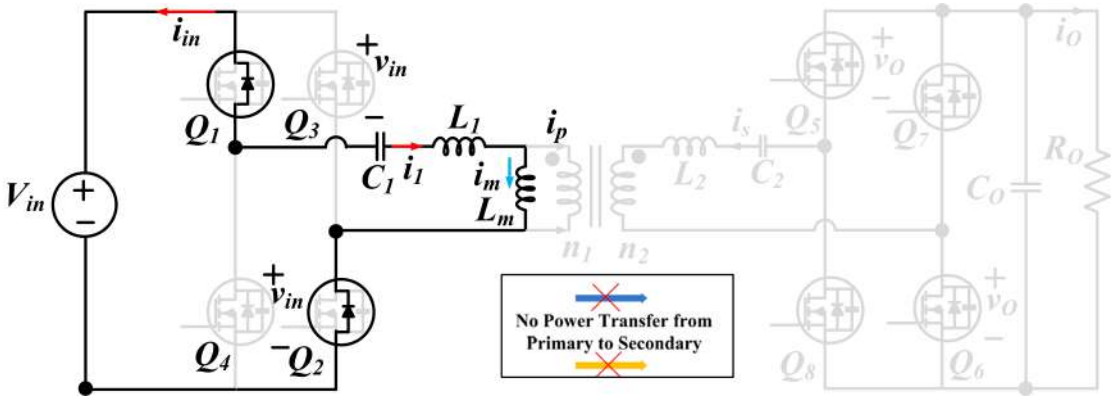


Fig. 3.8 Mode 8 : Forward Power Transfer Mode-D (FPTM-D)

is opposite to that in PPFM-A, that is, in the negative direction. The resonant current on the primary side continues to flow, and its direction is such that it charges the parasitic capacitance of switches Q_3 and Q_4, while discharging the parasitic capacitance of switches Q_1 and Q_2. This will enable these switches to turn on under the ZVS condition during the next stage of operation. During this stage, no power is transferred from the primary to the secondary side. The output current, i_0 is provided by the discharging output capacitor, C_0.

3.8 Mode 8 : Forward Power Transfer Mode-D (FPTM-D)

During the Mode 8 (or) FPTM-D mode of operation, as portrayed in the Figure 3.8, the anti-parallel diodes of the switches Q_1 and Q_2 starts to conduct, and this begins only when their respective parasitic capacitance have been completely discharged. The resonant current, i_1 circulating on the primary side is still in the negative direction, and therefore, the anti-parallel diodes of the switches, Q_1 and Q_2 conduct, thereby ensuring, that these switches are turned on under the ZVS condition. On the secondary side, the anti-parallel diodes of the switches, Q_5 and Q_6 participate in the conduction process, and hence, there is power transfer from the primary to the secondary side.

CHAPTER 4

DESIGN OF THE PROPOSED CONVERTER

The design of the CLLC resonant converter involves the following parts : (a) the design of the resonant tank elements, (b) the maximum value of the magnetising inductance, and (c) the selection of the appropriate transformer turns ratio, MOSFETs and diodes. Before designing the CLLC resonant converter, the following points are noteworthy (Zahid 2015) :

- The size of memory elements in inversely proportional to the switching frequency. Therefore, a high switching frequency implies reduced size of memory elements. High frequency also leads to a reduction in the switching stress of the capacitors.
- Hard switching at high switching frequencies leads to increased switching losses and reduced efficiency. Therefore, the design has to ensure ZVS operation on the primary sides, and soft switching commutation on the secondary sides to achieve higher efficiency at high switching frequencies.
- The resonant tank should draw nearly zero reactive power. In other words, the phase angle between the resonant tank input voltage and current should be as low as possible.
- The design should ensure reduction of voltage from $65V$ to $48-60V$ for the buck section by operating in the proper region.

4.1 Voltage gain calculation and choice of switching frequency

The voltage gain of the converter is calculated using equation (4.1). This gain also decides the transformer turns ratio.

$$Gain = \frac{V_{O,nominal}}{V_{in}} \tag{4.1}$$

The switching frequency depends on the device used, the driver IC, and the region of operation (in the gain curve). Higher switching frequency reduces the size of the magnetics.

4.2 Selection of Transformer Turns Ratio and Magnetizing Inductance

The turns ratio is represented using equation (4.2) for ideal converter.

$$n_{buck} = \frac{n_1}{n_2} \tag{4.2}$$

To ensure ZVS in the primary switches, it is necessary to keep their currents negative at the instant of turn-on. The current in each primary switch should charge and discharge the respective parasitic capacitor during the dead-time interval. The magnitude of this current depends on the magnetizing inductance. Therefore, ZVS depends on L_m, switch parasitic capacitance (C_{OSS}), switching frequency (f_{SW}), and dead-time duration (t_{dead}). The magnetizing inductance is calculated using equation (4.3).

$$L_m \leq \frac{\frac{1}{f_{sw}} \times t_{dead}}{16 \times C_{OSS}} \tag{4.3}$$

To ensure ZVS in the primary switches, the magnetizing inductance should be less than the calculated L_m. The choice of appropriate magnetizing inductance is a function on two factors (Zahid 2015):

- Magnetizing current: A low value of L_m lead to higher magnetizing current, leading to increased conduction losses, increased apparent power requirement of switches, and increased peak voltage requirement of primary capacitors. A large value of L_m results in lesser magnetizing current which limits the converter voltage gain.
- Dead time: Large dead time is necessary to achieve ZVS for wide input and output voltage range. This also allows us to increase the L_m. However, the RMS current in the primary will increase as a result.

4.3 Calculation of Resonant Inductance

In order to calculate the leakage inductance L_1, we assume an inductance ratio L_n defined by the following equation :

$$L_n = \frac{L_m}{L_1} \tag{4.4}$$

The inductance ratio directly affects the voltage gain of the converter and the switching frequency (Zahid 2015). A small value of L_n will reduce the switching frequency range. However, it will results in large leakage inductance which in turn results in increased size of inductors. On the other hand, large value of L_n limits the gain of the converter. After this choice, the secondary inductance L_2 is calculated using equation

(4.5) assuming a symmetric tank.

$$L_2 = \frac{L_1}{n_{buck}^2} \tag{4.5}$$

4.4 Calculation of Resonant Capacitance

The design of the capacitance of the capacitor in the primary side of the HFT depends on the operating frequency, since f_{sw} directly affects the efficiency. The value of capacitance of the primary resonant capacitors is calculated using equation (4.6).

$$C_1 = \frac{1}{L_1(2\pi f_{res})^2} \tag{4.6}$$

Then, the capacitance ratio (C_n) is decided, and the secondary capacitance of the symmetric bridge is calculated using equation (4.7).

$$C_2 = n_{buck}^2 C_1 C_n \tag{4.7}$$

4.5 Gain Curves

The attainment of resonance during the operation of the converter, pertaining to real-world conditions, depends heavily on the quality factor. Hence it is imperative, that a cohesive effort must be made in order to precisely ascertain it. For the different values of quality factor, the gain as a function of nominal frequency was plotted in MATLAB. Similarly, the gain is also a function of the load resistance, Hence, the variation of gain for different nominal frequencies, for various load resistances were also plotted in MATLAB. Both the gain curves have been represented in Figures 4.1 and 4.2.

4.6 Design Calculations

The gain for the buck mode will be 0.83, while considering a nominal voltage of $54V$. A transformer with a $1:1$ turns ratio was selected for the Buck mode of operation, in accordance with the available test bench in the laboratory. The input voltage is $65V$ DC and the nominal battery voltage is $54V$. The power drawn by the load is considered to be $125W$. The primary side resonant frequency was selected to be $100kHz$. The switch chosen for the bridge circuits is the CoolSiC AIMW120R045M1 Infineon SiC MOSFET rated $1200V$, $52A$. From the datasheet, its drain-source parasitic capacitance is found to be $107pF$. For a frequency of $100kHz$, the time per cycle will be $10\mu s$. This implies that one cycle of the DC ripple has a time period of $10\mu s$. For selecting the dead time, we consider 1% of this time, and therefore the dead time will be $100ns$. The corresponding maximum value of magnetizing inductance was calculated

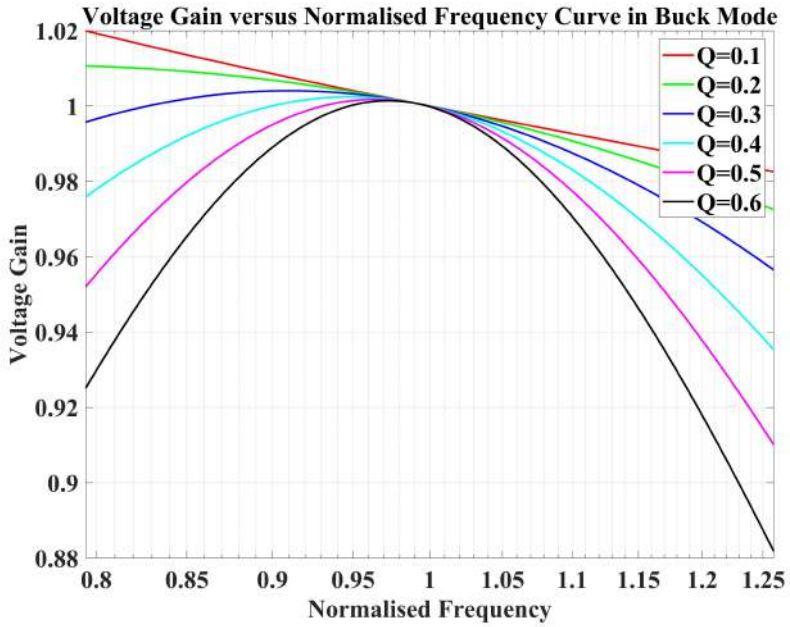


Fig. 4.1 Gain as a function of normalised frequency for various values of Quality (Q) factors

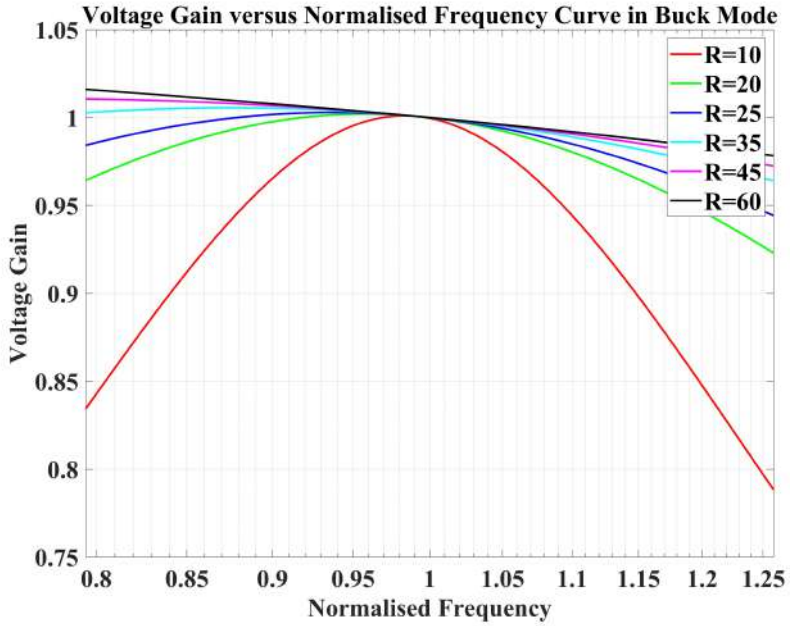


Fig. 4.2 Gain as a function of normalised frequency for various values of Load resistances

Table 4.1 Design Specifications of the Proposed CLLC Resonant Converter

Parameter	**Specifications**
Input Voltage	$65V$
Output Voltage	$48V$ to $65V$
Nominal gain for $54V$	0.8307
Turns ratio	$1:1$
Primary Inductor, L_1	$23.33\mu H$
Secondary Inductor, L_2	$23.33\mu H$
Primary Capacitor, C_1	$109nF$
Secondary Capacitor, C_2	$109nF$
Magnetising Inductance, L_m	$232.8uH$
Switching frequency	$111.284kHz$

using equation (4.3) to obtain $584\mu H$. Thus, ZVS can be maintained if the HFT has a magnetizing inductance of $584\mu F$ or lesser. For the transformer considered for buck mode, the magnetizing inductance were measured to be $232.8\mu H$. Since these magnetizing inductance are well below the maximum magnetizing inductance, ZVS will be ensured in the primary bridge switches. With a normalized inductance of 10 and a normalized switching frequency of 1, the primary resonant inductance and capacitance were calculated to be $23.33\mu H$ and $109nF$, respectively, while those of the secondary were equal to those in the primary due to the unity turns ratio. Based on the available inductance and capacitance, the primary resonant frequency was recalculated and obtained to be $111284.2504Hz$. The specifications of the various components, utilized in the converter have been mentioned and presented in the Table 4.1.

CHAPTER 5

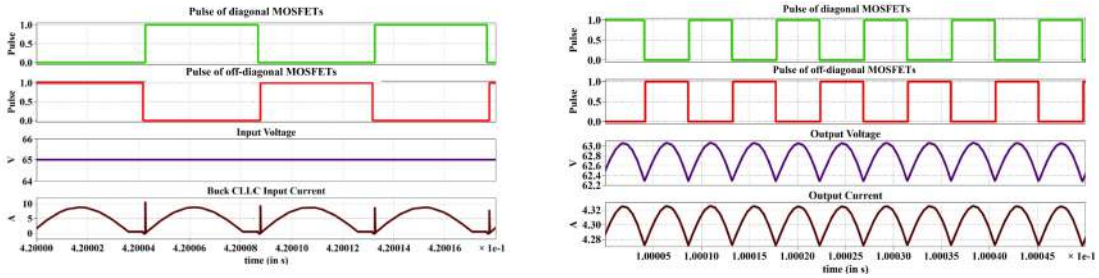
RESULTS

5.1 Simulation Results

The simulation of the proposed CLLC resonant converter was conducted on the PLECS software. The corresponding steady-state results of the simulation setup has been provided for a clearer comprehension and hence to provide better, concise and streamlined insights. For the sole purpose of simulation, lumped inductance and capacitance was used in the PLECS software. A transformer with the calculated turns ratio and magnetising inductance value was also utilized from the PLECS library.
The Figure 5.1a depicts the input side voltage and current levels. The input voltage is maintained at a constant DC voltage level, as a DC source was utilized for the simulation. It can be deduced from the current waveform that it always remains positive. The absence of any negative values ensure proper operation of the switches and hence the converter.
The output end voltage and current waveforms have been provided in the Figure 5.1b. The operation of the converter in the Buck mode is suggestive of the fact that the output voltage level is lesser than that of the input voltage. Further, the waveforms represent rectified DC waveforms, and not pure DC waveform, which is evident from the difference in representation when compared to Figure 5.1a. The output side diode bridge rectifies the AC voltage transferred by the transformer, and hence the said waveform.

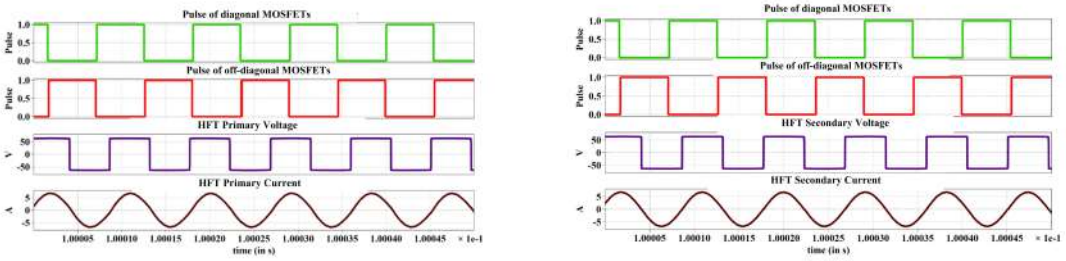
The High - Frequency Transformer (HFT) primary side voltage and current waveforms, along with the diagonal and off - diagonal MOSFET gate pulses, have been provided in the Figure 5.2a. Due to the occurrence of resonance, it is seen that the currents in the primary of both sections are sinusoidal, with the corresponding voltages having square wave-shape. Similar kinds of waveforms have been obtained in the Figure 5.2b, which depicts the transformer secondary voltage and current waveforms along the respective diagonal and off-diagonal MOSFET gate pulses.

The Figure 5.3a depicts the voltage across and the current through the primary side MOSFET Q_1, during the ON-time and the OFF-time period. When the gate pulse is



(a) **(b)**

Fig. 5.1 Waveforms of voltage and current on the (a) Input side and (b) Output side with the MOSFET gate pulses



(a) **(b)**

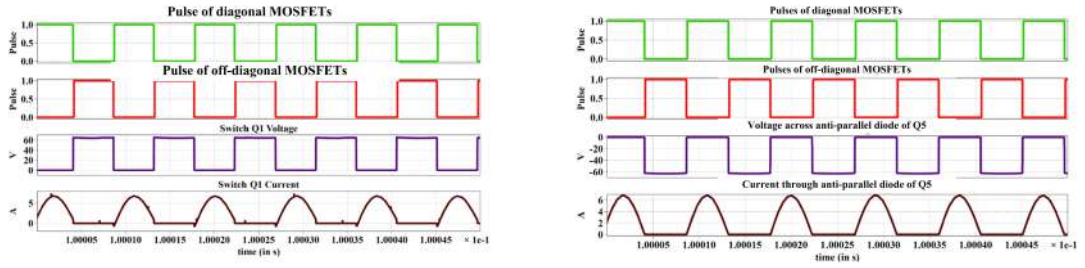
Fig. 5.2 Waveforms of Transformer (a) Primary voltage and current and (b) Secondary voltage and current with the MOSFET gate pulses

HIGH, the current flows through the MOSFET switch, which is evident from the fact that during the ON-time period of the diagonal MOSFETS, the current has a positive value and a sinusoidal curve, while the voltage across that particular MOSFET is zero. When the gate pulse is LOW, the current becomes zero and the voltage takes up a positive value.

The Figure 5.3b represents the switching of the anti-parallel diodes of the secondary side switches, along with the respective MOSFET gate pulses. In accordance with the modes of operation provided in the earlier chapters, the anti-parallel diodes must be in the ON state during the same time period as that of the primary side MOSFETs, for precise power transfer to take place through the attainment of resonance. This is timely switching is presented in the Figure 5.3, where the MOSFET Q_1 and the anti-parallel diode D_5 are in the ON state during the same time period.

5.2 Experimental Setup

In order to validate the operation of the proposed CLLC resonant converter, a low power hardware prototype was implemented in the laboratory. The validation was done using the Chroma DC electronic load 63202, which acted as the perfect stand-in for the Buck load the converter can face while charging an EV battery. The switch used for actuating



(a) **(b)**

Fig. 5.3 Waveforms of voltage and current of (a) Primary side MOSFETs and (b) Secondary side anti-parallel diodes with the MOSFET gate pulses

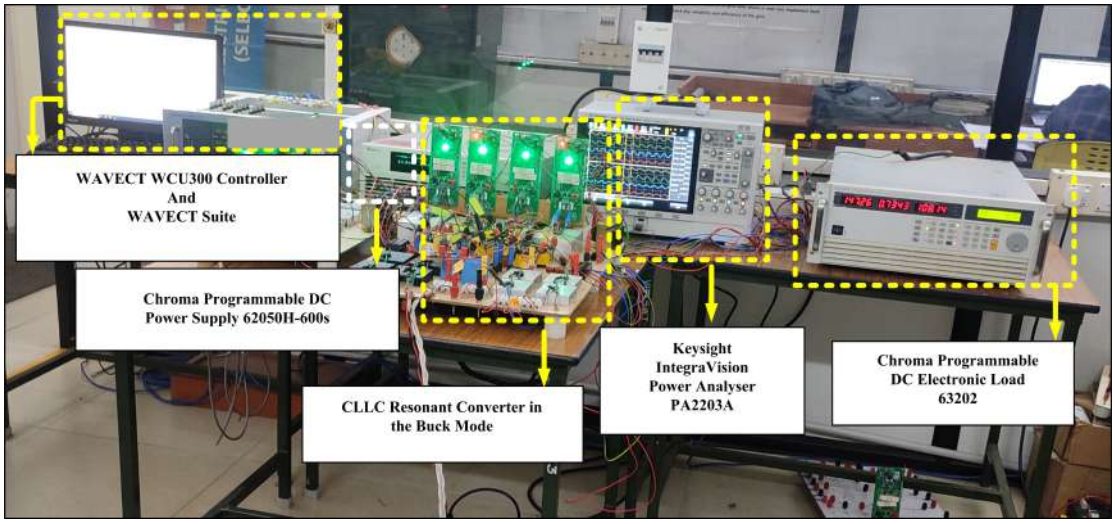


Fig. 5.4 Experimental Setup of the proposed CLLC resonant converter

the proposed converter was an Infineon AIMW120R045M1 SiC MOSFET, while the anti-parallel diodes were Infineon IDH20G65C6 SiC Schottky Diode. The TLP5751 opto-isolators were used in the MOSFET driver boards. The DC power supply for the proposed converter was provided using the Chroma programmable DC Power Supply 62050H-600S. The WAVECT WCU300 controller was used for generating the pulse logic for the MOSFETs. The oscilloscope used for recording the hardware results and efficiency was Keysight IntegraVision Power Analyzer PA2203A. The Figure 5.4 depicts the hardware setup implemented in the laboratory with these discrete components.

5.3 Hardware Results

The figure 5.6 depicts the operating voltage and current across the diagonal and off-diagonal switches (Q_1 and Q_2) during the validation of the hardware prototype. The figure also portrays the gate pulses applied to the respective switches as well.
The figure 5.8 depicts the real time voltage and current waveforms across the HFT pri-

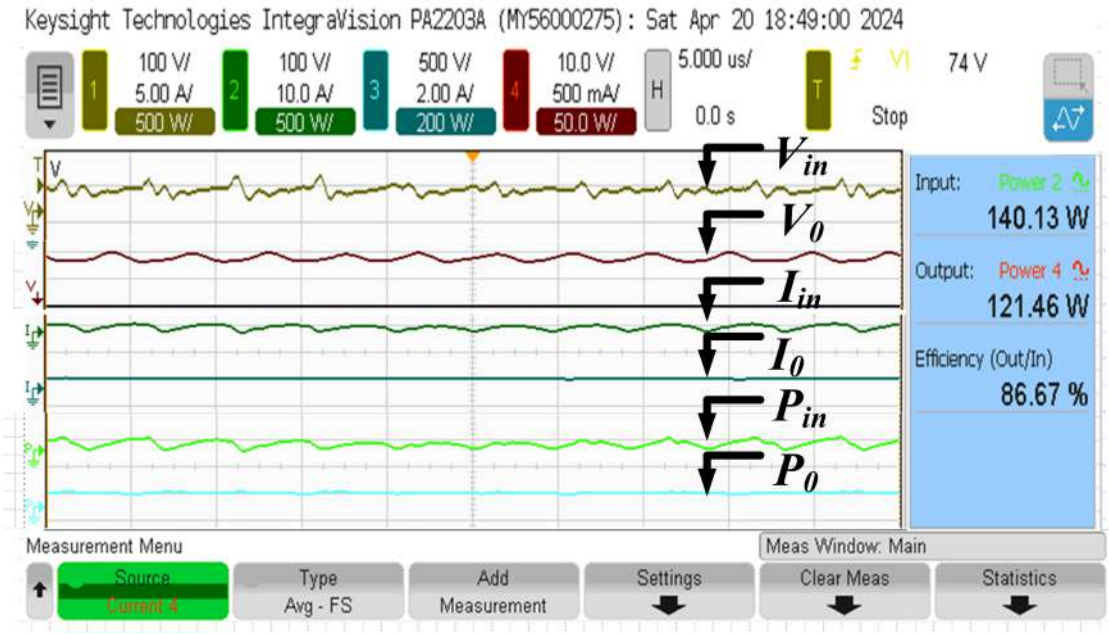


Fig. 5.5 Efficiency of the proposed converter as recorded on the oscilloscope

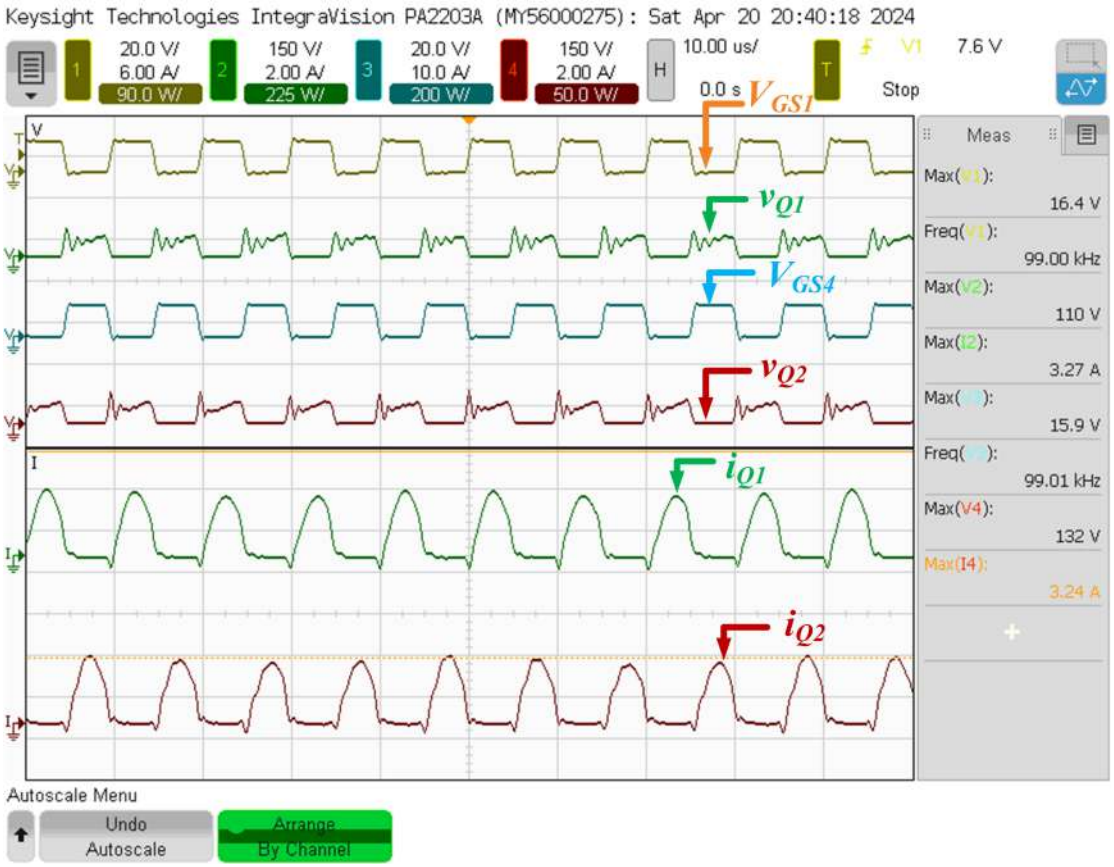


Fig. 5.6 Waveforms of voltage, current and gate pulse of diagonal and off-diagonal MOSFETS

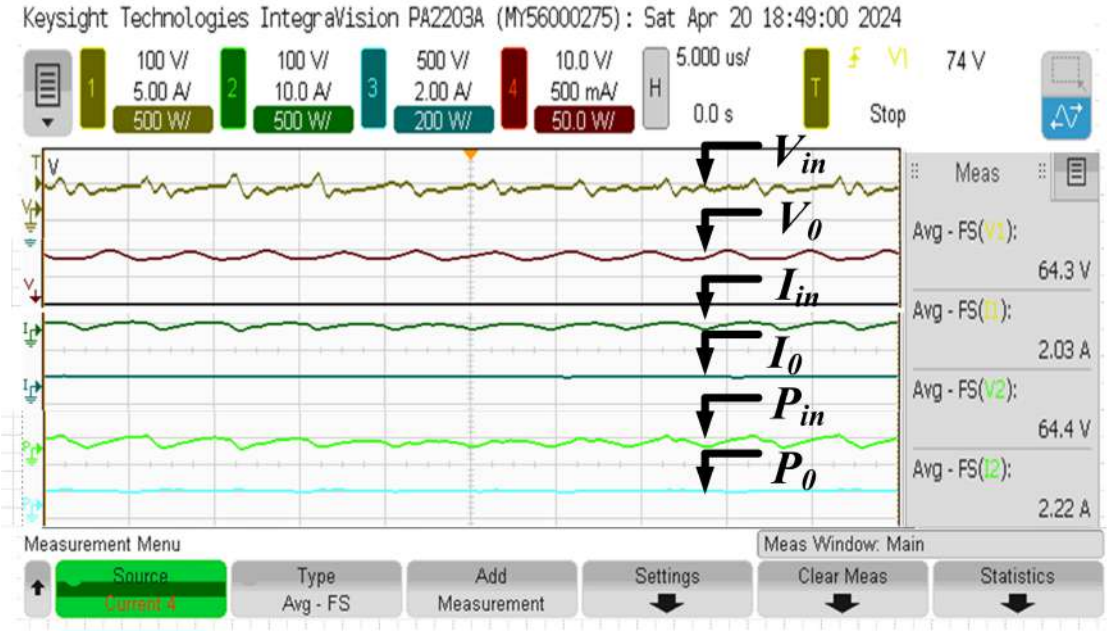


Fig. 5.7 Waveforms Input and Output side voltage, current and power

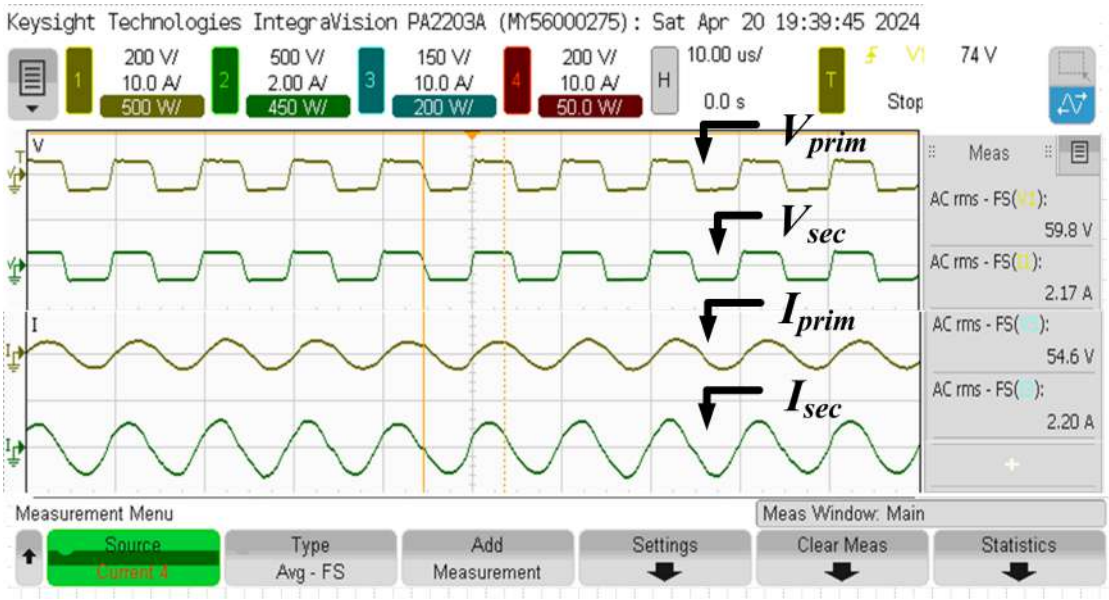


Fig. 5.8 Waveforms of Transformer primary and secondary side voltage and current

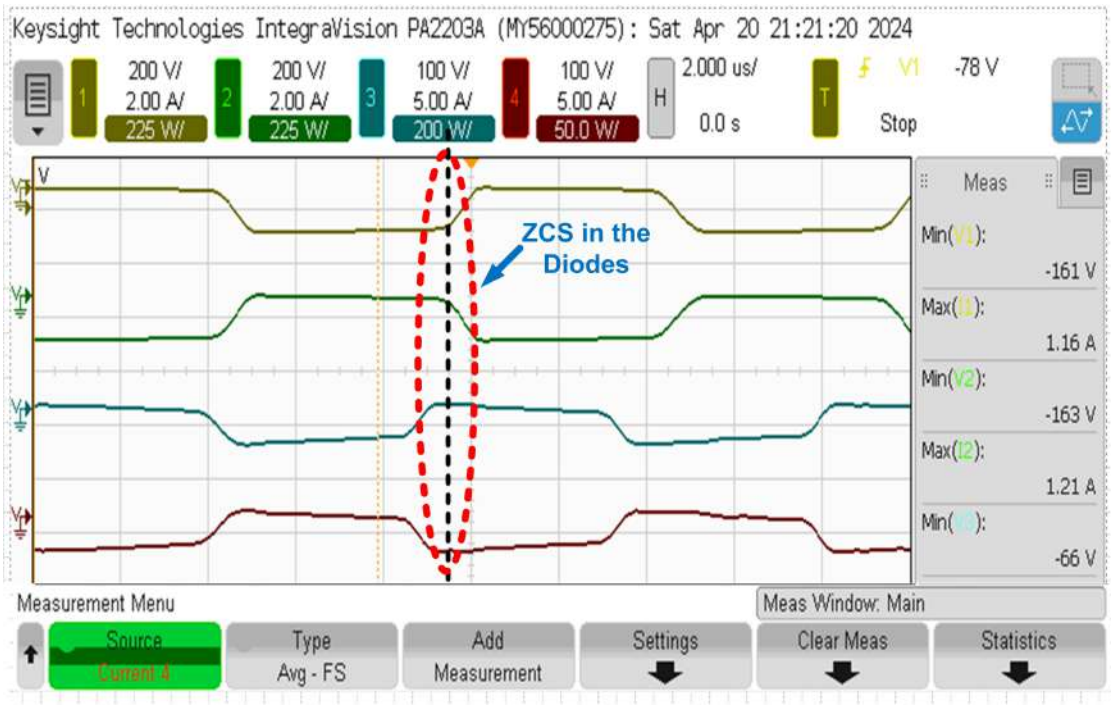


Fig. 5.9 Waveforms of ZCS attainment in the secondary side diodes

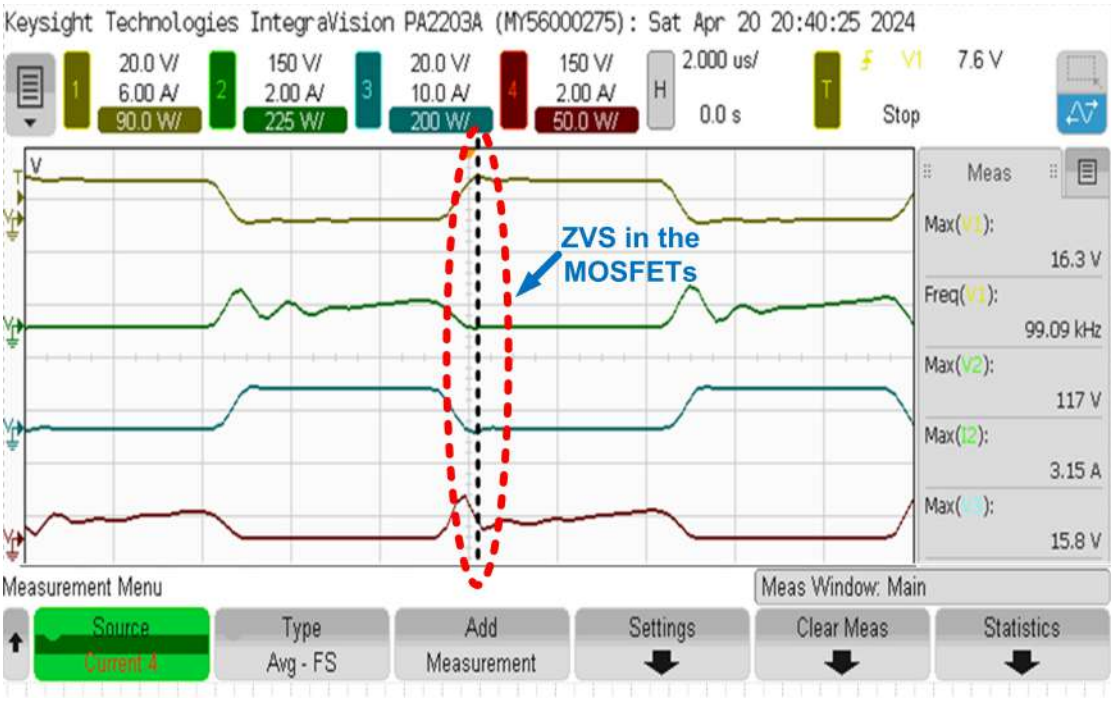


Fig. 5.10 Waveforms of ZVS attainment in the primary side MOSFETs

mary and secondary side, during the validation of the prototype. The attainment of resonance is evident from the fact that the voltage waveforms recorded are sinusoidal in nature and that the voltage and the current values on both the sides of the transformer are identical. This also represents the precise and accurate operation of the proposed CLLC converter.

The waveforms of the input side voltage and current, output side voltage and current and their respective powers have been provided in the figure 5.7.

The figure 5.5 portrays the instantaneous efficiency obtained during the hardware validation of the mentioned low-power prototype. The input and the output power recorded during the validation process is also presented in the said picture.

The figure 5.10 depicts the attainment of Zero Voltage Switching (or) ZVS in the primary side switches, while the figure 5.9 showcases the attainment of Zero Current Switching in the anti-parallel diodes of the secondary side switches.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

As a result of this project, we were able to successfully design, simulate and validate a CLLC resonant converter for Electric Vehicle (EV) battery charging applications in the buck mode. The project addressed the absence of proper hardware prototyping by developing a working a prototype with discrete components, and also provided a detailed operational analysis of the same. However, the presence of several shortcomings were also faced. The losses due to the use of wires of long length, absence of proper protection circuitry, and the absence of precise heat and insulation sinks culminated into a reduced efficiency, as opposed to the one obtained during the simulation. Thus, on a concluding note, it can be proclaimed that this project provides deep insights into the design, operation and validation of resonant converters, and also sheds light on the various difficulties a researcher can possibly face, when faced with a resonant converter design.

6.2 Future Scope

The hardware prototyping of the aforementioned CLLC resonant converter has opened the door to new possibilities. The documentation of a detailed hardware validation and result analysis can pave the way for several technologies which work with converters at their very core. One such future scope, is the possibility of a single input, multiple output EV battery charger. In order to reduce the time needed by vehicle owners to wait outside the charging stations, even before charging their own vehicles, multi-battery charging is the need of the hour. With a predicted increase by manifold times in the field of EV procurement, the design of multi-battery chargers, based on the lesser explored, but more efficient CLLC resonant converter, can prove to be a hidden miracle.

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