UNIVERSITY OF GHANA LEGON

DEPARTMENT OF COMPUTER ENGINEERING

SCHOOL OF ENGINEERING SCIENCES

CEPN 212: COMPUTER SYSTEM DESIGN

LAB 1

INTRODUCTION TO VHDL

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Assignment Date:	26th May, 2023
Submission Date:	11:59pm 1st June, 2023

Introduction

For our first lab, we looked at the general concepts behind the use of VHDL. We also looked at how important VHDL is in modern electronic circuit fabrications as well as the fundamental structure of every VHDL code. We understood that VHDL is not a programming language like C, C++ or Python but a Hardware Description language and code is run concurrently by default. Entry level details of components of VHDL such as libraries, data types and syntax rules were also intrduced. A simple simulation of an AND-gate was observed using the WAVE feature provided in ModelSim Student Edition.

To refresh our memory on what we discussed in class, VHDL is a language for describing digital electronic systems. It arose out of the United States government's Very High Speed Integrated Circuits (VHSIC) program, initiated in 1980. Hence the VHSIC Hardware Description Language (VHDL) was developed, and subsequently adopted as a standard by the Institute of Electrical and Electronic Engineers (IEEE) in the US.

VHDL was designed to fill a number of needs in the design process. VHDL is a standard language for describing the structure and function of designs and sub-designs while highlighting how the sub-designs are interconnected. VHDL allows a design to be simulated before being manufactured, so that designers can quickly compare alternatives and test for correctness without the delay and expense of hardware prototyping. The design process is expedited significantly since VHDL allows easy reuse of designs. The ease of scalability is greatly admired by all engineers.

ASSIGNED TASK

VHDL is a very description language and it provides many features. We will look to cover the fundamental aspects of VHDL.
Your tasks for this lab is to design the following logic gates using the concepts you learnt in class.

- NAND gate
- NOR gate
- Exclusive NOR gate

You are to also take advantage the simulation capabilities of VHDL to simulate the various logic gates you design. Using the WAVE feature provided by ModelSim, force signal values through the input terminals and visualize the waveform form of the design port.

Structure of Lab Report (Hammer Key Points)

1. Title Page: Should contain:
    a. Name
    b. ID number
    c. Date of Submission
    d. Lab index(Lab #X)
    e. Title of Lab
2. Abstract:
    a. A short but comprehensive summary of the entire lab report.
3. Introduction:
    a. Introduction to VHDL.
    b. What the lab report is about.
    c. Why is this lab session and task important?
4. Methodology:
    a. Block diagram of entity showing port terminals and datatype.
    b. Explanation of architecture(s)
5. Results and Discussion:
    a. Truth Table of logic Gates
    b. Waveform simulation of design for all possible input combinations.
    c. Compare truth table with results and explain why you have same or different outcomes.
6. Conclusion
    a. What did you take from the lab you just did?

NOTE!! :

- Marks will be awarded for good VHDL design practices.
- Number of inputs is up to you future engineer.
- Submit VHDL file as well as a pdf of your lab report in a compressed **.zip** or **.rar** file.
- The lab report should follow this naming format: **ID_SURNAME_LAB1**
- Try to avoid late submissions.

SEEK HELP IF YOU HAVE A PROBLEM WITH THE LAB!!!!