UNIVERSITY OF GHANA LEGON

DEPARTMENT OF COMPUTER ENGINEERING

SCHOOL OF ENGINEERING SCIENCES

CEPN 212: COMPUTER SYSTEM DESIGN

LAB 2

HIERARCHICAL DESIGN IN VHDL

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Assignment Date: 2ND June, 2023

Submission Date: 8TH June,2023

Introduction

For this lab, we looked at the hierarchical design concept of VHDL. The hierarchical principle of design in VHDL allows engineers to design small parts of a larger design separately. A component or sub-design could be designed once and reused across the entire scope of a project as many times as needed by just instantiating the sub-design. VHDL has some rules and syntax requirements to follow in order to take effectively apply hierarchical design principle in VHDL. These principles were covered in class. As always, understanding the structure and behavior of your design is pivotal in describing your design to a VHDL compiler.

ASSIGNED TASK

One of the advantages of VHDL is the high level of scalability. The hierarchical design property of VHDL allows us to use smaller and simpler designs to implement larger designs. In class, we learnt how to take advantage of VHDL's hierarchical design property to design a 1-bit full adder by using design of a half adder.

Your tasks for this lab is to design a 4-bit adder using the principle of hierarchical design in VHDL.

You are to also take advantage the simulation capabilities of VHDL to simulate your design. Using the WAVE feature provided by ModelSim, force signal values through the input terminals and visualize the waveform form of your 4-bit adder.

Structure of Lab Report (Hammer Key Points)

1. Title Page: Should contain:
    a. Name
    b. ID number
    c. Date of Submission
    d. Lab index(Lab #X)
    e. Title of Lab
2. Abstract:
    a. A short but comprehensive summary of the entire lab report.
3. Introduction:
    a. Introduction to VHDL.
    b. What the lab report is about.
    c. Why is this lab session and task important?
4. Methodology:
    a. Block diagram of entity showing port terminals and datatype.

b. Explanation of architecture(s)

5. Results and Discussion:
    a. Truth Table of logic Gates
    b. Waveform simulation of design for all possible input combinations.
    c. Compare truth table with results and explain why you have same or different outcomes.
6. Conclusion
    a. What did you take from the lab you just did?

NOTE!! :

- Marks will be awarded for good VHDL design practices.
- Procedure used is up to you engineering but must show the hierarchical design advantage of VHDL.
- Submit VHDL file as well as a pdf of your lab report in a compressed **.zip** or **.rar** file.
- The lab report should follow this naming format: **ID_SURNAME_LAB1**
- Try to avoid late submissions.

SEEK HELP IF YOU HAVE A PROBLEM WITH THE LAB!!!!