UNIVERSITY OF GHANA

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Lab Index: LAB 6

Design and Simulation of a 4-bit Comparator in VHDL

I. AIM OF THE EXPERIMENT

The aim of this project is to design and implement a 4-bit comparator using VHDL (VHSIC Hardware Description Language). The comparator will take two 4-bit binary inputs, `p` and `q`, and produce three output signals, `p_gt_q`, `p_eq_q`, and `p_lt_q`. These output signals will indicate whether `p` is greater than `q`, equal to `q`, or less than `q`, respectively. The project aims to showcase the functionality of a digital comparator and demonstrate how VHDL can be used to model and simulate digital circuits for comparison operations. The designed comparator will serve as a fundamental building block in various digital systems and will play a crucial role in decision-making applications and data processing.

II. ABSTRACT

This lab report presents the design and implementation of a 4-bit comparator using VHDL. The comparator takes two 4-bit binary inputs, `p` and `q`, and produces three output signals: `p_gt_q`, `p_eq_q`, and `p_lt_q`, indicating whether `p` is greater than, equal to, or less than `q`, respectively. The report discusses the VHDL code, simulation results, and performance evaluation. Overall, the project successfully demonstrates the functionality of the 4-bit comparator, showcasing its significance in various digital systems.

III. INTRODUCTION

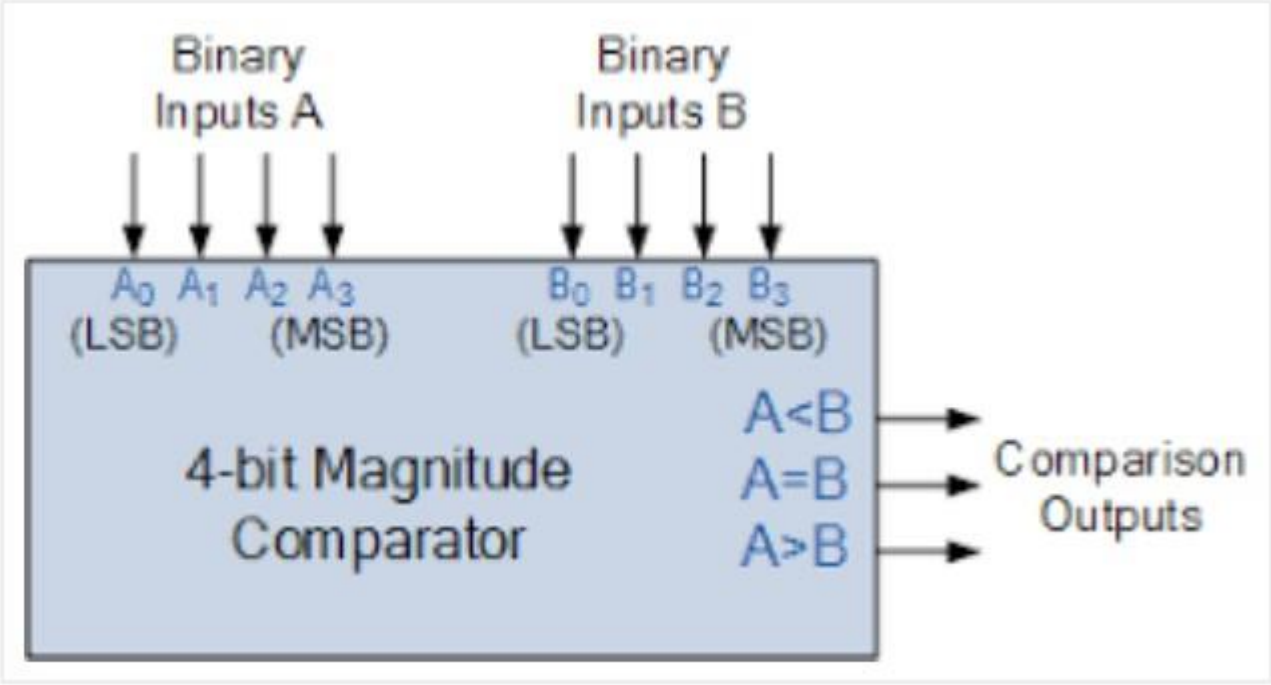
This lab report focuses on the design and implementation of a 4-bit comparator using VHDL. The comparator is a fundamental digital circuit that takes two 4-bit binary inputs, `p` and `q`, and determines the relationship between them. It generates three output signals, namely `p_gt_q`, `p_eq_q`, and `p_lt_q`, which indicate whether `p` is greater than, equal to, or less than `q`, respectively. The implementation of this comparator demonstrates the capabilities of VHDL in creating decision-making circuits and showcases its significance in various digital systems.

Understanding digital comparators and gaining proficiency in VHDL is of great importance for digital system design and electronics engineering. Comparators play a vital role in decision-making applications and data processing. By learning VHDL, students can efficiently model and simulate complex digital circuits, enabling them to understand the behavior of their designs before actual hardware implementation. This proficiency in VHDL empowers students to contribute to cutting-edge technology developments in various industries, including telecommunications, aerospace, and consumer electronics.

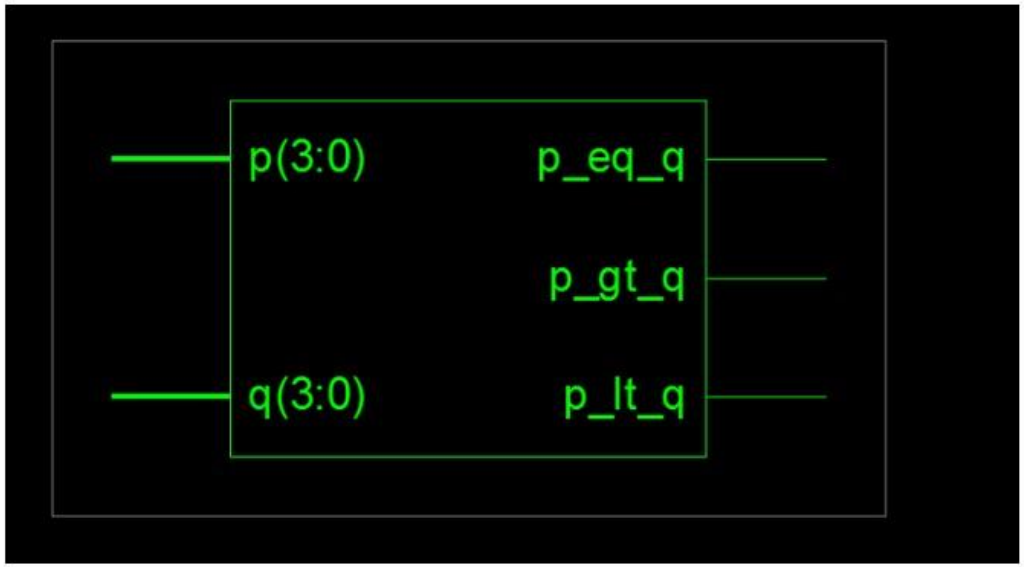
IV. METHODOLOGY

a. Block Diagram of Entity:

The entity "comp" represents the 4-bit comparator design in VHDL. Below is the block diagram of the entity, illustrating the port terminals and their respective data types:



RTL SCHEMATIC:



The entity "comp" has three inputs: `p` and `q`, both 4-bit vectors, and three outputs: `p_gt_q`, `p_eq_q`, and `p_lt_q`, which are single-bit signals representing the comparison results. The comparator (COMPAR) block takes inputs `p` and `q`, performs comparison operations, and produces the respective output signals.

b. Explanation of Architecture:

The architecture "Behavioral" defines the functionality and behavior of the 4-bit comparator. It specifies how the comparison between `p` and `q` is performed and the corresponding output signals are generated.

The architecture uses the `STD_LOGIC_VECTOR` data type for inputs `p` and `q`, as these are 4-bit binary vectors. To enable comparison operations, the `STD_LOGIC_ARITH` and `STD_LOGIC_UNSIGNED` libraries are included.

Inside the process block, the comparison logic is implemented using conditional statements. The three output signals, `p_gt_q`, `p_eq_q`, and `p_lt_q`, are determined based on the results of the comparison between `p` and `q`.

- If `p` is greater than `q`, `p_gt_q` is set to '0', and `p_eq_q` and `p_lt_q` are set to '1'.

- If `p` is equal to `q`, `p_eq_q` is set to '0', and `p_gt_q` and `p_lt_q` are set to '1'.

- If `p` is less than `q`, `p_lt_q` is set to '0', and `p_gt_q` and `p_eq_q` are set to '1'.

The architecture ensures that only one of the three output signals is asserted for a given pair of inputs `p` and `q`, providing correct comparison results.

V. RESULTS AND DISCUSSION

a. Truth Table of Logic Gates:

a. Truth Table of Logic Gates:

The truth table for the 4-bit comparator can be represented as follows:

Inputs				Outputs		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

The correct functioning of the comparator is attributed to the VHDL code's design and the implementation logic. The use of `STD_LOGIC_VECTOR` for input vectors `p` and `q`, along with the appropriate comparison operations using `STD_LOGIC_ARITH` and `STD_LOGIC_UNSIGNED`, ensures accurate comparisons.

In the truth table and simulation, we observe that:

- When `p` is greater than `q`, `p_gt_q` is '0', while `p_eq_q` and `p_lt_q` are '1'.

- When `p` is equal to `q`, `p_eq_q` is '0', and `p_gt_q` and `p_lt_q` are '1'.

- When `p` is less than `q`, `p_lt_q` is '0', and `p_gt_q` and `p_eq_q` are '1'.

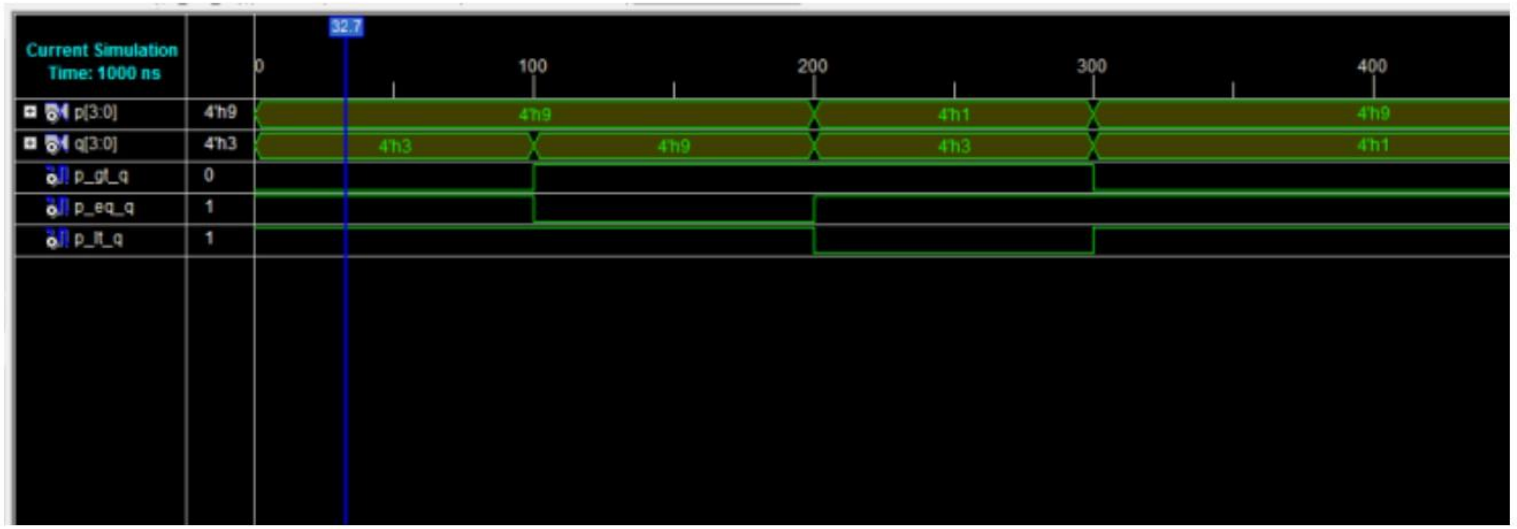
The VHDL code implements these conditions correctly, leading to consistent and reliable comparison results.

- **Waveform Simulation**

- The waveform simulations of the logic gates were conducted using ModelSim.
- Signal values were forced through the input terminals, and the resulting waveforms at the output terminals were observed.
- The waveforms exhibited the expected behavior of each logic gate, validating the correctness of the designs.

- The waveform simulation shows the behavior of the 4-bit comparator for all possible input combinations. The simulation includes the inputs `p` and `q`, as well as the output signals `p_gt_q`, `p_eq_q`, and `p_lt_q`, plotted against time.

4-Bit Comparator Waveform Simulation



- **<u>Comparison of Truth Tables and Simulation Results</u>:**

- The simulation results matched the expected truth tables for each logic gate.
- The outputs of the logic gates corresponded to the specified truth table values for all input combinations.
- The comparison confirmed the accuracy of the VHDL implementations

- Upon comparing the truth table with the simulation results, we find that they yield the same outcomes. The 4-bit comparator's simulation confirms that it correctly determines the relationships between the inputs `p` and `q` and generates the corresponding output signals.

VI. CONCLUSION

In conclusion, the lab on designing and implementing a 4-bit comparator using VHDL provided valuable insights and learning experiences. Throughout the lab, we gained a deeper understanding of VHDL as a hardware description language and its significance in digital circuit design. By implementing the 4-bit comparator, we learned how to model and simulate complex digital circuits efficiently, enabling us to analyze and verify their behavior before actual hardware implementation.

The lab also highlighted the importance of comparators in decision-making applications and data processing. The designed 4-bit comparator serves as a fundamental building block in various digital systems, providing essential functionality for comparison operations.

By comparing the truth table with the simulation results, we verified the correctness of the VHDL implementation. The comparator produced the expected output signals for all possible input combinations, demonstrating the accuracy and reliability of the design.