Parallel-Partition

And (almost) in-place parallel-partition using only exclusive read/write shared variables.

See how-to-use.txt for more information.

TODO

Confusions:

- [ ] Q: Is this really EREW? A: Emphasizez that CREW is really just as good, we assume for loops contant depth, but dispersal of local variables in EREW is "really" log-depth
  @: Bill
- [ ] Q: inplace - used the term "lowspace" for a not inplace algorithm (space > polylog n) A:
  - more emph in prelims
  - reminder in each section on first use
  - clarify that low-space is not in-place @: Alek (?)
- [ ] Q: How phases in first alg fit together A: lemma-based format for what invariants are at the end of each phase @: BIG TODO for Bill
- [ ] Q: pseudocode A: add it to an appendix @: alek
- [ ] Q: Cache Confusions A:
  1) U_i is polylog size and can be partitioned *in cache*
  2) More detailed cache analysis (separate lemma for cache analysis)
  3) Teach Bill what the 2 cache papers [A], [B] are @: Alek
- [ ] Q: Why no worst-case inputs for strided (*3) A: ???????????/ @:

minor

- [ ] Q: footnote 5 A: increase clarity @: alek does, bill checks
- [ ] Q: pg 11 3.5 and 0.5 #s A: clarify @: Bill
- [ ] Q: separate phase to figure out if preds > succ in first alg A: separate phase to figure out if preds > succ in first alg @: Bill
- [ ] Q: 1 based arrays as convention A: clarify @: Alek
- [ ] Q: Regeneron Minor Edits A: add @: Alek

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- [ ] Q: Pinning isn't a real functionality (confused by analysis vs alg barrier) A: Need sentence: Not actually assuming pinning, Just using the possibility of OPT doing it in the analysis @: Bill
- [ ] Q: If you have a lot of threasds could't they use lots of memory? A: polylog cache *per* processor [[add in prelims]] @: Bill
- [ ] Q: More minor critiques