PCIe Connector

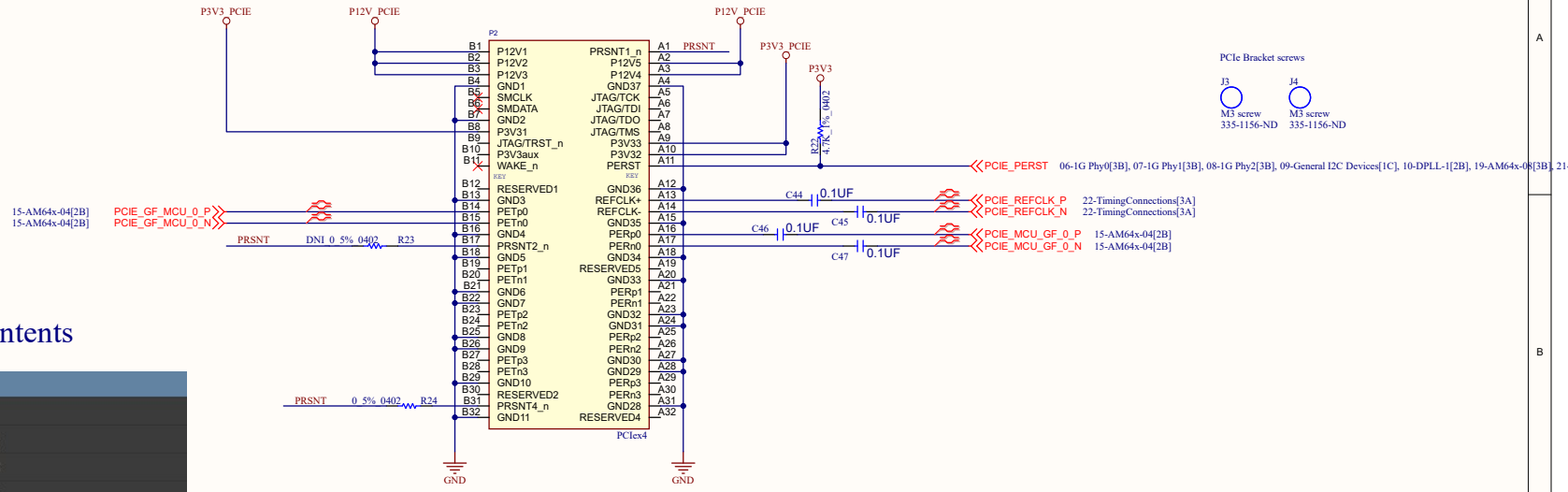


Table of contents

Cannot open file C:\Users\beta\Desktop\Timecard Logo\TIMECARD.jpg. File does not exist.

REV P3 DATE 09/14/21

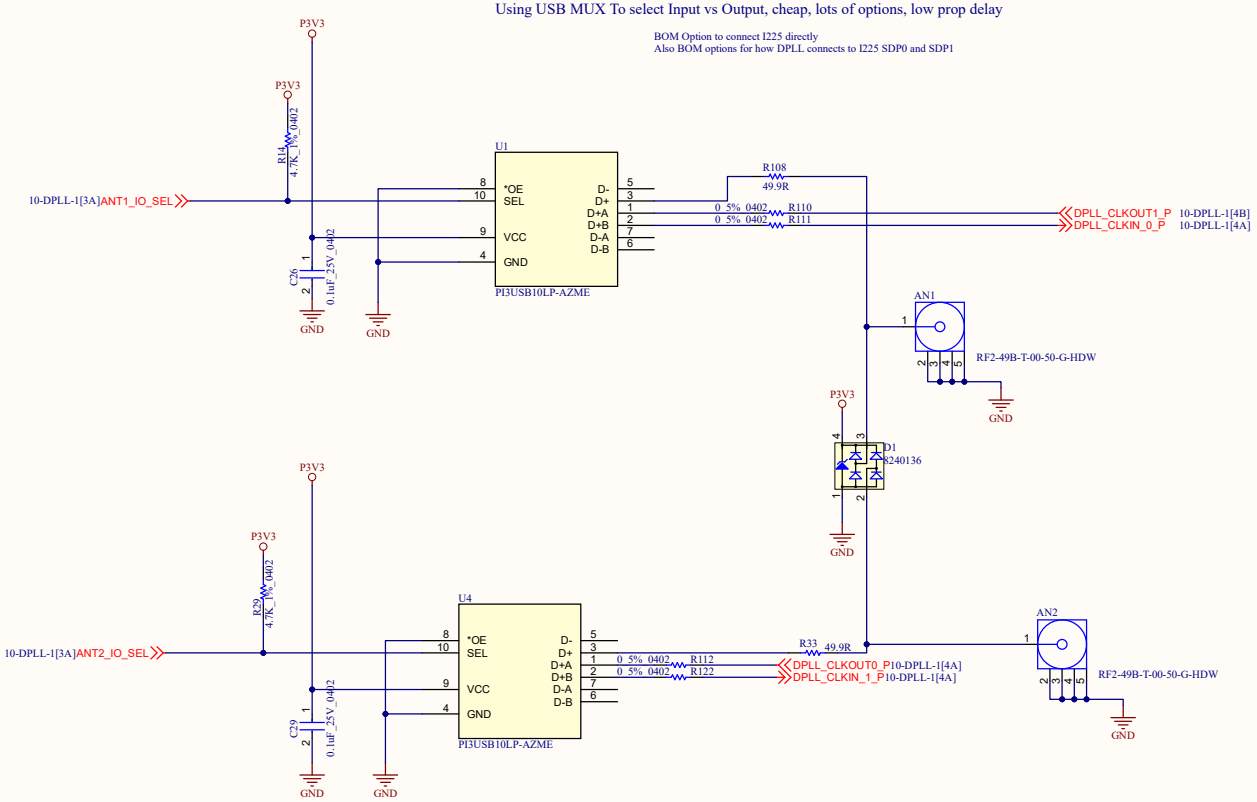
timingcard.com

SHEET 1 OF 25

INPUT/OUTPUT SMA

Using USB MUX To select Input vs Output, cheap, lots of options, low prop delay

BOM Option to connect I225 directly
Also BOM options for how DPLL connects to I225 SDP0 and SDP1



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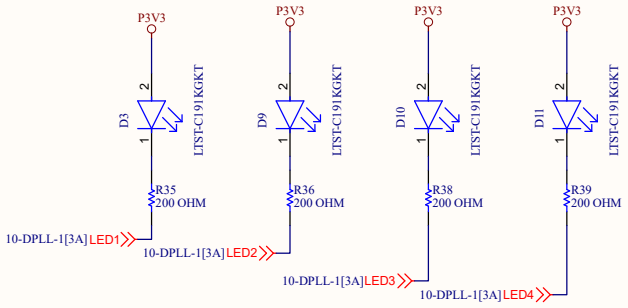
REV P3 DATE 09/14/21

timingcard.com

SHEET 2 OF 25

SYSTEM STATUS LEDS



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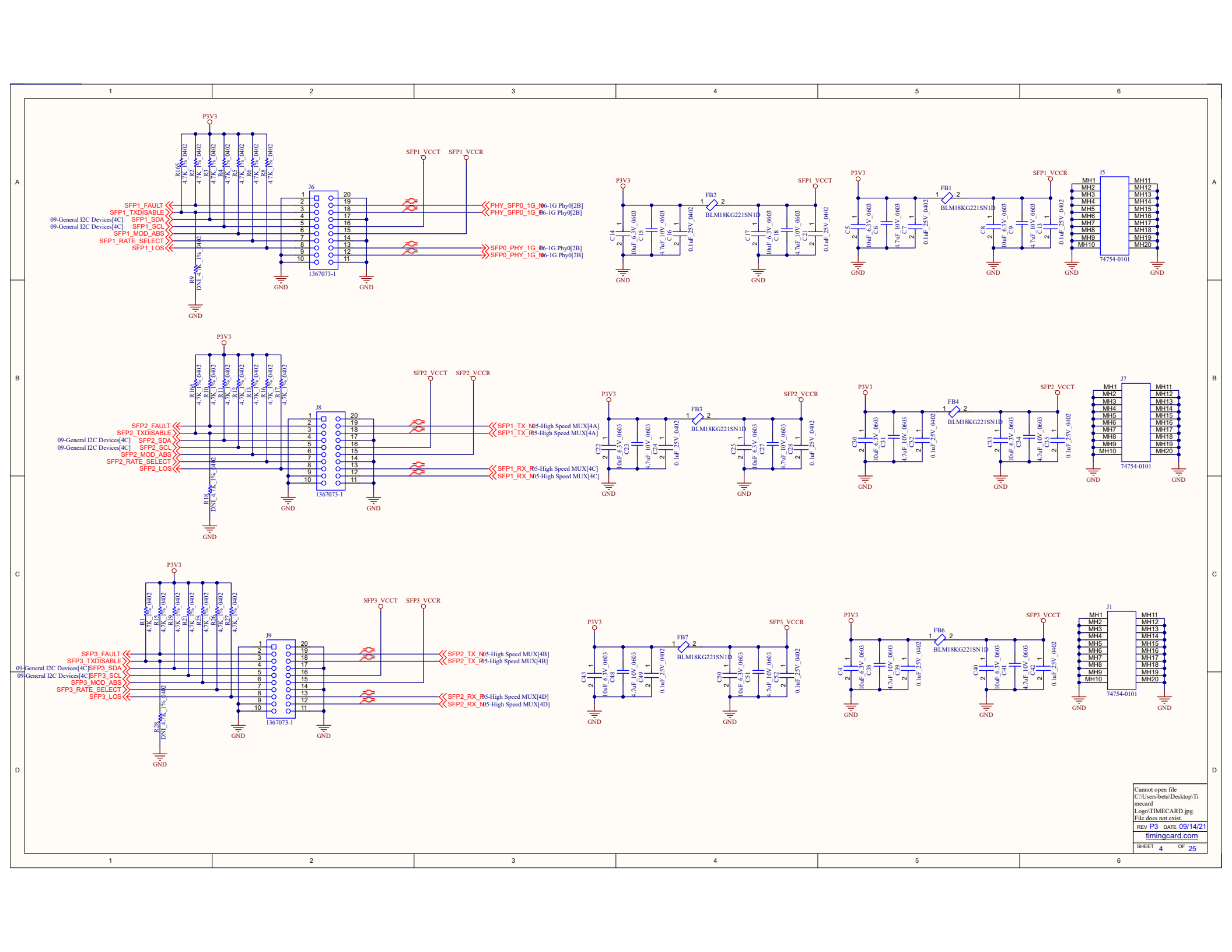

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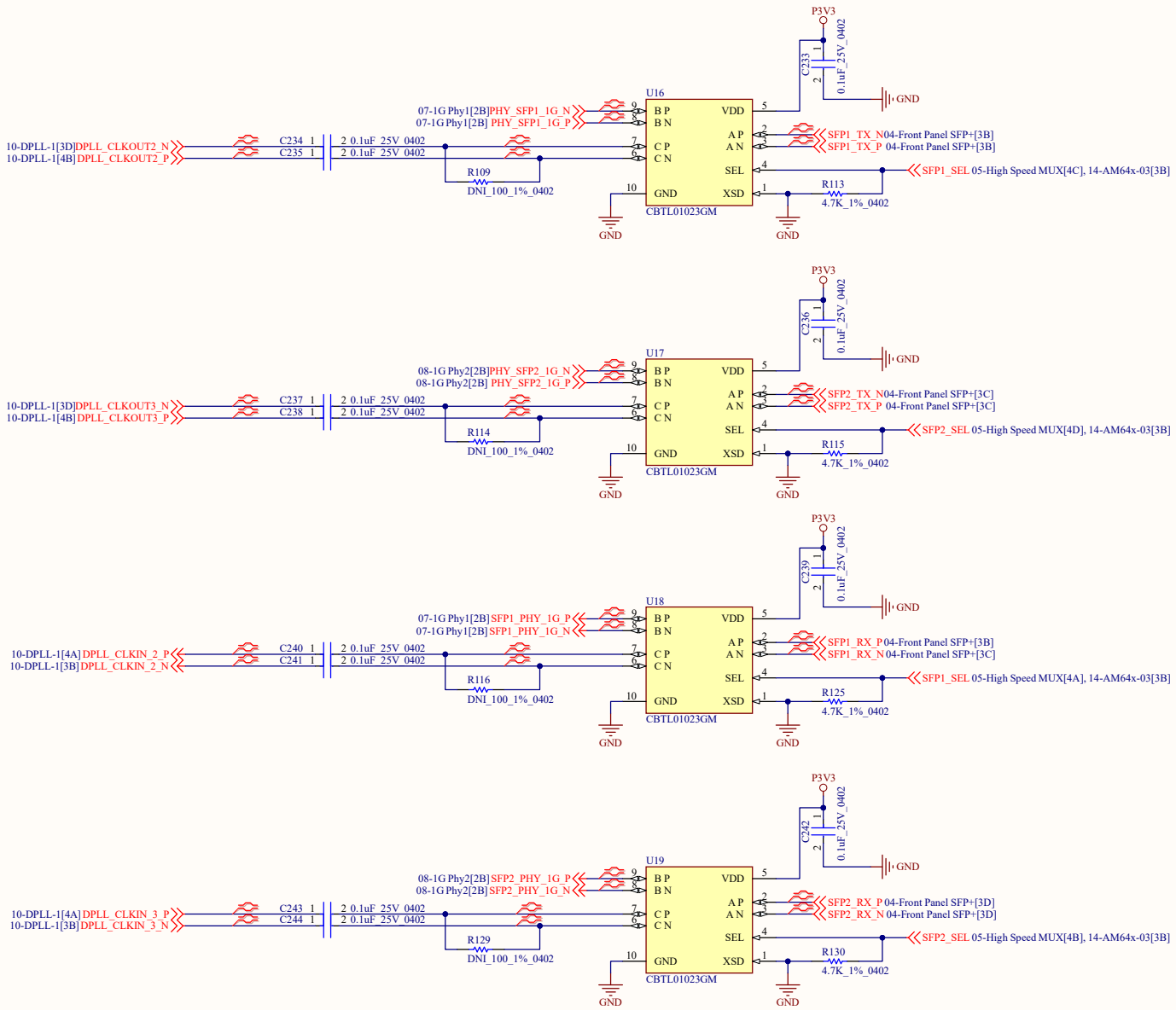
SHEET 4 OF 25

SFP*_TX is input to SFP module



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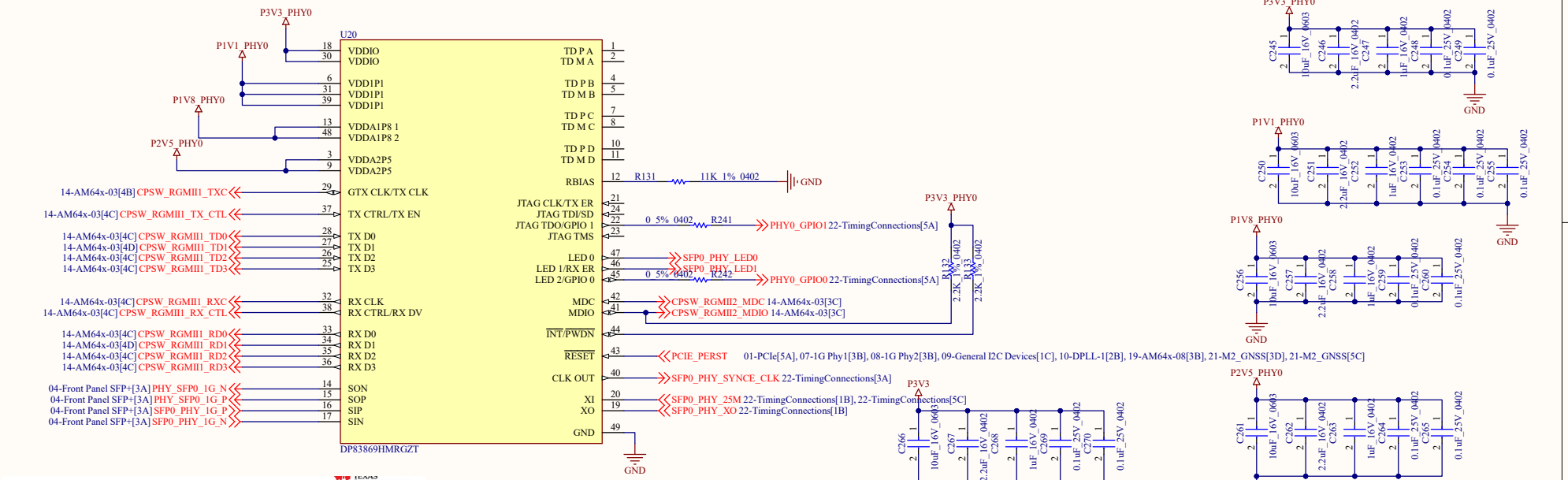


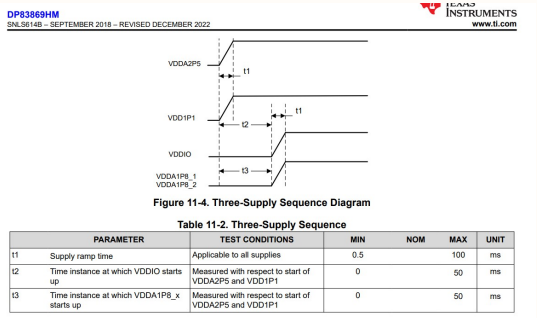
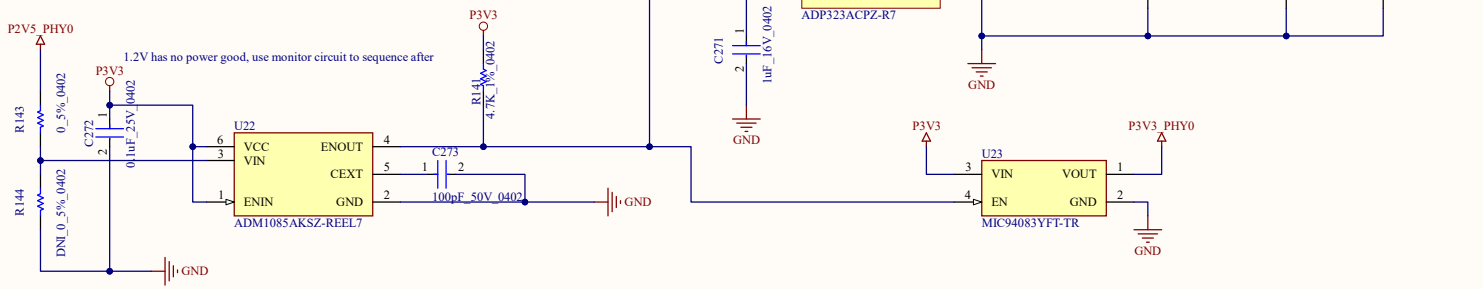


Figure 11-4. Three-Supply Sequence Diagram

Table 11-2. Three-Supply Sequence

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t1	Supply ramp time	Applicable to all supplies	0.5		100	ms
t2	Time instance at which VDDIO starts up	Measured with respect to start of VDDA2P5 and VDD1P1	0		50	ms
t3	Time instance at which VDDA1P8_x starts up	Measured with respect to start of VDDA2P5 and VDD1P1	0		50	ms



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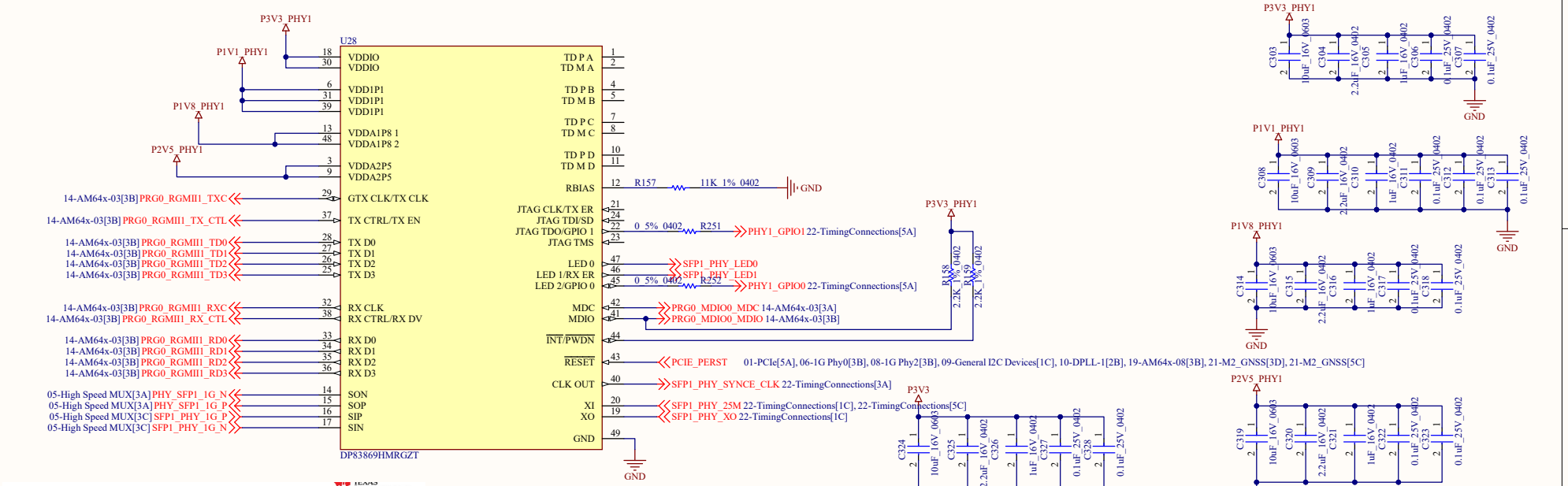

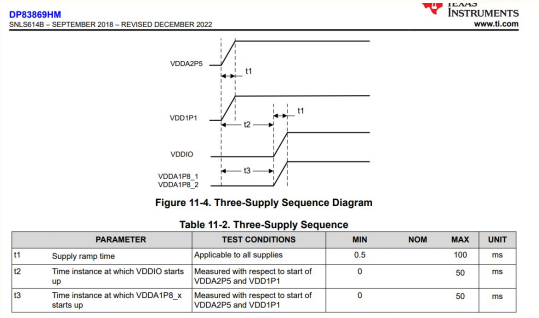

DP83869HM
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Figure 11-4. Three-Supply Sequence Diagram

Table 11-2. Three-Supply Sequence

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t1	Supply ramp time	Applicable to all supplies	0.5		100	ms
t2	Time instance at which VDDIO starts up	Measured with respect to start of VDDA2P5 and VDD1P1	0		50	ms
t3	Time instance at which VDDA1P8_x starts up	Measured with respect to start of VDDA2P5 and VDD1P1	0		50	ms

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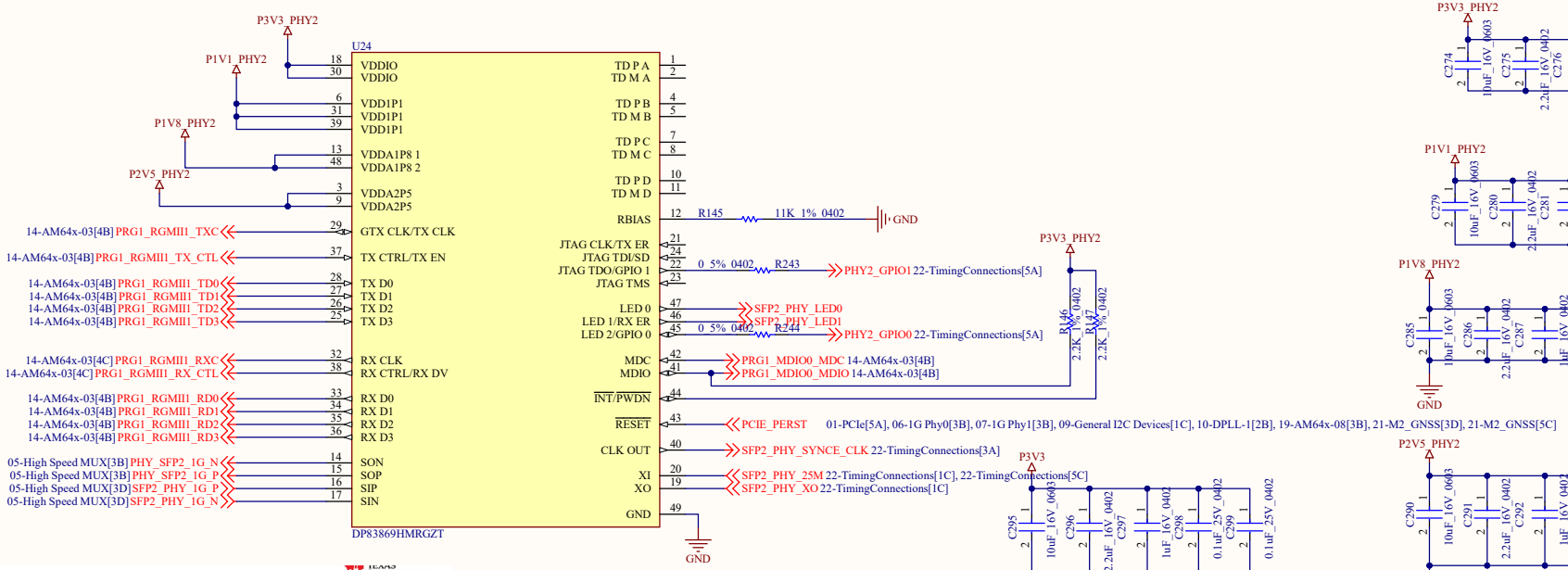


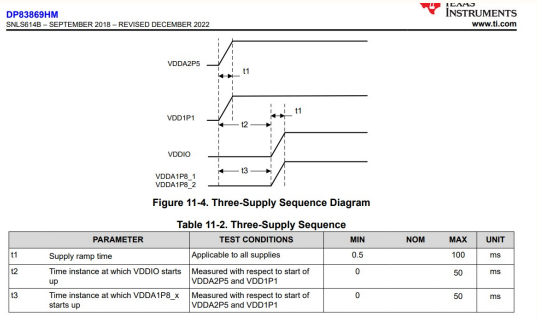
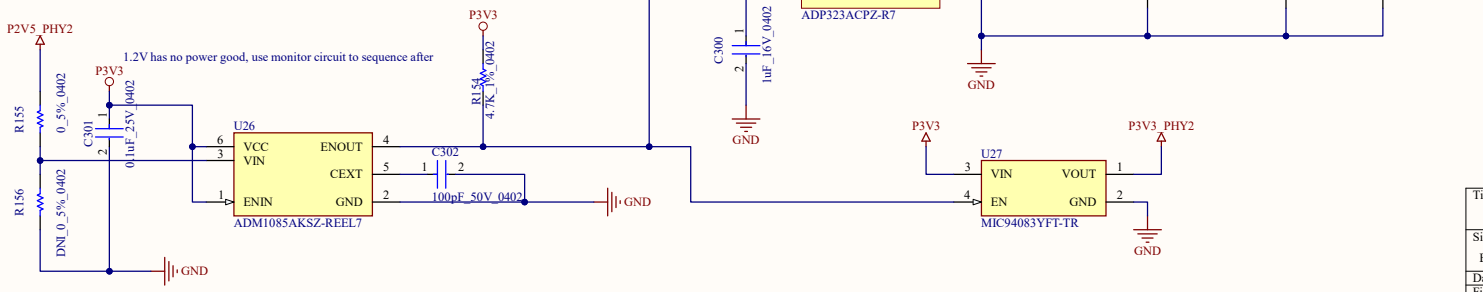


Figure 11-4. Three-Supply Sequence Diagram

Table 11-2. Three-Supply Sequence

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t1	Supply ramp time	Applicable to all supplies	0.5		100	ms
t2	Time instance at which VDDIO starts up	Measured with respect to start of VDDA2P5 and VDD1P1	0		50	ms
t3	Time instance at which VDDA1P8_x starts up	Measured with respect to start of VDDA2P5 and VDD1P1	0		50	ms



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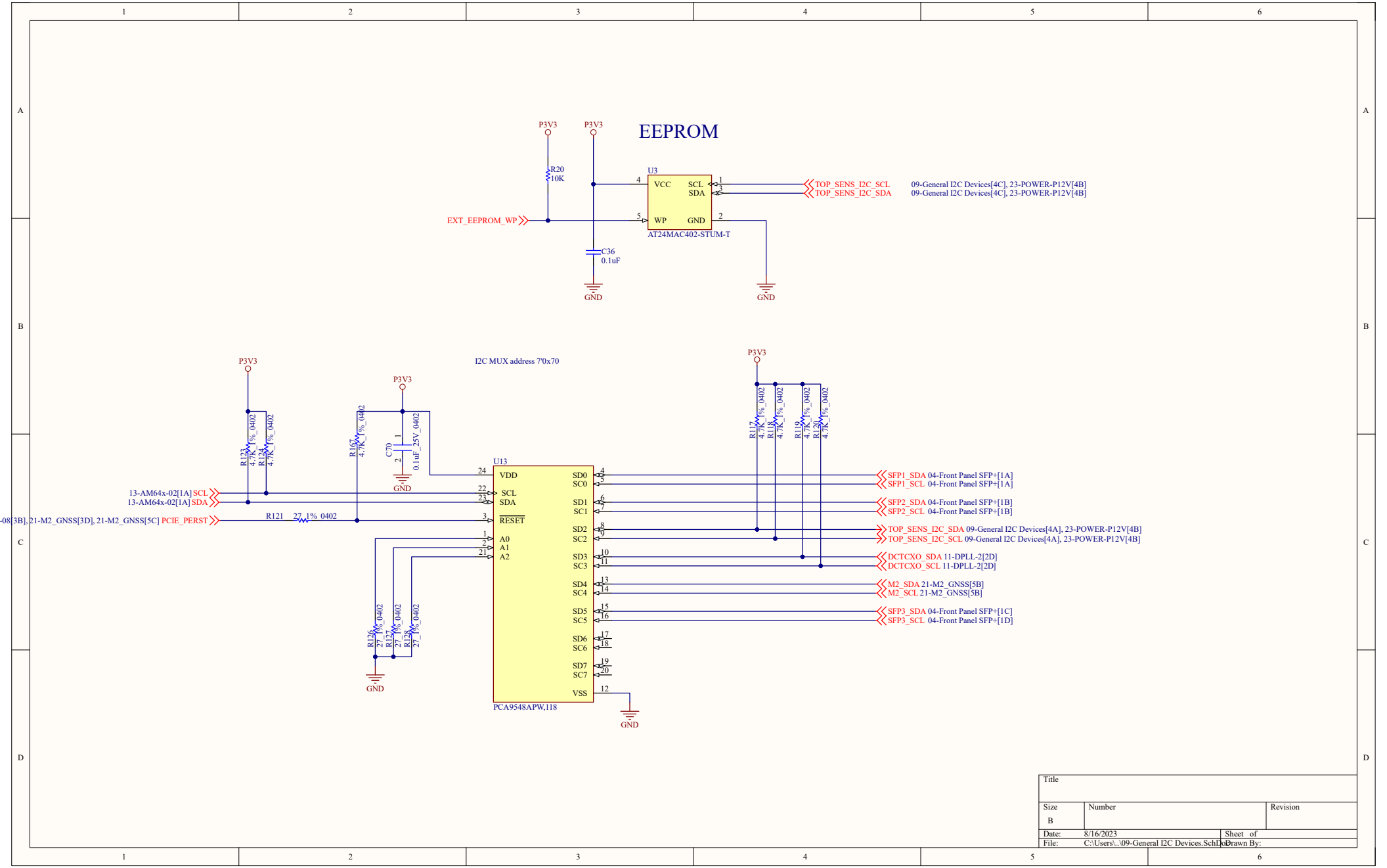
EEPROM
P3V3
P3V3
R20
10K
U3
VCC
SCL
SDA
WP
GND
AT24MAC402-STUM-T
EXT_EEPROM_WP
C36
0.1uF
GND
GND
TOP_SENS_I2C_SCL
TOP_SENS_I2C_SDA
09-General I2C Devices[4C], 23-POWER-P12V[4B]
09-General I2C Devices[4C], 23-POWER-P12V[4B]
I2C MUX address 7'0x70
P3V3
P3V3
P3V3
R123 4.7K_1%_0402
R124 4.7K_1%_0402
R16 4.7K_1%_0402
C70 0.1uF_25V_0402
GND
U13
VDD
SCL
SDA
RESET
A0
A1
A2
VSS
PCA9548APW,118
GND
13-AM64x-02[1A] SCL
13-AM64x-02[1A] SDA
-08[3B], 21-M2_GNSS[3D], 21-M2_GNSS[5C] PCIE_PERST
R121 27_1%_0402
R126 27_1%_0402
R127 27_1%_0402
R128 27_1%_0402
GND
R117 4.7K_1%_0402
R118 4.7K_1%_0402
R119 4.7K_1%_0402
R120 4.7K_1%_0402
SD0
SC0
SD1
SC1
SD2
SC2
SD3
SC3
SD4
SC4
SD5
SC5
SD6
SC6
SD7
SC7
SFP1_SDA 04-Front Panel SFP+[1A]
SFP1_SCL 04-Front Panel SFP+[1A]
SFP2_SDA 04-Front Panel SFP+[1B]
SFP2_SCL 04-Front Panel SFP+[1B]
TOP_SENS_I2C_SDA 09-General I2C Devices[4A], 23-POWER-P12V[4B]
TOP_SENS_I2C_SCL 09-General I2C Devices[4A], 23-POWER-P12V[4B]
DCTCXO_SDA 11-DPLL-2[2D]
DCTCXO_SCL 11-DPLL-2[2D]
M2_SDA 21-M2_GNSS[5B]
M2_SCL 21-M2_GNSS[5B]
SFP3_SDA 04-Front Panel SFP+[1C]
SFP3_SCL 04-Front Panel SFP+[1D]
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Size
B
Number
Revision
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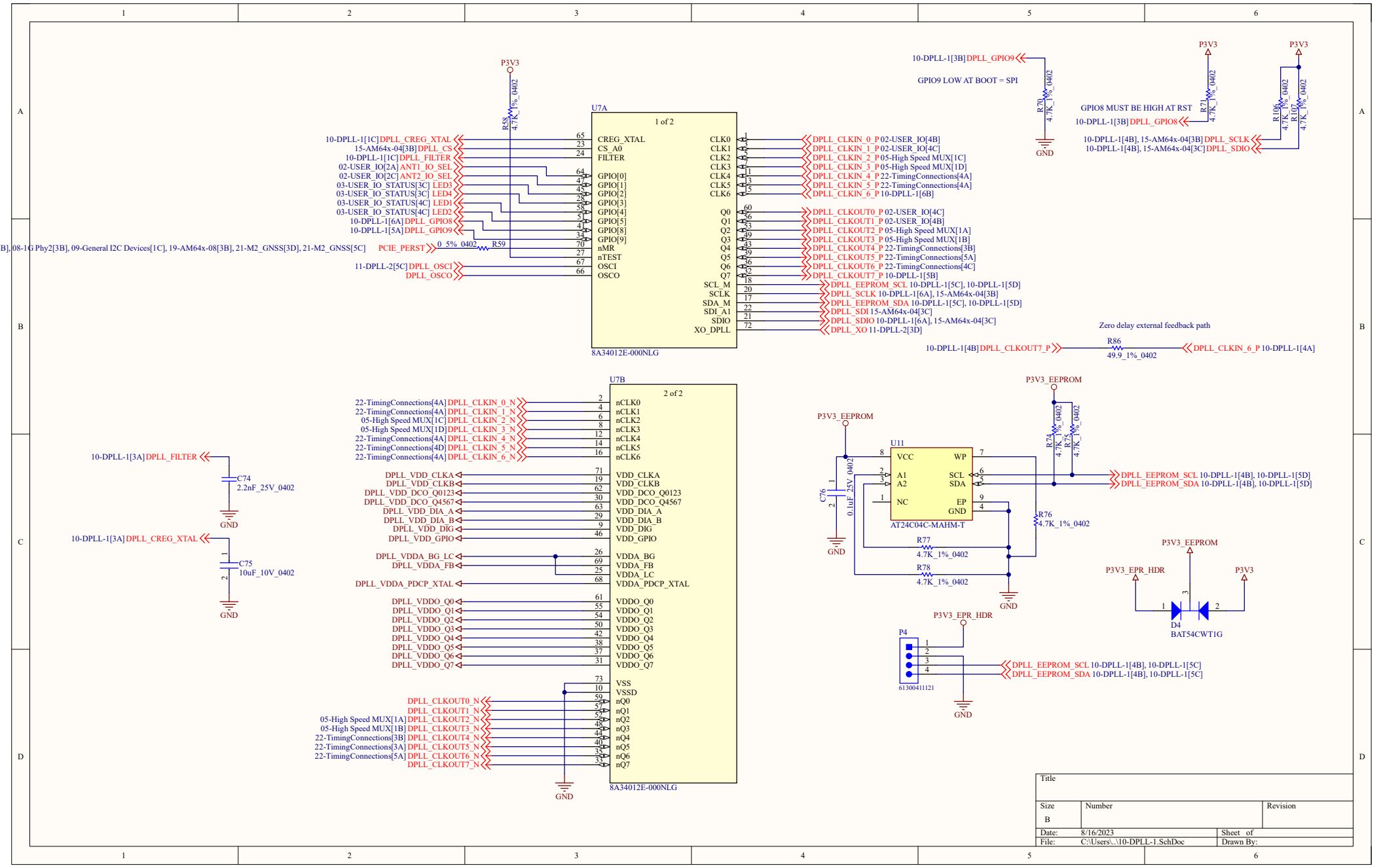
P3V3
R58
4.7K_1%_0402
U7A
1 of 2
10-DPLL-1[1C] DPLL_CREG_XTAL
15-AM64x-04[3B] DPLL_CS
10-DPLL-1[1C] DPLL_FILTER
02-USER_IO[2A] ANT1_IO_SEL
02-USER_IO[2C] ANT2_IO_SEL
03-USER_IO_STATUS[3C] LED3
03-USER_IO_STATUS[3C] LED4
03-USER_IO_STATUS[4C] LED1
03-USER_IO_STATUS[4C] LED2
10-DPLL-1[6A] DPLL_GPIO8
10-DPLL-1[5A] DPLL_GPIO9
B], 08-1G Phy2[3B], 09-General I2C Devices[1C], 19-AM64x-08[3B], 21-M2_GNSS[3D], 21-M2_GNSS[5C]
PCIE_PERST
0_5%_0402
R59
11-DPLL-2[5C] DPLL_OSCI
DPLL_OSCO
CREG_XTAL
CS_A0
FILTER
GPIO[0]
GPIO[1]
GPIO[2]
GPIO[3]
GPIO[4]
GPIO[5]
GPIO[8]
GPIO[9]
nMR
nTEST
OSCI
OSCO
CLK0
CLK1
CLK2
CLK3
CLK4
CLK5
CLK6
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
SCL_M
SCLK
SDA_M
SDI_A1
SDIO
XO_DPLL
DPLL_CLKIN_0_P 02-USER_IO[4B]
DPLL_CLKIN_1_P 02-USER_IO[4C]
DPLL_CLKIN_2_P 05-High Speed MUX[1C]
DPLL_CLKIN_3_P 05-High Speed MUX[1D]
DPLL_CLKIN_4_P 22-TimingConnections[4A]
DPLL_CLKIN_5_P 22-TimingConnections[4A]
DPLL_CLKIN_6_P 10-DPLL-1[6B]
DPLL_CLKOUT0_P 02-USER_IO[4C]
DPLL_CLKOUT1_P 02-USER_IO[4B]
DPLL_CLKOUT2_P 05-High Speed MUX[1A]
DPLL_CLKOUT3_P 05-High Speed MUX[1B]
DPLL_CLKOUT4_P 22-TimingConnections[3B]
DPLL_CLKOUT5_P 22-TimingConnections[5A]
DPLL_CLKOUT6_P 22-TimingConnections[4C]
DPLL_CLKOUT7_P 10-DPLL-1[5B]
DPLL_EEPROM_SCL 10-DPLL-1[5C], 10-DPLL-1[5D]
DPLL_SCLK 10-DPLL-1[6A], 15-AM64x-04[3B]
DPLL_EEPROM_SDA 10-DPLL-1[5C], 10-DPLL-1[5D]
DPLL_SDI 15-AM64x-04[3C]
DPLL_SDIO 10-DPLL-1[6A], 15-AM64x-04[3C]
DPLL_XO 11-DPLL-2[3D]
8A34012E-000NLG
10-DPLL-1[3B] DPLL_GPIO9
GPIO9 LOW AT BOOT = SPI
R70
4.7K_1%_0402
GND
P3V3
R71
4.7K_1%_0402
GPIO8 MUST BE HIGH AT RST
10-DPLL-1[3B] DPLL_GPIO8
P3V3
R106
4.7K_1%_0402
R107
4.7K_1%_0402
10-DPLL-1[4B], 15-AM64x-04[3B] DPLL_SCLK
10-DPLL-1[4B], 15-AM64x-04[3C] DPLL_SDIO
Zero delay external feedback path
10-DPLL-1[4B] DPLL_CLKOUT7_P
R86
49.9_1%_0402
DPLL_CLKIN_6_P 10-DPLL-1[4A]
U7B
2 of 2
22-TimingConnections[4A] DPLL_CLKIN_0_N
22-TimingConnections[4A] DPLL_CLKIN_1_N
05-High Speed MUX[1C] DPLL_CLKIN_2_N
05-High Speed MUX[1D] DPLL_CLKIN_3_N
22-TimingConnections[4A] DPLL_CLKIN_4_N
22-TimingConnections[4D] DPLL_CLKIN_5_N
22-TimingConnections[4A] DPLL_CLKIN_6_N
DPLL_VDD_CLKA
DPLL_VDD_CLKB
DPLL_VDD_DCO_Q0123
DPLL_VDD_DCO_Q4567
DPLL_VDD_DIA_A
DPLL_VDD_DIA_B
DPLL_VDD_DIG
DPLL_VDD_GPIO
DPLL_VDDA_BG_LC
DPLL_VDDA_FB
DPLL_VDDA_PDCP_XTAL
DPLL_VDDO_Q0
DPLL_VDDO_Q1
DPLL_VDDO_Q2
DPLL_VDDO_Q3
DPLL_VDDO_Q4
DPLL_VDDO_Q5
DPLL_VDDO_Q6
DPLL_VDDO_Q7
VSS
VSSD
DPLL_CLKOUT0_N
DPLL_CLKOUT1_N
05-High Speed MUX[1A] DPLL_CLKOUT2_N
05-High Speed MUX[1B] DPLL_CLKOUT3_N
22-TimingConnections[3B] DPLL_CLKOUT4_N
22-TimingConnections[3A] DPLL_CLKOUT5_N
22-TimingConnections[5A] DPLL_CLKOUT6_N
DPLL_CLKOUT7_N
8A34012E-000NLG
GND
10-DPLL-1[3A] DPLL_FILTER
C74
2.2nF_25V_0402
GND
10-DPLL-1[3A] DPLL_CREG_XTAL
C75
10uF_10V_0402
GND
P3V3_EEPROM
U11
VCC
A1
A2
NC
WP
SCL
SDA
EP
GND
AT24C04C-MAHM-T
C76
0.1uF_25V_0402
GND
R74
4.7K_1%_0402
R75
4.7K_1%_0402
DPLL_EEPROM_SCL 10-DPLL-1[4B], 10-DPLL-1[5D]
DPLL_EEPROM_SDA 10-DPLL-1[4B], 10-DPLL-1[5D]
R76
4.7K_1%_0402
R77
4.7K_1%_0402
R78
4.7K_1%_0402
GND
P3V3_EEPROM
P3V3_EPR_HDR
P3V3
D4
BAT54CWT1G
P3V3_EPR_HDR
P4
61300411121
DPLL_EEPROM_SCL 10-DPLL-1[4B], 10-DPLL-1[5C]
DPLL_EEPROM_SDA 10-DPLL-1[4B], 10-DPLL-1[5C]
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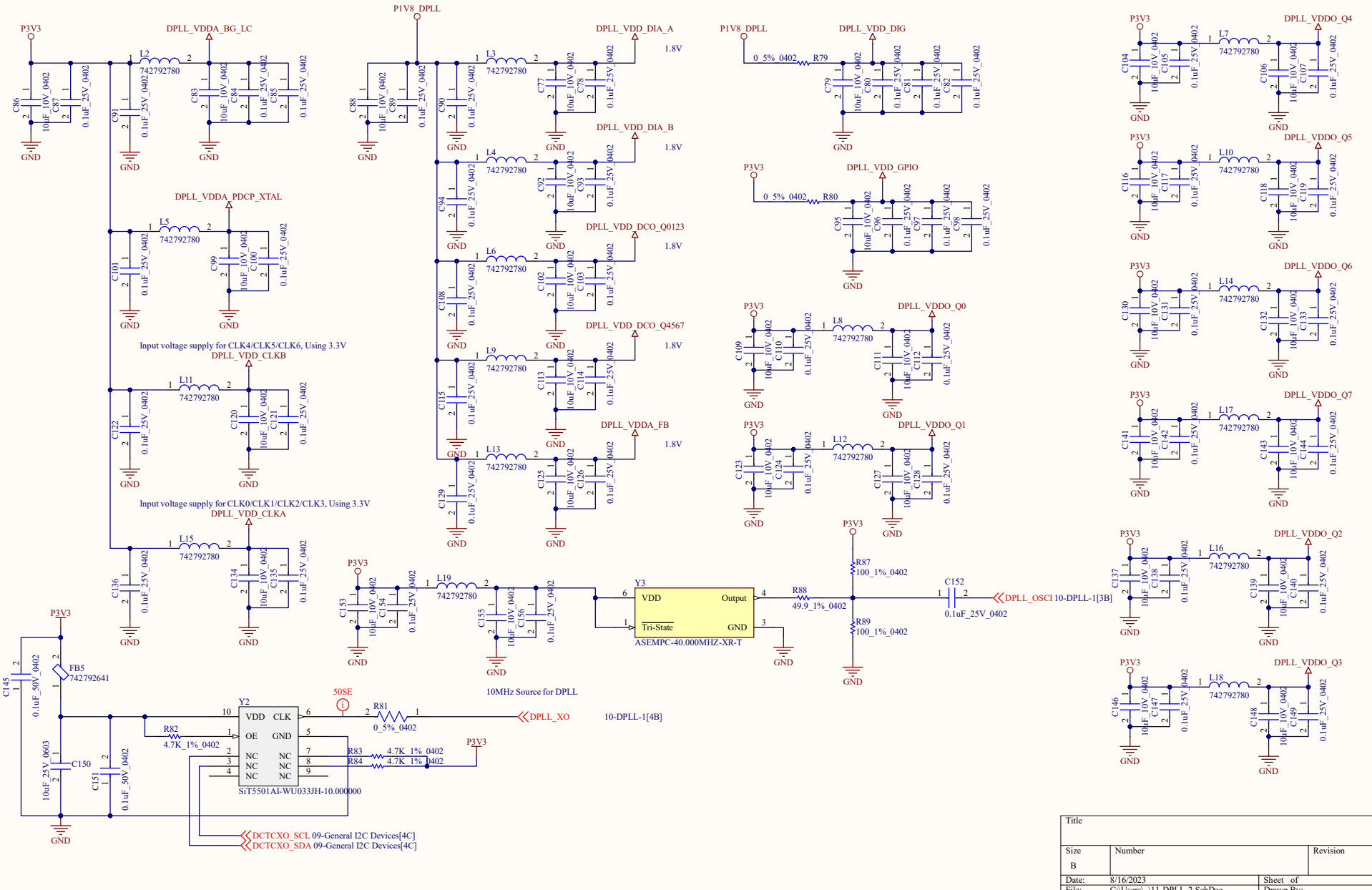
P3V3
DPLL_VDDA_BG_LC
L2
742792780
C86
10uF_10V_0402
C87
0.1uF_25V_0402
C91
0.1uF_25V_0402
C83
10uF_10V_0402
C84
0.1uF_25V_0402
C85
0.1uF_25V_0402
GND
DPLL_VDDA_PDCP_XTAL
L5
742792780
C101
0.1uF_25V_0402
C99
10uF_10V_0402
C100
0.1uF_25V_0402
Input voltage supply for CLK4/CLK5/CLK6, Using 3.3V
DPLL_VDD_CLKB
L11
742792780
C122
0.1uF_25V_0402
C120
10uF_10V_0402
C121
0.1uF_25V_0402
Input voltage supply for CLK0/CLK1/CLK2/CLK3, Using 3.3V
DPLL_VDD_CLKA
L15
742792780
C136
0.1uF_25V_0402
C134
10uF_10V_0402
C135
0.1uF_25V_0402
P1V8_DPLL
DPLL_VDD_DIA_A
1.8V
L3
742792780
C88
10uF_10V_0402
C89
0.1uF_25V_0402
C90
0.1uF_25V_0402
C77
10uF_10V_0402
C78
0.1uF_25V_0402
DPLL_VDD_DIA_B
1.8V
L4
742792780
C94
0.1uF_25V_0402
C92
10uF_10V_0402
C93
0.1uF_25V_0402
DPLL_VDD_DCO_Q0123
1.8V
L6
742792780
C108
0.1uF_25V_0402
C102
10uF_10V_0402
C103
0.1uF_25V_0402
DPLL_VDD_DCO_Q4567
1.8V
L9
742792780
C115
0.1uF_25V_0402
C113
10uF_10V_0402
C114
0.1uF_25V_0402
DPLL_VDDA_FB
1.8V
L13
742792780
C129
0.1uF_25V_0402
C125
10uF_10V_0402
C126
0.1uF_25V_0402
P1V8_DPLL
DPLL_VDD_DIG
0_5%_0402
R79
C79
10uF_10V_0402
C80
0.1uF_25V_0402
C81
0.1uF_25V_0402
C82
0.1uF_25V_0402
P3V3
DPLL_VDD_GPIO
0_5%_0402
R80
C95
10uF_10V_0402
C96
0.1uF_25V_0402
C97
0.1uF_25V_0402
C98
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q0
L8
742792780
C109
10uF_10V_0402
C110
0.1uF_25V_0402
C111
10uF_10V_0402
C112
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q1
L12
742792780
C123
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C124
0.1uF_25V_0402
C127
10uF_10V_0402
C128
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q4
L7
742792780
C104
10uF_10V_0402
C105
0.1uF_25V_0402
C106
10uF_10V_0402
C107
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q5
L10
742792780
C116
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C117
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C118
10uF_10V_0402
C119
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q6
L14
742792780
C130
10uF_10V_0402
C131
0.1uF_25V_0402
C132
10uF_10V_0402
C133
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q7
L17
742792780
C141
10uF_10V_0402
C142
0.1uF_25V_0402
C143
10uF_10V_0402
C144
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q2
L16
742792780
C137
10uF_10V_0402
C138
0.1uF_25V_0402
C139
10uF_10V_0402
C140
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q3
L18
742792780
C146
10uF_10V_0402
C147
0.1uF_25V_0402
C148
10uF_10V_0402
C149
0.1uF_25V_0402
P3V3
L19
742792780
C153
10uF_10V_0402
C154
0.1uF_25V_0402
C155
10uF_10V_0402
C156
0.1uF_25V_0402
Y3
VDD
Output
Tri-State
GND
ASEMPC-40.000MHZ-XR-T
R88
49.9_1%_0402
R87
100_1%_0402
R89
100_1%_0402
C152
0.1uF_25V_0402
DPLL_OSCI
10-DPLL-1[3B]
P3V3
FB5
742792641
C145
0.1uF_50V_0402
C150
10uF_25V_0603
C151
0.1uF_50V_0402
Y2
VDD
CLK
OE
GND
NC
NC
NC
NC
NC
SiT5501AI-WU033JH-10.000000
50SE
R81
0_5%_0402
DPLL_XO
10-DPLL-1[4B]
10MHz Source for DPLL
R82
4.7K_1%_0402
R83
4.7K_1%_0402
R84
4.7K_1%_0402
P3V3
DCTCXO_SCL
09-General I2C Devices[4C]
DCTCXO_SDA
09-General I2C Devices[4C]
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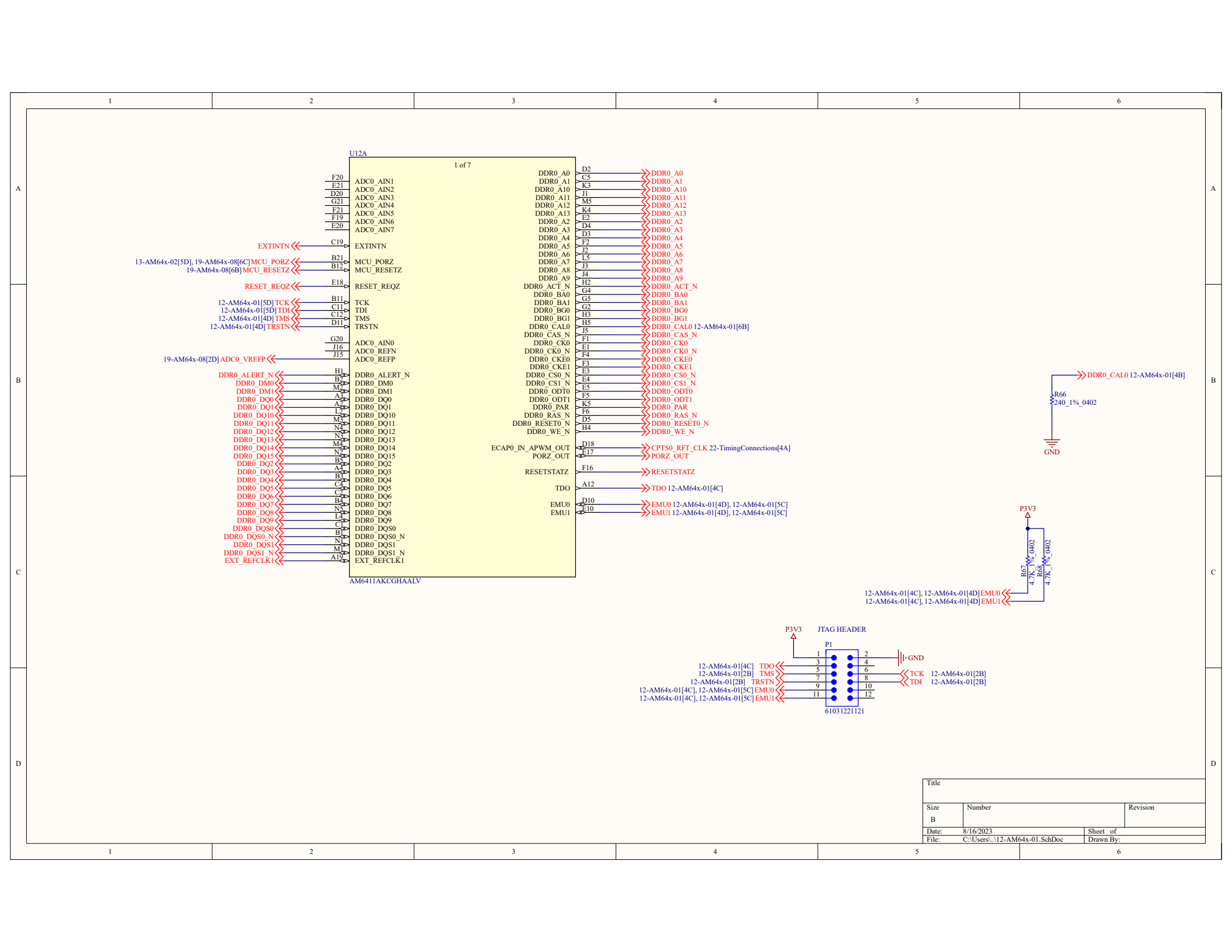
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1 of 7
AM6411AKCGHAALV
ADC0_AIN1
ADC0_AIN2
ADC0_AIN3
ADC0_AIN4
ADC0_AIN5
ADC0_AIN6
ADC0_AIN7
EXTINTN
MCU_PORZ
MCU_RESETZ
RESET_REQZ
TCK
TDI
TMS
TRSTN
ADC0_AIN0
ADC0_REFN
ADC0_REFP
DDR0_ALERT_N
DDR0_DM0
DDR0_DM1
DDR0_DQ0
DDR0_DQ1
DDR0_DQ10
DDR0_DQ11
DDR0_DQ12
DDR0_DQ13
DDR0_DQ14
DDR0_DQ15
DDR0_DQ2
DDR0_DQ3
DDR0_DQ4
DDR0_DQ5
DDR0_DQ6
DDR0_DQ7
DDR0_DQ8
DDR0_DQ9
DDR0_DQS0
DDR0_DQS0_N
DDR0_DQS1
DDR0_DQS1_N
EXT_REFCLK1
DDR0_A0
DDR0_A1
DDR0_A10
DDR0_A11
DDR0_A12
DDR0_A13
DDR0_A2
DDR0_A3
DDR0_A4
DDR0_A5
DDR0_A6
DDR0_A7
DDR0_A8
DDR0_A9
DDR0_ACT_N
DDR0_BA0
DDR0_BA1
DDR0_BG0
DDR0_BG1
DDR0_CAL0
DDR0_CAS_N
DDR0_CK0
DDR0_CK0_N
DDR0_CKE0
DDR0_CKE1
DDR0_CS0_N
DDR0_CS1_N
DDR0_ODT0
DDR0_ODT1
DDR0_PAR
DDR0_RAS_N
DDR0_RESET0_N
DDR0_WE_N
ECAP0_IN_APWM_OUT
PORZ_OUT
RESETSTATZ
TDO
EMU0
EMU1
13-AM64x-02[5D], 19-AM64x-08[6C] MCU_PORZ
19-AM64x-08[6B] MCU_RESETZ
12-AM64x-01[5D] TCK
12-AM64x-01[5D] TDI
12-AM64x-01[4D] TMS
12-AM64x-01[4D] TRSTN
19-AM64x-08[2D] ADC0_VREFP
DDR0_CAL0 12-AM64x-01[6B]
CPTS0_RFT_CLK 22-TimingConnections[4A]
TDO 12-AM64x-01[4C]
EMU0 12-AM64x-01[4D], 12-AM64x-01[5C]
EMU1 12-AM64x-01[4D], 12-AM64x-01[5C]
DDR0_CAL0 12-AM64x-01[4B]
R66
240_1%_0402
GND
P3V3
R67
4.7K_1%_0402
R68
4.7K_1%_0402
12-AM64x-01[4C], 12-AM64x-01[4D] EMU0
12-AM64x-01[4C], 12-AM64x-01[4D] EMU1
JTAG HEADER
P1
12-AM64x-01[4C] TDO
12-AM64x-01[2B] TMS
12-AM64x-01[2B] TRSTN
12-AM64x-01[4C], 12-AM64x-01[5C] EMU0
12-AM64x-01[4C], 12-AM64x-01[5C] EMU1
TCK 12-AM64x-01[2B]
TDI 12-AM64x-01[2B]
61031221121
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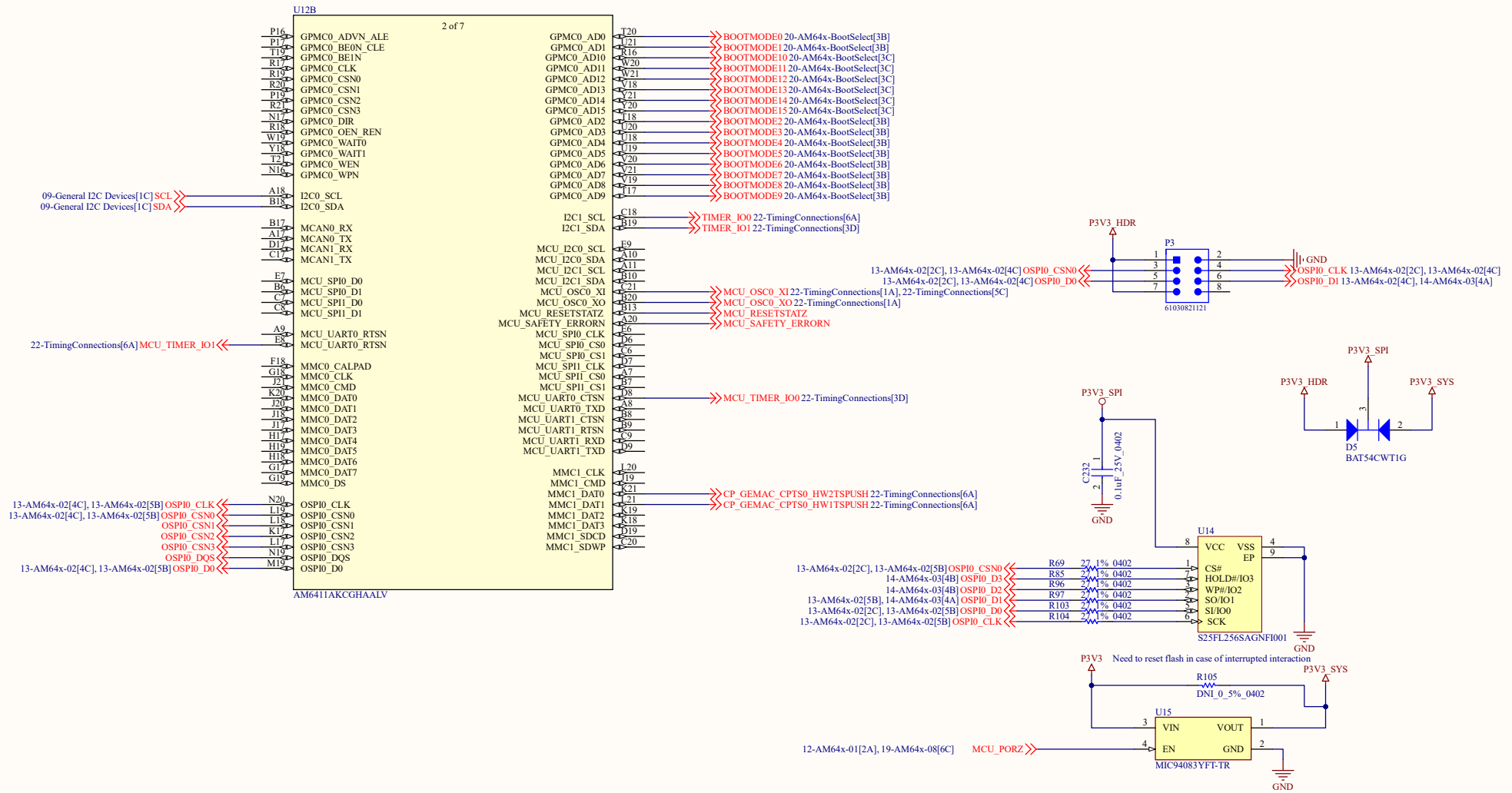
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2 of 7
AM6411AKCGHAALV
GPMC0_ADVN_ALE
GPMC0_BE0N_CLE
GPMC0_BE1N
GPMC0_CLK
GPMC0_CSN0
GPMC0_CSN1
GPMC0_CSN2
GPMC0_CSN3
GPMC0_DIR
GPMC0_OEN_REN
GPMC0_WAIT0
GPMC0_WAIT1
GPMC0_WEN
GPMC0_WPN
I2C0_SCL
I2C0_SDA
MCAN0_RX
MCAN0_TX
MCAN1_RX
MCAN1_TX
MCU_SPI0_D0
MCU_SPI0_D1
MCU_SPI1_D0
MCU_SPI1_D1
MCU_UART0_RTSN
MCU_UART0_RTSN
MMC0_CALPAD
MMC0_CLK
MMC0_CMD
MMC0_DAT0
MMC0_DAT1
MMC0_DAT2
MMC0_DAT3
MMC0_DAT4
MMC0_DAT5
MMC0_DAT6
MMC0_DAT7
MMC0_DS
OSPI0_CLK
OSPI0_CSN0
OSPI0_CSN1
OSPI0_CSN2
OSPI0_CSN3
OSPI0_DQS
OSPI0_D0
GPMC0_AD0
GPMC0_AD1
GPMC0_AD10
GPMC0_AD11
GPMC0_AD12
GPMC0_AD13
GPMC0_AD14
GPMC0_AD15
GPMC0_AD2
GPMC0_AD3
GPMC0_AD4
GPMC0_AD5
GPMC0_AD6
GPMC0_AD7
GPMC0_AD8
GPMC0_AD9
I2C1_SCL
I2C1_SDA
MCU_I2C0_SCL
MCU_I2C0_SDA
MCU_I2C1_SCL
MCU_I2C1_SDA
MCU_OSC0_XI
MCU_OSC0_XO
MCU_RESETSTATZ
MCU_SAFETY_ERRORN
MCU_SPI0_CLK
MCU_SPI0_CS0
MCU_SPI0_CS1
MCU_SPI1_CLK
MCU_SPI1_CS0
MCU_SPI1_CS1
MCU_UART0_CTSN
MCU_UART0_TXD
MCU_UART1_CTSN
MCU_UART1_RTSN
MCU_UART1_RXD
MCU_UART1_TXD
MMC1_CLK
MMC1_CMD
MMC1_DAT0
MMC1_DAT1
MMC1_DAT2
MMC1_DAT3
MMC1_SDCD
MMC1_SDWP
09-General I2C Devices[1C] SCL
09-General I2C Devices[1C] SDA
22-TimingConnections[6A] MCU_TIMER_IO1
13-AM64x-02[4C], 13-AM64x-02[5B] OSPI0_CLK
13-AM64x-02[4C], 13-AM64x-02[5B] OSPI0_CSN0
OSPI0_CSN1
OSPI0_CSN2
OSPI0_CSN3
OSPI0_DQS
13-AM64x-02[4C], 13-AM64x-02[5B] OSPI0_D0
BOOTMODE0 20-AM64x-BootSelect[3B]
BOOTMODE1 20-AM64x-BootSelect[3B]
BOOTMODE10 20-AM64x-BootSelect[3C]
BOOTMODE11 20-AM64x-BootSelect[3C]
BOOTMODE12 20-AM64x-BootSelect[3C]
BOOTMODE13 20-AM64x-BootSelect[3C]
BOOTMODE14 20-AM64x-BootSelect[3C]
BOOTMODE15 20-AM64x-BootSelect[3C]
BOOTMODE2 20-AM64x-BootSelect[3B]
BOOTMODE3 20-AM64x-BootSelect[3B]
BOOTMODE4 20-AM64x-BootSelect[3B]
BOOTMODE5 20-AM64x-BootSelect[3B]
BOOTMODE6 20-AM64x-BootSelect[3B]
BOOTMODE7 20-AM64x-BootSelect[3B]
BOOTMODE8 20-AM64x-BootSelect[3B]
BOOTMODE9 20-AM64x-BootSelect[3B]
TIMER_IO0 22-TimingConnections[6A]
TIMER_IO1 22-TimingConnections[3D]
MCU_OSC0_XI 22-TimingConnections[1A], 22-TimingConnections[5C]
MCU_OSC0_XO 22-TimingConnections[1A]
MCU_RESETSTATZ
MCU_SAFETY_ERRORN
MCU_TIMER_IO0 22-TimingConnections[3D]
CP_GEMAC_CPTS0_HW2TSPUSH 22-TimingConnections[6A]
CP_GEMAC_CPTS0_HW1TSPUSH 22-TimingConnections[6A]
P3V3_HDR
P3
61030821121
GND
13-AM64x-02[2C], 13-AM64x-02[4C] OSPI0_CSN0
13-AM64x-02[2C], 13-AM64x-02[4C] OSPI0_D0
OSPI0_CLK 13-AM64x-02[2C], 13-AM64x-02[4C]
OSPI0_D1 13-AM64x-02[4C], 14-AM64x-03[4A]
P3V3_SPI
P3V3_HDR
P3V3_SYS
D5
BAT54CWT1G
C232
0.1uF_25V_0402
U14
VCC
VSS
EP
CS#
HOLD#/IO3
WP#/IO2
SO/IO1
SI/IO0
SCK
S25FL256SAGNFI001
13-AM64x-02[2C], 13-AM64x-02[5B] OSPI0_CSN0
14-AM64x-03[4B] OSPI0_D3
14-AM64x-03[4B] OSPI0_D2
13-AM64x-02[5B], 14-AM64x-03[4A] OSPI0_D1
13-AM64x-02[2C], 13-AM64x-02[5B] OSPI0_D0
13-AM64x-02[2C], 13-AM64x-02[5B] OSPI0_CLK
R69 27_1%_0402
R85 2_1%_0402
R96 2_1%_0402
R97 2_1%_0402
R103 2_1%_0402
R104 2_1%_0402
P3V3
Need to reset flash in case of interrupted interaction
R105
DNI_0_5%_0402
U15
VIN
VOUT
EN
GND
MIC94083YFT-TR
12-AM64x-01[2A], 19-AM64x-08[6C]
MCU_PORZ
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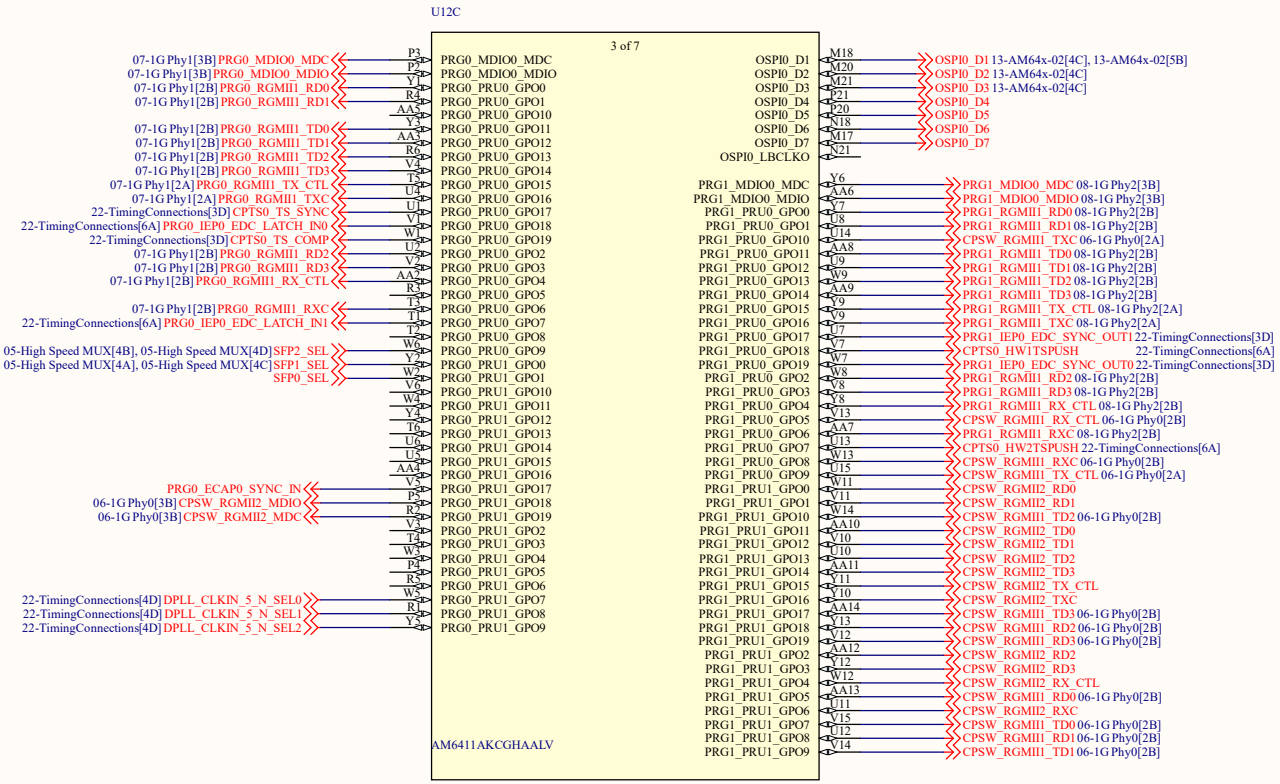

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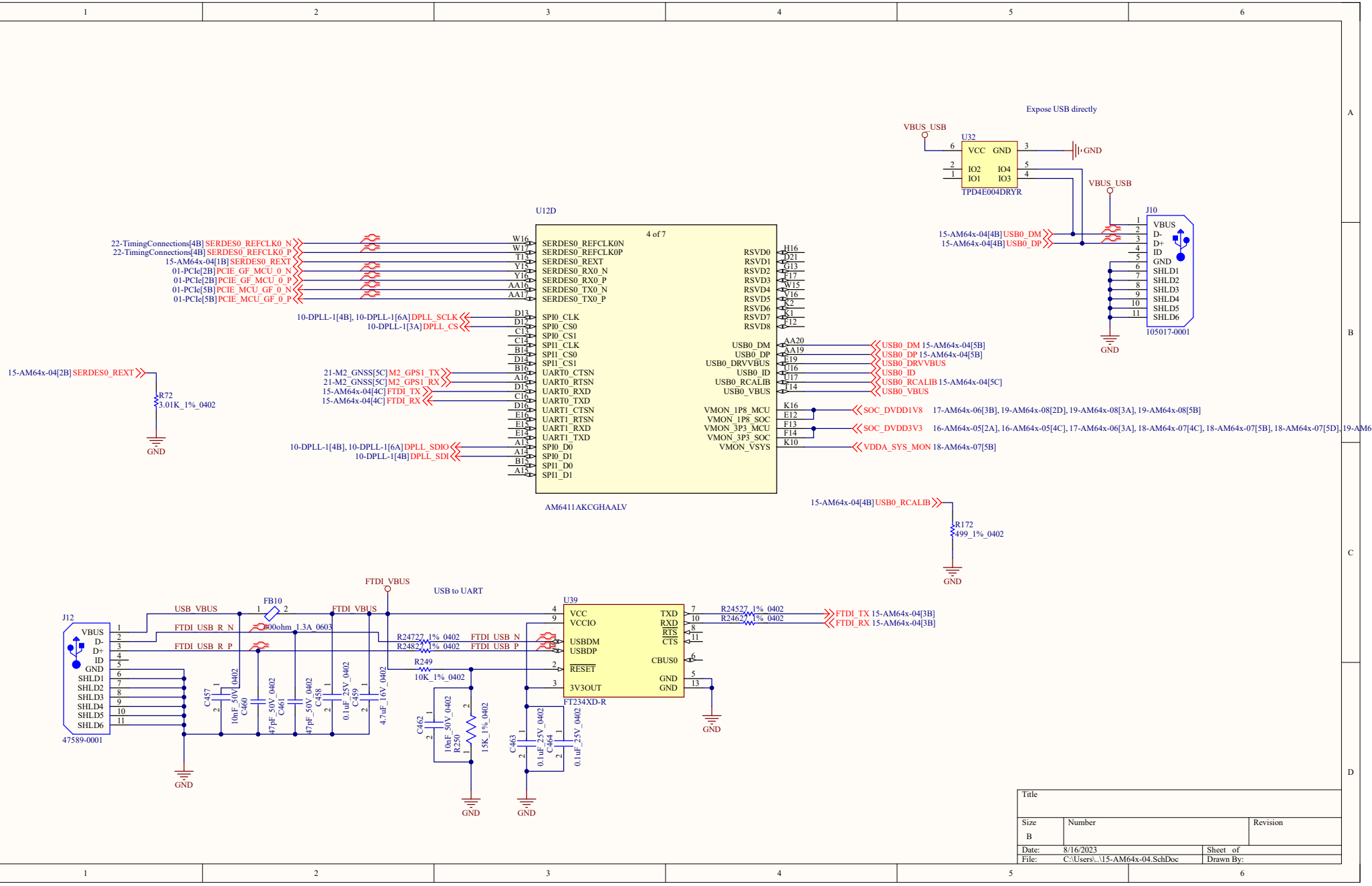
Expose USB directly
VBUS_USB
U32
VCC GND
IO2 IO4
IO1 IO3
TPD4E004DRYR
GND
J10
VBUS
D-
D+
ID
GND
SHLD1
SHLD2
SHLD3
SHLD4
SHLD5
SHLD6
105017-0001
15-AM64x-04[4B] USB0_DM
15-AM64x-04[4B] USB0_DP
U12D
4 of 7
AM6411AKCGHAALV
22-TimingConnections[4B] SERDES0_REFCLK0_N
22-TimingConnections[4B] SERDES0_REFCLK0_P
15-AM64x-04[1B] SERDES0_REXT
01-PCIe[2B] PCIE_GF_MCU_0_N
01-PCIe[2B] PCIE_GF_MCU_0_P
01-PCIe[5B] PCIE_MCU_GF_0_N
01-PCIe[5B] PCIE_MCU_GF_0_P
10-DPLL-1[4B], 10-DPLL-1[6A] DPLL_SCLK
10-DPLL-1[3A] DPLL_CS
15-AM64x-04[2B] SERDES0_REXT
R72
3.01K_1%_0402
21-M2_GNSS[5C] M2_GPS1_TX
21-M2_GNSS[5C] M2_GPS1_RX
15-AM64x-04[4C] FTDI_TX
15-AM64x-04[4C] FTDI_RX
10-DPLL-1[4B], 10-DPLL-1[6A] DPLL_SDIO
10-DPLL-1[4B] DPLL_SDI
USB0_DM 15-AM64x-04[5B]
USB0_DP 15-AM64x-04[5B]
USB0_DRVVBUS
USB0_ID
USB0_RCALIB 15-AM64x-04[5C]
USB0_VBUS
SOC_DVDD1V8 17-AM64x-06[3B], 19-AM64x-08[2D], 19-AM64x-08[3A], 19-AM64x-08[5B]
SOC_DVDD3V3 16-AM64x-05[2A], 16-AM64x-05[4C], 17-AM64x-06[3A], 18-AM64x-07[4C], 18-AM64x-07[5B], 18-AM64x-07[5D], 19-AM6
VDDA_SYS_MON 18-AM64x-07[5B]
15-AM64x-04[4B] USB0_RCALIB
R172
499_1%_0402
FTDI_VBUS
USB to UART
J12
47589-0001
USB_VBUS
FTDI_USB_R_N
FTDI_USB_R_P
FB10
600ohm_1.3A_0603
R24727_1%_0402
R24824_1%_0402
FTDI_USB_N
FTDI_USB_P
R249
10K_1%_0402
U39
VCC
VCCIO
USBDM
USBDP
RESET
3V3OUT
TXD
RXD
RTS
CTS
CBUS0
GND
FT234XD-R
R24527_1%_0402
R24624_1%_0402
FTDI_TX 15-AM64x-04[3B]
FTDI_RX 15-AM64x-04[3B]
C457 10nF_50V_0402
C460
C461 47pF_50V_0402
C458 47pF_50V_0402
C459 0.1uF_25V_0402
C459 4.7uF_16V_0402
C462 10nF_50V_0402
R250 15K_1%_0402
C463 0.1uF_25V_0402
C464 0.1uF_25V_0402
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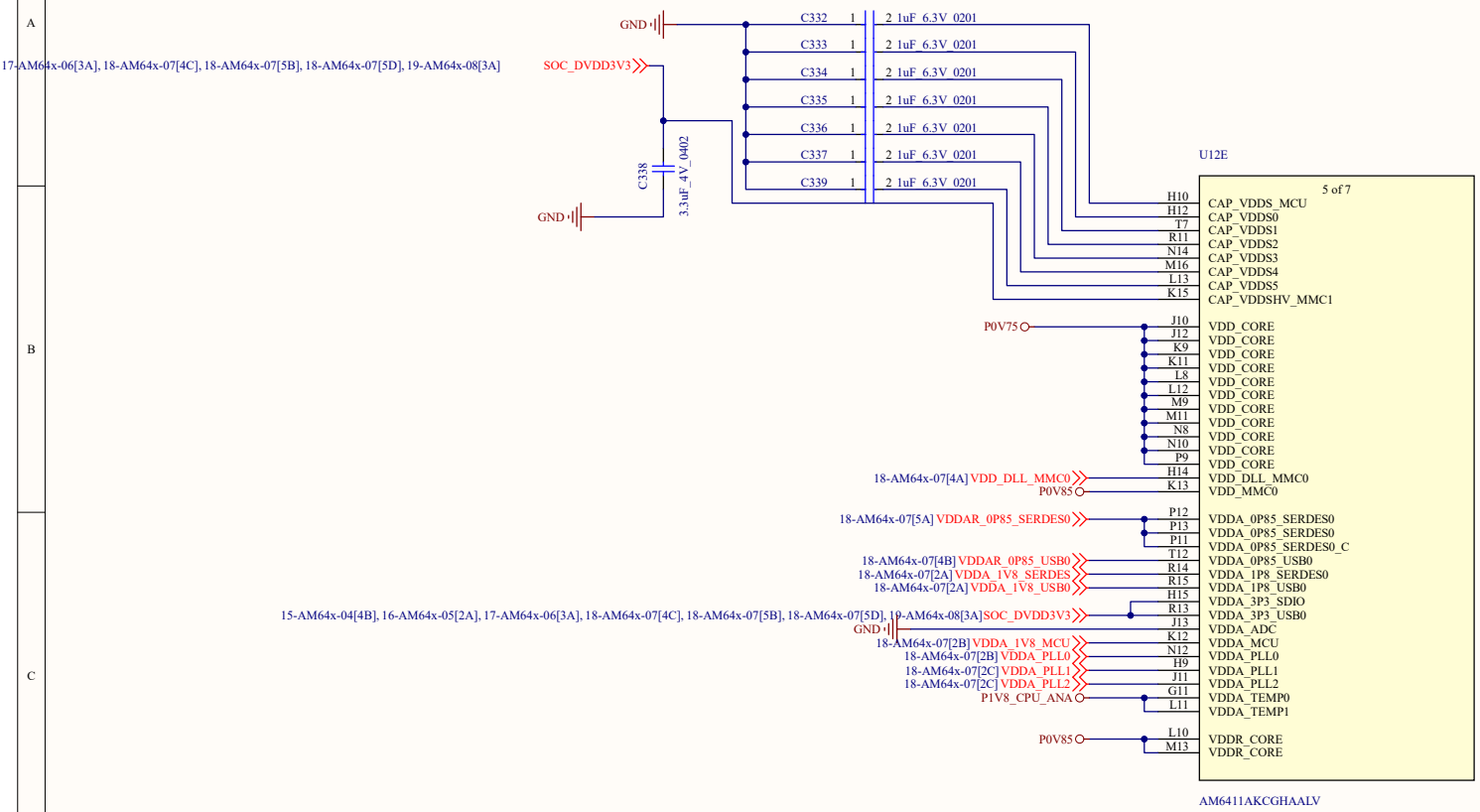

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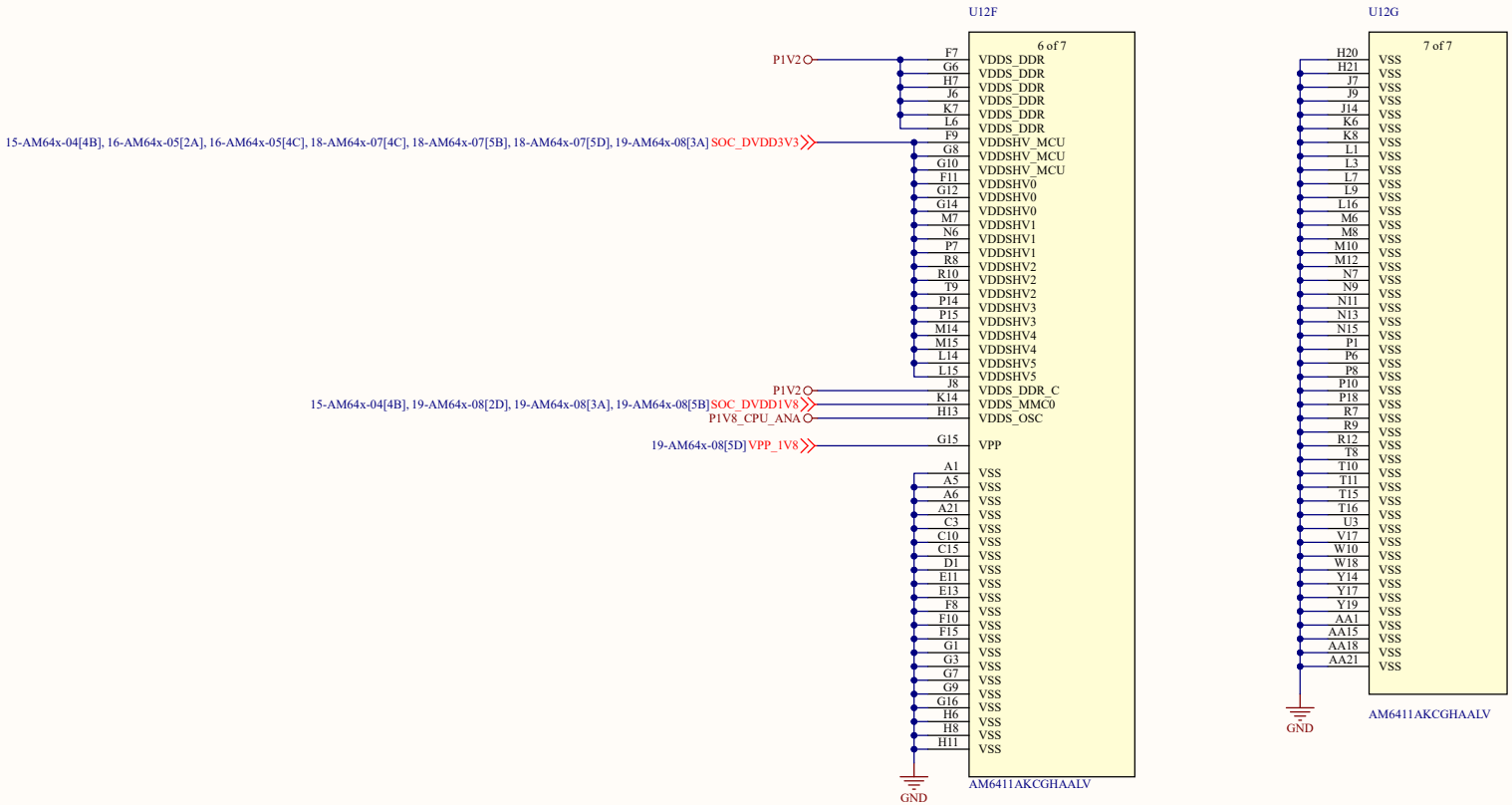

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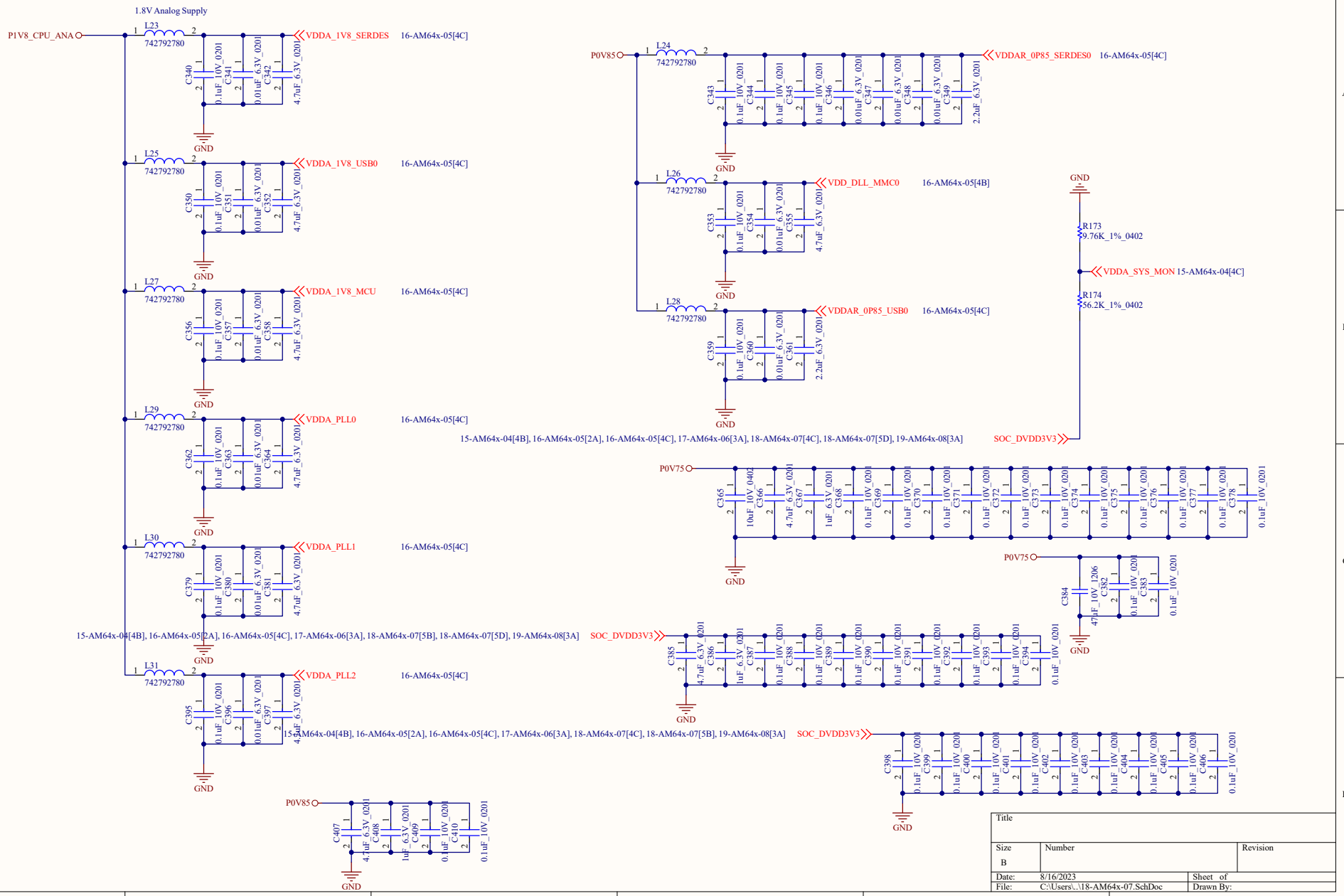
1.8V Analog Supply
P1V8_CPU_ANA
L23
742792780
VDDA_1V8_SERDES
16-AM64x-05[4C]
C340 0.1uF_10V_0201
C341 0.01uF_6.3V_0201
C342 4.7uF_6.3V_0201
GND
L25
742792780
VDDA_1V8_USB0
16-AM64x-05[4C]
C350 0.1uF_10V_0201
C351 0.01uF_6.3V_0201
C352 4.7uF_6.3V_0201
GND
L27
742792780
VDDA_1V8_MCU
16-AM64x-05[4C]
C356 0.1uF_10V_0201
C357 0.01uF_6.3V_0201
C358 4.7uF_6.3V_0201
GND
L29
742792780
VDDA_PLL0
16-AM64x-05[4C]
C362 0.1uF_10V_0201
C363 0.01uF_6.3V_0201
C364 4.7uF_6.3V_0201
GND
L30
742792780
VDDA_PLL1
16-AM64x-05[4C]
C379 0.1uF_10V_0201
C380 0.01uF_6.3V_0201
C381 4.7uF_6.3V_0201
15-AM64x-04[4B], 16-AM64x-05[2A], 16-AM64x-05[4C], 17-AM64x-06[3A], 18-AM64x-07[5B], 18-AM64x-07[5D], 19-AM64x-08[3A]
GND
L31
742792780
VDDA_PLL2
16-AM64x-05[4C]
C395 0.1uF_10V_0201
C396 0.01uF_6.3V_0201
C397 4.7uF_6.3V_0201
15-AM64x-04[4B], 16-AM64x-05[2A], 16-AM64x-05[4C], 17-AM64x-06[3A], 18-AM64x-07[4C], 18-AM64x-07[5B], 19-AM64x-08[3A]
GND
P0V85
C407 4.7uF_6.3V_0201
C408 1uF_6.3V_0201
C409 0.1uF_10V_0201
C410 0.1uF_10V_0201
GND
P0V85
L24
742792780
VDDAR_0P85_SERDES0
16-AM64x-05[4C]
C343 0.1uF_10V_0201
C344 0.1uF_10V_0201
C345 0.1uF_10V_0201
C346 0.01uF_6.3V_0201
C347 0.01uF_6.3V_0201
C348 0.01uF_6.3V_0201
C349 2.2uF_6.3V_0201
GND
L26
742792780
VDD_DLL_MMC0
16-AM64x-05[4B]
C353 0.1uF_10V_0201
C354 0.01uF_6.3V_0201
C355 4.7uF_6.3V_0201
GND
L28
742792780
VDDAR_0P85_USB0
16-AM64x-05[4C]
C359 0.1uF_10V_0201
C360 0.01uF_6.3V_0201
C361 2.2uF_6.3V_0201
GND
GND
R173
9.76K_1%_0402
VDDA_SYS_MON
15-AM64x-04[4C]
R174
56.2K_1%_0402
15-AM64x-04[4B], 16-AM64x-05[2A], 16-AM64x-05[4C], 17-AM64x-06[3A], 18-AM64x-07[4C], 18-AM64x-07[5D], 19-AM64x-08[3A]
SOC_DVDD3V3
P0V75
C365 10uF_10V_0402
C366 4.7uF_6.3V_0201
C367 1uF_6.3V_0201
C368 0.1uF_10V_0201
C369 0.1uF_10V_0201
C370 0.1uF_10V_0201
C371 0.1uF_10V_0201
C372 0.1uF_10V_0201
C373 0.1uF_10V_0201
C374 0.1uF_10V_0201
C375 0.1uF_10V_0201
C376 0.1uF_10V_0201
C377 0.1uF_10V_0201
C378 0.1uF_10V_0201
GND
P0V75
C384 47uF_10V_1206
C382 0.1uF_10V_0201
C383 0.1uF_10V_0201
GND
SOC_DVDD3V3
C385 4.7uF_6.3V_0201
C386 1uF_6.3V_0201
C387 0.1uF_10V_0201
C388 0.1uF_10V_0201
C389 0.1uF_10V_0201
C390 0.1uF_10V_0201
C391 0.1uF_10V_0201
C392 0.1uF_10V_0201
C393 0.1uF_10V_0201
C394 0.1uF_10V_0201
GND
SOC_DVDD3V3
C398 0.1uF_10V_0201
C399 0.1uF_10V_0201
C400 0.1uF_10V_0201
C401 0.1uF_10V_0201
C402 0.1uF_10V_0201
C403 0.1uF_10V_0201
C404 0.1uF_10V_0201
C405 0.1uF_10V_0201
C406 0.1uF_10V_0201
GND
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7.10.2.2.1 Power-Up Sequencing

Figure 7-5 describes the device power-up sequencing.

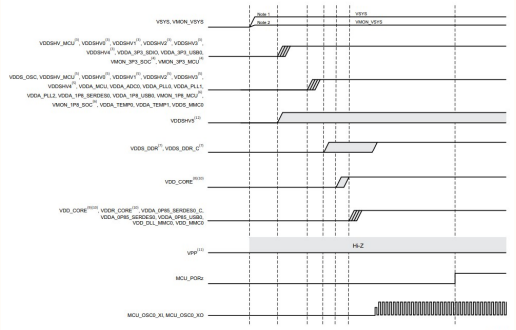

Figure 7-5. Power-Up Sequencing

P3V3 — FB8 — SOC_DVDD3V3 — ILHB1812ER121V

15-AM64x-04[4B], 16-AM64x-05[2A], 16-AM64x-05[4C], 17-AM64x-06[3A], 18-AM64x-07[4C], 18-AM64x-07[5B], 18-AM64x-07[5D]

P1V8 — FB9 — SOC_DVDD1V8 — ILHB1812ER121V

15-AM64x-04[4B], 17-AM64x-06[3B], 19-AM64x-08[2D], 19-AM64x-08[5B]

P3V3: C411 4.7uF_6.3V_0201, C412 0.1uF_10V_0201 — GND

P1V2: C413 10uF_10V_0402, C414 4.7uF_6.3V_0201, C415 1uF_6.3V_0201, C416 0.1uF_10V_0201, C417 0.1uF_10V_0201 — GND

P1V8_CPU_ANA: C418 4.7uF_6.3V_0201, C419 0.1uF_10V_0201, C420 0.1uF_10V_0201, C421 0.1uF_10V_0201, C422 0.1uF_10V_0201 — GND

15-AM64x-04[4B], 17-AM64x-06[3B], 19-AM64x-08[2D], 19-AM64x-08[3A] — SOC_DVDD1V8: C423 4.7uF_6.3V_0201, C424 0.1uF_10V_0201, C425 0.1uF_10V_0201, C426 0.1uF_10V_0201, C427 0.1uF_10V_0201, C428 0.1uF_10V_0201 — GND

25-Power-CPU[3C] P1V8_EN — R175 0_5%_0402 — P3V3_PG 24-Power-P3V3_P1V8DPLL[4B]

25-Power-CPU[4C] P1V8_CPU_ANA_EN — R176 0_5%_0402

25-Power-CPU[1C] P1V2_EN — R177 0_5%_0402 — P1V8_CPU_ANA_PG 25-Power-CPU[5D], 25-Power-CPU[6B]

25-Power-CPU[2A] P0V75_EN — R178 0_5%_0402 — P1V2_PG 19-AM64x-08[2C]

25-Power-CPU[4B] P0V85_EN — R179 0_5%_0402 — P0V75_PG 25-Power-CPU[4B]

01-PCIe[5A], 06-1G Phy0[3B], 07-1G Phy1[3B], 08-1G Phy2[3B], 09-General I2C Devices[1C], 10-DPLL-1[2B], 21-M2_GNSS[3D], 21-M2_GNSS[5C] — PCIE_PERST

P3V3: C429 0.1uF_10V_0201; U33B SN74LVC1G08DBVR (VCC, GND) — GND

P1V2: R183 0_5%_0402; R184 DNI_0_5%_0402; C431 0.1uF_10V_0201; U35 ADM1085AKSZ-REEL7 (VCC, VIN, ENOUT, CEXT, ENIN, GND); R182 4.7K_1%_0402; C433 100pF_50V_0402 — GND

1.2V has no power good, use monitor circuit to sequence after

P1V2_PG 19-AM64x-08[2B]

Hold CPU Reset longer than PCIe reset and after power up, let DPLL come up, say 50ms

25-Power-CPU[5D], 25-Power-CPU[6C] P0V85_PG — U33A SN74LVC1G08DBVR

P3V3: C430 0.1uF_10V_0201; U34 ADM1085AKSZ-REEL7 (VCC, VIN, ENOUT, CEXT, ENIN, GND); R181 4.7K_1%_0402; R180 0_5%_0402; C432 10nF_50V_0402 — GND

MCU_RESETZ 12-AM64x-01[2A]

MCU_PORZ — 12-AM64x-01[2A], 13-AM64x-0

P1V2: C434 NFM15PC104D0J3D, C435 NFM15PC104D0J3D, C436 NFM15PC104D0J3D — GND

P1V8: J11 87898-0204; VPP GND except by header; 17-AM64x-06[3B] VPP_1V8; R185 4.7K_1%_0402 — GND

15-AM64x-04[4B], 17-AM64x-06[3B], 19-AM64x-08[3A], 19-AM64x-08[5B] — SOC_DVDD1V8

DNI_0_5%_0402 R186

12-AM64x-01[2B] ADC0_VREFP — 0_5%_0402 R187 — GND

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This design is intended for embedded use case, QSPI is intended boot source

4.3 Boot Mode Pins

Boot Mode pins provide means to select the boot mode and options before the device is powered up. After every POR, they are the main source to populate the Boot Parameter Tables. See Section 4.6, *Boot Parameter Tables* for table list and description.

Boot mode pins can be divided into the following categories:

- **BOOTMODE[02:00]** – Denote system clock frequency (MCU_OSC0_XI/XO) to ROM code for PLL configuration.
- **BOOTMODE[06:03]** – Select the requested boot (primary) mode after POR, that is, the peripheral/memory to boot from.
- **BOOTMODE[09:07]** – These pins provide optional configurations for primary boot and are used in conjunction with the boot mode selected.
- **BOOTMODE[12:10]** – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.
- **BOOTMODE[13]** – This pin provides optional configurations for the backup boot devices.
- **BOOTMODE[15:14]** – Reserved pins.

Table 4-3. PLL Reference Clock Selection

PLL Config Pins			Ref Clock (MHz)
B2	B1	B0	
0	1	1	25

Note

All BOOTMODE[15:00] signals must be pulled high through a resistor to VDDSHV3, or pulled low to ground, including Reserved signals. Reserved BOOTMODE signals must not be left floating.

Table 4-4. Primary Boot Mode Selection

Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Reserved	Reserved	Reserved	0	0	0	0	Reserved
Reserved	Iclk	Csel	0	0	0	1	OSPI
Reserved	Iclk	Csel	0	0	1	0	QSPI
Reserved	Mode	Csel	0	0	1	1	SPI
Clkout	0	Link Info	0	1	0	0	Ethernet RGMII
Clkout	Clk src	0	0	1	0	1	Ethernet RMII
Bus reset	Reserved	Addr	0	1	1	0	I2C
Reserved	Reserved	Reserved	0	1	1	1	UART
Port	Reserved	Fs/raw	1	0	0	0	MMCSD Boot (SD Card Boot or eMMC Boot using UDA)

Table 4-4. Primary Boot Mode Selection (continued)

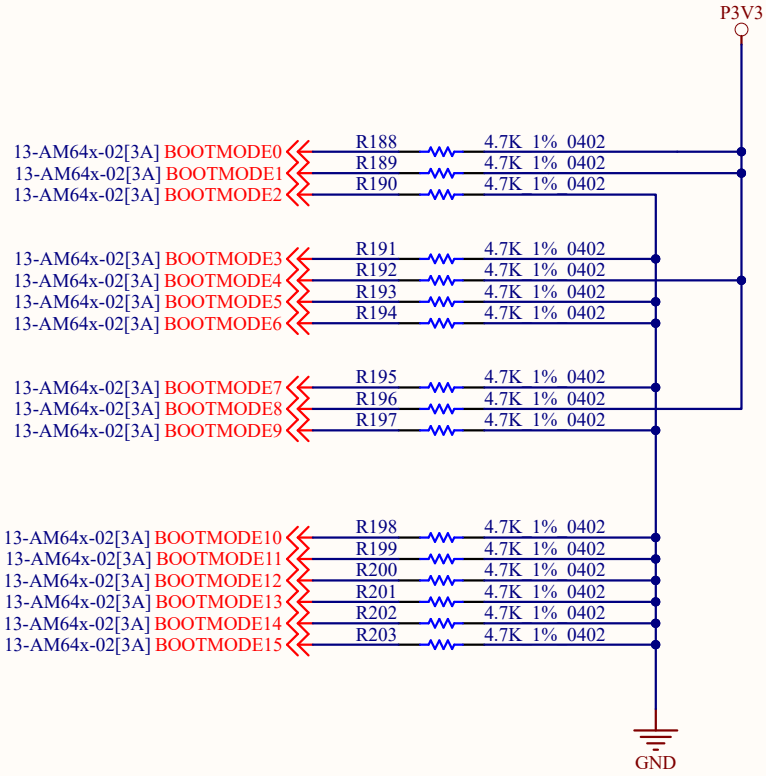
Primary Boot Mode Config							Primary Boot Mode
B9	B8	B7	B6	B5	B4	B3	
Reserved	Reserved	Reserved	1	0	0	1	eMMC Boot
Core Volt	Mode	Lane Swap	1	0	1	0	USB
Reserved	Reserved	Reserved	1	0	1	1	GPMC NAND
Reserved	Reserved	Reserved	1	1	0	0	GPMC NOR
Reserved	Reserved	Clocking	1	1	0	1	PCIe
SFPD	Read Cmd	Mode	1	1	1	0	xSPI
Reserved	Reserved	No/Dev	1	1	1	1	No-boot/Dev boot

4.3.1.2 Backup Boot Mode Selection and Configuration

The backup boot mode is selected via pins within the main BOOTMODE map. Table 4-5 lists all possible backup boot modes.

Table 4-5. Backup Mode Selection

Backup Boot Config	Backup Boot Mode Selection			Backup Boot Mode Selected
B13	B12	B11	B10	
Reserved	0	0	0	None
Mode	0	0	1	USB
Reserved	0	1	0	Reserved
Reserved	0	1	1	UART
IF	1	0	0	Ethernet
Port	1	0	1	MMCSD Boot (SD Card Boot or eMMC Boot)
Reserved	1	1	0	SPI
Reserved	1	1	1	I2C



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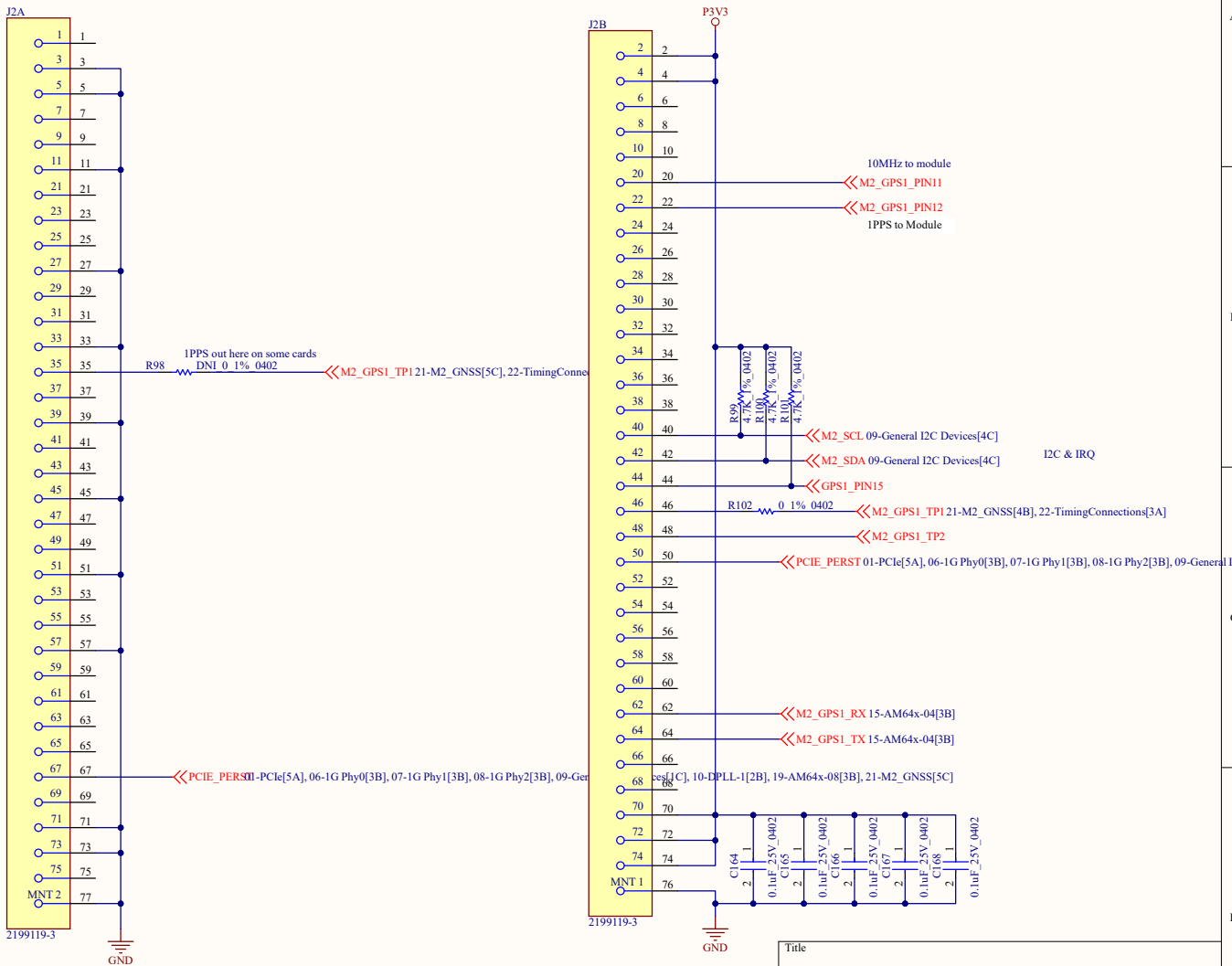
Socket 2 Key B PCIe-based WWAN Adapter Pinout , table 3-21 in M.2 spec



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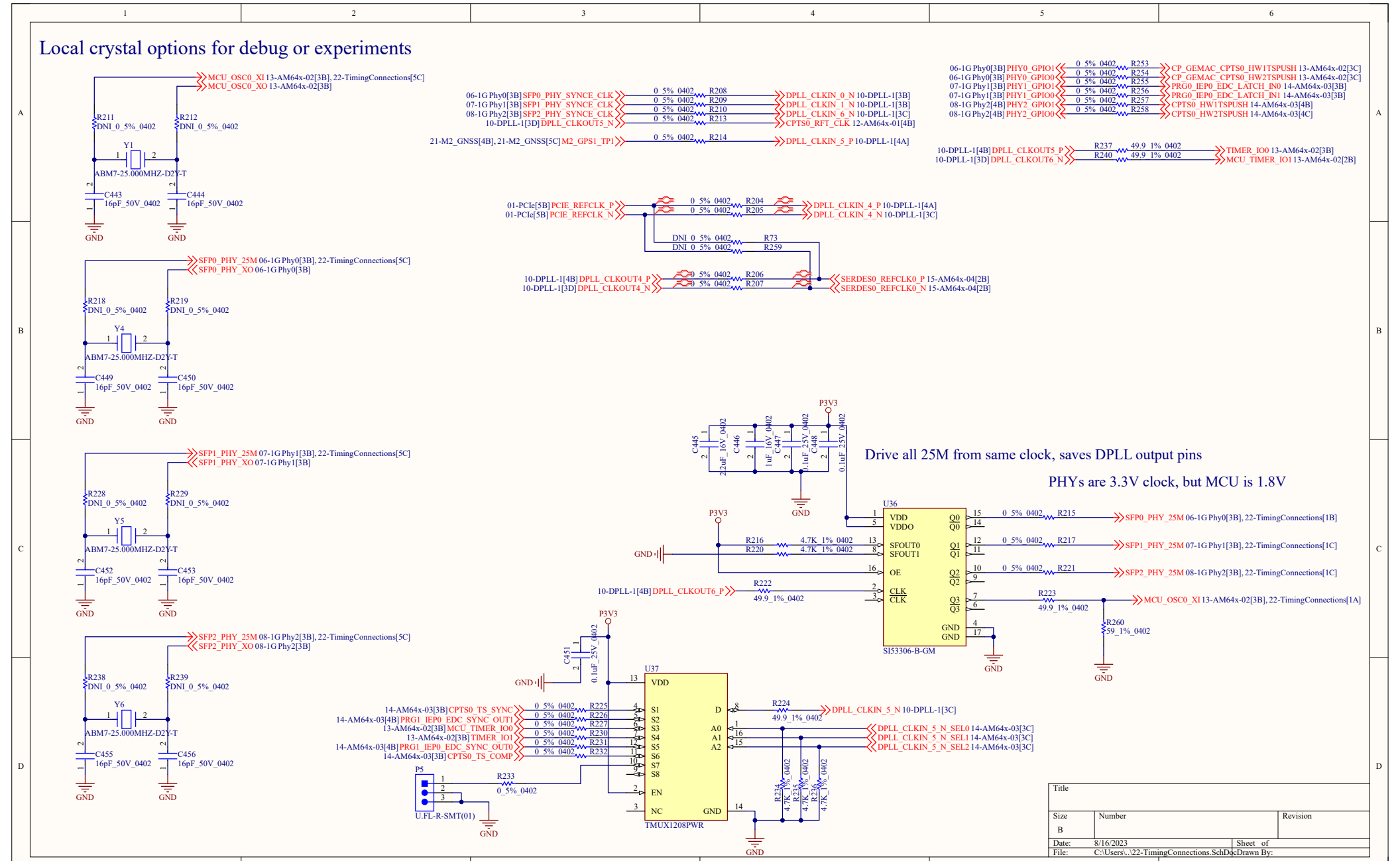
Local crystal options for debug or experiments



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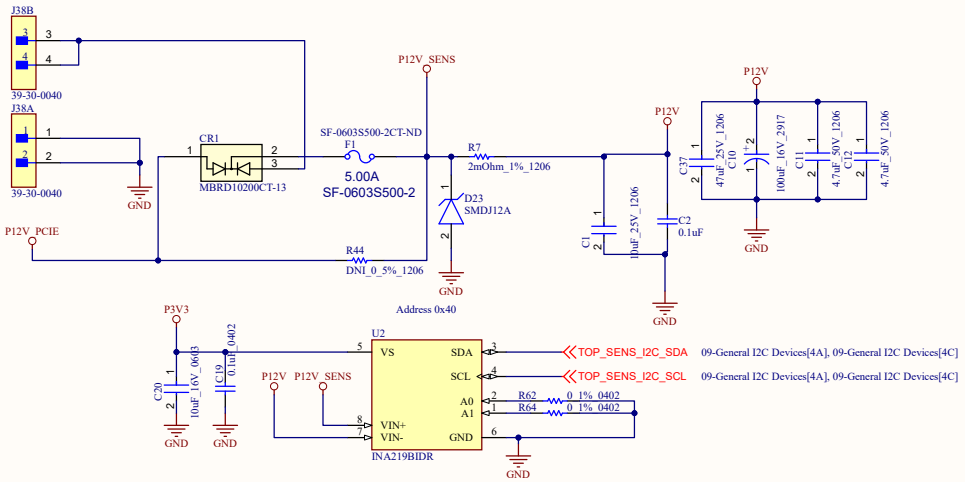
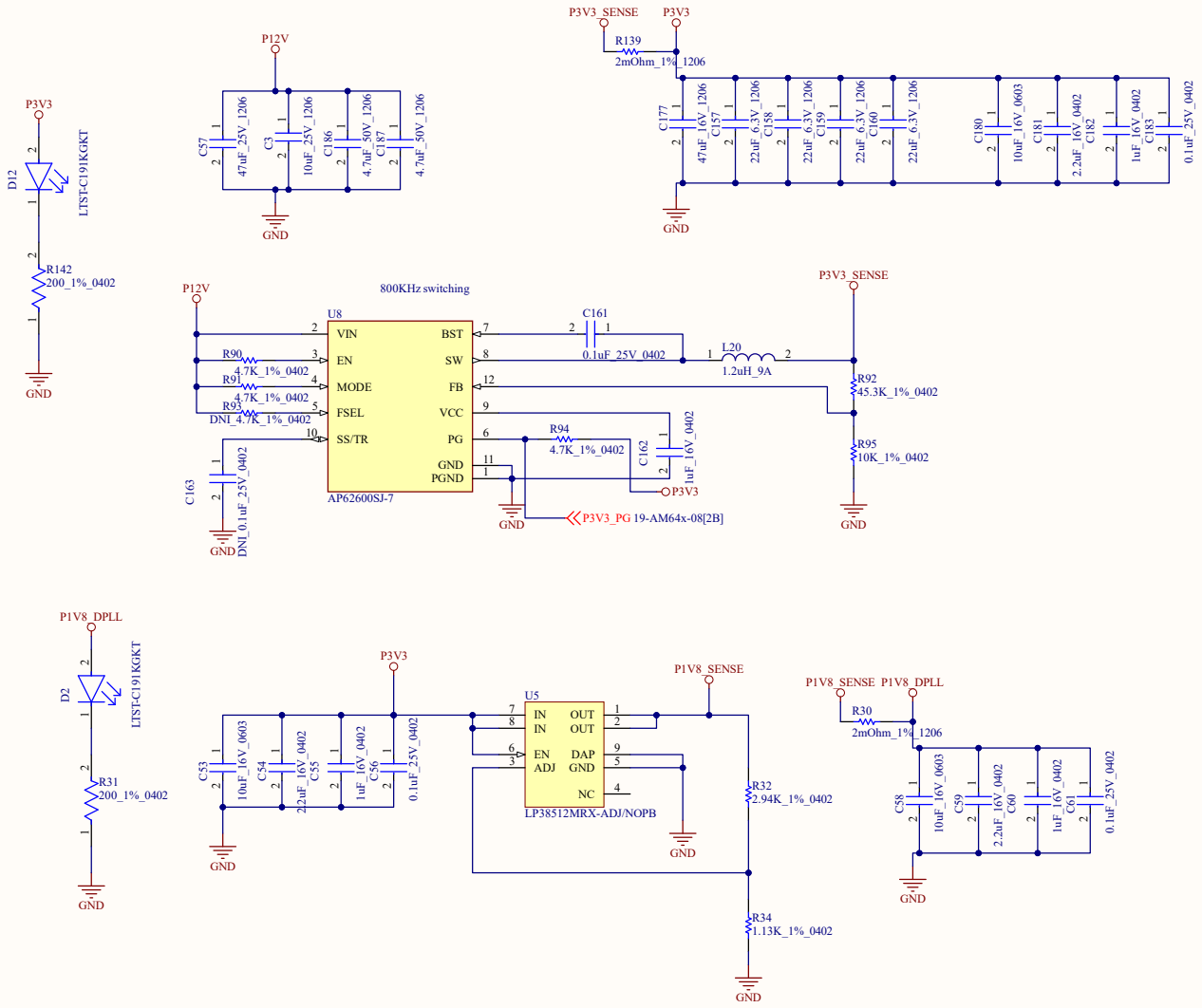


Cannot open file C:\Users\beta\Desktop\Timecard Logo\TIMECARD.jpg. File does not exist.

REV P3 DATE 09/14/21

timingcard.com

SHEET 23 OF 25



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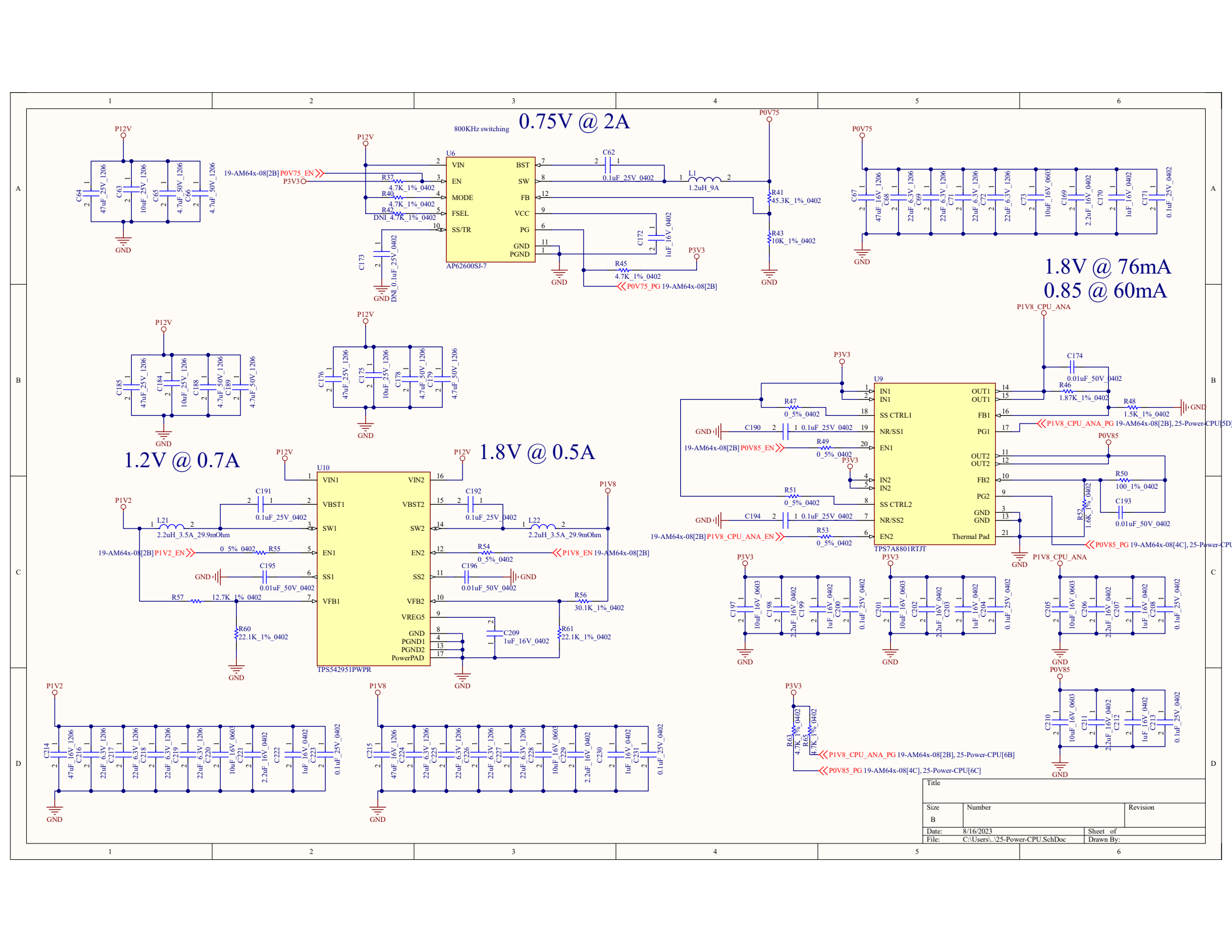
0.75V @ 2A
800KHz switching
1.8V @ 76mA
0.85 @ 60mA
1.2V @ 0.7A
1.8V @ 0.5A
U6
AP62600SJ-7
U9
TPS7A8801RTJT
U10
TPS542951PWPR
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