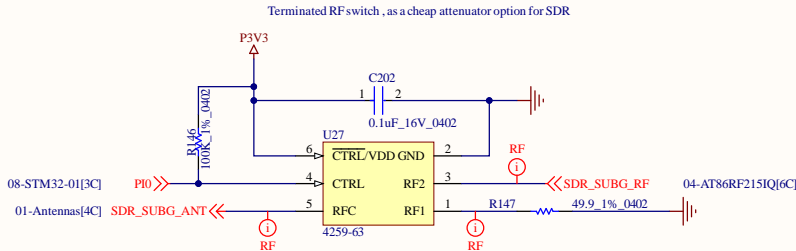
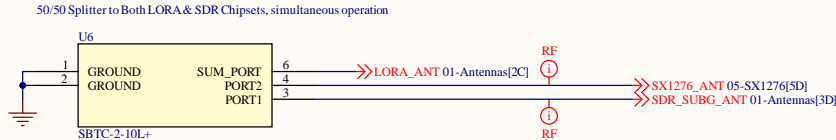
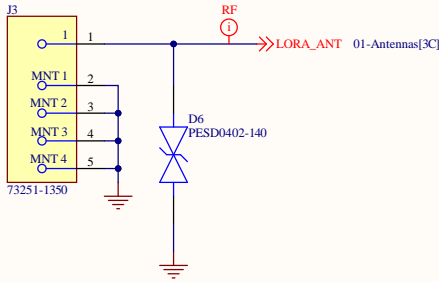
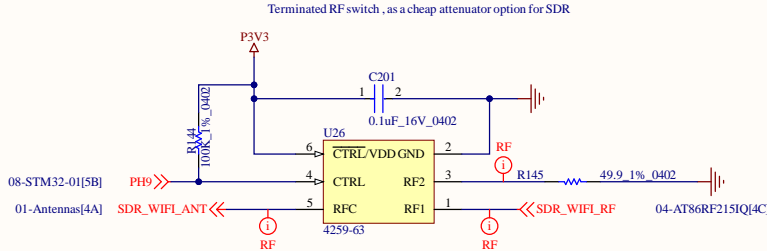
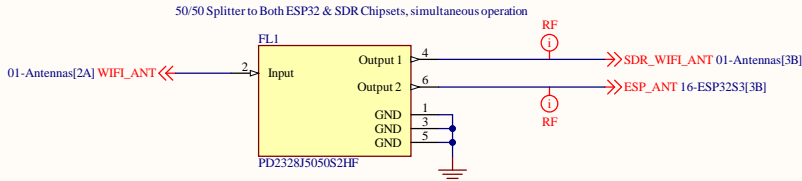
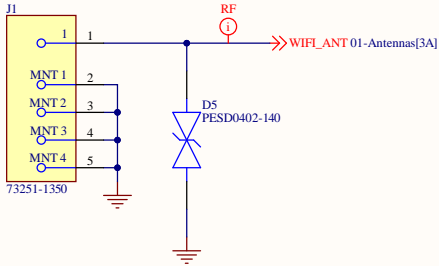
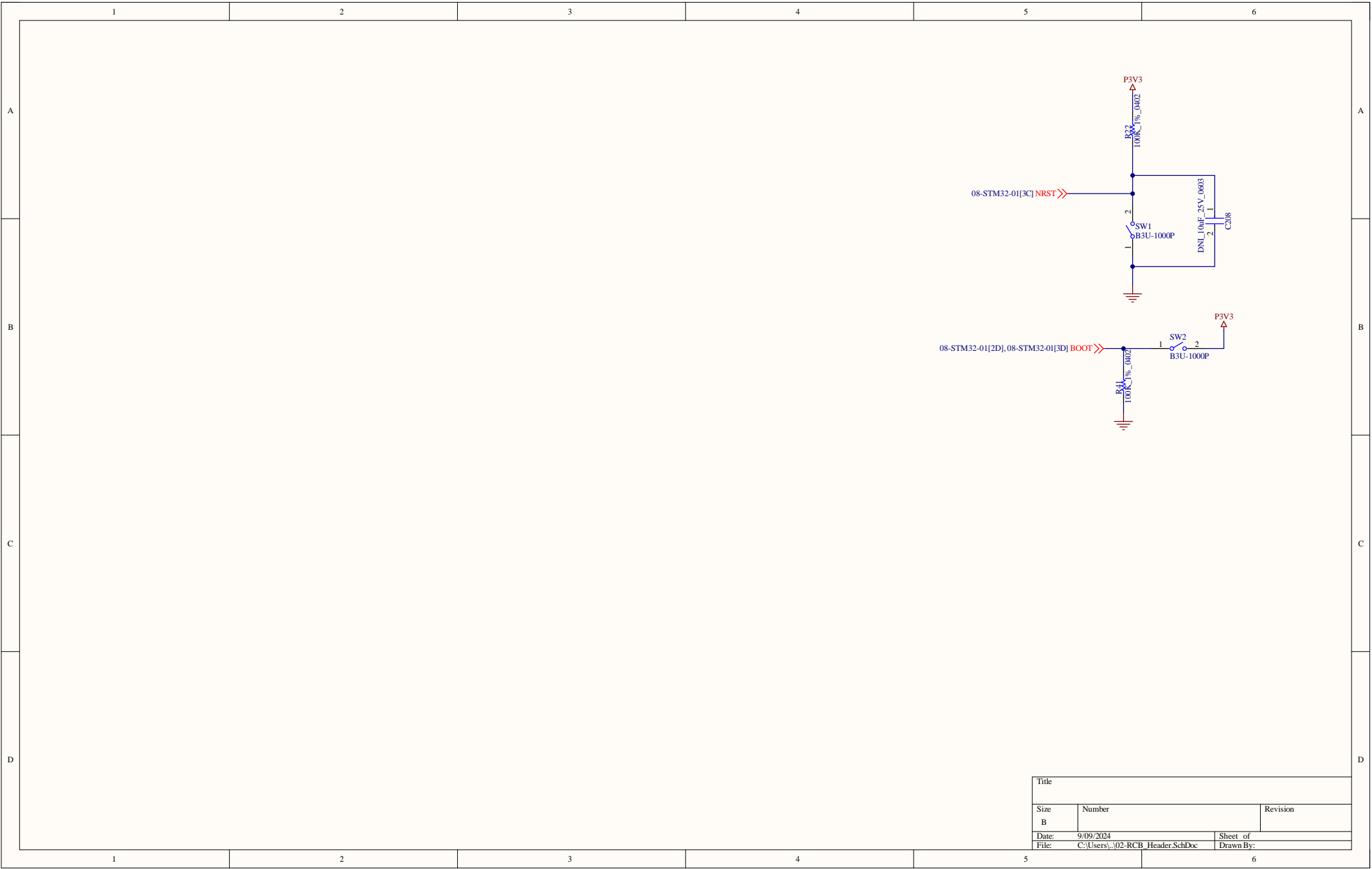


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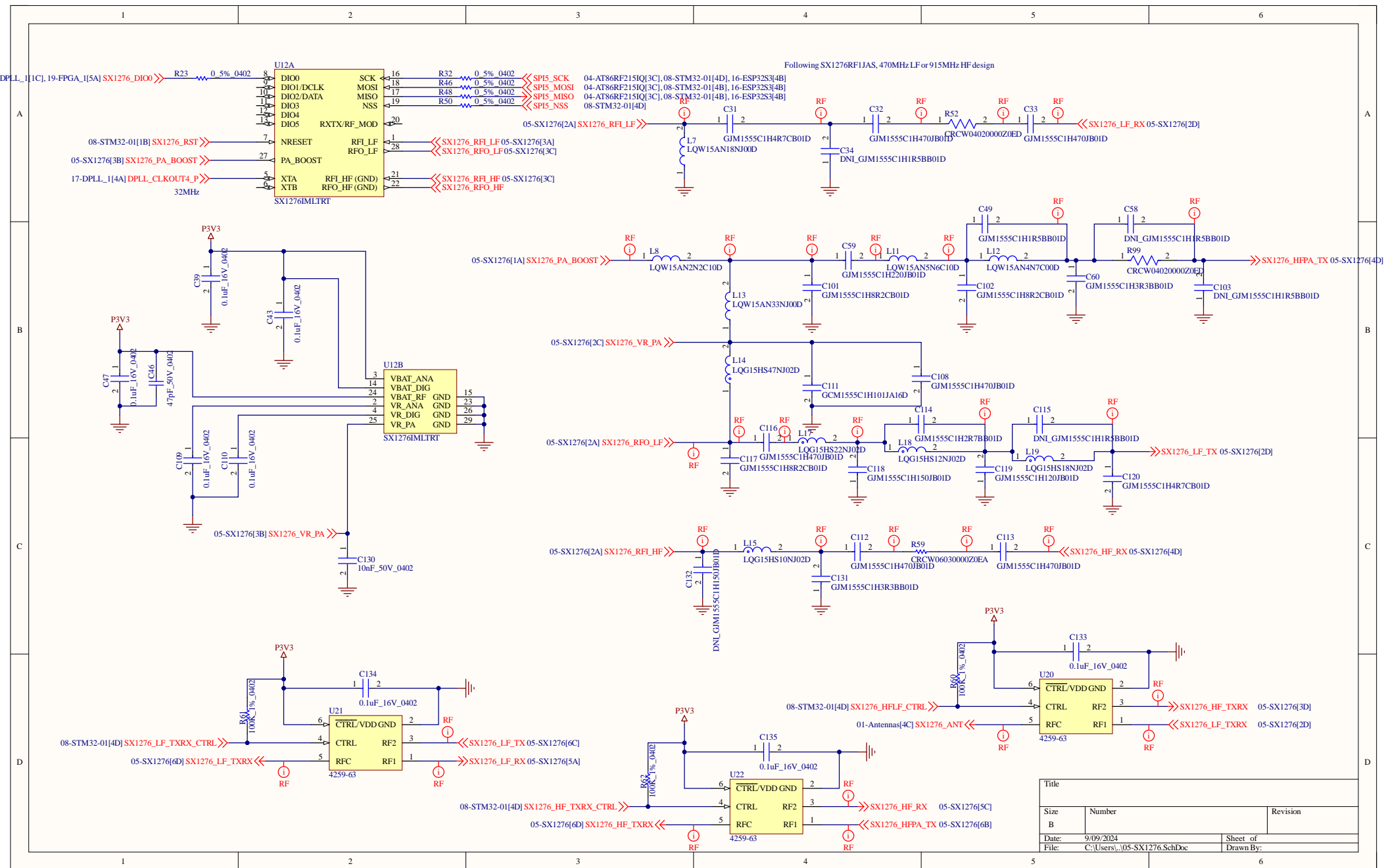
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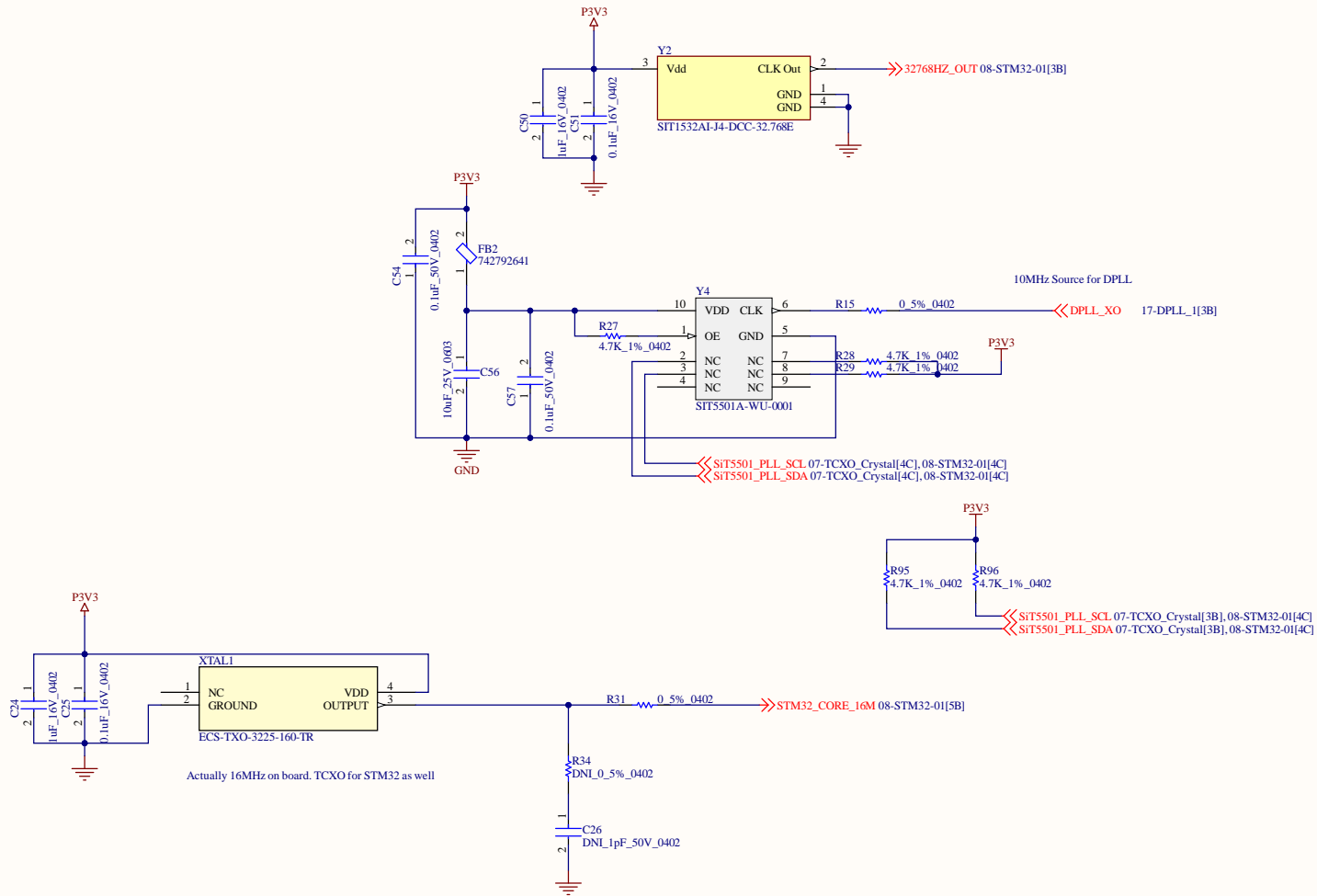


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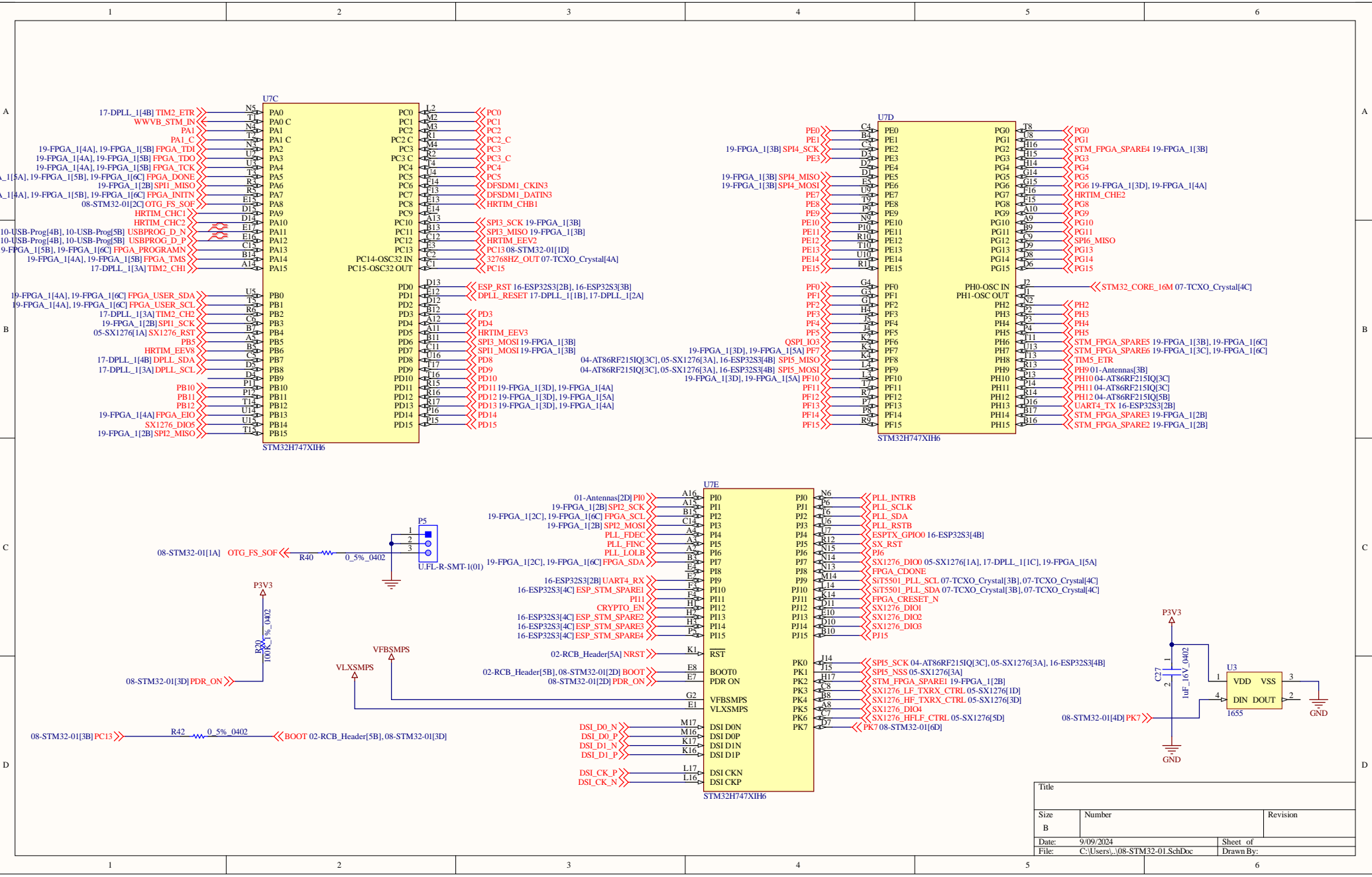
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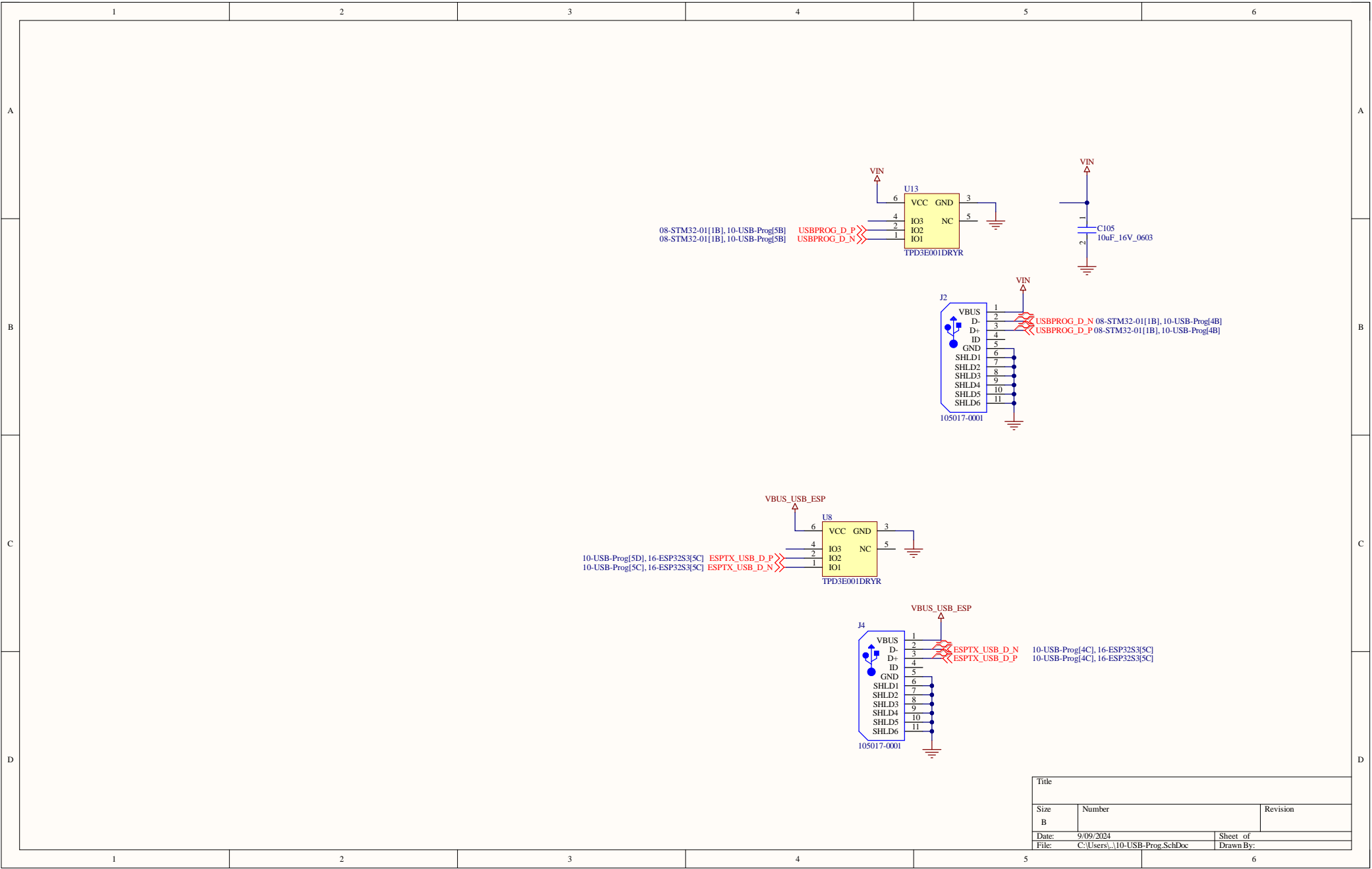
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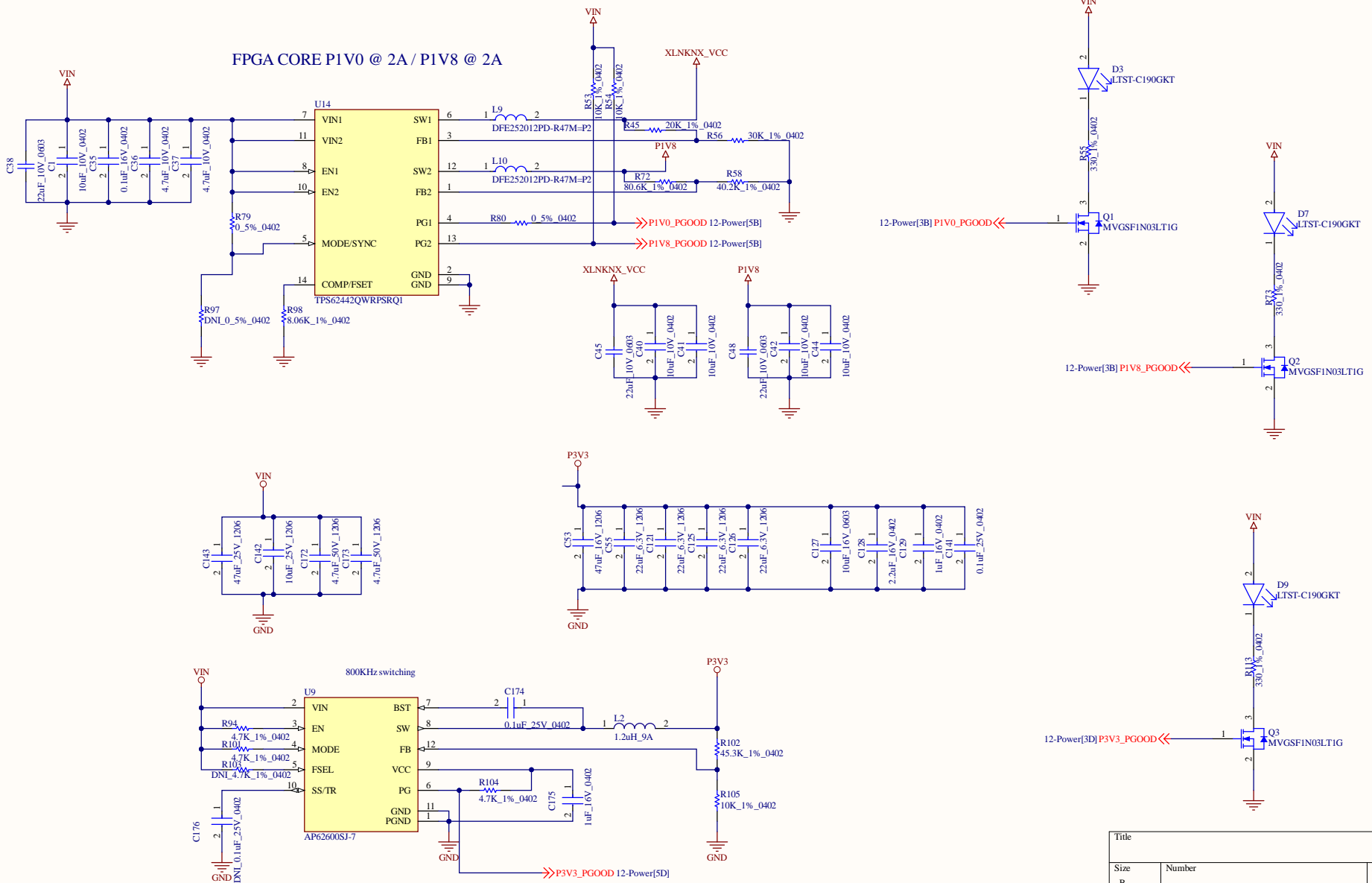




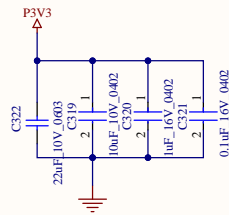


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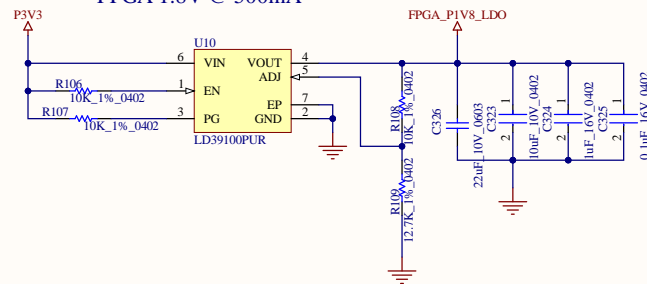
# FPGA CORE P1V0 @ 2A / P1V8 @ 2A



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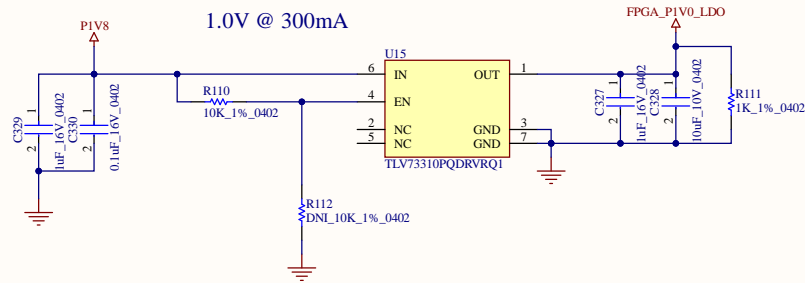


### FPGA 1.8V @ 500mA



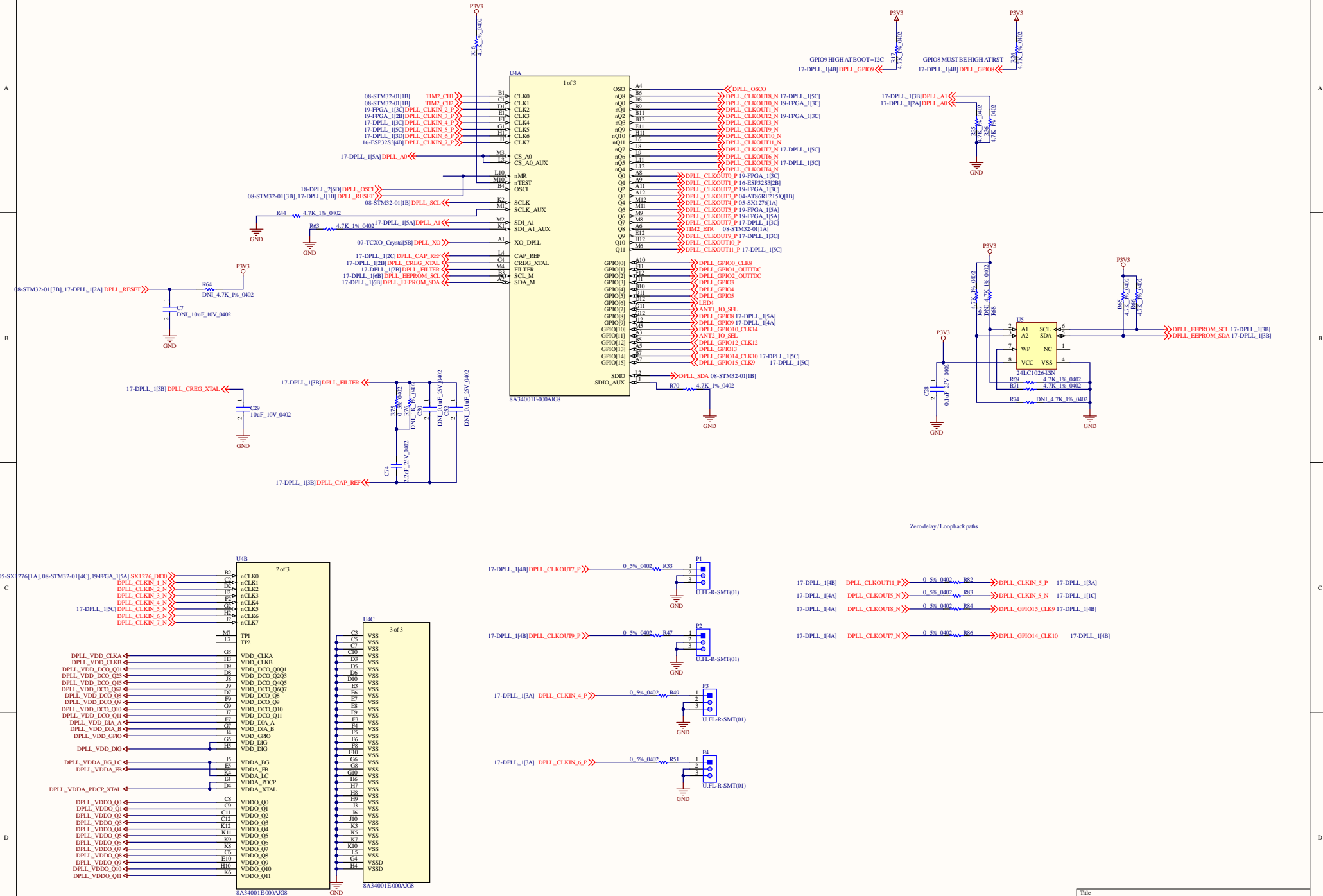
### Analog VCCA 1.0 V Power for DPHY and Serdes

#### 1.0V @ 300mA



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