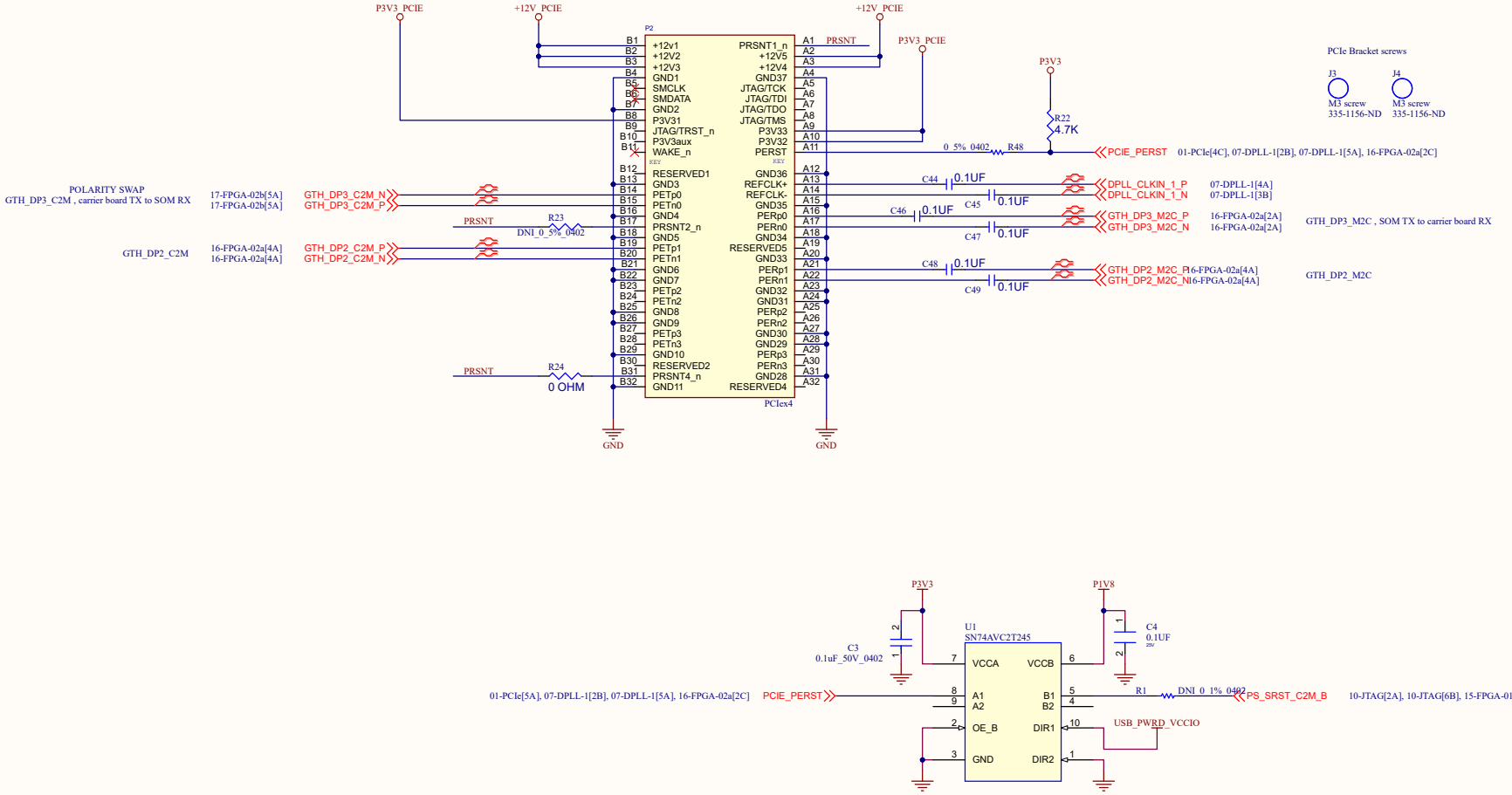
PCIe Connector



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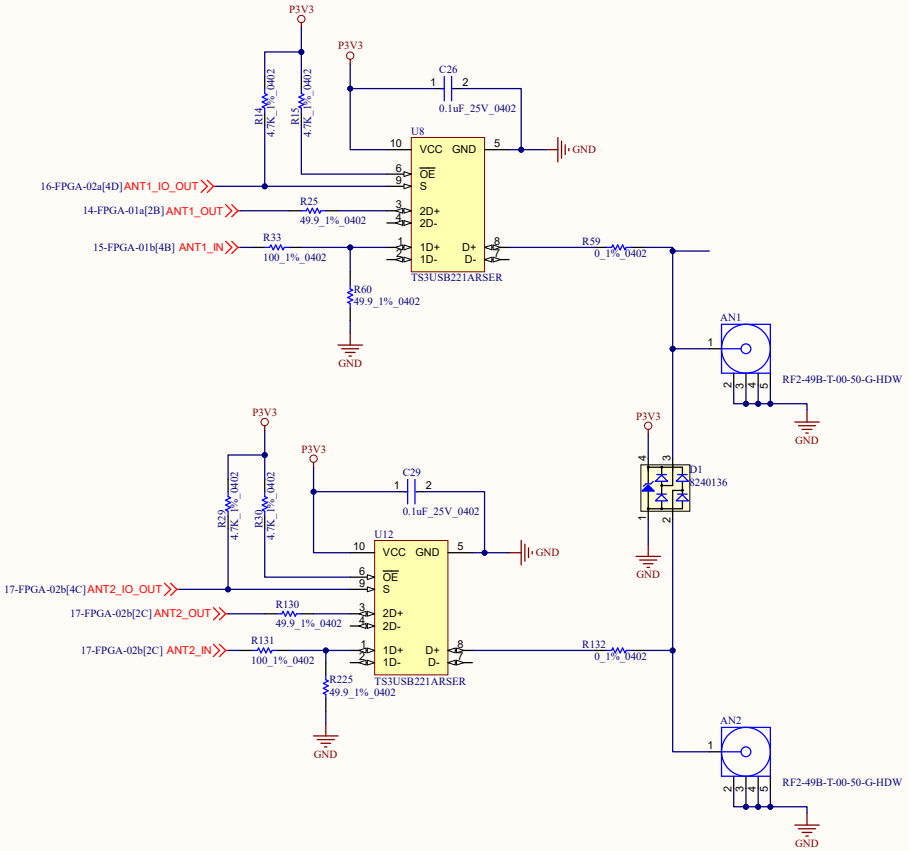
REV P3 DATE 09/14/21

timingcard.com

SHEET 1 OF 20

INPUT/OUTPUT SMA



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DATE	09/14/21

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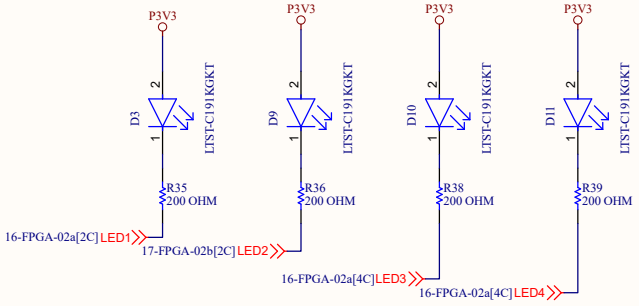
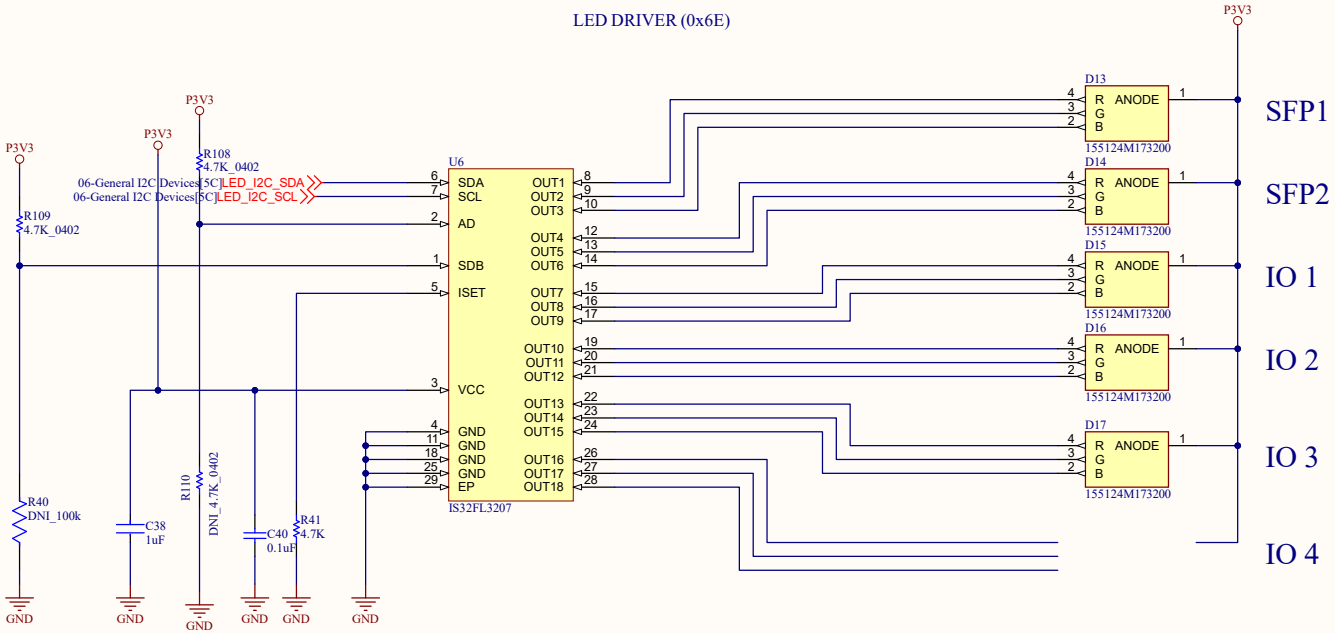
SHEET 2 OF 20

SYSTEM STATUS LEDS



IO STATUS LEDS

LED DRIVER (0x6E)



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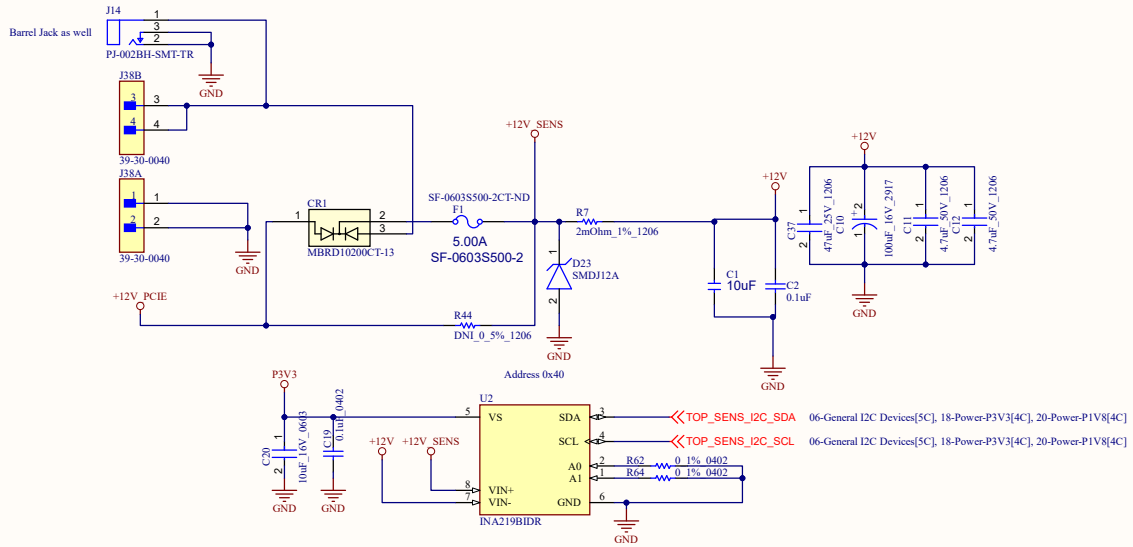

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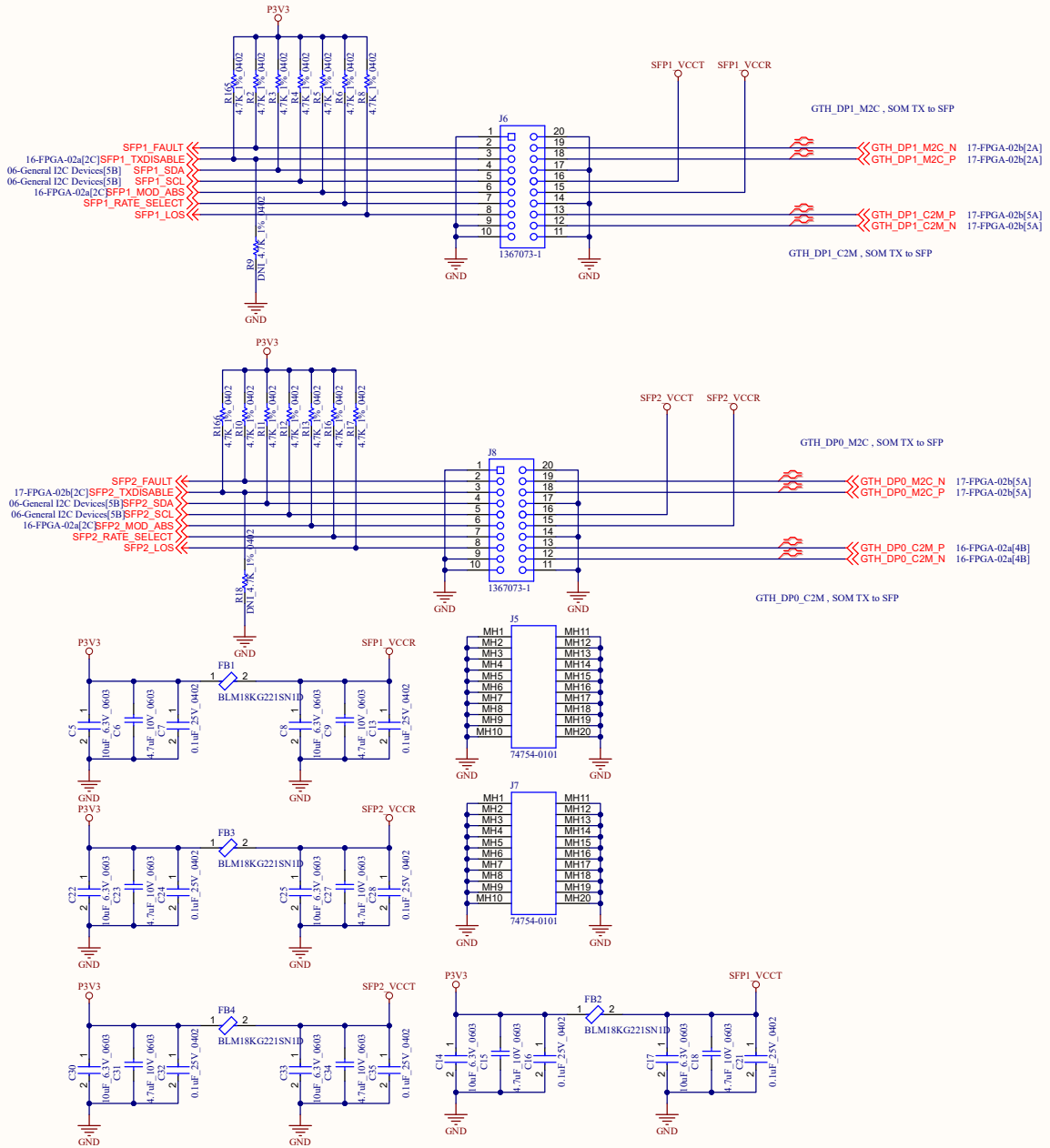
SHEET 4 OF 20



Published SFF-8419 Rev 1.3

TABLE 2 SFP+ MODULE AND HOST ELECTRICAL CONTACT DEFINITION

Contacts	Logic 1 *1	Symbol	Power Sequence Order	Name/Description	Note
case		case	*2	Module case	
1		VeeT	1st	Module Transmitter Ground	*3
2	LVTTL-O	Tx_Fault	3rd	Module Transmitter Fault	*4
3	LVTTL-I	Tx_Disable	3rd	Transmitter Disable; Turns off transmitter laser output	*5
4	LVTTL-I/O	SDA	3rd	2-wire Serial Interface Data Line (Same as MOD-DEF2 in INF-8074i)	*6
5	LVTTL-I/O	SCL	3rd	2-wire Serial Interface Clock (Same as MOD-DEF1 in INF-8074i)	*6
6		Mod_ABS	3rd	Module Absent, connected to VeeT or VeeR in the module	*7
7	LVTTL-I	RS0	3rd	Rate Select 0, optionally controls SFP+ module receiver.	*8
8	LVTTL-O	Rx_LOS	3rd	Receiver Loss of Signal Indication (In FC designated as Rx_LOS and in Ethernet designated as Signal Detect)	*4
9	LVTTL-I	RS1	3rd	Rate Select 1, optionally controls SFP+ module transmitter	*8
10		VeeR	1st	Module Receiver Ground	*3
11		VeeR	1st	Module Receiver Ground	*3
12	CML-O	RD-	3rd	Receiver Inverted Data Output	
13	CML-O	RD+	3rd	Receiver Non-Inverted Data Output	
14		VeeR	1st	Module Receiver Ground	*3
15		VccR	2nd	Module Receiver 3.3 V Supply	
16		VccT	2nd	Module Transmitter 3.3 V Supply	
17		VeeT	1st	Module Transmitter Ground	*3
18	CML-I	TD+	3rd	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	3rd	Transmitter Inverted Data Input	
20		VeeT	1st	Module Transmitter Ground	*3

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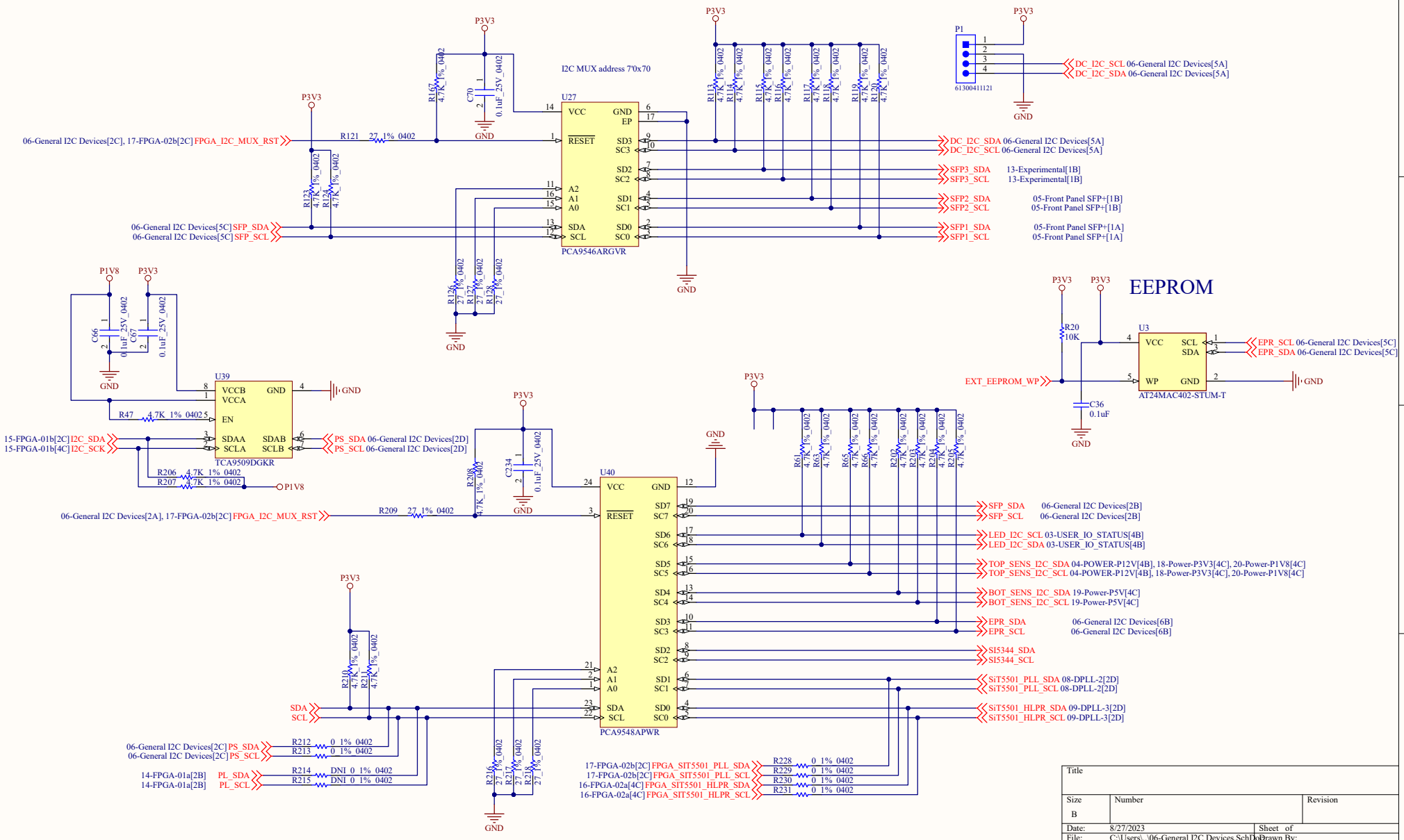
SHEET 5 OF 20


I2C MUX address 7'0x70
U27
PCA9546ARGVR
P1
61300411121
DC_I2C_SCL 06-General I2C Devices[5A]
DC_I2C_SDA 06-General I2C Devices[5A]
06-General I2C Devices[2C], 17-FPGA-02b[2C] FPGA_I2C_MUX_RST
R121 27_1% 0402
06-General I2C Devices[5C] SFP_SDA
06-General I2C Devices[5C] SFP_SCL
SFP3_SDA 13-Experimental[1B]
SFP3_SCL 13-Experimental[1B]
SFP2_SDA 05-Front Panel SFP+[1B]
SFP2_SCL 05-Front Panel SFP+[1B]
SFP1_SDA 05-Front Panel SFP+[1A]
SFP1_SCL 05-Front Panel SFP+[1A]
EEPROM
U3
AT24MAC402-STUM-T
EPR_SCL 06-General I2C Devices[5C]
EPR_SDA 06-General I2C Devices[5C]
EXT_EEPROM_WP
R20 10K
C36 0.1uF
U39
TCA9509DGKR
15-FPGA-01b[2C] I2C_SDA
15-FPGA-01b[4C] I2C_SCK
PS_SDA 06-General I2C Devices[2D]
PS_SCL 06-General I2C Devices[2D]
R47 4.7K 1% 0402
R206 4.7K 1% 0402
R207 4.7K 1% 0402
P1V8
U40
PCA9548APWR
06-General I2C Devices[2A], 17-FPGA-02b[2C] FPGA_I2C_MUX_RST
R209 27_1% 0402
SFP_SDA 06-General I2C Devices[2B]
SFP_SCL 06-General I2C Devices[2B]
LED_I2C_SCL 03-USER_IO_STATUS[4B]
LED_I2C_SDA 03-USER_IO_STATUS[4B]
TOP_SENS_I2C_SDA 04-POWER-P12V[4B], 18-Power-P3V3[4C], 20-Power-P1V8[4C]
TOP_SENS_I2C_SCL 04-POWER-P12V[4B], 18-Power-P3V3[4C], 20-Power-P1V8[4C]
BOT_SENS_I2C_SDA 19-Power-P5V[4C]
BOT_SENS_I2C_SCL 19-Power-P5V[4C]
EPR_SDA 06-General I2C Devices[6B]
EPR_SCL 06-General I2C Devices[6B]
SI5344_SDA
SI5344_SCL
SiT5501_PLL_SDA 08-DPLL-2[2D]
SiT5501_PLL_SCL 08-DPLL-2[2D]
SiT5501_HLPR_SDA 09-DPLL-3[2D]
SiT5501_HLPR_SCL 09-DPLL-3[2D]
06-General I2C Devices[2C] PS_SDA
06-General I2C Devices[2C] PS_SCL
14-FPGA-01a[2B] PL_SDA
14-FPGA-01a[2B] PL_SCL
17-FPGA-02b[2C] FPGA_SIT5501_PLL_SDA
17-FPGA-02b[2C] FPGA_SIT5501_PLL_SCL
16-FPGA-02a[4C] FPGA_SIT5501_HLPR_SDA
16-FPGA-02a[4C] FPGA_SIT5501_HLPR_SCL
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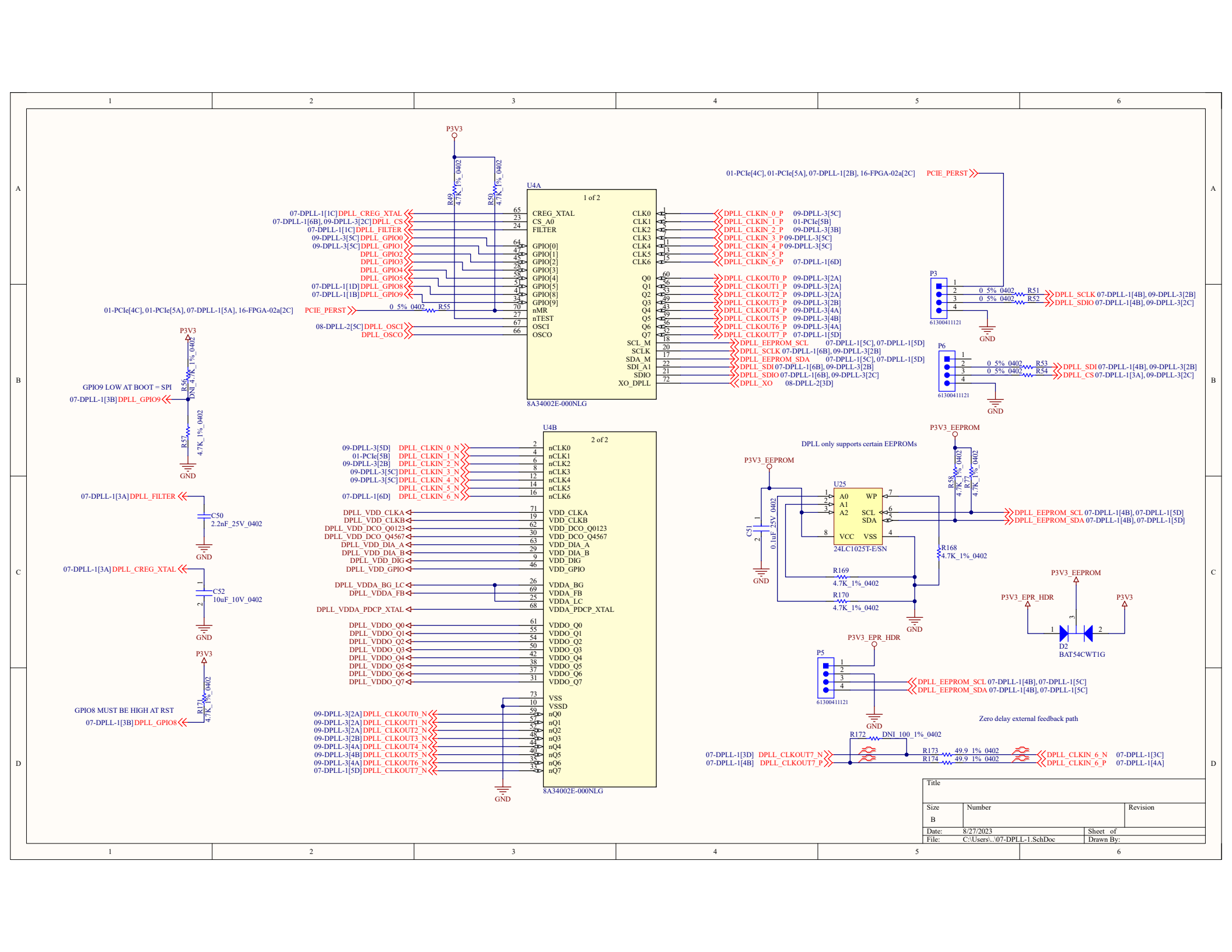
P3V3
U4A
1 of 2
8A34002E-000NLG
U4B
2 of 2
8A34002E-000NLG
GND
U25
24LC1025T-E/SN
P3V3_EEPROM
DPLL only supports certain EEPROMs
P3
P5
P6
61300411121
P3V3_EPR_HDR
D2
BAT54CWT1G
GPIO9 LOW AT BOOT = SPI
GPIO8 MUST BE HIGH AT RST
Zero delay external feedback path
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Number
Revision
Date: 8/27/2023
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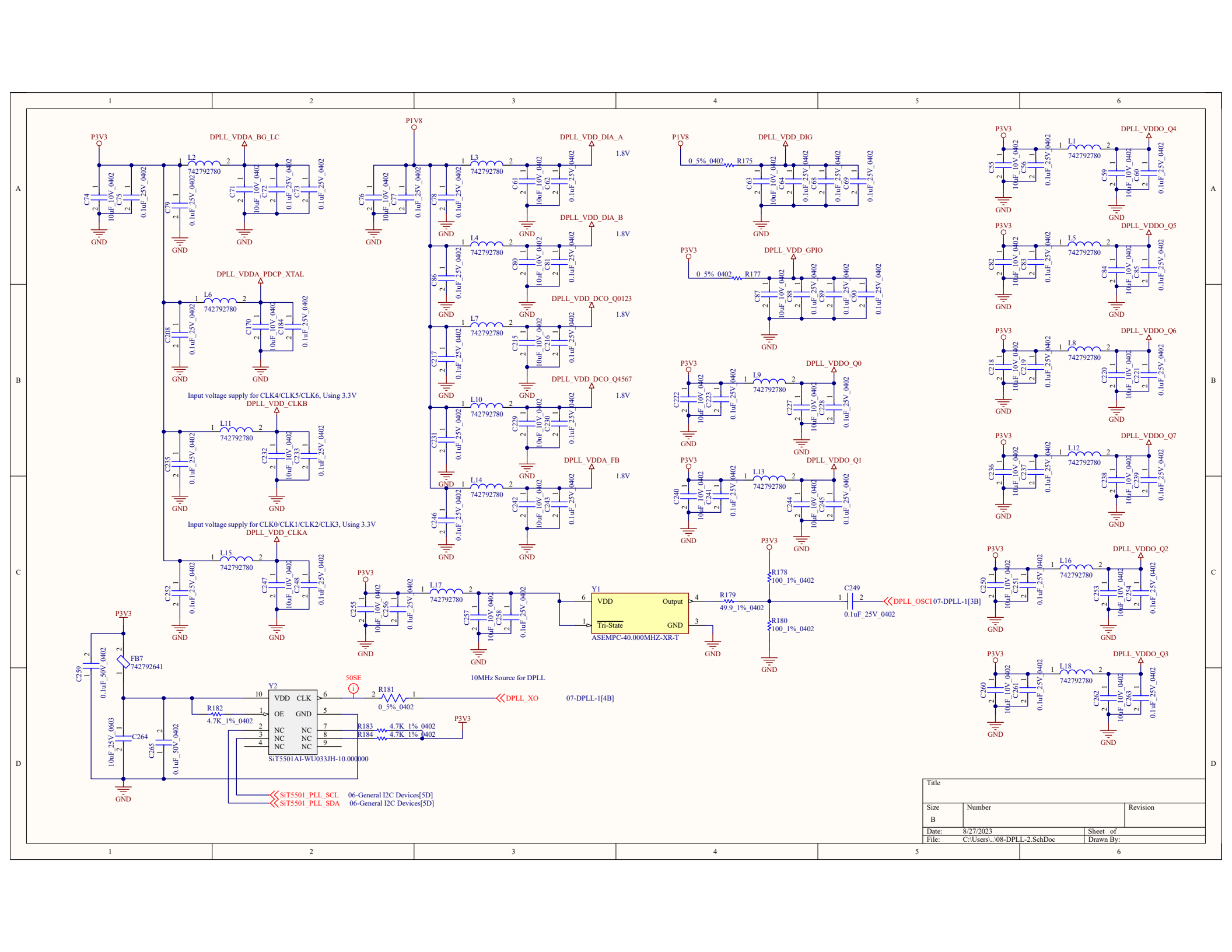
P3V3
DPLL_VDDA_BG_LC
L2
742792780
C74
10uF_10V_0402
C75
0.1uF_25V_0402
C79
0.1uF_25V_0402
C71
10uF_10V_0402
C72
0.1uF_25V_0402
C73
0.1uF_25V_0402
GND
DPLL_VDDA_PDCP_XTAL
L6
742792780
C208
0.1uF_25V_0402
C170
10uF_10V_0402
C184
0.1uF_25V_0402
Input voltage supply for CLK4/CLK5/CLK6, Using 3.3V
DPLL_VDD_CLKB
L11
742792780
C235
0.1uF_25V_0402
C232
10uF_10V_0402
C233
0.1uF_25V_0402
Input voltage supply for CLK0/CLK1/CLK2/CLK3, Using 3.3V
DPLL_VDD_CLKA
L15
742792780
C252
0.1uF_25V_0402
C247
10uF_10V_0402
C248
0.1uF_25V_0402
P1V8
DPLL_VDD_DIA_A
1.8V
L3
742792780
C76
10uF_10V_0402
C77
0.1uF_25V_0402
C78
0.1uF_25V_0402
C61
10uF_10V_0402
C62
0.1uF_25V_0402
DPLL_VDD_DIA_B
1.8V
L4
742792780
C86
0.1uF_25V_0402
C80
10uF_10V_0402
C81
0.1uF_25V_0402
DPLL_VDD_DCO_Q0123
1.8V
L7
742792780
C217
0.1uF_25V_0402
C215
10uF_10V_0402
C216
0.1uF_25V_0402
DPLL_VDD_DCO_Q4567
1.8V
L10
742792780
C231
0.1uF_25V_0402
C229
10uF_10V_0402
C230
0.1uF_25V_0402
DPLL_VDDA_FB
1.8V
L14
742792780
C246
0.1uF_25V_0402
C242
10uF_10V_0402
C243
0.1uF_25V_0402
P1V8
DPLL_VDD_DIG
0_5%_0402
R175
C63
10uF_10V_0402
C64
0.1uF_25V_0402
C68
0.1uF_25V_0402
C69
0.1uF_25V_0402
P3V3
DPLL_VDD_GPIO
0_5%_0402
R177
C87
10uF_10V_0402
C88
0.1uF_25V_0402
C89
0.1uF_25V_0402
C90
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q0
L9
742792780
C222
10uF_10V_0402
C223
0.1uF_25V_0402
C227
10uF_10V_0402
C228
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q1
L13
742792780
C240
10uF_10V_0402
C241
0.1uF_25V_0402
C244
10uF_10V_0402
C245
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q4
L1
742792780
C55
10uF_10V_0402
C56
0.1uF_25V_0402
C59
10uF_10V_0402
C60
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q5
L5
742792780
C82
10uF_10V_0402
C83
0.1uF_25V_0402
C84
10uF_10V_0402
C85
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q6
L8
742792780
C218
10uF_10V_0402
C219
0.1uF_25V_0402
C220
10uF_10V_0402
C221
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q7
L12
742792780
C236
10uF_10V_0402
C237
0.1uF_25V_0402
C238
10uF_10V_0402
C239
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q2
L16
742792780
C250
10uF_10V_0402
C251
0.1uF_25V_0402
C253
10uF_10V_0402
C254
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q3
L18
742792780
C260
10uF_10V_0402
C261
0.1uF_25V_0402
C262
10uF_10V_0402
C263
0.1uF_25V_0402
P3V3
L17
742792780
C255
10uF_10V_0402
C256
0.1uF_25V_0402
C257
10uF_10V_0402
C258
0.1uF_25V_0402
Y1
VDD
Output
Tri-State
GND
ASEMPC-40.000MHZ-XR-T
R178
100_1%_0402
R179
49.9_1%_0402
R180
100_1%_0402
C249
0.1uF_25V_0402
DPLL_OSCI
07-DPLL-1[3B]
FB7
742792641
C259
10uF_25V_0603
C264
0.1uF_50V_0402
C265
0.1uF_50V_0402
Y2
VDD
CLK
OE
GND
NC
NC
NC
NC
NC
SiT5501AI-WU033JH-10.000000
50SE
R181
0_5%_0402
DPLL_XO
07-DPLL-1[4B]
10MHz Source for DPLL
R182
4.7K_1%_0402
R183
4.7K_1%_0402
R184
4.7K_1%_0402
SiT5501_PLL_SCL
SiT5501_PLL_SDA
06-General I2C Devices[5D]
06-General I2C Devices[5D]
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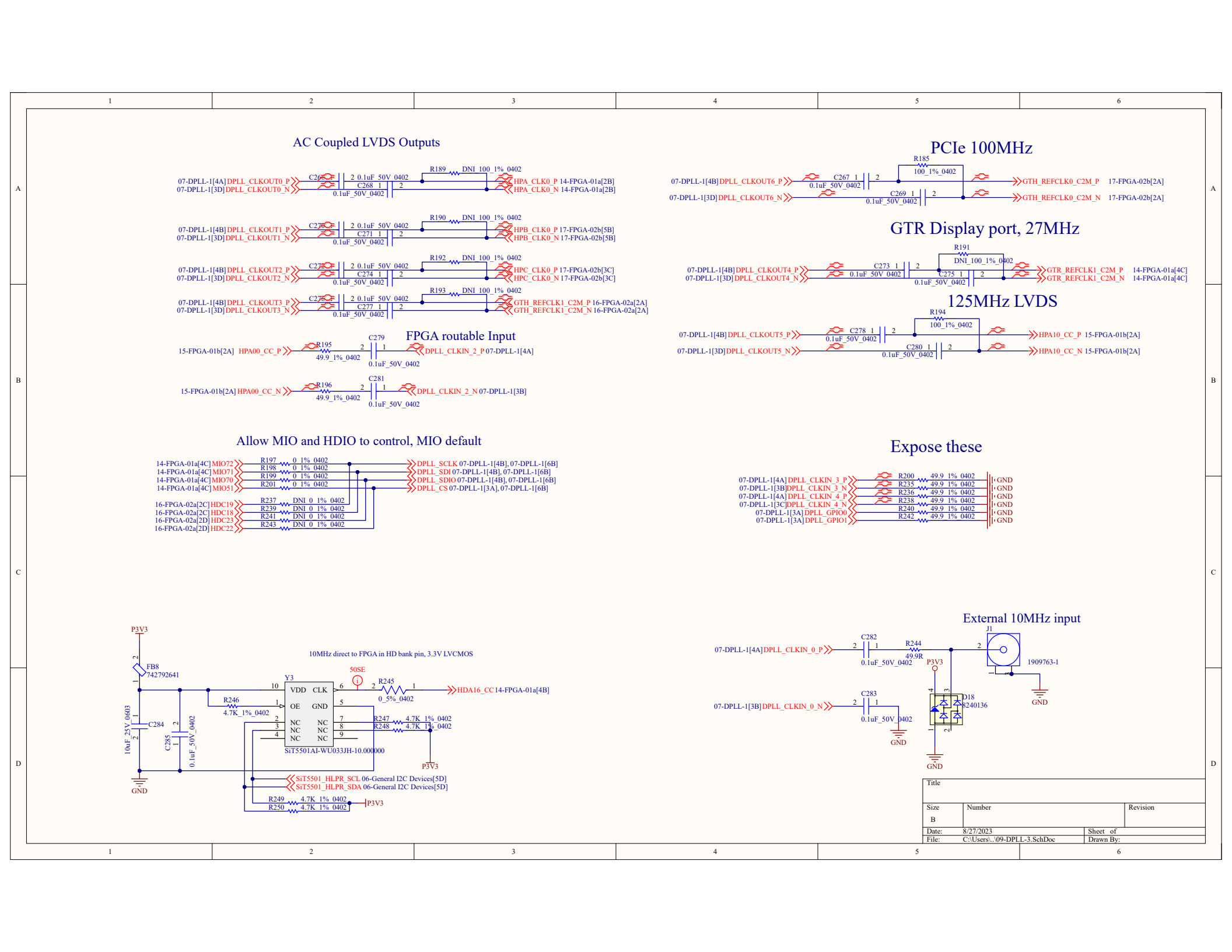
AC Coupled LVDS Outputs
07-DPLL-1[4A] DPLL_CLKOUT0_P
07-DPLL-1[3D] DPLL_CLKOUT0_N
C266 2 0.1uF_50V_0402
C268 1 2 0.1uF_50V_0402
R189 DNI_100_1%_0402
HPA_CLK0_P 14-FPGA-01a[2B]
HPA_CLK0_N 14-FPGA-01a[2B]
07-DPLL-1[4B] DPLL_CLKOUT1_P
07-DPLL-1[3D] DPLL_CLKOUT1_N
C270 2 0.1uF_50V_0402
C271 1 2 0.1uF_50V_0402
R190 DNI_100_1%_0402
HPB_CLK0_P 17-FPGA-02b[5B]
HPB_CLK0_N 17-FPGA-02b[5B]
07-DPLL-1[4B] DPLL_CLKOUT2_P
07-DPLL-1[3D] DPLL_CLKOUT2_N
C272 2 0.1uF_50V_0402
C274 1 2 0.1uF_50V_0402
R192 DNI_100_1%_0402
HPC_CLK0_P 17-FPGA-02b[3C]
HPC_CLK0_N 17-FPGA-02b[3C]
07-DPLL-1[4B] DPLL_CLKOUT3_P
07-DPLL-1[3D] DPLL_CLKOUT3_N
C276 2 0.1uF_50V_0402
C277 1 2 0.1uF_50V_0402
R193 DNI_100_1%_0402
GTH_REFCLK1_C2M_P 16-FPGA-02a[2A]
GTH_REFCLK1_C2M_N 16-FPGA-02a[2A]
FPGA routable Input
15-FPGA-01b[2A] HPA00_CC_P
R195 49.9_1%_0402
C279 2 1 0.1uF_50V_0402
DPLL_CLKIN_2_P 07-DPLL-1[4A]
15-FPGA-01b[2A] HPA00_CC_N
R196 49.9_1%_0402
C281 2 1 0.1uF_50V_0402
DPLL_CLKIN_2_N 07-DPLL-1[3B]
PCIe 100MHz
07-DPLL-1[4B] DPLL_CLKOUT6_P
07-DPLL-1[3D] DPLL_CLKOUT6_N
C267 1 2 0.1uF_50V_0402
C269 1 2 0.1uF_50V_0402
R185 100_1%_0402
GTH_REFCLK0_C2M_P 17-FPGA-02b[2A]
GTH_REFCLK0_C2M_N 17-FPGA-02b[2A]
GTR Display port, 27MHz
07-DPLL-1[4B] DPLL_CLKOUT4_P
07-DPLL-1[3D] DPLL_CLKOUT4_N
C273 1 2 0.1uF_50V_0402
C275 1 2 0.1uF_50V_0402
R191 DNI_100_1%_0402
GTR_REFCLK1_C2M_P 14-FPGA-01a[4C]
GTR_REFCLK1_C2M_N 14-FPGA-01a[4C]
125MHz LVDS
07-DPLL-1[4B] DPLL_CLKOUT5_P
07-DPLL-1[3D] DPLL_CLKOUT5_N
C278 1 2 0.1uF_50V_0402
C280 1 2 0.1uF_50V_0402
R194 100_1%_0402
HPA10_CC_P 15-FPGA-01b[2A]
HPA10_CC_N 15-FPGA-01b[2A]
Allow MIO and HDIO to control, MIO default
14-FPGA-01a[4C] MIO72
14-FPGA-01a[4C] MIO71
14-FPGA-01a[4C] MIO70
14-FPGA-01a[4C] MIO51
R197 0_1%_0402
R198 0_1%_0402
R199 0_1%_0402
R201 0_1%_0402
DPLL_SCLK 07-DPLL-1[4B], 07-DPLL-1[6B]
DPLL_SDI 07-DPLL-1[4B], 07-DPLL-1[6B]
DPLL_SDIO 07-DPLL-1[4B], 07-DPLL-1[6B]
DPLL_CS 07-DPLL-1[3A], 07-DPLL-1[6B]
16-FPGA-02a[2C] HDC19
16-FPGA-02a[2C] HDC18
16-FPGA-02a[2D] HDC23
16-FPGA-02a[2D] HDC22
R237 DNI_0_1%_0402
R239 DNI_0_1%_0402
R241 DNI_0_1%_0402
R243 DNI_0_1%_0402
Expose these
07-DPLL-1[4A] DPLL_CLKIN_3_P
07-DPLL-1[3B] DPLL_CLKIN_3_N
07-DPLL-1[4A] DPLL_CLKIN_4_P
07-DPLL-1[3C] DPLL_CLKIN_4_N
07-DPLL-1[3A] DPLL_GPIO0
07-DPLL-1[3A] DPLL_GPIO1
R200 49.9_1%_0402
R235 49.9_1%_0402
R236 49.9_1%_0402
R238 49.9_1%_0402
R240 49.9_1%_0402
R242 49.9_1%_0402
GND
P3V3
FB8 742792641
10MHz direct to FPGA in HD bank pin, 3.3V LVCMOS
Y3
VDD CLK OE GND NC NC NC NC
SiT5501AI-WU033JH-10.000000
50SE
R245 0_5%_0402
HDA16_CC 14-FPGA-01a[4B]
R246 4.7K_1%_0402
R247 4.7K_1%_0402
R248 4.7K_1%_0402
C284 10uF_25V_0603
C285 0.1uF_50V_0402
SiT5501_HLPR_SCL 06-General I2C Devices[5D]
SiT5501_HLPR_SDA 06-General I2C Devices[5D]
R249 4.7K_1%_0402
R250 4.7K_1%_0402
External 10MHz input
07-DPLL-1[4A] DPLL_CLKIN_0_P
07-DPLL-1[3B] DPLL_CLKIN_0_N
C282 2 1 0.1uF_50V_0402
C283 2 1 0.1uF_50V_0402
R244 49.9R
J1
1909763-1
D18 BAT54S
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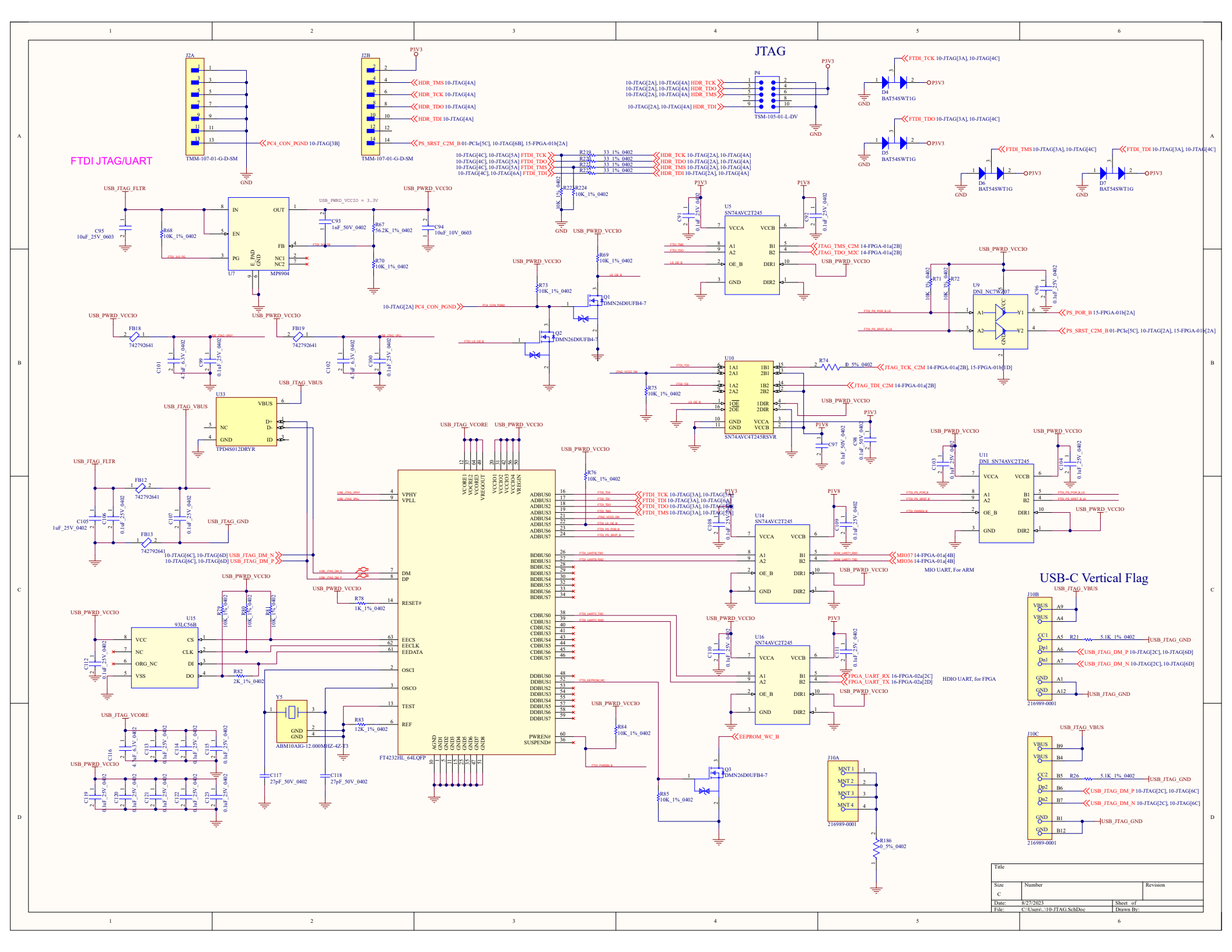
JTAG
FTDI JTAG/UART
USB-C Vertical Flag
J2A
TMM-107-01-G-D-SM
J2B
TMM-107-01-G-D-SM
P4
TSM-105-01-L-DV
D4
BAT54SWT1G
D5
BAT54SWT1G
D6
BAT54SWT1G
D7
BAT54SWT1G
U5
SN74AVC2T245
U7
MP8904
U9
DNI_NC7WZ07
U10
SN74AVC4T245RSVR
U11
DNI_SN74AVC2T245
U14
SN74AVC2T245
U15
93LC56B
U16
SN74AVC2T245
U33
TPD4S012DRYR
FT4232HL_64LQFP
ABM10AIG-12.000MHZ-4Z-T3
Q1
DMN26D0UFB4-7
Q2
DMN26D0UFB4-7
Q3
DMN26D0UFB4-7
J10A
J10B
J10C
216989-0001
MIO UART, For ARM
HDIO UART, for FPGA
P3V3
GND
USB_JTAG_VBUS
USB_JTAG_GND
USB_PWRD_VCCIO
USB_JTAG_VCORE
EEPROM_WC_B
FTDI_TCK 10-JTAG[3A], 10-JTAG[4C]
FTDI_TDO 10-JTAG[3A], 10-JTAG[4C]
FTDI_TMS 10-JTAG[3A], 10-JTAG[4C]
FTDI_TDI 10-JTAG[3A], 10-JTAG[4C]
HDR_TCK 10-JTAG[4A]
HDR_TDO 10-JTAG[4A]
HDR_TMS 10-JTAG[4A]
HDR_TDI 10-JTAG[4A]
PC4_CON_PGND 10-JTAG[3B]
PS_SRST_C2M_B 01-PCIe[5C], 10-JTAG[6B], 15-FPGA-01b[2A]
JTAG_TCK_C2M 14-FPGA-01a[2B], 15-FPGA-01b[1D]
JTAG_TDI_C2M 14-FPGA-01a[2B]
JTAG_TMS_C2M 14-FPGA-01a[2B]
JTAG_TDO_M2C 14-FPGA-01a[2B]
PS_POR_B 15-FPGA-01b[2A]
MIO37 14-FPGA-01a[4B]
MIO36 14-FPGA-01a[4B]
FPGA_UART_RX 16-FPGA-02a[2C]
FPGA_UART_TX 16-FPGA-02a[2D]
USB_JTAG_DM_P 10-JTAG[2C], 10-JTAG[6D]
USB_JTAG_DM_N 10-JTAG[2C], 10-JTAG[6D]
USB_PWRD_VCCIO = 3.3V
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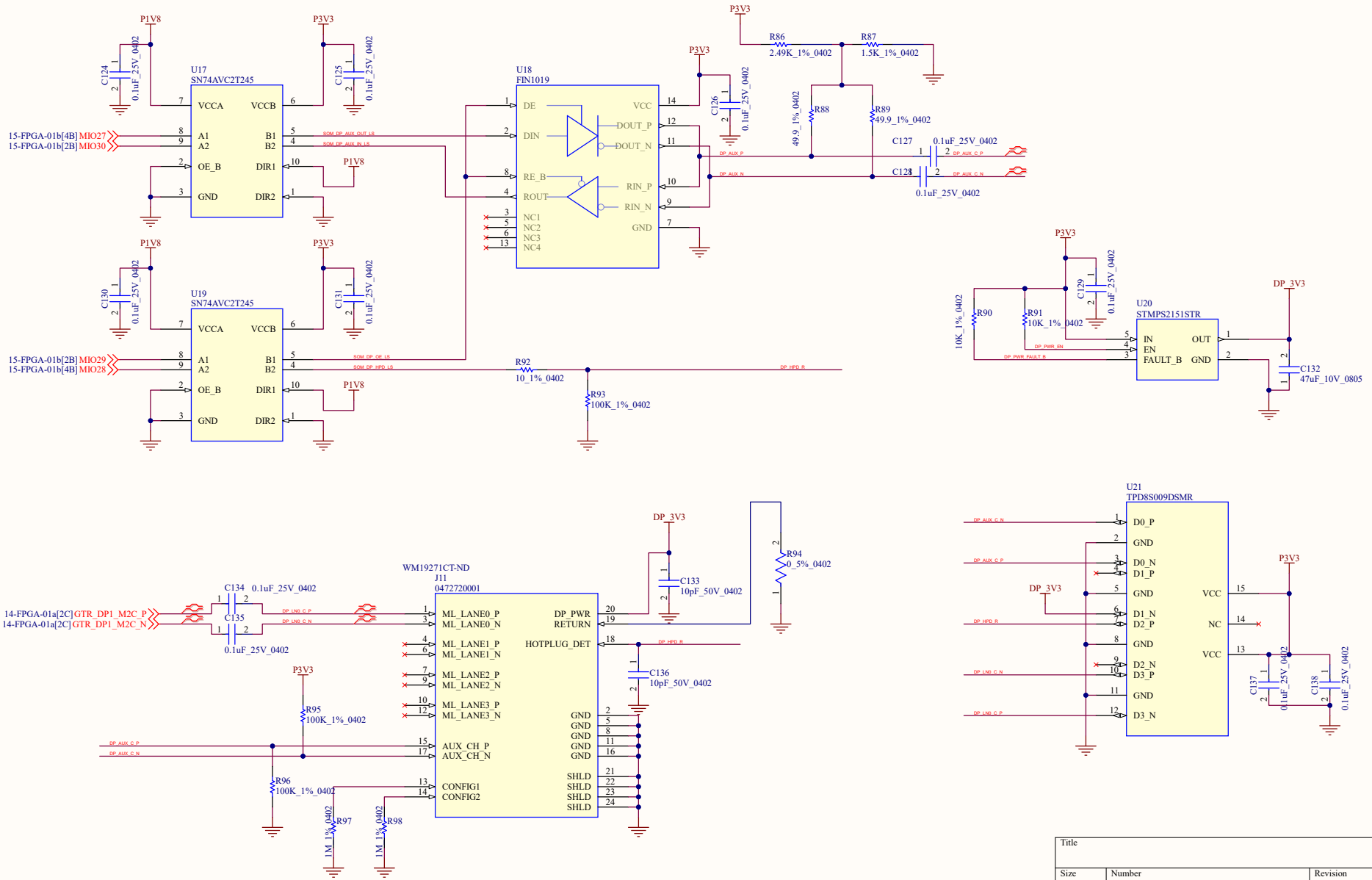
P1V8
P3V3
U17
SN74AVC2T245
VCCA
VCCB
A1
A2
B1
B2
OE_B
DIR1
DIR2
GND
C124 0.1uF_25V_0402
C125 0.1uF_25V_0402
15-FPGA-01b[4B] MIO27
15-FPGA-01b[2B] MIO30
SOM_DP_AUX_OUT_LS
SOM_DP_AUX_IN_LS
U18
FIN1019
DE
DIN
RE_B
ROUT
VCC
DOUT_P
DOUT_N
RIN_P
RIN_N
GND
NC1
NC2
NC3
NC4
C126 0.1uF_25V_0402
R86 2.49K_1%_0402
R87 1.5K_1%_0402
R88 49.9_1%_0402
R89 49.9_1%_0402
C127 0.1uF_25V_0402
C128 0.1uF_25V_0402
DP_AUX_P
DP_AUX_N
DP_AUX_C_P
DP_AUX_C_N
U19
SN74AVC2T245
C130 0.1uF_25V_0402
C131 0.1uF_25V_0402
15-FPGA-01b[2B] MIO29
15-FPGA-01b[4B] MIO28
SOM_DP_OE_LS
SOM_DP_HPD_LS
R92 10_1%_0402
R93 100K_1%_0402
DP_HPD_R
U20
STMPS2151STR
IN
EN
FAULT_B
OUT
GND
C129 0.1uF_25V_0402
R90 10K_1%_0402
R91 10K_1%_0402
DP_PWR_EN
DP_PWR_FAULT_B
DP_3V3
C132 47uF_10V_0805
WM19271CT-ND
J11
0472720001
ML_LANE0_P
ML_LANE0_N
ML_LANE1_P
ML_LANE1_N
ML_LANE2_P
ML_LANE2_N
ML_LANE3_P
ML_LANE3_N
AUX_CH_P
AUX_CH_N
CONFIG1
CONFIG2
DP_PWR
RETURN
HOTPLUG_DET
SHLD
C134 0.1uF_25V_0402
C135 0.1uF_25V_0402
14-FPGA-01a[2C] GTR_DP1_M2C_P
14-FPGA-01a[2C] GTR_DP1_M2C_N
DP_LN0_C_P
DP_LN0_C_N
C133 10pF_50V_0402
C136 10pF_50V_0402
R94 0_5%_0402
R95 100K_1%_0402
R96 100K_1%_0402
R97 1M_1%_0402
R98 1M_1%_0402
U21
TPD8S009DSMR
D0_P
D0_N
D1_P
D1_N
D2_P
D2_N
D3_P
D3_N
VCC
NC
C137 0.1uF_25V_0402
C138 0.1uF_25V_0402
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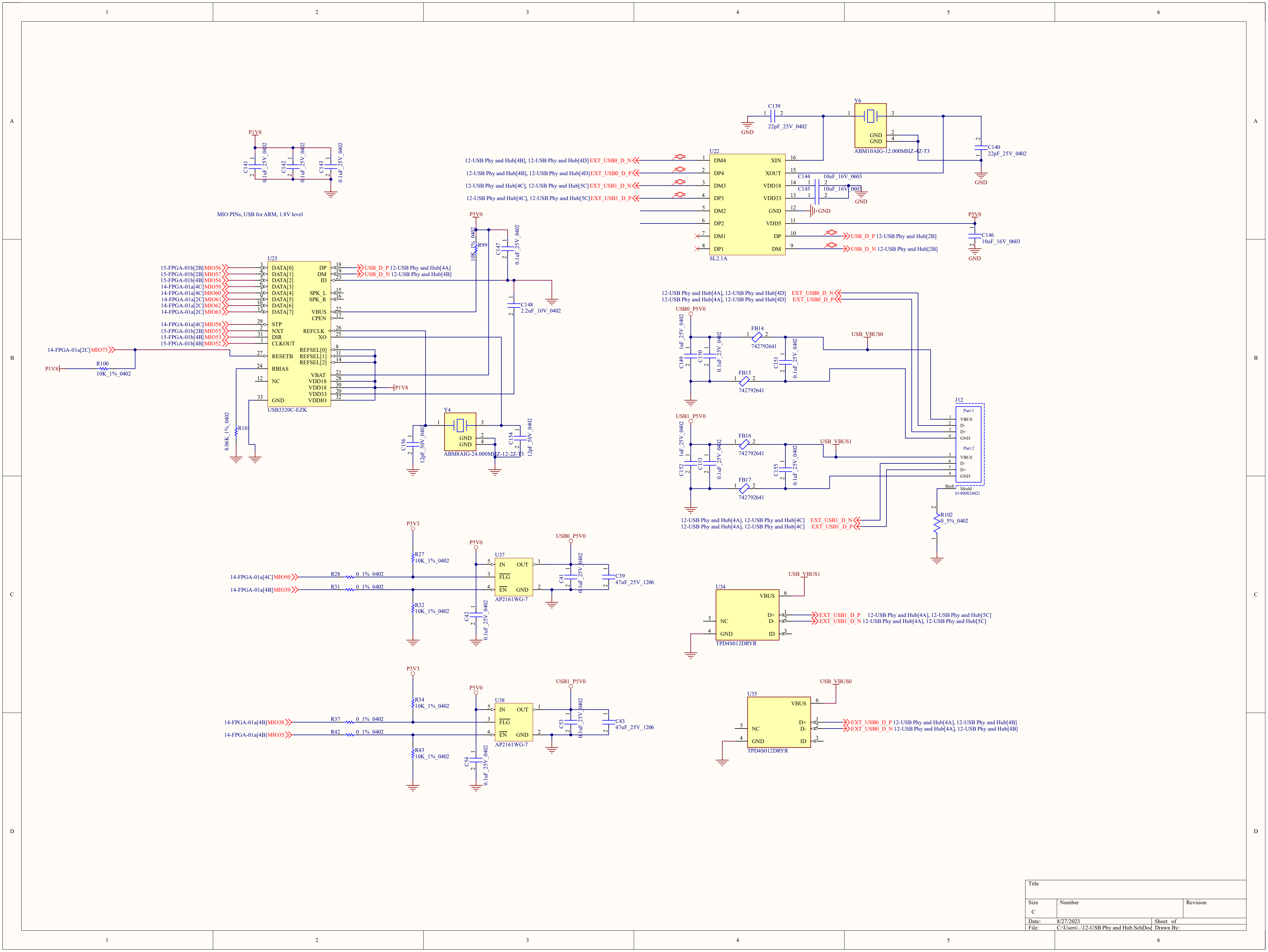

MIO PINs, USB for ARM, 1.8V level
P1V8
C141 0.1uF_25V_0402
C142 0.1uF_25V_0402
C143 0.1uF_25V_0402
U23
USB3320C-EZK
DATA[0] DATA[1] DATA[2] DATA[3] DATA[4] DATA[5] DATA[6] DATA[7]
STP NXT DIR CLKOUT RESETB RBIAS NC GND
DP DM ID SPK_L SPK_R VBUS CPEN REFCLK XO REFSEL[0] REFSEL[1] REFSEL[2] VBAT VDD18 VDD18 VDD33 VDDIO
15-FPGA-01b[2B] MIO56
15-FPGA-01b[2B] MIO57
15-FPGA-01b[4B] MIO54
14-FPGA-01a[4C] MIO59
14-FPGA-01a[4C] MIO60
14-FPGA-01a[2C] MIO61
14-FPGA-01a[2C] MIO62
14-FPGA-01a[2C] MIO63
14-FPGA-01a[4C] MIO58
15-FPGA-01b[2B] MIO55
15-FPGA-01b[4B] MIO53
15-FPGA-01b[4B] MIO52
14-FPGA-01a[2C] MIO73
R100 10K_1%_0402
R101 8.06K_1%_0402
USB_D_P 12-USB Phy and Hub[4A]
USB_D_N 12-USB Phy and Hub[4B]
P5V0
R99 10K_1%_0402
C147 0.1uF_25V_0402
C148 2.2uF_10V_0402
Y4 ABM8AIG-24.000MHZ-12-2Z-T3
C156 12pF_50V_0402
C154 12pF_50V_0402
U22 SL2.1A
DM4 DP4 DM3 DP3 DM2 DP2 DM1 DP1
XIN XOUT VDD18 VDD33 GND VDD5 DP DM
12-USB Phy and Hub[4B], 12-USB Phy and Hub[4D] EXT_USB0_D_N
12-USB Phy and Hub[4B], 12-USB Phy and Hub[4D] EXT_USB0_D_P
12-USB Phy and Hub[4C], 12-USB Phy and Hub[5C] EXT_USB1_D_N
12-USB Phy and Hub[4C], 12-USB Phy and Hub[5C] EXT_USB1_D_P
C139 22pF_25V_0402
Y6 ABM10AIG-12.000MHZ-4Z-T3
C140 22pF_25V_0402
C144 10uF_16V_0603
C145 10uF_16V_0603
C146 10uF_16V_0603
USB_D_P 12-USB Phy and Hub[2B]
USB_D_N 12-USB Phy and Hub[2B]
12-USB Phy and Hub[4A], 12-USB Phy and Hub[4D] EXT_USB0_D_N
12-USB Phy and Hub[4A], 12-USB Phy and Hub[4D] EXT_USB0_D_P
USB0_P5V0
C149 1uF_25V_0402
C150 0.1uF_25V_0402
C151 0.1uF_25V_0402
FB14 742792641
FB15 742792641
USB_VBUS0
USB1_P5V0
C152 1uF_25V_0402
C153 0.1uF_25V_0402
C155 0.1uF_25V_0402
FB16 742792641
FB17 742792641
USB_VBUS1
J12 61400826021
Part 1 VBUS D- D+ GND
Part 2 VBUS D- D+ GND
Shell Shield
R102 0_5%_0402
12-USB Phy and Hub[4A], 12-USB Phy and Hub[4C] EXT_USB1_D_N
12-USB Phy and Hub[4A], 12-USB Phy and Hub[4C] EXT_USB1_D_P
P3V3
R27 10K_1%_0402
R28 0_1%_0402
R31 0_1%_0402
R32 10K_1%_0402
14-FPGA-01a[4C] MIO50
14-FPGA-01a[4B] MIO39
U37 AP2161WG-7
IN OUT FLG EN GND
USB0_P5V0
C41 0.1uF_25V_0402
C39 47uF_25V_1206
C42 0.1uF_25V_0402
U34 TPD4S012DRYR
VBUS NC GND D+ D- ID
USB_VBUS1
EXT_USB1_D_P 12-USB Phy and Hub[4A], 12-USB Phy and Hub[5C]
EXT_USB1_D_N 12-USB Phy and Hub[4A], 12-USB Phy and Hub[5C]
R34 10K_1%_0402
R37 0_1%_0402
R42 0_1%_0402
R43 10K_1%_0402
14-FPGA-01a[4B] MIO38
14-FPGA-01a[4B] MIO35
U38 AP2161WG-7
USB1_P5V0
C53 0.1uF_25V_0402
C43 47uF_25V_1206
C54 0.1uF_25V_0402
U35 TPD4S012DRYR
USB_VBUS0
EXT_USB0_D_P 12-USB Phy and Hub[4A], 12-USB Phy and Hub[4B]
EXT_USB0_D_N 12-USB Phy and Hub[4A], 12-USB Phy and Hub[4B]
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Experiment: 1G SFP driven from HPIO instead of GTH

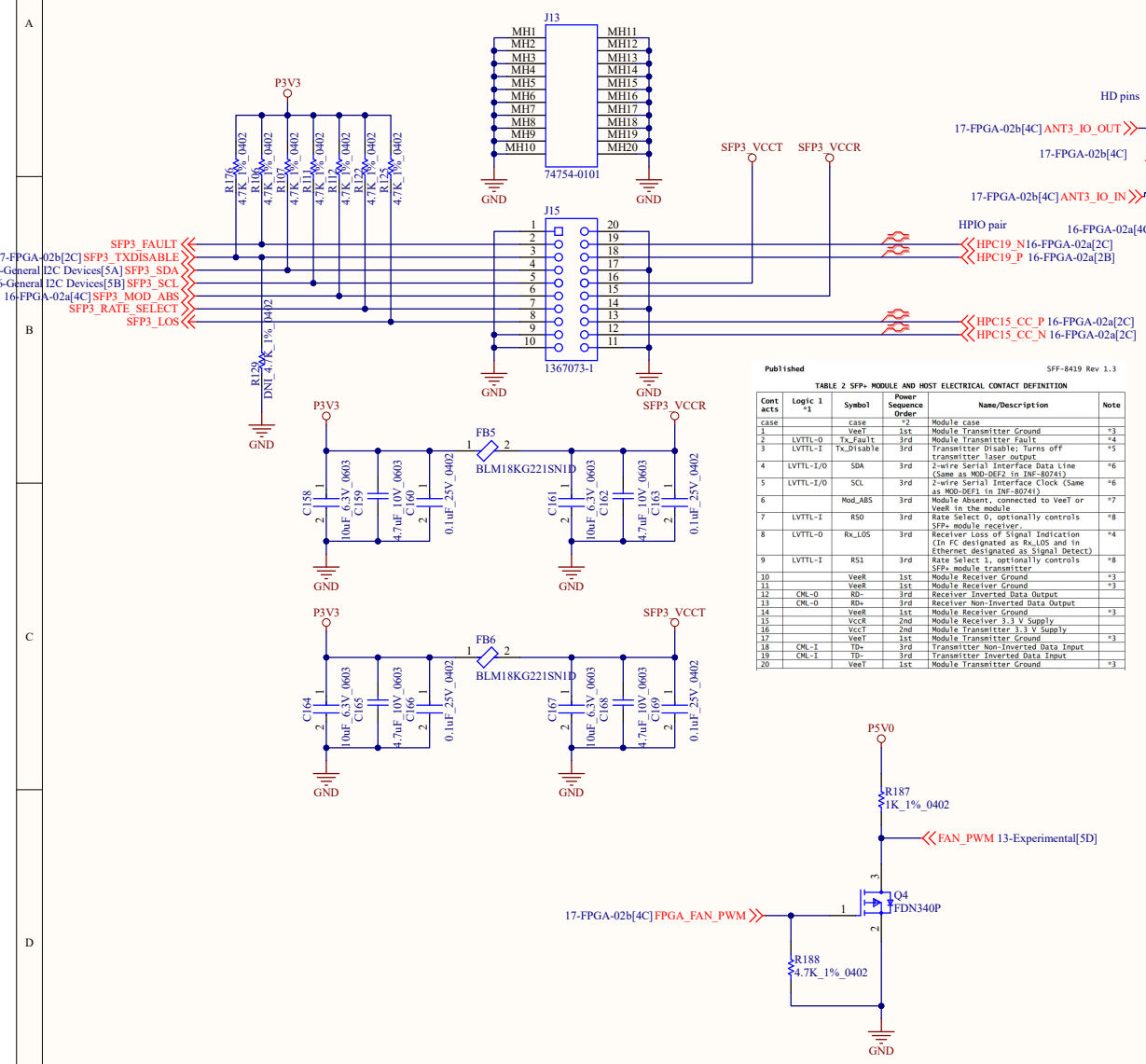

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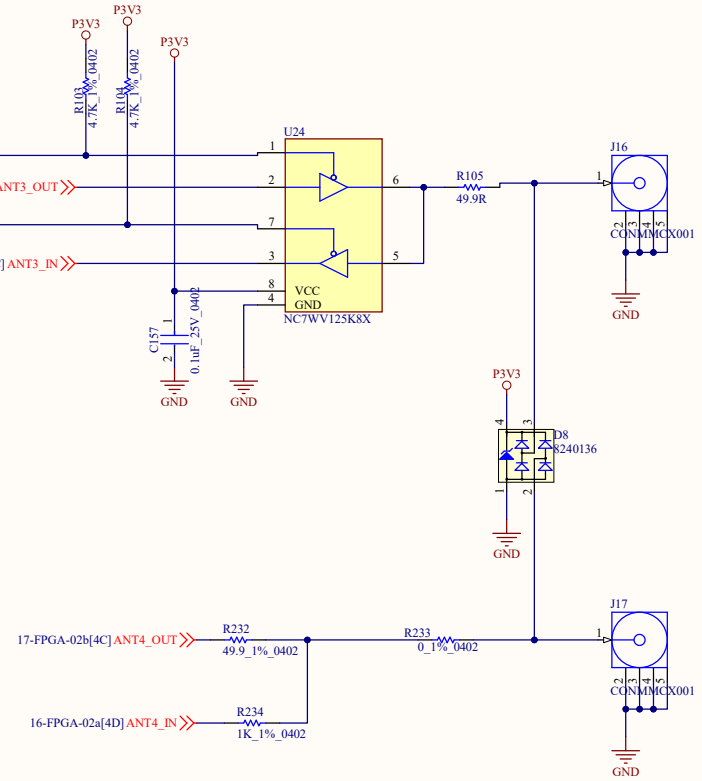
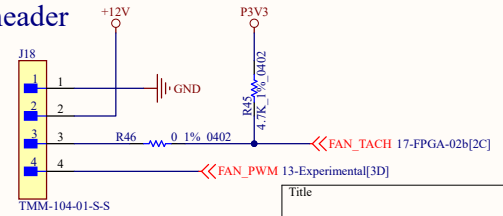
TABLE 2 SFP+ MODULE AND HOST ELECTRICAL CONTACT DEFINITION

Contacts	Logic 1 =1	Symbol	Power Sequence Order	Name/Description	Note
case		case	*2	Module case	
1		VeeT	1st	Module Transmitter Ground	*3
2	LVTTL-O	Tx_Fault	3rd	Module Transmitter Fault	*4
3	LVTTL-I	Tx_Disable	3rd	Transmitter Disable; Turns off transmitter laser output	*5
4	LVTTL-I/O	SDA	3rd	2-wire Serial Interface Data Line (Same as MOD-DEF2 in INF-8074i)	*6
5	LVTTL-I/O	SCL	3rd	2-wire Serial Interface Clock (Same as MOD-DEF1 in INF-8074i)	*6
6		Mod_ABS	3rd	Module Absent, connected to VeeT or VeeR in the module	*7
7	LVTTL-I	RSO	3rd	Rate Select 0, optionally controls SFP+ module receiver.	*8
8	LVTTL-O	Rx_LOS	3rd	Receiver Loss of Signal Indication (In FC designated as Rx_LOS and in Ethernet designated as Signal Detect)	*4
9	LVTTL-I	RS1	3rd	Rate Select 1, optionally controls SFP+ module transmitter	*8
10		VeeR	1st	Module Receiver Ground	*3
11		VeeR	1st	Module Receiver Ground	*3
12	CML-O	RD-	3rd	Receiver Inverted Data Output	
13	CML-O	RD+	3rd	Receiver Non-Inverted Data Output	
14		VeeR	1st	Module Receiver Ground	*3
15		VccR	2nd	Module Receiver 3.3 V Supply	
16		VccT	2nd	Module Transmitter 3.3 V Supply	
17		VeeT	1st	Module Transmitter Ground	*3
18	CML-I	TD+	3rd	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	3rd	Transmitter Inverted Data Input	
20		VeeT	1st	Module Transmitter Ground	*3

Experiment: Reserve UFL on board



Fan header



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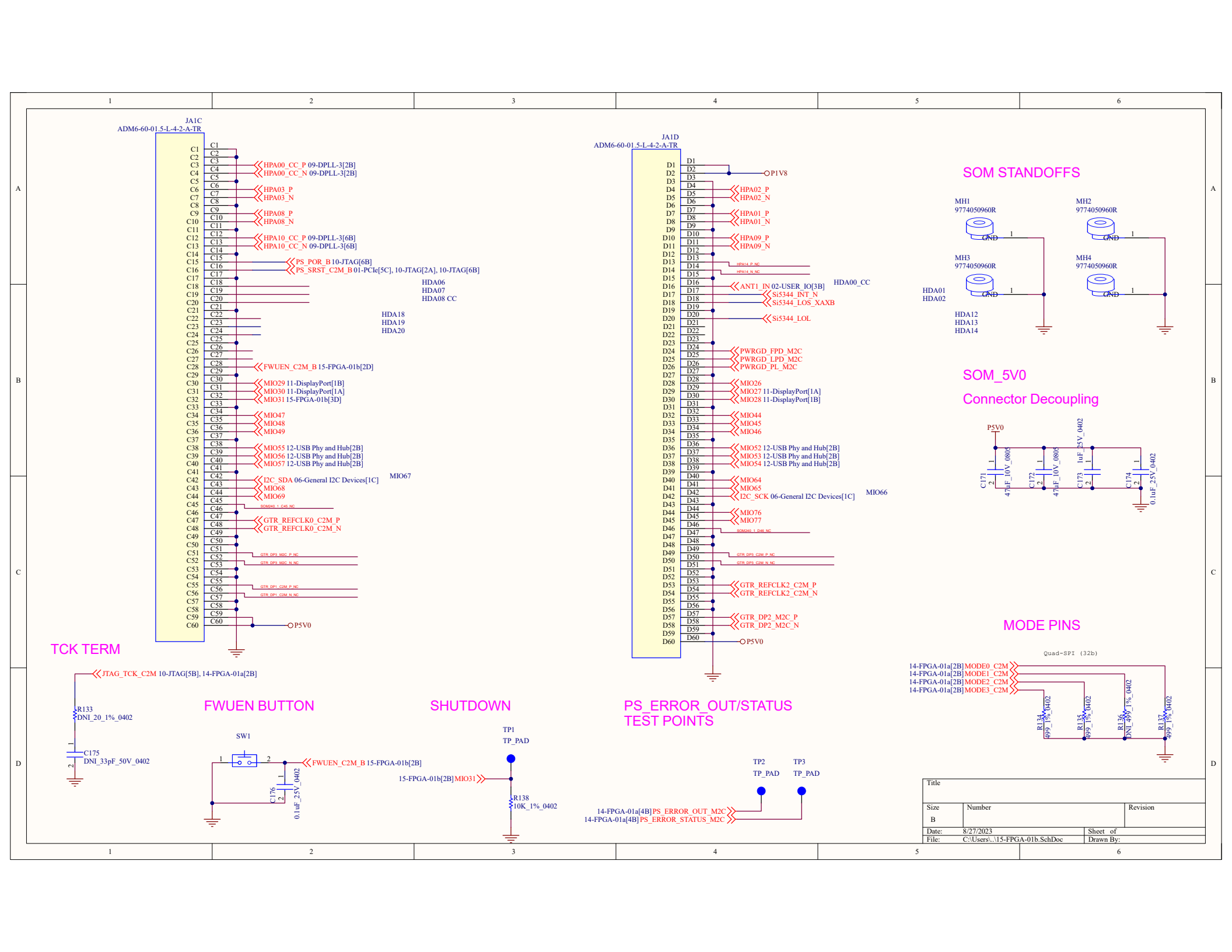
JA1C
ADM6-60-01.5-L-4-2-A-TR
HPA00_CC_P 09-DPLL-3[2B]
HPA00_CC_N 09-DPLL-3[2B]
HPA03_P
HPA03_N
HPA08_P
HPA08_N
HPA10_CC_P 09-DPLL-3[6B]
HPA10_CC_N 09-DPLL-3[6B]
PS_POR_B 10-JTAG[6B]
PS_SRST_C2M_B 01-PCIe[5C], 10-JTAG[2A], 10-JTAG[6B]
HDA06
HDA07
HDA08 CC
HDA18
HDA19
HDA20
FWUEN_C2M_B 15-FPGA-01b[2D]
MIO29 11-DisplayPort[1B]
MIO30 11-DisplayPort[1A]
MIO31 15-FPGA-01b[3D]
MIO47
MIO48
MIO49
MIO55 12-USB Phy and Hub[2B]
MIO56 12-USB Phy and Hub[2B]
MIO57 12-USB Phy and Hub[2B]
MIO67
I2C_SDA 06-General I2C Devices[1C]
MIO68
MIO69
SOM240_1_C45_NC
GTR_REFCLK0_C2M_P
GTR_REFCLK0_C2M_N
GTR_DP3_M2C_P_NC
GTR_DP3_M2C_N_NC
GTR_DP1_C2M_P_NC
GTR_DP1_C2M_N_NC
P5V0
JA1D
ADM6-60-01.5-L-4-2-A-TR
P1V8
HPA02_P
HPA02_N
HPA01_P
HPA01_N
HPA09_P
HPA09_N
HPA14_P_NC
HPA14_N_NC
ANT1_IN 02-USER_IO[3B]
HDA00_CC
Si5344_INT_N
Si5344_LOS_XAXB
Si5344_LOL
PWRGD_FPD_M2C
PWRGD_LPD_M2C
PWRGD_PL_M2C
MIO26
MIO27 11-DisplayPort[1A]
MIO28 11-DisplayPort[1B]
MIO44
MIO45
MIO46
MIO52 12-USB Phy and Hub[2B]
MIO53 12-USB Phy and Hub[2B]
MIO54 12-USB Phy and Hub[2B]
MIO64
MIO65
MIO66
I2C_SCK 06-General I2C Devices[1C]
MIO76
MIO77
SOM240_1_D46_NC
GTR_DP3_C2M_P_NC
GTR_DP3_C2M_N_NC
GTR_REFCLK2_C2M_P
GTR_REFCLK2_C2M_N
GTR_DP2_M2C_P
GTR_DP2_M2C_N
P5V0
SOM STANDOFFS
MH1
9774050960R
MH2
9774050960R
MH3
9774050960R
MH4
9774050960R
GND
HDA01
HDA02
HDA12
HDA13
HDA14
SOM_5V0
Connector Decoupling
P5V0
C171
47uF_10V_0805
C172
47uF_10V_0805
C173
1uF_25V_0402
C174
0.1uF_25V_0402
TCK TERM
JTAG_TCK_C2M 10-JTAG[5B], 14-FPGA-01a[2B]
R133
DNI_20_1%_0402
C175
DNI_33pF_50V_0402
FWUEN BUTTON
SW1
FWUEN_C2M_B 15-FPGA-01b[2B]
C176
0.1uF_25V_0402
SHUTDOWN
TP1
TP_PAD
15-FPGA-01b[2B] MIO31
R138
10K_1%_0402
PS_ERROR_OUT/STATUS
TEST POINTS
TP2
TP_PAD
TP3
TP_PAD
14-FPGA-01a[4B] PS_ERROR_OUT_M2C
14-FPGA-01a[4B] PS_ERROR_STATUS_M2C
MODE PINS
Quad-SPI (32b)
14-FPGA-01a[2B] MODE0_C2M
14-FPGA-01a[2B] MODE1_C2M
14-FPGA-01a[2B] MODE2_C2M
14-FPGA-01a[2B] MODE3_C2M
R134
499_1%_0402
R135
499_1%_0402
R136
DNI_499_1%_0402
R137
499_1%_0402
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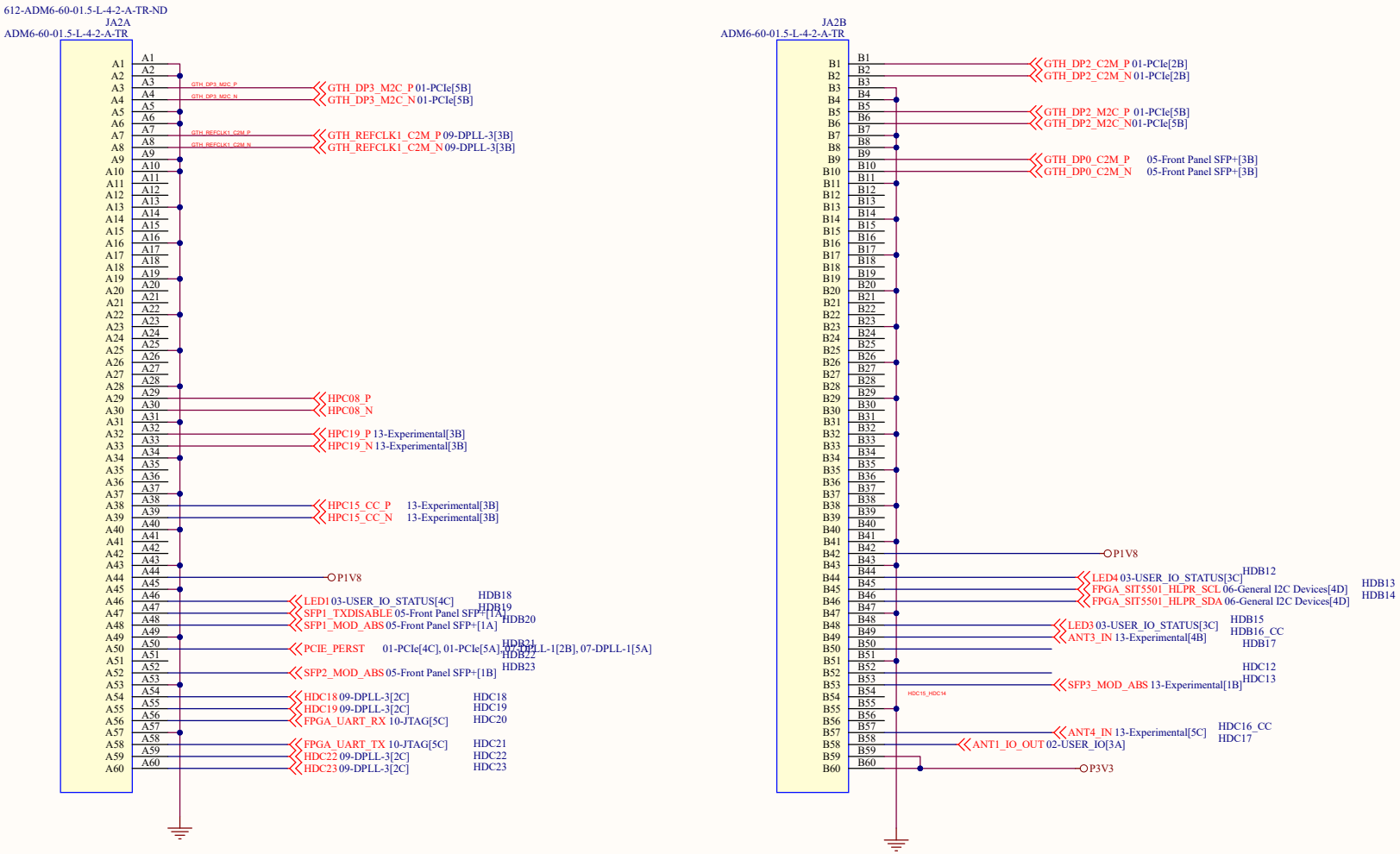

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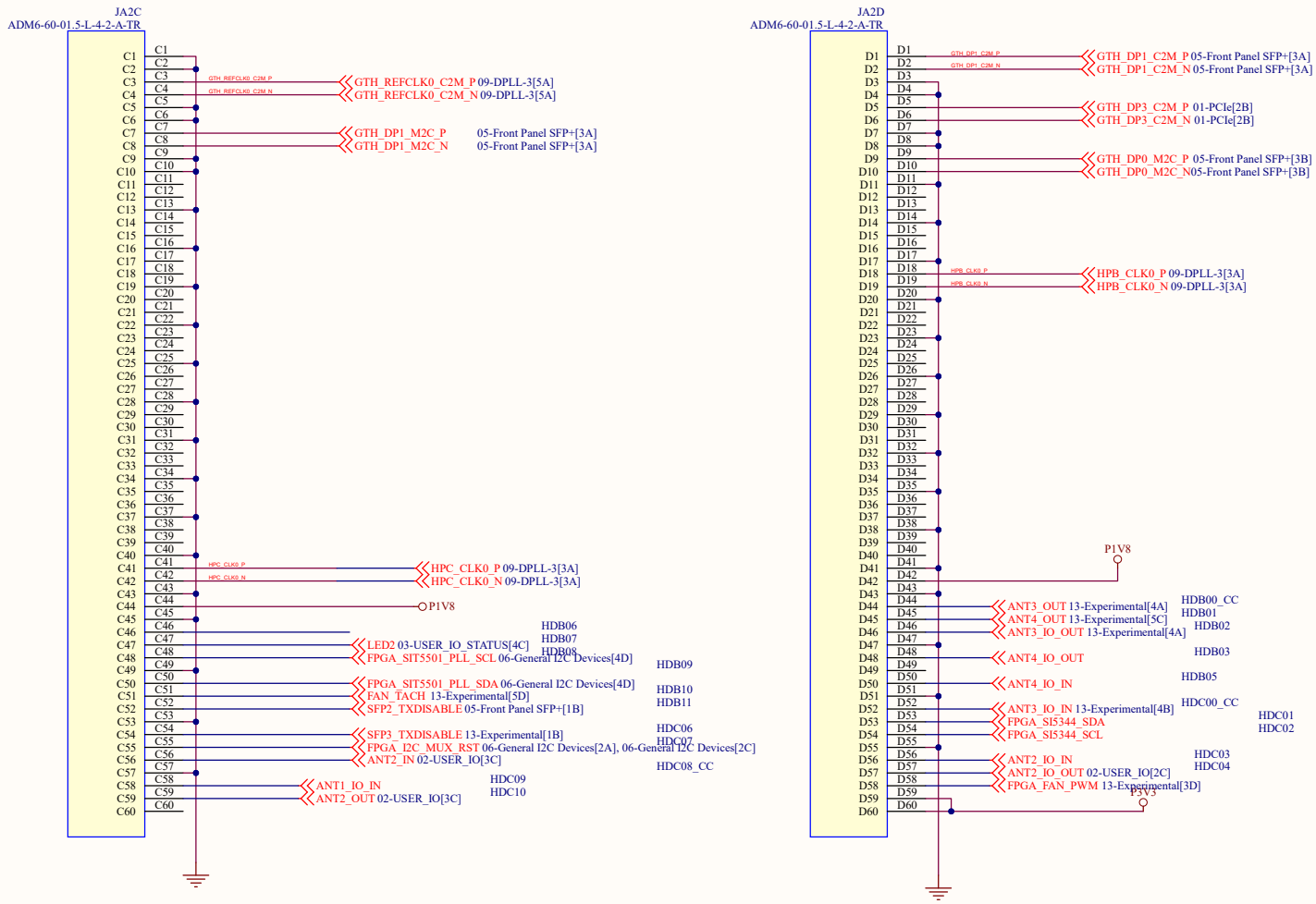

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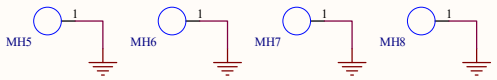

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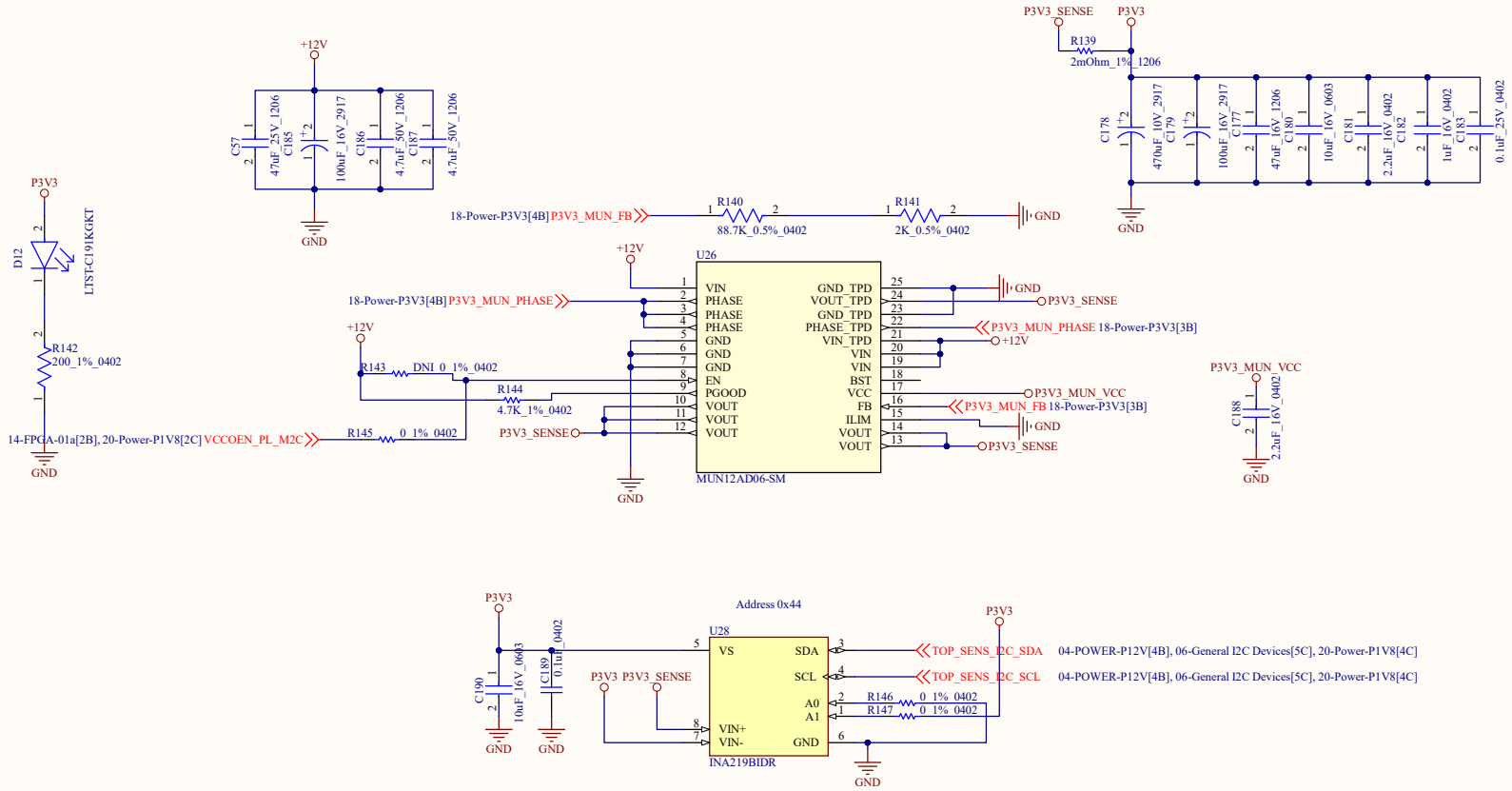

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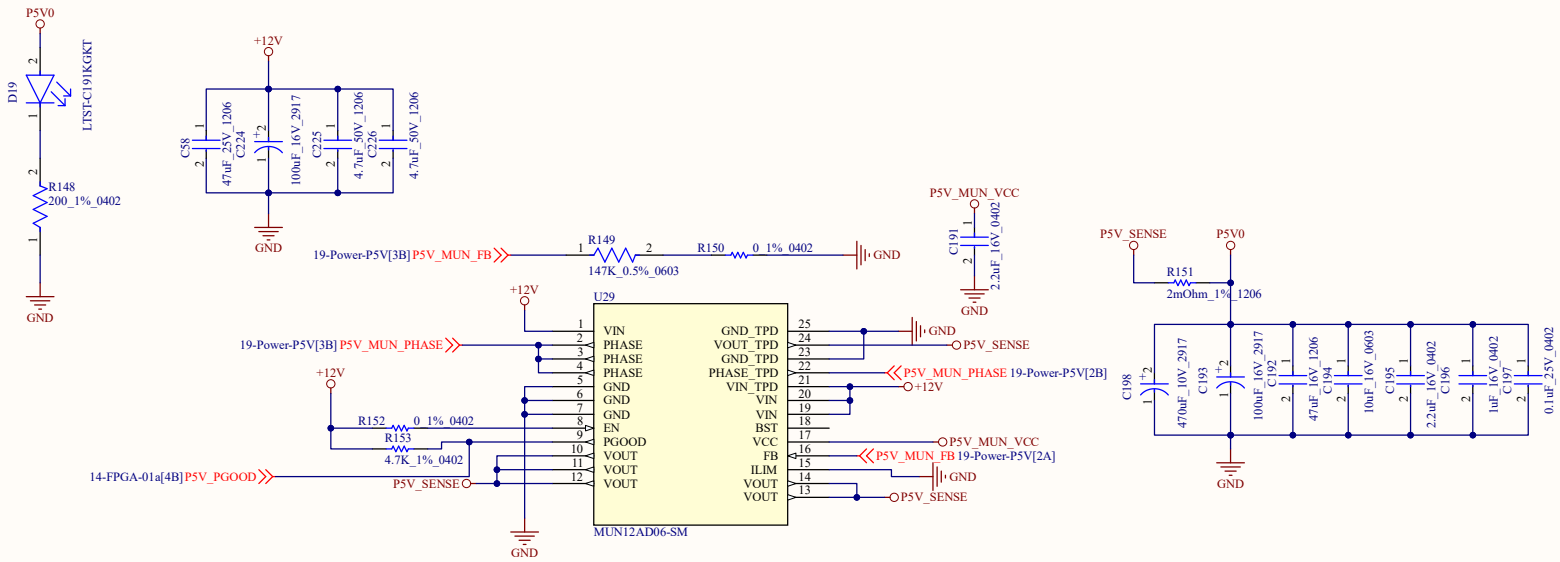

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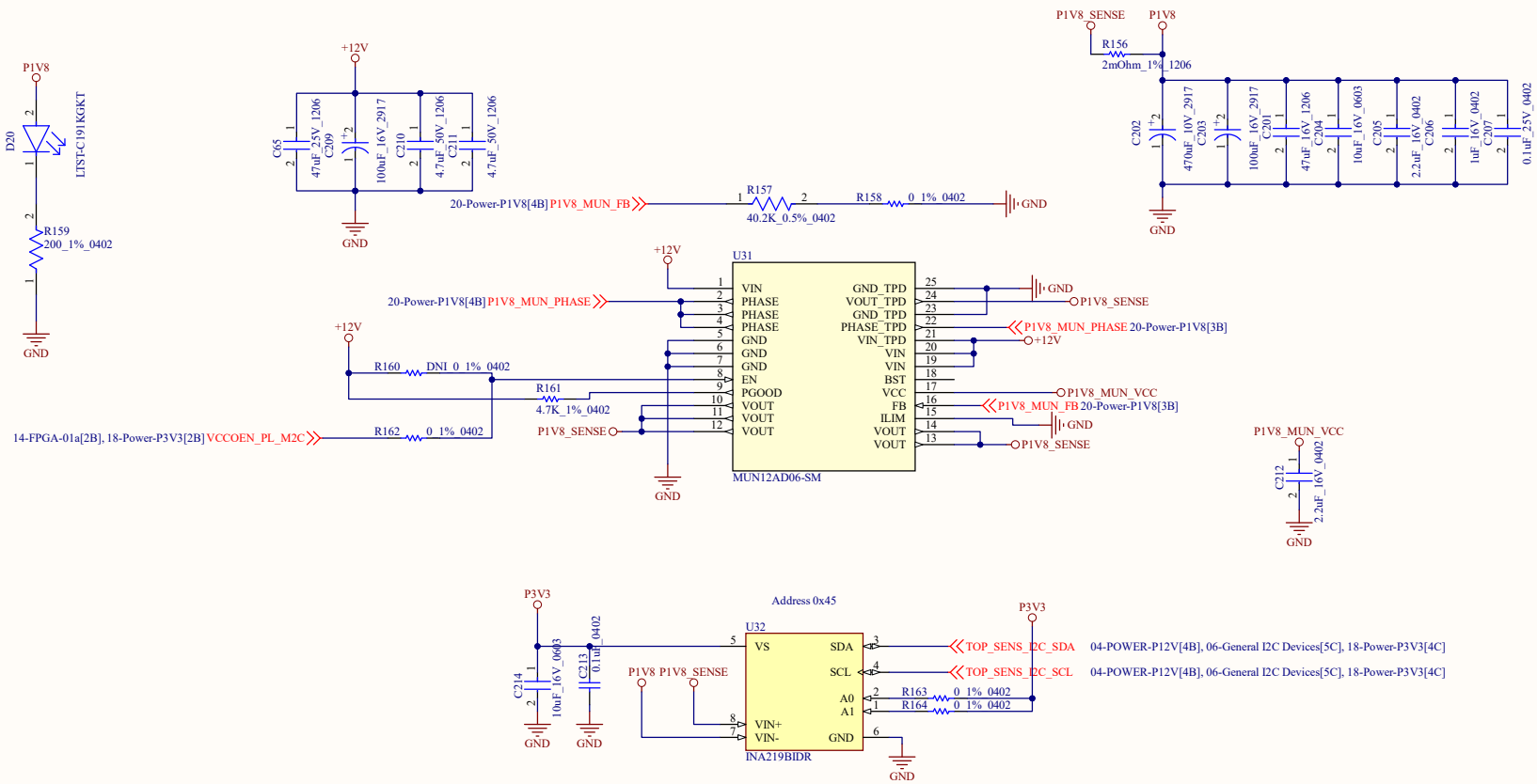

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