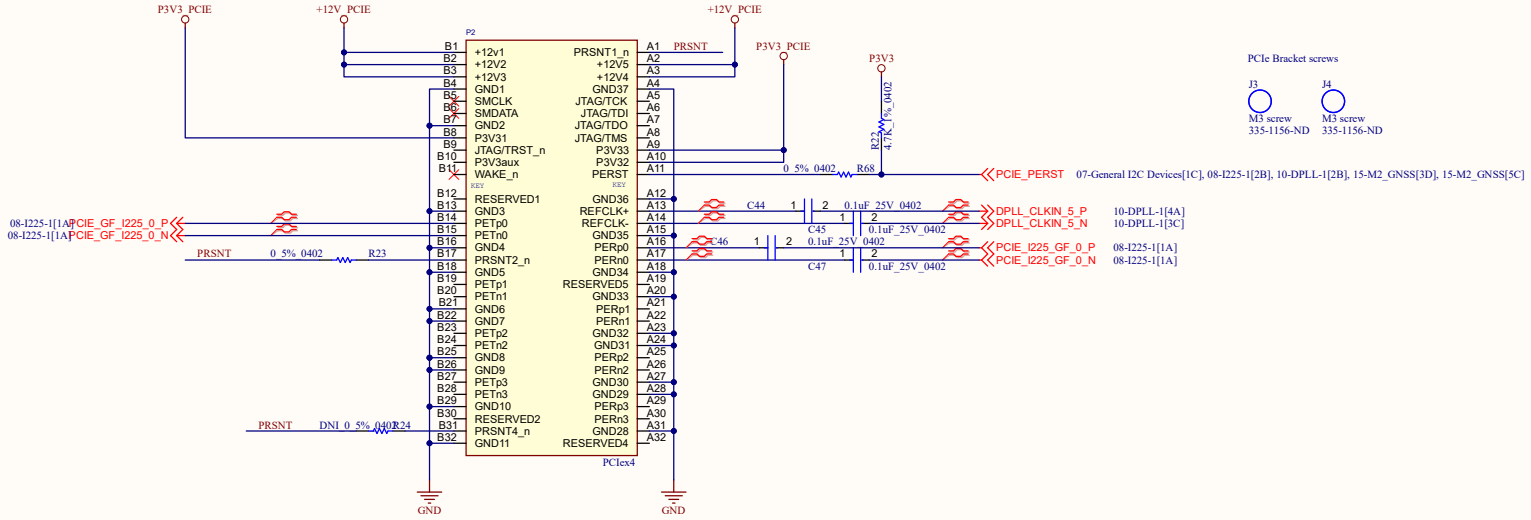
PCIe Connector



Cannot open file C:\Users\beta\Desktop\Timecard Logo\TIMECARD.jpg. File does not exist.

REV	DATE
P3	09/14/21

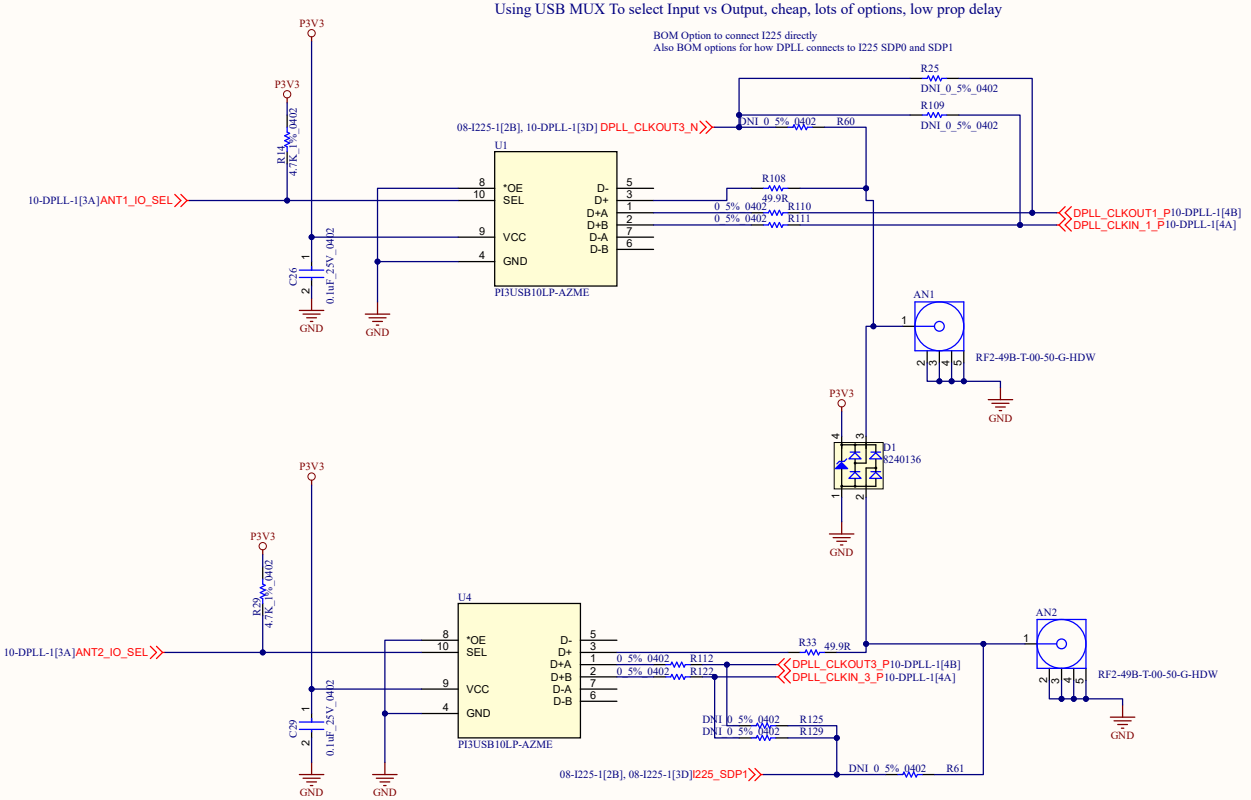
timingcard.com

SHEET 1 OF 14

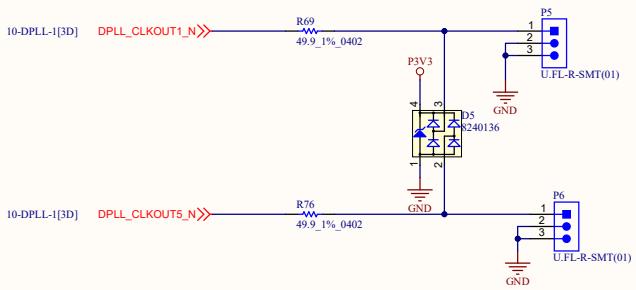
INPUT/OUTPUT SMA

Using USB MUX To select Input vs Output, cheap, lots of options, low prop delay

BOM Option to connect I225 directly
Also BOM options for how DPLL connects to I225 SDP0 and SDP1



Unused DPLL outputs to U.FL



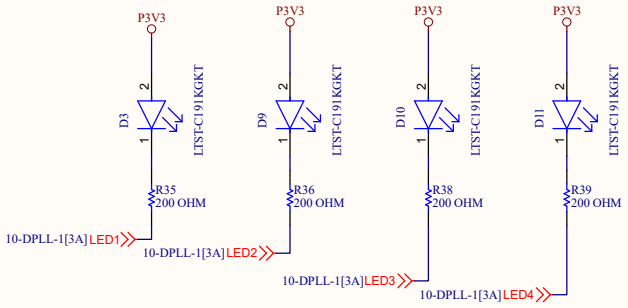
Cannot open file C:\Users\beta\Desktop\Timecard Logo\TIMECARD.jpg. File does not exist.

REV P3 DATE 09/14/21

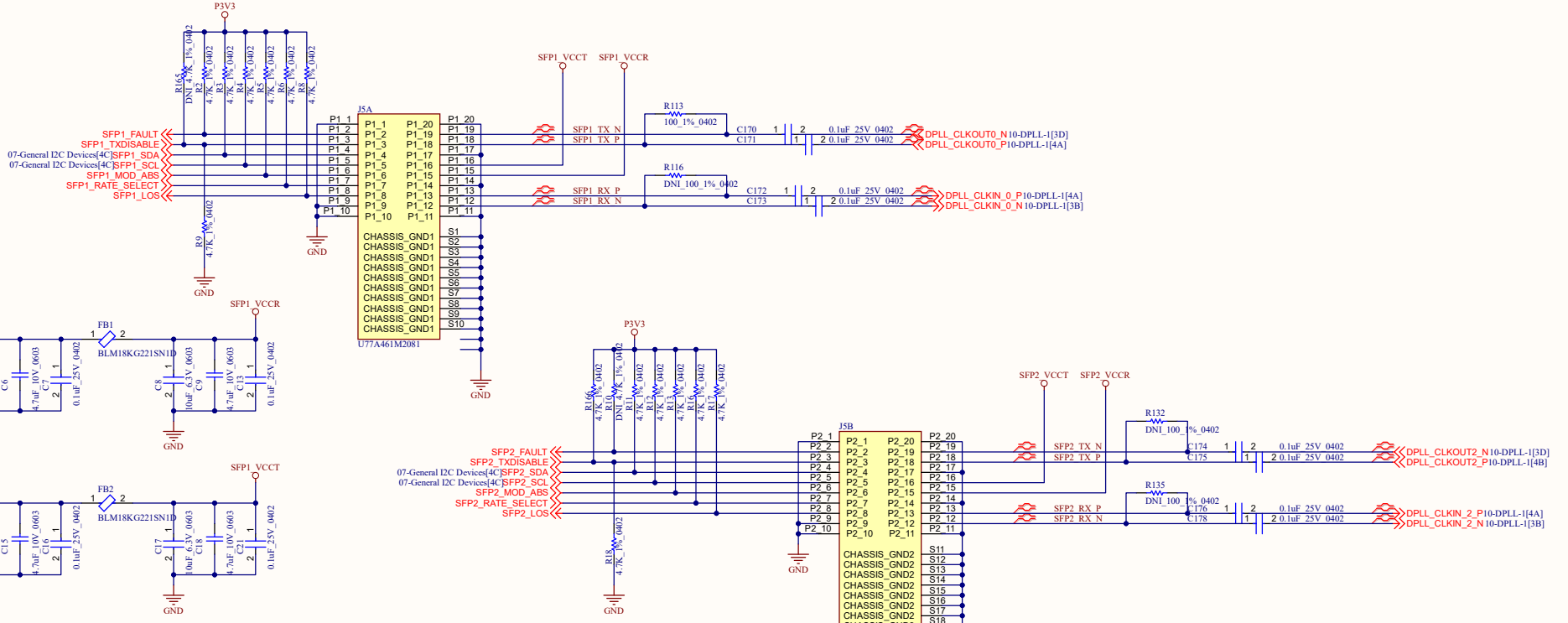
timingcard.com

SHEET 2 OF 14

SYSTEM STATUS LEDS



Title		
Size: B	Number	Revision
Date: 8/27/2023		Sheet of
File: C:\Users\..\03-USER_IO_STATUS.SchDoc		Drawn By:

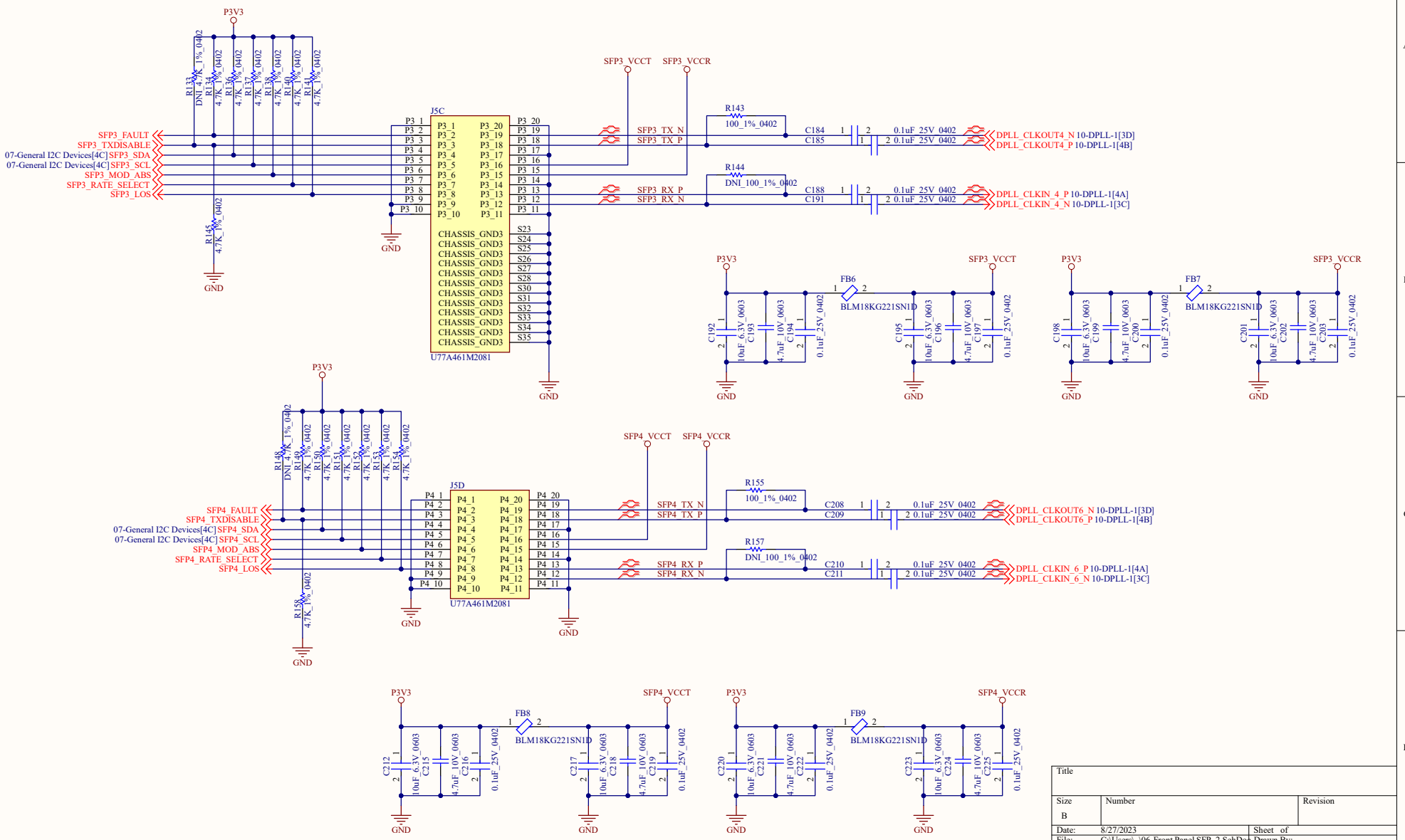


Cannot open file C:\Users\beta\Desktop\Timecard Logo\TIMECARD.jpg. File does not exist.

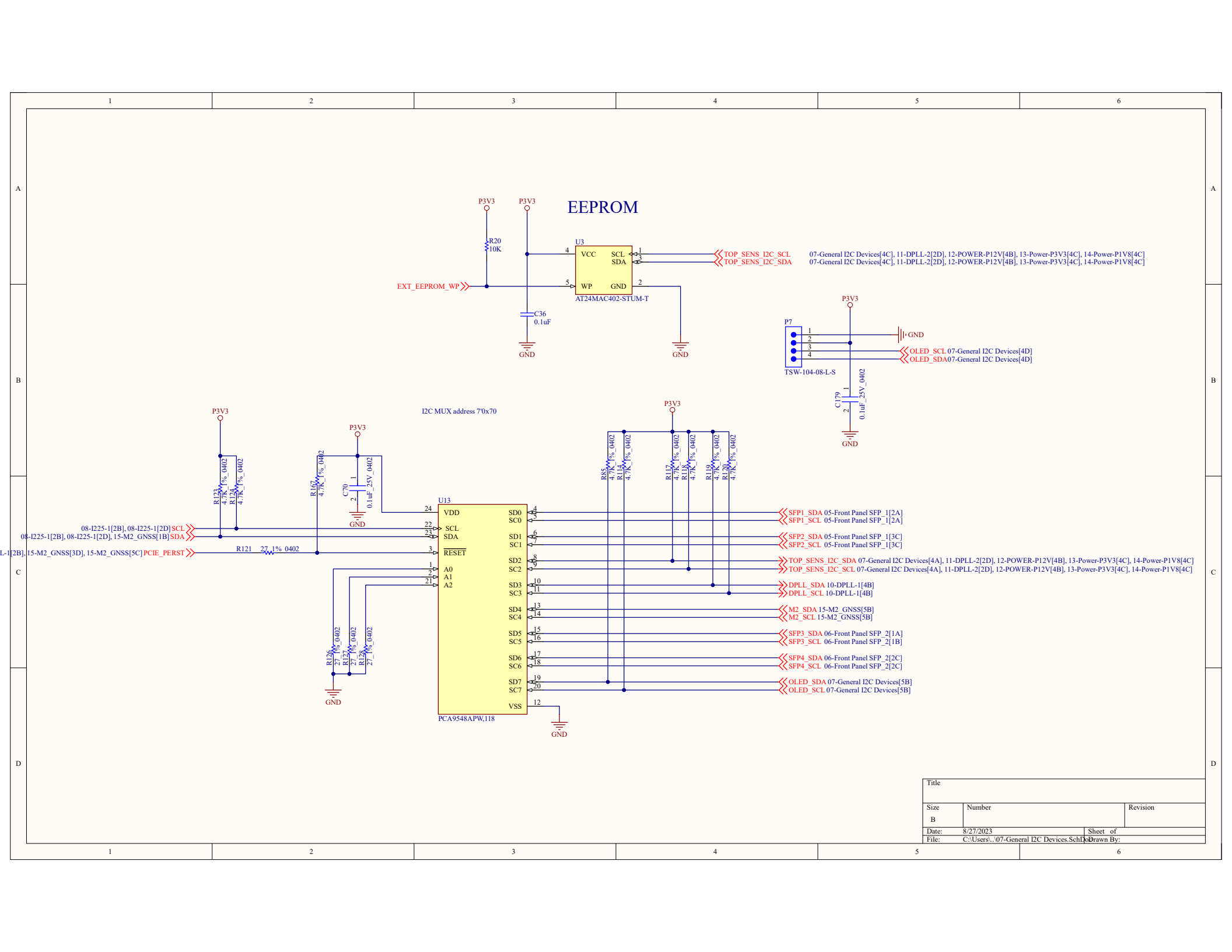
REV P3 DATE 09/14/21

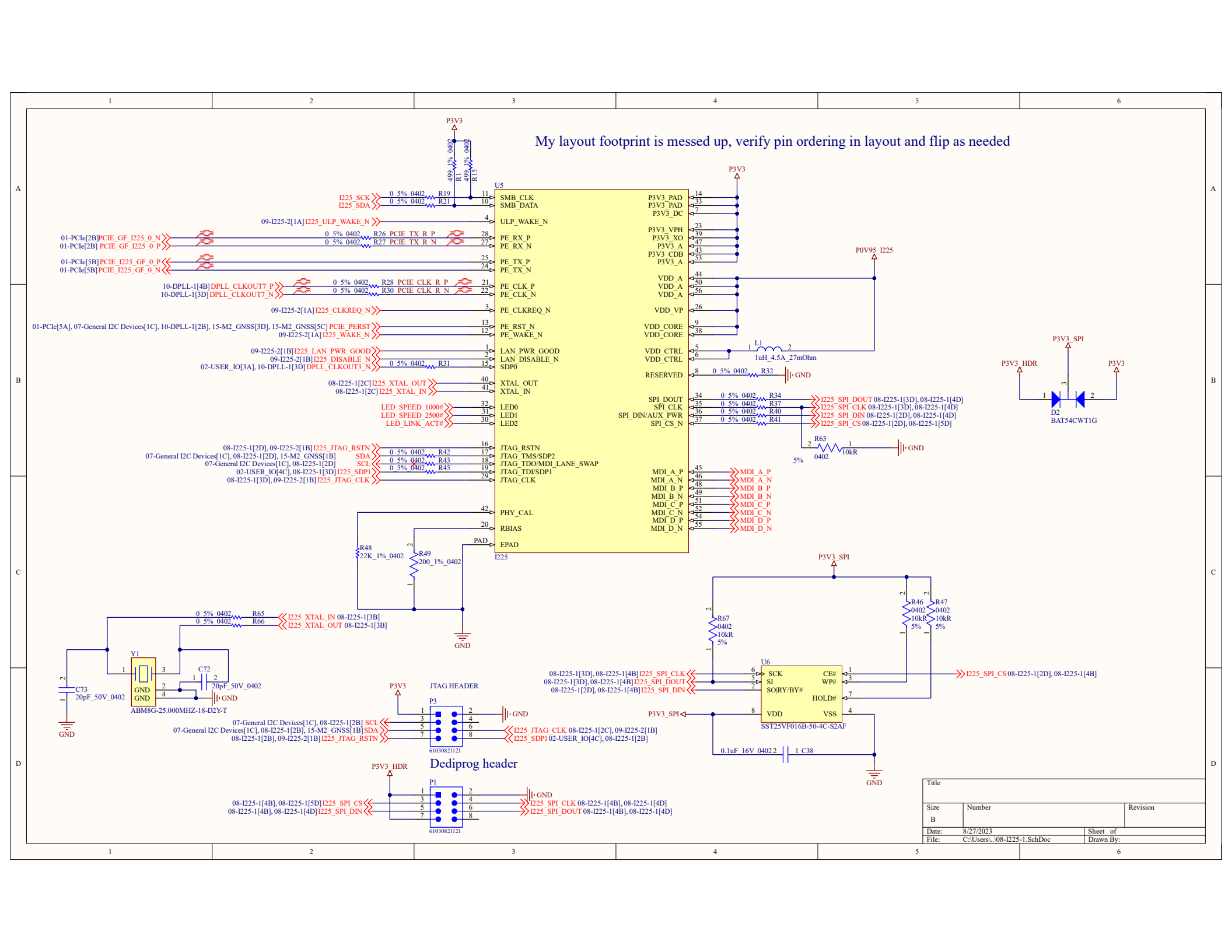
timingcard.com

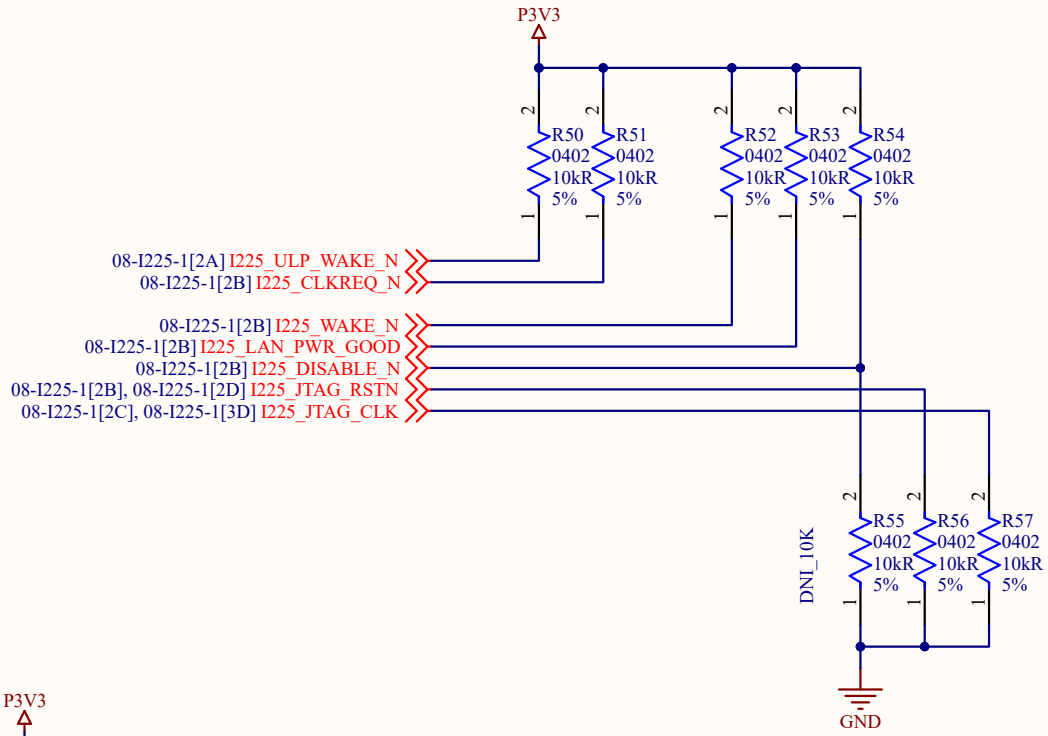
SHEET 4 OF 14

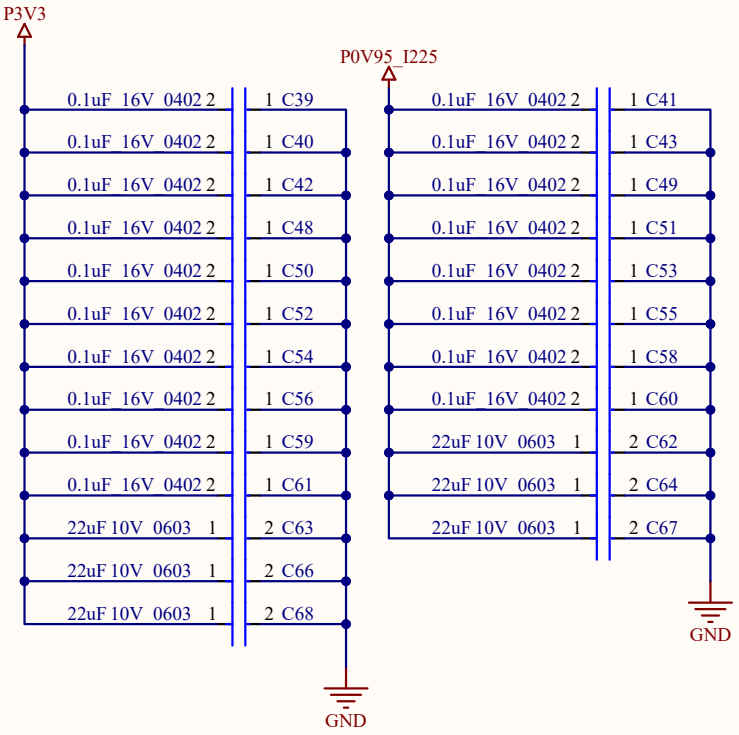


Title		
Size: B	Number	Revision
Date: 8/27/2023		Sheet of
File: C:\Users\..\06-Front Panel SFP_2.SchDoc		Drawn By:

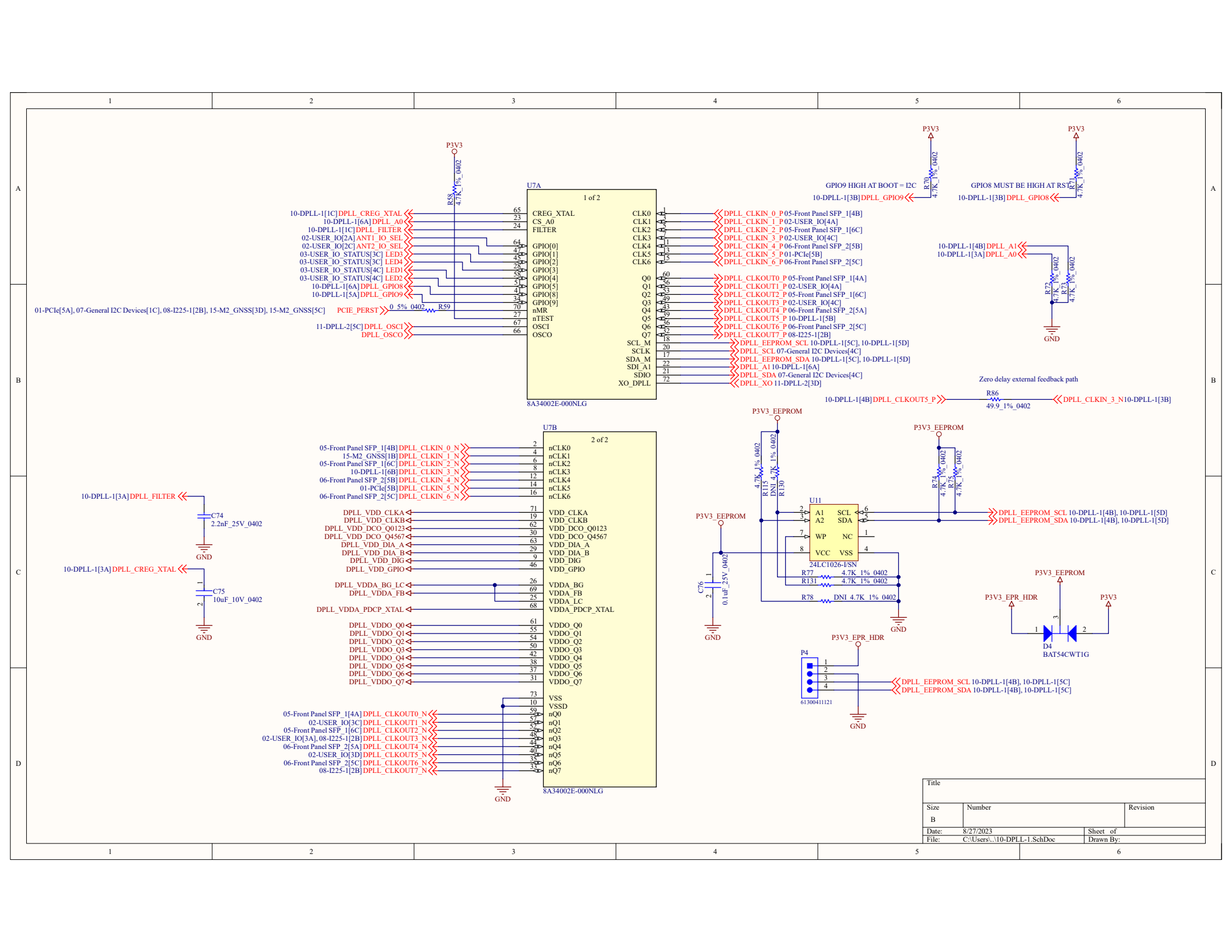

EEPROM
P3V3
P3V3
R20
10K
U3
VCC
SCL
SDA
WP
GND
AT24MAC402-STUM-T
EXT_EEPROM_WP
C36
0.1uF
GND
GND
TOP_SENS_I2C_SCL
TOP_SENS_I2C_SDA
07-General I2C Devices[4C], 11-DPLL-2[2D], 12-POWER-P12V[4B], 13-Power-P3V3[4C], 14-Power-P1V8[4C]
07-General I2C Devices[4C], 11-DPLL-2[2D], 12-POWER-P12V[4B], 13-Power-P3V3[4C], 14-Power-P1V8[4C]
P7
TSW-104-08-L-S
GND
OLED_SCL 07-General I2C Devices[4D]
OLED_SDA07-General I2C Devices[4D]
C179
0.1uF_25V_0402
GND
I2C MUX address 7'0x70
P3V3
P3V3
P3V3
R123
4.7K_1%_0402
R124
4.7K_1%_0402
R16
4.7K_1%_0402
C70
0.1uF_25V_0402
GND
R85
4.7K_1%_0402
R114
4.7K_1%_0402
R117
4.7K_1%_0402
R118
4.7K_1%_0402
R119
4.7K_1%_0402
R120
4.7K_1%_0402
U13
VDD
SCL
SDA
RESET
A0
A1
A2
VSS
SD0
SC0
SD1
SC1
SD2
SC2
SD3
SC3
SD4
SC4
SD5
SC5
SD6
SC6
SD7
SC7
PCA9548APW,118
GND
08-I225-1[2B], 08-I225-1[2D] SCL
08-I225-1[2B], 08-I225-1[2D], 15-M2_GNSS[1B] SDA
L-1[2B], 15-M2_GNSS[3D], 15-M2_GNSS[5C] PCIE_PERST
R121 27.1% 0402
R125
27.1%_0402
R126
27.1%_0402
R127
27.1%_0402
R128
27.1%_0402
GND
SFP1_SDA 05-Front Panel SFP_1[2A]
SFP1_SCL 05-Front Panel SFP_1[2A]
SFP2_SDA 05-Front Panel SFP_1[3C]
SFP2_SCL 05-Front Panel SFP_1[3C]
TOP_SENS_I2C_SDA 07-General I2C Devices[4A], 11-DPLL-2[2D], 12-POWER-P12V[4B], 13-Power-P3V3[4C], 14-Power-P1V8[4C]
TOP_SENS_I2C_SCL 07-General I2C Devices[4A], 11-DPLL-2[2D], 12-POWER-P12V[4B], 13-Power-P3V3[4C], 14-Power-P1V8[4C]
DPLL_SDA 10-DPLL-1[4B]
DPLL_SCL 10-DPLL-1[4B]
M2_SDA 15-M2_GNSS[5B]
M2_SCL 15-M2_GNSS[5B]
SFP3_SDA 06-Front Panel SFP_2[1A]
SFP3_SCL 06-Front Panel SFP_2[1B]
SFP4_SDA 06-Front Panel SFP_2[2C]
SFP4_SCL 06-Front Panel SFP_2[2C]
OLED_SDA 07-General I2C Devices[5B]
OLED_SCL 07-General I2C Devices[5B]
Title
Size
B
Number
Revision
Date: 8/27/2023
Sheet of
File: C:\Users\..\07-General I2C Devices.SchDoc
Drawn By:

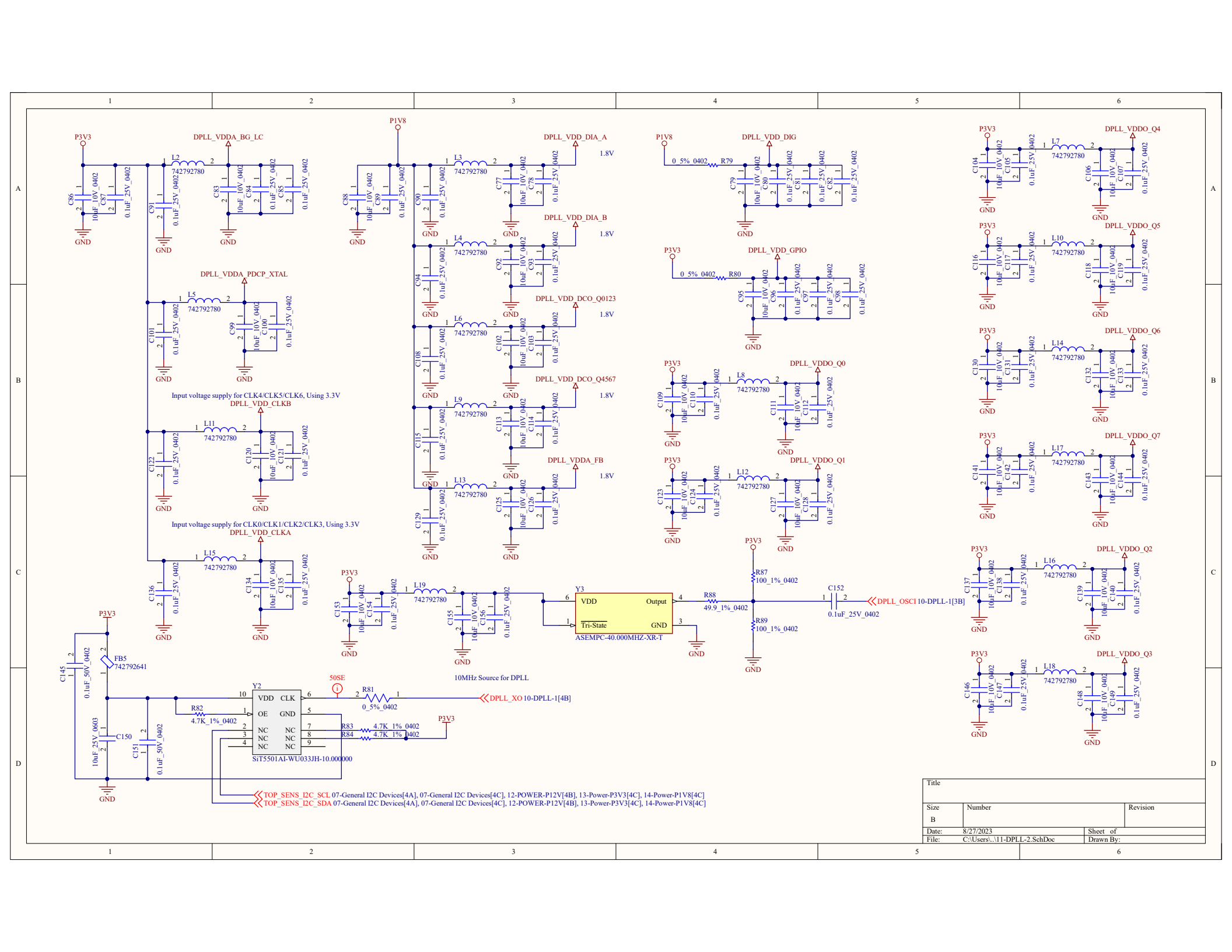

My layout footprint is messed up, verify pin ordering in layout and flip as needed
U5
I225
SMB_CLK
SMB_DATA
ULP_WAKE_N
PE_RX_P
PE_RX_N
PE_TX_P
PE_TX_N
PE_CLK_P
PE_CLK_N
PE_CLKREQ_N
PE_RST_N
PE_WAKE_N
LAN_PWR_GOOD
LAN_DISABLE_N
SDP0
XTAL_OUT
XTAL_IN
LED0
LED1
LED2
JTAG_RSTN
JTAG_TMS/SDP2
JTAG_TDO/MDI_LANE_SWAP
JTAG_TDI/SDP1
JTAG_CLK
PHY_CAL
RBIAS
EPAD
PAD
P3V3_PAD
P3V3_DC
P3V3_VPH
P3V3_XO
P3V3_A
P3V3_CDB
VDD_A
VDD_VP
VDD_CORE
VDD_CTRL
RESERVED
SPI_DOUT
SPI_CLK
SPI_DIN/AUX_PWR
SPI_CS_N
MDI_A_P
MDI_A_N
MDI_B_P
MDI_B_N
MDI_C_P
MDI_C_N
MDI_D_P
MDI_D_N
P3V3
P0V95_I225
L1
1uH_4.5A_27mOhm
R1
R15
R19
R21
R26
R27
R28
R30
R31
R32
R34
R37
R40
R41
R42
R43
R45
R48
22K_1%_0402
R49
200_1%_0402
R63
10kR
GND
P3V3_SPI
P3V3_HDR
D2
BAT54CWT1G
U6
SST25VF016B-50-4C-S2AF
SCK
SI
SO|RY/BY#
CE#
WP#
HOLD#
VDD
VSS
R46
R47
R67
C38
0.1uF_16V_0402
Y1
ABM8G-25.000MHZ-18-D2Y-T
C72
20pF_50V_0402
C73
20pF_50V_0402
R65
R66
P3
JTAG HEADER
P1
Dediprog header
61030821121
I225_SCK
I225_SDA
I225_ULP_WAKE_N
I225_CLKREQ_N
I225_PERST
I225_WAKE_N
I225_LAN_PWR_GOOD
I225_DISABLE_N
I225_XTAL_OUT
I225_XTAL_IN
LED_SPEED_1000#
LED_SPEED_2500#
LED_LINK_ACT#
I225_JTAG_RSTN
I225_JTAG_CLK
I225_SDP1
I225_SPI_DOUT
I225_SPI_CLK
I225_SPI_DIN
I225_SPI_CS
SCL
SDA
PCIE_GF_I225_0_N
PCIE_GF_I225_0_P
PCIE_I225_GF_0_P
PCIE_I225_GF_0_N
PCIE_TX_R_P
PCIE_TX_R_N
PCIE_CLK_R_P
PCIE_CLK_R_N
DPLL_CLKOUT7_P
DPLL_CLKOUT7_N
DPLL_CLKOUT3_N
Title
Size
B
Number
Revision
Date:
8/27/2023
Sheet of
File:
C:\Users\..\08-I225-1.SchDoc
Drawn By:

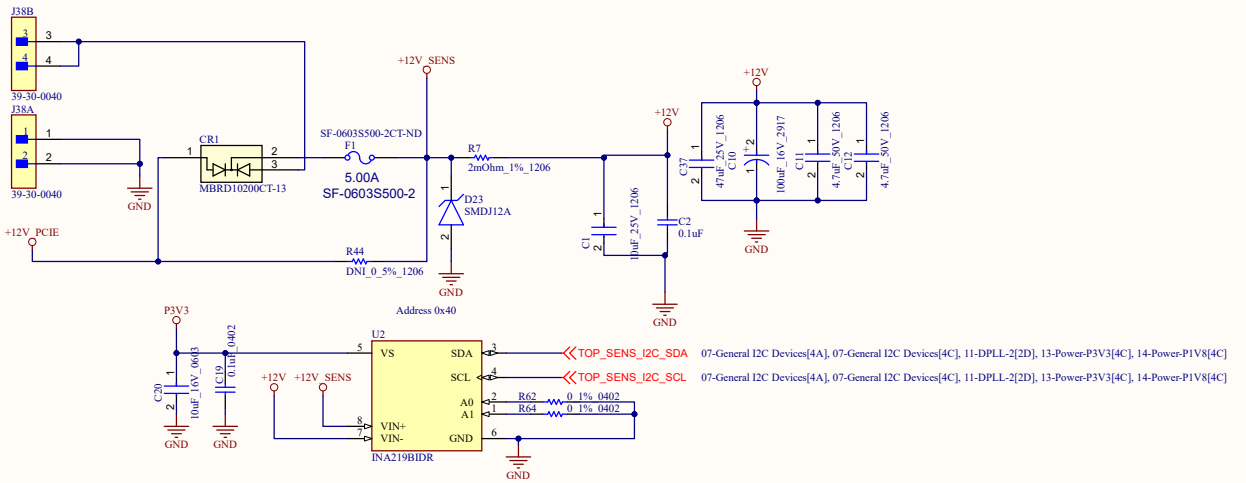




Title		
Size A	Number	Revision
Date: 8/27/2023		Sheet of
File: C:\Users\..\09-I225-2.SchDoc		Drawn By:


U7A
1 of 2
8A34002E-000NLG
U7B
2 of 2
8A34002E-000NLG
U11
24LC1026-I/SN
P4
61300411121
D4
BAT54CWT1G
P3V3
GND
P3V3_EEPROM
P3V3_EPR_HDR
Zero delay external feedback path
Title
Size
B
Number
Revision
Date: 8/27/2023
File: C:\Users\..\10-DPLL-1.SchDoc
Sheet of
Drawn By:


P3V3
DPLL_VDDA_BG_LC
L2
742792780
C86
10uF_10V_0402
C87
0.1uF_25V_0402
C91
0.1uF_25V_0402
C83
10uF_10V_0402
C84
0.1uF_25V_0402
C85
0.1uF_25V_0402
GND
DPLL_VDDA_PDCP_XTAL
L5
742792780
C101
0.1uF_25V_0402
C99
10uF_10V_0402
C100
0.1uF_25V_0402
Input voltage supply for CLK4/CLK5/CLK6, Using 3.3V
DPLL_VDD_CLKB
L11
742792780
C122
0.1uF_25V_0402
C120
10uF_10V_0402
C121
0.1uF_25V_0402
Input voltage supply for CLK0/CLK1/CLK2/CLK3, Using 3.3V
DPLL_VDD_CLKA
L15
742792780
C136
0.1uF_25V_0402
C134
10uF_10V_0402
C135
0.1uF_25V_0402
P1V8
DPLL_VDD_DIA_A
1.8V
L3
742792780
C88
10uF_10V_0402
C89
0.1uF_25V_0402
C90
0.1uF_25V_0402
C77
10uF_10V_0402
C78
0.1uF_25V_0402
DPLL_VDD_DIA_B
1.8V
L4
742792780
C94
0.1uF_25V_0402
C92
10uF_10V_0402
C93
0.1uF_25V_0402
DPLL_VDD_DCO_Q0123
1.8V
L6
742792780
C108
0.1uF_25V_0402
C102
10uF_10V_0402
C103
0.1uF_25V_0402
DPLL_VDD_DCO_Q4567
1.8V
L9
742792780
C115
0.1uF_25V_0402
C113
10uF_10V_0402
C114
0.1uF_25V_0402
DPLL_VDDA_FB
1.8V
L13
742792780
C129
0.1uF_25V_0402
C125
10uF_10V_0402
C126
0.1uF_25V_0402
P1V8
DPLL_VDD_DIG
0_5%_0402
R79
C79
10uF_10V_0402
C80
0.1uF_25V_0402
C81
0.1uF_25V_0402
C82
0.1uF_25V_0402
P3V3
DPLL_VDD_GPIO
0_5%_0402
R80
C95
10uF_10V_0402
C96
0.1uF_25V_0402
C97
0.1uF_25V_0402
C98
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q0
L8
742792780
C109
10uF_10V_0402
C110
0.1uF_25V_0402
C111
10uF_10V_0402
C112
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q1
L12
742792780
C123
10uF_10V_0402
C124
0.1uF_25V_0402
C127
10uF_10V_0402
C128
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q4
L7
742792780
C104
10uF_10V_0402
C105
0.1uF_25V_0402
C106
10uF_10V_0402
C107
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q5
L10
742792780
C116
10uF_10V_0402
C117
0.1uF_25V_0402
C118
10uF_10V_0402
C119
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q6
L14
742792780
C130
10uF_10V_0402
C131
0.1uF_25V_0402
C132
10uF_10V_0402
C133
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q7
L17
742792780
C141
10uF_10V_0402
C142
0.1uF_25V_0402
C143
10uF_10V_0402
C144
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q2
L16
742792780
C137
10uF_10V_0402
C138
0.1uF_25V_0402
C139
10uF_10V_0402
C140
0.1uF_25V_0402
P3V3
DPLL_VDDO_Q3
L18
742792780
C146
10uF_10V_0402
C147
0.1uF_25V_0402
C148
10uF_10V_0402
C149
0.1uF_25V_0402
P3V3
L19
742792780
C153
10uF_10V_0402
C154
0.1uF_25V_0402
C155
10uF_10V_0402
C156
0.1uF_25V_0402
Y3
VDD
Output
Tri-State
GND
ASEMPC-40.000MHZ-XR-T
R88
49.9_1%_0402
R87
100_1%_0402
R89
100_1%_0402
C152
0.1uF_25V_0402
DPLL_OSCI 10-DPLL-1[3B]
10MHz Source for DPLL
P3V3
FB5
742792641
C145
0.1uF_50V_0402
C150
10uF_25V_0603
C151
0.1uF_50V_0402
Y2
VDD
CLK
OE
GND
NC
NC
NC
NC
NC
SiT5501AI-WU033JH-10.000000
50SE
R81
0_5%_0402
DPLL_XO 10-DPLL-1[4B]
R82
4.7K_1%_0402
R83
4.7K_1%_0402
R84
4.7K_1%_0402
P3V3
TOP_SENS_I2C_SCL 07-General I2C Devices[4A], 07-General I2C Devices[4C], 12-POWER-P12V[4B], 13-Power-P3V3[4C], 14-Power-P1V8[4C]
TOP_SENS_I2C_SDA 07-General I2C Devices[4A], 07-General I2C Devices[4C], 12-POWER-P12V[4B], 13-Power-P3V3[4C], 14-Power-P1V8[4C]
Title
Size
B
Number
Revision
Date: 8/27/2023
Sheet of
File: C:\Users\..\11-DPLL-2.SchDoc
Drawn By:

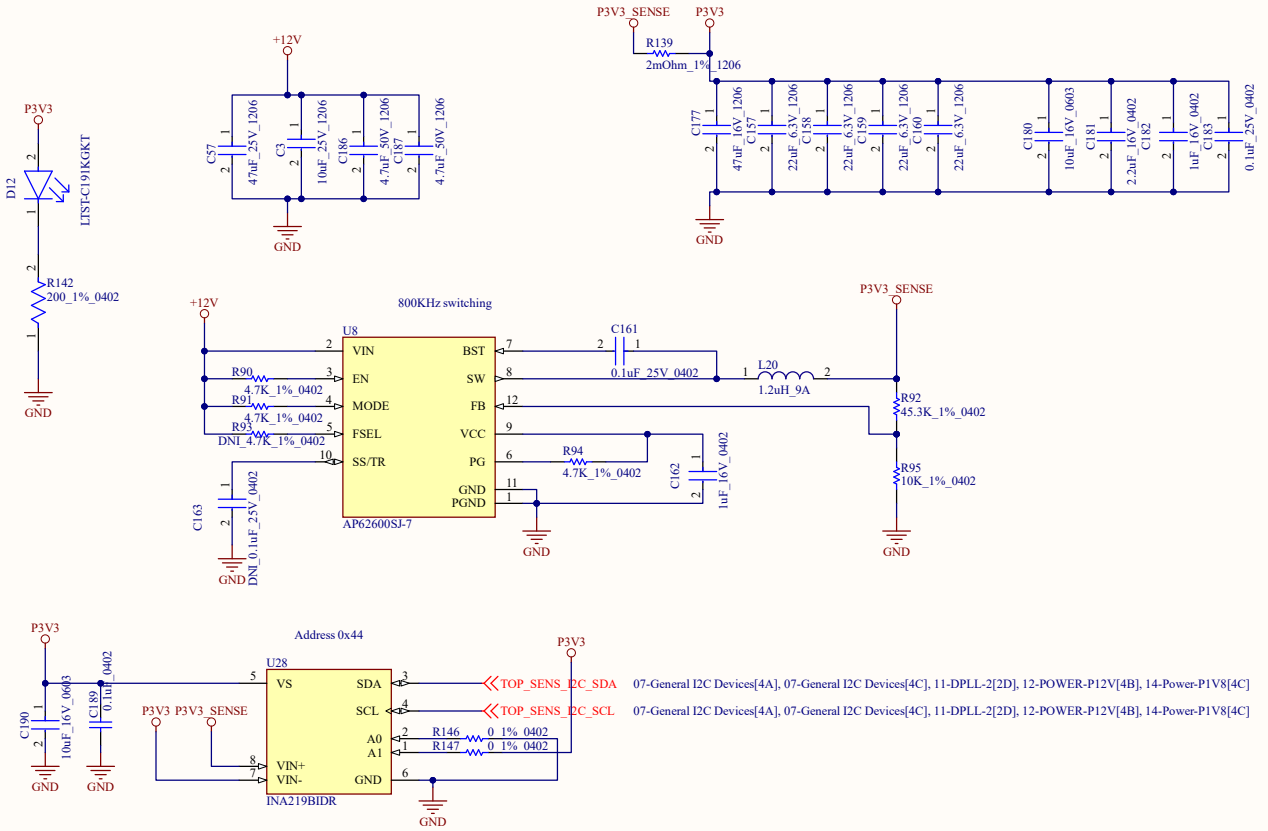


Cannot open file C:\Users\beta\Desktop\Timecard Logo\TIMECARD.jpg. File does not exist.

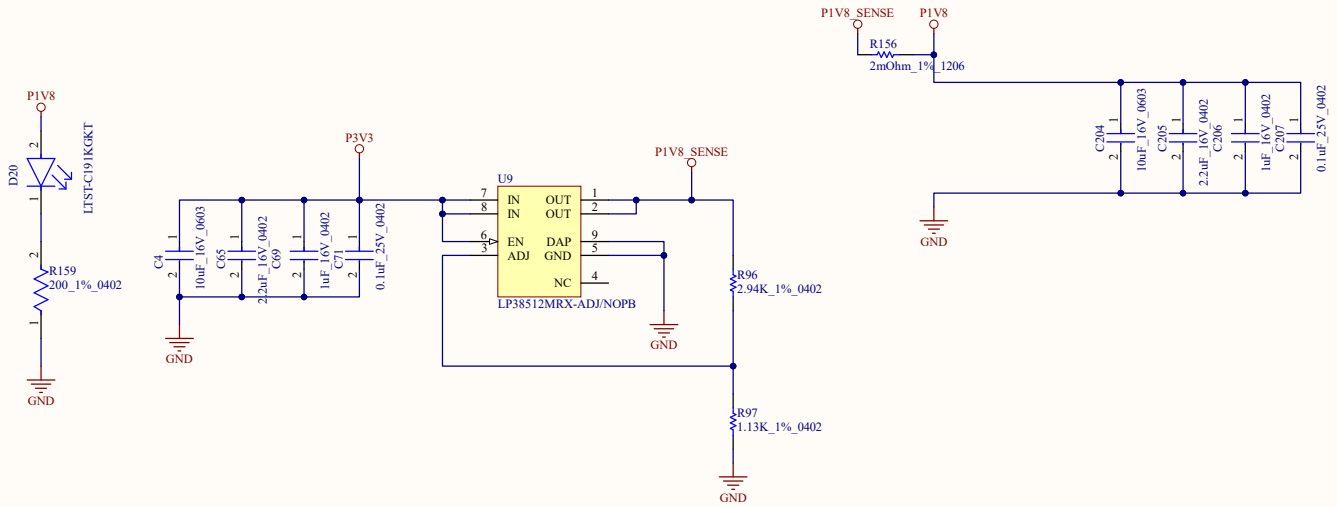
REV P3 DATE 09/14/21

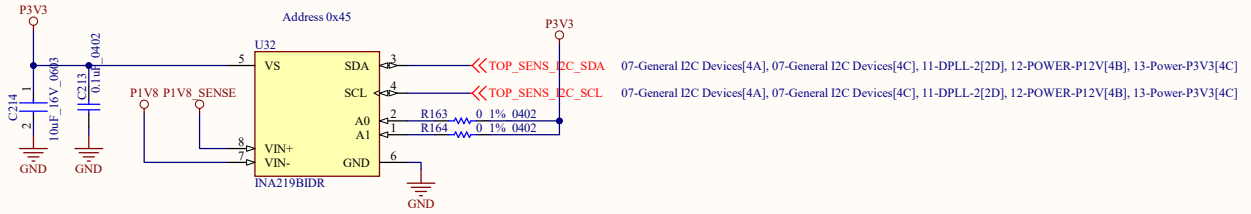
timingcard.com

SHEET 11 OF 14



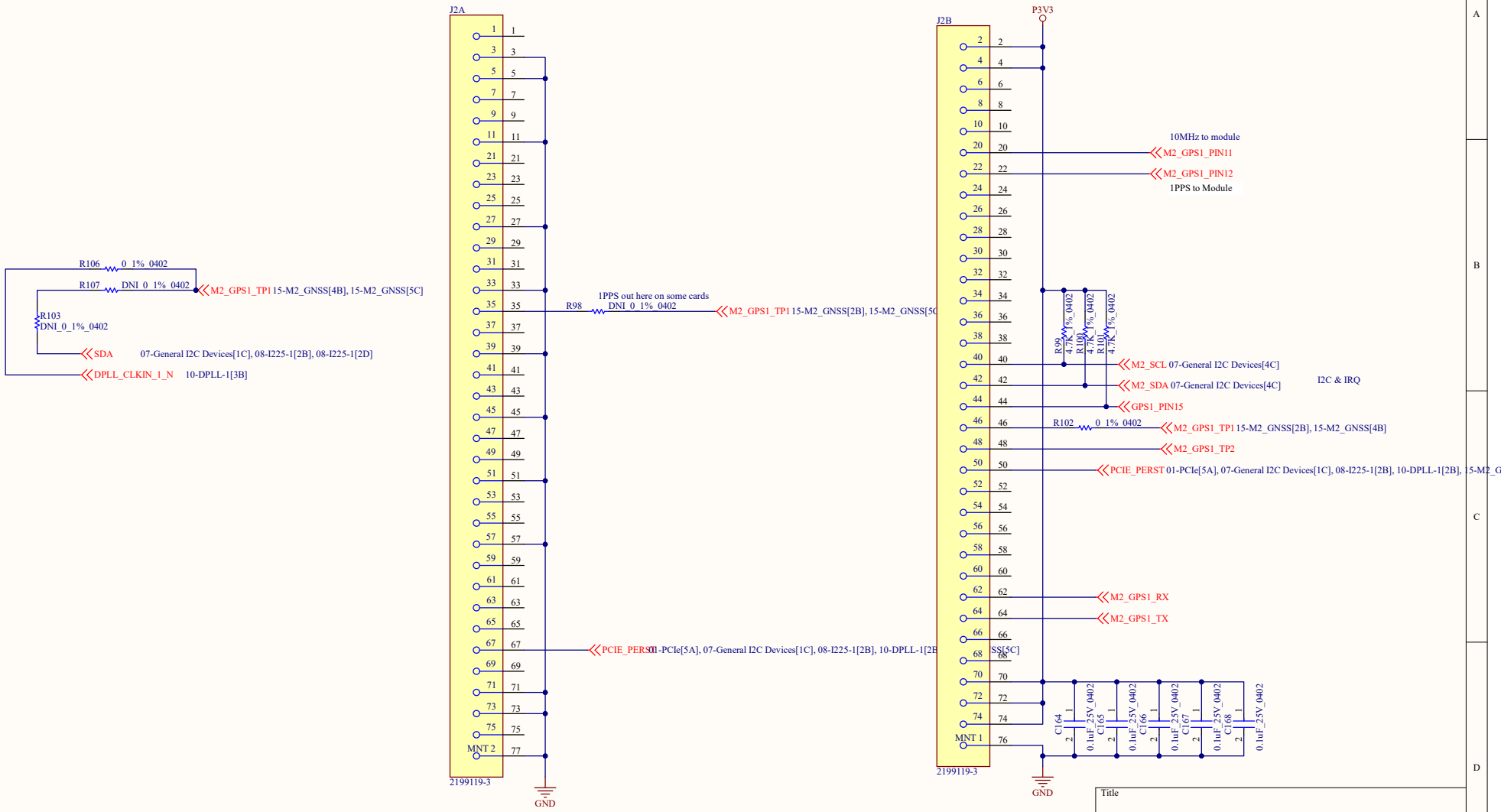
Title		
Size: B	Number	Revision
Date: 8/27/2023		Sheet of
File: C:\Users\..\13-Power-P3V3.SchDoc		Drawn By:





Title		
Size: B	Number	Revision
Date: 8/27/2023		Sheet of
File: C:\Users\..\14-Power-P1V8.SchDoc		Drawn By:

Socket 2 Key B PCIe-based WWAN Adapter Pinout , table 3-21 in M.2 spec



Title		
Size: B	Number	Revision
Date: 8/27/2023		Sheet of
File: C:\Users\..\15-M2_GNSS.SchDoc		Drawn By: