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| | |
|---|---|
| TITLE: | TIME CARD |
| DESCRIPTION: | X4 PCIE TIME CARD |

| | |
|---|---|
| DESIGNER: | BHUMARIN I., ZUJIAN ZHAO |
| REVIEWER: | BHOOSHAN URVA |
| APPROVER: | BHOOSHAN URVA |

R4006-G0001-03-SC REV2.0

MP: - SCHEMATIC RELEASE DATE: SEP 02, 2022.
- SCHEMATIC RELEASE FOR PCBA CPN: R4006-G0001-03 REV03.

PCB CPN: R4006-B0001-02_R01.

BOM NOTE: - MANUALLY CHANGE U34 FROM G222-00082-01 TO G229-10017-01 FOR THE BOM FILE.
- MANUALLY CHANGE U23 FROM G221-10224-01 TO G221-10359-01 FOR THE BOM FILE.

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: BHUMARIN I., ZUJIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 [MP] |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
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A3 (297X420)

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| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: BHUMARIN I., ZUJIAN ZHAO |
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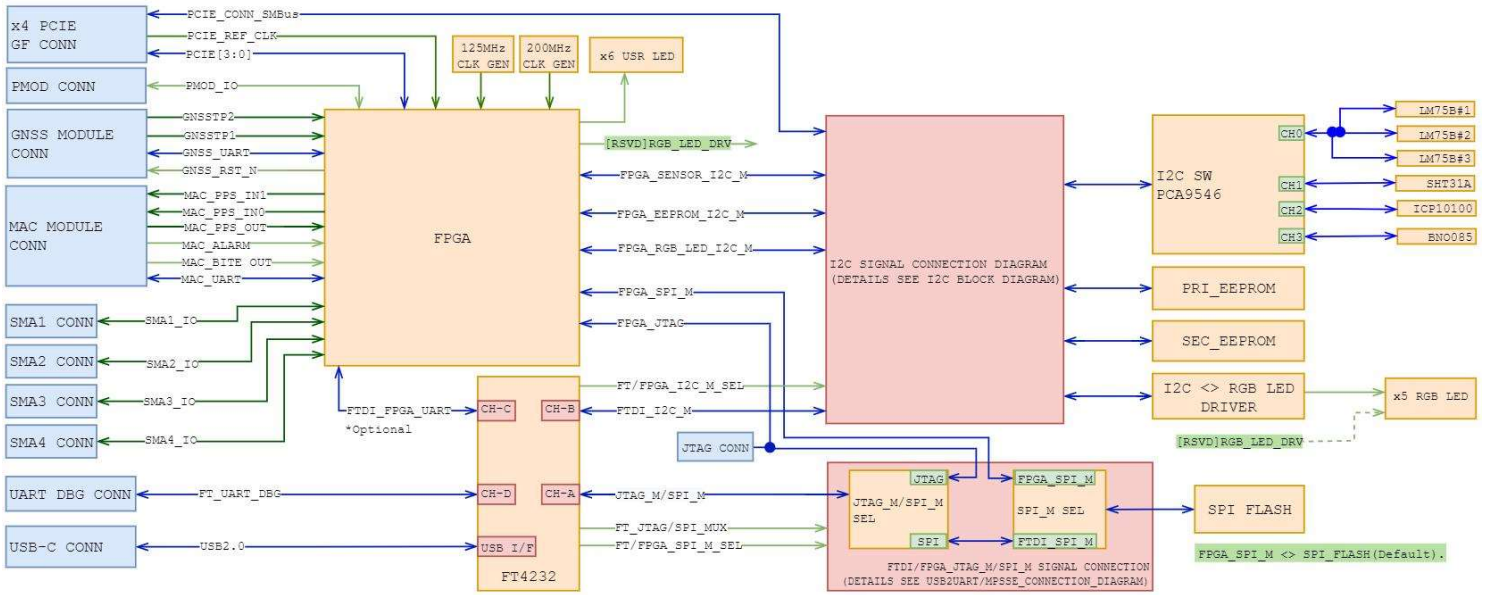
# SYS_BLOCK_DIAGRAM




| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
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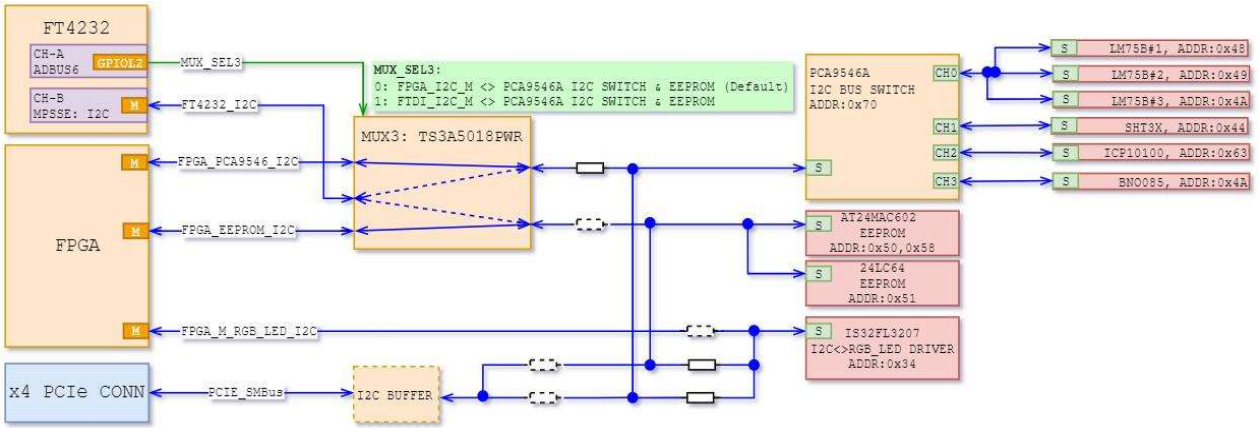
# I2C_BLOCK_DIAGRAM




| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: BHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
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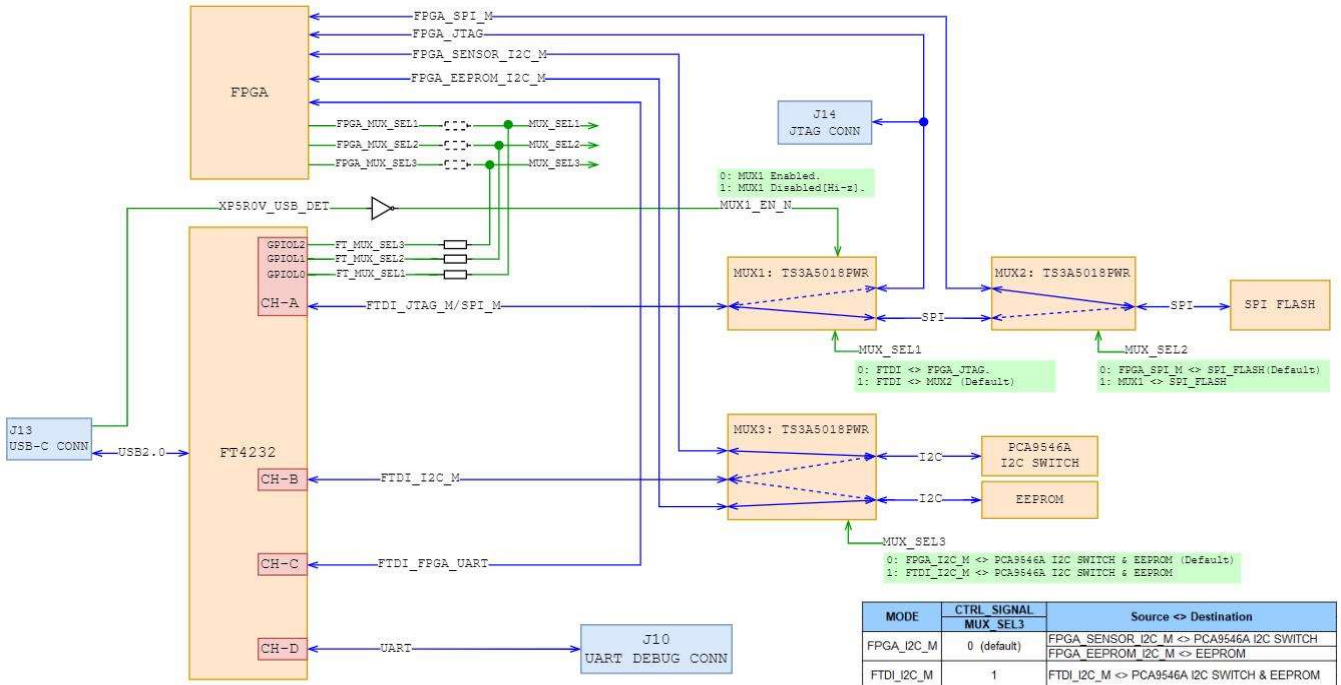
# USB2UART/MPSSE_CONNECTION_DIAGRAM




| MODE | CTRL_SIGNAL MUX_SEL3 | Source <> Destination |
|---|---|---|
| FPGA_I2C_M | 0 (default) | FPGA_SENSOR_I2C_M <> PCA9546A I2C SWITCH |
| | | FPGA_EEPROM_I2C_M <> EEPROM |
| FTDI_I2C_M | 1 | FTDI_I2C_M <> PCA9546A I2C SWITCH & EEPROM |
| | | |

| MODE | CTRL_SIGNAL MUX_SEL1 | CTRL_SIGNAL MUX_SEL2 | Source <> Destination | COMMENT |
|---|---|---|---|---|
| FTDI_JTAG_M | 0 | 0 | FTDI_JTAG<>FPGA<>SPI_FLASH | Use the FTDI chip as JTAG master to program the SPI flash by JTAG. |
| FTDI_JTAG_M | 0 | 1 | FTDI_JTAG_M <> FPGA_JTAG | FTDI JTAG master <> FPGA. |
| FPGA_SPI_M | 1 | 0 | FPGA_SPI_M <> SPI_FLASH | FPGA <> SPI flash config (Default) |
| FTDI_SPI_M | 1 | 1 | FTDI_SPI_M <> SPI_FLASH | FTDI SPI master <> SPI flash |
| | | | | |

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: BHUMARIN I., ZUTIAN ZHAO |
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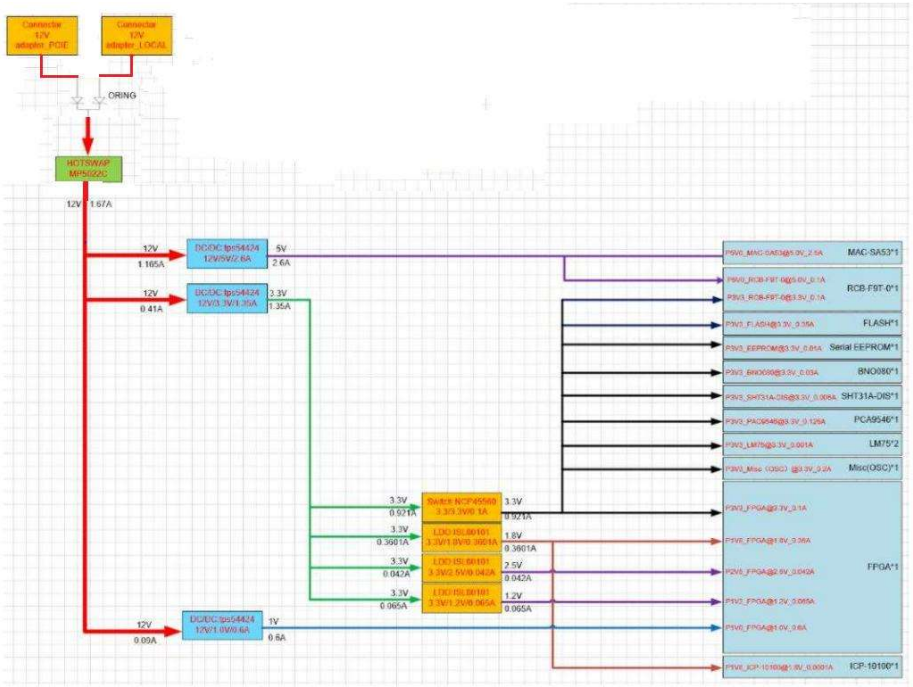
# PWR_BLOCK_DIAGRAM




PWR_BLOCK_DIAGRAM

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
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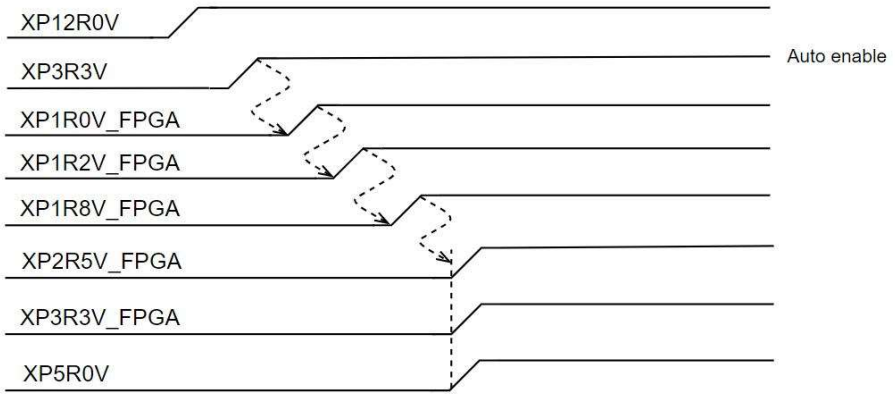
# PWR_SEQ_DIAGRAM




PWR_SEQ_DIAGRAM

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
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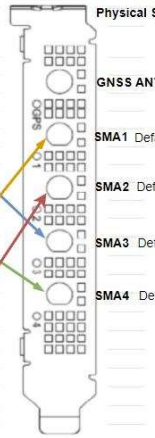
# FPGA<>SMA CONN MAPPING

**EVT**

| FPGA pin | Signal name | Buffer IC | SMA CONN |
|---|---|---|---|
| J15 | SMA1_SIG_OUT_BF_EN_N | U13 | J1 |
| W11 | ANT1_OUT | | |
| H15 | SMA1_SIG_IN_BF_EN_N | | |
| Y11 | ANT1_IN | | |
| | | | |
| H14 | SMA2_SIG_OUT_BF_EN_N | U14 | J2 |
| W12 | ANT2_OUT | | |
| J14 | SMA2_SIG_IN_BF_EN_N | | |
| Y12 | ANT2_IN | | |
| | | | |
| K13 | SMA3_SIG_OUT_BF_EN_N | U15 | J3 |
| V10 | ANT3_OUT | | |
| K14 | SMA3_SIG_IN_BF_EN_N | | |
| AA21 | ANT3_IN | | |
| | | | |
| M13 | SMA4_SIG_OUT_BF_EN_N | U16 | J4 |
| W10 | ANT4_OUT | | |
| L13 | SMA4_SIG_IN_BF_EN_N | | |
| AA20 | ANT4_IN | | |



Physical SMA CONN

GNSS ANT

**SMA1** Default = 10MHz Out

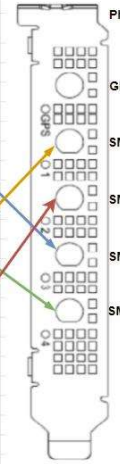
**SMA2** Default = 1PPS Out

**SMA3** Default = 10MHz In

**SMA4** Default = 1PPS In

**DVT**

| FPGA pin | Signal name | Buffer IC | SMA CONN |
|---|---|---|---|
| J15 | SMA3_SIG_OUT_BF_EN_N | U13 | J1 |
| W11 | ANT3_OUT | | |
| H15 | SMA3_SIG_IN_BF_EN_N | | |
| Y11 | ANT3_IN | | |
| | | | |
| H14 | SMA4_SIG_OUT_BF_EN_N | U14 | J2 |
| W12 | ANT4_OUT | | |
| J14 | SMA4_SIG_IN_BF_EN_N | | |
| Y12 | ANT4_IN | | |
| | | | |
| K13 | SMA1_SIG_OUT_BF_EN_N | U15 | J3 |
| V10 | ANT1_OUT | | |
| K14 | SMA1_SIG_IN_BF_EN_N | | |
| AA21 | ANT1_IN | | |
| | | | |
| M13 | SMA2_SIG_OUT_BF_EN_N | U16 | J4 |
| W10 | ANT2_OUT | | |
| L13 | SMA2_SIG_IN_BF_EN_N | | |
| AA20 | ANT2_IN | | |



Physical SMA CONN

GNSS ANT

**SMA1** Default = 10MHz Out

**SMA2** Default = 10MHz In

**SMA3** Default = 1PPS In

**SMA4** Default = 1PPS Out

FPGA<>SMA CONN MAPPING

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
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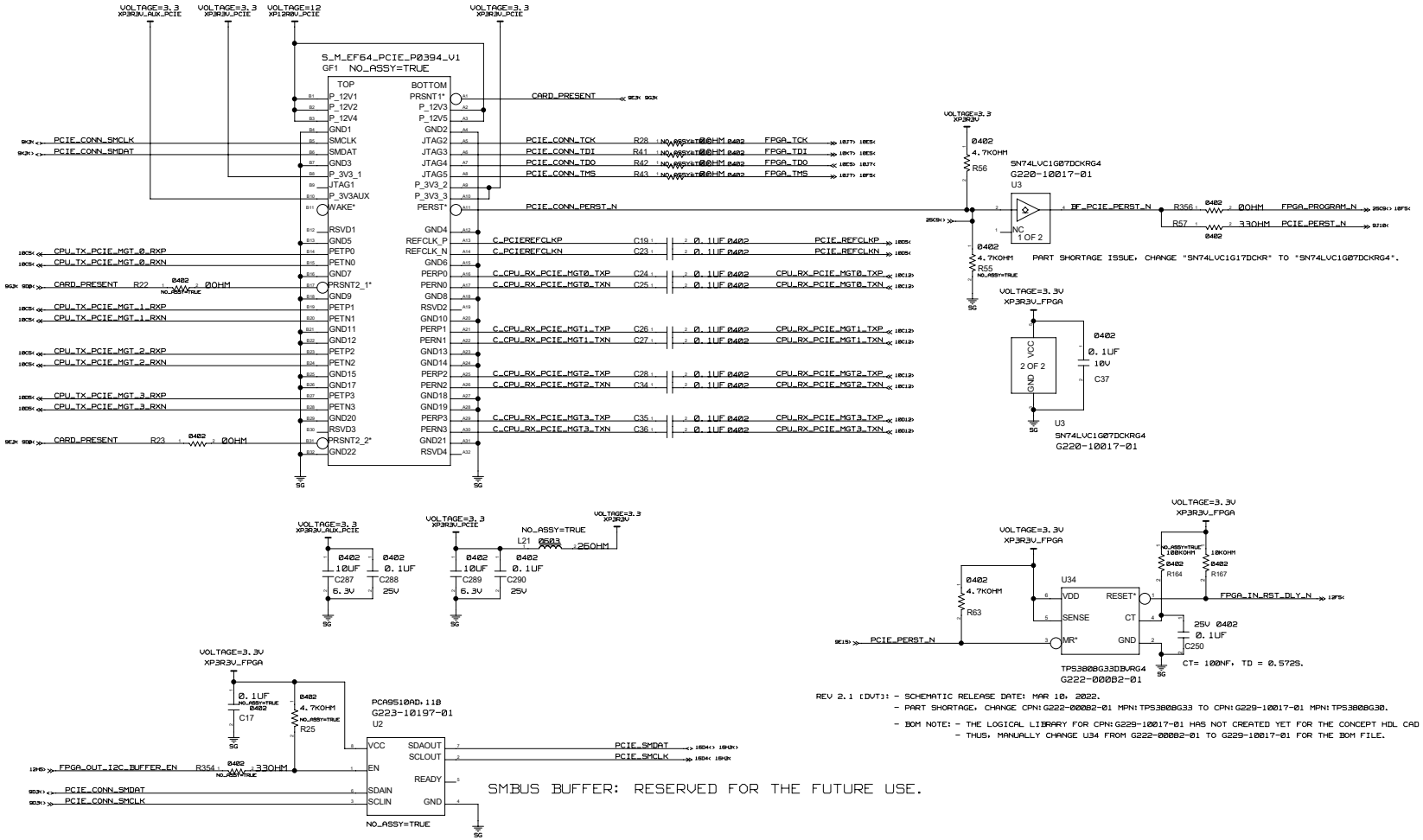
# PCIE_X4_GF_CONN




REV 2.1 [DVT]: - SCHEMATIC RELEASE DATE: MAR 10, 2022.
- PART SHORTAGE, CHANGE CPN:G222-00082-01 MPN:TPS3808G33 TO CPN:G229-10017-01 MPN:TPS3808G30.
- BOM NOTE: - THE LOGICAL LIBRARY FOR CPN:G229-10017-01 HAS NOT CREATED YET FOR THE CONCEPT HDL CAD
- THUS, MANUALLY CHANGE U34 FROM G222-00082-01 TO G229-10017-01 FOR THE BOM FILE.

PCIEx4_GF_CONN

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 [MP] |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
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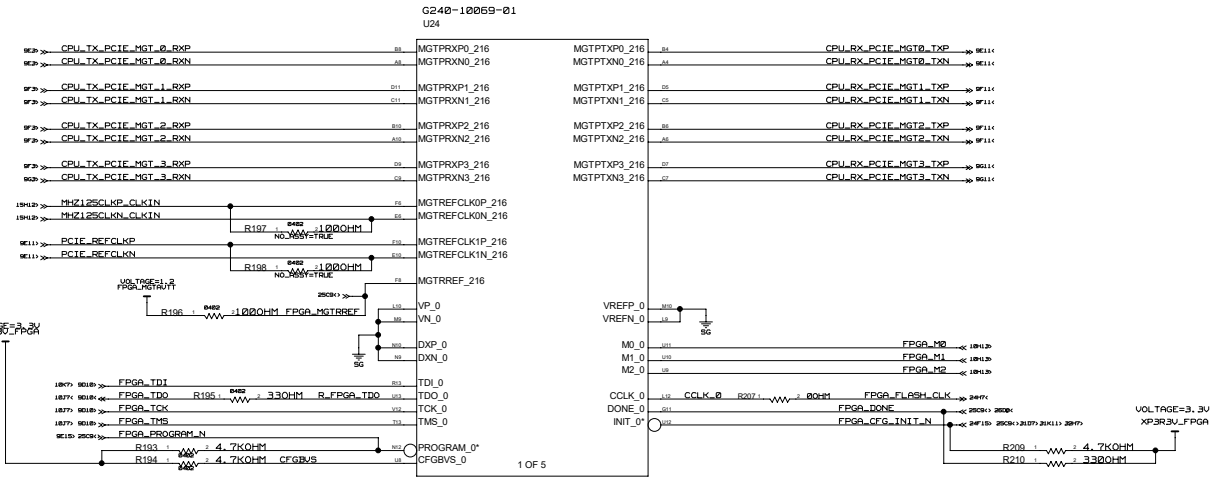
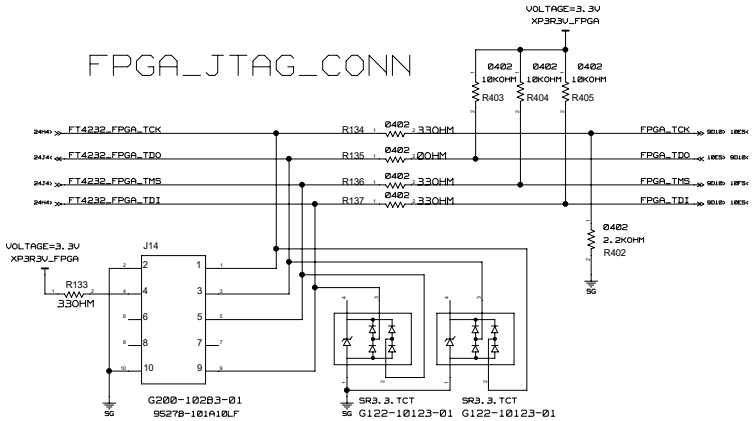
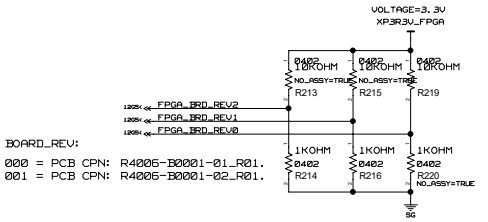
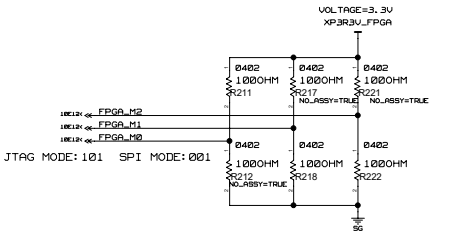
# FPGA 1/5



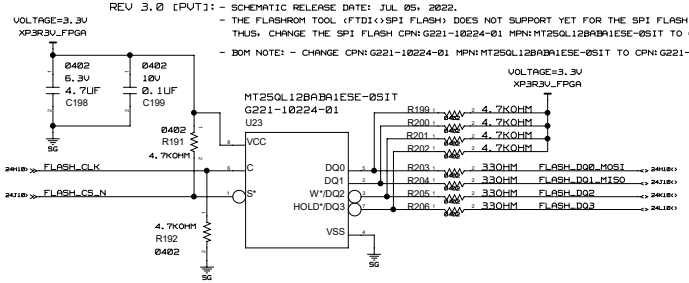

# FPGA_JTAG_CONN




REV 3.0 [PVT]: - SCHEMATIC RELEASE DATE: JUL 05, 2022.
- THE FLASHROM TOOL (FTDI<>SPI FLASH) DOES NOT SUPPORT YET FOR THE SPI FLASH CPN: G221-10224-01 MPN: MT25QL128ABA1ESE-0SIT. THUS, CHANGE THE SPI FLASH CPN: G221-10224-01 MPN: MT25QL128ABA1ESE-0SIT TO CPN: G221-10359-01 MPN: MX25L25645GM2I-08G.
- BOM NOTE: - CHANGE CPN: G221-10224-01 MPN: MT25QL128ABA1ESE-0SIT TO CPN: G221-10359-01 MPN: MX25L25645GM2I-08G.




FPGA_1/5

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 [MP] |
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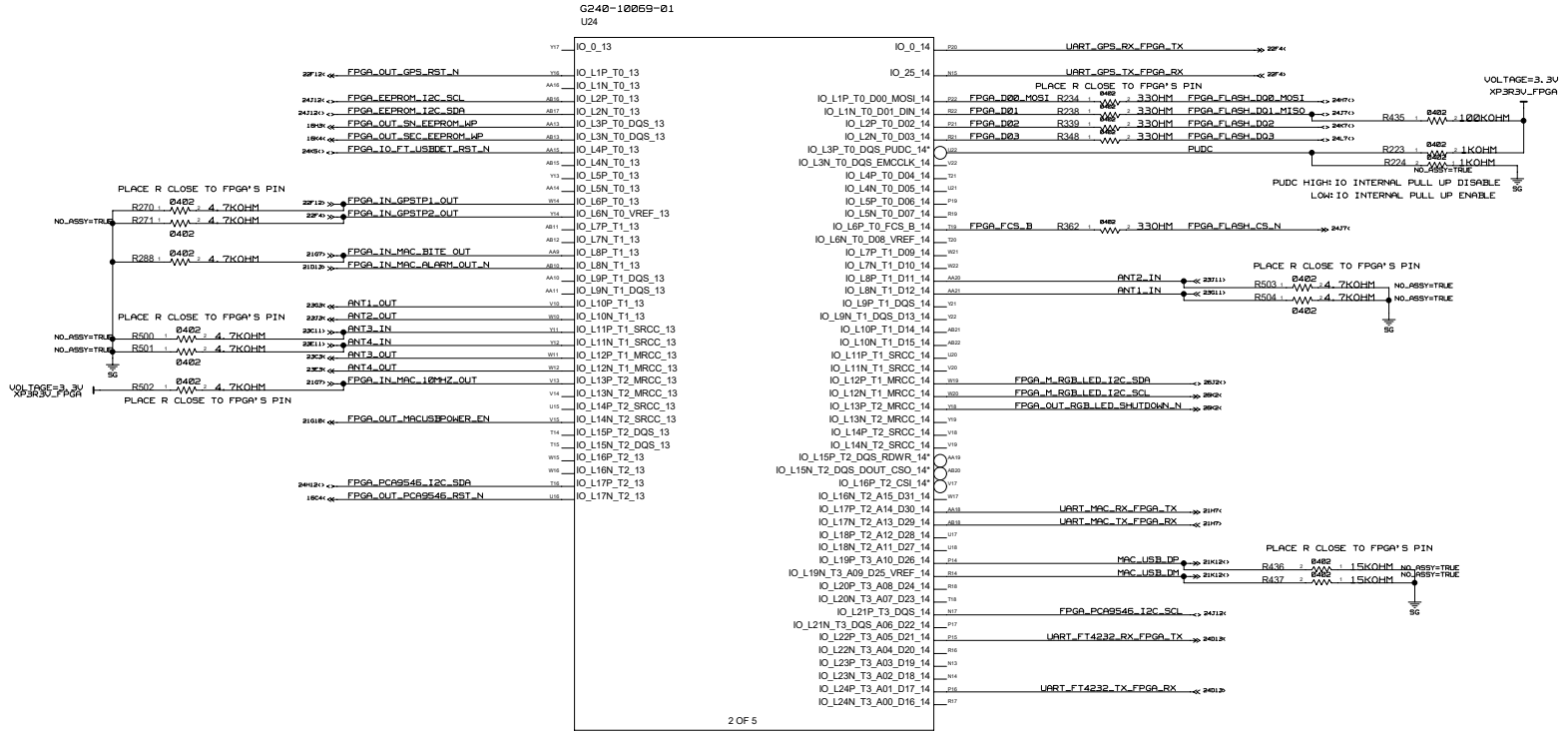
# FPGA 2/5




FPGA_2/5

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
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# FPGA 3/5

G240-10069-01
U24

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | J16 | IO_0_15 | IO_0_16 | F15 | | |
| | | M17 | IO_25_15 | IO_25_16 | F21 | | |
| 24J5< | FPGA_OUT_MUX1_SEL | H13 | IO_L1P_T0_AD0P_15 | IO_L1P_T0_16 | F13 | FPGA_OUT_SMA1_LED_BLUE_N | >26D12 |
| 24J5< | FPGA_OUT_MUX2_SEL | G13 | IO_L1N_T0_AD0N_15 | IO_L1N_T0_16 | F14 | FPGA_OUT_SMA1_LED_GREEN_N | >26C12 |
| 24J12< | FPGA_OUT_MUX3_SEL | G15 | IO_L2P_T0_AD8P_15 | IO_L2P_T0_16 | F16 | FPGA_OUT_SMA1_LED_RED_N | >26D12 |
| | | G16 | IO_L2N_T0_AD8N_15 | IO_L2N_T0_16 | E17 | | |
| 23K3< 25E6< | SMA4_SIG_IN_BF_EN_N | J14 | IO_L3P_T0_DQS_AD1P_15 | IO_L3P_T0_DQS_16 | C14 | FPGA_OUT_SMA2_LED_BLUE_N | >26F12 |
| 23K3< 25F6< | SMA4_SIG_OUT_BF_EN_N | H14 | IO_L3N_T0_DQS_AD1N_15 | IO_L3N_T0_DQS_16 | C15 | FPGA_OUT_SMA2_LED_GREEN_N | >26E12 |
| | | G17 | IO_L4P_T0_15 | IO_L4P_T0_16 | E13 | FPGA_OUT_SMA2_LED_RED_N | >26E12 |
| | | G18 | IO_L4N_T0_15 | IO_L4N_T0_16 | E14 | | |
| 23C3< 25D5< | SMA3_SIG_OUT_BF_EN_N | J15 | IO_L5P_T0_AD9P_15 | IO_L5P_T0_16 | E16 | | |
| 23C3< 25C5< | SMA3_SIG_IN_BF_EN_N | H15 | IO_L5N_T0_AD9N_15 | IO_L5N_T0_16 | C16 | | |
| | | H17 | IO_L6P_T0_15 | IO_L6P_T0_16 | D14 | LED_DATOUT2 | >26C3 |
| | | H18 | IO_L6N_T0_VREF_15 | IO_L6N_T0_VREF_16 | D15 | LED_DATOUT3 | >26B3 |
| 25J12>25H5<> | FPGA_IO_0 | J22 | IO_L7P_T1_AD2P_15 | IO_L7P_T1_16 | B15 | | |
| 25J5<> 25J12<> | FPGA_IO_1 | H22 | IO_L7N_T1_AD2N_15 | IO_L7N_T1_16 | B16 | | |
| 25J5<> 25J12<> | FPGA_IO_2 | H20 | IO_L8P_T1_AD10P_15 | IO_L8P_T1_16 | C13 | LED_DATOUT1 | >26C3 |
| 25J5<> 25J12<> | FPGA_IO_3 | G20 | IO_L8N_T1_AD10N_15 | IO_L8N_T1_16 | B13 | LED_DATOUT0 | >26C3 |
| 25J7<> 25J5<> | FPGA_IO_4 | K21 | IO_L9P_T1_DQS_AD3P_15 | IO_L9P_T1_DQS_16 | A15 | | |
| 25K5<> 25J7<> | FPGA_IO_5 | K22 | IO_L9N_T1_DQS_AD3N_15 | IO_L9N_T1_DQS_16 | A16 | | |
| 25K5<> 25J7<> | FPGA_IO_6 | M21 | IO_L10P_T1_AD11P_15 | IO_L10P_T1_16 | A13 | FPGA_USR_LED1 | >26D3 |
| 25K5<> 25J7<> | FPGA_IO_7 | L21 | IO_L10N_T1_AD11N_15 | IO_L10N_T1_16 | A14 | FPGA_USR_LED0 | >26D3 |
| 9H15> | FPGA_IN_RST_DLY_N | J20 | IO_L11P_T1_SRCC_15 | IO_L11P_T1_SRCC_16 | B17 | | |
| | | J21 | IO_L11N_T1_SRCC_15 | IO_L11N_T1_SRCC_16 | B18 | | |
| 18G15> | FPGA_IN_SHT3X_ALERT_N | J19 | IO_L12P_T1_MRCC_15 | IO_L12P_T1_MRCC_16 | D17 | FPGA_OUT_SMA3_LED_BLUE_N | >26G12 |
| 18G12< | FPGA_OUT_SHT3X_RST_N | H19 | IO_L12N_T1_MRCC_15 | IO_L12N_T1_MRCC_16 | C17 | FPGA_OUT_SMA3_LED_GREEN_N | >26G12 |
| | | K19 | IO_L13P_T2_MRCC_15 | IO_L13P_T2_MRCC_16 | C18 | FPGA_OUT_SMA3_LED_RED_N | >26G12 |
| | | K19 | IO_L13N_T2_MRCC_15 | IO_L13N_T2_MRCC_16 | C19 | | |
| | | L19 | IO_L14P_T2_SRCC_15 | IO_L14P_T2_SRCC_16 | E19 | FPGA_OUT_SMA4_LED_BLUE_N | >26J12 |
| | | L20 | IO_L14N_T2_SRCC_15 | IO_L14N_T2_SRCC_16 | D19 | FPGA_OUT_SMA4_LED_GREEN_N | >26H12 |
| 25D6< 17D12> | FPGA_IN_LM75B_INT1_N | N22 | IO_L15P_T2_DQS_15 | IO_L15P_T2_DQS_16 | F18 | FPGA_OUT_SMA4_LED_RED_N | >26H12 |
| 25D6< 17G12> | FPGA_IN_LM75B_INT2_N | M22 | IO_L15N_T2_DQS_ADV_B_15 | IO_L15N_T2_DQS_16 | E18 | | |
| 25D6< 17K12> | FPGA_IN_LM75B_INT3_N | M19 | IO_L16P_T2_A28_15 | IO_L16P_T2_16 | B20 | FPGA_OUT_GPS_LED_BLUE_N | >26K12 |
| | | L19 | IO_L16N_T2_A27_15 | IO_L16N_T2_16 | A20 | FPGA_OUT_GPS_LED_GREEN_N | >26K12 |
| 18H18> | FPGA_BRD_REV2 | N18 | IO_L17P_T2_A26_15 | IO_L17P_T2_16 | A18 | FPGA_OUT_GPS_LED_RED_N | >26K12 |
| 18H18> | FPGA_BRD_REV1 | N19 | IO_L17N_T2_A25_15 | IO_L17N_T2_16 | A19 | | |
| 18H18> | FPGA_BRD_REV0 | N20 | IO_L18P_T2_A24_15 | IO_L18P_T2_16 | F19 | | |
| | | M20 | IO_L18N_T2_A23_15 | IO_L18N_T2_16 | F20 | | |
| 23G3< 25G5< | SMA1_SIG_OUT_BF_EN_N | K13 | IO_L19P_T3_A22_15 | IO_L19P_T3_16 | D20 | | |
| 23G3< 25G5< | SMA1_SIG_IN_BF_EN_N | K14 | IO_L19N_T3_A21_VREF_15 | IO_L19N_T3_VREF_16 | C20 | | |
| 23J7< 25G5< | SMA2_SIG_OUT_BF_EN_N | M13 | IO_L20P_T3_A20_15 | IO_L20P_T3_16 | C22 | IO_L20P_16 | <>25C3> |
| 23K3< 25G5< | SMA2_SIG_IN_BF_EN_N | L13 | IO_L20N_T3_A19_15 | IO_L20N_T3_16 | B22 | IO_L20N_16 | <>25C3> |
| | | K17 | IO_L21P_T3_DQS_15 | IO_L21P_T3_DQS_16 | B21 | IO_L21P_16 | <>25C3> |
| 28F15< | FPGA_OUT_BN0088_RST_N | J17 | IO_L21N_T3_DQS_A18_15 | IO_L21N_T3_DQS_16 | A21 | IO_L21N_16 | <>25C3> |
| 28F2> | FPGA_IN_BN0088_INT_N | L14 | IO_L22P_T3_A17_15 | IO_L22P_T3_16 | E22 | IO_L22P_16 | <>25C3> |
| 28F2< | FPGA_OUT_BN0088_BOOT_N | L15 | IO_L22N_T3_A16_15 | IO_L22N_T3_16 | D22 | IO_L22N_16 | <>25C3> |
| | | L16 | IO_L23P_T3_FOE_B_15 | IO_L23P_T3_16 | E21 | IO_L23P_16 | <>25C3> |
| 9K2< | FPGA_OUT_I2C_BUFFER_EN | K16 | IO_L23N_T3_FWE_B_15 | IO_L23N_T3_16 | D21 | IO_L23N_16 | <>25C3> |
| 21H14> | FPGA_IN_MAC_USB_OC_N | M16 | IO_L24P_T3_RS1_15 | IO_L24P_T3_16 | G21 | IO_L24P_16 | <>25D3> |
| 21L5< | RSVD_DBG_USB_MUX_SEL | M16 | IO_L24N_T3_RS0_15 | IO_L24N_T3_16 | G22 | IO_L24N_16 | <>25D3> |

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FPGA_3/5

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: BHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 12 of 35 | CELESTICA |

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USE PURSUANT TO COMPANY INSTRUCTIONS

# FPGA 4/5

## VCCIO = 2.5V.

G240-10069-01
U24

| | | | |
|---|---|---|---|
| F4 | IO_0_35 | IO_0_34 | T3 |
| L6 | IO_25_35 | IO_25_34 | U7 |
| B1 | IO_L1P_T0_AD4P_35 | IO_L1P_T0_34 | T1 |
| A1 | IO_L1N_T0_AD4N_35 | IO_L1N_T0_34 | U1 |
| C2 | IO_L2P_T0_AD12P_35 | IO_L2P_T0_34 | U2 |
| B2 | IO_L2N_T0_AD12N_35 | IO_L2N_T0_34 | V2 |
| E1 | IO_L3P_T0_DQS_AD5P_35 | IO_L3P_T0_DQS_34 | R3 |
| D1 | IO_L3N_T0_DQS_AD5N_35 | IO_L3N_T0_DQS_34 | R2 |
| E2 | IO_L4P_T0_35 | IO_L4P_T0_34 | W2 |
| D2 | IO_L4N_T0_35 | IO_L4N_T0_34 | V2 |
| G1 | IO_L5P_T0_AD13P_35 | IO_L5P_T0_34 | W1 |
| F1 | IO_L5N_T0_AD13N_35 | IO_L5N_T0_34 | V1 |
| F3 | IO_L6P_T0_35 | IO_L6P_T0_34 | U3 |
| E3 | IO_L6N_T0_VREF_35 | IO_L6N_T0_VREF_34 | V3 |
| K1 | IO_L7P_T1_AD6P_35 | IO_L7P_T1_34 | AA1 |
| J1 | IO_L7N_T1_AD6N_35 | IO_L7N_T1_34 | AB1 |
| H2 | IO_L8P_T1_AD14P_35 | IO_L8P_T1_34 | AB3 |
| G2 | IO_L8N_T1_AD14N_35 | IO_L8N_T1_34 | AB2 |
| K2 | IO_L9P_T1_DQS_AD7P_35 | IO_L9P_T1_DQS_34 | Y3 |
| J2 | IO_L9N_T1_DQS_AD7N_35 | IO_L9N_T1_DQS_34 | AA3 |
| J5 | IO_L10P_T1_AD15P_35 | IO_L10P_T1_34 | AA5 |
| H5 | IO_L10N_T1_AD15N_35 | IO_L10N_T1_34 | AB5 |
| H3 | IO_L11P_T1_SRCC_35 | IO_L11P_T1_SRCC_34 | Y4 |
| G3 | IO_L11N_T1_SRCC_35 | IO_L11N_T1_SRCC_34 | AA4 |
| H4 | IO_L12P_T1_MRCC_35 | IO_L12P_T1_MRCC_34 | Y4 |
| G4 | IO_L12N_T1_MRCC_35 | IO_L12N_T1_MRCC_34 | W4 |
| K4 | IO_L13P_T2_MRCC_35 | IO_L13P_T2_MRCC_34 | R4 |
| J4 | IO_L13N_T2_MRCC_35 | IO_L13N_T2_MRCC_34 | T4 |
| L3 | IO_L14P_T2_SRCC_35 | IO_L14P_T2_SRCC_34 | T5 |
| K3 | IO_L14N_T2_SRCC_35 | IO_L14N_T2_SRCC_34 | U5 |
| M1 | IO_L15P_T2_DQS_35 | IO_L15P_T2_DQS_34 | W6 |
| L1 | IO_L15N_T2_DQS_35 | IO_L15N_T2_DQS_34 | W5 |
| M3 | IO_L16P_T2_35 | IO_L16P_T2_34 | U6 |
| M2 | IO_L16N_T2_35 | IO_L16N_T2_34 | V5 |
| K6 | IO_L17P_T2_35 | IO_L17P_T2_34 | R6 |
| J6 | IO_L17N_T2_35 | IO_L17N_T2_34 | T6 |
| L5 | IO_L18P_T2_35 | IO_L18P_T2_34 | Y6 |
| L4 | IO_L18N_T2_35 | IO_L18N_T2_34 | AA6 |
| N4 | IO_L19P_T3_35 | IO_L19P_T3_34 | V7 |
| N3 | IO_L19N_T3_VREF_35 | IO_L19N_T3_VREF_34 | W7 |
| P1 | IO_L20P_T3_35 | IO_L20P_T3_34 | AB7 |
| P1 | IO_L20N_T3_35 | IO_L20N_T3_34 | AB6 |
| P5 | IO_L21P_T3_DQS_35 | IO_L21P_T3_DQS_34 | V9 |
| P4 | IO_L21N_T3_DQS_35 | IO_L21N_T3_DQS_34 | V8 |
| P2 | IO_L22P_T3_35 | IO_L22P_T3_34 | AA8 |
| N2 | IO_L22N_T3_35 | IO_L22N_T3_34 | AB8 |
| M6 | IO_L23P_T3_35 | IO_L23P_T3_34 | Y8 |
| M5 | IO_L23N_T3_35 | IO_L23N_T3_34 | Y7 |
| P6 | IO_L24P_T3_35 | IO_L24P_T3_34 | W9 |
| N5 | IO_L24N_T3_35 | IO_L24N_T3_34 | Y9 |

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| | | | |
|---|---|---|---|
| 25P2(1) | IO_L20P_35 | IO_L20P_34 | 25S2(1) |
| 25P2(1) | IO_L20N_35 | IO_L20N_34 | 25S2(1) |
| 25P2(1) | IO_L21P_35 | IO_L21P_34 | 25S2(1) |
| 25P2(1) | IO_L21N_35 | IO_L21N_34 | 25S2(1) |
| 25P2(1) | IO_L22P_35 | IO_L22P_34 | 25S2(1) |
| 25P2(1) | IO_L22N_35 | IO_L22N_34 | 25S2(1) |
| 25P2(1) | IO_L23P_35 | IO_L23P_34 | 25S2(1) |
| 25P2(1) | IO_L23N_35 | IO_L23N_34 | 25S2(1) |
| 25P2(1) | IO_L24P_35 | IO_L24P_34 | 25S2(1) |
| 25P2(1) | IO_L24N_35 | IO_L24N_34 | 25S2(1) |

RSVD EXTERNAL R TERM. PLACE R CLOSE TO FPGA'S PIN

NO_ASSY=TRUE
R275 0402 100OHM
FPGA_IN_MAC_PPS_OUTP
FPGA_IN_MAC_PPS_OUTN
21D4
21D4
R438 0402 10KOHM
R439 0402 10KOHM
R440 0402 10KOHM
R441 0402 10KOHM
VOLTAGE=2.5V
XP2RSV_FPGA
SG

NO_ASSY=TRUE
R276 0402 100OHM
FPGA_OUT_MAC_PPS_IN0P
FPGA_OUT_MAC_PPS_IN0N
21C4
21D4
LVDS_25 OUTPUT

NO_ASSY=TRUE
R277 0402 100OHM
FPGA_OUT_MAC_PPS_IN1P
FPGA_OUT_MAC_PPS_IN1N
21C4
21C4
LVDS_25 OUTPUT

R278 0402 100OHM
MHZ200CLKP_CLKIN
MHZ200CLKN_CLKIN
15D12
15D12
R355 0402 10KOHM
R358 0402 10KOHM
R359 0402 10KOHM
R360 0402 10KOHM
VOLTAGE=2.5V
XP2RSV_FPGA
SG

FPGA_4/5

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
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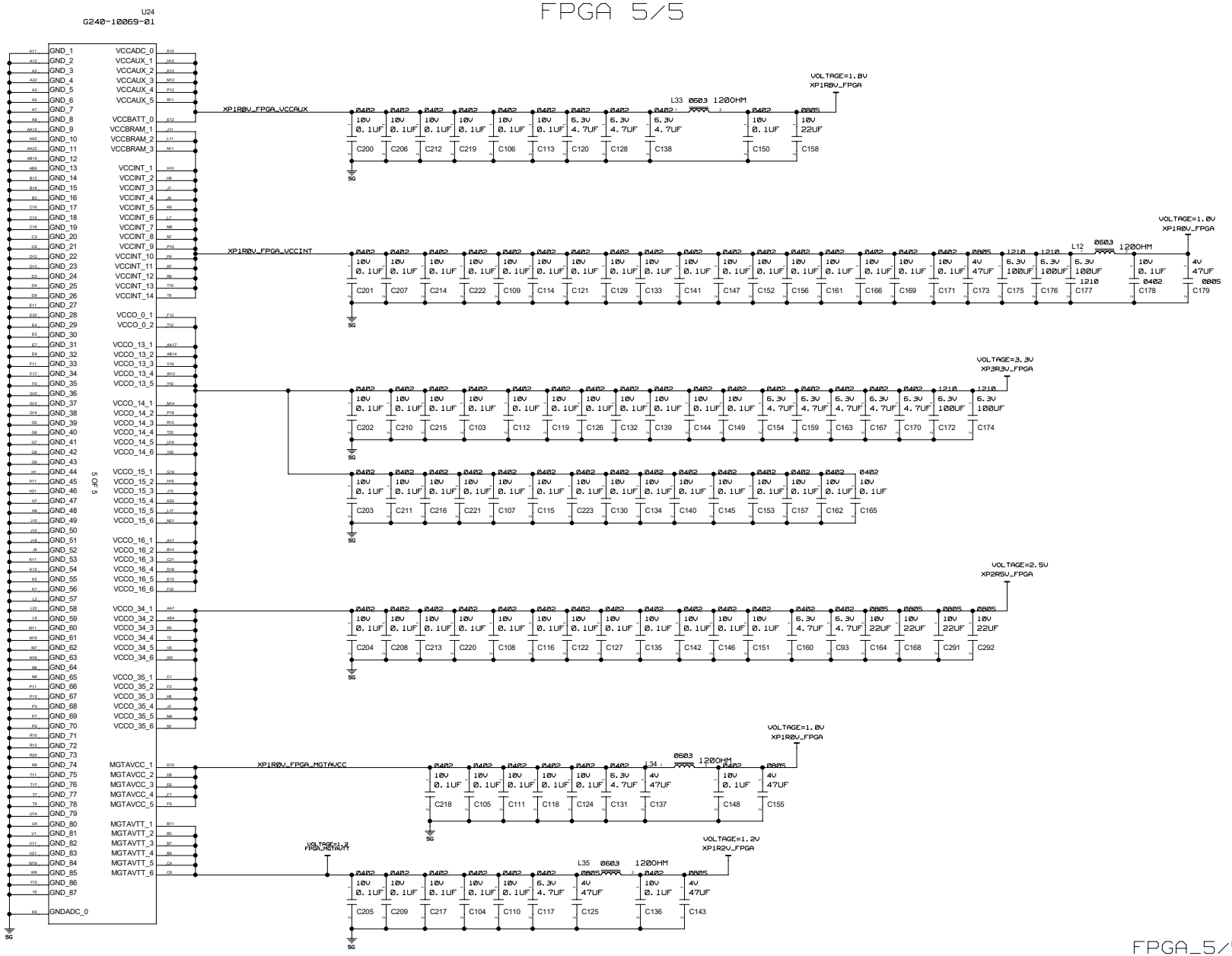
# FPGA 5/5




FPGA_5/5

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: BHUMARIN I., ZUFIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 [MP] |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
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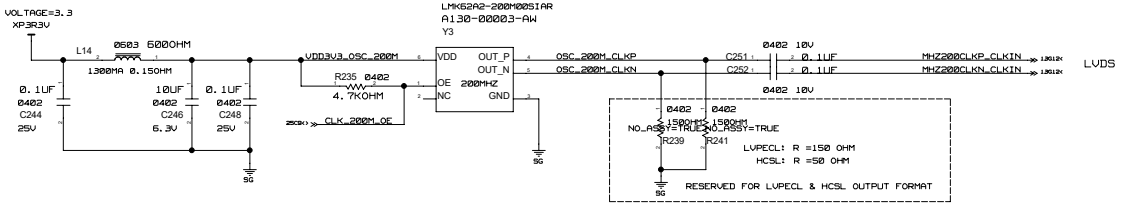
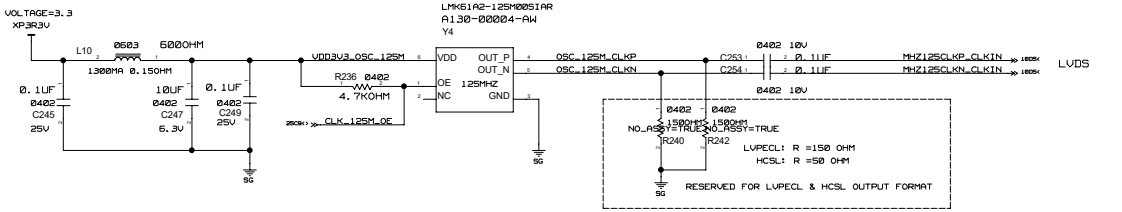
# CLOCK_GENERATOR

## CLOCK GENERATOR: 200MHZ.




## CLOCK GENERATOR: 125MHZ.




CLOCK_GENERATOR

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
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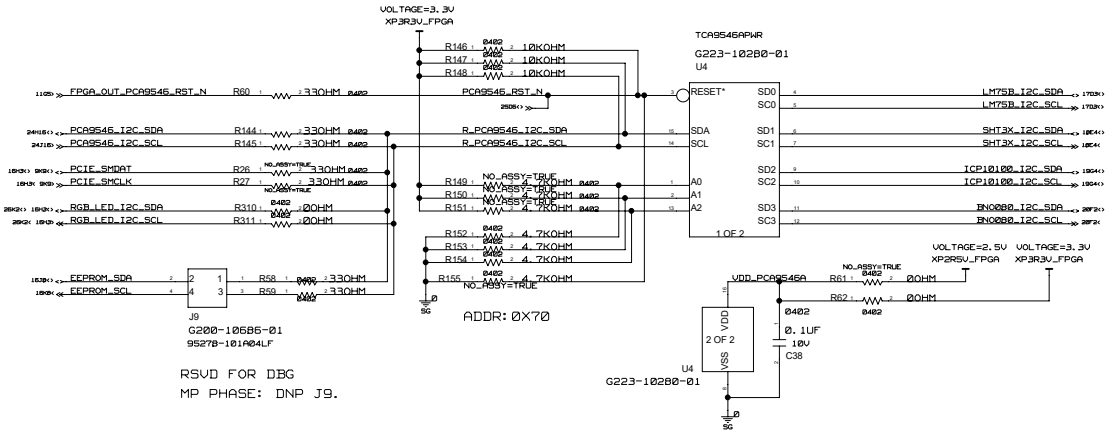
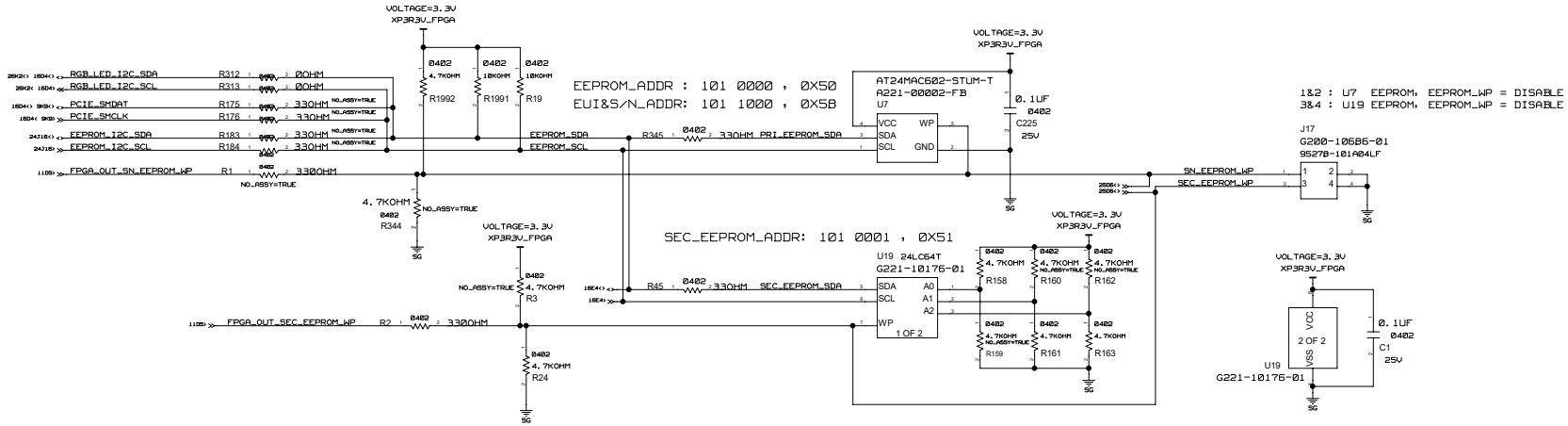
# PCA9546A_I2C_SWITCH




# EEPROM




# I2C_SWITCH&EEPROM

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: BHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
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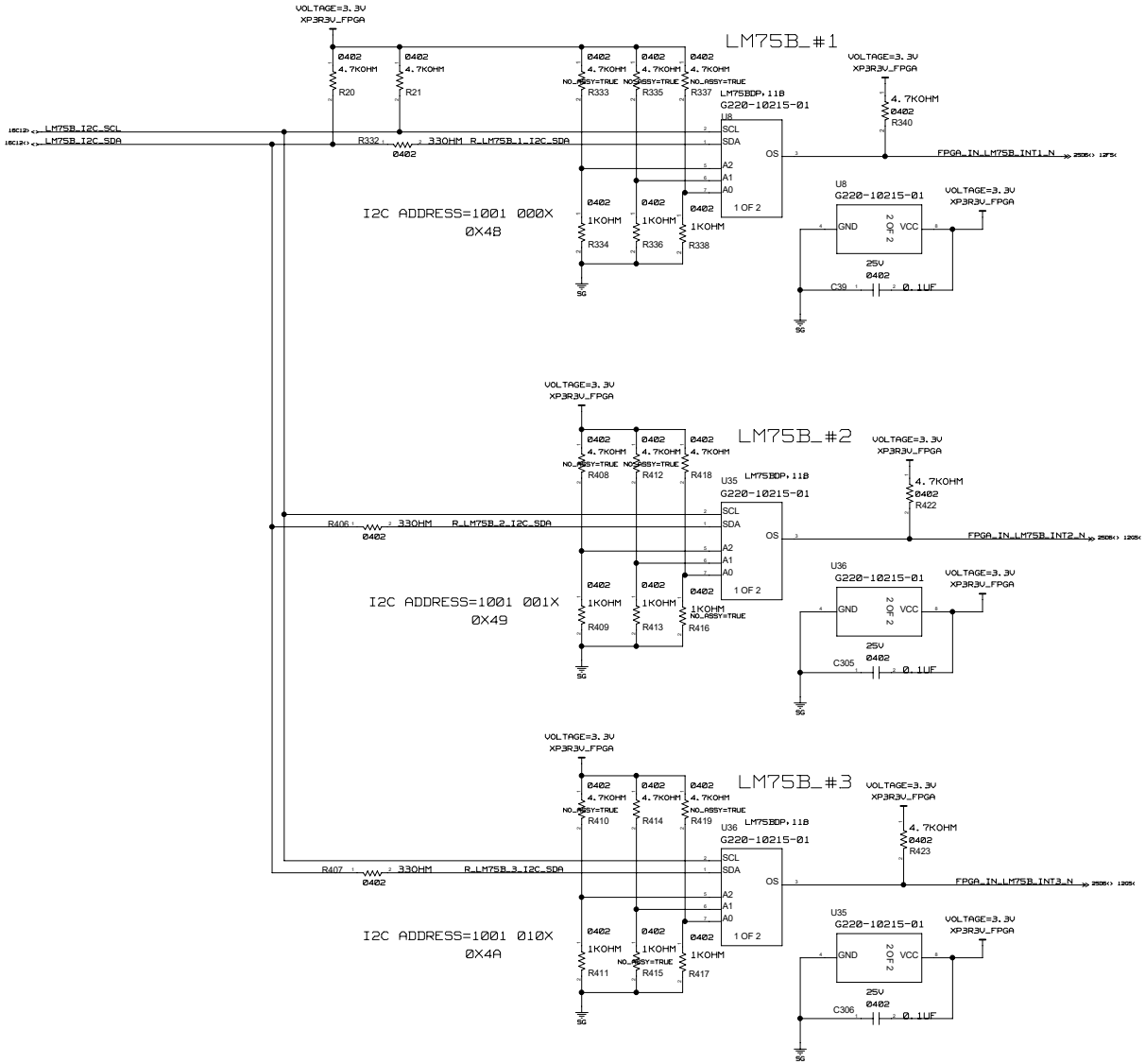
# TEMPERATURE_SENSOR




TEMPERATURE_SENSOR

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 17 of 35 | CELESTICA |

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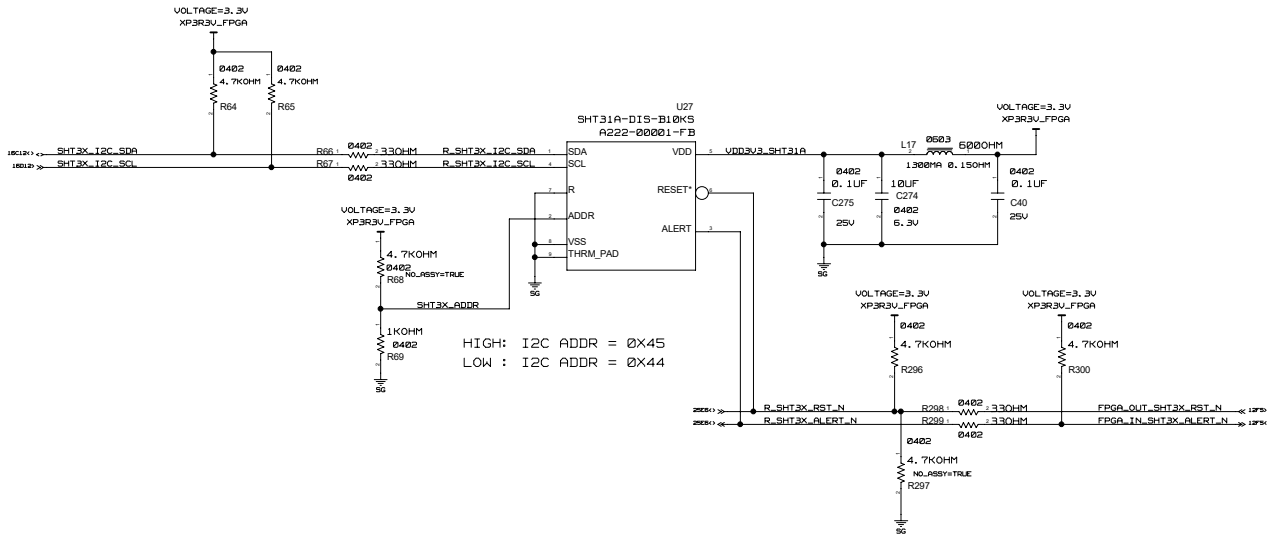
# HUMIDITY_SENSOR




HUMIDITY_SENSOR

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 1B of 35 | CELESTICA |

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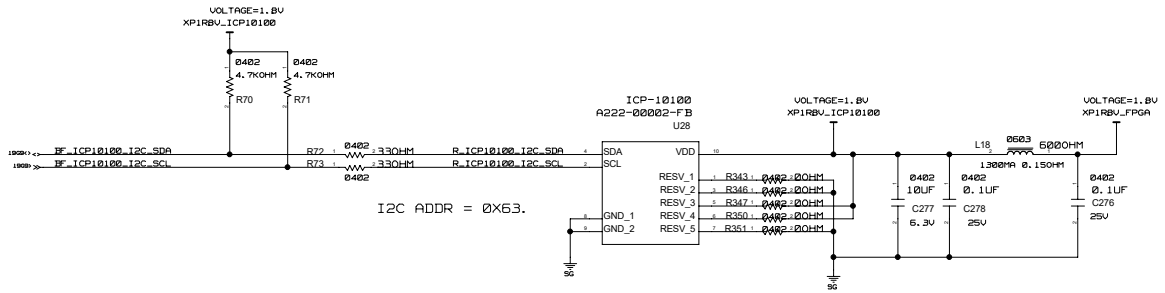
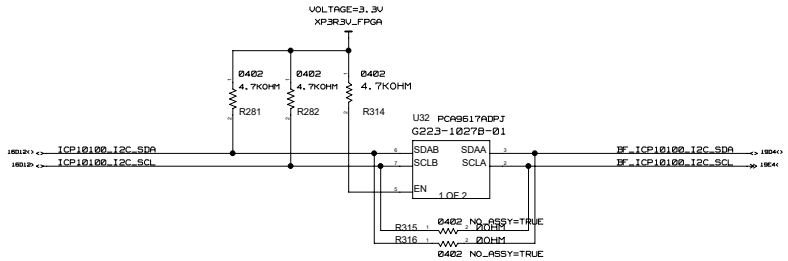
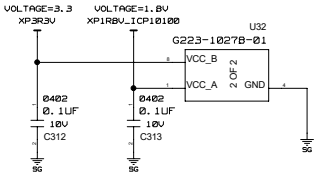
# AIR_PRESSURE_SENSOR




U32: - G220-10219-01 (EVT) SHOW NOT FOR NEW DESIGN IN THE ENOVIA SYSTEM.
- THE EVT >> DVT PHASE, CHANGE G220-10219-01 TO G223-1027B-01.

- G223-1027B-01: - P1GULS5V9617AUEX: VCC(B) AND VCC(A) CAN BE APPLIED IN ANY SEQUENCE AT POWER-UP
- PCA9617ADPJ : VCC(B) AND VCC(A) CAN BE APPLIED IN ANY SEQUENCE AT POWER-UP
- TCA9617ADGKR : DURING POWER-UP, VCCB MUST RISE BEFORE VCCA.

- THUS, TO SUPPORT TI CHIP (TCA9617ADGKR). FOR THE DVT, CONNECT VCC_B PIN TO XP3R3V.

AIR_PRESSURE_SENSOR

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: BHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
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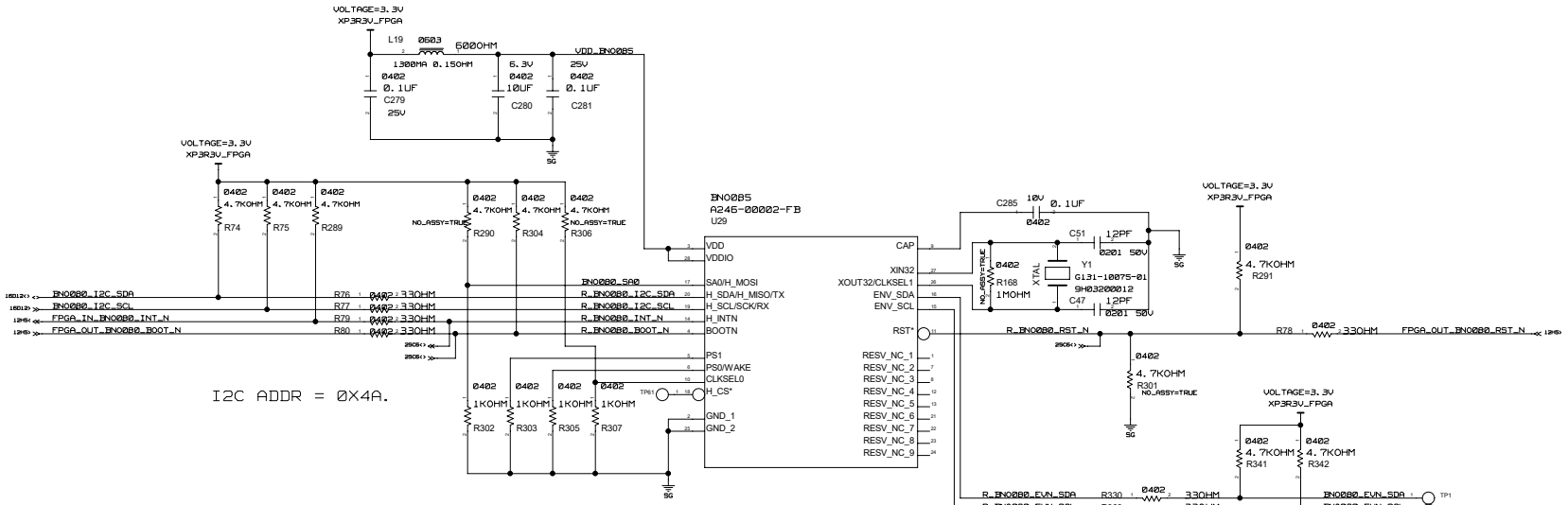
# VIBRATION_SENSOR




## VIBRATION_SENSOR

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUITAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
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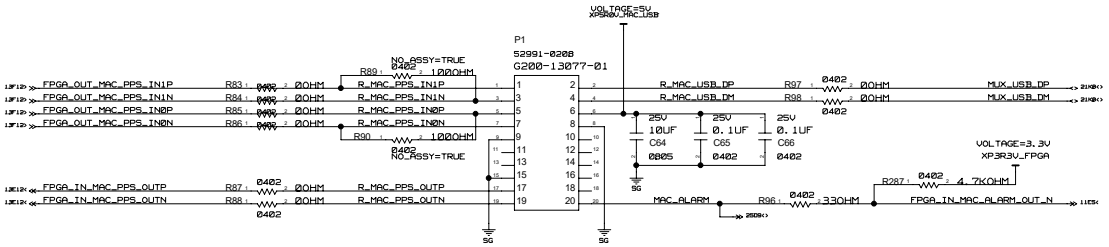
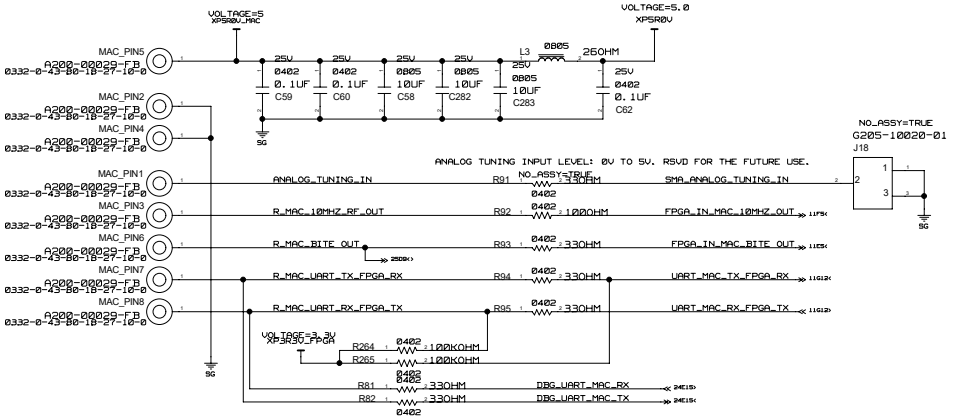
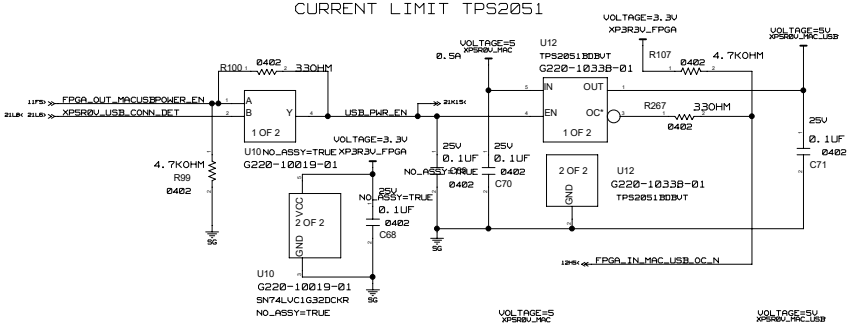
# MINIATURE_ATOMIC_CLOCK_MODULE

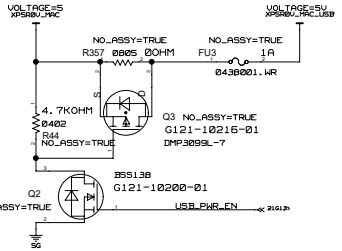



## CURRENT LIMIT TPS2051

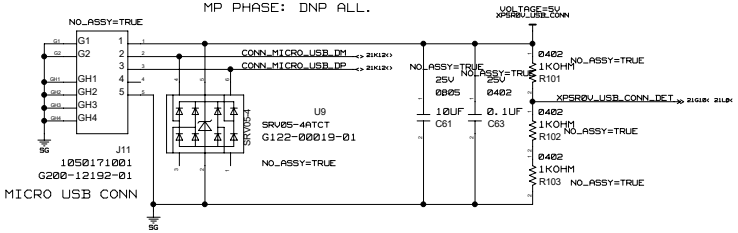


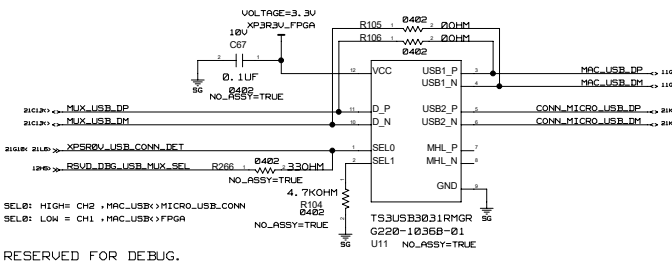

MP PHASE: DNP U10 AND POP R100.




## RESERVED FOR DEBUG

MP PHASE: DNP ALL.




RESERVED FOR DEBUG.

MP PHASE: DNP ALL AND POP ONLY R105,R106.

## MAC_MODULE_CONN

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
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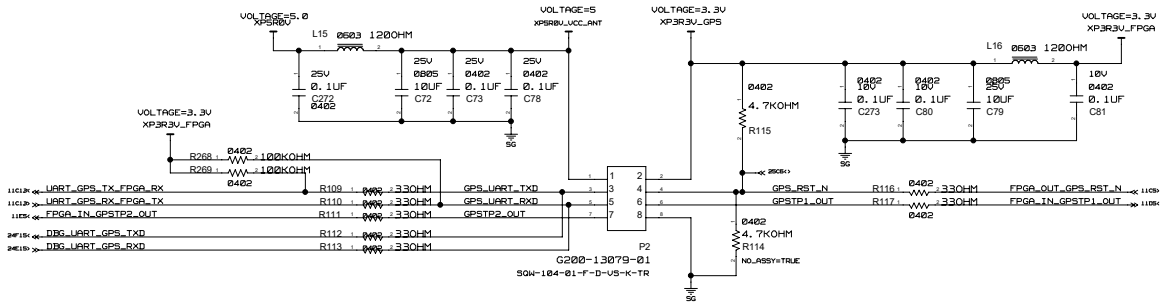
# GPS_MODULE_CONN




GPS_MODULE_CONN

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
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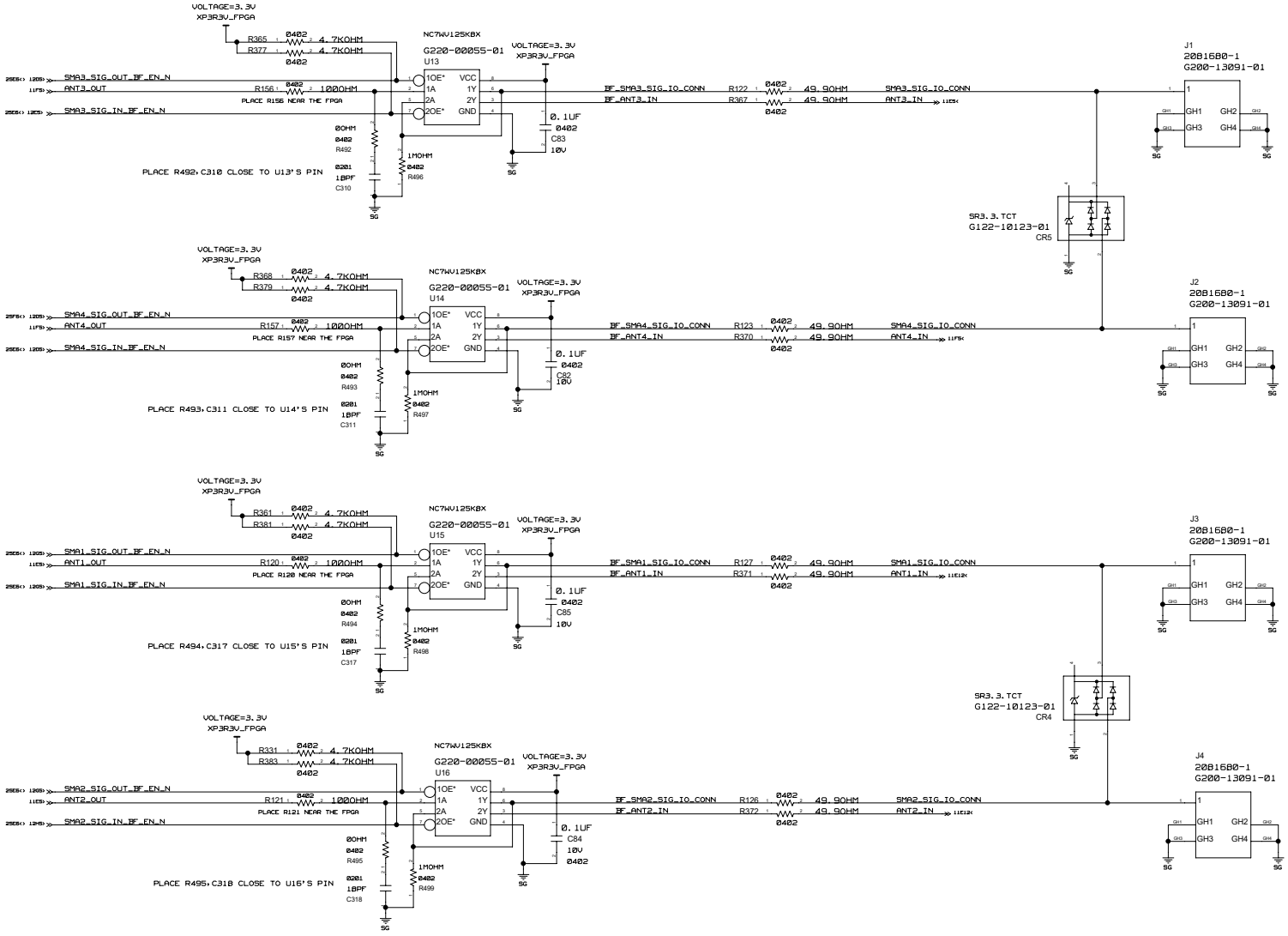
# SMA_CONN




SMA_CONN

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
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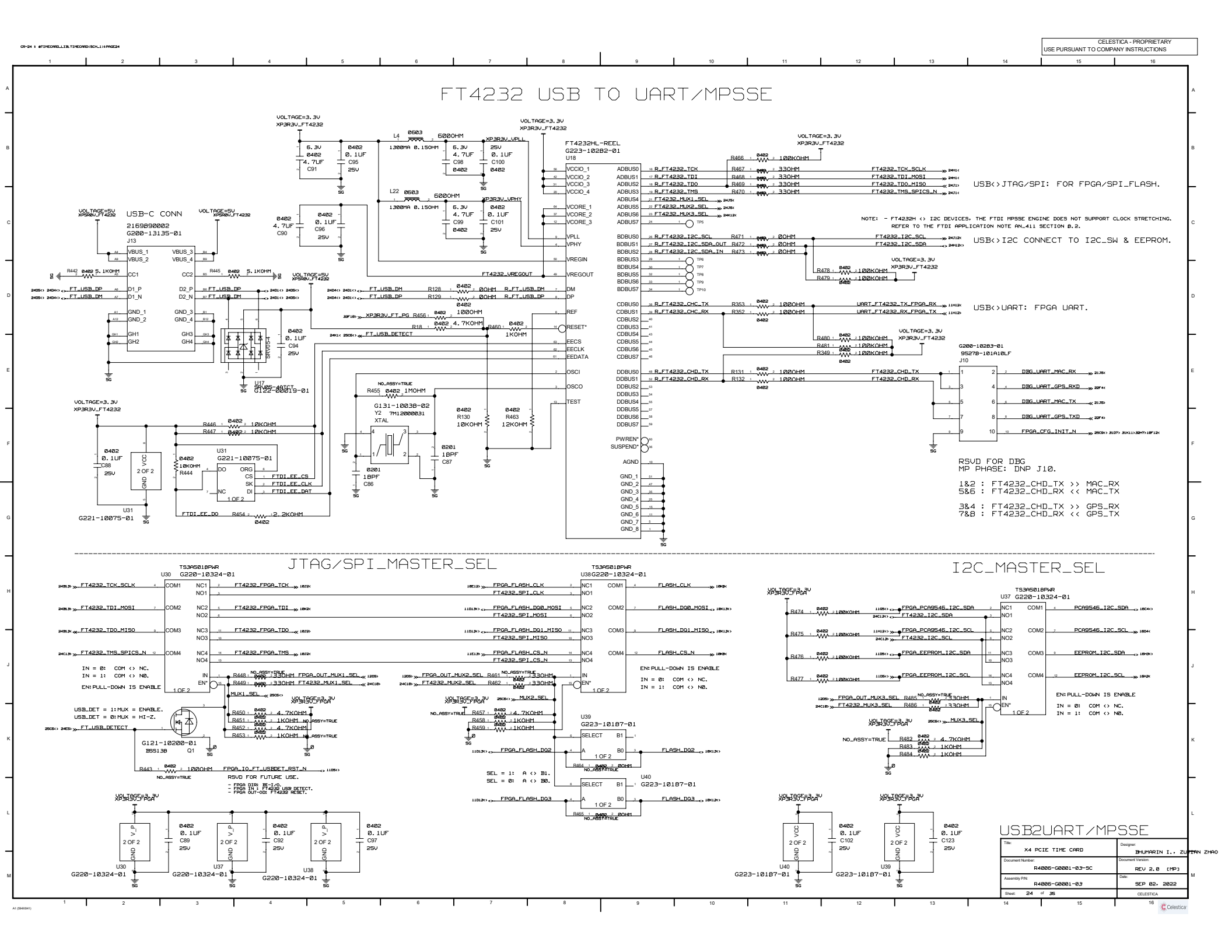
# FT4232 USB TO UART/MPSSE




## USB2UART/MPSSE

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUITIN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 24 of 35 | CELESTICA |

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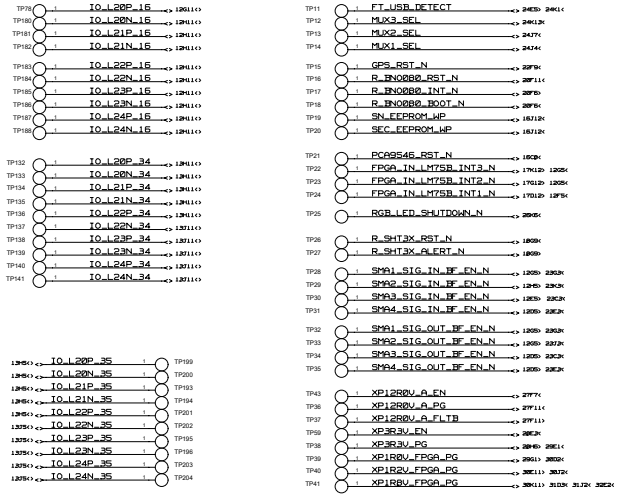
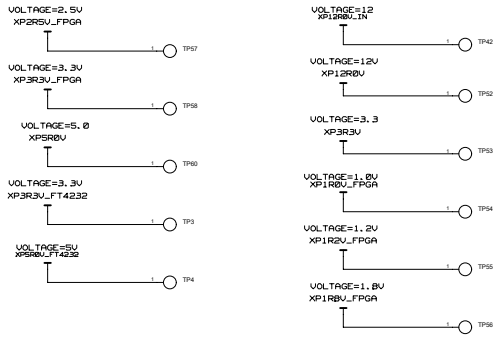
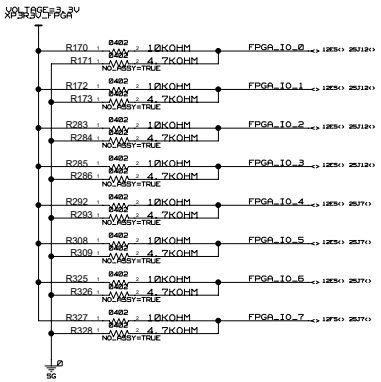
# TEST POINT



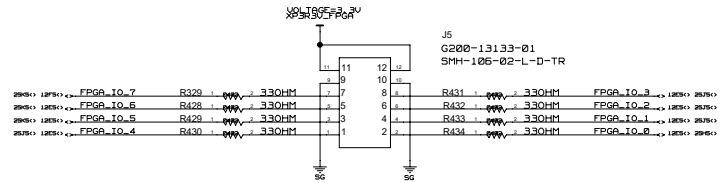




PLACE ALL TEST POINTS AT THE BOTTOM SIDE OF THE PCB

---




## PMOD CONN




## TEST_POINT&PMOD_CONN

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUITIN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 25 of 35 | CELESTICA |

A1 (5940341)

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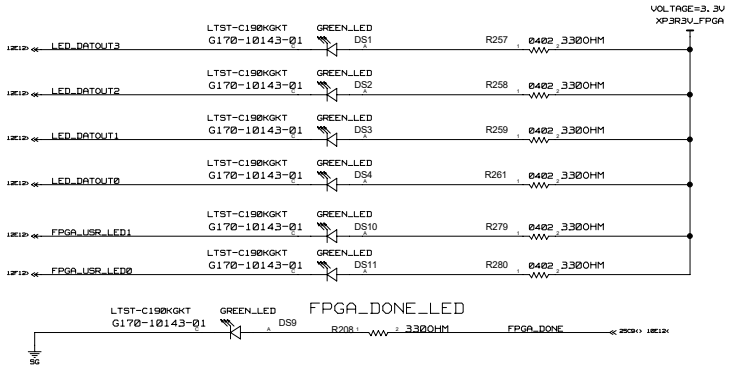
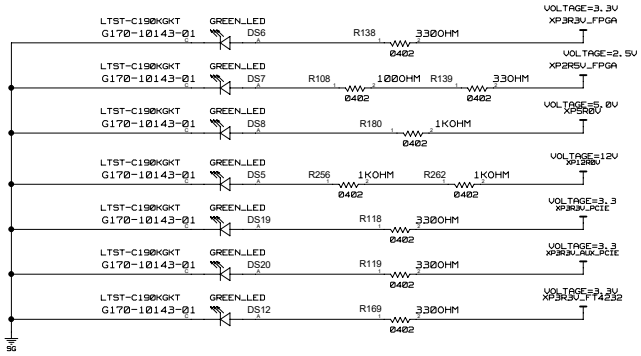
## USR_LED_STATUS



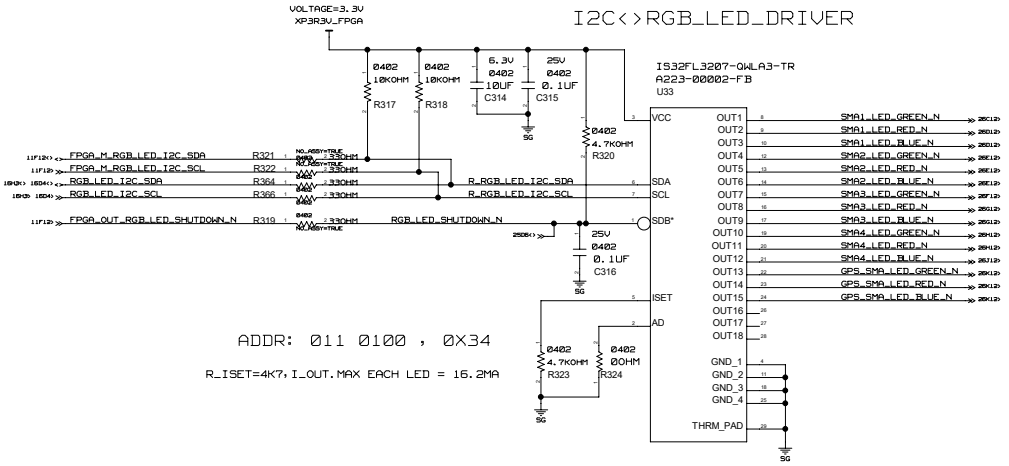

## FPGA_DONE_LED




## PWR_LED_STATUS



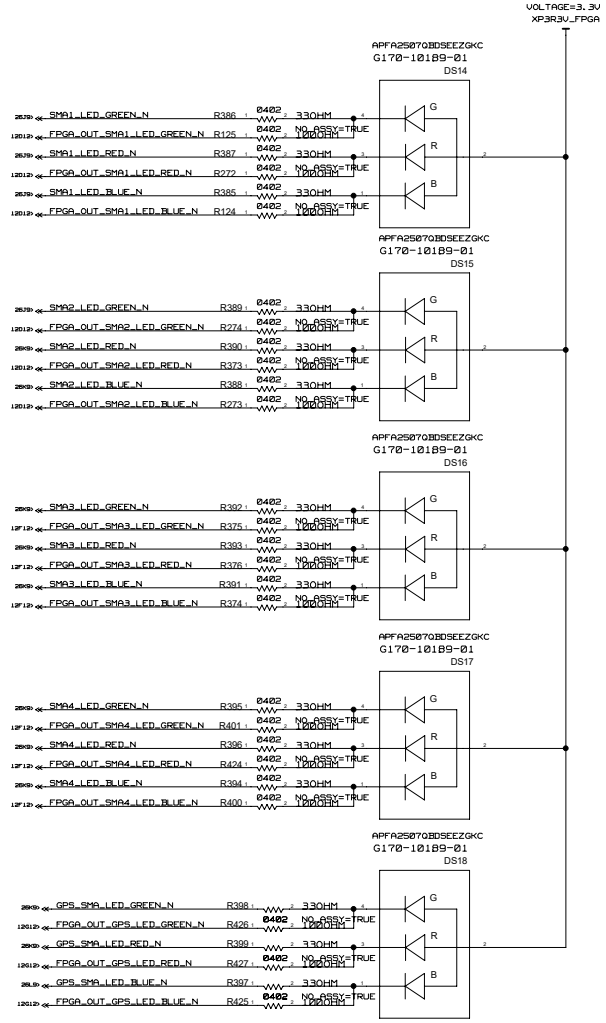

## I2C<>RGB_LED_DRIVER




ADDR: 011 0100 , 0X34

R_ISET=4K7, I_OUT.MAX EACH LED = 16.2MA

## RGB_LED_STATUS




## LED_INDICATOR

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 26 of 35 | CELESTICA |

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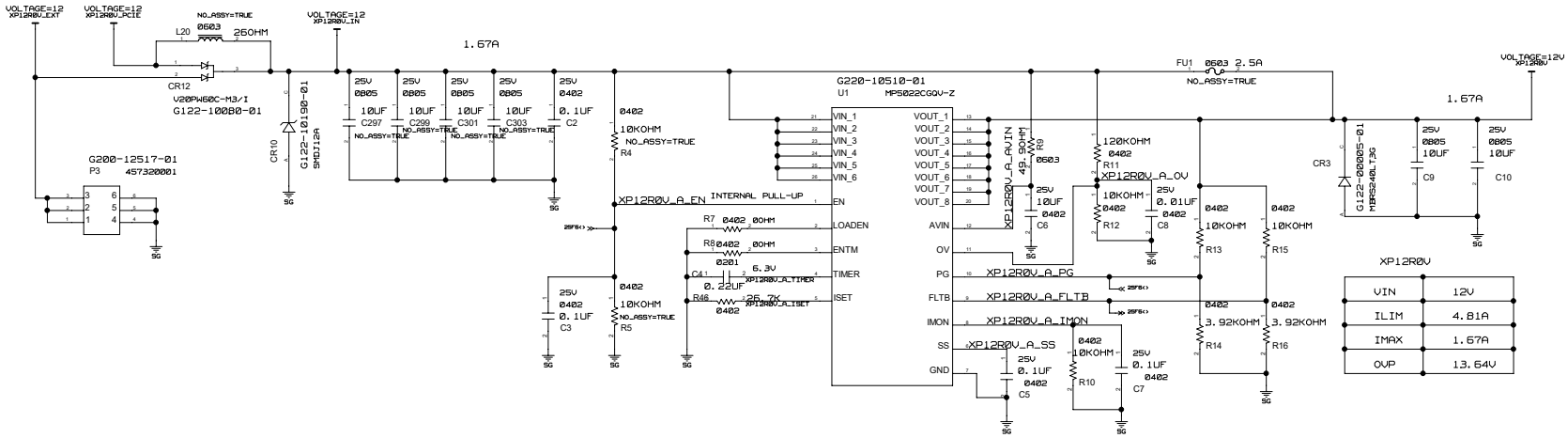
USE PURSUANT TO COMPANY INSTRUCTIONS

# XP12R0V INPUT




XP12R0V

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 27 of 35 | CELESTICA |

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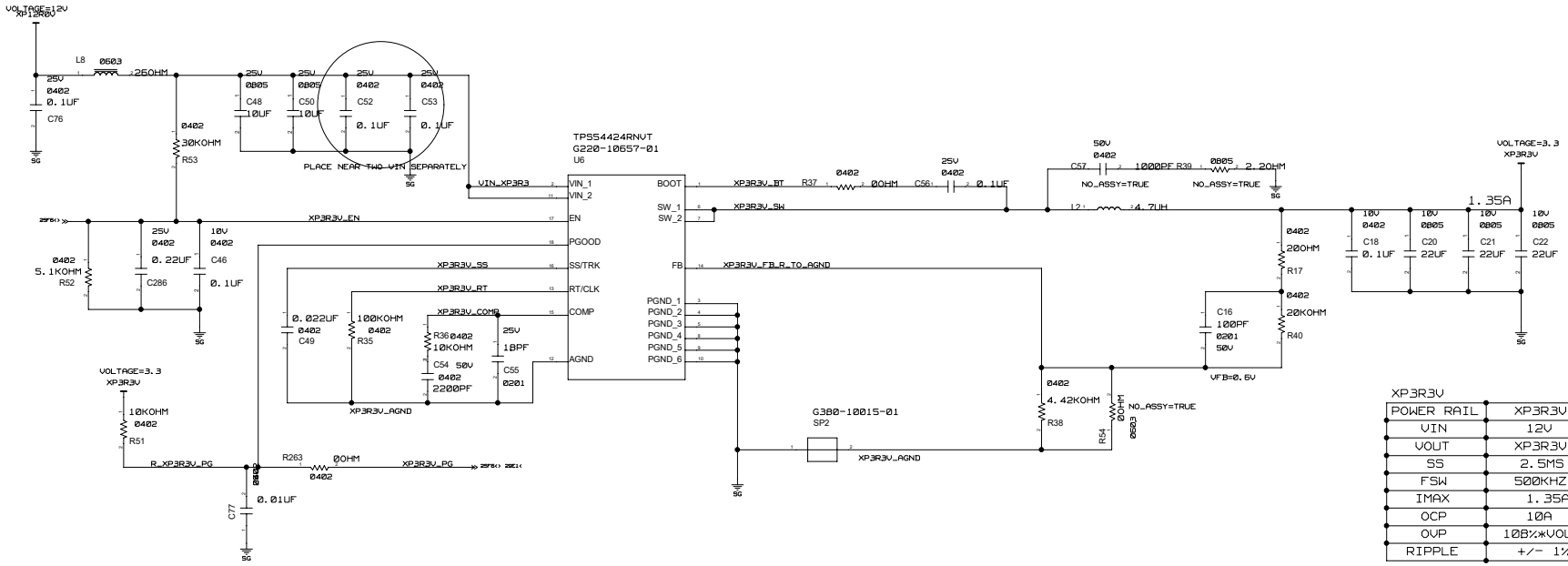
# XP3R3V



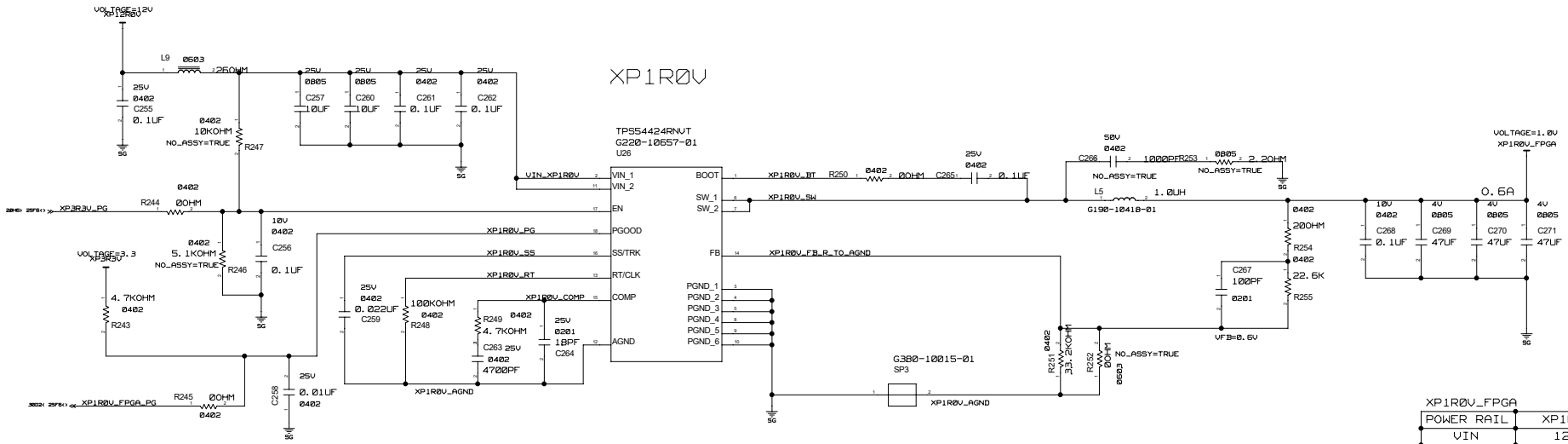

XP3R3V

| POWER RAIL | XP3R3V |
|---|---|
| VIN | 12V |
| VOUT | XP3R3V |
| SS | 2.5MS |
| FSW | 500KHZ |
| IMAX | 1.35A |
| OCP | 10A |
| OVP | 108%*VOUT |
| RIPPLE | +/- 1% |

XP3R3V

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 28 of 35 | CELESTICA |

# XP1R0V_FPGA




| XP1R0V_FPGA | |
|---|---|
| POWER RAIL | XP1R0V |
| VIN | 12V |
| VOUT | XP1R0V |
| SS | 2.5MS |
| FSW | 500KHZ |
| IMAX | 0.6A |
| OCP | 10A |
| OVP | 108%xVOUT |
| RIPPLE | +/- 1% |

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Celestica, Inc.
Enterprise Server & Storage Development
5000 Long Dong Ave.
Shanghai P.R.C. 201203
Engr BHUMARIN I., ZUJIAN ZHAO

| | | | |
|---|---|---|---|
| Title | X4 PCIE TIME CARD | Sheet | XP1R0V_FPGA |
| Size C+ | Document Number R4005-G0001-03-SC | Rev REV 2.0 (MP) | Sheet 29 OF 35 |
| Date: | SEP 02, 2022 | | |

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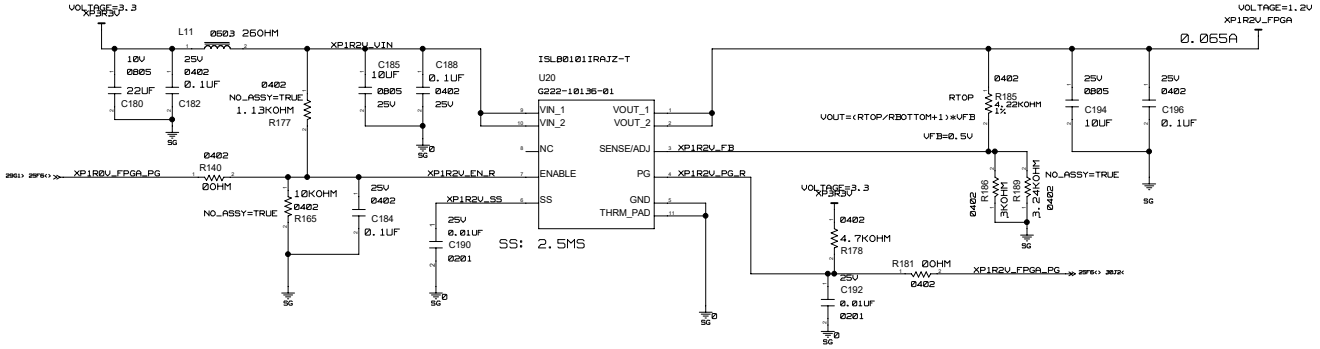
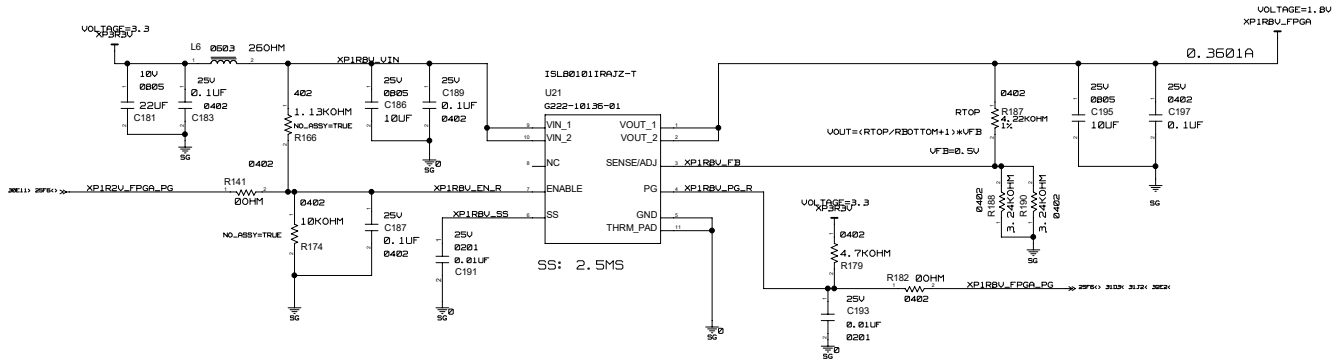
# XP1R2V_FPGA




| XP1R2V_FPGA | |
|---|---|
| PARAMETERS | VALUE(TYP) |
| VIN | 3.3V |
| VOUT | 1.2V |
| IOUT | 0.065A |
| OCP | 1.75A |

# XP1R8V_FPGA




| XP1R8V_FPGA | |
|---|---|
| PARAMETERS | VALUE(TYP) |
| VIN | 3.3V |
| VOUT | 1.8V |
| IOUT | 0.3601A |
| OCP | 1.75A |

## XP1R2V_FPGA & XP1R8V_FPGA

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 30 of 35 | CELESTICA |

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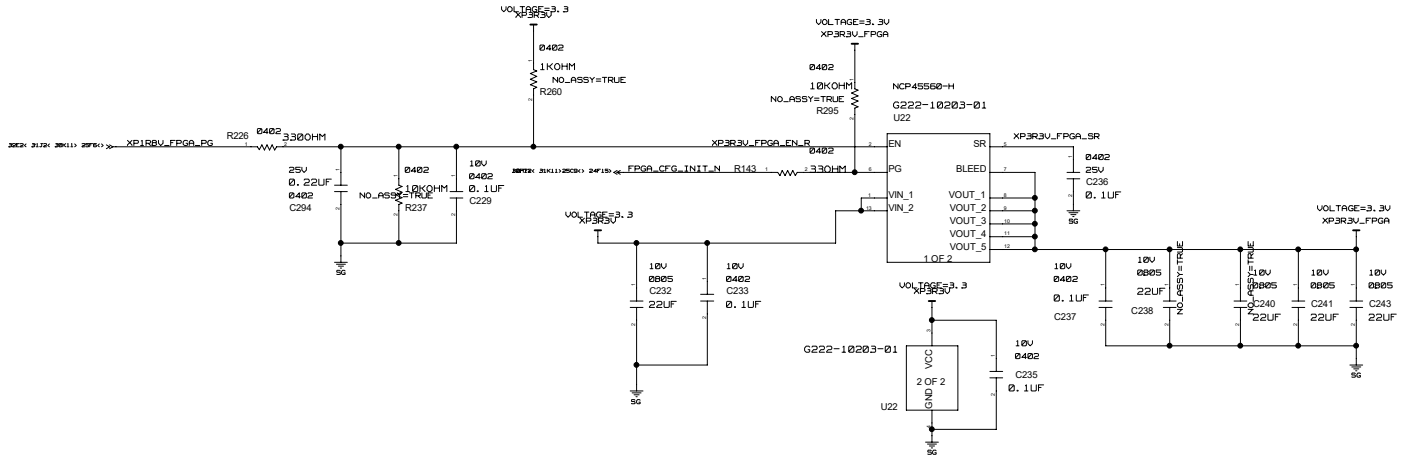
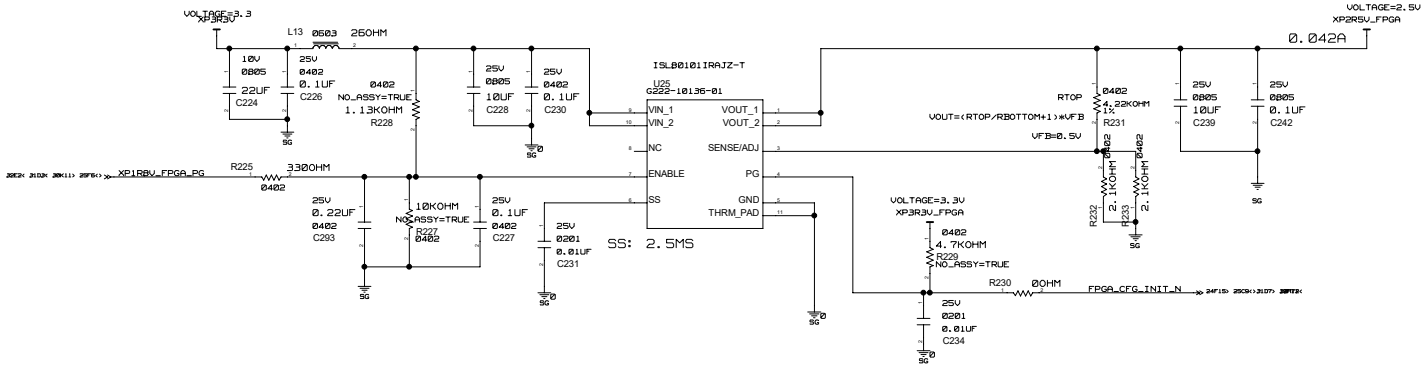
# XP3R3V_FPGA




| XP3R3V_FPGA | |
|---|---|
| VIN | 3V3 |
| RDSON | 4.3MOHM |
| IMAX | 0.1A |

# XP2R5V_FPGA




| XP2R5V_FPGA | |
|---|---|
| PARAMETERS | VALUE(TYP) |
| VIN | 3.3V |
| VOUT | 2.5V |
| IOUT | 0.042A |
| OCP | 1.75A |

## XP2R5V_FPGA&XP3R3V_FPGA

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 31 of 35 | CELESTICA |

CR-32 : @TIMECARD.LIB,TIMECARD(SCH_1):PAGE32

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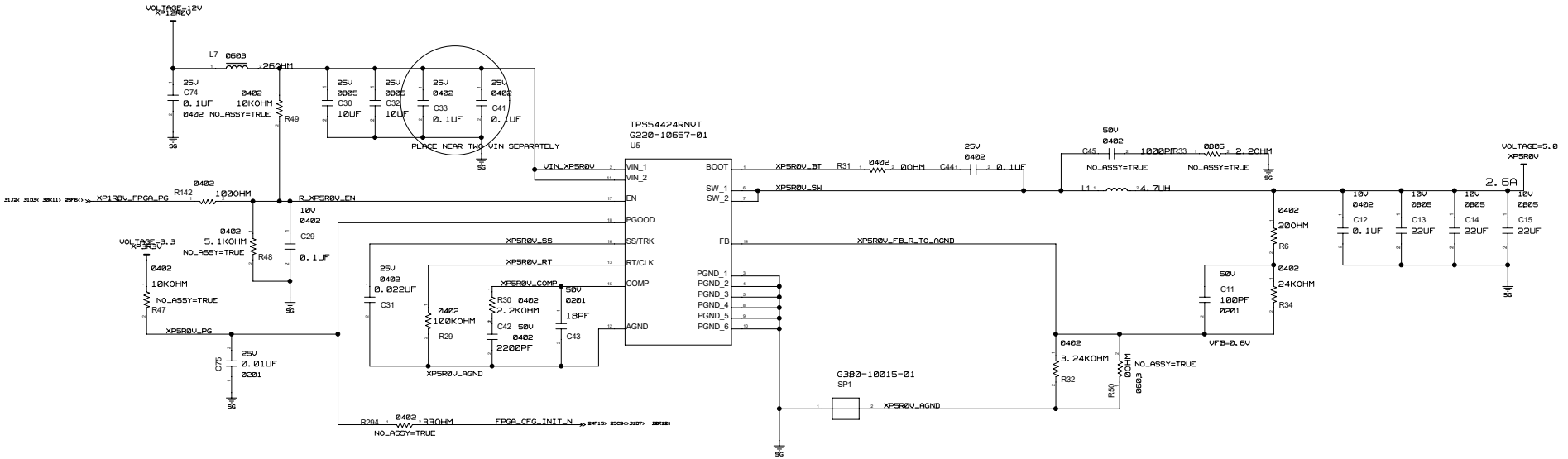
# XP5R0V




| XP5R0V | |
|---|---|
| POWER RAIL | XP5R0V |
| VIN | 12V |
| VOUT | XP5R0V |
| SS | 2.5MS |
| FSW | 500KHZ |
| IMAX | 2.6A |
| OCP | 10A |
| OVP | 108%*VOUT |
| RIPPLE | +/- 1% |

XP5R0V

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: BHUMARIN I., ZUMIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 [MP] |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 32 of 35 | CELESTICA |

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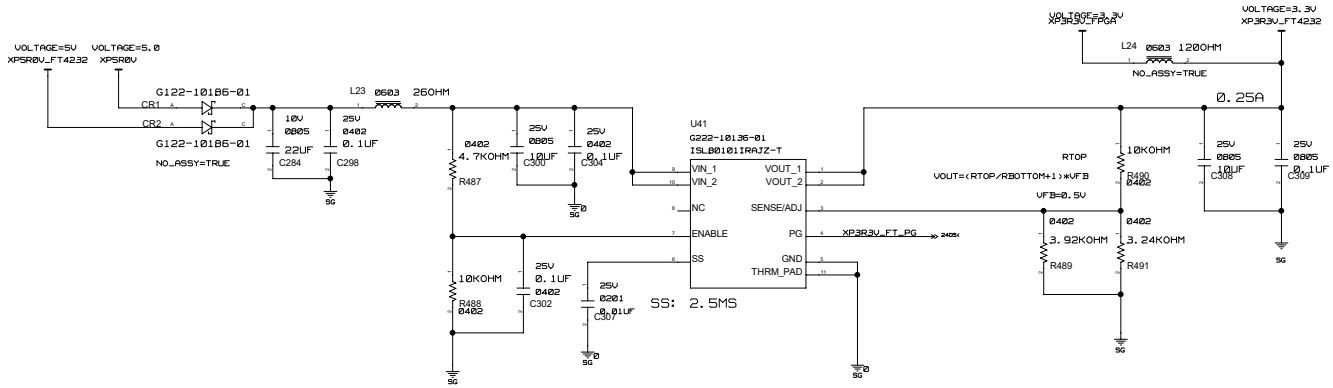
# XP3R3V_REG_FT




## XP3R3V_FT4232

| PARAMETERS | VALUE(TYP) |
|---|---|
| VIN | 5.0V |
| VOUT | 3.3V |
| IOUT | 0.25A |
| OCP | 1.75A |

## XP3R3V_FTDI

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 33 of 35 | CELESTICA |

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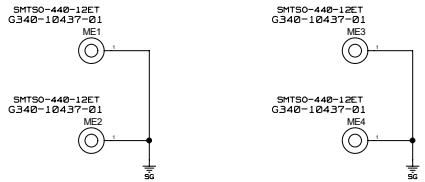
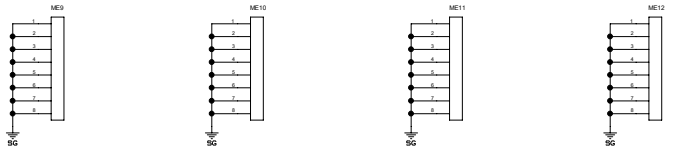
## STANDOFFS FOR GPS MODULE.




## MOUNTING HOLES FOR MAC MODULE.

## MOUNTING HOLES FOR THE PCIE CARD




## SOLDER PREFORM, ALLOY SAC305, 0603H

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| G3B0-10013-01 SP42 | G3B0-10013-01 SP43 | G3B0-10013-01 SP44 | G3B0-10013-01 SP45 | G3B0-10013-01 SP46 | G3B0-10013-01 SP47 | G3B0-10013-01 SP48 | G3B0-10013-01 SP49 | G3B0-10013-01 SP50 | G3B0-10013-01 SP51 | G3B0-10013-01 SP52 | G3B0-10013-01 SP53 |
| G3B0-10013-01 SP54 | G3B0-10013-01 SP55 | G3B0-10013-01 SP56 | G3B0-10013-01 SP57 | G3B0-10013-01 SP58 | G3B0-10013-01 SP59 | G3B0-10013-01 SP60 | G3B0-10013-01 SP61 | G3B0-10013-01 SP62 | G3B0-10013-01 SP63 | G3B0-10013-01 SP64 | G3B0-10013-01 SP65 |
| G3B0-10013-01 SP66 | G3B0-10013-01 SP67 | G3B0-10013-01 SP68 | G3B0-10013-01 SP69 | G3B0-10013-01 SP70 | G3B0-10013-01 SP71 | | | | | | |

## SOLDER PREFORM, ALLOY SAC305, 0201

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| G3B0-10015-01 SP4 | G3B0-10015-01 SP5 | G3B0-10015-01 SP6 | G3B0-10015-01 SP7 | G3B0-10015-01 SP8 | G3B0-10015-01 SP9 | G3B0-10015-01 SP10 | G3B0-10015-01 SP11 | G3B0-10015-01 SP12 | G3B0-10015-01 SP13 | G3B0-10015-01 SP14 | G3B0-10015-01 SP15 |
| G3B0-10015-01 SP16 | G3B0-10015-01 SP17 | G3B0-10015-01 SP18 | G3B0-10015-01 SP19 | G3B0-10015-01 SP20 | G3B0-10015-01 SP21 | G3B0-10015-01 SP22 | G3B0-10015-01 SP23 | G3B0-10015-01 SP24 | G3B0-10015-01 SP25 | G3B0-10015-01 SP26 | G3B0-10015-01 SP27 |
| G3B0-10015-01 SP28 | G3B0-10015-01 SP29 | G3B0-10015-01 SP30 | G3B0-10015-01 SP31 | G3B0-10015-01 SP32 | G3B0-10015-01 SP33 | G3B0-10015-01 SP34 | G3B0-10015-01 SP35 | G3B0-10015-01 SP36 | G3B0-10015-01 SP37 | G3B0-10015-01 SP38 | G3B0-10015-01 SP39 |
| G3B0-10015-01 SP40 | G3B0-10015-01 SP41 | | | | | | | | | | |

MECH_PART

| | |
|---|---|
| Title: X4 PCIE TIME CARD | Designer: IHUMARIN I., ZUTIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 (MP) |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 34 of 35 | CELESTICA |

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# CHANGE_LIST

| PAGE/REV | CONTENT | PAGE/REV | CONTENT |
|---|---|---|---|
| R4006-G0001-01-SC<br>REV 1.0 [EVT] | - SCHEMATIC RELEASE DATE: OCT 12, 2021.<br>- SCHEMATIC RELEASE FOR THE PCB CPN: R4006-B0001-01_R01.PCB RELEASE DATE: OCT 12, 2021. | | |
| | - SCHEMATIC RELEASE DATE: OCT 14, 2021.<br>- SCHEMATIC RELEASE FOR ASSY_CPN:R4006-G00001-01. | | |
| R4006-G0001-01-SC<br>REV 2.0 [EVT] | - SCHEMATIC RELEASE DATE: OCT 20, 2021.<br>- CHANGED R1B5 FROM CPN:G155-03241-01 TO CPN:G155-03001-01. R1B9 = NO_ASSY. | | |
| | | | |
| R4006-G0001-02-SC<br>REV 1.0 [DVT] | - SCHEMATIC RELEASE DATE: FEB 25, 2022.<br>- SCHEMATIC RELEASE FOR THE PCB CPN: R4006-B0001-02.PCB RELEASE DATE: FEB 25,2022. | | |
| R4006-G0001-02-SC<br>REV 2.0 [DVT] | - SCHEMATIC RELEASE DATE: MAR 10, 2022. SCHEMATIC RELEASE FOR PCBA CPN:R4006-G0001-02 REV03.<br>- PART SHORTAGE, CHANGED CPN:G222-00002-01"TPS3B0BG33" TO CPN:G229-10017-01"TPS3B0BG30". | | |
| | - THE LOGICAL LIBRARY FOR CPN:G229-10017-01 HAS NOT CREATED YET FOR THE CONCEPT HDL CAD<br>- THUS, MANUALLY CHANGE U34 FROM G222-00002-01 TO G229-10017-01 FOR THE BOM FILE. | | |
| | | | |
| R4006-G0001-03-SC<br>REV 1.0 [PVT] | - SCHEMATIC RELEASE DATE: JUL 05, 2022.<br>- SCHEMATIC RELEASE FOR PCBA CPN:R4006-G0001-03 REV01. | | |
| | - THE FLASHROM TOOL (FTDI<>SPI FLASH) DOES NOT SUPPORT YET FOR THE SPI FLASH CPN:G221-10224-01 MPN:MT25QL128ABA1ESE-0SIT.<br>- THUS, MANUALLY CHANGE U23 FROM G221-10224-01 TO G221-10359-01 FOR THE BOM FILE. | | |
| | | | |
| R4006-G0001-03-SC<br>REV 2.0 [MP] | - SCHEMATIC RELEASE DATE: SEP 02, 2022.<br>- SCHEMATIC RELEASE FOR PCBA CPN:R4006-G0001-03 REV03. | | |
| | - R450 = ASSY. R451 = NO_ASSY. R402= 2K2.<br>- CTH-MFG REQ. CHANGE Q'TY FOR CPN G300-10015-01 FROM 63 PCS TO 41 PCS. CPN G300-10013-01 FROM 62 PCS TO 30 PCS. | | |
| | - CTH-MFG REQ. CHANGE REFDES FOR CPN:G300-10015-01= SP1-SP41. THIS CHANGE WILL NOT AFFECT THE PCB LAYOUT.<br>- CTH-MFG REQ. CHANGE REFDES FOR CPN:G300-10013-01= SP42-SP71. THIS CHANGE WILL NOT AFFECT THE PCB LAYOUT. | | |
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|---|---|
| Title: X4 PCIE TIME CARD | Designer: BHUMARIN I., ZUJIAN ZHAO |
| Document Number: R4006-G0001-03-SC | Document Version: REV 2.0 [MP] |
| Assembly P/N: R4006-G0001-03 | Date: SEP 02, 2022 |
| Sheet: 35 of 35 | CELESTICA |

A3 (297X420)