**ТЕХНИЧЕСКИ УНИВЕРСИТЕТ - СОФИЯ**

**ФАКУЛТЕТ ПО ТЕЛЕКОМУНИКАЦИИ**

Протокол №4

*Проектиране на схеми на суматори и умножители на VHDL с помощта на WARP 6.2*

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Група: 46 Дата: 18.03.2015 г.

Преподавател: доц. д-р Галя Маринова Подпис:

1. Пълен еднобитов суматор

* Поведенческо описание на VHDL:

library ieee;

use ieee.std\_logic\_1164. all;

entity ADD is port (a, b, k : in std\_logic;

s, c : out std\_logic);

end ADD;

architecture archADD of ADD is

begin

process (a, b, k)

begin s<= a xor b xor k;

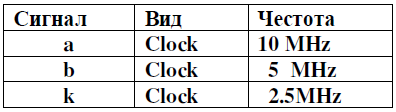
c<= (a and b) or ((a xor b) and k);

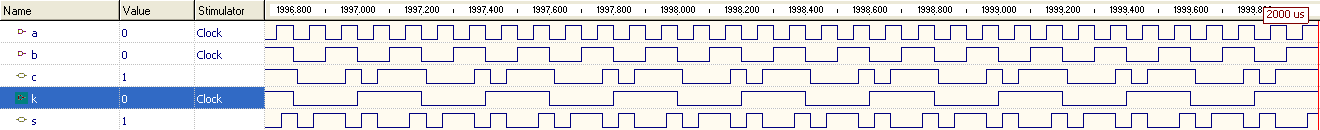
end process;

end archADD;



* + Резултати от симулацията на ACTIVE-HDL SIM с входни сигнали:





Фиг. 1

Получените резултати отговарят на таблицата на истинност на суматора.

* + Резултати от репорт файловете:

DESIGN EQUATIONS (14:00:10)

c =

b \* k

+ a \* k

+ a \* b

s =

a \* b \* k

+ /a \* /b \* k

+ /a \* b \* /k

+ a \* /b \* /k

PINOUT INFORMATION (14:00:11)

Device: cy37256p160

Package: cy37256p160-83ac

19 : k

20 : VCC

21 : GND

22 : b

31 : GND

59 : a

152 : s

156 : c

160 : VCC

RESOURCE UTILIZATION (14:00:11)

Information: Macrocell Utilization.

Description Used Max

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

| Dedicated Inputs | 1 | 1 |

| Clock/Inputs | 2 | 4 |

| I/O Macrocells | 2 | 128 |

| Buried Macrocells | 0 | 128 |

| PIM Input Connects | 3 | 624 |

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

8 / 885 = 0 %

Required Max (Available)

CLOCK/LATCH ENABLE signals 0 20

Input REG/LATCH signals 0 133

Input PIN signals 3 5

Input PINs using I/O cells 0 0

Output PIN signals 2 128

Total PIN signals 5 133

Macrocells Used 2 256

Unique Product Terms 7 1280

TIMING PATH ANALYSIS (14:00:11) using Package: cy37256p160-83ac

Messages:

----------------------------------------------------------------------------

Signal Name | Delay Type | tmax | Path Description

----------------------------------------------------------------------------

cmb::s[152]

inp::a

tPD 15.0 ns 1 pass

----------------------------------------------------------------------------

cmb::c[156]

inp::b

tPD 15.0 ns 1 pass

----------------------------------------------------------------------------

Worst Case Path Summary

-----------------------

tPD = 15.0 ns for s

* + Структурно описание на VHDL:

library ieee;

use ieee.std\_logic\_1164. all;

entity HalfADD is port (a, b : in std\_logic;

s, c : out std\_logic);

end HalfADD;

architecture archHalfADD of HalfADD is

begin

process (a, b)

begin s<= a xor b;

c<= a and b;

end process;

end archHalfADD;

library ieee;

use ieee.std\_logic\_1164.all;

entity FullADD is port (x,y,cin : in std\_logic;

s1, c1 : out std\_logic);

end FullADD;

architecture archFullADD of FullADD is

component HalfADD port (a, b : in std\_logic;

s, c : out std\_logic);

end component;

signal s2, c2, c3: std\_logic;

begin

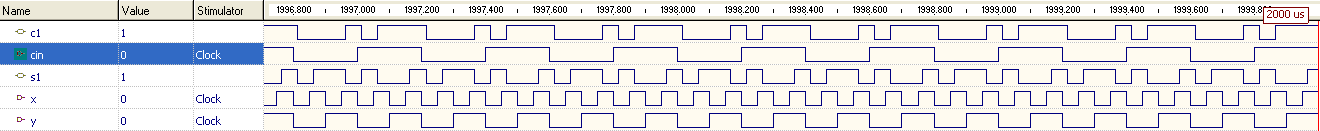
HalfADD1: HalfADD port map (x,y,s2,c2);

HalfADD2: HalfADD port map (s2,cin,s1,c3);

c1<=c2 or c3;

end archFullADD;

* + Резултати от симулацията на ACTIVE-HDL SIM:



Фиг. 2

* + Резултати от репорт файловете:

DESIGN EQUATIONS (14:10:09)

c1 =

x \* y

+ cin \* y

+ cin \* x

s1 =

cin \* x \* y

+ /cin \* /x \* y

+ /cin \* x \* /y

+ cin \* /x \* /y

PINOUT INFORMATION (14:10:10)

Device: cy37256p160

Package: cy37256p160-83ac

1 : GND

19 : y

22 : x

59 : cin

60 : VCC

151 : GND

152 : s1

156 : c1

160 : VCC

RESOURCE UTILIZATION (14:10:10)

Information: Macrocell Utilization.

Description Used Max

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

| Dedicated Inputs | 1 | 1 |

| Clock/Inputs | 2 | 4 |

| I/O Macrocells | 2 | 128 |

| Buried Macrocells | 0 | 128 |

| PIM Input Connects | 3 | 624 |

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

8 / 885 = 0 %

Required Max (Available)

CLOCK/LATCH ENABLE signals 0 20

Input REG/LATCH signals 0 133

Input PIN signals 3 5

Input PINs using I/O cells 0 0

Output PIN signals 2 128

Total PIN signals 5 133

Macrocells Used 2 256

Unique Product Terms 7 1280

TIMING PATH ANALYSIS (14:10:10) using Package: cy37256p160-83ac

Messages:

----------------------------------------------------------------------------

Signal Name | Delay Type | tmax | Path Description

----------------------------------------------------------------------------

cmb::s1[152]

inp::cin

tPD 15.0 ns 1 pass

----------------------------------------------------------------------------

cmb::c1[156]

inp::x

tPD 15.0 ns 1 pass

----------------------------------------------------------------------------

Worst Case Path Summary

-----------------------

tPD = 15.0 ns for s1

Резултатите от симулациите на двата модела са идентични: закъсненията и в двата варианта са по 15ns, използваните ресурси са еднакви, както и използваните изводи на схемата.

1. Четирибитов суматор, описан на VHDL със структурен модел.

library ieee;

use ieee.std\_logic\_1164.all;

entity adder\_1\_bit is port (a,b,Cin : in std\_logic; S, Cout : out

std\_logic);

end adder\_1\_bit;

architecture structure of adder\_1\_bit is

begin

process (a,b,Cin)

begin

S<= a xor b xor Cin;

Cout<= (a and b) or (b and Cin) or (a and Cin);

end process;

end structure;

library ieee;

use ieee.std\_logic\_1164.all;

entity adder\_4\_bit is

port ( Cin: in std\_logic;

a,b: in std\_logic\_vector(3 downto 0);

S: out std\_logic\_vector(3 downto 0);

Cout: out std\_logic );

end adder\_4\_bit;

architecture structure of adder\_4\_bit is

signal t: std\_logic\_vector (4 downto 0);

constant n: integer:=4;

**component adder\_1\_bit**

**port (a,b,Cin : in std\_logic;**

**S, Cout : out std\_logic);**

**end component;**

begin

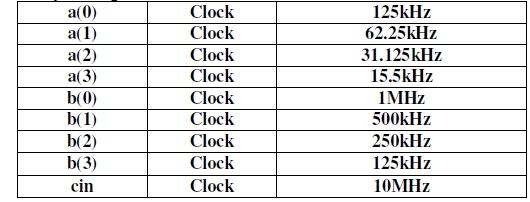
t(0) <=Cin; Cout <=t(n);

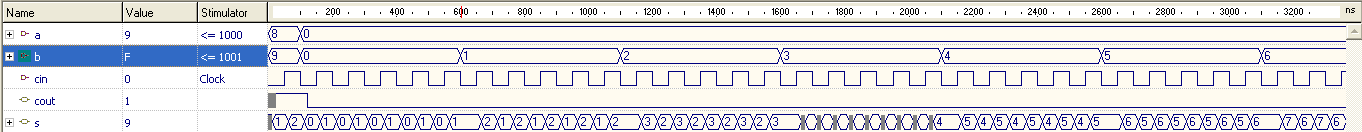
FA\_f: for i in 0 to n-1 **generate**

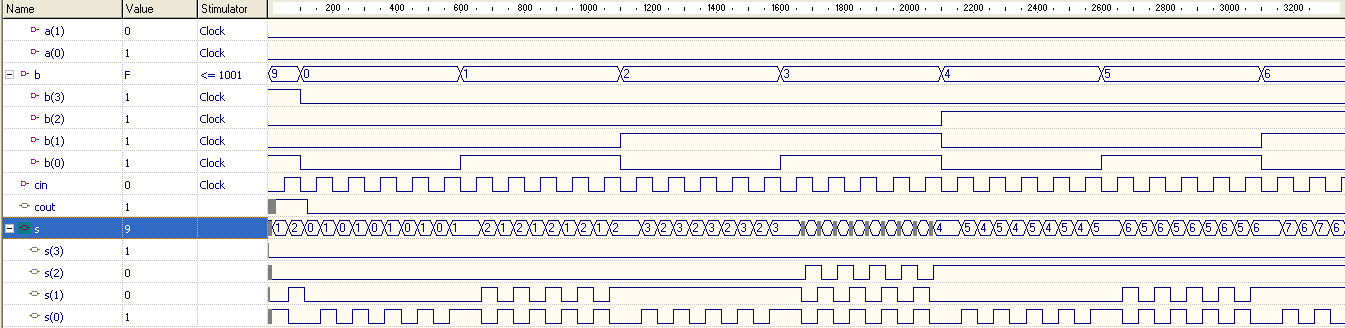
FA\_i: adder\_1\_bit port map (t(i), a(i), b(i), S(i), t(i+1));

end generate;

end structure;

* + Резултати от симулацията на ACTIVE-HDL SIM с входни сигнали:



Фиг.3

Фиг.4

* + Резултати от репорт файловете:

PINOUT INFORMATION (14:15:17)

Device: cy37256p160

Package: cy37256p160-83ac

1 : GND

19 : cin

20 : VCC

21 : GND

22 : b(3)

32 : (S\_2)

38 : (S\_7)

49 : a(1)

58 : a(0)

59 : b(2)

72 : s(3)

82 : s(1)

85 : s(0)

91 : s(2)

99 : b(1)

102 : b(0)

103 : cout

138 : a(3)

150 : a(2)

----------------------------------------------------------------------------

RESOURCE UTILIZATION (14:15:17)

Information: Macrocell Utilization.

Description Used Max

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

| Dedicated Inputs | 1 | 1 |

| Clock/Inputs | 4 | 4 |

| I/O Macrocells | 11 | 128 |

| Buried Macrocells | 6 | 128 |

| PIM Input Connects | 26 | 624 |

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

48 / 885 = 5 %

Required Max (Available)

CLOCK/LATCH ENABLE signals 0 20

Input REG/LATCH signals 0 133

Input PIN signals 5 5

Input PINs using I/O cells 4 4

Output PIN signals 5 124

Total PIN signals 14 133

Macrocells Used 13 256

Unique Product Terms 123 1280

TIMING PATH ANALYSIS (14:15:17) using Package: cy37256p160-83ac

Messages:

----------------------------------------------------------------------------

Signal Name | Delay Type | tmax | Path Description

----------------------------------------------------------------------------

cmb::s(3)[72]

inp::b(0)

---->S\_1

tPD 26.0 ns 2 passes

----------------------------------------------------------------------------

cmb::s(1)[82]

inp::b(0)

tPD 15.0 ns 1 pass

----------------------------------------------------------------------------

cmb::s(0)[85]

inp::b(0)

tPD 15.0 ns 1 pass

----------------------------------------------------------------------------

cmb::s(2)[91]

inp::b(0)

---->S\_5

tPD 26.0 ns 2 passes

----------------------------------------------------------------------------

cmb::cout[103]

inp::b(0)

---->S\_7

tPD 26.0 ns 2 passes

----------------------------------------------------------------------------

Worst Case Path Summary

tPD = 26.0 ns for s(3)

1. 16-битов суматор, описан на VHDL с поведенчески модел.

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

use ieee.std\_logic\_unsigned.all;

entity adder\_n\_bit is **generic(n: natural :=16);**

port( A: in std\_logic\_vector(**n-1** downto 0);

B: in std\_logic\_vector(**n-1** downto 0);

carry: out std\_logic;

sum: out std\_logic\_vector(**n-1** downto 0));

end adder\_n\_bit;

architecture behv of adder\_n\_bit is

signal result: std\_logic\_vector(**n** downto 0);

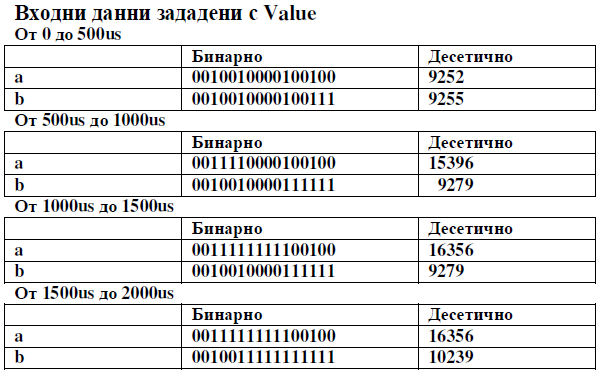
begin

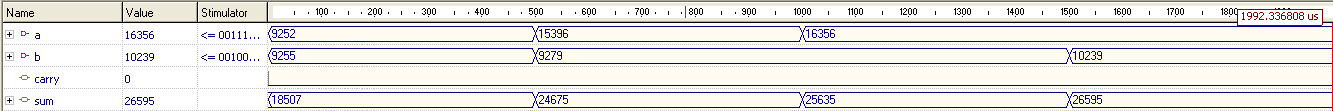
result <= ('0' & A)+('0' & B);

sum <= result(**n-1** downto 0);

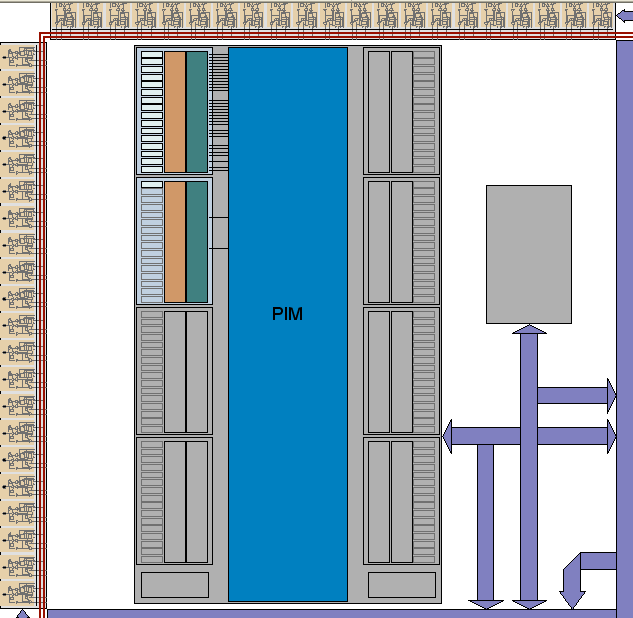
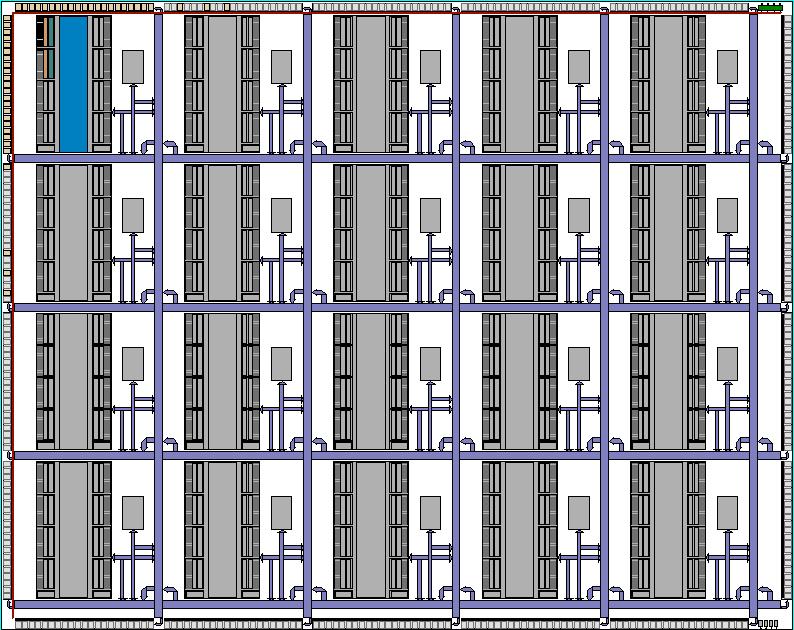
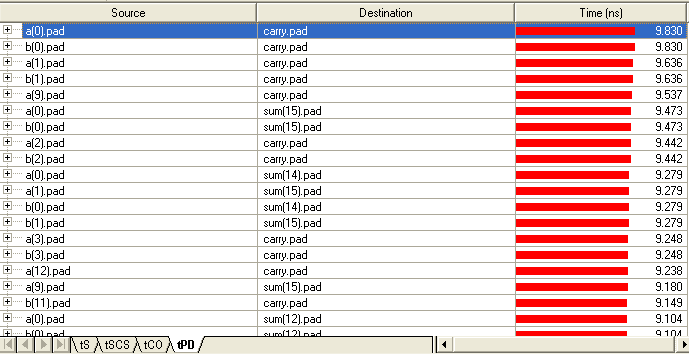
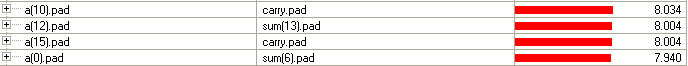
carry <= result(**n**);

end behv;

* + Резултати от симулацията на ACTIVE-HDL SIM с входни сигнали:



Фиг. 5

* + Заета площ и времезакъснения, представени с модула **Architecture Explorer**
  + Задаване на 32-битов суматор чрез промяна на VHDL кода и промяна на заетата площ:

library ieee;

use ieee.std\_logic\_1164.all; use ieee.std\_logic\_arith.all;

use ieee.std\_logic\_unsigned.all;

entity adder\_n\_bit is **generic(n: natural :=32);**

port( A: in std\_logic\_vector(**n-1** downto 0);

B: in std\_logic\_vector(**n-1** downto 0);

carry: out std\_logic;

sum: out std\_logic\_vector(**n-1** downto 0));

end adder\_n\_bit;

architecture behv of adder\_n\_bit is

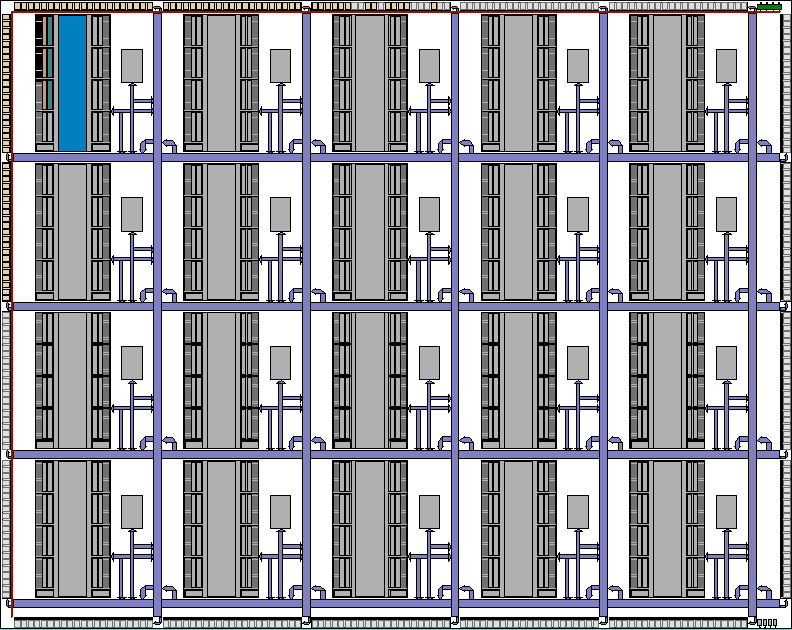
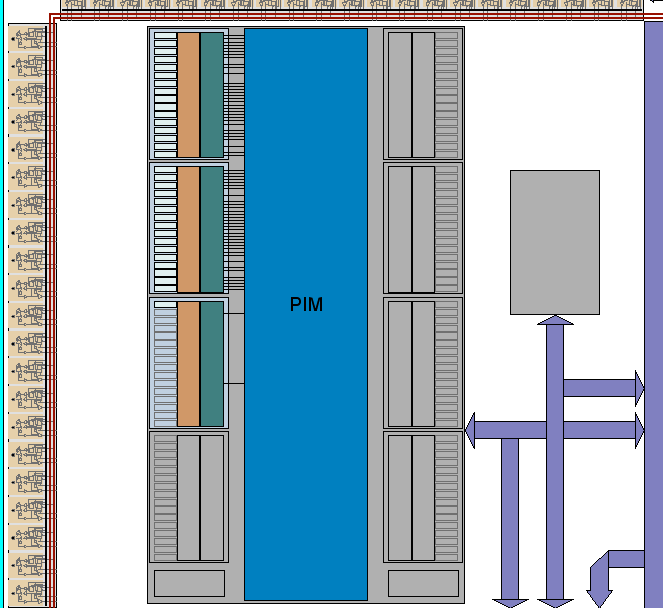
signal result: std\_logic\_vector(**n** downto 0);

begin

result <= ('0' & A)+('0' & B);

sum <= result(**n-1** downto 0);

carry <= result(**n**);

end behv;

Chip resource summary – 16-битов суматор

------------------------------------------------------------

Resource Type : Used : Free : Max : % Used

======================================

Macrocells : 17 : 2543 : 2560 : 0.66%

Cluster Memories : 0 : 40 : 40 : 0.00%

Channel Memories : 0 : 20 : 20 : 0.00%

IO Cells : 49 : 329 : 378 : 12.96%

Global Clocks : 0 : 4 : 4 : 0.00%

Global Controls : 0 : 4 : 4 : 0.00%

Logic Blocks : 2 : 158 : 160 : 1.25%

Cluster Blocks : 1 : 19 : 20 : 5.00%

Chip resource summary – 32-битов суматор

------------------------------------------------------------

Resource Type : Used : Free : Max : % Used

======================================

Macrocells : 33 : 2527 : 2560 : 1.29%

Cluster Memories : 0 : 40 : 40 : 0.00%

Channel Memories : 0 : 20 : 20 : 0.00%

IO Cells : 97 : 281 : 378 : 25.66%

Global Clocks : 0 : 4 : 4 : 0.00%

Global Controls : 0 : 4 : 4 : 0.00%

Logic Blocks : 3 : 157 : 160 : 1.88%

Cluster Blocks : 1 : 19 : 20 : 5.00%

1. Натрупващ умножител с 8-битови множители и 16-битово произведение

library ieee;

use ieee.std\_logic\_1164.all;

entity math is port (

clk, rst: std\_logic;

a, b: in std\_logic\_vector(7 downto 0);

q: buffer std\_logic\_vector(15 downto 0));

end math;

use work.std\_arith.all;

architecture math of math is

begin

p1: process (rst, clk)

begin

if rst = '1' then

q <= (others => '0');

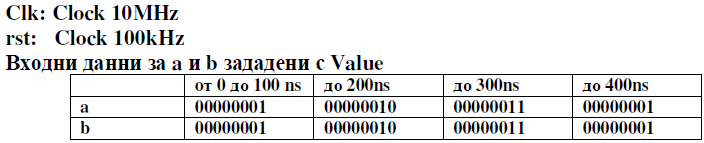
elsif clk'event and clk='1' then

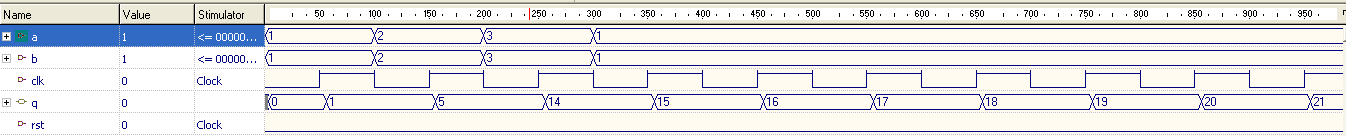
q <= (a \* b) + q;

end if;

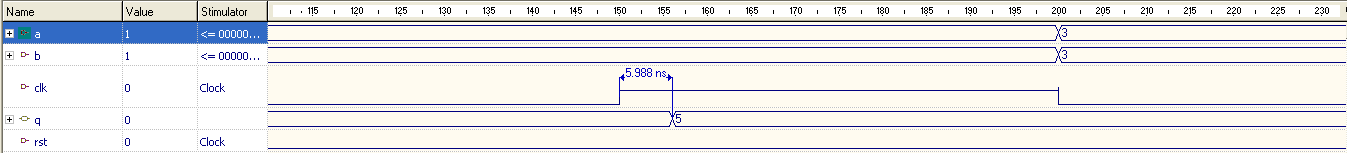
end process;

end math;

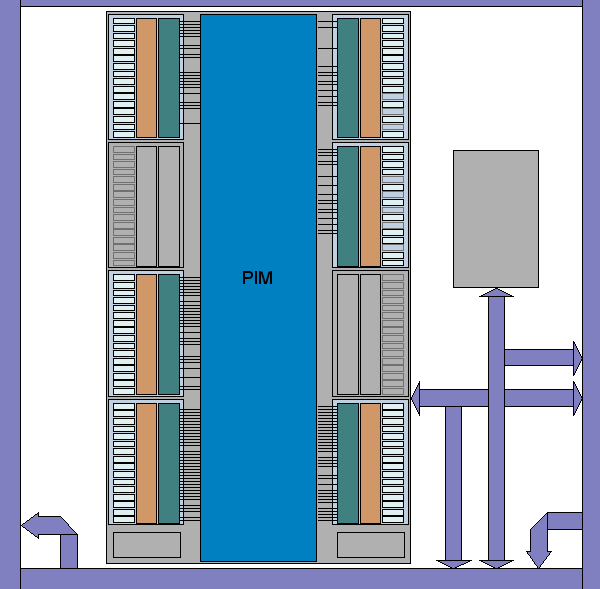
* + Резултати от симулацията на ACTIVE-HDL SIM с входни сигнали:

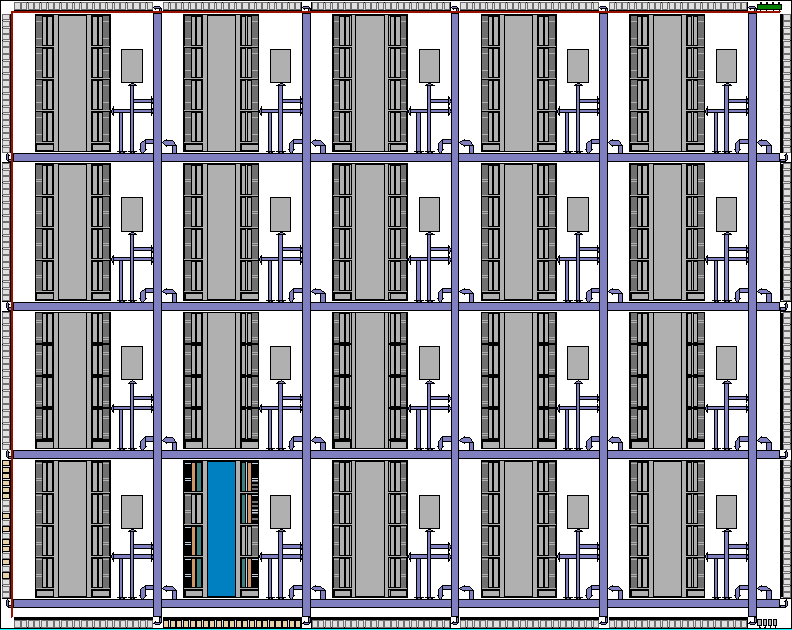
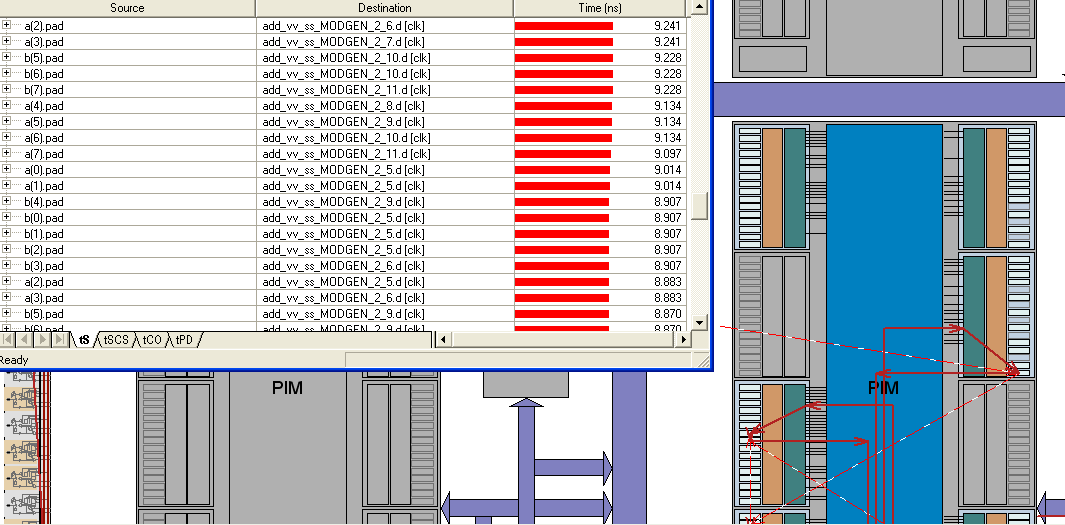
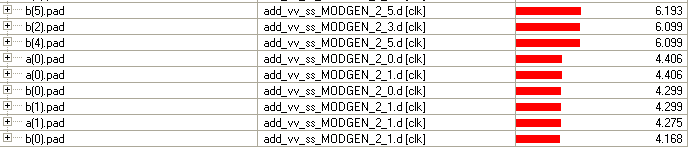


Фиг. 5

* + Времезакъснения, определени от времедиаграмата: 5,988ns

Фиг. 6

* + Заета площ и времезакъснения, представени с модула **Architecture Explorer**



Chip resource summary

--------------------------------

Resource Type : Used : Free : Max : % Used

=================================

Macrocells : 88 : 2472 : 2560 : 3.44%

Cluster Memories : 0 : 40 : 40 : 0.00%

Channel Memories : 0 : 20 : 20 : 0.00%

IO Cells : 33 : 345 : 378 : 8.73% Global Clocks : 1 : 3 : 4 : 25.00% Global Controls : 0 : 4 : 4 : 0.00% Logic Blocks : 6 : 154 : 160 : 3.75% Cluster Blocks : 1 : 19 : 20 : 5.00%