



EE308
MICROPROCESSORS LABORATORY

LAB -6-

Safe Lock

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The main body

```
LAB6.c startup_TM4C123.s
1  #include <stdint.h>
2  #include <stdlib.h>
3  #include <tm4cl23gh6pm.h> /*By adding the header file we don't need to define the registers*/
4
5  /* Declaring functions we may use */
6  void SysClock_40MHz ();
7  void SysTick_init();
8  void SysTick_Wait(unsigned long reload);
9  void SysTick_Wait_n_ms(unsigned long n);
10 void Port_A_init ();
11 void Port_B_init ();
12 void Port_F_init ();
13 unsigned long resistanceRead();
14 void ADC0_PE3_init(void);
15
16
17 int main(void)
18 {
19     SysClock_40MHz ();
20     SysTick_init();
21     Port_A_init ();
22     Port_B_init ();
23     Port_F_init ();
24     ADC0_PE3_init();
25
26     int set, open, phase=0;          // Variables to save the 1)set button read 2)open button read 3)The phases
27     int L[3], S[3];                 // Arrays to hold POT variables (L[3] for setting S[3] for opening
28
29     while(1)
30     {
31         set = GPIO_PORTF_DATA_R & 0x10; // Read and hold SW1 value (set button)
32         open = GPIO_PORTF_DATA_R & 0x01; // Read and hold SW2 value (open button)
33
34         if(GPIO_PORTA_DATA_R == 0x00)    // This line is to check the locks state. If they are locked
                                           // and set button is pressed it will not enter the setting phase
```

```
30 set = GPIO_PORTF_DATA_R & 0x10; // Read and hold SW1 value (set button)
31 open = GPIO_PORTF_DATA_R & 0x01; // Read and hold SW2 value (open button)
32
33 if(GPIO_PORTA_DATA_R == 0x00) // This line is to check the locks state. If they are locked
34 // and set button is pressed it will not enter the setting phase
35 {
36     while(set==0) // If set button(negative logic) has been pressed enter the set phase
37     {
38         switch(phase)
39         { case 0: // Setting the value of the 1st lock
40             GPIO_PORTA_DATA_R ^= 0x80; // Toggle only the first LED-PA7 (Lock 1)
41             SysTick_Wait_n_ms(250); // Toggling with 1/4 sec intervals
42             if((GPIO_PORTB_DATA_R & 0x10)==0x10) // Reading the next button (PB4).If it pressed:
43             { L[0]= (resistanceRead()/100); // Hold the POT value divided by 100 in the first element of L array.
44                 // Lock 1 value is set
45                 GPIO_PORTA_DATA_R |= 0x80; // Stop toggling (Lit) first LED (Lock 1 is locked)
46                 phase++; // Go to the next phase
47             }
48             break;
49
50             case 1: // Setting the value of the 2nd lock
51                 GPIO_PORTA_DATA_R ^= 0x40; // Toggle only the 2nd LED-PA6 (Lock 2).The 1st LED has been lit
52                 // in previous phase and it will not change because we XORing it with 0
53                 SysTick_Wait_n_ms(250); // Toggling with 1/4 sec intervals
54                 if((GPIO_PORTB_DATA_R & 0x10)==0x10) // Reading the next button (PB4).If it pressed:
55                 { L[1]= (resistanceRead()/100); // Hold the POT value divided by 100 in the 2nd element of L array.
56                     // Lock 2 value is set
57                     GPIO_PORTA_DATA_R |= 0x40; // Stop toggling(Lit) 2nd LED (Lock 2 is locked)
58                     phase++; // Go to the next phase
59                 }
60                 break;
61
62             case 2: // Setting the value of the 3rd lock
63                 GPIO_PORTA_DATA_R ^= 0x20; // Toggle only the 3rd LED-PA5(Lock 3).The 1st&2nd LEDs have been lit
```

```

62         case 2:                // Setting the value of the 3rd lock
63             GPIO_PORTA_DATA_R ^= 0x20;    // Toggle only the 3rd LED-PA5(Lock 3).The 1st&2nd LEDs have been lit
64                                           // in previous phase and they will not change because we XORing them with 0
65             SysTick_Wait_n_ms(250);        // Toggling with 1/4 sec intervals
66             if((GPIO_PORTB_DATA_R & 0x10)==0x10) // Reading the next button (PB4).If it pressed:
67             { L[2]= (resistanceRead()/100);      // Hold the POT value divided by 100 in the 3rd element of L array.
68                                           // Lock 3 value is set
69             GPIO_PORTA_DATA_R |= 0x20;        // Stop toggling(Lit) 3rd LED (Lock 3 is locked)
70             phase++;                          // Go to the next phase
71         }
72         break;
73
74         case 3:                // Ending setting phase
75             set=1;phase=0;      // Clear set value(negative logic) and clear phase value
76         break;
77     }
78 }
79 }
80
81 if(GPIO_PORTA_DATA_R == 0xE0)    // This line is to check the locks state. If they are open
82                                 // and open button is pressed it will not enter the opening phase
83 {
84     while(open==0)              // If open button(negative logic) has been pressed enter the open phase
85     {
86         switch(phase)
87         { case 0:                // Opening the 1st lock
88             GPIO_PORTA_DATA_R ^= 0x80;    // Toggle only the first LED-PA7 (Lock 1)
89             SysTick_Wait_n_ms(250);        // Toggling with 1/4 sec intervals
90             if((GPIO_PORTB_DATA_R & 0x10)==0x10) // Reading the next button (PB4).If it pressed:
91             { S[0]= (resistanceRead()/100);      // Hold the POT value divided by 100 in the first element of S array.
92                                           // someone entered value to open 1st lock
93             if(L[0]==S[0])                // Compare the set value of 1st lock (previously set) with the value
94                                           // recently entered. If they are equal:
95             { GPIO_PORTA_DATA_R &= ~0x80;    // Stop toggling(Turn OFF) first LED (Lock 1 is opened)

```



```
84 while(open==0) // If open button(negative logic) has been pressed enter the open phase
85 {
86     switch(phase)
87     { case 0: // Opening the 1st lock
88         GPIO_PORTA_DATA_R ^= 0x80; // Toggle only the first LED-PA7 (Lock 1)
89         SysTick_Wait_n_ms(250); // Toggling with 1/4 sec intervals
90         if((GPIO_PORTB_DATA_R & 0x10)==0x10) // Reading the next button (PB4).If it pressed:
91         { S[0]= (resistanceRead()/100); // Hold the POT value divided by 100 in the first element of S array.
92         // someone entered value to open 1st lock
93         if(L[0]==S[0]) // Compare the set value of 1st lock (previously set) with the value
94         // recently entered. If they are equal:
95         { GPIO_PORTA_DATA_R &= ~0x80; // Stop toggling(Turn OFF) first LED (Lock 1 is opened)
96         phase++; // Go to the next phase
97         }
98     }
99     break;
100
101     case 1: // Opening the 2nd lock
102         GPIO_PORTA_DATA_R ^= 0x40; // Toggle only the 2nd LED-PA6 (Lock 2)
103         SysTick_Wait_n_ms(250); // Toggling with 1/4 sec intervals
104         if((GPIO_PORTB_DATA_R & 0x10)==0x10) // Reading the next button (PB4).If it pressed:
105         { S[1]= (resistanceRead()/100); // Hold the POT value divided by 100 in the 2nd element of S array.
106         // someone entered value to open 2nd lock
107         if(L[1]==S[1]) // Compare the set value of 2nd lock (previously set) with the value
108         // recently entered. If they are equal:
109         { GPIO_PORTA_DATA_R &= ~0x40; // Stop toggling(Turn OFF) 2nd LED (Lock 2 is opened)
110         phase++; // Go to the next phase
111         }
112     }
113     break;
114
115     case 2: // Opening the 3rd lock
116         GPIO_PORTA_DATA_R ^= 0x20; // Toggle only the 3rd LED-PA5 (Lock 3)
117         SysTick_Wait_n_ms(250); // Toggling with 1/4 sec intervals
```

```

114
115     case 2:                                // Opening the 3rd lock
116         GPIO_PORTA_DATA_R ^= 0x20;        // Toggle only the 3rd LED-PA5 (Lock 3)
117         SysTick_Wait_n_ms(250);           // Toggling with 1/4 sec intervals
118         if((GPIO_PORTB_DATA_R & 0x10)==0x10) // Reading the next button (PB4).If it pressed:
119         { S[2]= (resistanceRead()/100);    // Hold the POT value divided by 100 in the 3rd element of S array.
120                                             // someone entered value to open 3rd lock
121             if(L[2]==S[2])                // Compare the set value of 3rd lock (previously set) with the value
122                                             // recently entered. If they are equal:
123             { GPIO_PORTA_DATA_R &= ~0x20; // Stop toggling(Turn OFF) 3rd LED (Lock 3 is opened)
124               phase++;                    // Go to the next phase
125             }
126         }
127         break;
128
129     case 3:                                // Ending opening phase
130         open=1;phase=0;                   // Clear open value(negative logic) and clear phase value
131         break;
132     }
133 }
134 }
135 }
136
137 return 0;
138 }
139
140
141
142
143 /* Function to set system clock for 40MHz */
144 void SysClock_40MHz ()
145 { /* 1- Enabling USERCC2 in RCC2 */
146   SYSTL_RCC2_R |= 0x80000000;           //RCC2{31}=1
147   /* 2- Bypass PLL while initializing */

```

The functions we used

```
LAB6.c startup_TM4C123.s
140
141
142
143 /* Function to set system clock for 40MHz */
144 void SysClock_40MHz ()
145 { /* 1- Enableing USERCC2 in RCC2 */
146     SYSCTL_RCC2_R |= 0x80000000; //RCC2[31]=1
147     /* 2- Bypass PLL while initializing */
148     SYSCTL_RCC2_R |= 0x00000800; //RCC2[11]=1
149     /* 3- Setting external crystal value and oscillator source for PLL */
150     SYSCTL_RCC_R = (SYSCTL_RCC_R &~ 0X000007C0) //Clearing RCC[10:6] then setting XTAL=RCC[10:6]=15 (16MHz ext. OSC.
151                     +(0x15<<6);
152     /* 4- Configuration for main oscillator source */
153     SYSCTL_RCC2_R &= ~0x00000070; //Clearing RCC2[6:4] OSCSRRC2 =000=MOSC
154     /* 5- Clearing PWRDN to active PLL */
155     SYSCTL_RCC2_R &= ~0x00002000; //Clearing RCC2[13]=PERDN=0
156     /* 6- Setting system clock */
157     SYSCTL_RCC2_R |= 0x40000000; //Setting RCC2[30]=1 (selecting DIV400=400MHz
158     /* 7- Setting system clock divider RCC[28:22] */
159     SYSCTL_RCC2_R = (SYSCTL_RCC2_R &~ 0x1FC00000)+(0x09<<22); //Gives N=9
160     /* 8- Wait for PLL to lock by polling PLLRIS */
161     while ((SYSCTL_RIS_R &0x00000040)==0){};
162     /* 9- Setting BYPASS to 0, select PLL as the source of system clock */
163     SYSCTL_RCC2_R &= ~0x00000800; //RCC2[11]=1
164 }
165
166 /* Function for initializing SysTick counter */
167 void SysTick_init(void)
168 { NVIC_ST_CTRL_R =0; // Disabling
169   NVIC_ST_RELOAD_R =0x00FFFFFF; // Max reload value
170   NVIC_ST_CURRENT_R =0; // Any write clears it
171   NVIC_ST_CTRL_R =0x00000005; // Enabling SysTick with core clock
172 }
173
```



```
172 }
173
174 /* Function to determine reload value (how many clock cycles to wait).40MHz (25ns period) clock */
175 void SysTick_Wait(unsigned long reload)
176 { NVIC_ST_RELOAD_R = reload;
177   NVIC_ST_CURRENT_R = 0;
178   while((NVIC_ST_CTRL_R & 0x00010000)==0){} //Waiting for flag
179 }
180
181 /* Function for wait n ms (considering 40MHz clock) */
182 void SysTick_Wait_n_ms(unsigned long n)
183 { unsigned long i;
184   for(i=0 ; i<n ; i++)
185     {SysTick_Wait(39999);}
186 }
187
188 /* Function to initilaize Port B */
189 void Port_B_init ()
190 { SYSTCL_RCGCGPIO_R |= 0x02 ; // GPIO Port B Run Mode Clock Gating Control
191   while((SYSTCL_PRGPIO_R & 0x02) == 0){}; // Waiting for peripherals to be ready
192   GPIO_PORTB_DIR_R |= ~0x10; // Specifie PB4 input (Next botton)
193   GPIO_PORTB_DEN_R |= 0x10; // Enabling pin as digital
194   GPIO_PORTB_DATA_R = 0x00; // Intialize data to 0
195 }
196
197 /* Function to initilaize Port A */
198 void Port_A_init ()
199 { SYSTCL_RCGCGPIO_R |= 0x01 ; // GPIO Port A Run Mode Clock Gating Control
200   while((SYSTCL_PRGPIO_R & 0x01) == 0){}; // Waiting for peripherals to be ready
201   GPIO_PORTA_DIR_R = 0xE0; // Specifie PA7-5 output (The three Locks(LEDs) respectively)
202   GPIO_PORTA_DEN_R = 0xE0; // Enabling pins as digital
203   GPIO_PORTA_DATA_R = 0; // Intialize data to 0
204 }
205
```

```
206 /* Function to initialize Port F */
207 void Port_F_init ()
208 {
209     SYSCTL_RCGCGPIO_R |= 0x20 ;           // GPIO Port F Run Mode Clock Gating Control
210     while((SYSCTL_PRGPIO_R & 0x20) == 0){}; // Waiting for peripherals to be ready
211     GPIO_PORTF_LOCK_R = 0x4c4f434b;       // Unlocking Port F
212     GPIO_PORTF_CR_R = 0xFF;               // Allow changing to the pins
213     GPIO_PORTF_PUR_R |= 0x11;             // Enabling Pull-Up resistors for PF4 and PF0
214     GPIO_PORTF_DIR_R = ~0x11;            // Specifie PF4 and PF0 inputs (Set locks/open locks buttons respectively)
215     GPIO_PORTF_DEN_R = 0x11;             // Enabling digital functionality
216     GPIO_PORTF_DATA_R = 0;               // Initialize data to 0
217 }
218
219 void ADC0_PE3_init(void) {
220
221     SYSCTL_RCGCADC_R |= 0x01;             // Activate ADC0
222     SYSCTL_RCGCGPIO_R |= 0x10;           // Activate clock for Port E
223     while((SYSCTL_PRGPIO_R & 0x10) == 0){}; // Wait for stabilization
224     GPIO_PORTE_DIR_R &= ~0x08;           // Make PE3 input
225     GPIO_PORTE_AFSEL_R |= 0x08;          // Enable alternate function on PE3
226     GPIO_PORTE_DEN_R &= ~0x08;           // Disable digital I/O on PE3
227     GPIO_PORTE_AMSEL_R |= 0x08;          // Enable analog functionality on PE3
228     ADC0_PC_R &= ~0xF;                  // Clear sampling rate
229     ADC0_PC_R |= 0x1;                   // Configure for 125K samples/sec
230     ADC0_SS PRI_R = 0x0123;              // Sequencer 3 is highest priority
231     ADC0_ACTSS_R &= ~0x0008;            // Disable sample sequencer 3
232     ADC0_EMUX_R &= ~0xF000;             // Seq3 is software trigger
233     ADC0_SSMUX3_R &= ~0xF;              // Clear channel selection
234     ADC0_SSMUX3_R += 0;                  // Set channel AIN0
235     ADC0_SSCTL3_R = 0x6;                 // No TS0 D0, Yes IE0 END0
236     ADC0_ACTSS_R |= 0x8;                 // Enable SS3
237 }
238
239
```

```
218
219 void ADC0_PE3_init(void){
220
221
222     SYSCTL_RCGCADC_R |= 0x01;           // Activate ADC0
223     SYSCTL_RCGCGPIO_R |= 0x10;         // Activate clock for Port E
224     while((SYSCTL_PRGPIO_R&0x10) == 0){}; // Wait for stabilization
225     GPIO_PORTE_DIR_R &= ~0x08;         // Make PE3 input
226     GPIO_PORTE_AFSEL_R |= 0x08;        // Enable alternate function on PE3
227     GPIO_PORTE_DEN_R &= ~0x08;        // Disable digital I/O on PE3
228     GPIO_PORTE_AMSEL_R |= 0x08;       // Enable analog functionality on PE3
229     ADC0_PC_R &= ~0xF;                 // Clear sampling rate
230     ADC0_PC_R |= 0x1;                  // Configure for 125K samples/sec
231     ADC0_SSPRI_R = 0x0123;             // Sequencer 3 is highest priority
232     ADC0_ACTSS_R &= ~0x0008;          // Disable sample sequencer 3
233     ADC0_EMUX_R &= ~0xF000;           // Seq3 is software trigger
234     ADC0_SSMUX3_R &= ~0xF;            // Clear channel selection
235     ADC0_SSMUX3_R += 0;                 // Set channel AINO
236     ADC0_SSCTL3_R = 0x6;               // No TSO D0, Yes IE0 END0
237     ADC0_ACTSS_R |= 0x8;               // Enable SS3
238 }
239
240 /* Function convert from ADC value to readale voltage */
241 unsigned long resistanceRead ()
242 {
243     unsigned long ADC_result, R;
244
245     ADC0_PSSI_R = 0x0008;               // Initiate SS3
246     while((ADC0_RIS_R&0x08)==0){};      // Wait for A/D conversion to finish
247     ADC_result = ADC0_SSIFIFO3_R&0xFFF; // Get ADC result
248     ADC0_ISC_R = 0x0008;               // Clear interrupt status for SS3 to be able to start sampling again
249     return R = (ADC_result)*(10000/4095.0); // Convert ADC value to resistance by quantizing
250 }
```

Video Link

<https://youtu.be/vYyftYnwnLE>

AIKEN questions

Digital Sample = (Analog Input x 4095) / max analog value.

A) TRUE

B) FALSE

ANSWER: A

Which of the following register is used to read the ADC0 result?

A) ADC0_SS PRI_R

B) ADC0_SSMUX3_R

C) ADC0_SSCTL3_R

D) ADC0_SS FIFO3

ANSWER: D

Which of the following is not one of the four limitations exist when sampling data?

- A) Amplitude resolution
- B) Amplitude range
- C) Time quantization
- D) ADC pins number

ANSWER: D

Which of the following enables sample sequencer 1?

- A) `ADC0_ACTSS_R |= 0x0008;`
- B) `ADC0_ACTSS_R |= 0x0004;`
- C) `ADC0_ACTSS_R |= 0x0002;`
- D) `ADC0_ACTSS_R |= 0x0001;`

ANSWER: C

Which of the following enables alternate function on PE3?

- A) `GPIO_PORTE_AMSEL_R |= 0x08;`
- B) `GPIO_PORTE_AFSEL_R |= ~0x08;`
- C) `GPIO_PORTE_AMSEL_R |= 0xF7;`
- D) `GPIO_PORTE_AFSEL_R |= ~0xF7;`

ANSWER: D

When using "switch" in C, we put "break;" after each case so the program go into the next case.

A) TRUE

B) FALSE

ANSWER: B

ADC0_PC_R register is used to specify the sampling rate.

A) TRUE

B) FALSE

ANSWER: A