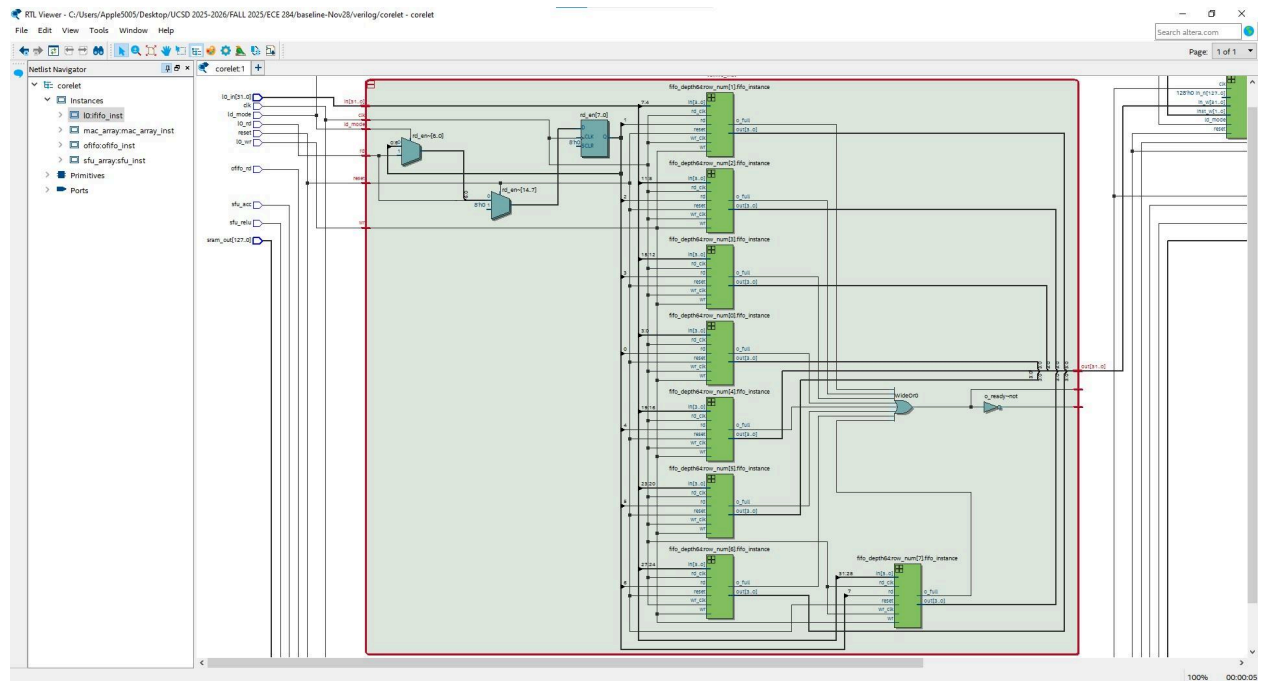
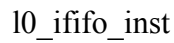
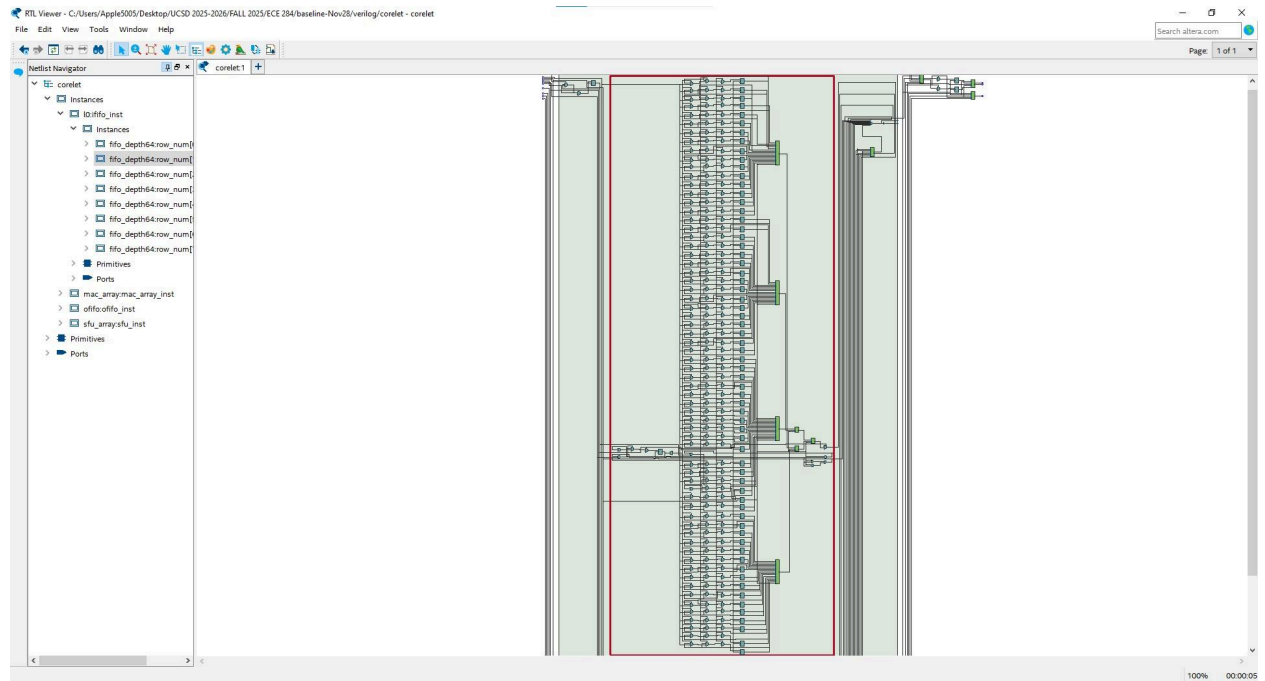


<b>Metric</b>	<b>Measured Result</b>
I/O Pins	427
Combinational ALUTs	12,391
Dedicated Logic Registers (Total Regs)	12,276
Number of Regs Using Synchronous Clear	1,269
Number of Regs using Synchronous Load	192
Number Regs using Clock Enable	11,817
Total Logic Elements	17,416
Slow 1200mv 100C Model Fmax	146.69 MHz
Slow 1200mV -40C Model Fmax	168.21 MHz
Worst Case Slack	-5.817
Total Thermal Power Dissipation	338.69 mW
Core Dynamic Thermal Power Dissipation	43.27 mW
Core Static Thermal Power Dissipation	119.59 mW
I/O Thermal Power Dissipation	175.82 mW

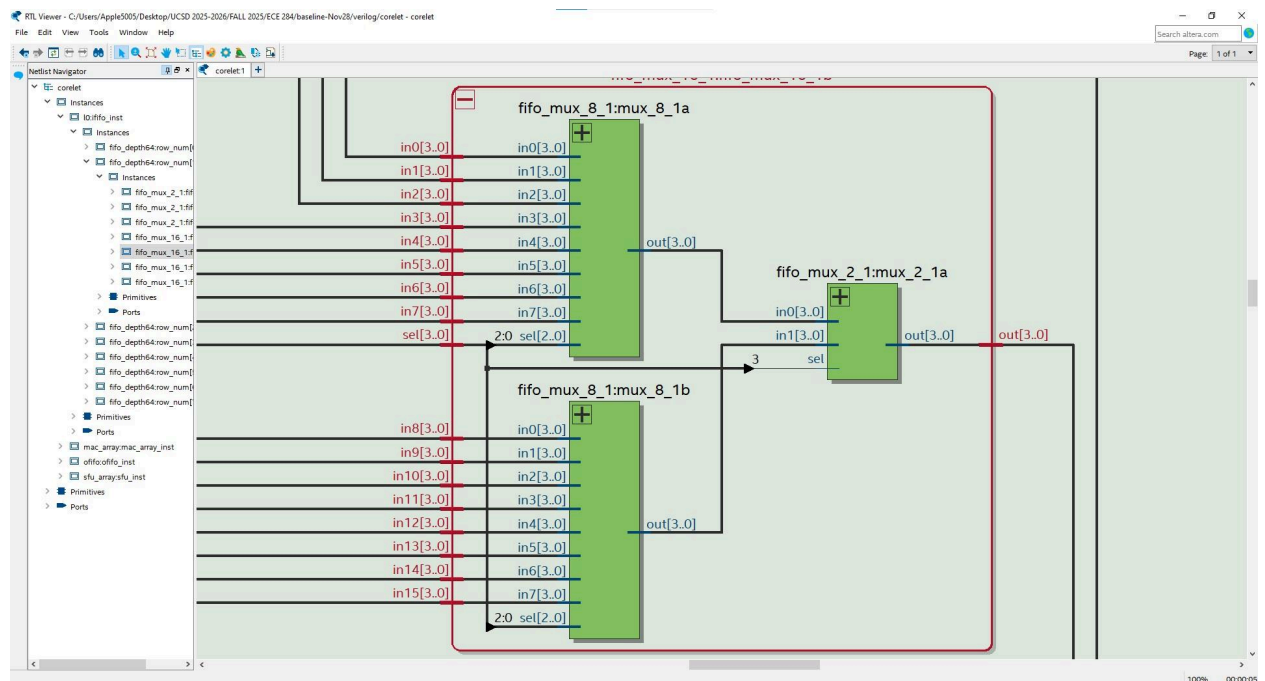
RTL Viewer - C:\Users\Apple5005\Desktop\UCSD 2025-2026\FALL 2025\ECE 284\baseline-Nov28\verilog\corelet - corelet



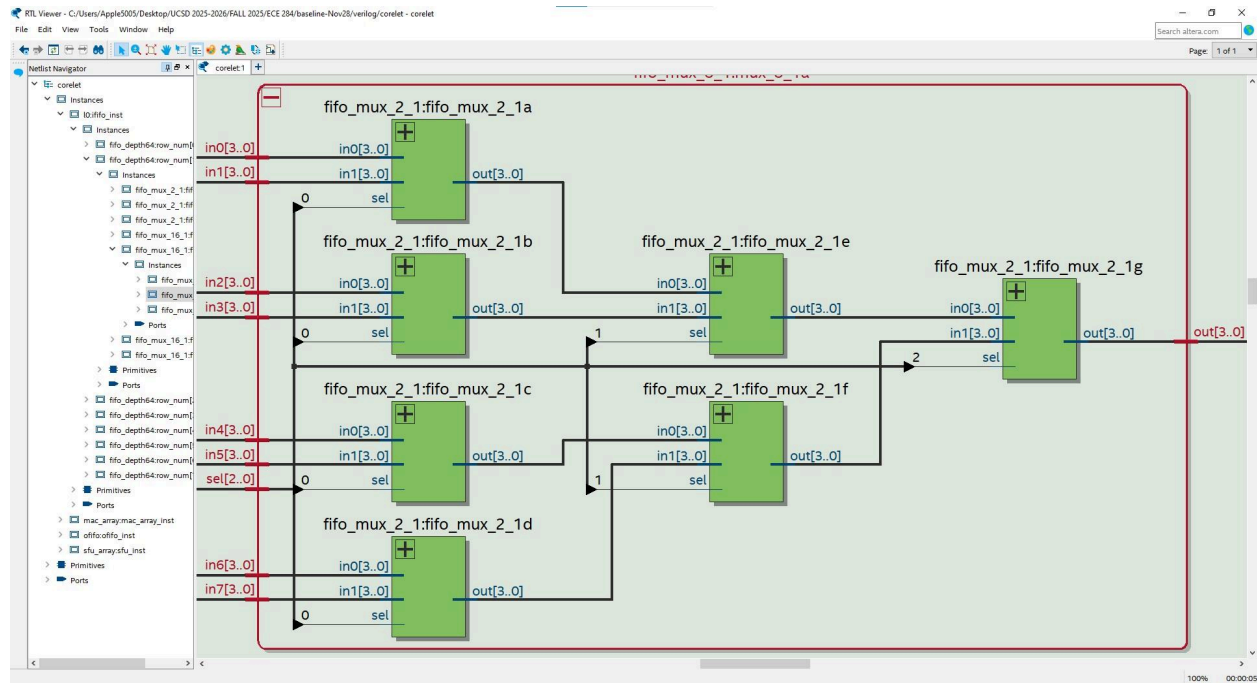
## fifo\_depth\_64



## fifo\_mux\_16



## fifomux\_8



## fifo\_mux\_2



ofifo

