American International University – Bangladesh

Faculty of Engineering – Electrical & Electronics Engineering

Make sure to add the following table and questions with your assignment as your cover page.

Course Name :	Microprocessor and Embedded Systems	**Course Code:**	EEE 4103
Semester :	Fall 24-25	**Section:**	M

Assignment No :	1 **(individual submission consisting of 30 marks)**

Student Name:	MD Abdul Aziz	**Student ID:**	22-47013-1

Submission Date:	30-01-2025	**Submission deadline:**	**Day of final exam.**
Submission link: https://forms.office.com/r/TriiTgFhdC			

Answer all questions given below, each question contains 3 marks

1) Design a n-bit Adder/ Subtractor circuit, where collect the value from your ID , consider ID is XX-XXXXn-X.

2) If your ID is XX-XXABC-X, then explain the working principle of bus organization where the number of registers is Y=A+B+C in a micro-operation R1=R2-R0+5.

3) Now, based on question number 2, design and explain the working process of scratchpad memory and a two-port memory system.

4) Explain the process of control logic design including all steps for a signed addition function only.

5) Explain the process of control logic design including all steps for a signed subtraction function only.

6) Deduce a flowchart and microinstruction table for counting the number of 1's in register R_A and storing the count in register R_B. Include the values of A and B from your ID if it is XX-XXXXAB-X.

7) Deduce a flowchart and microinstruction table for counting the number of 0's in register R_A and storing the count in register R_B. Include the values of A and B from your ID if it is XX-XXXXAB-X.

American International University – Bangladesh

Faculty of Engineering – Electrical & Electronics Engineering

8) For the processor unit with 16-bit control word variable as in table below, deduce the control words (using table from question no 10) for the following listed micro-operations:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A			B			D			F			Cin	H		

i) R2←SHL (R3 OR R6)

ii) R4←1

iii) R3+$\overline{R5}$ +1

iv) R4←input

v) R4 ←CLC R2

9) Design a 4-bit shifter from the given table of question number of 10.

10) Design a 4-bit ALU using table below [consider A & B as ALU source selection, F as the ALU function selection, D as the destination selection and H as shift operation selection variables]

Binary Code	Function of selection variables					
	B	A	F with C_{in} = 0	F with C_{in} = 1	D	H
0 0 0	Input Data	Input Data	A-1	A	None	-
0 0 1	R1	R1	A-B-1	A-B	R1	No shift
0 1 0	R2	R2	A+B	A+B+1	R2	Circulate-Right with Carry
0 1 1	R3	R3	A	A +1	R3	0's to the output Bus
1 0 0	R4	R4	A'	A'	R4	Shift Right with I_R=0
1 0 1	R5	R5	A XOR B	A XOR B	R5	Shift Left with I_L=0
1 1 0	R6	R6	A ∪ B	A ∪ B	R6	Circulate-Left with Carry
	R7	R7	A ∩ B	A ∩ B	R7	1's to the output Bus