ECE 385

Fall 2023

Experiment 1

Introductory Experiment

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Friday 2:45 pm

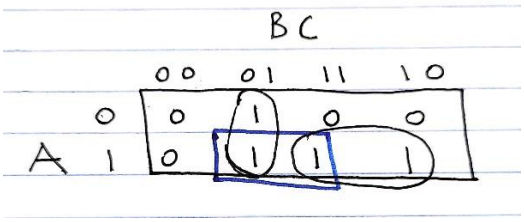
NY

Introduction:

This lab introduces the testing of TTL Chips and how to identify a static hazard (glitch) in a circuit involving SOP K-maps. The goal of this lab is to understand static hazards and how to avoid them when constructing a circuit. Two circuits were constructed and then compared with their outputs to see how the glitch is fixed by adding the additional terms from the K-maps back into the circuit logic.

Description:

Circuit A is designed to be a 2:1 multiplexer which is a device to allow multiple input signals to share one device which allows for Boolean functions to be implemented. The circuit is formed by having 4 NAND Gates which have input A and B into 1 gate followed by having B into its own to invert the input and connect that output to another NAND gate with input C. These two outputs from the NANDs are connected to another NAND to get the input for Z. B is the selector input which means when B is high indicating a value of 1 the input from A is selected and when B is low the input from C is selected. After passing through either A or C the last NAND determines which input to take making this a 2:1 MUX. The second circuit B fixes the issue of a Static 1 Hazard which is caused by the propagation delay in the Logic Gates which causes an output of a 1 to be 0 momentarily when the selector signal is switched. This is fixed in circuit B by looking at the SOP of the K map and adding back the missing group in the Boolean function which in this case is AC. This means adding 3 other NAND gates to account for the extra term. Which inputs A and C are going through their own NAND gate and then go through another NAND with the input of the previous NAND gate to get the output of Z. This doesn't change the truth table of A at all and just adding the extra term serves as the same function but will remove the static hazard caused from the missing minterm.

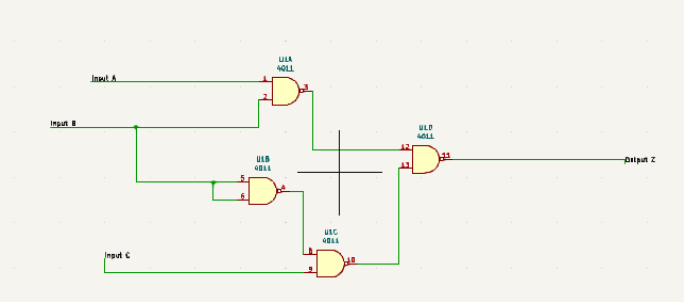


K-Map: 2:1 Multiplexer (Extra Term Marked in Blue)

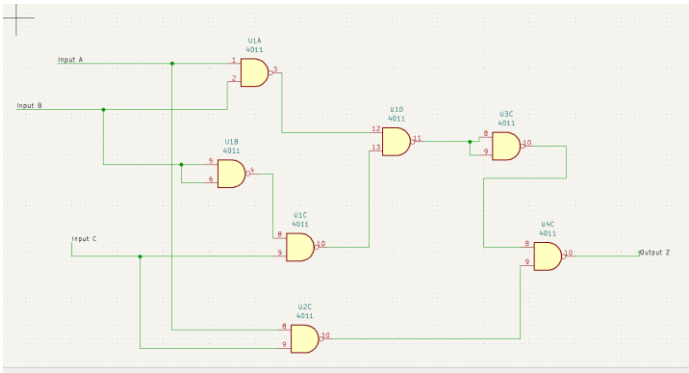
Boolean Equations:

Z = BA + B`C (With Glitch)

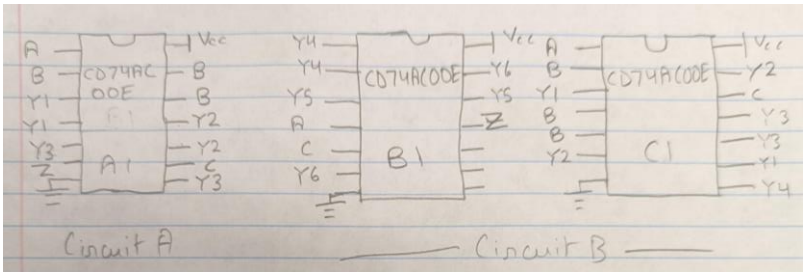
Z = BA + B`C + AC (Without Glitch by Adding in Extra Term)



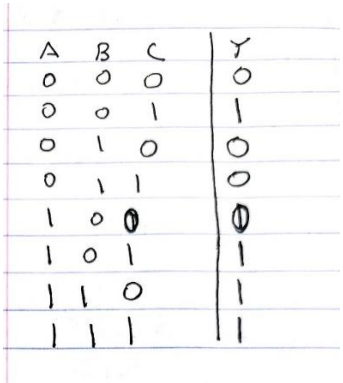
Circuit A Logic Gate Schematic



Circuit B Logic Gate Schematic



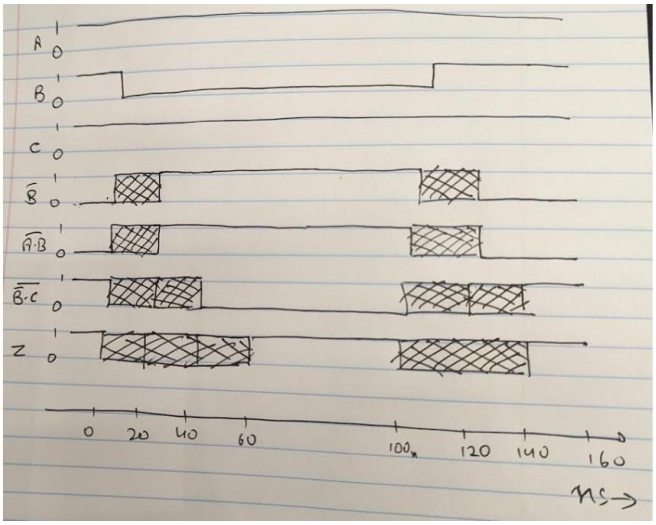
Component Layout



Circuit A Truth Table (~BC+AB)

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

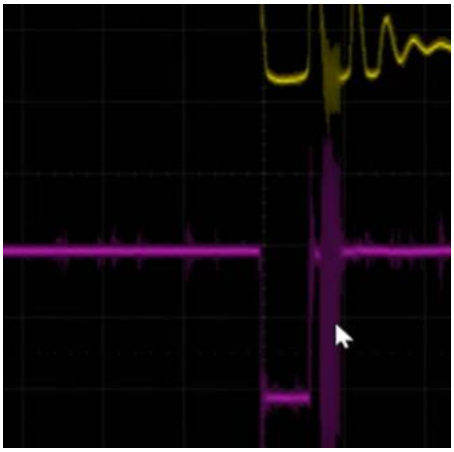
Circuit B Truth Table (~BC+AB+AC)



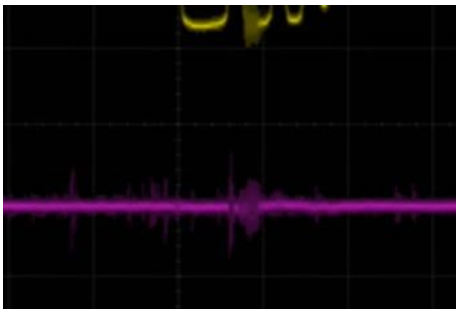
Timing Diagram for Circuit A

Pre Lab Questions/Answers:

1) Some groups may not experience a static 1 hazard because it occurs extremely fast and may be hard to identify at first because the noise from the circuit itself, but adding a capacitor can act as a delay and help show the propgation delay from the inverter more clearly to view in an osiliscope. While the capacitor charges the time it takes for the voltage to rise acts as a delay which helps show how the inverter in circuit A is causing a static 1 hazard.



Glitch from Circuit A because of propagation delay from the inverter.



Glitched removed when adding minterm Circuit B

The static 1 hazard has been resolved by adding in the additional minterm in circuit B because the hazard is caused by how the 1s are grouped and adding more Boolean logic will not affect the overall function of the circuit but resolve the glitch.

Post Lab Questions/Answers:

1) It will take 60ns for Z to stabilize on the falling edge of B and on the rising edge 40 ns.
2) The de-bouncer circuit with the two pull up resistors helps to stop contact bounces between the switches by making sure when the switch inputs are turned on and off the logic value is either pulled to 1 to 0 from the opposite end and not ground to avoid any contact between each other. When the switch is changed the contacts momentarily are separated which creates a contact bounce, but the use of a pull up resistor brings the input to a logical value debouncing the switch.

General Guide Questions:

1) The advantages of larger noise immunity prevent the action of spurious gate switching from low input to high.

2) The last inverter is observed because it will stop for random situations and when connected in series the output can sense a change from low to high.
3) To find the overall nose immunity taking the average of the lowest X and Y values for each input from the inverter would give the noise immunity.
4) Sharing resistors between LED is bad practice because the TTL base chips may be forced to supply more current than they can support.
5) The purpose of keeping a capacitor close to each chip avoids noise to keep the performance effective and to stop it from transmitting noise to other components in the circuit.
6) When a CMOS circuit switches it affects the activity power and toggles from high to low.

Conclusion:

The purpose of this lab was to understand the concept of a static 1 hazard and how certain circuit components have delays which need to be accounted for and how these glitches have solutions to avoid these problems. When dealing with inverters in any circuit delays and glitches must be tested and checked throughout because of static hazards and propagation delay due to missing Boolean logic gates. When adding the additional minterms for an SOP function the glitch was removed because then the additional term was accounted for and the glitch which was observed was removed. Understanding the difference noise and propagation delay was also observed and how noise can be confused for this. Noise can affect the performance of components but adding capacitors to a circuit can reduce this noise and protect other components. A possible remedy could be reducing the time of the clock and lowering it down to account for the delay. Overall, this lab introduced the concepts of static hazards, noise, and delays in components and various solutions and methods to test for these and find out where these occur in a circuit.