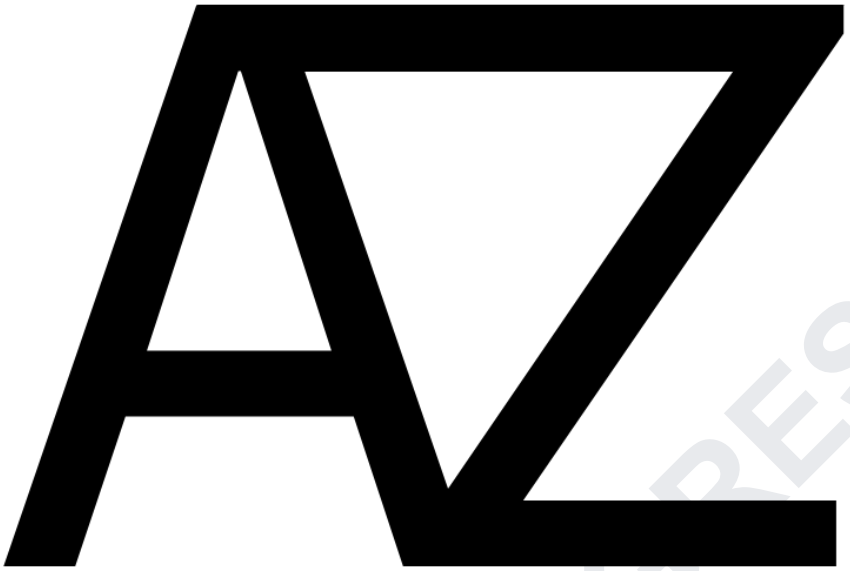

SensorSuite ToF+ v0.08

(Preliminary) Design Review 0001 - Version 2

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The AZ SensorSuite is a range of Bluetooth compatible portable ultra-low-power sensors.

This document details the design of the first sensor in the family. This document is intended as a learning tool for sensor development rather than as an integration manual for large-scale sensor implementation in commercial or industrial environments.

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YELLOW HIGHLIGHTED TEXT INDICATES THAT IT IS A PLACEHOLDER

TBD-
PCB REVIEW
CASE REVIEW
MANUFACTURE REVIEW
CODE REVIEW

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CHANGELOG

V0	Initial Commit- COVER, CHANGELOG, ABBREVIATIONS, INTRODUCTION	AZ	30/08/25
V1	ADDED SCHEMATIC REVIEW	AZ	01/09/25
V2	ADDED PCB REVIEW C1	AZ	14/09/25
V3	ADDED TAPR OHL LICENSE	AZ	28/09/25

ABBREVIATIONS

PCB - Printed Circuit Board
GCSE - General Certificate of Secondary Education
IR - Infra Red
LED - Light Emitting Diode
(Microchip) PIC - Programmable Interface Controller
FDM - Fusion Deposition Modelling
BLE - Bluetooth Low Energy
CE - Conformité Européenne
UKCA - UK Conformity Assessed
LASER - Light Amplification by The Stimulated Emission of Radiation
ToF - Time of Flight
PMMA - Polymethyl Methacrylate (Common name Acrylic)
I^2C - Inter Integrated Circuit
BOM - Bill of Materials
API - Application Programming Interface
IC - Integrated Circuit
RH - Relative Humidity
RTC - Real Time Clock
GPIO - General Purpose Input Output
µC - Microcontroller
SoC - System on Chip
(Nordic) OPP - Online Power Profiler
(Q)SPI - (Quad) Serial Peripheral Interface
USB - Universal Serial Bus
SMPS - Switching Mode Power Supply
SEPIC - Single Ended Primary Inductor Converter
EDA - Electronic Design Automation
ADC - Analog to Digital Converter
LGA - Land Grid Array
PTM - Push to Make
BGA - Ball Grid Array
(Inductor) DCR - Direct Current Resistance
PMOS - P Channel MOSFET
MOSFET - Metal Oxide Semiconductor Field Effect Transistor
TVS (Diode) - Transient Voltage Suppression
ESD - Electrostatic Discharge
V_RWM - Reverse Breakdown Voltage
VC - Clamping Voltage
EMC - Electromagnetic Compatibility
ENIG - Electroless Nickel Immersion Gold
MLCC - Multilayer ceramic capacitor
RPP - Reverse Polarity Protection
EMI - Electromagnetic Interference
PDN - Power Delivery Network
DMM - Digital Multimeter

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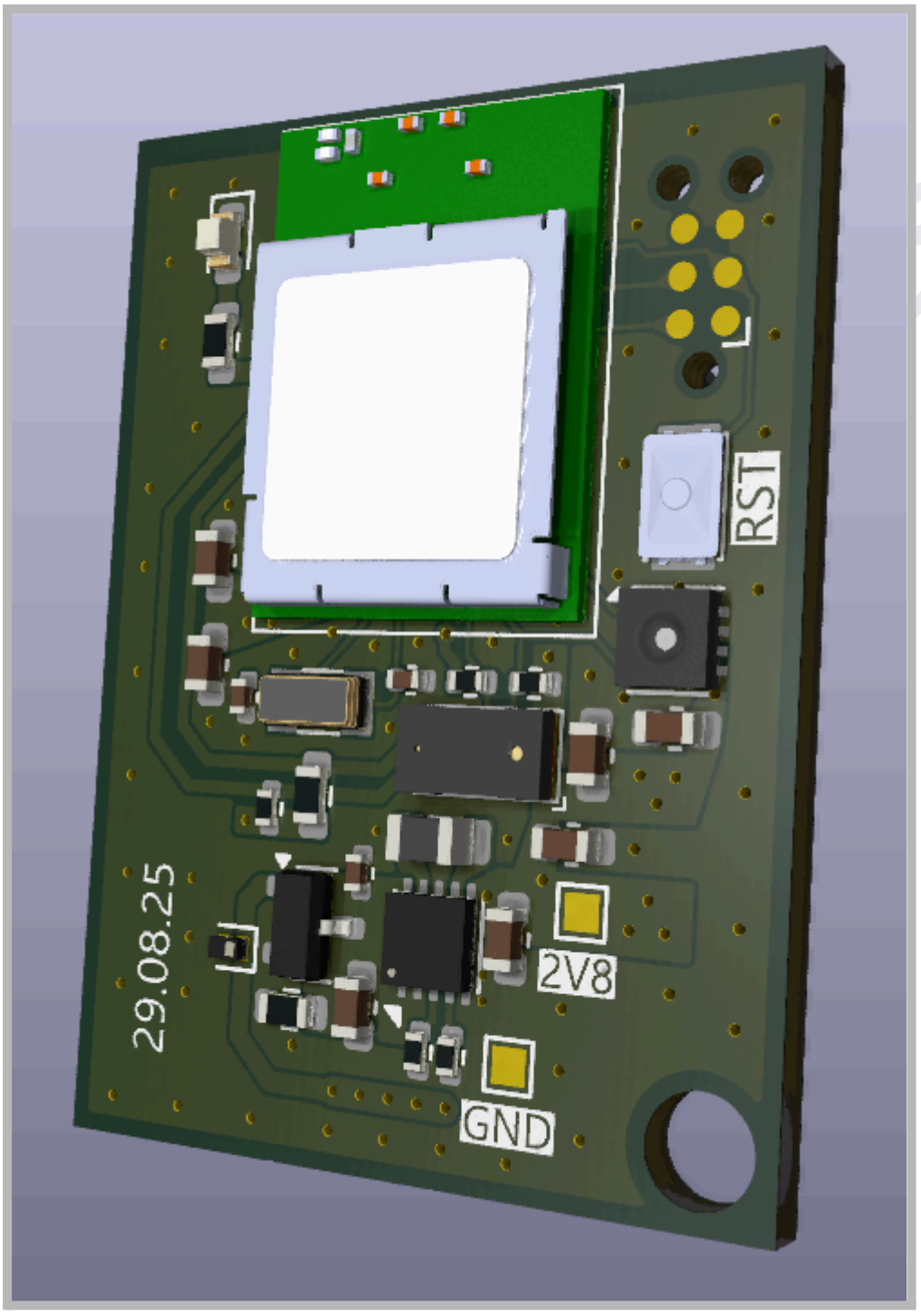
Introduction

This section features an overview into the context, initial planning and idea development that led towards the core foundation upon which the project was developed. The context is not vital to the rest of the document and may be skipped.



Render of V0.07 of the PCB

Context

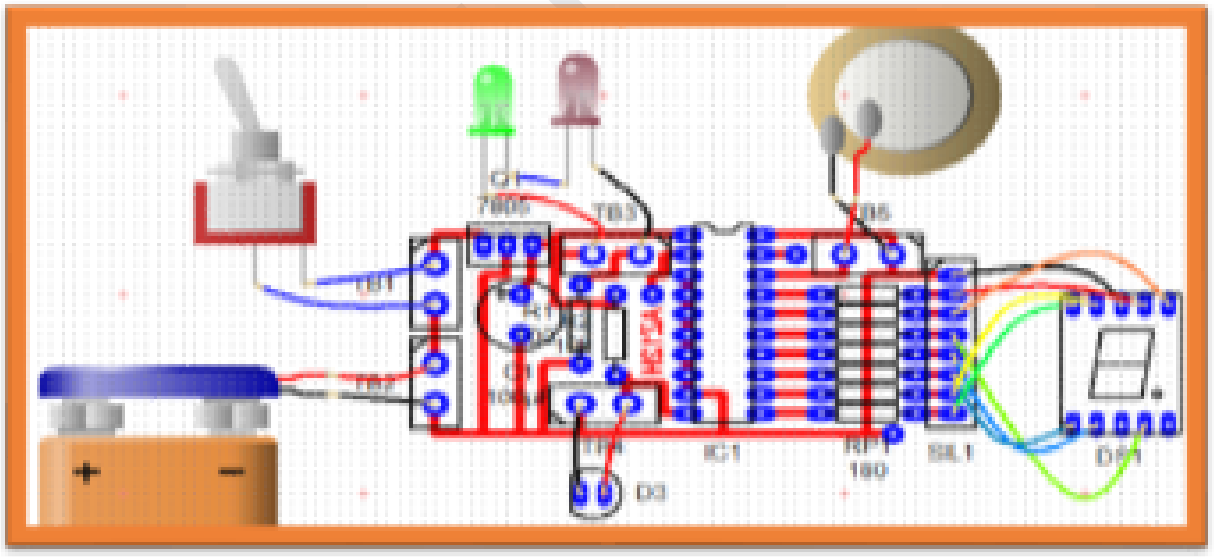
Many months/years before this project I was taking my GCSE in Technology and Design and was faced with the task of designing a product for my Continuous Assessment. The theme I chose was “Reducing Litter in Schools” and ultimately after not much thought I settled on the bin-object-counter idea. A fairly device that would detect objects falling into a bin and somehow convey the total amount of objects to the user.

Frankly, (even though it scored 39/40 points) it was terrible. It used an IR LED and IR photodiode to detect reflected light. This input would then go to a PIC µC without any processing which would then drive a seven-segment and a buzzer. This concoction was powered by a PP3 (commonly known as 9V) battery going into a L7805CV linear voltage regulator that was probably obsolete 10 years ago

Firstly, in my infinite wisdom I put the IR LED and power LED in series to save current. By some miracle of aliexpress tolerances their forward voltages exceeded 5V and the IR LED wasn’t lighting up fully decreasing the sensing range. By some grace of the gods the PIC accepted the noisy voltage input and the photodiode’s output and drove the seven-segment.

However, you may now start to see one of the main problems of the design. The ~55% efficiency of the linear regulator combined with around 120mA mean current draw to produce an abysmal battery life of 5 hours. A product designed to be used 24/7 for months on end where a single battery costs ~£2 and that was to be installed on every bin in a school. One could say it would “burn money”.

PROGRESS



Highest resolution image of the single layer PCB that I designed. The footprints for the terminal blocks ended up being too small anyway and I had to improvise.

Secondly, the casing was no better, an FDM 3D printed main body with acrylic panels stuck and screwed to it. During the assembly of the project several other problems arose. I think it is best if they are laid out in chronological order.

1) The seven-segment is glued in with a surrounding acrylic window.

2) The dupont connectors that were going to connect the seven-segment to the mainboard are loose and fall out with vibration.

3) An attempt is made to glue the connectors while the seven segment display is in the housing. It fails.

4) The housing is hit with a wooden mallet to remove the seven segment display. Understandably the plastic disintegrates.

5) The 3D printers in the school are set up horribly and it takes a week for a new case.

6) The buzzer is not secured to the case in the frantic race to finish the project in the now-twice-delayed deadline and is inaudible.

IN PROGRESS

You can imagine the nascent kindling of discontent for the design. When I finally finished that project, a yearn for a better version was born that is finally being satisfied. The untapped potential of object detection prompted me to diversify the project. Truthfully, during the design process of the bin sensor project I downloaded KiCAD for the first time and tried to make my own version, but the class had taught me nothing relevant so the idea died off.

Now, after lurking in r/printedcircuitboard and watching an unhealthy amount of lectures and seminars on youtube, I felt ready to design my improved “bin sensor”. The idea popped back into my head when I was sick on holiday in Barcelona (would not recommend), as aforementioned quite a lot of time had passed and my skills had quite substantially increased. Furthermore, a local competition was/is upcoming (I hope) and I wanted to present my updated bin sensor there and hopefully win a prize. This documentation is mainly being made as an effort to compete with the extensive design documents required for GCSE/GCE Continuous Assessment work which makes up a majority of entries.

As such I wanted to expand on the previous project and solve its problems. I was mainly concerned with tackling:

- The horrific battery life
- The lack of data available about the object detection
- The very large form factor
- The singular fixed mounting method
- The large amount of manual assembly

This and more will be discussed in detail in the remainder of this document.

Sincerely,
Adam Zembrzuski 30/08/2025

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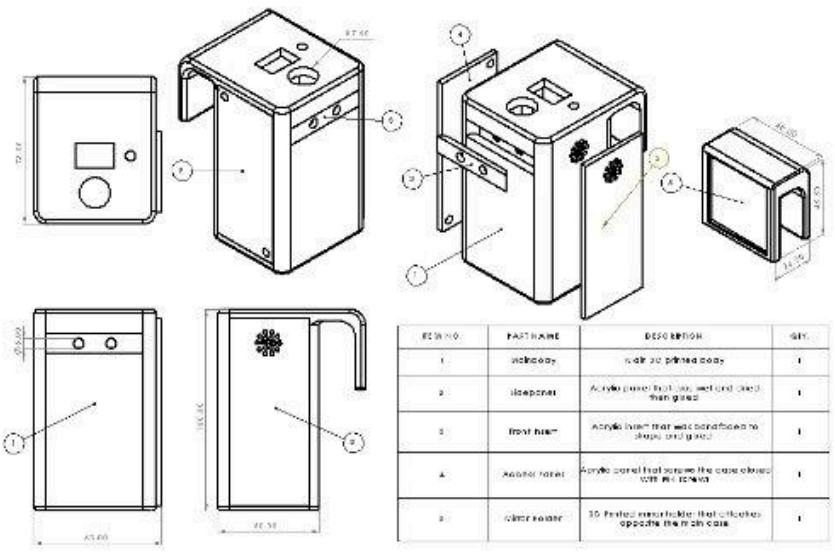

Design Intent and Specification

To create a portable, programmable sensor that can be controlled over BLE and can be deployed in permanent or remote locations. The sensor should output a rich dataset that can be analysed by the end-user to optimise user-specific problems. Such as optimal bin placement or flow control through pathways. The project's digital interface will be customisable to facilitate custom use cases through a scripting language.

In essence, a competent version of the Bin Sensor.

ELECTRICAL SPECIFICATION

- Minimum of 1000 hours of active operation with periodic 1Hz measurements on a single battery/charge.
- Responsive BLE interface with less than 100ms of delay
- Minimum 1 metre of detection length in all conditions
- Minimum Bluetooth range of 20m
- Each datapoint should be timestamped with relative time from initialisation
- 95% of pads on one side of PCB
- At least one fault indication output
- 100% Lead Free
- CE and UKCA Conformity

MECHANICAL SPECIFICATION

- Secure case and mounting methods that deter casual criminals from theft
- Resistance to light rainfall less than 2mm hr^{-1}
- Drop resistance to 1 metre
- Less than four screws required for assembly
- Smaller than 60x60x20mm
- Cost per kilounit of assembled project below £20000
- Single unit setup in 5 minutes

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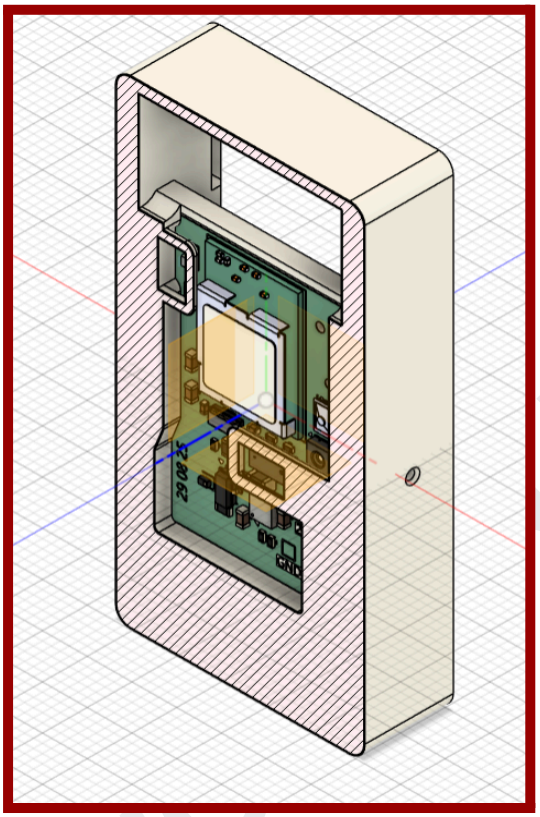
Design Review

Each subsection of the design review will feature decisions split by “class”, decision classes are summarised in the table below.

CLASS NUMBER	IMPORTANCE	EXAMPLE
Class 1	High Importance	Core design choices or part selection
Class 2	Medium Importance	Ease of life or functional improvements
Class 3	Low Importance	Aesthetic or minor adjustments

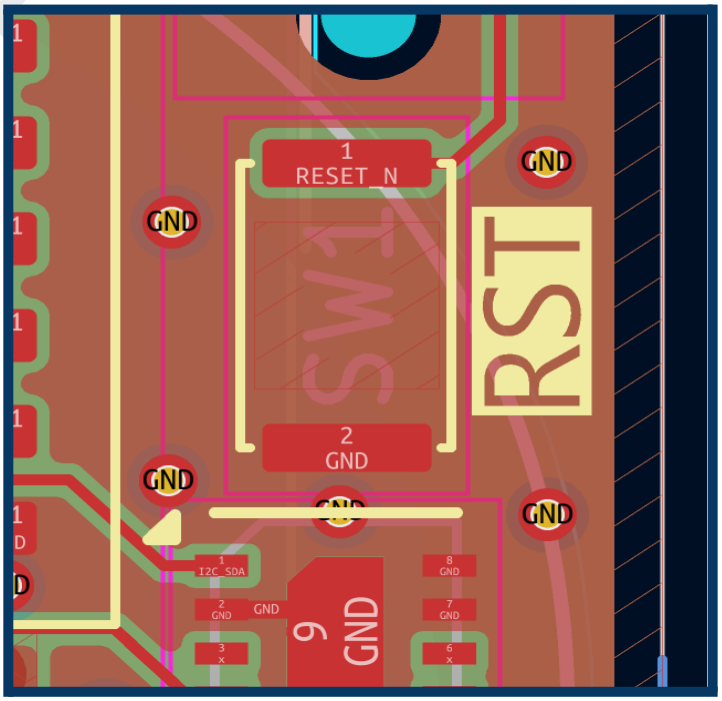


Class 3 Decision - Silkscreen sizing

Explanation - The silkscreen does not affect the rest of the PCB and does not take priority to any other design-related tasks. It can be done last.

Class 1 Decision - PCB location in case

Explanation - The strength of the antenna is highly dependent on its surroundings. The case has to be designed around the air gap necessary for the antenna. Adding the air gap later will add unnecessary work and require restructuring.



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Schematic Review

This section contains the class-based review of the relevant schematic and design choices. A full page printed schematic is available at the end of this section.

CLASS 1

SENSOR SELECTION

The object detection sensor cannot work without an object-detecting sensor. This is why it is at the top of the priority list for the design. An appropriate sensor had to be chosen that would be easy to integrate, very low current and be reasonably cheap. At a first glance, I eliminated IR beams due to their high current. The first option that I considered was the VL53L1X from STMicroelectronics (who will from now on referred to as “ST”).

Image of VL53L1X sensor
Source: ST Microelectronics

This is a state-of-the-art Laser ToF ranging sensor that operates on a single 2V8 input voltage and has a range of up to 4m in long range mode. The minimum ranging distance was also only 1mm with a cost of £2.73 per unit when buying a full reel. So far it ticks all of the specification boxes. It can also be placed behind a transparent PMMA “cover glass” (commonly known as acrylic) to stop water entering the case. So far it ticks all the boxes.

However, if we scroll down to section 6.4 of the datasheet, “Electrical Characteristics” we see a problem. 0.9 to 1.4 mW mean operating power at 1Hz with a 20ms timing budget. This may not seem terrible but it equates to ~500µA. If we assume a battery with 300mAh for simplicity, the sensor alone would run the battery out in 600 hours without any other circuitry. Clearly, this is too much for the 1000 hours of operating time that the product needs. So, I looked to alternatives.

Firstly, I looked at the TDK CH101. This is an ultrasonic ToF sensor that has a much lower power draw than the VL53L1X. It consumes only 15µA at 1Hz with a 1V8 power input. It also features a customisable FoV up to 180° and a range of up to 1.2 metres. It also only requires a single decoupling capacitor and communicates over I^2C. That is where the positives end. Since it uses ultrasound waves it cannot be covered with a cover material meaning that it would be susceptible to liquid damage from outside.

WORK IN PROGRESS

Furthermore, it requires a plastic “horn” to be fitted onto it to direct the ultrasonic waves which would add to the PCB’s thickness and increase the BOM count. It also requires the use of a proprietary firmware that would increase the software implementation time exponentially. Ultimately, I decided that the wonderful specs on paper were not worth the hassle of integrating it into my design and I continued searching.

Having exhausted my list of usual forums and youtube channels, I turned to ChatGPT to recommend some sensors that I might have overlooked. It was then that I was enlightened about the existence of the VL53L4CD by ST that is very similar to the VL53L1X but has an ultra-low-power firmware that consumes only 55µA at a 2V8 supply. Much more manageable with the current dropping to only 9µA in standby mode. The other specs remained similar, with a 1.2 metre range, single 2V8 supply, I^2C interface and a cost of £1.78 per unit when buying a full reel. It is also pin compatible with the VL53 family of sensors meaning a higher power version can be soldered at any time (with a firmware correction).

The VL53L4CD (and VL53L1X for that matter) are programmed by a C-based API provided by ST. This will allow for the controller to get data from the I^2C interface and allow initial calibration as per ST AN5870 and UM2931. This will allow for a very large range of controllers to be used as the API is in standard C and as I^2C is a very common protocol on embedded ICs.

Next, I wanted to add another sensor to improve the value of the dataset being produced, for this reason I wanted to add a temperature/humidity sensor. Honestly, this thought came to me at the end of the PCB design phase when I realised that there was a redundant 1206 resistor on the board. Removing it made enough space for another sensor IC.

Render of SHT30 sensor
Source: Sensirion AG

Initially, I wanted to use the SHTC3 by Sensirion AG due to its tiny footprint and ease of implementation, (I^2C and power was all that it needed) however the footprint did not align with my preexisting PCB layout and I did not want to increase the capacitance on the I^2C bus by adding unnecessary vias (see pg22). For this reason I pivoted to an extremely similar sensor called the SHT30 (also by Sensirion). However with the I^2C pins in different locations so that they fit my PCB layout without vias. The SHT30 has ±2% RH accuracy across 10 to 90% RH and 0.2°C temperature accuracy.

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CONTROL SYSTEM

Let's look at the specification for a second, the main points that pertain to the control system are - low power, long range Bluetooth communication and an RTC for timekeeping. We must also have a 400KHz capable I^2C interface and at least 2 free GPIO pins for a minimal application. In reality we want at least 10 available GPIO pins in case of future expansion and/or debugging. It would also be preferable to power both the sensor and controller with a single voltage, thus we should look for 2V8 capability.

The first question is how do we plan on doing Bluetooth and achieving an RTC. We can either use separate ICs (µC, BLE transmitter and receiver, RTC) or we can attempt to find a single IC that combines all of these. This IC concept is called a system on chip (SoC) and they are fairly available for common use cases such as portable bluetooth devices so I was able to settle on one fairly quickly.

It was the Nordic NRF54LXX. The two Xs can be either 05,10 or 15 and pertain to the amount of flash memory and RAM that the SoC has. Otherwise they are identical (pin-compatible and all). This SoC is very low power and using Nordic's OPP for BLE an estimate of 10µA mean current when connected and 30µA when advertising is calculated. The NRF54L15 also incorporates a 2.4GHz radio suitable for BLE 6.0 and an RTC that can wake the SoC on demand (given that the appropriate crystal is connected). It also features many interfaces such as I^2C, SPI, QSPI, USB and many others. As well as having a maximum of 32 GPIO pins.

Image of NRF54L15 in QFN48 (6x6mm) package
Source: Nordic Semiconductor

WORK IN PROGRESS

However, the bare SoC does not feature an antenna. This is a problem as creating and tuning an antenna could take months of work and would require certifying the product as an "intentional radiator" which would dramatically increase costs of certification. For this reason, I decided to use a pre-certified module designed with the NRF54L15 and a pretuned PCB antenna. As of the time of development the only module available in stock (due to the newness of the NRF54L15) was the U-Blox Nora B206. It featured a tricky footprint that will be discussed in the PCB review but other than that it was fairly solid. There was also a version with a U.FL connector for external antennas, however I decided against it as I would be limited to a small range of antennas certified with the module and they would all be much larger than the PCB antenna.

POWER SUPPLY

Ultimately, I had two main power supply options for this project due to the necessary portability and the 2V8 supply. Either, a rechargeable or single-use battery. Lithium polymer and lithium ion rechargeable batteries have become so widespread that their application in hobby-grade projects has become very straightforward. With a Li-Ion battery, a charging IC and a protection IC you already have almost the full implementation. The battery can then be connected by some sort of standard connector (usually JST or molex) et voila, the battery supplies your project.

However, this volatility that allows charging is also a downside, as Li-Ion batteries must be sourced locally as international shipping can be very dangerous due to Li-Ion batteries having the ability to spontaneously combust. This only applies to standard vendors, some sites like AliExpress do offer cheap, Chinese Li-Ion batteries however there is no guarantee of quality.

The idea to use a single-use battery didn't appear in my head until almost halfway into the project, (at which point I had to redesign all of the power circuitry) as I skipped past single-use batteries as they had similar energy density to Li-Ions and could not be recharged. However, as I was researching other ultra low power devices I saw that most if not all were using some sort of button cell. I questioned myself as to why this was.

I found three main reasons:

1) Single-use batteries are much less volatile than rechargeable batteries and so more easily purchasable.

2) Single-use batteries do not require charging, which takes a lot longer than a simple battery replacement , and necessitates charging circuitry.

3) I could use dedicated coin cell holders soldered onto the PCB to reduce the overall thickness of the product.

Image of CR2032 coin cell used in a computer motherboard
Source Unknown

WORK IN PROGRESS

However, as with anything in life, there were compromises; the operating voltage range of a 3V nominal CR2032 coin cell is 3V2 to 2V. This range falls above and below the 2V8 system voltage so a more complex voltage regulation arrangement had to be used.

Fig. 1 shows the continuous discharge characteristics of an Energizer CR2032 battery. Notice how the voltage is above 2V8 for most of the lifecycle and then falls below for approximately the last quarter.

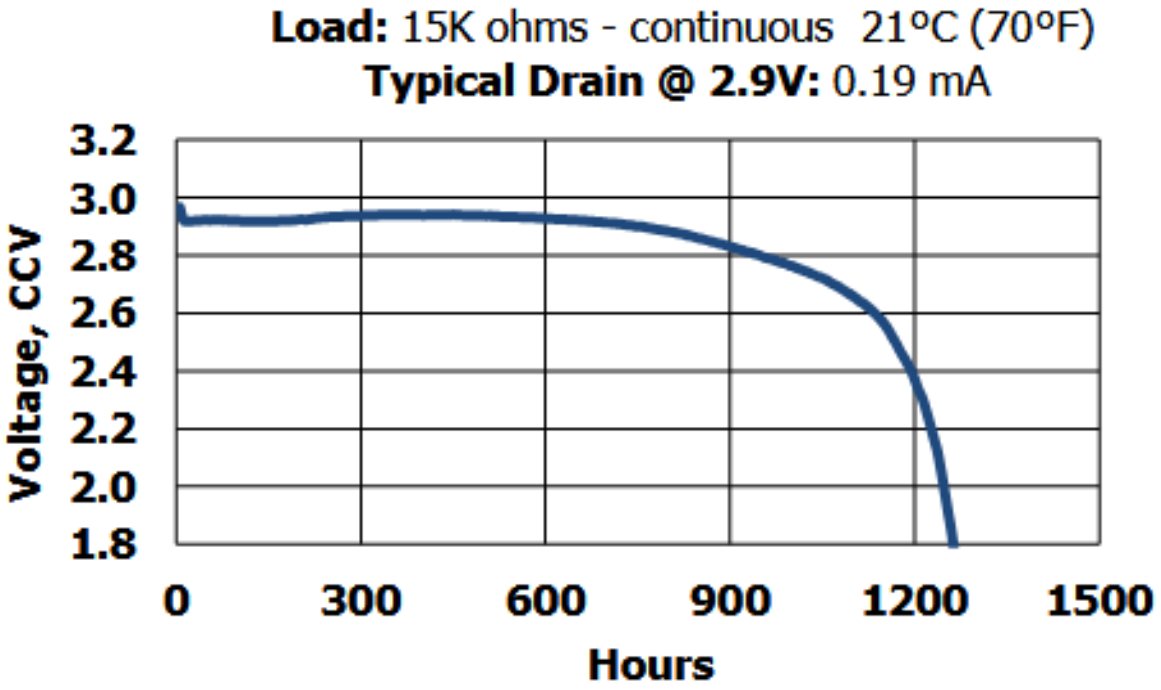


Figure 1
Source: Energizer

Furthermore, many small coin-cell holders allow the battery to be inserted upside down due to the coin-cell's approximate symmetry. This would apply a reverse voltage to the circuit and destroy most if not all of the components. It is safe to say that that would be a common catastrophe if an uneducated user was using the project. For this reason I needed reverse polarity protection and other protections that are detailed in the power design subsection of Class 2.

As for regulation, clearly we can see above that simply regulating the battery voltage down would leave around 300 hours of unused battery life, as the regulator could not operate when the voltage fell below 2V8, (V(900) ≈ 2.8). Thus the design required an IC to step voltages both down and up as required. The SMPS topology that I decided to use was buck-boost. This is due to the fact that it requires very little supporting circuitry relative to something like a SEPIC topology supply. My buck boost design only required a single inductor as opposed to two in a SEPIC supply. More information on IC selection is in the power design subsection of Class 2.

CLASS 2

NORA B206 INTEGRATION

Integrating the Nora B206 was one of the first tasks that I completed in this project as it was a simple case of drawing some symbols and footprints, and adding some simple external components. As my EDA tool did not have a symbol for the fairly new Nora B2 module family, I had to draw my own symbol. I placed all of the GPIO pins without alternate peripheral assignments *(not including ADC inputs)* on the left side of the symbol, and all of the pins with alternate peripherals on the right side. As per usual power pins were on the top and ground pins on the bottom. This allowed me to maintain a clean and very legible schematic.

The footprint for the Nora B206 was the first LGA footprint that I had ever made, so it took me a bit of time to figure out the grid snap controls and pad sizing. I also had to implement the keep out zone for the antenna to keep as much of its performance as possible. More info on the design of the antenna surroundings is in the PCB review section. After an initial struggle and an hour or two of staring at the datasheet the footprint was finished.

Following that, I could move on to placing the passive components for operation and some additional debugging components. Firstly, the decoupling capacitors C5 and C6 were added as per the suggestion of the Nora B206 datasheet. I aimed for at least 10V, X7R capacitors throughout the whole project to reduce DC bias and maintain a roughly constant capacitance across a large temperature range.

Furthermore, for accurate RTC operation I decided to add an external 32.768KHz crystal that would provide the clock for the RTC system. I picked the SC32S-7PF20PPM manufactured by Seiko Instruments as it has a low load capacitance that slightly reduces the overall power consumption, low tolerance of 20PPM and comes in a small package. The load capacitors had to be calculated by the formula $C_L = (C_1 * C_2)/(C_1 + C_2) + C_{Stray}$ which simplified to $14 - 2C_{stray} = C$. C_{Stray} was measured physically to be xpF and the final load capacitors were xpF.

For programming and general debugging, I opted to add a Tag Connect TC2030NL programming header that would connect to the debug output of the Nordic NRF54L15 Development Kit. This would allow me to use the Segger J-Link OB to debug the SoC without having to solder any wires or use permanent connectors. Mass programming also becomes much faster as the TC2030 uses pogo pins to connect to the target. I also added a PTM button to enable the user to reset the system as there is no power switch.

Finally, I added a low current LED that will turn on when a fault is detected to notify the user of a problem, prompting a system reset. The fault will also be broadcast in the bluetooth communications. The LED will also be used during development for various development purposes such as checking that processes are working. The LED output is also connected to a test pad; the GPIO's output will actually be data sent at 10KHz so that it is legible by human inspection on an oscilloscope or similar without affecting visibility.

WORK IN PROGRESS

SENSOR INTEGRATION

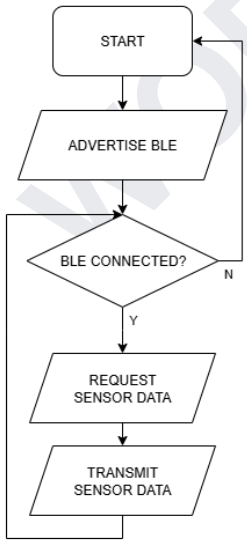
Continuing from the last section, here I will discuss the integration of the selected sensor (VL53L4CD and SHT31) and the I²C bus. Both sensors accept 2V8 as their operating voltage so they are both powered from the main power supply. This “engineered simplicity” of having a single power supply greatly cleans the schematic and will help with the PCB routing. As per before, both sensors require minimal decoupling capacitors, a 4.7µF and 0.1µF for the VL53L4CD and a 0.1µF for the SHT31.

As for specifics, the VL53L4CD features the pins “GPIO1” and “XSHUT” which are used for power saving in the SoC. Namely, GPIO1 goes low to alert the SoC when data is ready to be read, which wakes the SoC and initiates many I²C reads via the api. Whereas, XSHUT is driven by the SoC and can put the VL53L4CD in or out of standby mode by driving the pin low or high respectively. Both GPIO1 and XSHUT must be driven at all times for proper operation, so 1M pull up resistors are used to keep the signal high when possible.

1M pull up resistors are used as a compromise between pull up strength and current draw; as smaller resistors would have more noise immunity and allow faster rise times (due to the parasitic capacitance an RC delay is formed), however they would take more current. The two 1M resistors draw a constant 3.4µA which helps to lengthen the battery life. These large resistances are starting to push at the edge of usable noise however due to the low speed nature of the signals and with some careful PCB design we can ensure stable operation.

Similarly, the SHT31 features two additional pins, NRESET and ALERT. As the name suggests NRESET is an active low reset. There is an internal pull up resistor so it can be left floating. ALERT can be configured to send an interrupt when a condition is achieved such as temperature surpassing a set point, this works similarly to the GPIO1 pin of the VL53L4CD however as the SHT31 will be used in one-shot mode this is irrelevant.

One-shot mode is the mode where a single measurement is taken and then the sensor goes back to sleep. Here is a very simplified flow diagram of the B206’s logic.



Importantly, upon requesting the data, the SoC goes into System Idle mode, and wakes up based on the GPIO1 pin going low on the VL53L4CD so as to not waste battery life. Furthermore, due to the long measurement time of the SHT31, the B206 requests readings on one cycle but then only sends them during a later cycle, as a humidity reading takes up to 8 seconds and a temperature reading takes up to 2 seconds.

The SHT31 readings should never take precedence over constant VL53L4CD readings so that the object detection is uninterrupted.

WORK IN PROGRESS

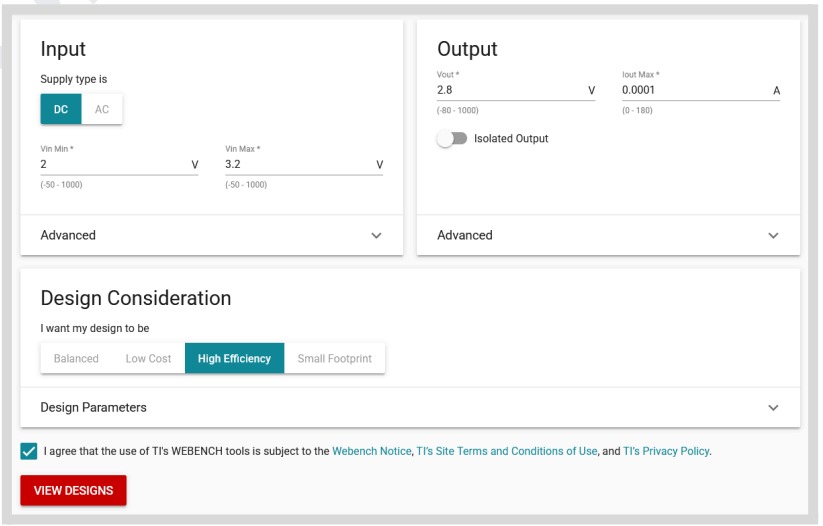
I also optimised the I²C pull up resistors similarly to what was required for the 32.768KHz crystal's load capacitors. Due to the high frequency of the I²C bus (100KHz to 1MHz), signal rise times become a very prominent matter when choosing pull-up resistor values. The parasitic/stray capacitances of the controller, pcb traces and each device add up to form an RC delay which delays the signal as the "capacitor" created by the stray capacitance (dis)charges. This meant that I had to measure the capacitance of the PCB and then use a calculator to calculate the maximum allowed resistors for my application. For a standard mode (100KHz), I²C signal, the rise time must be below 1000nS (1µS). This meant that for my 40pF of capacitance at 2V8 I could have up to 28K resistors.

However, this would prove unnecessary as after finishing the design of the PCB I realised that it would be more efficient to simply disconnect the pull-ups when the I²C bus was not in use. This would result in much lower mean current meaning more of the power budget could be dedicated to the ICs.

This meant that I would either 1) have to add mosfets as low side switches to disable the resistors when required (obviously connected to GPIO) or 2) use the NRF54L15's internal configurable pullups. I chose to use the NRF54L15's internal pullups as I did not want to add to the BOM and truthfully I did not have enough space on the PCB for even the smallest of SMD transistors and I did not want to do a PCB (and consequently) case redesign. Albeit, the internal pull ups on the NRF54L15 are only 13K meaning that power consumption could be reduced in a new revision.

POWER DESIGN

At the start of most of my power designs I navigate to Texas Instruments' WEBENCH online tool. WEBENCH is a very powerful tool that works by having you enter some key specs (Input voltage range, output voltage, load current etc.) and then presenting you with power solutions filtered by efficiency, cost, footprint area, etc. The image below is my whole input, which generated a list of suitable ICs. The TPS63900 was the most efficient non-BGA design which is mainly why I chose it. (I do not have BGA soldering capabilities)



WORK IN PROGRESS

By using the datasheet implementation of the IC, I was bypassing 80% of the research required to make an efficient power implementation. WEBENCH stated that ideally my design would work at 88.6% efficiency when boosting from 2V to 2V8 and at 92.6% in buck mode. This is helped by the fact that the TPS63900 boasts an insanely low 75nA quiescent current.

I measured peak inductor current on the PCB to select an inductor with the appropriate saturation current; however the project's production has seen delays as I am waiting for a confirmation of my Arkwright Scholarship in early September so that I can use the funds provided. As a placeholder I selected a low DCR inductor with saturation current similar to what is in the recommended inductors section of the datasheet. (AOTA-B201210S2R2MT)

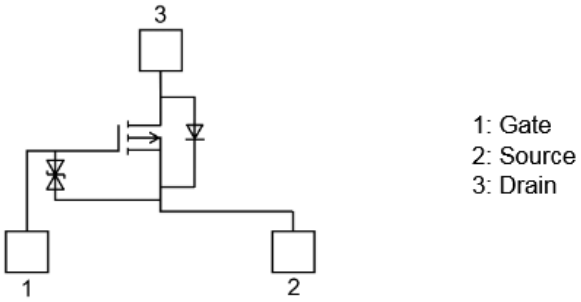
It was also necessary to use a 13.3K resistor to set the output voltage, and I added an optional 1.87K resistor to limit the input current to 25mA so as to not exceed the maximum pulse current capacity of the CR2032. The soft-start capability of the TPS63900 also helps to not surpass this peak current on initial battery connection.

Furthermore, the TPS63900 integrates output short-circuit and overtemperature protection, which greatly increases the safety of the device in the case of a fault. As aforementioned I also had to implement reverse voltage protection to protect against the battery being inserted upside down. The two approaches that I considered were, using a zener diode in series with the battery, using a P Channel MOSFET (PMOS). The zener diode approach is the simplest as it involves just a single part, however the diode has a voltage drop which would dissipate energy as heat. Additionally, the battery output voltage would be lower leading to lower buck-boost efficiency.

On the contrary, we can use a PMOS as a high side switch that operates with a very low resistance. The battery +ve is connected to the drain and the output is connected to the source, then the gate is connected to ground. I also placed an optional large resistor (4M7) between gate and source to prevent the gate from floating and disrupting operation.

The basis of using a PMOS as reverse voltage protection is this. A PMOS requires a negative voltage difference, V_{GS} to conduct. Otherwise the PMOS conducts through the body diode which is inefficient due to the voltage drop. However, when a +ve voltage is applied, the source becomes almost the drain voltage as current passes through the forward biased body diode, making V_{GS} lower (above the minimum threshold) and enhancing the PMOS so that it can conduct with its low resistance (RDS_{ON}).

WORK IN PROGRESS



Pin assignment of SSM3J338R
Source: Toshiba

If a -ve voltage is applied, only minimal leakage current can go through from drain to source as the body diode becomes reverse biased. The PMOS does not enhance as the V_{GS} becomes +ve whereas it needs to be -ve. For example, the PMOS that I chose (SSM3J338R,LF) has a V_{GS} of -1.8V meaning that I need to apply at least that to the source for the PMOS to conduct. When the PMOS starts conducting the resistance is only ~20mOhms meaning that a very minimal voltage drop occurs. Theoretically we can maintain 99.97% efficiency.

Another form of protection that I implemented was a TVS diode for transients generated from ESD events. A TVS diode is a zener diode designed with the intent of clamping voltage spikes to a low level. The diode is reverse biased and when a voltage greater than the zener breakdown voltage appears at the battery +ve, the TVS diode rapidly opens a path to ground to absorb the energy of the ESD event instead of it going through the circuit. Even walking across a carpet can create an ESD event near 10kV.

The TVS diode must be carefully chosen for its reverse breakdown voltage (V_{RWM}), i.e. the voltage below which the diode will not conduct significantly, its clamping voltage (VC), the maximum voltage that appears across the diode in a transient event and the reverse leakage current, the current that can leak through the diode in reverse bias. With that in mind I chose the AQ1250-01ETG, which has a VWM of 5V (much more than out theoretical 3V2 max, a VC of 8.7V which our PFET and voltage regulator can tolerate, and finally an ultra low quiescent current of 20nA which will barely affect battery longevity.

Image of AQ1250-01ETG in SOD-882 package (1 x 0.6mm)
Source: Littelfuse

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CLASS 3

Ultimately, most of the design work for the schematic must be done with a lot of care and consideration as it is the backbone for the rest of the design; for this reason Classes 3 will have less writing in this schematic review section. Expect more in the following reviews.

GENERAL IMPROVEMENTS

In order to save a few nA, I only used port 1 GPIO on the Nora B206 as it means that only that port has to be enabled. Port 1 also has interrupt and wake up capabilities unlike port 2. Port 0 was unsuitable as it only has 4 or 5 exposed pins depending on the package.

Another improvement I made was removing a resistor that I planned to solder on after programming. It was an NRESET pullup however as per the Nora B2 System Integration Manual there is already an internal pullup on the NRESET meaning an additional pull up would only waste current and space.

Penultimately, I added a few status LEDs and relevant test points so that when the first prototype inevitably didn't work I could pinpoint why faster. It was also important to place ground test points near all data test points to reduce parasitics in order to produce a truer representation of the signals on an oscilloscope.

The last functional improvement that I made was adding 2V8 and ground test points, the battery voltage can be measured by directly probing the holder. I did not place test points on the I^2C traces as the stubs would add capacitance which would then reduce the maximum pull up resistance and increase current as mentioned earlier.

For the final note of this section I will talk about the aesthetic and legibility improvements to the schematic. Firstly, I ordered the designator numbers by their position in the schematic - the schematic should be read in the order ->

1) POWER

2) SoC

3) DEBUG

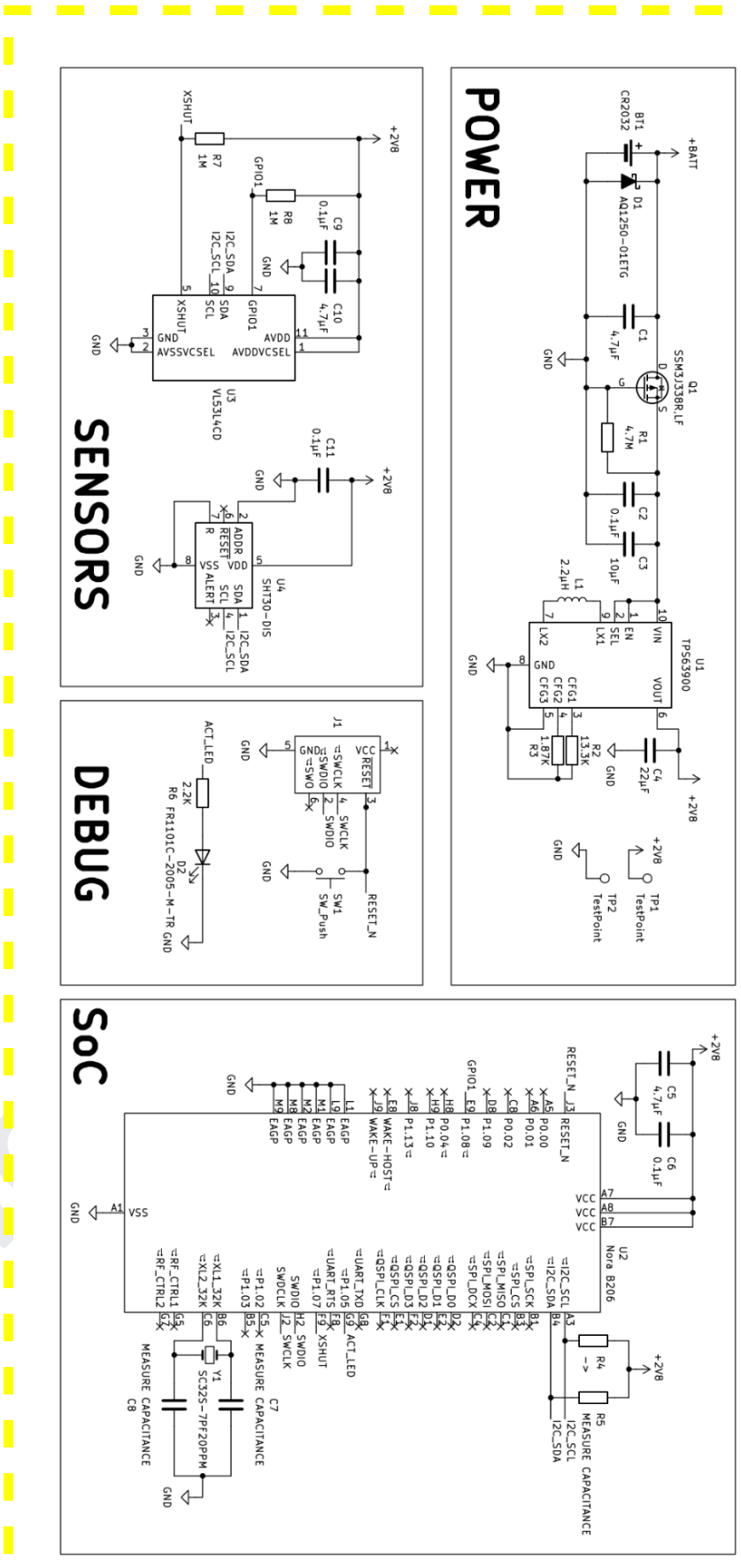
4) SENSORS

I also added bounding boxes around each subsection to make the schematic clearer. I also applied general schematic design rules throughout the entire design such as power symbols facing up, ground symbols facing down, and no four way junctions of wires. I also used appropriately named labels for all important signals and power.

As promised before, the full schematic is on the page below

WORK IN PROGRESS

UPDATE THIS


POWER
SENSORS
DEBUG
SoC
+BATT
+2V8
GND
BT1
CR2032
D1
AQ1250-01ETG
Q1
SSM3J338R,LF
U1
TP563900
U2
Nora B206
U3
VL53L4CD
U4
SHT30-DIS
J1
SW1
SW_Push
D2
TP1
TP2
TestPoint
Y1
SC32S-7PF20PPM
MEASURE CAPACITANCE
RESET_N
SWCLK
SWDIO
I2C_SCL
I2C_SDA
XSHUT
ACT_LED
WAKE-HOST
WAKE-UP

PCB Review

This section contains the class-based review of the pcb design including but not limited to, part placement, signal integrity and package selection. The front and rear copper layers are available at the end of the section.

CLASS 1

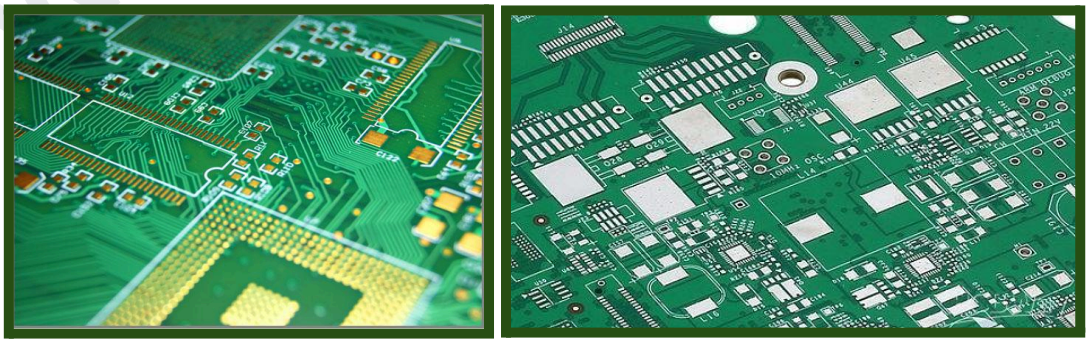
PCB FABRICATION SPECIFICATIONS

For better understanding of the following sections, it is a good idea to discuss the fab specifications for the PCB. This includes the number of layers (and physical stackup), surface finish/material, via covering method et cetera. As a sidenote, I decided to assemble the PCB myself to reduce costs and to be able to use component distributors with European warehouses that stocked the relatively new Nora B2x6 modules.

Initially, after the first layout, it was obvious to me that I should use a four layer board. Power routing on a two layer board increased routing complexity significantly and having dedicated ground planes on a four layer board would improve signal integrity. I ended up with the following electrical stackup:

Layer 1 - Signal
Layer 2 - Ground
Layer 3 - Power (2V8)
Layer 4 - Ground

Layer 1 was where all of the signal routing took place, it was also surrounded with a ground pour for copper balance and improved noise immunity/signal integrity. Squeezing as much immunity to noise as possible into the PCB was imperative so that the weak GPIO pull up resistors could function. Layer 2 was an uninterrupted ground plane. Importantly it is the next layer from the signal which brings similar effects as the ground pour on Layer 1. All ground layers were stitched with vias to ensure ground integrity. Similarly, Layer 3 carried all of the power. Layer 4, was in majority a ground plane with the exception of a short trace carrying the battery positive a short distance. In practice this ground is not used much and the trace was quite short so the EMC implications are negligible.



ENIG (left) vs HASL (right) aesthetic appearance

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As detailed in the next section, the surface finish and and via covering were heavily dependent on the battery retainer. Firstly, a 2µ" ENIG (Electroless Nickel Immersion Gold) surface finish was chosen for its increased durability, excellent surface planarity (which improves fine pitch soldering reliability), increased corrosion resistance and for the fact that it is lead-free. As opposed to a single layer of SnPb (or alternatives) in HASL, ENIG involves a layer of electroless nickel and a very thin layer of immersion gold (0.05 to 0.1 µm). The design also required tented vias so that power vias did not contact against the battery negative and cause a short-circuit fault.

PACKAGE SELECTION

Firstly, the size of the PCB was constrained by the battery holder (and battery) size plus the antenna keepout zone. The PCB size was going to be heavily based off of the battery holder size so I had to choose a small holder. There were two main options, battery retainers and battery holders.

A battery retainer contacts against only one side of the battery (CR2032 cells have a positive contact on one side and a negative on the other), where the PCB requires exposed conductor (commonly some type of gold). Ideally hard gold would be selectively electroplated onto just the battery contact pad however this would drastically increase costs unless manufacturing in bulk. For this reason ENIG is the preferred finish for low-volume prototypes.

In contrast, battery holders generally contact both sides of the battery meaning the battery doesn't physically touch the PCB. This improves connection reliability, almost nullifies the risk of long term failure from repeated abrasion on the battery contact pad meaning that more expensive surface finishes such as ENIG are not strictly required.

Battery holders, however, are usually a few millimeters longer than holders due to being more than a single piece of shaped metal. Thus I chose to use the Keystone 3034 retainer as I already had a footprint for it and it was readily available at major distributors such as Digikey.

As for major IC package selection, I was constrained to the footprint of each particular IC. If I needed a specific feature, it was rather unlikely that I could find an IC with a different footprint but with the same features. For example, the Nora B206 is the only available NRF54Lxx module available in large quantities as of writing (13/09/25) meaning I must put up with its very dense LGA package. Similarly, ST only manufactures their ToF sensor range in LGA however all of the pads are on the perimeter of the package meaning routing is straightforward. The SMPS IC also only had a single footprint (non LGA/BGA).

However, due to the late nature of the addition of the temp/humidity sensor, the pinout/package was very important. Look at *Figure 2* below, showing the I^2C traces leaving the SoC. The I^2C traces going downwards are going to the ToF and are not to be changed, the temp sensor is to the right. Visibly, the data trace is above the clock trace. (I^2C development will be discussed in detail in the software review).

WORK IN PROGRESS

This meant I had to find an IC with its data and clock pins in the same orientation, otherwise I would have to cross them. I did not want to cross them as I would have to use vias which would add unnecessary capacitance (see pg15) or use zero ohm resistors which would add to the BoM. This meant that I did not use the first temp sensor that I found (which was the SHTC3), that offered a slightly smaller package and slightly better package but its larger cousin, the SHT30.

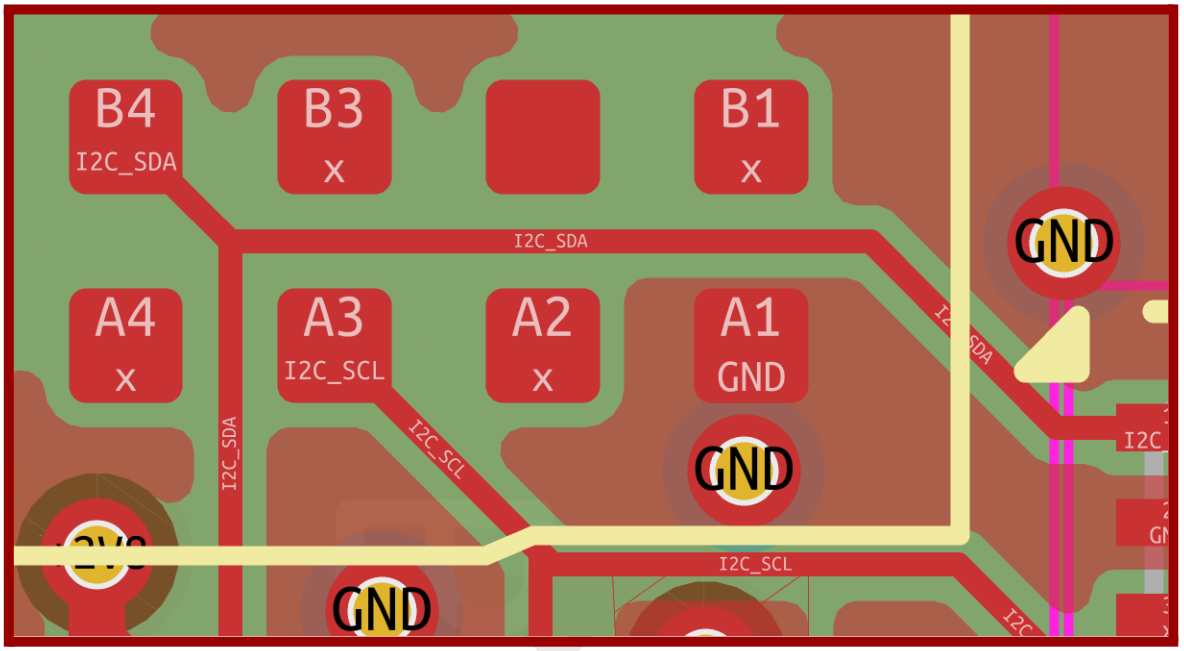


Figure 2

As for passives, the minimum package that I set was 0402 (Imperial, equivalent to 1005 metric). This was the smallest size that I felt I could put onto the board with tweezers so that it could be soldered by hotplate. Advantages of small packages include cheaper prices and increased component density potential. However, small packages usually mean worse power handling and thermal performance. Small packaged MLCCs can also struggle to achieve large capacitances with decent specs.

For this reason, I tried to use 0605 components whenever possible unless 0402 made a significant space saving or small loop area was required (eg in the SMPS). Notably I used an 0805 inductor instead of a larger power inductor as due to the orientation of the buck-boost IC (discussed in the next section) it would extend the board length by a noticeable amount.

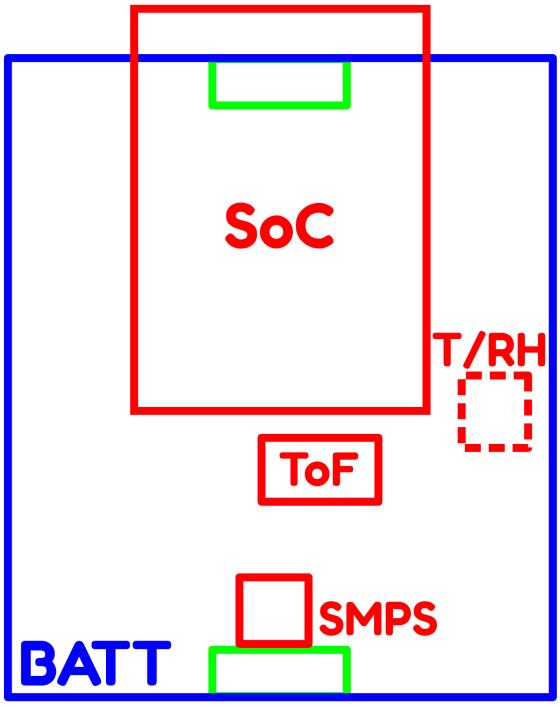
Furthermore, the DCR increase was manageable,112mOhms in the 0805 vs ~60mOhms in a power inductor. The difference at the (expected) low current is negligible as other factors will dominate power consumption however I plan to use this IC and inductor combination in other projects where it may make a significant difference.

CORE LAYOUT

The approximate layout of major components was the first step of the design of the actual PCB. I had a lot of flexibility at this stage as there were only two main constraints, the SoC's antenna had to be on the edge of the board, and the board could not be smaller than the battery holder *(duh)*.

Quite surprisingly, my initial layout worked very well. In Figure 3 below, red lines represent top layer components and blue lines represent bottom layer components. The temperature sensor is dashed as it was not present at the start of the layout design.

Figure 3



Evidently, the battery holder dictates the minimum PCB size. This meant that the major IC placements could be optimised for routing instead of board size which greatly improved the ease of development.

The SoC was the first component I placed as the antenna has to be on the edge of the board and be away from tall components. It served as the reference for where all of the other components should be.

I then placed the battery as far upwards as possible without overlapping the keep out zone of the antenna. As to minimise the perimeter size of the board.

Then, I added the ToF sensor. The I^2C pads of the NORA B206 are located near the bottom right (looking down on the copper on the pcb) so that it aligned with the I^2C pads on the ToF sensor. The ToF sensor was placed very close to the SoC so that the trace length could be minimised, reducing stray capacitance and improving noise immunity. The ToF is slightly offset to the right so that the 32.768KHz crystal could be accommodated.

Finally, the SMPS was placed next to one of the battery +ve pads (as visible in green in Fig. 3). This was so that I could minimise the distance from the +ve to the SMPS V_{in} to reduce ohmic losses and voltage drop as an effect of increased resistance. The shorter connection also minimised parasitic inductance which helps to reduce noise and improves efficiency.

WORK IN PROGRESS

CLASS 2

SMPS LAYOUT

Power supply layout was a key task in order to achieve high efficiency thereby extending battery life. Below, Figure 4 displays the power supply layout. In the middle we see the heart of the power supply, the TPS63900 buck boost converter. The layout revolves around this IC so it is imperative that it is placed and orientated efficiently. In this configuration, the 2V8 output is close to the ICs that require it above and all connections can be made without the use of vias.

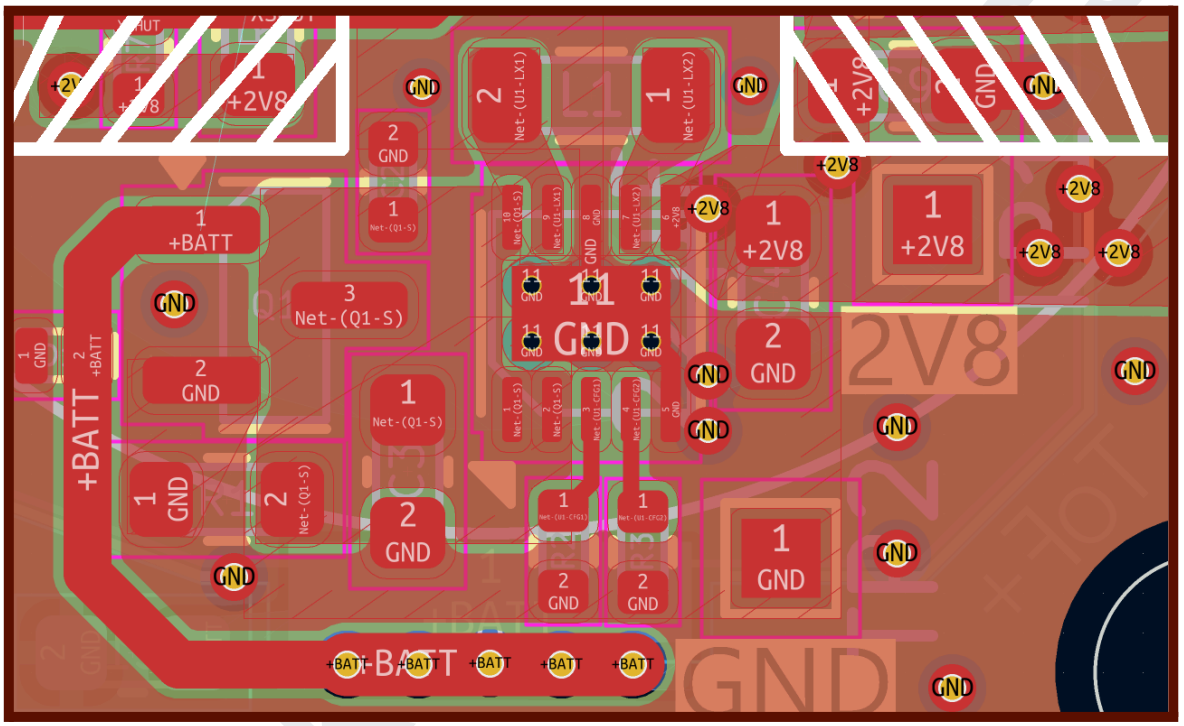


Figure 4

Components not relevant to the power supply have been marked by white boxes.

However, let's talk about the layout sequentially, from battery to 2V8 output. First, a cluster of five vias connects the +ve terminal of the battery holder to the PMOS responsible for RPP. The net is labeled +BATT. Before +BATT reaches the PMOS however, there is the aforementioned ESD diode (visible on the very left of the image). It is closer to the battery than the transistor so that ESD events are clamped through it instead of destroying the transistor.

Next, the net Q1-S connects to all relevant pads via a large ground pour. This is a common theme in this design and serves to reduce ohmic losses and voltage drop by decreasing resistance, and to reduce noise by reducing parasitic inductance. The two config resistors appear at the bottom of the layout, above the +BATT via cluster. As I had the space I placed them very close to the IC however their placement is not crucial and they could be fairly far away on the board if necessary (within reason).

Notice how all of the capacitors are very close to the main IC with many ground vias for return current. This is to reduce the loop inductance, minimising noise and EMI. Furthermore, as the capacitors get further and further away from the IC, the impedance of the PDN increases, and their ability to attenuate electrical noise decreases, causing a worse output with more noise. This is due to the return loop getting larger. In a similar fashion, if the capacitors are close to the IC but the ground path is long, the PDN impedance increases and the design suffers. Similar principles apply to the connection of the inductor, although it obviously is not used for noise purposes but to complete the buck boost topology.

Lastly, the power supply connects to the power (2V8) plane with a via cluster to the right side. The three vias reduce the resistance that the current sees reducing ohmic losses and voltage drop. Next to it, there is a test point to test (using a DMM or similar) if 2V8 is actually produced. The ground reference is below, near the config resistors. They are both marked by silkscreen.

NOISE IMMUNITY AND SIGNAL INTEGRITY PART 1

PROGRAMMING

LGA FAN OUT

RF DESIGN

Being conscious of RF performance was necessary throughout the entirety of the PCB design phase. Bad antenna layout would mean reduced range (due to the worse antenna performance) and increased power consumption (due to more retransmissions due to lost data).

CLASS 3

SILKSCREEN

MINIATURIZATION

COMPONENT SPECIFIC REQS

SIGNAL INTEGRITY PART 2

WORK IN PROGRESS