NATIONAL UNIVERSITY
of Computer & Emerging Sciences, Lahore

Department of Computer Science

EE2013 – Computer Architecture

Spring 2026

Instructor Name: **TA Name:**
Email address: **Email:**
Office Location/Number: **Office Hours:**

Course Information
Program: BS **Credit Hours:** 3 **Type:** Core
Pre-requisites (if any): Computer Organization and Assembly Language (EE2003)
Class Meeting Time:
Class Venue:

Course Description/Objectives/Goals:
The main objective of this course is to provide a profound understanding of the architectural design and internal working of a microprocessor, enabling computer science students to appreciate concepts like optimization and hardware level performance issues. This course also introduces advanced concepts including pipelining and superscalar architecture. Additionally, the fundamentals of GPUs are discussed.

Course Learning Outcomes:

Course Textbook
1. David A. Patterson, John L. Hennessy, *Computer Organization and Design: The hardware/software interface, RISC-V Edition*.
2. David A. Patterson, John L. Hennessy, *Computer Architecture: A Quantitative Approach* 6th edition.

Additional references and books related to the course:
1. John Paul Shen and Mikko H. Lipasti *Modern Processor Design: Fundamentals of Superscalar Processors*.
2. M. Morris Mano, *Computer System Architecture* 3rd Edition 1993, Prentice Hall.
3. William Stallings, *Computer Organization and Architecture: Designing for Performance*, Prentice Hall, 11th edition.

Tentative Weekly Schedule

Lect #	Topics to be covered	Readings	Assignments
1-2	Introduction to basic hardware components and devices, Arithmetic and Logical Operations, Signed and unsigned binary numbers	Text1 (Section 2.4, Appendix-A), Reference Material	
3	Understanding and evaluating CPU Performance	Text1 (Section 1.6)	
4-5	Computer Instructions and instruction codes, Introduction to RISC-V Assembly Language, RISC-V Instruction Types	Text1 (Section 2.1-2.7)	
6	Integer Multiplication, Division	Text1 (Section 3.3-3.4)	
7	Floating point representation, Floating Point Addition Operation	Text1 (Section 3.5)	
8-9	Design of Control and Datapath of a Single Cycle RISC-V Machine	Text1 (Section 4.1 – 4.4)	Assignment 1
10	Multi-cycle Motivation, Revision for Mid-1	Text1 (Section 4.4 - 4.5)	
Midterm-1			
11	Introduction to pipelining, Enhancing Performance with Pipelining	Text1 (Section 4.5)	
12-13	Pipelined datapath and control	Text1 (Section 4.6)	
14	Data Hazards: RAW, WAR, WAW	Text1 (Section 4.5, 4.7)	
15	Control Hazards, Branch Prediction	Text1 (Section 4.5, 4.8)	Assignment 2
16	Exceptions	Text1 (Section 4.9)	
17	Difference between RISC, CISC and VLIW, Introduction to Superscalar Processor	Text2 (Section 3.1), Reference Material	
18-19	Instruction Level parallelism (ILP), Data dependence, hazards and control dependence for ILP	Text2 (Section 3.1)	
20	Revision for Mid-2		
Midterm-2			

21	Code Scheduling, Loop Unrolling	Text2 (Section 3.2)	
22	Memory Hierarchy basic concepts Basics and Direct mapped caches	Text1 (Section 5.1-5.3)	
23	Associative Caches and Miss Rates	Text1 (Section 5.3)	
24	Processor performance evaluation with cache / Multi-level Caches.	Text1 (Section 5.4)	
25	Virtual Memory	Text1 (Section 5.7)	
26	Introduction to parallel processors, Amdahl's Law	Text1 (Section 1.10, 6.1-6.2)	Assignment 3
27	GPUs, NVIDIA GPU Architecture	Text1 (Section 6.6)	
28	Revision for final exam		

(Tentative) Grading Criteria

1. 3-4 Assignments (10%)
2. 4-5 Quizzes (15%)
3. 2 Midterm Exams (30%)
4. Final Exam (45%)

Course Policies

1. Quizzes may be un-announced.
2. No makeup for missed quiz or assignment.
3. 80% attendance