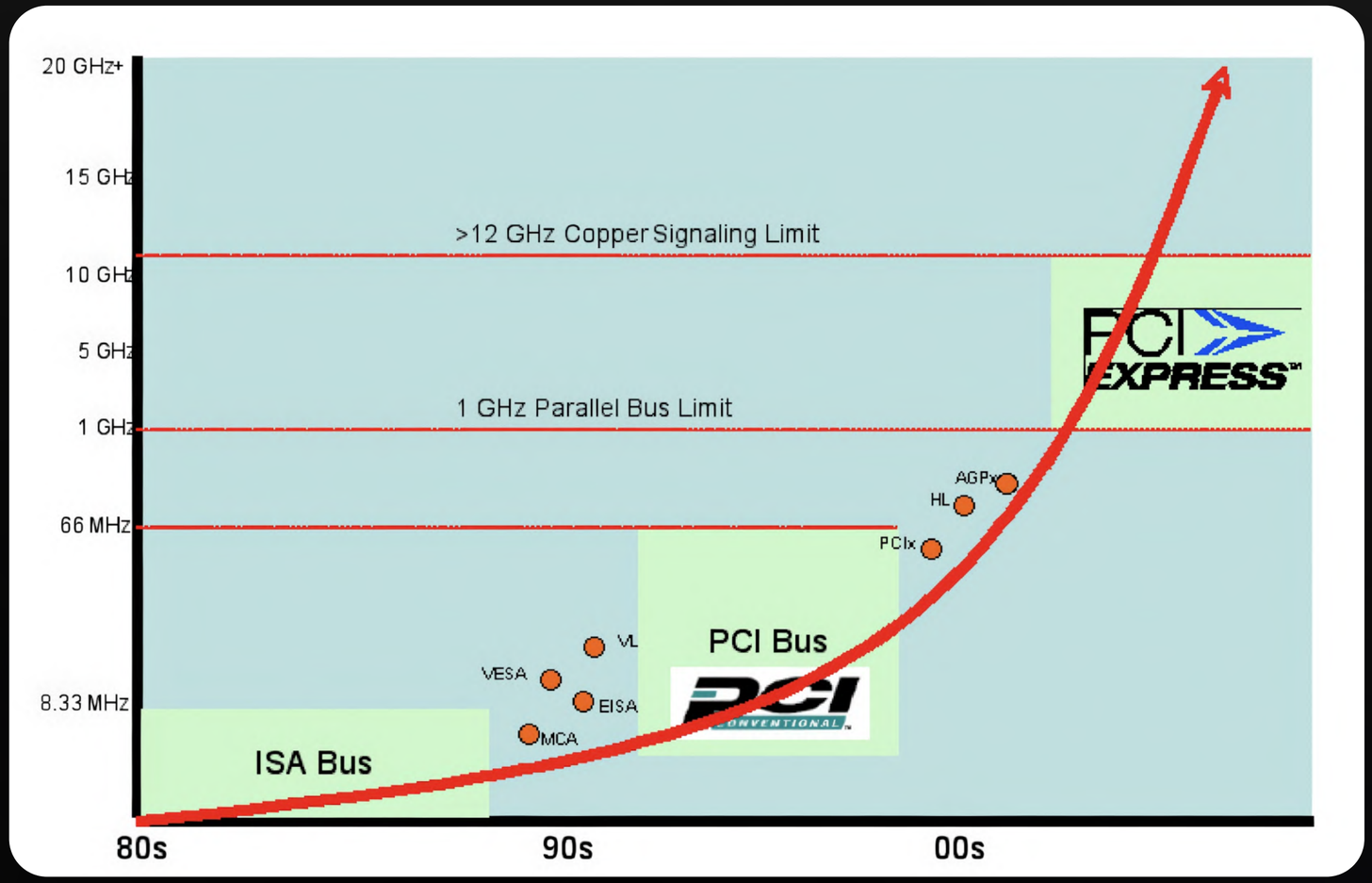
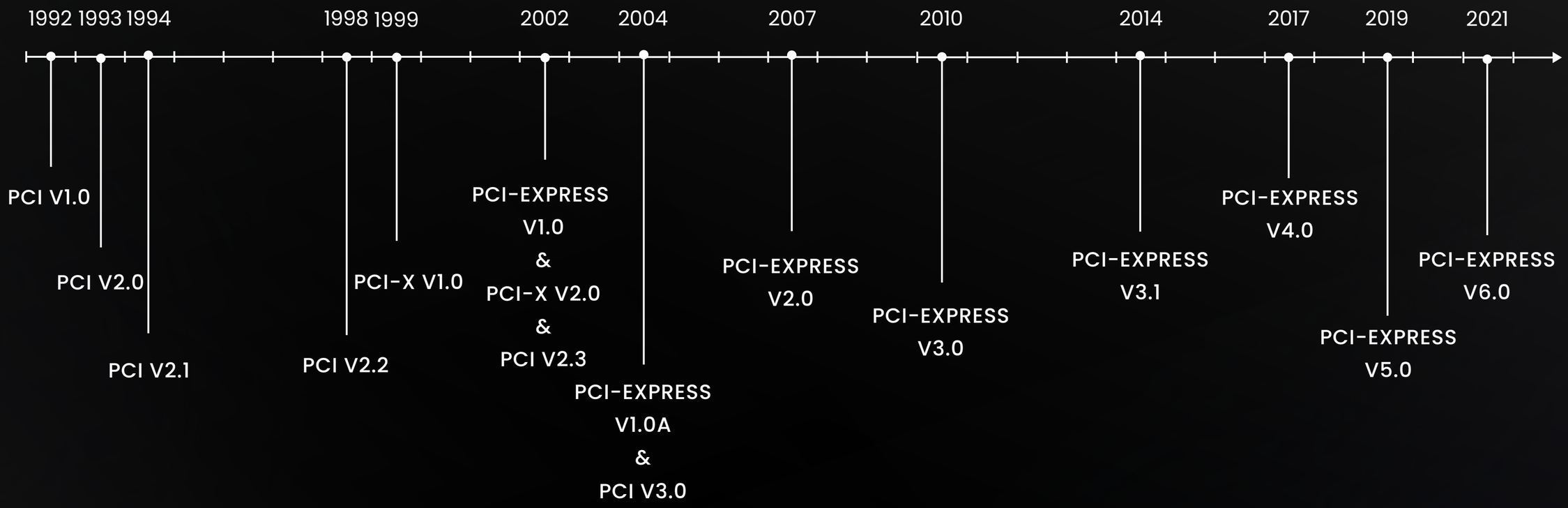
ALEXEY LAPIN

PCI-Express Overview

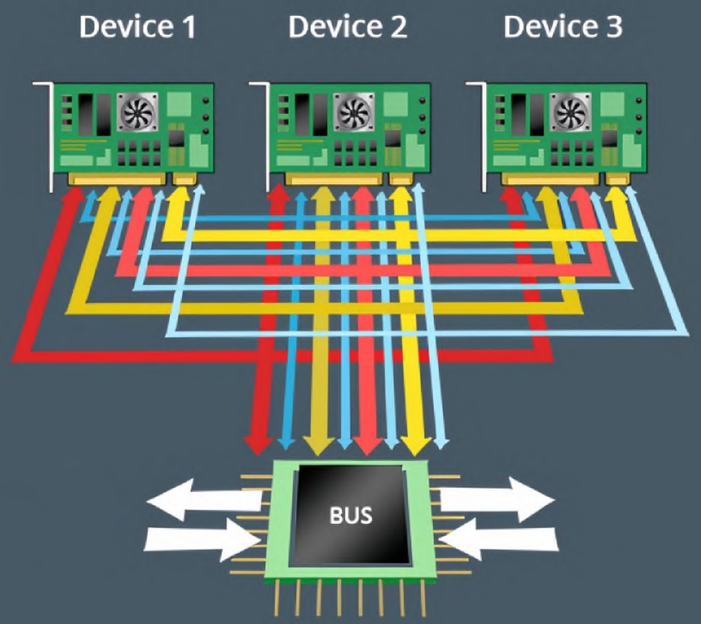
Evolution


20 GHz+
15 GHz
10 GHz
5 GHz
1 GHz
66 MHz
8.33 MHz
>12 GHz Copper Signaling Limit
1 GHz Parallel Bus Limit
PCI EXPRESS
AGPx
HL
PCIx
VL
VESA
EISA
MCA
PCI Bus
PCI CONVENTIONAL
ISA Bus
80s
90s
00s

Evolution & Versions

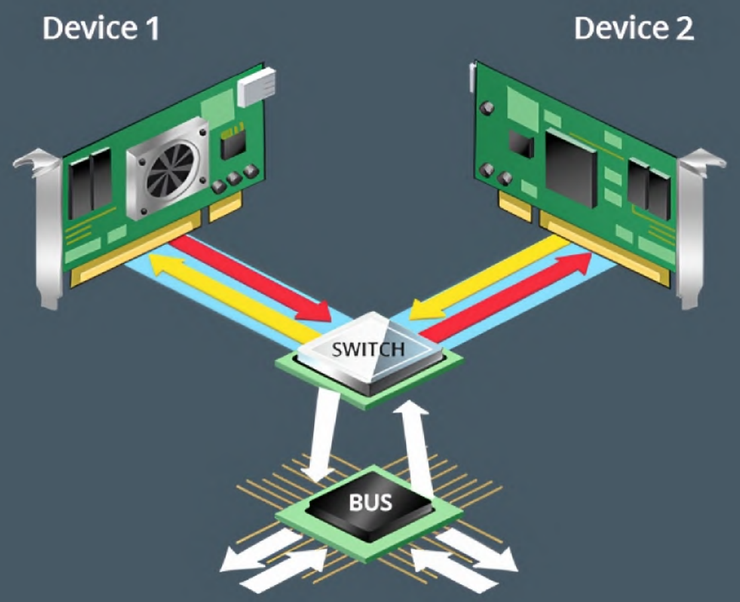


PCI & PCIe



PCI/PCI-X

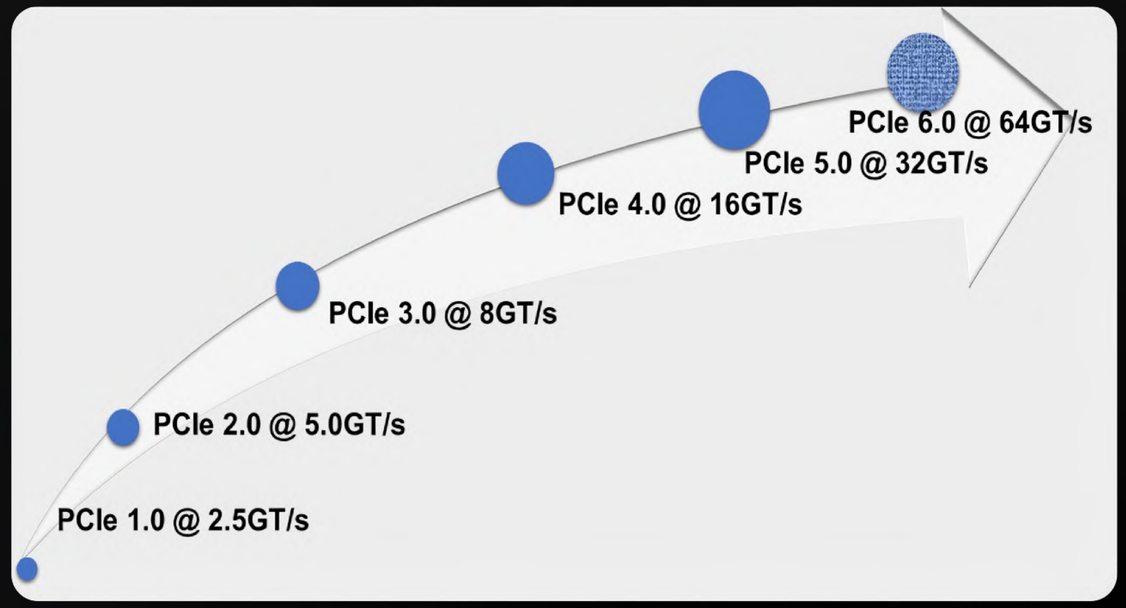
Parallel Connection



PCI-E

Serial Connection

Evolution & Versions

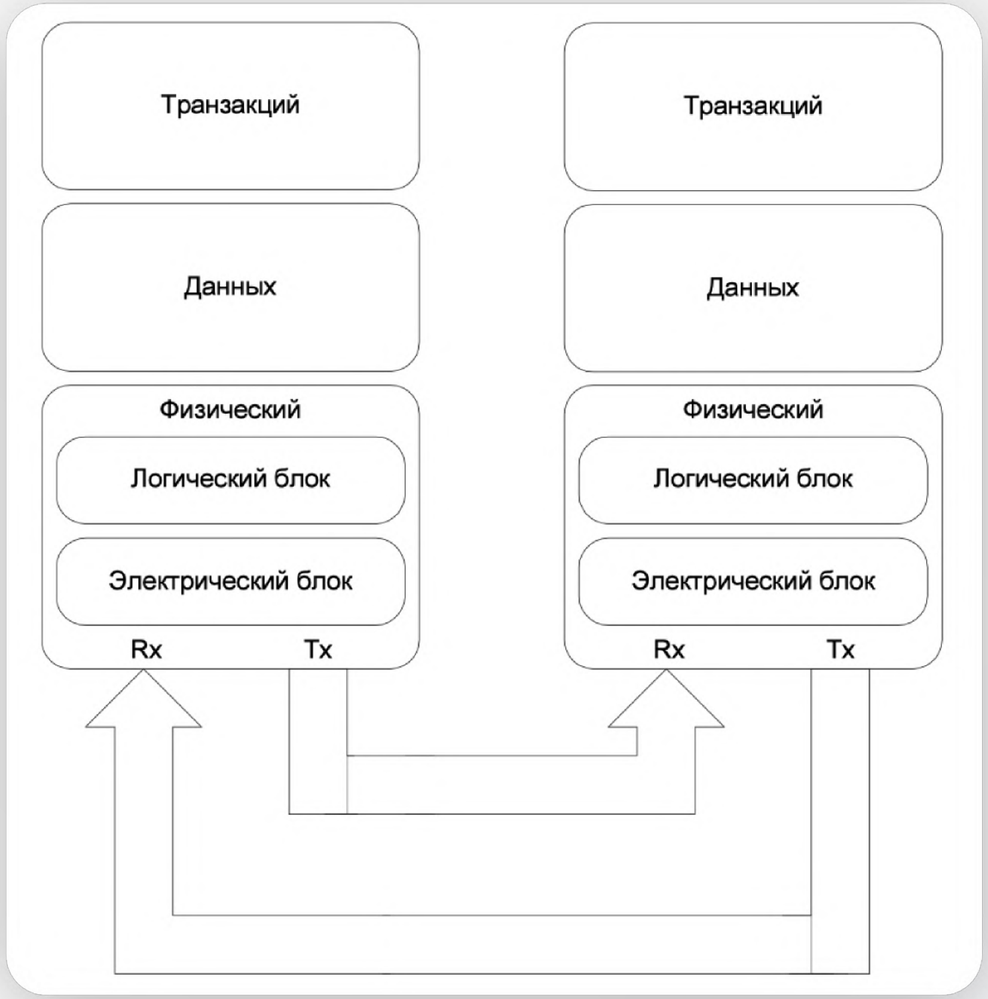


PCIe Specification	Data Rate(GbZs) (Encoding)	Year
1.0	2.5 (8b/10b)	2003
2.0	5.0 (8b/10b)	2007
3.0	8.0(128b/130b)	2010
4.0	16.0 (128b/130b)	2017
5.0	32.0 (128b/130b)	2019
6.0	64.0 (PAM-4, Flit)	2021

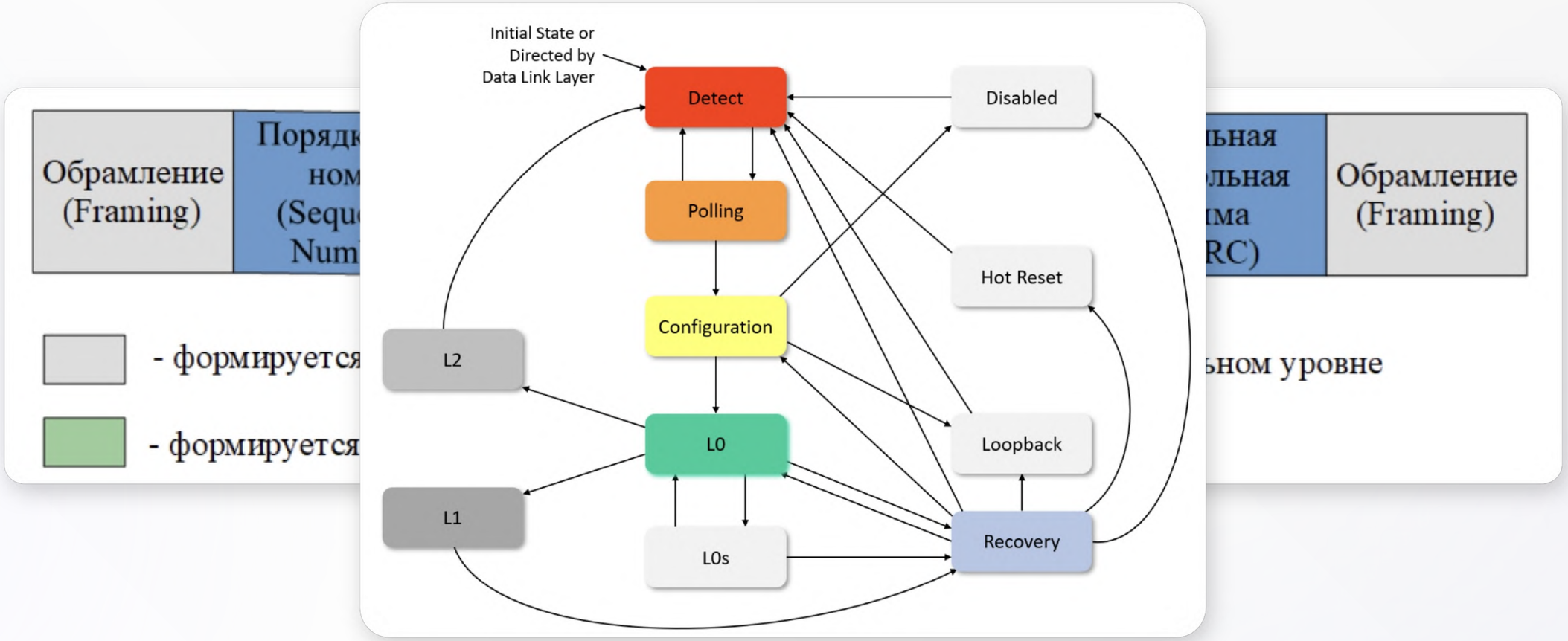
Speeds

Version	Introduced	Line code		Transfer rate per lane	Throughput				
					x1	x2	x4	x8	x16
1	2003	NRZ	8b/10b	2.5 GT/s	0.250 GB/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s
2	2007			5.0 GT/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s	8.000 GB/s
3	2010		128b/130b	8.0 GT/s	0.985 GB/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s
4	2017			16.0 GT/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s
5	2019			32.0 GT/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s	63.015 GB/s
6	2022	PAM-4 FEC	1b/1b 242B/256B FLIT	64.0 GT/s	7.563 GB/s	15.125 GB/s	30.250 GB/s	60.500 GB/s	121.000 GB/s
7	2025 (planned)			128.0 GT/s	15.125 GB/s	30.250 GB/s	60.500 GB/s	121.000 GB/s	242.000 GB/s

PCI Express Protocol Stack



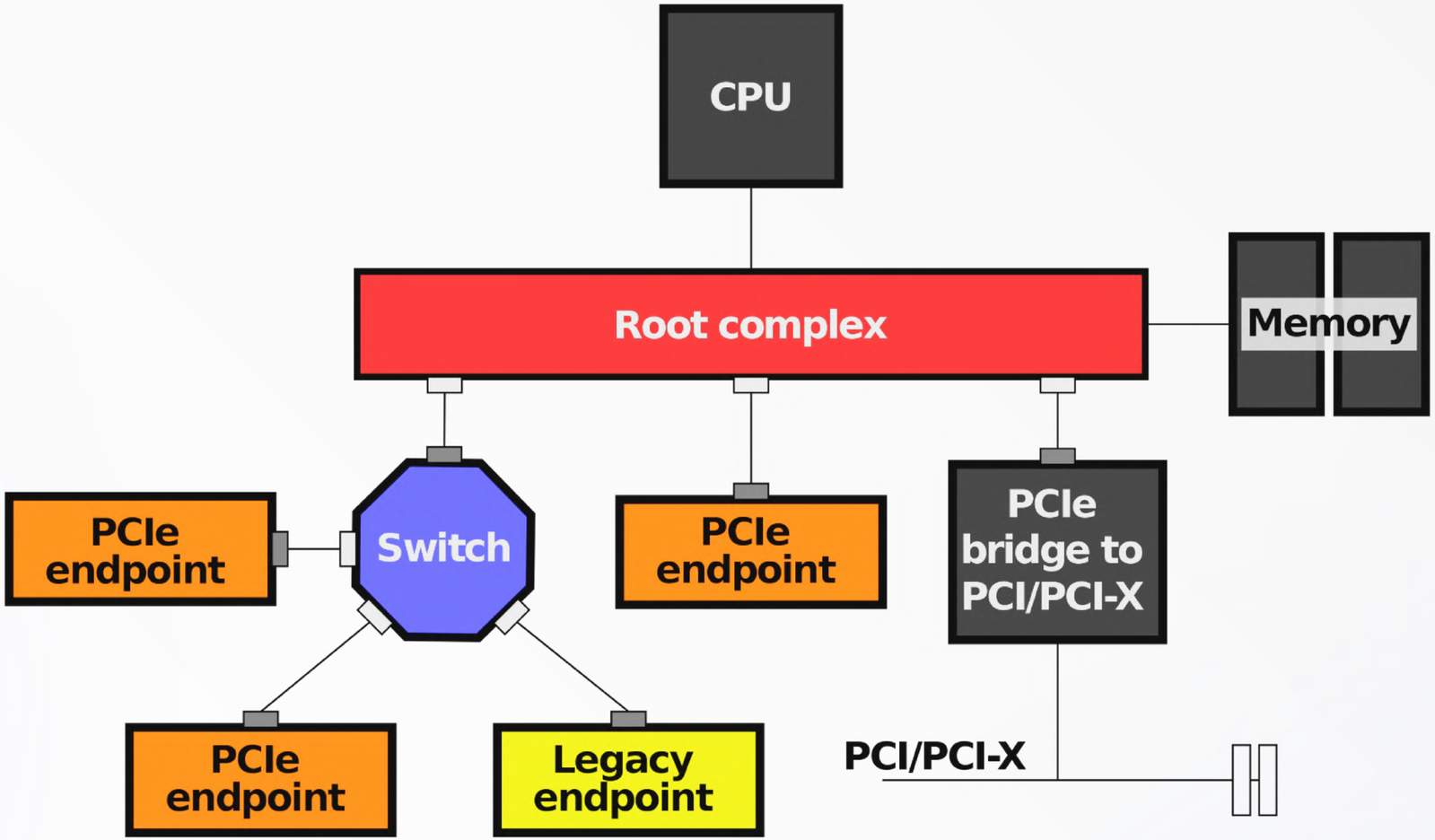
PCI Express Protocol Stack



PCI Express Trace Length

Version	Max Trace Lenght
1.0	20 inches (~50 cm)
2.0	20 inches (~50 cm)
3.0	14 inches (~35 cm)
4.0	10-12 inches (~25-30 cm)
5.0	13 inches (~33 cm)
6.0	13 inches (~33 cm)

PCI-Express Topology

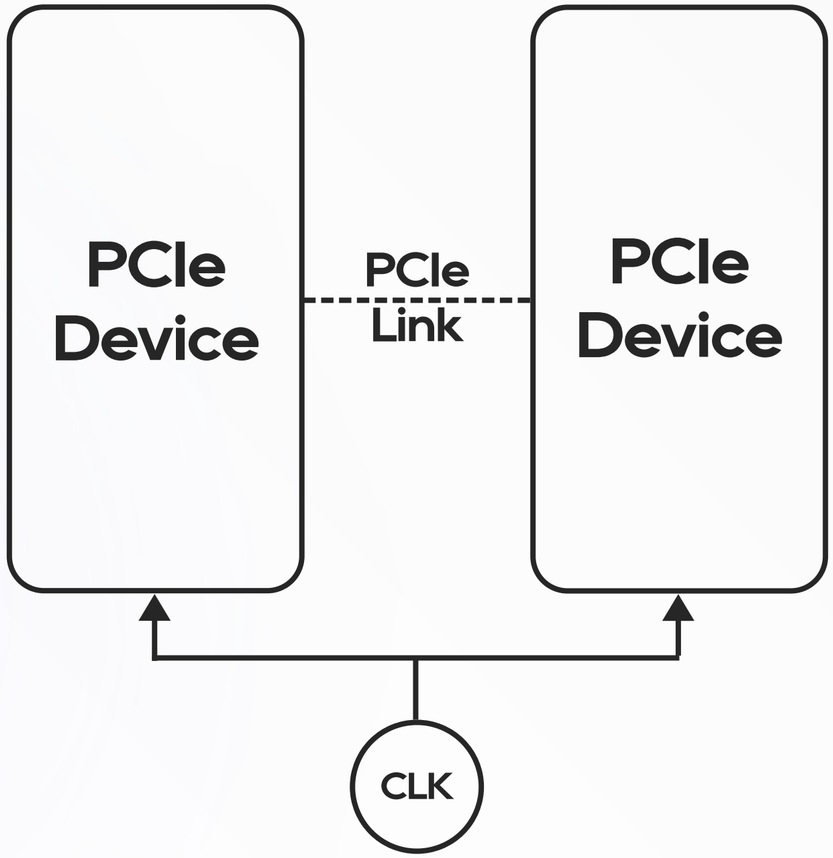


Reliable data transmission

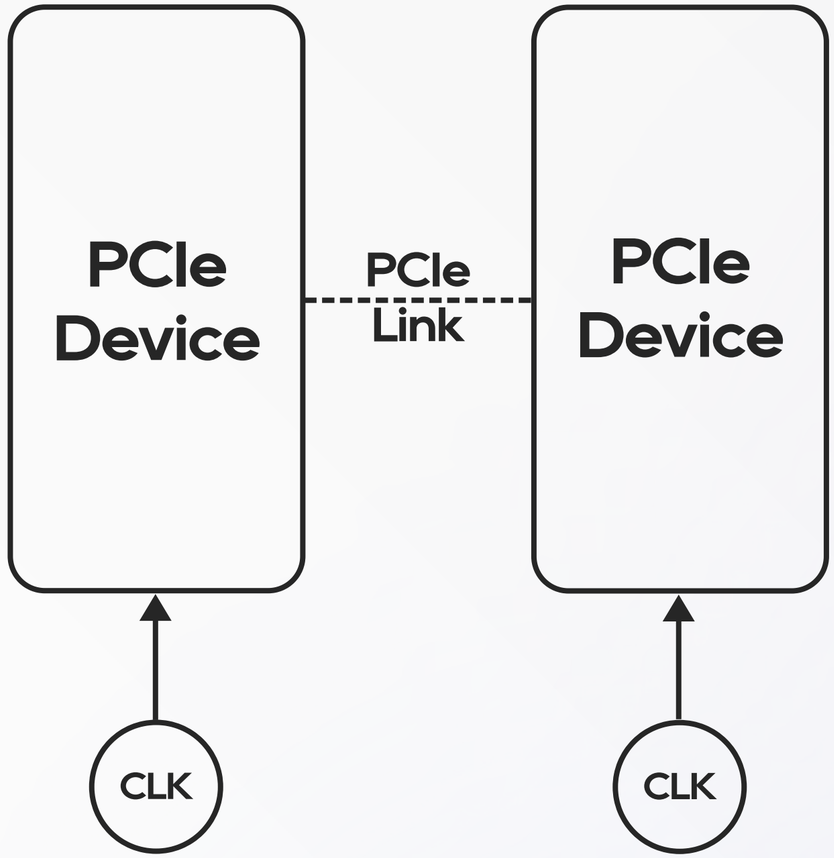
1. CRC
2. Acknowledge-retransmit mechanism
3. Flow control mechanism

Synchronous / Asynchronous

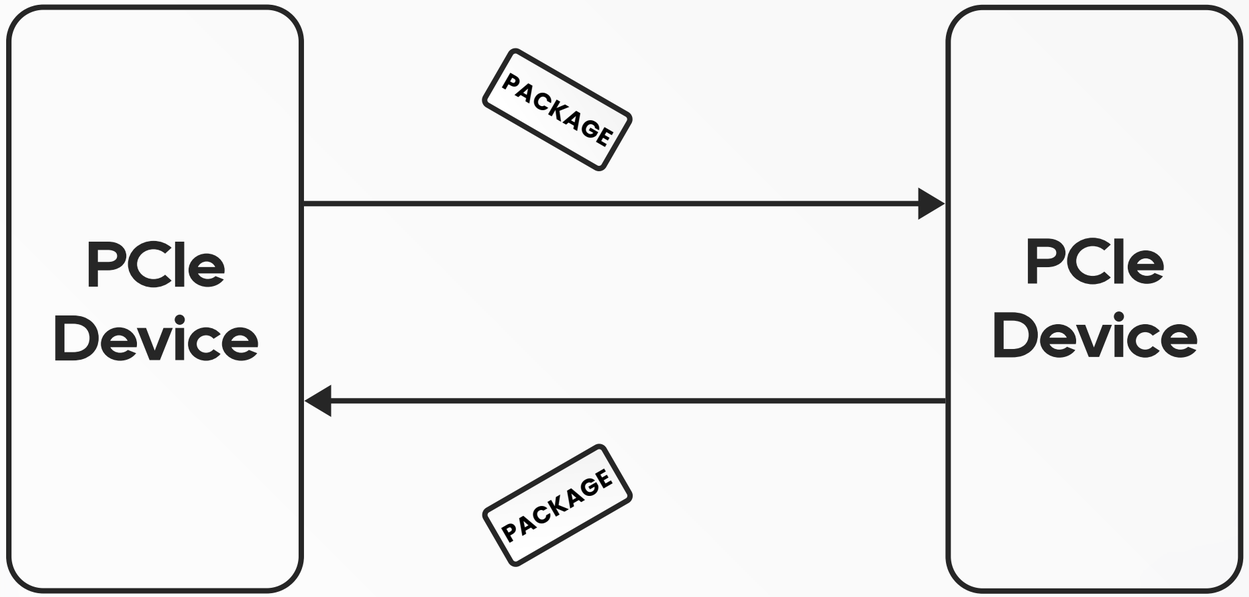
Common Clock

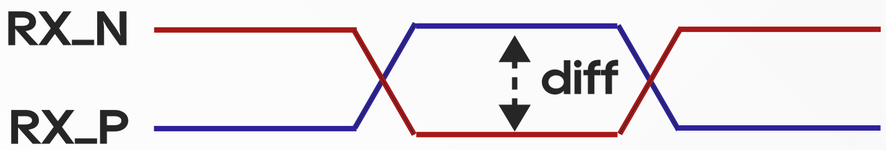


Separate Clock

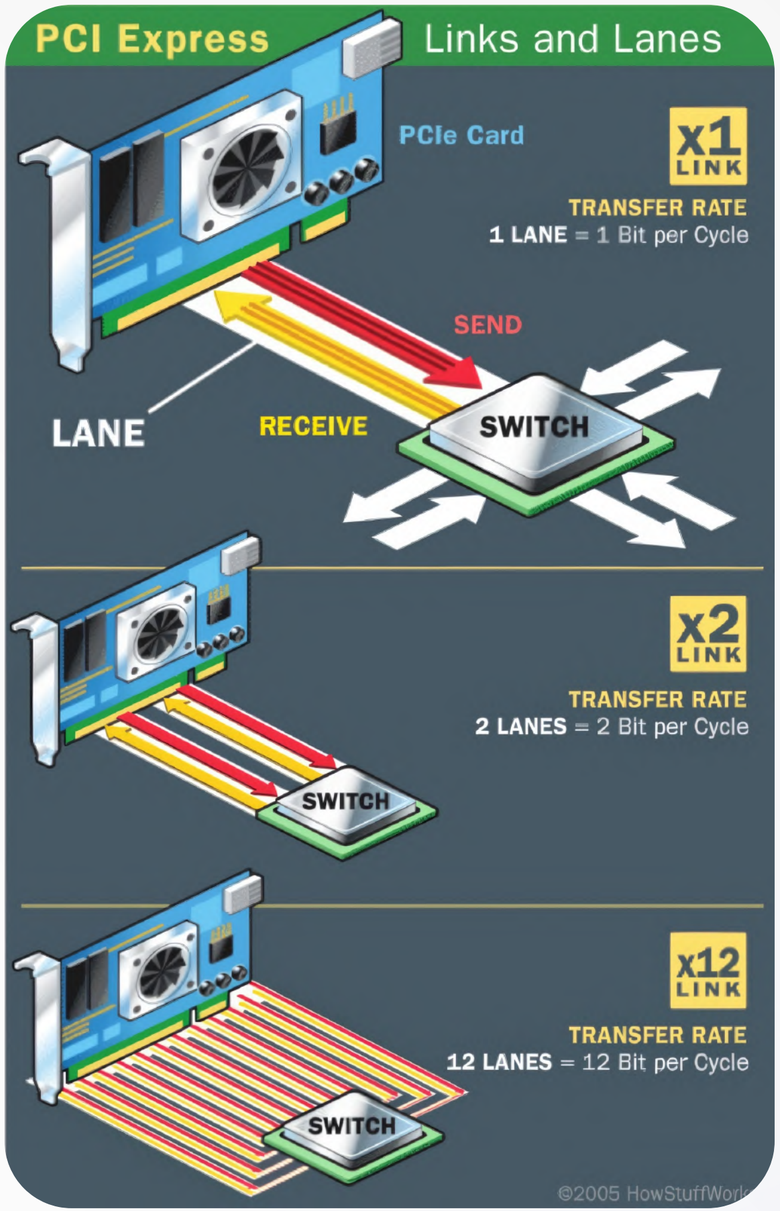


PCI Express Link

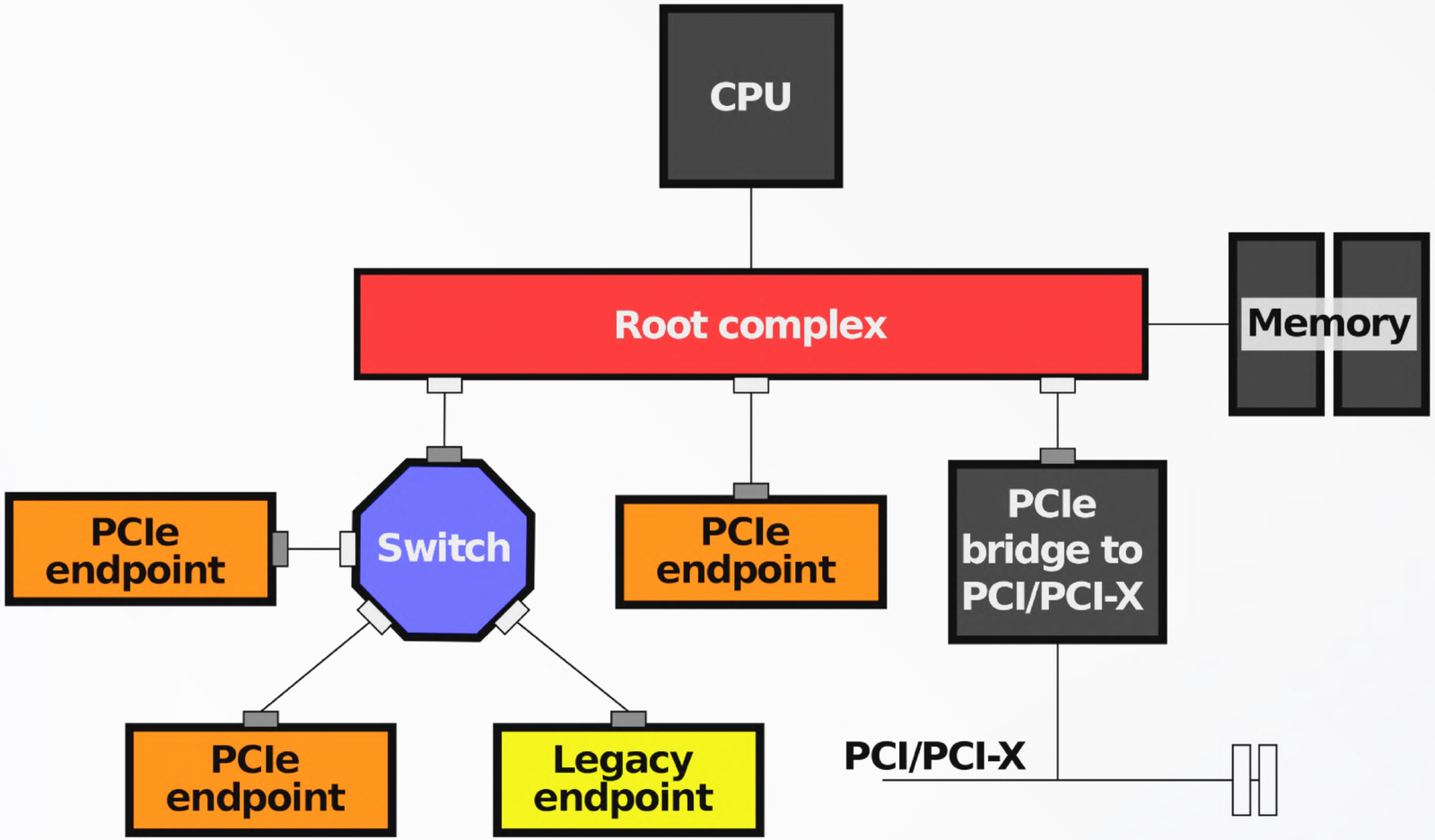




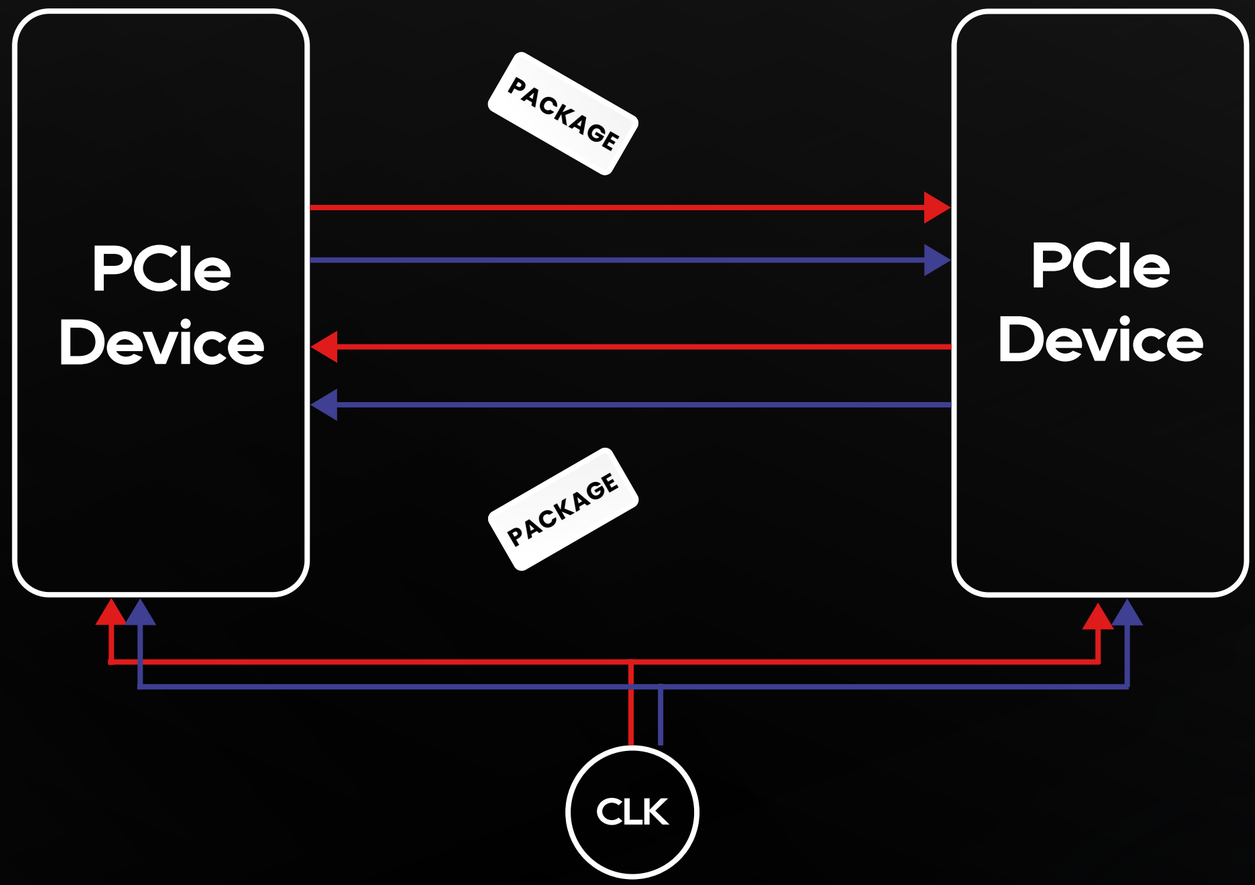
PCI Express Link



Device Roles

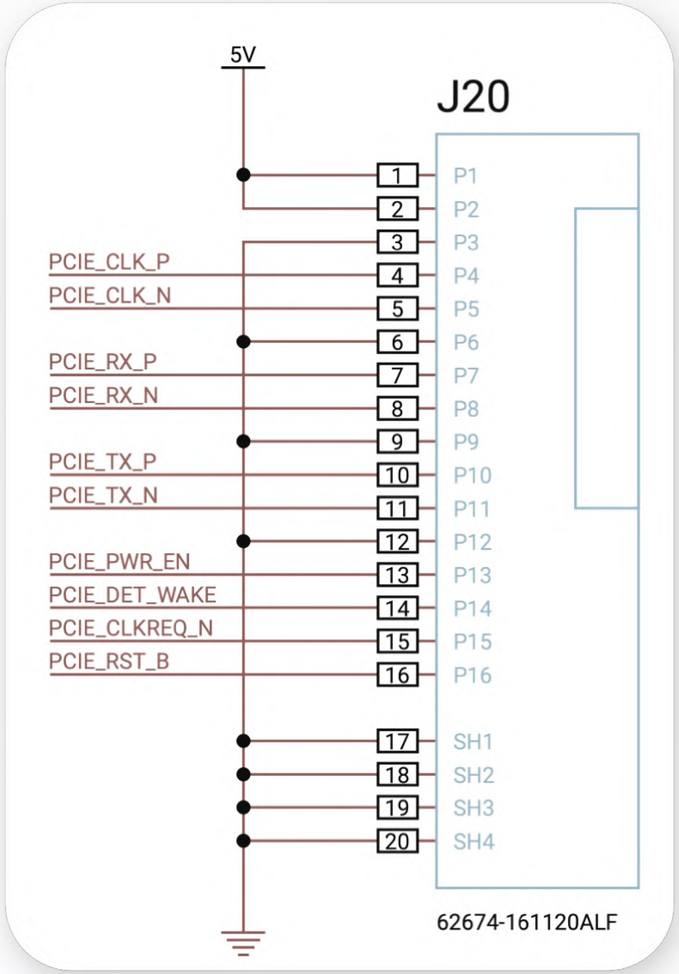


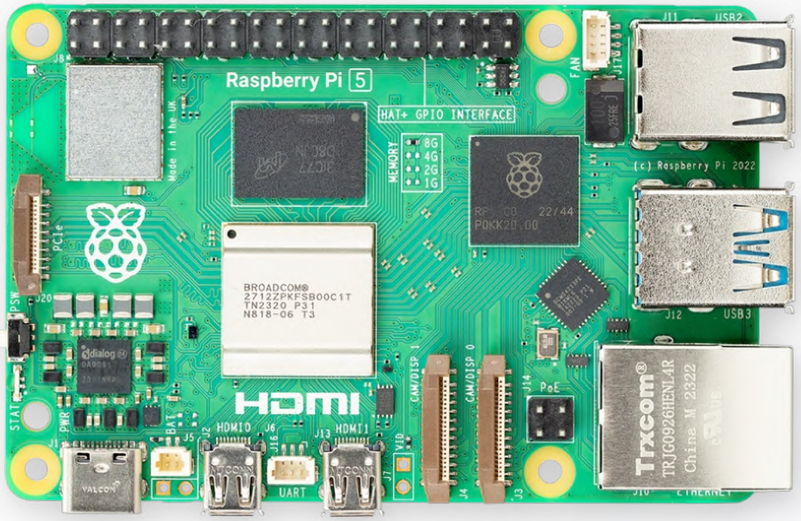
Minimal Configuration



ALEXEY LAPIN

Raspberry Pi Connector for PCIe





PCIe pinout

Pin	Side B	Side A	Description
01	+12 V	PRSNT1#	Must connect to farthest PRSNT2# pin
02	+12 V	+12 V	Main power pins
03	+12 V	+12 V	
04	Ground	Ground	SMBus and JTAG port pins
05	SMCLK	TCK	
06	SMDAT	TDI	
07	Ground	TDO	
08	+3.3 V	TMS	
09	TRST#	+3.3 V	
10	+3.3 V aux	+3.3 V	Aux power & Standby power
11	WAKE#	PERST#	Link reactivation; fundamental reset
Key notch			
12	CLKREQ#	Ground	Clock Request Signal
13	Ground	REFCLK+	Reference clock differential pair
14	HSOp(0)	REFCLK-	Lane 0 transmit data, + and -
15	HSOn(0)	Ground	
16	Ground	HSIp(0)	Lane 0 receive data, + and -
17	PRSNT2#	HSIn(0)	
18	Ground	Ground