sainathjs.vlsi@gmail.com
Bangalore
Phone: +91-9035026880

SAINATH SHANBHAG

Summary: Worked in architecture, design, validation of VLSI and Embedded for 14 years Intel Higher Education, Texas Instruments (USA), Freescale Semiconductors, Xilinx, Wipro, Infosys.

Experience Summary

- **1 year, 6 months in Intel Higher Education as Technical Project Manager, India**
- 10 years in VLSI and Embedded based on ARM based Design, Verification and Validation.
- 2 years in Software Testing and Development.

Education

- **Pursuing Part-time PhD in Data Visualisation at IIIT Bangalore**
- M.Tech in VLSI and System Design from HITAM, JNTU, Hyderabad, 2014: 77%
- B.E in Electronics and Communications, MIT, Manipal, 2001 : 77%
- 12th CBSE, Kendriya Vidyalaya 1997: 88 %
- 10th CBSE, Kendriya Vidyalaya, 1995: 77 %

Experience Profile

- **Technical Project Manager, India for Intel Higher Education (1 year 3 months)**
- Chief Architect: Setup a start-up technology company. (6 months)
- Senior Engineer: SoC Verification/ Validation: Xilinx, Hyderabad (2 years 3 months)
- Chip Design Lead Engineer: Freescale Semiconductors, Noida (2 years)
- Module Leader: VLSI IP Design/Verification for ARM: Wipro Technologies, Bangalore (8 months)
- Validation Engineer: Presilicon Verification(Emulation)/Validation/ Test suite development for ARM based design at Texas Instruments, USA as Wipro Contractor (2 years)
- ARM Processor Architecture Validation Engineer, Wipro, Bangalore (11 months)
- Software Engineer: Optical Network (Telecom) EMS/NMS Testing at Infosys, Bangalore (2 years)
- Assistant Manager: Embedded System/Instruments at Nicholas Piramal, Cochin (5 months)
- Software Engineer: Embedded Software Design at MEDI, Cochin (7 months)

Significant Achievements

- Won IEEE National student level Electronics Design Contest twice in 1999 and 2000.
- Won Individual Excellence Award in Infosys in 2003; Award in Wipro in 2007.
- Made at least two good inventions during my 12 years of career in VLSI and Embedded. Protocol Replicator; Secure JTAG.
- IEEE paper/ASQED on “A systems approach to verification using hardware acceleration” http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5548241&tag=1

Experience

Technical Project Manager for India - Intel Higher Education **Oct 2013 – to-date (1year 9months)**
Employer: Intel, Bangalore as contractor from FICE

- Conducted IOT and Embedded sessions for faculties from IITs, NITs, and other prestigious Govt and academic institutions across India.
- Conducted training sessions at IIT Kharagpur, NIT Tirchy, Uttar Pradesh Technical University, JNTU, Hyderabad.
- Technical Project Management for the Intel Embedded Platform throughout India.
- Technical Content Development for Universities for the Intel Embedded Platform.
- Mentoring Students during Intel's Ideathon Contests.
- Support teams with technical queries for the Intel India Embedded Challenge.
- Technical Interface for the Colleges and Universities including IISc, IIT, NITs, UPTU - Uttar Pradesh Technical University, JNTU – Jawaharlal Nehru Technical University etc.

Chief Architect – Embedded Strartup Company **July 2013 – Dec 2013 (6 months)**
Employer: Self

- Design Embedded Solutions in niche medical areas.
- Develop solution to analyse health based on biomedical signals.

SoC System Level Verification and Validation Engineer **Sept 2010 – July 2013 (2.8 years)**
Employer: Xilinx India Pvt Ltd, Hyderabad, India

- Building AXI based design on FPGA and system level verification and validation of various IPs using C-Based Random Constrained Verification Environment.
- System level Verification and Validation of Zynq (Cortex A9 Processor + FPGA) using C-Based Random Constrained Verification Environment on Palladium and FPGA based Emulator.
- Building and modifying design in one of the FPGAs in a FPGA Emulation Platform

SoC Emulation (System Bringup) Engineer **April 2008 – Sept 2010 (2.5 years)**
Employer: Freescale Semiconductors India Ltd, Noida

- Test-bench development and porting of a multicore(8 core) SoC on Palladium Emulator. Added synthesisable memories like SRAM, DDR2, DDR3 etc. Developed Bus Functional Models(BFM), Benchmarking on the SoC performance, Initial bring up of Linux.
- Worked on Internal Secure Boot Code bring up of an eight core chip on Palladium Emulator at an early stage of integration cycle. Involved going through RTL of various modules involved in boot up, understand interface, work with verification/design team to get the boot up done.
- Lead a team of 3 engineers to bring up a dual core multiprocessor chip on Palladium emulator while working as an individual contributor for a multimillion gate SoC bring up.

- Ported a dual core SoC on palladium. Added RGMII (Ethernet), DIU(Digital Interface Unit), SSI(Audio) BFM and Monitors. Helping software team with scripts to get the benchmarking.
- Worked on porting dual core SoC on Chip-IT-FPGA based emulator. (Multiple FPGA based emulator). Involved in changing code at RTL level for removal of clock gating, adding constraints for the clock etc.

ASIC IP Design/Verification Engineer **July 2007 – March 2008 (8 months)**
Employer: Wipro Technologies, Cochin.
IP (ASIC) Design and Verification of peripherals and system modules.

- Designed IP modules namely JTAG security module in VHDL from specification to synthesis. Having a system level knowledge of the SoC gave me an edge in suggesting changes in the initial specification of the module which later helped in reducing the IP design time.
- Done bug fixes and modifications to complex IPs like Real Time Interrupt module, Data Modification Module, A2D module in VHDL and Verilog. The design cycle involved specification review, RTL coding in Verilog/ VHDL, RTL Checking, Power Analysis, Simulations using VCS, Modelsim, Synthesis, Equivalence Checking, Netlist Simulations etc.
- Involved in functional verification test plan development for IPs. Test cases I suggested in functional plan helped cover several bugs.
- Engineered an idea of developing a generic compiler that helped reduce simulation time and cut down the debug time several folds. I developed a paper on it that was selected at an organisation level and implemented by several projects.

Presilicon Verification on Emulator(Zebu) **May 2005 – June 2007 (2 years)**
Work Location: Texas Instruments, Houston, USA
Employer: Wipro Technologies, USA

- Responsible for the pre-silicon verification of TMS470 series of ARM based microcontrollers on hardware emulator Zebu. As part of it I have developed C/assembly test cases for system and peripheral modules like IceCrusher (debugger) Module, Ram Trace Port (RTP), Data Modification Module (DMM), and Digital Watchdog Timer (DWD), Stepper motor controller. I have also maintained test cases for modules like CAN, SPI, I2C, RTI etc.
- Took up the initiative to convert the existing test suit architecture to one that can be used across a wide platform of SoCs with minimal changes. I developed tcl and perl scripts that generated a database of test cases suitable for a particular SoC.
- Came up with an idea to automate the test regression. I wrote a script that coordinated the IDE (Code composer) running on windows platform and the emulator running on Linux. This helped us run the test cases overnight, thereby reducing the presilicon verification time per SoC. I used Labview as a wrapper to this application.

Development of ARMv7 Architecture Validation Suite. **June 2004 – May 2005 (11 months)**
Employer: Wipro Technologies, Bangalore, India
Client: ARM Ltd, UK

- Developed the implementation plan for the verification of Memory Management and the cache instruction of the ARMv7 Architecture. I developed ARM assembly test cases for verifying the Cache operations and Multiprocessor Shared Exclusive instructions for ARM Cortex series of processors.
- Took up the initiative of developing a web page for our project that contained the link to the various sub projects in the team, the basic documents, the weekly status etc.

Testing of Element/Network Management Software **June 2002 – June 2004(2 years)**
Employer: **Infosys Technologies**, Bangalore, India
Client: Cisco Systems

- Tested the Cisco Element Management Software (EMS) which managed the SONET/SDH switches/add drop multiplexers. I did testing in the circuit provisioning, equipment provisioning, fault monitoring, performance monitoring, SNMP etc and caught the highest number of bugs among my peer levels.
- Developed Unix shell scripts that browsed the log files being written by the server, checked for keywords which suggested error and piped it to another file that could be used for bug reporting. Reporting a bug required server log files to be attached. My script along with the GUI developed in TK allowed easy retrieval of the server logs. This made reporting of the bug very easy and decreased the rejection of bugs for the want of server logs.
- Developed an application in java that would spawn http connections to all the network elements, get the required inventory data and present it in a GUI. This also helped the test engineers reduce the visits to the lab.
- Developed an in-house SNMP snooper with C/ tcl which could be used in place of licensed software for doing the SNMP testing. This reduced the project IT spends on software.

Biomedical Service/ Design Engineer **Feb 2002 – June 2002 (5 months)**
Employer: Nicholas Piramal India Ltd, Kerala, India
Client: Roche, Hitachi

- Serviced and maintained Biomedical Instruments/ Machines like blood analysers, serum analysers in hospitals spread across a geographic location of 1000kms. The work involved debugging computer software, electronic boards, mechanical pumps, robotic arms etc. It gave me a good exposure to customer service and customer interaction.
- To cater to the needs of smaller hospitals I suggested and came up with a low cost design for a water bath based on a PIC microcontroller.

Biomedical Systems Engineer **Sep 2001 – Feb 2002 (6 months)**
Employer: Martins Electronic Devices and Instruments(MEDI), Cochin, India

- Developed the software for UPS that monitored the Voltage/Current/Power etc and display it on an LCD. The design was based on microchip PIC16 microcontroller.

- Designed a single output two input pulse width modulator (PWM) that controlled the duty cycle based on two inputs. The design was based on 8051 based system.