Bapuji Educational Association®
Bapuji Institute of Engineering and Technology, Davanagere
An Autonomous Institute Affiliated to VTU

Third Semester BE/B Tech Degree

MODEL QUESTION BANK

Course: Digital Design and Computer Organization (BCSPCC303)

Q. No.	Question	Marks	CO	RL
	Module 1			
1	**Simplify** the following Boolean expressions to a minimum number of literals: (i) $xy + xy'$ (ii) $(x + y)(x + y')$ (iii) $(x + y)'(x' + y')'$	6	1	2
2	Define duality. State and prove Absorption Theorem.	6	1	3
3	Find the complement of F = wx + yz. Also show that $FF' = 0$ and $F + F' = 1$	7	1	2
4	Find the complement and simplify the Boolean function and also write logic circuit $F = A'B'C' + A'BC$	6	1	2
5	**Simplify** the following Boolean functions, using Karnaugh map method (i) $F(x,y,z) = \sum m(0,1,4,5,6) + d(2,3,7)$ (ii) $F(A,B,C,D) = \sum m(3,7,11,13,14,15)$	7	1	2
6	**Obtain** the **simplified** Boolean expression in SOP using K-map F(A,B,C,D) = A`B` + CD` + ABC + A`B`CD` + ABCD`	6	1	2
7	Find the minimal SOP and minimal POS of the following Boolean function using K-map. $f(a,b,c,d) = \sum m(6,7,9,10,13) + d(1,4,5,11)$	5	1	2
8	**Simplify** the following expression using K-map i) $f(A,B,C) = m0+m2+m5+m6$ ii) $f(A,B,C,D) = \Sigma m(1,3,5,7,9) + \Sigma d(6,12,13)$ iii) $f(A,B,C,D) = \Sigma m(0,2,3,5,6,7,8,10,11,14,15)$	8	1	2
9	For the following function, **find** the minimum sum-of-product solution using Quine- McCluskey method $f(a,b,c,d) = \Sigma m(0,1,2,5,6,7,8,9,10,14)$	8	1	2
10	**Simplify** the following expressions using Karnaugh map. Implement the simplified circuit using the gates as indicated: $(i)\, f(w,x,y,z) = \sum m(1,5,7,9,10,13,15) + d(8,11,14)$ using NAND gates. $(ii)\, f(A,B,C,D) = \Pi M(0,1,2,4,5,6,8,9,12,13,14)$ using NOR gates.	8	1	2
11	**Define** canonical Minterm form and canonical Maxterm form.	6	1	2

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12	**State** and prove De Morgan's Theorems	6	1	3
13	**Realize** the XOR gate using (i) NAND gate (ii) NOR gate.	6	3	3
14	**Identify** the prime implicants and essential prime implicants of the following functions: f(A,B,C,D) = $\sum m$(1,3,4,5,10,11,12,13,14,15) f(W,X,Y,Z)= $\sum m$(0,1,2,5,7,8,10,15)	10	1	3
15	**List** all Postulates and Theorems available in Boolean algebra?	6	1	1
	Module 2			
1	**Define** multiplexer. **Show how** to make 16:1 MUX using four 4:1 MUX and three 2:1 MUXes	10	2	2
2	**Implement** the following function using 8:1 MUX. Use D as Map Entered Variable. F(A,B,C,D)= Σm(1,2,3,7,9,10,11,13,15)	8	2	3
3	Define Latch.with neat diagram, explain S-R Latch using NOR gate. Derive characteristics equation	8	2	1
4	**Explain** the working of Four-bit adders using 4-full Adders.	6	2	2
5	**Define** priority encoder. Design 4:2 priority encoder with necessary diagram	6	2	1
6	**Write** difference between sequential circuits and combinational circuits.	6	2	2
7	**Write** Verilog program for demultiplexer, multiplexer, flip-flops.	10	2	1
8	**Differentiate** between Latches and flip-flops	6	2	2
9	**Explain** the working of Master Slave J K flip flop with a logic diagram.	6	2	2
10	**Explain** the operation of D, T, SR, and JK latches.	8	2	2
11	**Mention** the differences between decoder and demultiplexer.	6	2	2
12	**Write** the verilog program to implement Full Adder and Full Subtractors circuits	10	2	2
13	**Write** the characteristics table and equations of SR, D and T Flip Flops	8	2	1
14	**Construct** a 4:1 multiplexer using only a 2:1 multiplexer and also write a Verilog program.	8	2	3

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15	**Design** 4:1 multiplexer for Boolean function f(A,B,C)=Σ(0,2,3,5,6,7)			
	Module 3			
1	**Write** one address, two address, and three address instructions to carry out C← [A] + [B].	**5**	**3**	**3**
2	**Explain** the basic operation concepts of the computer with a neat diagram.	**8**	**3**	**2**
3	**Explain** a) Processor Clock, b) Basic performance equation, c) Clock rate d) Performance measurement	**8**	**3**	**2**
4	**Write** ALP of adding a list of n numbers using indirect addressing mode.	**5**	**3**	**3**
5	Define addressing mode? List the types of addressing modes. **Describe** the types of addressing modes with an example.	**8**	**3**	**2**
6	**Explain** the following: (i) Byte addressability (ii) Big-endian assignment (i) Little-endian assignment	**8**	**3**	**2**
7	**Using** two-address and three-address instruction, show how X = (A+B)*(C+D) will be converted.	**8**	**3**	**3**
8	**Explain** the basic operational concepts between the processor and memory	**8**	**3**	**2**
9	**With** a neat diagram, describe the functional units of a computer	**8**	**3**	**2**
10	**With** a neat diagram, discuss the operation concepts in a computer highlighting the role of PC, MAR, MDR & IR	**8**	**3**	**2**
11	Show how below expression will be executed in one address, two address, zero address and three address processor in an accumulator organization X=(A * B)+(C * D)	**8**	**3**	**1**
12	**Write** a note on Single bus structure	**5**	**3**	**2**
	Module 4			
1	Draw a neat block diagram of memory hierarchy in a computer system, **Discuss** the variation of size, speed and cost per bit in the hierarchy.	**10**	**4**	**2**
2	What is bus arbitration? **Explain** the arbitration methods with neat diagrams.	**10**	**4**	**2**
3	What is DMA Bus arbitration? **Explain** different bus arbitration techniques.	**10**	**4**	**2**
4	With neat sketches, **explain** various methods for handling multiple interrupt requests raised by multiple devices.	**10**	**4**	**2**
5	What is cache memory? **Explain** the different mapping functions used in cache memory.	**10**	**4**	**2**
6	**Explain** interrupt and interrupt hardware. State steps in enabling and disabling of interrupts.	**8**	**4**	**2**

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7	**Explain** the operations using registers in a DMA interface	8	4	2
8	**Explain** the following: a) interrupt service routine b) interrupt latency c) interrupt disabling.	8	4	2
9	With a neat diagram **explain** various methods for handling multiple interrupt requests.	10	4	2
10	**Explain** how interrupt requests from several I/0 devices can be communicated to a processor through a single INTR line.	10	4	2
11	**Explain** memory map I/O and I/O interface for an input device with a diagram.	10	4	2
12	With a neat diagram **explain** the concept of accessing I/O devices	8	4	2
13	**Explain** centralized bus arbitration	8	4	2
14	**Explain** synchronous bus transfer during input operation	8	4	2
15	**Explain** the following with respect to interrupts with diagram i) Vectored interrupt ii) Interrupt nesting iii) Simultaneous request	8	4	2
	Module 5			
1	**Explain** the single-bus organization of computers and fundamental concepts with a neat diagram.	10	5	2
2	**Write** and **explain** the control sequence for execution of the instruction Add (R3), R1.	10	5	3
3	**Explain** with an example the different types of hazards that occur during pipelining.	10	5	2
4	**Write** and **explain** the control sequence for the execution of an unconditional branch instruction.	10	5	3
5	With the help of a timing diagram **explain** the 4-stage pipeline.	8	5	2
6	**Write** and **explain** the control sequence for the instruction Add R1, R2, R3.	10	5	3
7	**Explain** the process of fetching a word from memory in processor.	10	5	2
8	**Describe** how an ALU perform on arithmetic and logic operation along with input gating diagram.	10	5	2

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9	With the help of diagram **explain** the concept of register transfer and fetching of words from memory.	10	5	3
10	**Explain** the role of cache memory and pipeline performance.	10	5	2
11	**Describe** how does execution of complete instruction carried out.	10	5	3
12	Define pipeline. **Explain** the performance of pipeline with an example,	10	5	2