	c	Define decoder. Describe the working principle of a 3:8 decoder. Draw the logic diagram of the 3:8 decoder with enabled input. Realize the following Boolean expressions using a 3:8 decoder and multi-input OR gates: $F1(A, B, C) = \sum m(1, 3, 7)$ $F2(A, B, C) = \sum m(2, 3, 5)$.	
Module-3			
Q. 05	a	Write one address, two address, and three address instructions to carry out C← [A] + [B].	
	b	Explain the basic operation concepts of the computer with a neat diagram.	
	c	Explain a) Processor Clock, b) Basic performance equation, c) Clock rate d) Performance measurement	
OR			
Q. 06	a	Write ALP of adding a list of n numbers using indirect addressing mode	
	b	What is an addressing mode? Explain the different addressing modes. With an example for each.	
	c	Explain the following: (i) Byte addressability (ii) Big-endian assignment (i) Little-endian assignment.	
Module-4			
Q. 07	a	Draw a neat block diagram of memory hierarchy in a computer system. Discuss the variation of size, speed and cost per bit in the hierarchy.	
	b	What is DMA Bus arbitration? Explain different bus arbitration techniques.	
OR			
Q. 08	a	With neat sketches, explain various methods for handling multiple interrupt requests raised by multiple devices.	
	b	What is cache memory? Explain the different mapping functions used in cache memory.	
Module-5			
Q. 09	a	Explain the single-bus organization of computers and fundamental concepts with a neat diagram.	
	b	Write and explain the control sequence for execution of the instruction Add(R3), R1	
OR			
Q. 10	a	Explain with an example the different types of hazards that occur during pipelining.	
	b	Write and explain the control sequence for the execution of an unconditional branch instruction.	

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs attained by every bit of question.

Note: 01. Answer any FIVE full questions, choosing at least ONE question from each MO

		Module -1	*Bloom Taxonor Level
Q.01	a	Demonstrate the nonassociativity of the NOR gate	L2
	b	Design a car safety alarm circuit diagram. The system considers four inputs: door (D), key (K), seat pressure (P) and seat belt (B). The input is considered HIGH (1) if the door is closed, the key is in, the driver is on the seat, or the seat belt is fastened. The alarm (A) should sound with two conditions as stated below: The door is not closed, and the key is in. The door is closed, the key is in the driver's seat, and the seat belt is not closed. (a) Construct a truth table for the system based on input arrangement D, K, P, B with A as an output (b)Design a Karnaugh map to verify the simplified expression (c) Draw the simplified circuit using NOR gates only	L3
	c	With an example explain the working of Test Bench in Verilog.	L2
		OR	
Q.02	a	Demonstrate the positive and negative logic signal	L2
	b	A digital system is to be designed in which the month of the year is given as I/P in four-bit form. The month of January is represented as '0000', February as "0001" and so on. The output of the system should correspond to the input of the month containing 31 days, or otherwise, it is '0'. Consider the excess number in the I/P beyond 1011' as don't care condition: (i) Write truth table, SOP Em and POSIIM form (ii) Simplify for SOP using K-map (iii) Realize using basic gates	L3
	c	What is User-Defined Primitives in Verilog? What are the general rules for UDP? Explain with an example HDL for user defined primitive. Draw the Schematic for the Circuit with UDP_02467	L2
		Module-2	
Q. 03	a	Differentiate Latches and Flip-Flops.	L2
	b	Explain the working of Four-bit adders using 4-full Adders.	L3
	c	Implement Y (A, B, C, D) = $\sum$m (0, 1, 6, 7, 8, 9, 10, 11, 12, 14) using 16-to-1 multiplexer and 8-to-1 multiplexer.	L3
		OR	
Q.04	a	Explain different modeling styles used to write the code in VERILOG with an example.	L2
	b	Design a BCD-to-excess-3 code converter.	

		Module – 4
Q.7	a.	Explain the I/O interfacing and I/O device with computers.
	b.	What is Bus Arbitration? Explain types of bus arbitration.
		OR
Q.8	a.	What is cache memory? Explain the different type of cache mapping function.
	b.	Explain basic concepts involved for memory structures of computers.
		Module – 5
Q.9	a.	Explain with neat diagram of single bus organization.
	b.	Explain complete execution steps for instruction ADD (R3), R1.
		OR
Q.10	a.	Explain execution of complete instruction carry out.
	b.	What is pipeline? Explain with example of pipeline performance.

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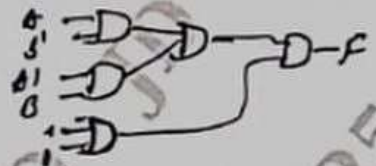
BCS302

Third Semester B.E./B.Tech. Degree Supplementary Examination
June/July 2024
Digital Design and Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: **1.** ***Answer any FIVE full questions, choosing ONE full question from each module.***
2. ***M : Marks , L: Bloom's level , C: Course outcomes.***

		Module – 1	M	L	C
Q.1	a.	Simplify the Boolean function i) $F(x, y, z) = \Sigma(2, 3, 4, 5)$ ii) $F(x, y, z) = \Sigma(3, 4, 6, 7)$	10	L3	CO1
	b.	Obtain a minimum product of sum with a Karnaugh Map $F(w, x, y, z) = x'z' + wyz + w'y'z' + x'y$	10	L3	CO1
		OR			
Q.2	a.	Define multiplexer. Explain 2 to 1 line multiplexer.	10	L2	CO1
	b.	Write the verilog code and time diagram for the given circuit with propagation delay where the AND, OR gate has a delay of 30ns and 10ns.  Fig Q2(b)	5	L2	CO1
	c.	Explain implementation of full adder with logic diagram.	5	L3	CO1
		Module – 2			
Q.3	a.	Explain with neat diagram and 4 input priority encodes.	10	L2	CO2
	b.	Explain 2 : 4 time decoder with help of logic diagram and truth table.	10	L2	CO2
		OR			
Q.4	a.	Define Latch. Explain S-R flip flop based on NOR Gate with neat diagram.	10	L2	CO2
	b.	Explain clocked D flip flop with neat diagram.	10	L2	CO2
		Module – 3			
Q.5	a.	With neat diagram, explain the basic operational concepts of computers.	10	L2	CO3
	b.	Write a program to evaluate arithmetic statement $Y = (A + B) * (C + D)$ using 3 address, 2 address, one address and zero address instruction.	10	L3	CO3
		OR			
Q.6	a.	Describe the concept of Blanch instruction with example.	10	L2	CO3
	b.	Explain 5 addressing modes with example.	10	L2	CO3

		Module – 3		
Q.5	a.	Explain four types of operation performed by computer with an example.	10	L
	b.	Show how below expression will be executed in one address, two address zero address and three address processor in an accumulator organization $X = (A * B) + (C * D)$.	10	L
		OR		
Q.6	a.	What is addressing mode? Explain different types of addressing mode with an examples.	10	L
	b.	With a neat diagram, explain basic operational concepts of a computer.	10	L
		Module – 4		
Q.7	a.	Explain the following with respect to interrupts with diagram. i) Vector interrupt ii) Interrupt nesting iii) Simultaneous request.	10	L
	b.	Explain Direct Memory Access with a neat diagram.	10	L
		OR		
Q.8	a.	What is Bus arbitration? Explain different types of bus arbitration.	10	L
	b.	Discuss different types of mapping functions of coaches.	10	L
		Module – 5		
Q.9	a.	Draw and explain the single-bus organization of the data path inside a processor.	10	L
	b.	List out the actions needed to execute the instruction ADD (R3), R1 write and explain the sequence of control steps for the execution of the same.	10	L
		OR		
Q.10	a.	Analyze how does execution of a complete instruction carry out.	10	L4
	b.	What is pipeline? Explain the performance of pipeline with an example.	10	L4

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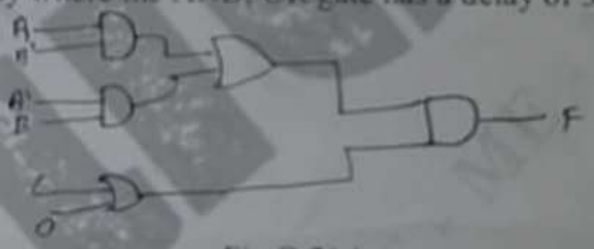
Third Semester B.E./B.Tech. Degree Examination, Dec.2023/Jan.2024
Digital Design and Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Obtain a minimum product of sums with a Karnaugh map. $F(w, x, y, z) = x' z' + wyz + w' y' z' + x' y$.	10	L3	CO1
	b.	Find the minimum sum of products for each function using a Karnaugh map i) $F_1(a, b, c) = M_0 + M_2 + M_5 + M_6$ ii) $F_2(d, e, f) = \sum m(0, 1, 2, 4)$ iii) $F_3(r, s, t) = rt' + r's' + r's$	10	L3	CO1
		OR			
Q.2	a.	Identify the prime implicants and essential prime implicants of the following functions: i) $f(A, B, C, D) = \sum (1, 3, 4, 5, 10, 11, 12, 13, 14, 15)$ ii) $f(W, X, Y, Z) = \sum(0, 1, 2, 5, 7, 8, 10, 15)$.	10	L3	CO1
	b.	Write the verilog code for the given expression using dataflow and behavioral model where $Y = (AB' + A'B) (CB + AD) (AB'C + AC)$.	5	L2	CO1
	c.	Write the verilog code and time diagram for the given circuit with propagation delay where the AND, OR gate has a delay of 30ns and 10ns.  Fig.Q.2(c)	5	L2	CO1
		Module – 2			
Q.3	a.	What is Latch? With neat diagram, explain S-R latch using NOR gate. Derive characteristics equation.	10	L3	CO2
	b.	What is priority encoder? Design 4:2 priority encoder with necessary diagrams.	10	L3	CO2
		OR			
Q.4	a.	Design and explain four bit adder with carry look ahead.	10	L3	CO2
	b.	What is multiplexer? Design 9:1 mux using 2:1 mux.	10	L3	CO2

	b.	Illustrate an indexed addressing mode with a assembly language program to find the sum of the Test 1, Test 2 and Test 3 scores of the N number of students.	10	L2	CO3
		Module – 4			
Q.7	a.	Explain Hardware interrupt, enabling/disabling of interrupts and sequence of events in handling interrupt request from a single device.	10	L2	CO4
	b.	Explain memory mapped I/O and I/O interface for an input device with a diagram.	10	L2	CO4
		OR			
Q.8	a.	Describe DMA with its register and controllers.	10	L2	CO4
	b.	Explain the effect of size, cost and speed in memory Hierarchy.	10	L2	CO4
		Module – 5			
Q.9	a.	Explain the process of Fetching word from memory in processor.	10	L2	CO5
	b.	With a diagram, explain the single bus organization of the data path inside a processor.	10	L2	CO5
		OR			
Q.10	a.	Describe how an ALU perform on arithmetic and logic operation along with input gating diagrams.	10	L2	CO5
	b.	Explain the complete set of operations involved in executing the instruction Add (R_3) R^1 along with control sequence.	10	L2	CO5

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CBCS SCHEME

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BCS302

Third Semester B.E./B.Tech. Degree Examination, June/July 2024
Digital Design and Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Reduce the following Boolean expressions to the minimum number of literals. i) $x(x' + y)$ ii) $x + x'y$ iii) $(x + y)(x + y')$ iv) $xy + x'z + yz$ v) $(x + y)(x' + z)(y + z)$	10	L3	CO1
	b.	Determine the minimum SOP form using Karnaugh Map $F = A'B'C' + B'CD' + A'BCD' + AB'C'$.	10	L3	CO1
		OR			
Q.2	a.	Simplify the Boolean function $F(w, x, y, z) = \Sigma(1, 3, 7, 11, 15)$ which has the don't care conditions $d(w, x, y, z) = \Sigma(0, 2, 5)$	10	L3	CO1
	b.	Simplify and implement the following Boolean function using NAND gates $F(x, y, z) = (1, 2, 3, 4, 5, 7)$.	10	L3	CO1
		Module – 2			
Q.3	a.	Implement the design of combinational circuit BCD and excess 3 code converter.	10	L2	CO2
	b.	Implement full adder circuit using 3:8 decoders.	10	L2	CO2
		OR			
Q.4	a.	With Truth table and K-map simplification, implement the full adder with basic gates and using two half adders an OR gate.	10	L2	CO2
	b.	Realize the Boolean function using 8:1 multiplexer $F(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$.	10	L2	CO2
		Module – 3			
Q.5	a.	Explain Bus structure with diagram, explain how different peripherals connected to the bus.	10	L2	CO3
	b.	Explain in detail about the word alignment of a machine (microprocessor based systems) what is the consecutive addresses of aligned words for 16, 32 and 64 bit word length of the machine? Give consecutive address for each of the following specified above.	10	L2	CO3
		OR			
Q.6	a.	Write a note on ; i) Register Transfer Notation (RTN) ii) Assembly Language Notation.	10	L2	CO3

	b.	Mention four types of operations to be performed by instructions in a computer. Explain the basic types of instruction formats to carry out. $C \leftarrow [A] + [B]$	10	L2	CO3
		Module – 4			
Q.7	a.	With a neat diagram, explain the concept of accessing I/O devices.	10	L2	CO4
	b.	What is bus arbitration? Explain centralized and distributed arbitration method with a neat diagram.	10	L2	CO4
		OR			
Q.8	a.	With neat sketches, explain various methods for handling multiple interrupts requests raised by multiple devices.	10	L2	CO4
	b.	What is cache memory? Explain any two mapping function of cache memory.	10	L2	CO4
		Module – 5			
Q.9	a.	Draw the single bus architecture and write the control sequence for execution of instruction ADD (R_3), R_1.	10	L3	CO5
	b.	With suitable diagram, explain the concept of register transfer and fetching of word from memory.	10	L2	CO5
		OR			
Q.10	a.	With a neat diagram, explain the flow of 4-stage pipeline operation.	10	L2	CO5
	b.	Explain the role of cache memory and pipeline performance.	10	L2	CO5

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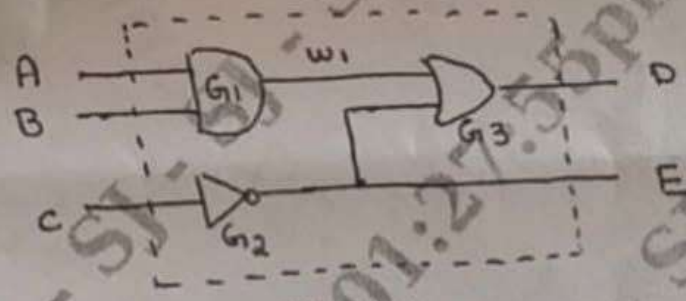
Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

			M	L	C
		Module – 1			
Q.1	**a.**	Determine the complement of the following function: (i) $F = xy' + x'y$ (ii) $F = x'yz' + x'y'z$	**06**	**L3**	**CO1**
	b.	Describe map method for three variables.	**04**	**L2**	**CO1**
	c.	Apply K map technique to simplify the following function: (i) $F(x, y, z) = \Sigma(0, 2, 4, 5, 6)$ (ii) $F(x, y, z) = x'y + yz' + y'z'$	**10**	**L3**	**CO1**
		OR			
Q.2	**a.**	Apply K map technique to simplify the function : $F(w, x, y, z) = \Sigma(1, 3, 7, 11, 15)$ and $d(w, x, y, z) = \Sigma(0, 2, 5)$	**06**	**L3**	**CO1**
	b.	Determine all the prime implicants for the Boolean function F and also determine which are essential $F(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$	**10**	**L3**	**CO1**
	c.	Develop a verilog gate-level description of the circuit shown in Fig.Q2(c).  Fig.Q2(c)	**04**	**L3**	**CO1**
		Module – 2			
Q.3	**a.**	Explain the combinational circuit design procedure with code conversion example.	**10**	**L2**	**CO2**
	b.	Design a full adder circuit. Also develop data flow verilog model for full adder.	**10**	**L3**	**CO2**
		OR			
Q.4	**a.**	Describe 4 × 1 MUX with block diagram and truth table. Also develop a behavioral model verilog code for 4 × 1 MUX.	**10**	**L2**	**CO2**
	b.	What are storage elements? Explain the working of SR and D latch along with logic diagram and function table.	**10**	**L2**	**CO2**
		Module – 3			
Q.5	**a.**	Explain the basic operational concepts between the processor and memory.	**10**	**L2**	**CO3**
	b.	Describe the following: (i) Processor clock (ii) Basic performance equation (iii) Clock rate (iv) SPEC rating	**10**	**L2**	**CO3**
		OR			
Q.6	**a.**	Define addressing mode. Explain any four types of addressing mode with example.	**10**	**L2**	**CO3**