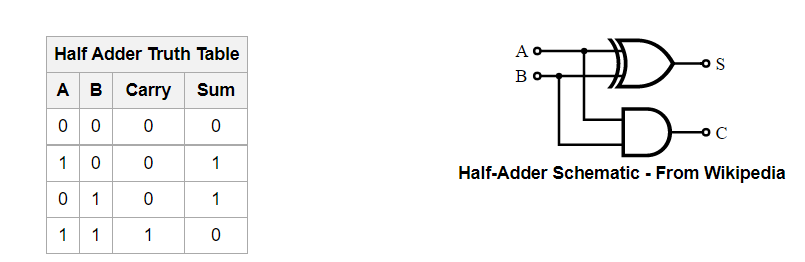
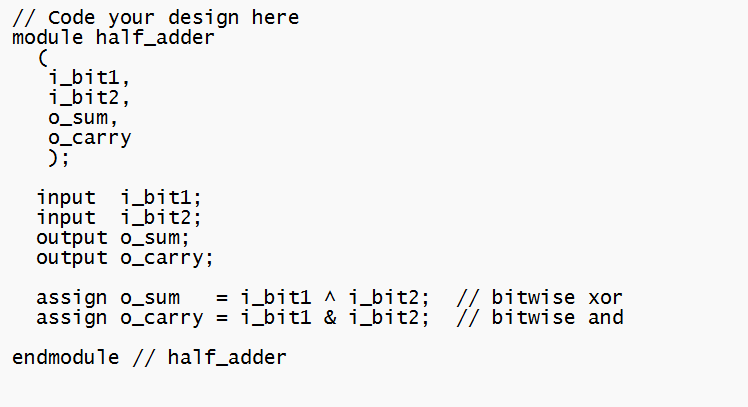
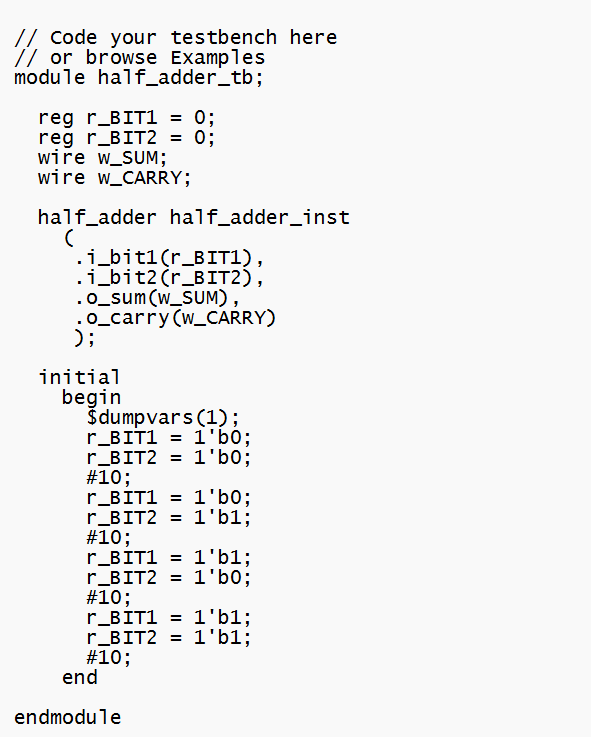
**Experiment 3**

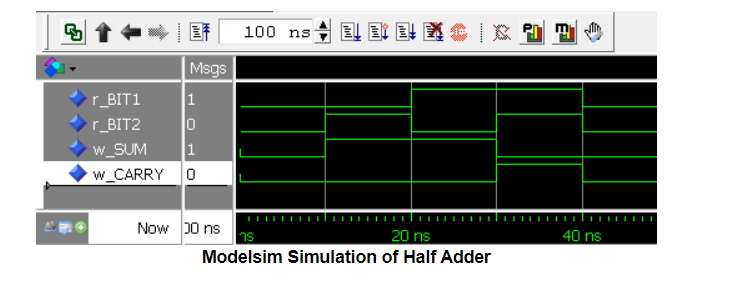
**Write an HDL code to describe the functions of a Half Adder and full adder**





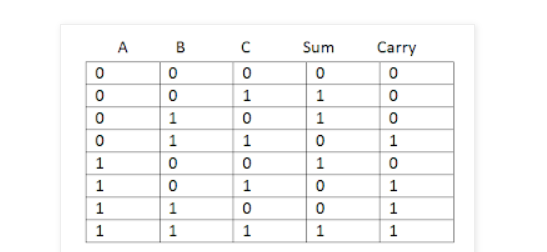
Test bench



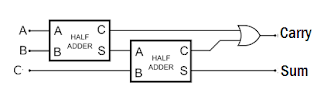


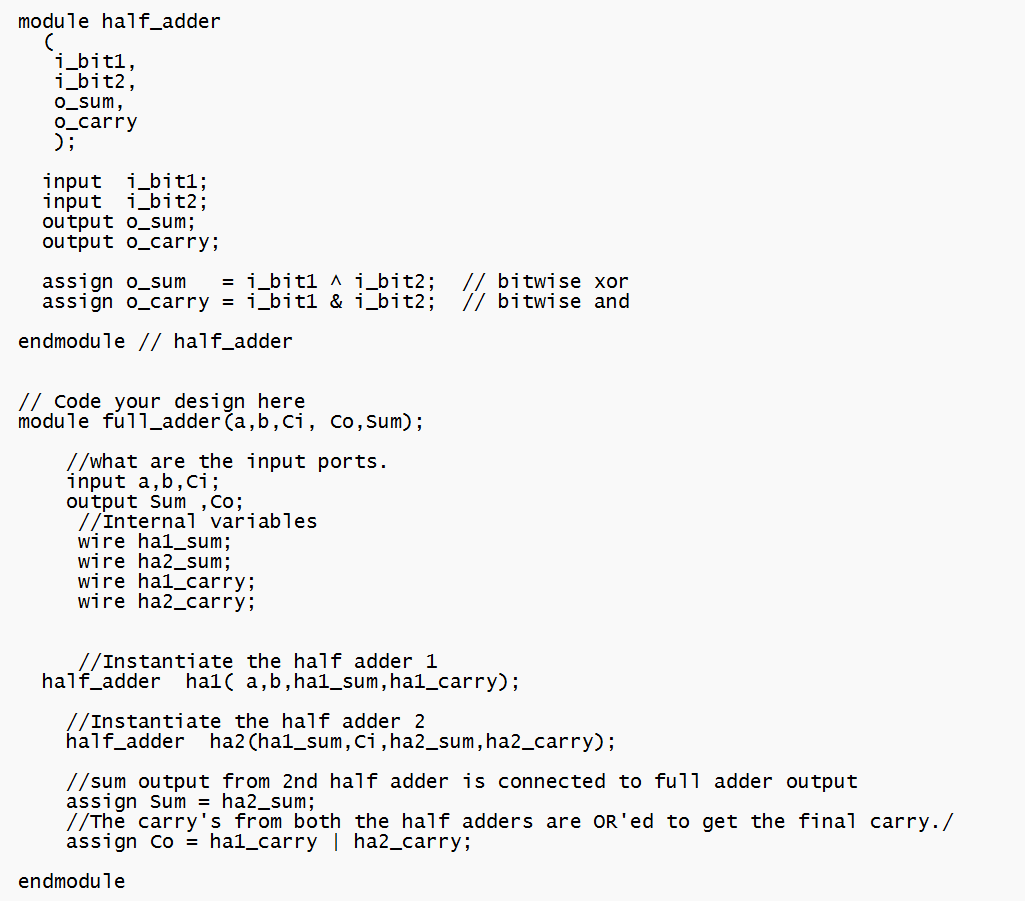
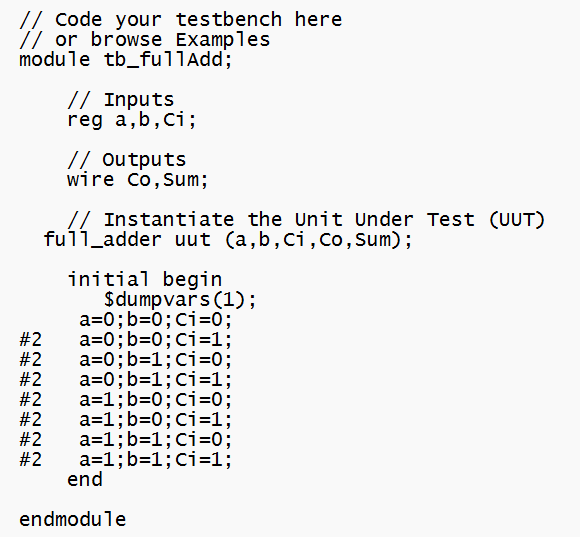
**Full adder using half adder**

Full adder Truth table



A Full adder can be implemented using half adders as shown below:

[](https://3.bp.blogspot.com/-ap9lRxQ4jDM/VicuhKzce8I/AAAAAAAAAOE/DAQD3B9J8pU/s1600/1.png)

The Verilog code can be written in structural modelling for the above circuit.  
 **Testbench Code for Full Adder:**  
 ****