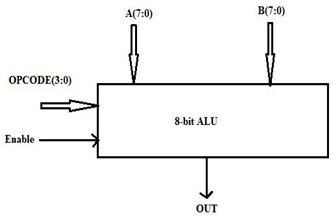
Experiment 4

Write a model for n bit ALU using the schematic diagram shown below



AIM:To design a verilog HDL for designing ALU using behaviral model. TOP MODULE

