

# COA - Assignment - 1

Aadithyan Raju  
AM.EN: V4 CSE 21301

1) ~~0000~~  $0x(00041440)$

R-format

2)  $sw, \$t_1, 4(\$t_0)$   
 $\begin{matrix} 43 & 9 & 8 \end{matrix}$

101011 01000 01001 0000 0000 0000 0100

$0x(AD090004)$

3)  $\$S2 = 0x(ABCD6789)$

a)  $0x(BCD67890)$

b)  $0x(00ABCD67)$

4)

a)  $\$t_2 = 0001\ 0001\ 0100\ 0010\ 0011\ 0100\ 1000\ 0001$

0100 0100 0110 1001 0000 0010 0000 0000  
 $\begin{matrix} 4 & 4 & 6 & 9 & 0 & 2 & 0 & 0 \end{matrix}$

$\$t_0 = 0x(\underline{44690200})$

b)  $131 = 10000011$

$\$t_0 = (\underline{44690283})_{16}$

c)  $\$t_1 = 0x(00123229)$

$\$t_2 = 0x(11223481)$

$\$S_0 = 0x(\underline{00023001})$

d)  $\$t_3 = 0x(4469810)$

$\$S_6 = 0x(00023001)$

$\$S_0 = 0x(\underline{4465A811})$

e)  $\$t_0 = 0x(BB9A77EF)$

f)  $\$t_0 = 0x(017734EF)$

0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

## 5) Moore's Law

no. of transistors on a microchip doubles every 2 years.

### 6) i) Simplicity & Regularity

- a) fixed sized instructions
- b) small no. of instruction formats
- c) opcode is always the first 6 bits.
- d) Simplicity & regularity to perform as good as it is in high level language.

### ii) Smaller is faster

- a) limited instruction set.
- b) limited no. of registers & register file.
- c) limited no. of addressing mode.

### iii) Make common case fast.

- a) Allows instruction to contain immediate operands
- b) Arithmetic operands from register file

### iv) Good design demands good compromises

- a) All MIPS instructions are of same size, i.e., same instruction length.
- b) 32 bits long
- c) This has forced the designs to provide 3 different formats, R, I, S types to meet the requirements.

→ 16 → transfers one byte of data from main memory to register.

→ 86 → transfers lowest byte of data from register to main memory.

8)

8) a) R format

opcode	rs	rt	rd	sa	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

⇒ sll, add

I format

opcode	rs	rt	immediate
(6 bits)	(5 bits)	(5 bits)	(16 bits)

⇒ lw, beq, andi, sw

J format

opcode	Jump
6 bits	26 bits

2) ~~3~~

b) loop: sll \$t1, \$s2, 2	2000	0x (0012 4880)
add \$t1, \$t1, \$s3	2004	0x (0133 4820)
lw \$t0, 0(\$t2)	2008	0x (8D48 6000)
beq \$t1, \$t0, finish	2012	0x (1928 6002)
andi \$s2, \$s2, 1	2016	0x (2252 0001)
j loop	2020	0x (6800 00F4)
finish: add \$s4, \$t0, \$t0	2024	0x (0168 A020)
sw \$s4, 0(\$t2)	2028	0x (AD54 0000)