

# Multiscale, Multiphysics Modeling and Simulation of Single-Event Effects in Digital Electronics: From Particles to Systems

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**Abstract**—This article aims to provide a survey of modeling and simulation of single-event effects (SEEs) in digital electronics at device, circuit, and system levels. It primarily focuses on the specific multiscale, multiphysics, multidomain nature of SEEs and on the main underlying physical mechanisms that lead to the occurrence of single events in digital devices and circuits. This article addresses different ways to model and simulate both in space and time this complex sequence of mechanisms from the particle–material interaction up to the electrical response of a given electronics device, circuit, or system. It highlights the specific features of each methodology and discusses simulation requirements, code, or model inputs and expected outputs.

**Index Terms**—Circuit simulation, compact models, device modeling and simulation, digital circuits, digital single-event transient (SET), radiation effects, radiation transport codes, single-event effects (SEEs), soft error rate (SER), transport models.

## I. INTRODUCTION

SINGLE-EVENT effects (SEEs) designate a set of multiphysics and multiscale phenomena that take place in a microelectronic device, component, subsystem, or system (digital or analog) impacted by a single energetic particle and that result in any measurable or observable change in its state, operation, or performance. SEEs were reported for the first time in the 1950s during nuclear weapon testing and observed in space electronics from the 1960s [1], [2], [3], [4]. Terrestrial cosmic-rays (atmospheric radiation) and traces of radioactive impurities (alpha-particle emitters) in circuit materials were identified later in the 1970s–1980s as the two major sources of SEEs at ground level [5], [6], [7], [8], [9], [10]. In the 1990s, the interaction of low-energy (thermal) cosmic-ray-induced neutrons with the  $^{10}\text{B}$  isotope potentially present in device materials was also identified as another major source of SEEs [11].

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In recent decades, the growing significance of SEEs in the reliability of modern electronics can be attributed to the extreme miniaturization of complementary metal–oxide–semiconductor (CMOS) devices combined with the increase of the circuit integration (i.e., the number of transistors per unit area) [12], [13], [14]. As feature-size scales down, the per-bit cross-sectional area exposed to an incoming ionizing particle decreases. This is accompanied by a reduction in the volume where energy is deposited by the traversing particle and by an increase of the particle’s region of influence within the affected device, cell, or circuit [12]. The ongoing reduction of the critical charge as devices shrink [12], [14], [15], [16] has made them increasingly susceptible to natural or artificial radiation in general and down to the most tenuous levels, as encountered, for example, at terrestrial ground level.

Alongside the experimental aspects, modeling and simulation have long been used for better understanding the effects of radiation on the operation of devices and circuits [17], [18], [19], [20], [21], [22]. Because of its increasingly predictive capacity, which goes hand in hand with the power of computational tools and advances in physical modeling, simulation offers the possibility of reducing radiation experiments and testing hypothetical devices or conditions, which are not feasible (or not easily measurable) by experiments. For the study of SEEs in future devices for which experimental investigation is still limited, numerical simulation is an ideal investigation tool for providing physical insights and predicting the operation of future devices expected at the end of the roadmap [13], [21].

As CMOS technologies move down to the nanometer scale and circuits become more complex, it becomes necessary to adopt a truly multiphysics and multiscale simulation approach to capture the essential physics of SEEs, from the particle–matter interaction to the response of a digital circuit or system. This raises several challenges in the development of powerful simulation tools and the management of interactions between simulation levels. In brief, multiscale simulations can be linked in two ways: 1) by incorporating direct links between input–output flows of different simulation types or 2) by transforming the results of a given simulation level into a simplified form and feeding them as input to another simulation level. A hierarchical structure of the interactions between simulation levels offers advantages in terms of efficiency, while also providing design insights [23].

This article deals with this important issue of modeling and simulation of SEEs in digital electronics at device, circuit, and system levels. This article primarily addresses key topics related to single-event transients (SETs) and single-event upsets (SEUs) occurring in digital devices and circuits. An SET is a temporary and unintended voltage or current fluctuation that occurs when ionizing particles, such as cosmic rays or high-energy particles from nuclear reactions, interact with the semiconductor materials inside electronic devices [24], [25]. These interactions can disrupt the normal operation of digital circuits, causing a momentary change in the logic state of a device/circuit or an operation interrupt. The other numerous effects induced by single events in electronics are only briefly mentioned at the beginning of this article to provide an overview of SEEs and to better contextualize the topics discussed here. This article is organized as follows. Section II primarily focuses on the specific multiscale, multiphysics, multidomain nature of SEEs and on the main underlying physical mechanisms that lead to the occurrence of soft errors (SEs) in digital circuits. In Section III, a meticulous review will address different ways to model and simulate both in space and time this complex sequence of mechanisms from the particle–material interaction up to the electrical response of a given circuit. Section IV explores in detail the main approaches for the modeling and simulation of SEEs at device and circuit cell levels such as sensitive volume (SV)-based models, the so-called diffusion-collection method, the random-walk drift–diffusion (RWDD) approach, and technology computer-aided design (TCAD) simulation. In Section V, we examine a few approaches of mixed-mode and circuit simulation used to investigate SEEs at the circuit level. Section VI presents the modeling of the soft error rate (SER) as well as different approaches of critical charge modeling in both memory circuits and combinational logic. Finally, in Section VII, we briefly review the modeling and simulation approaches of SEEs at the system level.

## II. UNDERSTANDING THE NATURE OF THE SEE PROBLEM

### A. Definition and Classification

We start with a general definition of an SEE, followed by a classification of different types of SEEs.

- 1) An SEE is initiated by the passage of a single energetic particle through the volume of an electronic device.
- 2) The striking particle may be an elementary particle (proton, neutron, muon, electron, ...), or an ion (alpha particle and heavy ion).
- 3) An SEE is created if the result of the interaction of the particle with the device or circuit interferes with its electrical operation, causing or not an observable functional error.
- 4) An SEE can result in a reversible (nonpermanent) or irreversible (permanent) change in device or circuit operation. In the first case, the error is recoverable and is qualified as an “SE”; in the second case, the error is generally the result of an unrecoverable damage and one speaks about “hard error.”

The recent revision of the JEDEC standard JESD89B [24] proposes a definition and a classification of different types of

SEEs, resulting from several years of discussion and effort to try to standardize this ensemble of technical terms. These are summarized in Fig. 1 and their extensive definitions, according to the JEDEC standard, are given as follows (all quotes correspond to definitions directly taken from [24]). SEs include SETs, SEUs, single-bit upsets (SBUs), single-cell upsets (SCUs), multiple-bit upsets (MBUs), multiple-cell upsets (MCU), and SETs that, if latched, become SEU [24].

- 1) *SEU*: “A nonpermanent error caused by a state change of a latch, flop, memory cell, or other bistable element from the particle strike. The energetic strike can occur directly on the circuit element or propagate to that circuit (see SET).”
- 2) *SBU*: “An SEU in which the observed error is a single logical or data bit.”
- 3) *SCU*: “An SEU where only one cell or logic element (latch, flip-flop (FF), etc.) is upset (compared to MCU).”
- 4) *MBU*: “A single event that induces upset of multiple cells where two or more of the upsets occur in the same logical word [or frame/column/sector, etc., for field-programmable gate arrays (FPGAs)]. NOTE: An MBU is a logical manifestation of a single event.”
- 5) *MCU*: “A single event that induces several cells (e.g., memory cells or FFs) in an integrated circuit (IC) to flip their state at one time.”
- 6) Single-event functional interrupt (SEFI): “A single event that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not result in permanent damage (i.e., hard error). Note that an SEFI is often associated with an SBU/MBU in a control bit or register, whereas a single-event latchup (SEL) is caused by the turn-on of a parasitic thyristor. Many SEFI events can be cleared with a component reset operation. In cases where resetting some configuration registers requires a complete power cycle of the device, it can be difficult to distinguish between an SEFI and an SEL (see the following). An SEFI event does not necessarily result in an extended increase in operational current like a high-current SEL.”
- 7) *SET*: “A time-dependent radiation-induced spurious current or voltage signal on a circuit node. A digital SET (DSET) occurs when an SET in a combinational logic gate (along data or control paths) propagates and is latched to create an error in the output of a sequential element. An analog SET (ASET) is a spurious signal in an analog circuit (e.g., a spurious signal on an input–output (IO) pin) that causes an erroneous output.”

Single-event hard errors (SEHEs) include single-event gate oxide ruptures (SEGRs), single-event dielectric ruptures (SEDRs), single-event burnouts (SEBs), and destructive SEL [24].

- 1) *SEGR*: “An event in which a single energetic particle strike results in a breakdown and subsequent conducting path through the gate oxide of a metal–oxide–semiconductor (MOS) transistor.”
- 2) *SEDR*: “An event in which a conducting path is created in a dielectric material from a single energetic particle strike.”

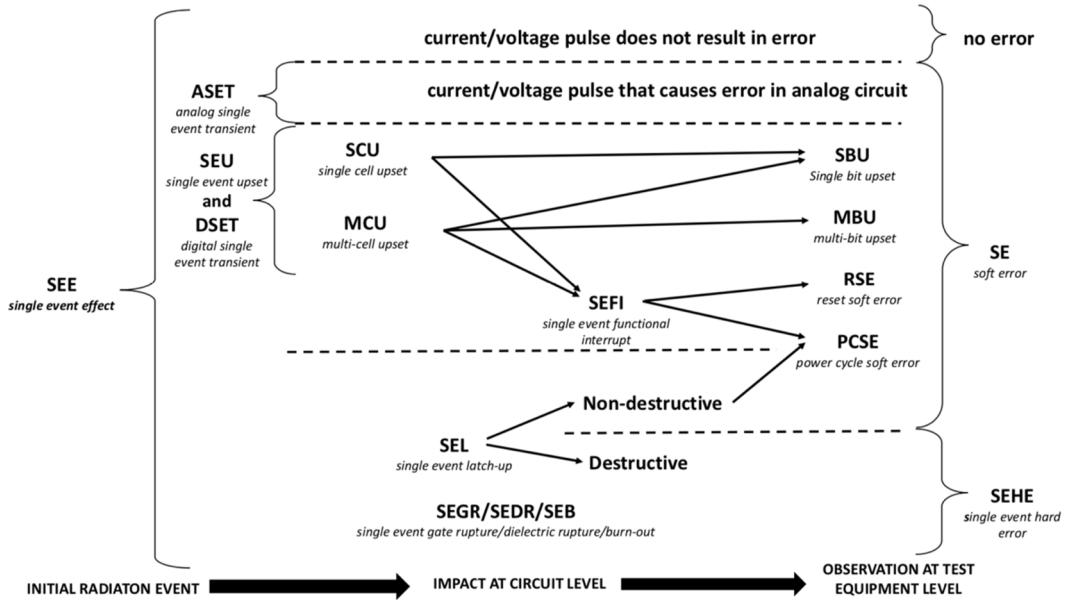


Fig. 1. Diagram of terms used to describe SEEs. (After JEDEC Standard JESD89B [24], ©JEDEC 2021.)

- 3) *SEB*: “An event in which a single energetic particle strike induces a localized high-current state in a device, resulting in catastrophic failure.”
- 4) *SEL*: “An abnormal current state in a circuit caused by the passage of a single energetic particle inducing a parasitic thyristor to turn on and remain in a fixed state regardless of inputs, until the device is power cycled. Some SEL events result in a measurable current increase (e.g., latchup of an IO circuit). Some SEL events may result in a difficult-to-detect increase in current (micro-SEL) compared to the quiescent current of the entire component (e.g., latchup of memory cells within a common well). A high-current SEL may cause permanent damage to the component and result in a hard error. Micro-SEL events are typically nondestructive due to the low current draw and can be cleared by power cycling.”

As explained in the Introduction, this article does not aim to cover the vast and exhaustive domain of all types of SEEs but mainly focuses on the most important issues concerning the modeling and simulation of SETs and SEUs induced by single events in digital electronics. For a detailed presentation of other SEEs and radiation effects in electronics (total-ionizing dose (TID), displacement damage), we invite the reader to consult [13], [26], [27], and [28] and the references cited therein.

#### B. Main Processes That Lead to the Production of an SEE in a Circuit/System (Summary)

Before surveying the main modeling and simulation approaches of SEEs in Sections III–VII and going into the substance of several underlying mechanisms for creating SEEs, we summarize in the text that follows and in Fig. 2 the main processes that lead to the production of an SEE in a circuit. We

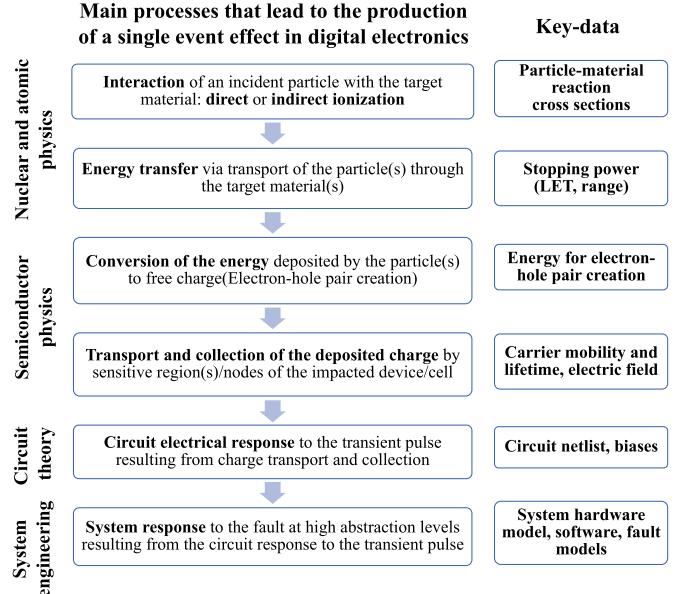


Fig. 2. Main processes that lead to the production of SEEs in digital electronics and key data considered for their modeling and simulation, from the particle interaction to the system level.

note that the physical processes occur on different timescales and are noninteracting.

1) *Interaction of the Incoming Particle With the Target Material*: An SEE is always initiated by the interaction of an incident particle with the target material. This interaction necessarily involves a transfer of energy from the particle to the medium via electromagnetic or nuclear processes. As a result of such processes, a fraction or the totality of the incoming particle energy is released inside the medium [29]. At this level, we can identify two primary interaction mechanisms for the typical particles that could potentially cause

SEEs in electronics: direct ionization and indirect ionization of matter [30].

Direct ionization typically concerns electrons, muons, low-energy protons ( $E < 1$  MeV), alpha particles, and heavy ions (with atomic number  $Z > 1$ ). These mainly interact with the electrons and nuclei of the target material [30]. In the initial phase of the passage of such a charged particle in matter, collisions with atomic electrons are the principal mode of energy loss in a very wide range of energies of the incident particle. These interactions gradually slow down the particle. In the final phase, the particle slowing and stopping are due to collisions with nuclei. The main mechanism that leads to energy loss and slowing down of the charged particle is then the ionization phenomenon. Ionization induces the generation of a large number of excited energetic electrons (delta rays), which generally have sufficient energy to ionize other atoms. An electronic cascade is activated in which the number of free electrons continues to increase while their average energy decreases. During the passage of the ionizing particle, a highly ionized channel of very small diameter (typically a few tens of nm) develops around the track of the particle. Very rapidly, the excited electrons in the plasma lose their kinetic energy through a series of elastic collisions with electrons of the lattice to finally reach an energy close to the binding energy of the material. Simultaneously, the ionized atoms, positively charged, rearrange their electrons resulting in the creation of holes in the valence band. A high-density column of electron-hole pairs is then formed in a narrow region around the particle track.

Indirect ionization primarily concerns neutrons, but also high-energy protons and heavy ions. These particles can interact with atomic nuclei following two major mechanisms, i.e., scattering (elastic and inelastic interactions) and capture (inelastic interactions or nuclear reactions). For elastic interactions, the total kinetic energy is conserved, and the incoming particle is deflected from its path as it transfers some of its energy to the target atom. In the case of inelastic scattering, the target nucleus rearranges its internal state to one of higher energy, and the total kinetic energy is not conserved. But in both cases, the nature of the recoil nucleus is left unmodified. Instead of being scattered, an incident neutron, proton, or ion may be absorbed or captured by a target material nucleus. After it has absorbed the impinging particle, the nucleus can get rid of excess protons or neutrons; it can undergo de-excitation by emitting a  $\gamma$ -ray, or it may even split into medium-sized fragments when the energies are high enough to trigger nuclear fission (a threshold energy exists for each such reaction). The produced fragments extend from the proton or neutron to the nucleus of the target atom; they can in turn directly ionize matter like any charged particle (previous case). It is important to note that nuclear reactions produced by high-energy ions are rare compared to ion-electron interactions, yet they hold significance in specific cases as explained in [31], [32], and [33]. These nuclear reactions yield one or multiple secondary ionizing particles with significantly different electronic stopping power (see below) compared to the primary incident particle. The relevance of nuclear reactions in error rate estimations strongly

depends on the critical charge of the circuit or device under consideration [31], [32], [33].

The number of nuclear interactions per type of interaction can be evaluated from cross-section data of the atom nuclei present in the target material. For monoenergetic neutrons or protons arriving perpendicularly on a thin sheet of natural material, the number of nuclear interactions occurring in the target is given by

$$N_X(E) = \sum_i f_i \sigma_{X,i}(E) \times 10^{-24} \times NV \times t \times M \quad (1)$$

where  $X$  is the type of considered interactions (elastic, inelastic, and nonelastic),  $E$  is the energy of the incident neutrons or protons,  $\sigma_{X,i}(E)$  is the value at energy  $E$  of the type  $X$  reaction cross section for isotope  $i$  (expressed in barn),  $f_i$  is the fraction of isotope  $i$  in the target isotopic composition,  $t$  is the target thickness (expressed in cm),  $NV$  is the number of atoms per cubic centimeter, and  $M$  is the number of incident monoenergetic neutrons or protons impacting the target.

*2) Energy Transfer From the Ionizing Particle(s) to the Target Material:* For both direct or indirect ionization, two key quantities can be introduced to characterize the energy transfer from an ionizing particle (i.e., an incident ionizing particle penetrating the target material or produced as a secondary particle in an interaction event involving a primary incoming particle and a target atom nucleus) to the target material: the stopping power and the range. We recall below the definitions of these two quantities.

*Stopping Power:* The stopping power is the amount of energy per unit length lost by a particle in the matter. It is usually expressed in keV/ $\mu\text{m}$  or MeV/ $\mu\text{m}$ . The total stopping power is decomposed into two components: 1) the electronic stopping power, corresponding to the loss of energy of the particle due to collisions with atomic electrons of the target material and 2) the nuclear-stopping power, corresponding to the loss of energy of the particle due to collisions with the nuclei of atoms of the target material. The electronic stopping power is also called linear energy transfer (LET). Thus, the LET characterizes the creation of electron-hole pairs by ionization of the target material, while nuclear-stopping power describes the atomic displacement of the target material [30]. The LET is expressed as a function of the energy particle  $E$  as

$$\text{LET} = -\frac{dE}{dx}. \quad (2)$$

For a nonrelativistic charged particle with speed  $v$ , charge  $z$  (in multiples of the electron charge) traveling into a target of electron density  $n$  and mean excitation potential  $I$ , the LET can be analytically evaluated from the reduced form of the Bethe–Bloch formula [34]

$$\text{LET} = \frac{4\pi n z^2}{m_e v^2} \cdot \left( \frac{e^2}{4\pi \epsilon_0} \right)^2 \cdot \ln \left( \frac{2m_e v^2}{I} \right) \quad (3)$$

where  $\epsilon_0$  is the vacuum permittivity, and  $e$  and  $m_e$  are the electron charge and rest mass, respectively. Equation (3) shows that LET increases with decreasing particle velocity until it reaches a maximum value when the particle is close to

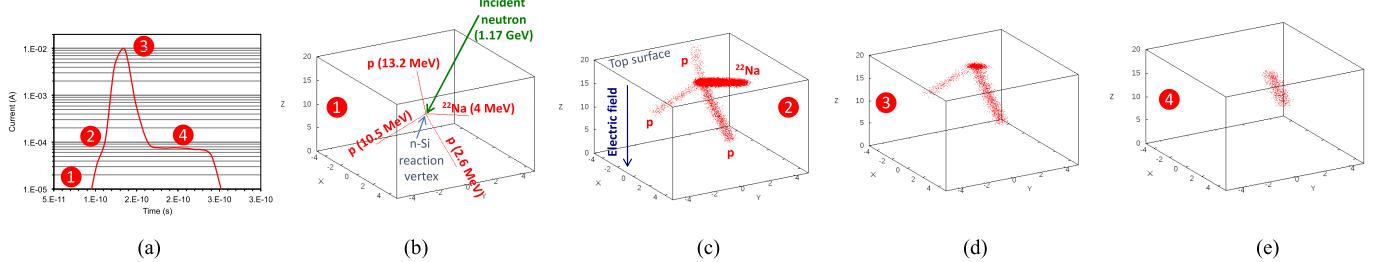


Fig. 3. (a) Particle RWDD numerical simulation (described in Section IV-C) of the transient current extracted from the junction contact (corresponding to the top surface) in a reverse-biased junction caused by the interaction of a 1.17-GeV neutron with a silicon atom (three protons and a  $^{22}\text{Na}$  ion produced). (b) Illustration of the charge generation and the transport and collection phases: (c) 2; (d) 3; and (e) 4 indicated on the transient plot. Dimensions on the three axes are in nanometers.

stopping. A weighted LET is generally used, defined as the ratio between the LET and the density  $\rho$  of the target material

$$\text{LET} = -\frac{1}{\rho} \frac{dE}{dx}. \quad (4)$$

The unit of this weighted LET is MeV/(mg/cm<sup>2</sup>).

*Range:* The range  $R$  is the distance traveled by an ionizing particle of initial kinetic energy  $E_0$  before it comes to rest in the stopping material; it is calculated from the LET of the particle as

$$R(E_0) = \int_{E_0}^0 -\frac{1}{\text{LET}} dE = \int_0^{E_0} \frac{1}{\text{LET}} dE \quad (5)$$

*3) Conversion of the Deposited Energy to an Electrical Charge:* The conversion of the energy deposited by an ionizing particle to free charge in a given target material can be evaluated from its mean value of energy for electron–hole pair creation  $E_{e,h}$ , a material-dependent constant usually experimentally measured or determined from band structure and quantum transport simulation (see, for example, recent work performed for bulk silicon and germanium [35]). When experimental or accurate simulated values are not available for a given semiconductor material,  $E_{e,h}$  can be estimated from Klein’s phenomenological model that establishes a linear relationship between the bandgap energy and  $E_{e,h}$  in semiconductor materials [36]

$$E_{e,h}(\text{eV}) \simeq \frac{14}{5} E_g(\text{eV}) + 0.66. \quad (6)$$

The well-known value for bulk silicon is  $E_{e,h} = 3.6$  eV at 300 K. From (6),  $E_{e,h}$  is expected to vary from  $\sim 1.1$  eV for InSb ( $E_g = 0.17$  eV at 300 K) to  $\sim 12$  eV for diamond ( $E_g = 5.47$  eV at 300 K).

For a given target semiconductor material characterized by its density  $\rho$  and its average energy for electron–hole pair creation  $E_{e,h}$  and considering a particle with a given LET value, it is possible to calculate the charge  $Q_{\text{dep}}$  deposited by this particle along a path of length  $\ell$  in the target material from the following expression:

$$Q_{\text{dep}} = \frac{16.02 \times \rho}{E_{e,h}} \int_{\text{path}} \text{LET}(\ell) d\ell \quad (7)$$

where  $Q_{\text{dep}}$  is given in fC if  $\rho$  is expressed in g/cm<sup>3</sup>,  $E_{e,h}$  is in eV, LET is in MeV/(mg/cm<sup>2</sup>), and  $\ell$  is in  $\mu\text{m}$ .

*4) Transport and Collection of the Deposited Charge in the Region of the Impacted Circuit:* Once a very dense column of electron–hole pairs has been created almost instantaneously (the practically instantaneous delivery of the ion energy to the electronic subsystem of a solid, lasting from 0.1 to  $10^3$  fs, creates a large number of electron–hole pairs per unit track length [37]) along the track of the ionizing particle, this deposited charge rapidly evolves under the action of different mechanisms that control the charge-carrier dynamics, e.g., its transport in the semiconductor material and its possible collection by a circuit node. It must be noted that these transport and collection processes of importance occur in the active semiconductor region of the device.

*Charge Transport:* The development of the column of electron–hole pairs starts in the femtosecond range after its creation following three mechanisms that contribute to the reduction of the density of excess carriers at the heart of the track: ambipolar diffusion, carrier recombination (Shockley–Read–Hall and Auger recombination) and separation between holes and electrons under the combined effect of diffusion and drift induced by local electrical fields [37]. Charges released from this plasma column and having escaped the initial massive recombination are quickly transported further into the semiconductor by diffusion and also by additional drift in regions where a nonzero electric field exists.

*Charge Collection:* Released charges in the “vicinity” of a circuit node at front-end-of-line (FEOL) level, e.g., near or across a reverse-biased p-n junction or a biased diffused area contact, can be collected via drift–diffusion (DD) by such a structure and be extracted from the semiconductor material to the circuit. This charge collection process is crucial in the formation of a parasitic transient current that is injected into the impacted node. In Section III, we will look in detail at the physics, modeling, and simulation of this key step in the formation of SEEs.

Fig. 3 illustrates the formation of a transient current pulse [shown in Fig. 3(a)] resulting from the charge transport and collection in the case of a neutron-silicon nuclear reaction. This reaction occurs in the volume of the space charge region (SCR) of a reverse-biased nanotransistor drain junction and produces four ionizing secondaries. Fig. 3(a) shows the result of a simplified particle Monte Carlo (MC) simulation, in which the radiation-induced minority carriers (here, the electrons grouped per packets of multiple charges) are represented by red points. After the production of secondaries and the energy

deposition along their tracks [Fig. 3(b)], the widening of the charge clouds reflects the diffusion of the carriers, their displacement toward the top surface, and their drift in the electrical field (here vertical) of the junction [Fig. 3(c)–(e)]. Carriers are finally extracted from the top surface (electrode) where they contribute to the formation of the transient current that is injected into the external circuit.

5) *Circuit Electrical Response*: The current transient pulse resulting from the radiation-induced charge collection and extraction at the level of a circuit node may induce disturbances in the circuit to which the impacted node is connected. The induced effects at the circuit level are different according to the intensity of the current transient, as well as the number of impacted circuit nodes. If the transient peak is sufficiently important in terms of current magnitude, it can induce a hard error (permanent damage) on gate insulators (gate rupture, SEGR) or provoke a short-circuit loop between different semiconductor regions (latchup, burnout). In other cases, the transient current may generally induce an SE which can be manifested by the change of logic state of one or more memory points (upset) or even a functional interrupt. In Section V, we will examine in detail the circuit electrical response to such radiation-induced pulses, and we will show that the circuit is not necessarily passive during this phase of charge collection. On the contrary, it can play an important role via the counter-reaction it develops on the impacted node potential following the collection of charges on it.

6) *System Response*: When a transient event occurs at the level of a circuit, hardware component of a larger electronic system, it can trigger various consequences that reverberate at the system level. One prominent consequence is data corruption. In digital systems, the sudden change in the state of a register or memory bit due to an SEU, for example, can lead to errors in calculations, memory storage, or communication protocols. This corruption compromises the integrity of critical information and can have cascading effects on subsequent operations. In addition to data corruption, the functionality of the affected circuit may be disrupted. This disruption may be transient, causing temporary malfunctions, or it may cause permanent changes in the logic of the circuit, resulting in unexpected behavior, system crashes, or erroneous responses. In some cases, a single event can even trigger a system reset, resulting in temporary downtime, potential loss of data, and disruption to overall system operation. Single events can also cause communication errors. Corruption of data as it is transmitted between different components of the system can lead to misinterpretation, protocol violations, or communication failures. Such errors can undermine the synchronization of subsystems, essential for the proper functioning of complex systems. SEEs at the system level can similarly alter the control flow within the software. An event-induced change in the logic of a program can lead to unintended branches or loops that were not intended by the original design. Consequently, the system might exhibit behavior that deviates from the expected and intended operational path, potentially causing software crashes or erroneous outcomes. There is also the risk of permanent damage caused by single events. In extreme

cases, the circuit can be irreparably harmed, rendering the system inoperable. Finally, SEEs might not always lead to immediate visible effects. Some events could introduce latent effects that manifest themselves later, making the diagnosis of system-level issues challenging.

### C. Multiphysics, Multiscale, and Multidomain Nature of Single Events

Sections II-A and II-B summarized different processes that lead to the production of an SEE in a digital circuit or a system. It showed that SEEs are inherently multiphysics, multiscale, and multidomain, as indicated in the following and illustrated in Figs. 4 and 5.

1) *Multiphysics*: SEEs are first initiated by particle–matter interactions, the fields of nuclear, and atomic physics. Then, they involve the creation of charges and their transport in materials, mainly semiconductors, governed by solid-state physics and quantum mechanics. The resulting transient current or voltage pulse created in the interconnected network of elementary structures that constitute the circuit itself, in the sense of the electronics function, obeys the fundamental laws of electrokinetics and circuit theory. Finally, the potentially disturbed circuit response can affect the system of which it is a part, governed by the general theory of systems.

2) *Multiscale*: SEEs are initiated by a single particle interaction at atomic level in the bulk of circuit materials and can lead to a functional error at circuit or system level. Between these two events, there are approximately 15 orders of magnitudes on the distance scale and approximately 20 orders of magnitude on the timescale, as illustrated in Fig. 4. In addition to the multiphysics nature of SEEs, these changes of scale both in time and in distance explain why is extremely difficult to simulate SEEs with a single tool from the beginning to the end of this sequence of events.

3) *Multidomain*: SEE, or more accurately the precursor event to an SEE, is first an atomic event before being transformed into an electrical signal then into an analog or logical event. Depending on when it is considered, it, therefore, belongs to different fields or domains: the domain of materials, then of devices, then of circuits, and finally of systems. To each domain corresponds a particular expression of this SEE precursor: secondary particles of a nuclear interaction, a bundle of electron–hole pairs, transient current, analog signal, logic pulse, value encoded in a memory, etc. When passing from one domain to the next, as defined in the SEE chronology formulation, the physics of the previous domain appears to be lost in the new domain; this can be overcome to a certain extent, as will be discussed in several places later in this article. For example, when the secondary particle energy is converted into e–h pairs, the nuclear physics is no longer appropriate for describing the formation of the SEE, and any information relating to the nuclear event is moreover lost. This vision is true until the final expression of the SEE at the system or application level, at the end of the chain.

Fig. 5 illustrates in a slightly different way the multiphysics and multiscale nature of SEE, emphasizing their multidomain character. Four domains can be defined in which an SEE precursor (or initial event) will have different expressions: at

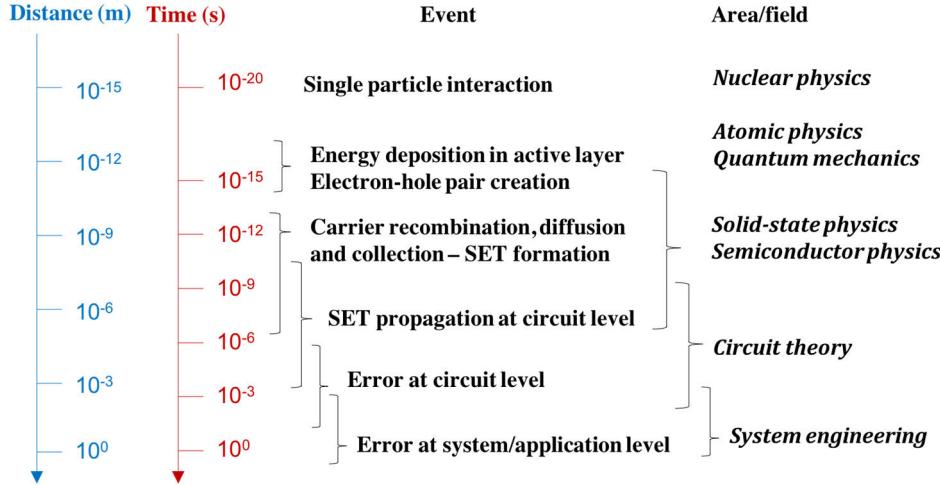


Fig. 4. Typical space and time scales for SEEs, from the single particle interaction to the detection of an error at the system level.

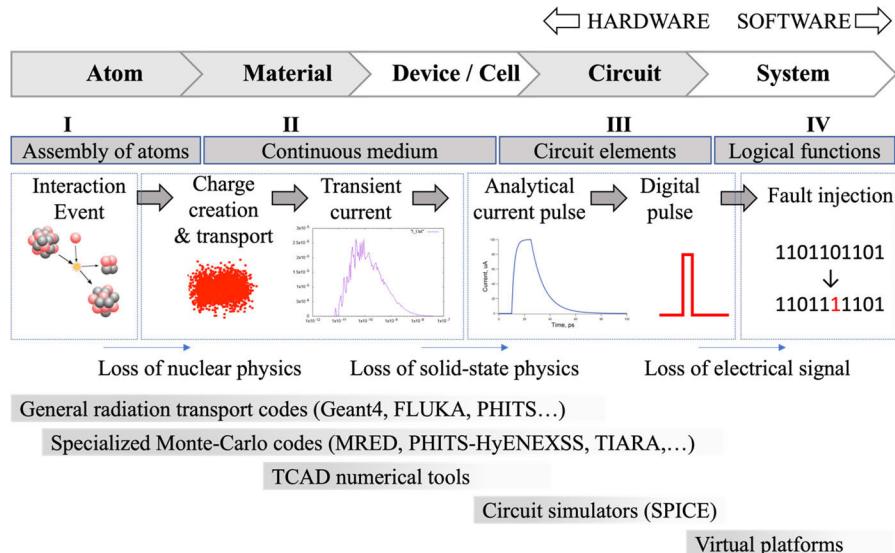


Fig. 5. Multiphysics, multiscale, and multidomain nature of SEE. The main simulation tools and platforms are also indicated.

the atomic level (assembly of atoms), at the material level (continuous media), at the circuit level (circuit elements), and at the system level (logical functions). The boundary is sometimes difficult to define, thus the notion of assembly of atoms to describe the domain in which nuclear interactions and energy deposition of secondary particles by ionization take place. The same applies to the notion of continuous medium to describe semiconductor or insulating materials, whether they are considered as bulk materials or part of a component.

When considering the chronological formulation of SEEs (from atoms to systems), each change of domain is marked by a loss of information concerning the mechanism that gave rise to the precursor signal of the SEE. The precursor of an SEE is first a nuclear interaction, then a cloud of charges, then an analog electrical signal, then a digital signal, and finally a binary value. Considering the electrical signature of an SEE no

longer allows us to go back to the interaction that gave rise to it; likewise, considering a binary change does not make it possible to go back to the original electrical signal. This loss of information concerning the physical mechanisms from the underlying domain to the next is an important element in understanding that an SEE can be simulated at different levels and with different physical manifestations. This point will be discussed in detail in Section III-A. In certain cases, results from a tool that simulates a level farther along in the chronological formulation of an SEE can be used to define inputs to a tool that appears earlier in the chronological view. While at first this seems counter intuitive, the rationale is in fact simple: if the outputs from a higher level tool can be simplified such that they can be used to define inputs to a lower level tool, then one gives up information from the high-level tool. This approach allows one to bypass higher level tools in the full analysis of an SEE, reducing simulation time

TABLE I  
SIMULATION LEVEL, AND TYPICAL SIMULATION INPUTS AND OUTPUTS FOR THE FIVE CATEGORIES OF CODES INTRODUCED IN FIG. 5 AND IN THE TEXT

Type of codes	Simulation level	Typical simulation inputs	Radiation input (or signal emulating radiation)	Typical simulation outputs
General radiation transport codes	Atom to small circuit	Simplified three-dimensional (3D) circuit architecture Sensitive volumes	Primary particles Sources of particles (or nuclear interaction databases)	Secondaries Energy deposited in sensitive volumes
Specialized Monte Carlo code as applied to SEEs				Secondaries Energy in sensitive volumes and/or collected charge Soft error rate
TCAD	Material to cell	Realistic device/circuit 3D architectures (possible link with process)	Radiation-induced generation rate	Device transient response Carrier and potential distributions
Cell circuit simulation codes	Material to cell	Transistor compact model	Numerical or analytical SETs	Cell transient response (time domain analysis)
Circuit simulators	Device to circuit	Circuit netlist Device library	Analytical SETs Logical SETs	Soft error rate
Hardware Description Language (HDL) simulators and virtual platforms	Circuit to system	Circuit design Application code	Logical faults	Soft error vulnerability Execution errors

significantly. This point is briefly described in Sections IV-A and V-D.

### III. TAXONOMY OF MODELING AND SIMULATION APPROACHES

In this section, we examine different types of methodologies of modeling and simulation of SEEs, as a function of the “simulation level” envisaged to perform a given study. We propose a classification of simulation tools in five main categories. We also examine the main modeling and simulation approaches for the transport and collection of the deposited charge induced by an ionizing radiation at device or circuit levels that allow us to distinguish methods using a collection charge concept with respect to methods considering the computation of a collected current.

#### A. Types of Methodologies: What Simulation Code, Input, and Output?

We start again from Fig. 5 which illustrates the domains covered by the main simulation tools and platforms used to simulate SEE in electronics (the list is far from exhaustive). This highlights that none of them can cover the entire chain, from particles to systems. We distinguish five categories of codes, briefly described in the following and in Table I.

- 1) General radiation transport codes like Geant4 [38], [39], FLUKA [40], [41], MCNP [42], [43], or PHITS [44], [45]: These codes are general-purpose, continuous-energy, generalized-geometry, time-dependent, and MC radiation transport codes designed to track many particle types over broad ranges of energies. These codes have many applications in high-energy experimental physics and engineering, shielding, detector and telescope design, cosmic ray studies, dosimetry, medical

physics, and radiobiology. In the context of SEE studies, these codes can be used to develop and compile complete applications from toolkits including source files and libraries. Alternatively, they can be used to perform various calculations from precompiled versions that read data input files.

- 2) Specialized MC radiation transport codes applied to SEEs like SEMM/SEMM-2 [46], [47], [48], MRED [31], [49], [50], [51], PHITS-HyENEXSS [52], TIARA [53], [54], [55], MUSCA-SEP3 [56], [57], IRT [58], MC-ORACLE [59], [60], and other codes (see references in [51]) based on nuclear and radiation transport physics: These MC-based radiation transport tools can simulate a variety of effects that result from energy transferred to a semiconductor material by a single particle event. The breadth and depth of the application of each specialized code solving SEEs problems vary dramatically, from almost nonexistent to a high level of detail, as illustrated in [51].
- 3) TCAD numerical simulation platforms like the Synopsys<sup>1</sup> [61], Silvaco<sup>1</sup> [62], or Cogenda<sup>1</sup> [63] suites: TCAD code suites are used to model and numerically simulate semiconductor fabrication and semiconductor device operation. Included are the modeling of process steps (such as diffusion and ion implantation), modeling of the behavior of the electrical devices based on fundamental semiconductor physics, and numerical solving of electrostatics and continuity equations for different carrier transport models (DD, hydrodynamics, quantum transport, . . . ), also taking into consideration of radiation effects and transport (see Section IV-D). Coupled with a circuit simulator, TCAD tools can simulate the impact of

<sup>1</sup>Registered trademark.

radiation at the circuit level in a mixed-mode approach (see Section V).

- 4) *Circuit Simulators*: They include analog simulators, digital simulators, and dedicated codes for mixed-signal analog/digital circuits. The most popular is Simulator Program with Integrated Circuit Emphasis (SPICE), which is certainly the most used electronics circuit simulator. SPICE refers to a wide variety of open source (Ngspice [64]) and commercial circuit simulation programs (PSpice<sup>1</sup> [65] and Eldo<sup>1</sup> [66]) offering extended capabilities via the integration of optional analog, radio frequency (RF), mixed signals, or digital circuit simulation modules. Analog circuit embedding digital content can, thus, be simulated. More generally speaking, SPICE also refers to a class of simulation approaches based on the conversion of a text netlist of electrical elements such as resistors, capacitors, diodes, transistors, and voltage/current sources and their connections to equations to be numerically solved. At this circuit level, SEEs can be modeled in the form of current or voltage pulses produced by a parametrized or arbitrary source inserted in the netlist and emulating the impact of an ionizing particle on a particular circuit node.

- 5) *System Simulators and Virtual Platforms (VPs)*: At complex digital circuit, system-on-chip (SoC), or system levels, the modeling and simulation of SEEs profoundly change in nature. SEE signals become logical (binary) information and are introduced during a simulation run via fault injection (FI) techniques. Their impact can be explored at different abstraction levels (gate-level, cycle-level, and transaction-level) using a wide variety of dedicated tools [67]. Full-system simulators or VPs, such as OVPsim [68] or gem5 [69], are used to explore the vulnerability of complete systems to SEEs: they must include not only the modeling of the full hardware system (i.e., processor, memory, and peripherals) but also the modeling of the full software system (the user application and the full operating system). The SE vulnerability of a complete system can be analyzed from the exhaustive characterization of the execution errors monitored during a simulation.

Table I summarizes the simulation level, typical simulation inputs, and outputs for different categories of codes defined in Fig. 5 and in the text above. We will examine in Sections IV–VII some specificities of these different simulation approaches, first focusing on the physics of the charge transport and collection at the semiconductor level, an essential step for the creation of transient signals that are at the origin of SEEs at device and circuit levels.

### B. Physics of the Charge Transport and Collection (Collected Charge and Current)

One of the most complex and central tasks in modeling and simulation of SEE is to correctly describe the interaction of an incoming particle with the sensitive zone(s) of a circuit and to determine the resulting transient electrical response susceptible to subsequently induce an SEE at the circuit level. We examine

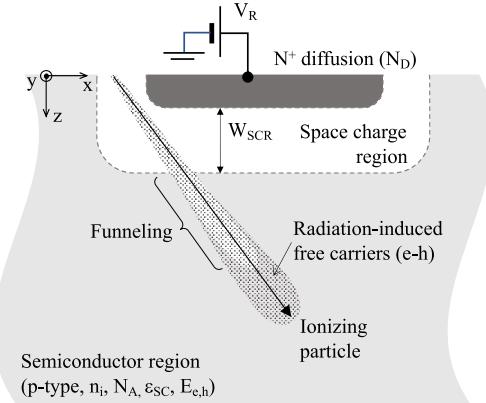


Fig. 6. Schematic illustration of the passage of an ionizing particle crossing the SCR of a reverse-biased p-n junction and stopping in the semiconductor region.

in this paragraph the underlying physics that controls the charge transport and collection at the level of an elementary device, a reverse-biased  $n^+$ -p junction integrated into bulk semiconductor material (silicon by default). We take as a starting point ( $t_0$ ) the moment immediately after the passage of the particle when the radiation-induced charge is just deposited in the form of a dense track of electron–hole pairs, as schematically illustrated in Fig. 6. The device of interest is defined by its geometry, type of materials, doping concentrations, and so on. Carrier transport and potential dynamics induced by the passage of the particle in the semiconductor domain can be resolved in time from the self-consistent solving (coupling) of a set of three fundamental equations.

- 1) The Poisson equation that addresses the electrostatic problem. Solving this equation amounts to finding the electric potential  $\varphi$  (V) for a given charge density distribution  $\rho$  ( $C \cdot m^{-3}$ )

$$\nabla(\epsilon \vec{\nabla} \phi) = -\rho = -q[N_D^+ - N_A^- + p - n] \quad (8)$$

where  $\epsilon$  is the material-dependent permittivity ( $F \cdot m^{-1}$ ),  $q$  is the absolute value of the electron charge,  $N_D^+$  and  $N_A^-$  are the doping ionized atom concentrations ( $m^{-3}$ ) for donor and acceptor impurities, respectively,  $n$  and  $p$  are the electron and hole densities ( $m^{-3}$ ), respectively.

- 2) The continuity equations that guarantee the continuity of electron and hole current densities  $J_n$  and  $J_p$  ( $A \cdot m^{-2}$ ), respectively,

$$\nabla \vec{J}_n = q(G - R) + q \frac{\partial n}{\partial t} \quad (9)$$

$$\nabla \vec{J}_p = -q(G - R) - q \frac{\partial p}{\partial t} \quad (10)$$

where  $G$  and  $R$  are the generation and recombination rates, respectively.

The electron and hole densities are calculated using the Fermi–Dirac statistics or using the Maxwell–Boltzmann approximation in the case of nondegenerate-doped semiconductors. In addition, to solve (9) and (10), a transport model must be chosen to express the current densities  $J_n$  and  $J_p$ . In the following, the classical DD model will be used as the transport model. This assumes that the carrier energy is

constantly in balance with the electric field so that the transport only depends on the electric field. In the DD model, the carrier transport is mainly due to electrostatic potential gradients and/or to carrier concentration gradients. The current densities of electrons and holes are then usually modeled as follows:

$$\vec{J}_n = -q\mu_n n \vec{\nabla}\phi + qD_n \vec{\nabla}n \quad (11)$$

$$\vec{J}_p = q\mu_p p \vec{\nabla}\phi - qD_p \vec{\nabla}p \quad (12)$$

where  $\mu_n$  ( $\mu_p$ ) is the electron mobility (respectively, holes),  $D_n$  ( $D_p$ ) is the thermal diffusion coefficient of electrons (respectively, of holes), and  $\phi$  is the electric potential, solution of (8).  $D_{n,p}$  and  $\mu_{n,p}$  depend on the material and electric field and are connected by the Einstein relation  $D_{n,p} = (kT_L/q) \times \mu_{n,p}$  where  $T_L$  is the lattice temperature. In (11) and (12), current densities are, therefore, given by the sum of the conduction or drift component (the first term of the right side of equations) and the diffusion component (the second term).

In (8)–(12), the quantities  $n$  and  $p$  include not only the free carrier concentrations at equilibrium given by the band bending of the semiconductor, but also the excess carrier densities produced during the passage of the ionizing particle in the device. In other words, these radiation-induced electrons and holes are in excess with respect to the charge carriers available at thermal equilibrium. It is evident that the presence (along the particle track at  $t_0$ ) and the evolution (due to diffusion, recombination, and drift in the SCR) of excess carriers locally modify the electrostatic potential and thus complexify the carrier dynamics and the transient device response.

One of the most important electrostatic manifestations of excess carriers is the drastic distortion of the electric field in the border of the SCR when the particle passes through this area, known as the funnel effect. After the particle penetration, the electric field, which was originally limited to the SCR, extends far down into the bulk semiconductor along the length of the particle track and can literally “funnel” many carriers into the struck junction, further enhancing charge collection. After a few nanoseconds, the field recovers to its position in the normal depletion layer, and, if the track is long enough, a residue of carriers is left to be transported by diffusion. The extent of this funneling is a function of substrate doping concentration, bias voltage, and particle energy. It is a clear manifestation of the self-consistent character of the problem posed by the solving of the Poisson and continuity equations in the presence of an ionizing particle penetration.

Solving self-consistently the set of (8)–(12) in the three spatial dimensions and in a time domain including the passage of the ionizing particle up to the return to equilibrium is, thus, a very complicated process that only becomes tractable when using full numerical simulation performed on a meshed structure, in which each node has specific associated properties, such as type of material, doping concentration, electrostatic potential, and quasi-Fermi levels. This meshing is used for solving discretized forms of (8)–(12) with given boundary conditions. In practice, only TCAD tools or some dedicated codes are capable of performing such fully numerical calculations (see Section IV).

To render this problem easier to solve in the context of SEE prediction at the circuit level, many simplifying assumptions

must be introduced. These simplifications relate to the two aspects of the problem: the electrostatics and the transport of charges.

- 1) The first is to decouple the Poisson equation from the continuity equations. In other words, the electrostatic potential at equilibrium (before the particle struck) is conserved throughout. The continuity equations are then solved considering an electric field fixed at the equilibrium of the structure, i.e., equal to zero in the semiconductor bulk and given by the p-n junction theory inside the SCR of the collecting junction. Consequently, electron and hole density currents are pure diffusion currents throughout the simulation domain, to which a drift component must be added only inside the SCR. Two time-dependent models can be derived from this simplified schema: the diffusion-collection model and the DD collection model, detailed in Sections IV-B and IV-C. These approaches allow a collected current to be computed, catch the dynamics of the event, and facilitate the consideration of the counter-reaction of the circuit in the case of mixed-mode simulation (Section V).
- 2) In addition to the previous simplification, the way in which the sensitive node collects the minority carriers resulting from the radiation can be greatly simplified by considering that only the carriers generated in a certain SV around the node will surely be collected. Here, diffusion and drift of excess carriers occur in an “invisible way,” and their action and efficiency are included in the geometrical parameters of the SV. The computation of the charge transport is no longer meaningful, and the time variable disappears from the calculation that reduces to a pure geometrical problem. Different models can be derived from this approach, and they are described in Section IV-A.

These simplifying assumptions lead to less accurate simulation results, but simplified implementation and faster simulation times. Depending on the level of simplification considered, the computation effort and accuracy will be obviously very different. From the considerations highlighted above, Fig. 7 proposes a classification of the main modeling-simulation approaches for the transport and collection of the deposited charge by an ionizing radiation at the semiconductor device level, detailed in the following.

#### IV. ANALYTICAL, COMPACT, AND FULL NUMERICAL METHODS AT DEVICE/CELL LEVEL

In this section, we examine in detail the main modeling and simulation approaches developed in the last decades by several research groups and authors concerning SEE at device and circuit cell levels. They include some popular SV-based models, the so-called diffusion-collection method, the RWDD approach, and TCAD simulation.

##### A. SV-Based Models

1) *Rectangular Parallelepiped (RPP) Model:* An SV is defined as “a region in space in which energy deposition

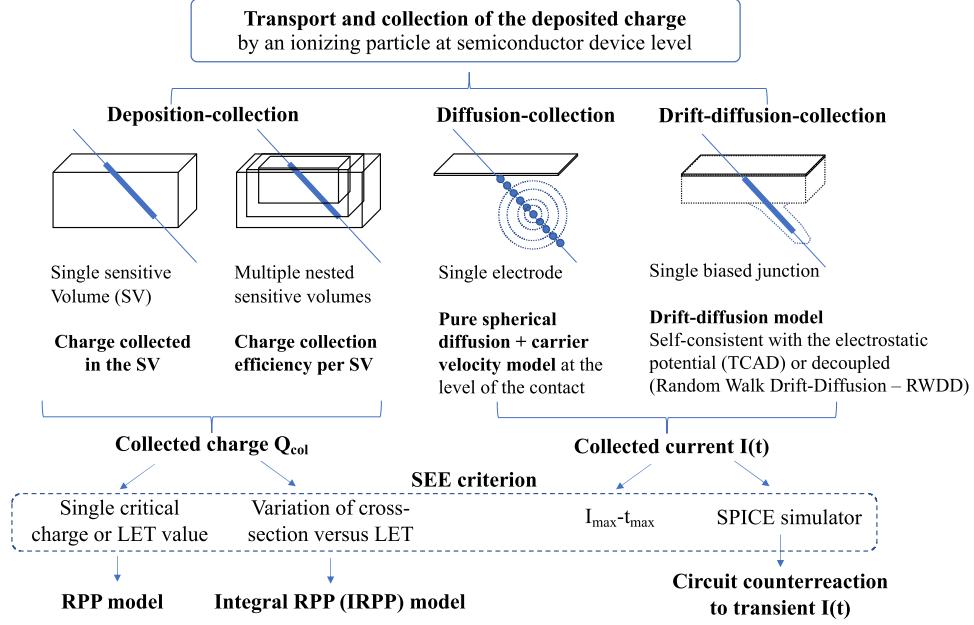


Fig. 7. Classification of the main modeling-simulation approaches for the transport and collection of the deposited charge induced by ionizing radiation at the semiconductor device level.

from the ionizing particle can affect the operation of a device. For SEE, the volume is often associated with the depletion region of a particular circuit node” [70]. This SV, also called “charge collection volume,” is generally treated as an RPP. The charge deposited by a given ionizing particle depends on its path in the SV. It can be evaluated from (7), where  $\ell$  is the length of the particle path in the SV, as illustrated in Fig. 8(a). An RPP volume is defined by a triplet of reals  $(a, b, c)$  where  $a, b$ , and  $c$  represent the three dimensions of the parallelepiped in decreasing order. For such an RPP volume, the chord maximum length  $\ell_{\max}$  corresponds to the main diagonal, i.e.,  $\ell_{\max}^2 = a^2 + b^2 + c^2$ , and the total surface area of the volume is  $S = 2(ab + ac + bc)$  [Fig. 8(a)].

SV approaches are based on the essential notion of circuit critical charge  $Q_{\text{crit}}$ , originally defined for memory circuits as “the minimum amount of collected charge that will cause a device node to change state and result in a SEU” [24]. In this definition, the critical charge is supposed to be independent of the current pulse shape, which supposes that the current pulse produced by the ionizing particle is short compared to the integration time constant of the circuit (including parasitic capacitances) [71].

The determination of the critical charge value can be evaluated from various mixed-mode, TCAD, or circuit simulation approaches, described later in this article. At this point, it is important to remember the remark that concluded Section II-C. This remark emphasizes that the outputs from a higher level of simulation (i.e., a circuit simulation) can be simplified (i.e., reduced to a single critical charge value) such that they can be used to define inputs to a lower level approach (i.e., the RPP model), thus bypassing higher level tools in the full analysis of the SEE problem and, in final, reducing simulation time significantly.

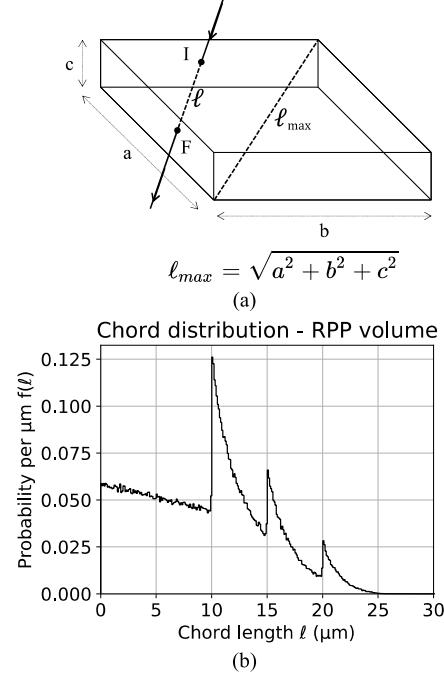


Fig. 8. (a) Definition of an RPP volume of dimensions  $a \times b \times c$ . (b) Chord distribution numerically calculated from MC simulation for an RPP volume with  $a = 20 \mu\text{m}$ ,  $b = 15 \mu\text{m}$ , and  $c = 10 \mu\text{m}$  (histogram on 570 612 chords).

Supposing that the SV of Fig. 8(a) is attached to a sensitive node of a given circuit cell characterized by a critical charge value  $Q_{\text{crit}}$ , in a first approximation (discussed and completed later), if the charge generated by the incident ionizing particle in the SV is greater or equal to  $Q_{\text{crit}}$ , then the circuit will be disturbed, and an SEE will be produced. This condition can be written as follows:

$$Q_{\text{dep}} = K \times \text{LET} \times \ell > Q_{\text{crit}} \quad (13)$$

where  $K$  is a material-dependent constant derived from (7) that depends on  $\rho$ , the density of the material, and  $E_{e,h}$ , the energy for electron–hole pair creation, and  $\ell$  is the length of the particle path inside the SV.

The primary interest of SV-based models is that it is possible to combine certain characteristics of the particle source with the calculation of the deposited charge and therefore, by comparison with a critical charge, to calculate directly the SEE error rate for a given radiation environment. In this sense, these models are particularly well-adapted for on-orbit environments characterized by an isotropic flux of heavy-ions. To be numerically tractable, a certain number of simplifying assumptions must be considered. These assumptions have been carefully reviewed and discussed by Petersen [71]. We recall in the following the most important (all are taken from [71]).

- 1) “The energy deposited in an SV is equal to the energy loss of an energetic ion passing through that volume as calculated using its LET.”
- 2) “Ions with the same LET have the same effect.”
- 3) “The change in LET along an ion track in the region of interest is negligible.”
- 4) “The charge generation is equal to the product of the LET of the ion and a chord of the region [as stated by (13)], perhaps augmented by a funnel region or a diffusion region.”
- 5) “The charge collection path is independent of the LET.”
- 6) “The SV is a convex body. The charge collected from an ion track is that generated along the chord defined by the path through the SV.”
- 7) “The particle flux is isotropic at the device, and therefore, the LET spectrum is the same for all directions.”

The charge deposited in the SV is given by the integral of the product of the chord length distribution  $f(\ell)$  of the RPP box by the LET distribution of the incoming particles [71]. Fig. 8(b) shows such a chord length distribution for an RPP volume in the form of a probability histogram. This histogram is upper bounded by the maximum chord length value, i.e.,  $\ell = \ell_{\max}$ .

To directly derive the SEE error rate from (13), one must evaluate for a given particle LET value  $\Lambda$ , the minimum chord length  $\ell_{\min}$  of the particle through the SV that will create enough electron–hole pairs to cause an upset. From (13), it is evident that  $\ell_{\min} = Q_{\text{crit}}/(K \times \Lambda)$ ; its minimum minimorum value is  $\ell_{\min} = Q_{\text{crit}}/(K \times \Lambda_{\max})$ , where  $\Lambda_{\max}$  corresponds to the maximum value of the LET spectrum related to the particle source. The number of events is then directly determined by the sum of possible paths that can lead to an adequate charge deposition in the SV. Pickel’s formulation [71] uses the combination of the ionizing integral particle flux in terms of its energy deposition  $\Phi(\Lambda)$  and the path probability  $f(\ell)$

$$N = \frac{S}{4} \int_{\ell_{\min}}^{\ell_{\max}} \Phi(\Lambda) f(\ell) d\ell \quad (14)$$

where  $S$  is the total area surface of the volume,  $\ell_{\max}$  is the maximum path length in the RPP volume, and  $\Lambda_{\min}$  is the minimum LET that can deposit critical charge in path length  $\ell$ . From (13), the quantity to be used in (14) is  $\Lambda_{\min} = Q_{\text{crit}}/(K \times \ell)$ . Note that  $\Phi(\Lambda)$  is derived from

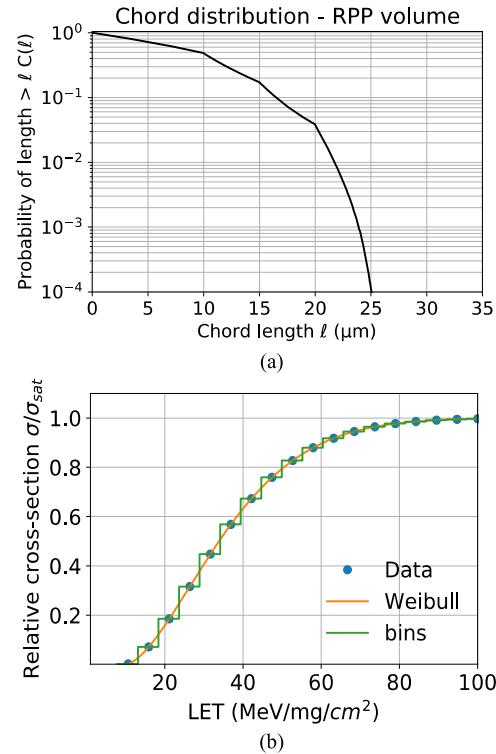


Fig. 9. (a) Integral chord length distribution corresponding to the integration of histogram of Fig. 8(b) using (15). (b) Typical relative cross-sectional data versus LET. The fitting of data with integral Weibull distribution is also plotted. The introduction of bins on the cross-section curve is needed for IRPP calculations.

the distribution in energy  $\Phi(E)$  using the transformation  $\Phi(\Lambda) = \Phi(E) \times (dE/d\Lambda)$ . The particle flux  $\Phi$  is supposed isotropic and is integrated over  $4\pi$  steradians.

For the convenience of calculation (availability of analytical approximations), the integral chord length distribution  $C(\ell)$  may be preferred to  $f(\ell)$ .  $C(\ell)$  corresponds to the probability of a particle traversing the SV with a chord length greater than  $\ell$  [see Fig. 9(a)], i.e.,

$$C(\ell) = \int_{\ell}^{\ell_{\max}} f(\ell') d\ell'. \quad (15)$$

Equation (14) can be rewritten following the basic form of Bradford’s formulation [71], [72]:

$$N = \frac{N}{4} \int_{\Lambda_0}^{\Lambda_{\max}} \Phi(\Lambda) \times C\left(\frac{Q_{\text{crit}}}{K\Lambda}\right) d\Lambda \quad (16)$$

where  $\Lambda_0$  and  $\Lambda_{\max}$  are, respectively, the minimum minimorum and the maximum value of the LET spectrum related to the particle source, and from (13),  $\Lambda_0 = Q_{\text{crit}}/(K \times \ell_{\max})$ .

2) *Integral RPP (IRPP) Model:* In the RPP method described above (formulations of Pickel and Bradford), there is a unique critical charge that must be exceeded for the circuit cell to upset. Consequently, the curve of cross section versus LET, for a circuit modeled as a collection of identical cells with the same SV parameters and a unique  $Q_{\text{crit}}$  value, will be necessarily a step function. Such a cross-section curve, expected if all parts of all cells had the same sensitivity, does not correspond to what is generally observed. Petersen [71] discussed in detail (and references therein) the inadequacy of

the single  $Q_{\text{crit}}$  (or LET threshold) for upset rate calculations and the necessity of integrating the LET spectrum with the cross-section curves to properly allow for changes of sensitivity across the circuit. This more general model is called the IRPP approach.

The IRPP model allows for the variation of the internal circuit sensitivity by integrating over a distribution of event rates corresponding to the variation of the circuit cross section versus LET,  $\sigma(\Lambda)$ . This curve is supposed to be experimentally known. The process consists in interpreting the  $\sigma(\Lambda)/\sigma_{\text{sat}}$  relative cross-section curve ( $\sigma_{\text{sat}}$  is the saturation cross section) in terms of a distribution of critical charges, assuming a single RPP SV with thickness  $c$ . The conversion from  $\Lambda$  to  $Q_{\text{crit}}$  is obtained at any part of the curve via the relationship:  $c = Q_{\text{crit}}/(K \times \Lambda)$ . From the experimental data [see Fig. 9(b)] and for each discrete value of  $Q_{\text{crit}}$  describing the curve, the number of events is calculated by integrating the RPP chord distribution with the LET spectrum of the environment, in the same way as in (14). The result is weighted with the quantity  $(\sigma(\Lambda)/\sigma_{\text{sat}}) \times \text{bin width}$  for the bin corresponding to the considered discrete  $Q_{\text{crit}}$  value [Fig. 9(b)]. The circuit response corresponds to the sum of these individual contributions over the entire curve [71]. In mathematical terms with continuous variables and functions, if we set  $\sigma(\Lambda)/\sigma_{\text{sat}} = F(\Lambda)$ , the number of events can be expressed as

$$N = \frac{N}{4} \int F(\Lambda') \int_{\Lambda_{\min}}^{\Lambda_{\max}} \Phi(\Lambda) \times C\left(\frac{\Lambda' c}{\Lambda}\right) d\Lambda d\Lambda' \quad (17)$$

where  $\Lambda_{\min}$  is the minimum LET value to deposit  $Q_{\text{crit}} = K \times \Lambda' \times c$  on the main diagonal of the RPP volume,  $\ell_{\max}$ , that gives  $K \times \Lambda_{\min} \times \ell_{\max} = K \times \Lambda' \times c$ , then  $\Lambda_{\min} = \Lambda' \times c/\ell_{\max}$ .

Different distribution functions can be used to model the  $\sigma(\Lambda)/\sigma_{\text{sat}}$  relative cross-section curve [71]. The most popular function is the integral Weibull distribution

$$\frac{\sigma(\Lambda)}{\sigma_{\text{sat}}} = F(\Lambda) = 1 - \exp\left\{-\left[\frac{(\Lambda - \Lambda_0)}{W}\right]^s\right\} \quad \Lambda \geq \Lambda_0 \\ = 0 \quad \Lambda < \Lambda_0 \quad (18)$$

where  $\Lambda$  is the LET,  $\Lambda_0$  is the LET threshold,  $W$  is the width parameter, and  $s$  is the shape parameter. Fig. 9(b) illustrates the plot of (18) with the following parameters:  $\Lambda_0 = 10 \text{ MeV}/(\text{mg/cm}^2)$ ,  $W = 30 \text{ MeV}/(\text{mg/cm}^2)$ , and  $s = 1.6$ .

*3) Introduction of Funneling in RPP/IRPP Models:* The charge-collection effect attributed to funneling, illustrated in Fig. 6, can be included in RPP/IRPP models following two different approaches summarized here.

- 1) The first method consists of increasing the depth of the SV to include the funnel contribution. The chord lengths will be then augmented, notably in the  $z$ -direction, from a funnel length  $\ell_f$ .
- 2) The second method is to add the funnel path to the charge-collection path, but not to change the basic RPP volume. As noted by Petersen [71], most of the simulation codes allow a separation of an intrinsic SV and an additional path length  $\ell_f$  attributed to the funnel.

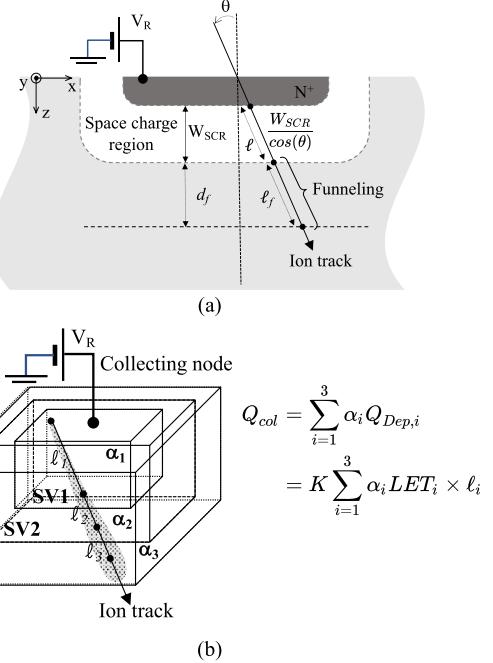


Fig. 10. (a) Definition of quantities used in Hu's funneling model [73]. (b) Conceptual drawing of an ionizing particle passing through three SVs. The total collected charge for the event is the sum of the charge generated in each segment  $\ell_i$  in volume SV*i* scaled by the collection efficiency for that region  $\alpha_i$ . (Adapted after Warren et al. [74], ©IEEE 2007.)

In this case, the charge deposited in the SV must be rewritten

$$Q_{\text{dep}} = K \times \text{LET} \times (\ell + \ell_f). \quad (19)$$

Consequently, different expressions for  $\ell_{\min}$ ,  $\ell_{\max}$ ,  $\Lambda_{\min}$ , and  $\Lambda_{\max}$  previously defined for (14), (16), and (17) must be reevaluated from (19).

A series of funneling model descriptions has been conducted by Messenger and Ash [72]. Different analytical expressions of the funnel lengths can be derived from the approximate solution of the continuity equations and the electroneutrality equation. The model developed by Hu [73] proposes simple expressions for the depth of collection  $d_f$  and length of collection  $\ell_f$  related to the funneling in a  $n^+$  p-junction subjected to an ion strike, as defined in Fig. 10(a)

$$\ell_f = \left(1 + \frac{\mu_n}{\mu_p}\right) \frac{W_{\text{SCR}}}{\cos(\theta)} \quad (20)$$

$$d_f = \left(1 + \frac{\mu_n}{\mu_p}\right) W_{\text{SCR}} \quad (21)$$

where  $W_{\text{SCR}}$  is the width of the SCR,  $\theta$  is the incident angle of the ionizing particle, and  $\mu_n$  and  $\mu_p$  are the electron and hole mobilities in the substrate material, respectively.

For the first method and as illustrated in Fig. 10(a), the depth of the SV has to be increased by the quantity  $d_f$  given by (21) to include the funneling. It should be noted that in this case, the angular dependence of the funnel contribution is not explicit since it is already integrated with the chord length distribution functions obtained with this RPP volume (with increased depth).

*4) Weighted SV Model:* This method was introduced to improve the traditional RPP approach that fails to account for different charge collection mechanisms such as drift, diffusion, or bipolar amplification [74], [75]. Indeed, considering the contributions of these mechanisms in the charge collection can lead to a notable difference between the amount of charge deposited in the RPP volume by the incident ion and the amount of charge effectively collected at the circuit node. A possible expansion of the single SV RPP method is to consider several distinct SVs or nested volumes, as depicted in Fig. 10(b). A weighting of the contributions of different volumes to the collected charge is introduced to describe intracell variation in charge collection. The model quantifies the charge collection at a node by an individual particle event as a linear combination of the charge deposited in each volume  $SV_i$  scaled by the respective coefficient  $\alpha_i$  which is related to the collection efficiency [see Fig. 10(b)] [76] by

$$Q_{\text{col}} = \sum_i \alpha_i Q_{\text{Dep},i} = K \sum_i \alpha_i \text{LET}_i \times \ell_i. \quad (22)$$

The principle of nested regions allows modeling the spatial charge collection efficiency that falls off with distance from the sensitive node. For example, as illustrated in Fig. 10(b), we could imagine an incident particle directly passing through and ionizing the innermost SV  $SV_1$  with 100% charge collection efficiency whereas those passing through a region immediately outside this volume could have only 50% charge collection efficiency in  $SV_2$  and 25% in  $SV_3$ .

The determination of the geometry, dimensions, and collection efficiency of different nested volumes can be typically performed using TCAD simulation (Section IV-D). Once more, the concluding remark of Section II-C takes on its full meaning: the nested volumes characterizing the collection of charge at a sensitive node can be defined only once per TCAD simulation, which then makes it possible to carry out a complete simulation of the circuit without using again TCAD simulations of higher level, which saves significant time.

To conclude, one additional remark: pushing this model to its limits with a very large number of SV (which would result in segmenting the trace of the particle into elementary sections), naturally leads to the collection-diffusion approach in which the expression of  $\alpha_i$  coefficients are derived from the diffusion law.

### B. Diffusion-Collection Models

In the so-called “diffusion-collection” models, the energy lost by a charged particle in the semiconductor material along its track is converted into electron–hole pairs that are rearranged in the form of a succession of point charge densities of electrons and holes,  $\delta n$  and  $\delta p$ , respectively, with  $\delta n = \delta p = \delta n_0$  just after energy deposition and creation of the pairs [see Fig. 11(a)]. The model then assumes that the transport of these discrete charge densities is governed by a pure 3-D spherical diffusion law in all regions of the semiconductor domain

$$\frac{\partial n(r, t)}{\partial t} = D \nabla^2 n(r, t) \quad (23)$$

where  $D$  is the diffusion coefficient.

In the neutral semiconductor region and in the absence of an external electric field, the separation of electron–hole pairs induces an internal field drawing the electrons and holes back together (this electric field arises from the small charge imbalance that inevitably occurs as low-mobility holes try to keep up with higher mobility electrons). Consequently, when the particle track begins to expand in its radial direction, electrons and holes in track are foremost transported together and diffuse in train. This corresponds to ambipolar diffusion and the coefficient  $D$  in (23) must be taken equal to the ambipolar coefficient  $D^*$  given by

$$D^* = \frac{(n + p) D_n D_p}{n D_n + p D_p} \quad (24)$$

where  $D_n$  and  $D_p$  are the diffusion coefficients for electrons and holes, respectively, and  $n$  and  $p$  are the total electron and hole densities, respectively.

The ambipolar diffusion constant has an intermediate value between  $D_n$  and  $D_p$  but is numerically closer to the diffusion constant of the less mobile species (holes in this case). For longer times after track formation when carrier densities are reduced,  $D$  reverts to its value  $D_n$ , the diffusion coefficient of electrons in the semiconductor at equilibrium. Equation (23) can be analytically solved with the limit condition.  $\lim_{t \rightarrow 0} \delta n(r_0, t) = \delta n_0$

The excess carrier density at time  $t$  and distance  $r$  from the initial track element  $\delta n_0$  is

$$\delta n(r, t) = \frac{\delta n_0}{(4\pi D^* t)^{\frac{3}{2}}} \exp\left(-\frac{r^2}{4D^* t} - \frac{t}{\tau}\right) \quad (25)$$

where  $\tau$  is the carrier lifetime.

The resulting elementary current density due to this pure diffusion process from the initial track element  $\delta n_0$  is

$$\delta \vec{J}(r, t) = q D \vec{\nabla}(\delta n). \quad (26)$$

The corresponding diffusion current passing through a given closed surface  $S$  is then given by

$$\int_S \delta \vec{J}(r, t) \cdot d\vec{S} = q D \iint_S \vec{\nabla} \delta n \cdot d\vec{S}. \quad (27)$$

From these preliminary results established for a single-point charge density  $\delta n_0$ , we can now generalize (25) and (27) in the case of a charge deposited along a particle track. Let us consider the case illustrated in Fig. 11(b) with the following considerations.

- 1) The ionizing particle of kinetic energy  $E$  is emitted (or arrives) at point  $I(x_I, y_I, z_I)$  and stops at point  $F(x_F, y_F, z_F)$ .
- 2) The total charge deposited by this particle is  $Q_0 = q n_0 = qE/E_{e,h}$  where  $E_{e,h}$  is the mean energy of creation for an electron–hole pair in the semiconductor bulk material. For simplicity, this charge is supposed to be linearly deposited between  $I$  and  $F$ .

The integration of (25) along the track segment  $IF$  gives

$$n(t) = \frac{n_0}{8\pi L D t} \exp\left(-\frac{l_0^2}{4Dt} - \frac{t}{\tau}\right) \exp\left(\frac{K^2}{L^2 4Dt}\right) \times \left\{ \operatorname{erf}\left(\frac{1}{\sqrt{4Dt}} \left(L + \frac{K}{L}\right)\right) - \operatorname{erf}\left(\frac{K}{L\sqrt{4Dt}}\right) \right\} \quad (28)$$

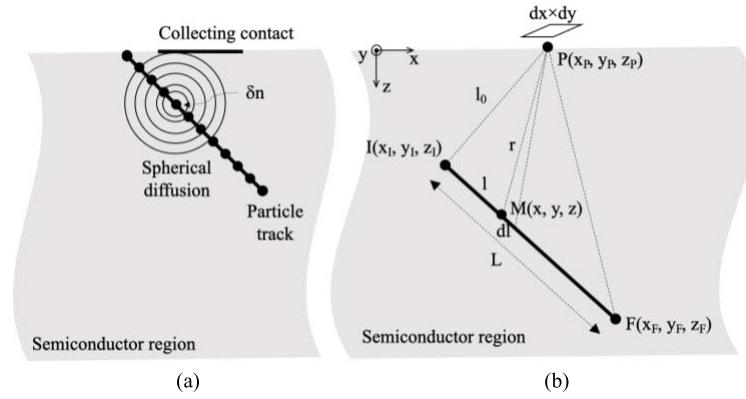


Fig. 11. (a) Schematic illustration of the diffusion-collection model principle: the ionizing particle track is divided into small elements containing  $\delta n = \delta p$  electrons and holes which can isotropically diffuse toward the collecting electrode. (b) Definition of the main notations used in the model.

where  $K = (x_I - x_P)(x_F - x_I) + (y_I - y_P)(y_F - y_I) + (z_I - z_P)(z_F - z_I)$ .

According to (27), the diffusion current passing through an elementary surface of dimensions  $\Delta x \times \Delta y$ , centered in point  $P$  and perpendicular to the axis ( $Oz$ ) is given by

$$\Delta I_{\text{diff}}(t) \approx q D \frac{\Delta n(t)}{\Delta z} \times \Delta x \Delta y \quad (29)$$

where  $\Delta n(t)/\Delta z$  is the gradient of  $n$  in the  $z$ -direction at time  $t$ , numerically evaluated from (28) at two points,  $P$  and  $P'(x_p, y_p, z_p + \Delta z)$ . The discrete summation of (29) over a given surface  $S$  (divided in  $\Delta x \times \Delta y$  elements) perpendicular to axis ( $Oz$ ) directly gives the diffusion current  $I_{\text{diff}}(t)$  that can be extracted by an electrode of surface  $S$  located at this level. Finally, the complete current pulse resulting from the passage of the ionizing particle in the semiconductor region can be computed from (28) and (29) considering a time mesh with uniform or nonuniform spacing (with a geometric progression, for example).

The current pulse analytically calculated from the previous procedure is a diffusion current, without any contribution of an electric field in such a pure diffusion approach. In this sense, it ignores the contribution of the electric field of the SCR in the transport and collection mechanism (Fig. 6). Several methods and model improvements have been published in these two last decades that attempt to solve this important limitation of the diffusion-collection approach. Briefly, all these methods modify the evaluation of the current, which is no longer based on the diffusion gradient, but which relies on the introduction of a collection velocity at the level of the collecting electrode. In its simplest revised version, the charge given by (28) is converted into a current by multiplying  $n(t)$  by the elementary charge and by the average collection velocity  $v_{\text{col}}$  evaluated over the SCR of the reverse-biased drain. This quantity is then integrated on the surface  $S$  of the collecting electrode

$$I(t) = q \iint_S v_{\text{col}} \cdot n(t) dx dy. \quad (30)$$

In (30),  $v_{\text{col}}$  can be evaluated using different approaches, for example, derived from the average value of the drift velocity induced by the junction electric field [30] or calculated using a time-dependent model including the time variations of the ambipolar diffusion coefficient [77].

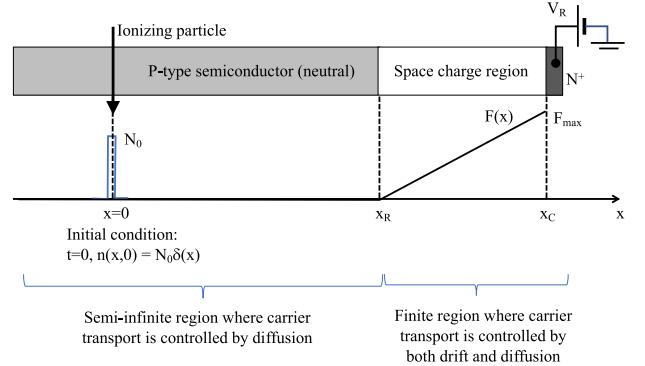


Fig. 12. 1-D problem of radiation-induced carrier transport in the presence of a nonconstant electric field. At  $t = 0$ , the ionizing particle deposits a charge  $N_0$  in  $x = 0$  (Dirac distribution).

*Important Remark:* To conclude, a final remark concerning the diffusion-collection approach. Unfortunately, this model cannot analytically treat the case of two adjacent domains for which diffusion is the main mechanism on one domain and DD controls the transport on the other domain, as illustrated in Fig. 12. This important case corresponds to the 1-D modeling of a  $N^+$ /P-junction with the bulk semiconductor region (neutral zone) and the SCR.

We recall here that, in the presence of an electric field  $F$ , (23) can be rewritten in 1-D as

$$\frac{\partial n}{\partial t} = \frac{\partial}{\partial x} \left[ D \frac{\partial n}{\partial x} + \mu_n n F \right]. \quad (31)$$

Equation (31) can be fully analytically solved on a single infinite domain with constant  $D$  and  $\mu_n$  in the case of  $F = 0$  or  $F = F_0$  on the whole domain. Suppose that at  $t = 0$ ,  $n(x, 0) = N_0 \delta(x)$ ; we then have the two following evident solutions:

$$F = 0 \quad n(x, t) = \frac{N_0}{\sqrt{4\pi Dt}} \exp\left(-\frac{x^2}{4Dt}\right) \quad (32)$$

$$F = F_0 \quad n(x, t) = \frac{N_0}{\sqrt{4\pi Dt}} \exp\left(-\frac{(x - \mu_n F_0 t)^2}{4Dt}\right). \quad (33)$$

Equation (33) does not apply in the case of Fig. 12, even if a constant electric field  $F_m = F_{\text{max}}/2$  is considered in the SCR

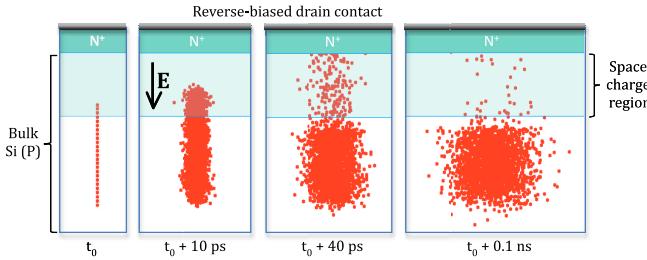


Fig. 13. Schematic illustrating the charge transport and collection processes after a 5-MeV alpha-particle strike in a reverse-biased junction (its geometrical and electrical parameters correspond to the 65-nm node). The biased contact collects charges that diffuse in silicon and is accelerated by the electric field developed in the SCR. (After Glorieux et al. [79], ©IEEE 2014.)

because carriers are subjected to the action of the electric field only from  $x = x_R$  and not from  $x = 0$ .

There is no analytical solution of (31) for the problem illustrated in Fig. 12. In other words, it is thus impossible to obtain an analytical expression of  $n(x_C, t)$  from which a collected current could be derived. This important limitation of the methods justifies the development of the fast numerical method presented in the following.

### C. RWDD Model

The RWDD model is a particle MC method that simultaneously simulates drift, via a velocity term derived from the electric field, and diffusion with a random-walk algorithm simulating a Brownian motion [78], [79], [80]. In a similar way to what was done in the diffusion-collection method [Fig. 11(a)], an ionizing particle track crossing a circuit at the silicon level is modeled as a series of charge packets spread along a straight segment whose length equals the ionizing particle range in the target material (see Fig. 13). The linear density of the charge packet along the particle track takes into account the nonconstant LET of the particle. The stopping and range of ions in matter (SRIM) code [81], [82] or approximate functions [83] can be used to compute both LET and range for the incoming particle. The accuracy of this charge discretization is ensured by the degree of “granularity” that can be fine-tuned by selecting the packet size, in practice from 1 to 100 elementary charges.

The transport and recombination of the electron and hole charge packets start immediately after the particle crosses the device. Excess carriers diffuse and drift in the “background” electric field that existed before the particle impact (at equilibrium). In this sense, the transport is decoupled from the electrostatic problem (Poisson equation) that remains unchanged. The DD motion from instants  $t$  to  $t + \Delta t$  of a charge packet located at  $\mathbf{r}(t)$  is calculated as follows:

$$\mathbf{r}(t + \Delta t) = \mathbf{r}(t) + \mu^* t \mathbf{F}_0(\mathbf{r}(t)) + \mathbf{N}_3(0, 1) \sqrt{2D^* \Delta t} \quad (34)$$

where  $\mu^*$  and  $D^*$  are the carrier ambipolar mobility and ambipolar diffusion coefficient [given by (24)], respectively,  $\mathbf{N}_3(0, 1)$  is a 3-D standard normal random vector (i.e., a triplet of reals between 0 and 1 distributed following the normal distribution [84]), and  $\mathbf{F}_0$  is the electric field before the particle strike.

At each time step of the simulation, the radiation-induced collected current is computed from the transport dynamics of minority charge packets governed by (34) and recombination is also considered by “killing” certain electron and hole packets, considering a fixed or a local carrier lifetime, as explained in the following.

- For the estimation of this collected current, two main procedures may be employed: the first technique is to use the semiconductor transport equations, and the second is to apply Shockley–Ramo’s theorem. Simulation tools used in microelectronics generally consider the first option; the transport equations are implemented in a TCAD simulator that numerically solves them self-consistently with Poisson’s equation. This approach considers the free-charge carrier distributions as continuous functions in time and space coordinates. The second option is generally used in instrumentation or high-energy physics for the calculation of detector responses to transient radiation events. In this second approach, Ramo’s theorem is used to treat each carrier considered individually and all the effects due to a given population of carriers are summed [85]. In this work, we implemented the first formalism (transport equations) by applying the continuity equation at the collecting (drain) contact. The transient current at the collecting node is directly computed from the number of carriers  $\Delta n$  that reach this contact during the time step  $\Delta t$ , i.e.,

$$I(t) \approx q \times \frac{\Delta n}{\Delta t}. \quad (35)$$

In this expression, the displacement current is neglected, a reasonable approximation in this case [86]. This collection current is then injected in the electrical simulation to model the circuit response.

- For modeling carrier recombination, a simple implementation consists in considering an exponential law that decreases the number of charge packets as a function of time:  $N(t) = N_0 \cdot \exp(-t/\tau)$ . In this exponential law,  $N_0$  is the initial number of charge packets deposited by the particle at  $t = t_0$  and the time constant  $\tau$  is equal to the average carrier lifetime. At each time step, the number of surviving packets is then fit to  $N(t)$  via a random killing of excess packets. A more sophisticated implementation has been proposed by Malherbe et al. [87]. It considers a local evaluation of the lifetime of excess carriers, which is given by  $\tau = \delta c/R$  where  $\delta c$  is the local excess density of carriers with respect to the equilibrium before particle strike and  $R$  is the total recombination rate (including Shockley–Read–Hall and Auger recombination). Certain packets are “killed” with a local probability of  $\Delta t/\tau = \Delta t \times R/\delta c$  (note that this only simulates geminate recombination, for simplicity).

The practical implementation of the RWDD model is greatly facilitated by using an object-oriented programming language, which offers considerable advantages in terms of advanced structures, such as classes, objects, and containers [80]. For example, the particle track can be then defined as a container

including all the charge packets described as independent objects. The members of the charge packet class include the geometrical coordinates of a given packet and its electrical charge. The container content may change during the simulation due to two different mechanisms cited previously: 1) carrier recombination or 2) carrier extraction that corresponds to particles that escape the simulation domain. This object-oriented programming of RWDD should facilitate the simulation of complex circuits with an arbitrary number of sensitive areas and collecting nodes, intrinsically considering, in this case, multiple node charge collection in the simulation process. As also explained in [80], in the RWDD approach, the behavior of each packet of charge is computed independently of the other charges. These processes being independent, the task of calculating the charge transport can be easily parallelized on a graphic processing unit (GPU) whose internal architecture is perfectly adapted to such a massive parallelism. Moreover, the RWDD model needs to implement a random number generation procedure that is usually time consuming; if the random numbers are independent, this task can also be easily parallelized on GPU. These two characteristics of the RWDD model are expected to result in a considerable improvement in computation speed since the number of parallelizable tasks in RWDD is relatively high. In [79], an acceleration factor of  $\times 140$  was reported using a single GPU with respect to the classical central processing unit (CPU) implementation for the simulation of 100 000 charge packets with 1000 time steps.

Fig. 13 illustrates a typical RWDD simulation. At  $t_0$ , a 5-MeV alpha particle is emitted in a reverse-biased N<sup>+</sup>/P-junction; its track partially overlaps the SCR. At  $t_0 + 10$  ps, the particle track has considerably radially extended and minority charge carriers (here, electron packets in red) in the SCR are drawn into the electric field and begin to approach the collecting N<sup>+</sup> region. At  $t_0 + 40$  ps, the drift regime in the SCR and the isotropic diffusion in the neutral substrate region are clearly visible, the track segment in the substrate tends to become a spherical cloud of charge packets that continues to extend with time. At  $t_0 + 0.1$  ns, minority carriers in the SCR are less numerous, and they have been massively collected at the N<sup>+</sup> electrode. The SCR remains supplied with carriers which are transported by diffusion in the substrate and entrained by the electric field as soon as they enter the SCR.

Fig. 14 shows a direct comparison of the transient currents and the corresponding charges collected by the drain of the nMOS transistor subjected to a 5-MeV alpha particle striking the center of the drain perpendicularly to the device, obtained from RWDD and TCAD simulations. One can observe a few differences between the two curves, especially in the early stages of the transient, mainly due to: 1) the arrival of discrete charge packets at the level of the collecting drain contact in RWDD which induces inherent granularities; 2) the slightly delayed charge generation considered in the TCAD simulation due to the introduction of a temporal distribution in the generation rate (see Section IV-D); and 3) because in RWDD, the transport is decoupled from the electrostatic problem (Poisson equation), contrary to TCAD. Values of

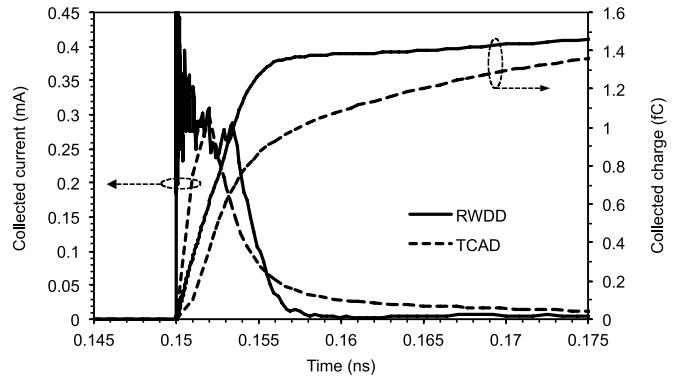


Fig. 14. Current and charge collected by an isolated OFF-state nMOS transistor (designed in 65-nm CMOS technology) after a 5-MeV alpha particle strike computed by TCAD and RWDD model. (After Autran et al. [78], ©Elsevier 2014.)

the collected charges obtained from TCAD and RWDD are very close at the end of the transient event, with a difference limited to a maximum of 15%, indicating that both modeling approaches have, in this case, very similar charge collection efficiencies.

#### D. TCAD Simulation

TCAD simulation, also known as numerical modeling (i.e., based on the numerical resolution of a set of physics equations) aims to quantify the understanding of the underlying technology and abstract this knowledge for use in circuit design. It consists of two distinct parts: the simulation of the manufacturing process (not described in this short course) and the simulation of the device electrical operation (device electrical simulator). This type of simulation does not generally correspond to a large circuit approach; it is restricted in practice to a single device, a circuit cell, or a portion of a given circuit limited to a few units/tens of transistors. TCAD simulation is nonetheless an essential step in the development of ICs and microelectronics. TCAD electrical simulation models the electrical behavior of a device/circuit cell of interest, considering its 3-D geometry, materials, and doping profiles. The effects of radiation on the device operation can be also simulated at this electrical simulation level. The starting point of the electrical simulation is the device/circuit cell of interest. It is represented as a meshed structure where each node has specific associated properties such as the type of material and the dopant concentration. This mesh is used for solving the main differential equation such as the Poisson equation and the transport and continuity equations, as described in Section III-B. As previously mentioned, solving self-consistently (8)–(12) in the three spatial dimensions and in a time domain including the passage of the ionizing particle up to the return to equilibrium is a very complicated process. The simulation starts with different initialization steps that concern device geometry, mesh properties, charge density, and biases applied to different device electrodes. After this initialization, the discretized Poisson equation is solved and the electrostatic potential in the device is calculated. The potential is afterward injected directly into the resolution of the continuity equation. The output of this module is used

to calculate a new carrier density to be used in the Poisson equation. In this way, a new potential is found and is injected into the continuity equation and so on. The loop stops when the convergence criterion is reached. In such a simulation scheme, the effect of a particle strike in the device is included in (9) and (10) in the form of a generation rate, depending on several radiation characteristics and representing an external generation source of carriers. This radiation-induced generation rate  $G$  is added to the other conventional generation rates that account for various direct generation-recombination mechanisms occurring in the device. A general expression for  $G$  is the following:

$$G(w, l, t) = F(l) \times R(w) \times T(t) \quad (36)$$

where  $F(l)$  gives the number of electron–hole pairs (per unit of length) created by the ionizing particle along its path,  $R(w)$  is a radial distribution function, and  $T(t)$  is a temporal distribution function. With respect to quantities introduced in (36), the particle track is described in a cylindrical coordinate system  $(w, \theta, l)$  that specifies point positions by the radial distance  $w$  from the track axis, the azimuth angle  $\theta$  (the axis rotation corresponds to the particle axis), and the axial coordinate  $l$  with respect to the origin  $O$  of the particle track.

$F(l)$  has the following expression:

$$F(l) = \frac{dN_{\text{ehp}}}{dl} = \frac{1}{E_{e,h}} \frac{dE}{dl} \quad (37)$$

where  $N_{\text{ehp}}$  is the number of electron–hole pairs created by the particle strike,  $E$  is the energy of the particle, and  $E_{e,h}$  is the mean value of energy for electron–hole pair creation in the considered material [given by (6)].  $F(l)$  varies as a function of the particle penetration in the material, expressed as the distance  $l$  traversed by the particle in the matter along its path. The quantity  $dE/dl$  is related to the LET of the particle.

For conservative reasons, the radiation-induced generation rate given in (36) must fill the condition

$$\int_0^\infty \int_0^{2\pi} \int_0^\infty G(w) dw d\theta dt = \frac{dN_{\text{ehp}}}{dl}. \quad (38)$$

Consequently, functions  $R(w)$  and  $T(t)$  are subjected to the following normalization conditions:

$$2\pi \int_0^\infty R(w) w dw = 1 \quad \int_{-\infty}^\infty T(t) dt = 1. \quad (39)$$

Ion track models implemented in commercial TCAD simulators usually propose an exponential function or a Gaussian function for the spatial distribution function

$$R(w) = \frac{1}{\pi r_c^2} \exp\left[-\left(\frac{w}{r_c}\right)^2\right] \quad (40)$$

where  $r_c$  is the characteristic radius of the Gaussian function. The temporal distribution function is usually modeled by a Gaussian function

$$T(t) = \frac{1}{t_c \sqrt{\pi}} \exp\left[-\left(\frac{t}{t_c}\right)^2\right] \quad (41)$$

where  $t_c$  is the characteristic time of the Gaussian function. The characteristic time and the characteristic radius are two

key parameters for tuning the radiation-induced pulse duration and the ion track width, respectively, during a simulation run.

Fig. 15(a) and (b) provides two examples of TCAD simulations. In Fig. 15(a), a 65-nm nMOS transistor was impacted by a 5-MeV alpha particle striking the center of the drain perpendicularly to the device. The radiation-induced charge was generated along the particle track using (36) with a characteristic radius of 20 nm and a characteristic time of 2 ps. In Fig. 15(b), a more complex event, requiring the simultaneous generation of five ion tracks in a 32-nm nMOS transistor was performed [88]. This simulation aimed at reproducing the impact of a high energetic neutron (233 MeV) in the device, initiating a nuclear reaction with a silicon nucleus of the target material ( $n + {}^{28}\text{Si} \rightarrow 3n + 2p + 2\alpha + {}^{16}\text{O}$ ). The linear density of charge deposited by the secondary ions and the ion track were assumed to have a Gaussian radial distribution with a characteristic radius of 30 nm. The device simulation was performed using the DD method in the 3-D TCAD simulator Hyper Environment for Exploration of Semiconductor Simulation (HyENEXSS). In Fig. 15(b), the time evolution of the electron density and the potential is shown after the five ion tracks were simultaneously created. Within tens of ps, the distortion of potential is formed and the charge collection by drift is enhanced. The potential variation becomes relaxed with time. The variations of the transient current response and the collected charge as a function of time (not shown here, see [88]) show that an initial high drain current is induced due to drift. After about 100 ps, the potential distortion disappears, and diffusion dominates the charge collection process.

## V. MIXED MODE AND CIRCUIT SIMULATION

Simulation at circuit level is essential for studying, understanding, and anticipating the impact of radiation on the real circuit operation and architecture, not reducible to a single device isolated from the rest of the circuit. A wide variety of techniques can be envisaged. First, we can distinguish two main approaches.

- 1) The methods based on SV(s) at the device or circuit level that considers scoring quantities (deposited energy, LET, ...) and related criteria (critical charge, threshold LET,  $I_{\max} - t_{\max}$ , ...) to evaluate the SEE event rate of a given device/circuit architecture. In these methods, the electrical operation of the device/circuit of interest is implicitly considered in the criterion used to determine if a given event is able or not to induce an error.
- 2) The methods are based on a device/circuit electrical simulation to determine the impact of a given radiation on the circuit operation. In this case, the electrical operation is performed explicitly using various techniques. These include pure circuit simulation (SPICE), mixed-mode approaches, and full numerical methods (TCAD). The “stimulus signal” (current or voltage transient) resulting from the passage of a particle in the sensitive region of the device/circuit can be obtained from different models able to catch, more or less accurately, the complex physics of the transport and collection of the radiation-induced charge. These models include

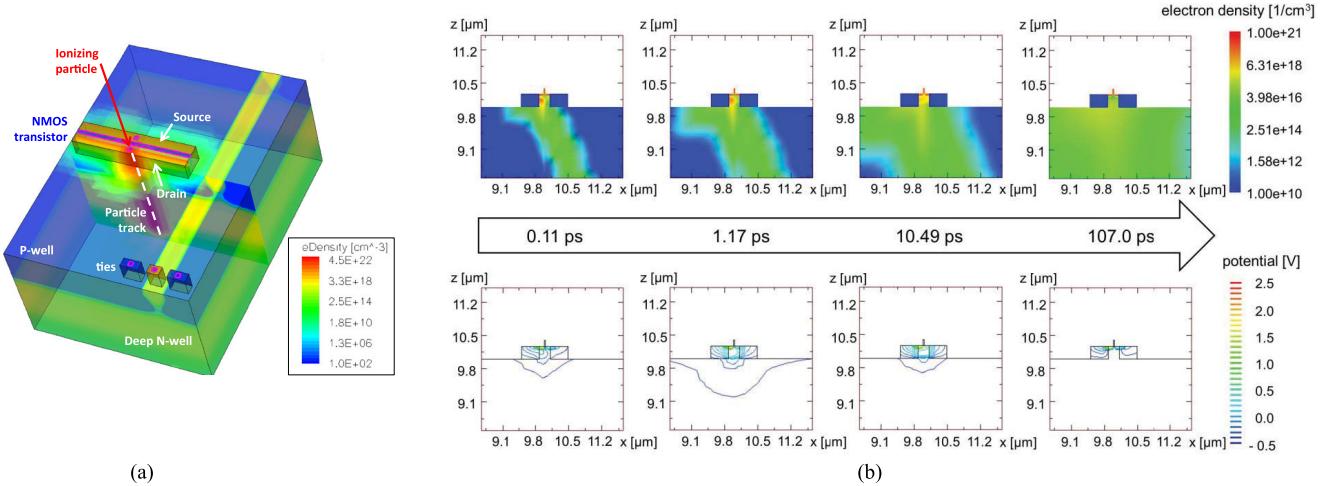


Fig. 15. (a) 3-D electron density distribution obtained by TCAD simulation at 2 ps after an alpha particle strikes the drain of an OFF-state isolated nMOS transistor (designed in 65-nm CMOS technology). To facilitate the picture analysis, spacers, gate material, and isolation oxide are not shown here. The long arrow indicates the location and direction of the ionizing particle strike (reprinted from Autran et al. [78], ©Elsevier 2014). (b) Time evolution of the electron density and the electrostatic potential in a 32-nm NMOSFET after the simultaneous generation of five ion tracks, created to simulate the nuclear reaction  $n + {}^{28}\text{Si} \rightarrow 3\text{n} + 2\text{p} + 2\alpha + {}^{16}\text{O}$  initiated by a 233-MeV neutron in the device. (After Abe et al. [88], ©IEEE 2011.)

the diffusion-collection models (see Section IV-B), the RWDD approach (see Section IV-C), and other full numerical methods, such as TCAD, or more sophisticated solutions of the transport problem treated using the Green's function formalism [21].

In the following, without wishing to be exhaustive, we examine a few approaches to illustrate this variety of methods that exist to investigate SEEs at the circuit level.

#### A. Circuit Simulation With Analytical SET Current Pulses

Circuit simulators solve systems of equations that describe the electrical operation of circuits, such as Kirchhoff's current and voltage laws. The basic components of these codes are compact models describing the operation of all elementary devices (transistors, diodes, resistors, etc.,) constituting the circuit. For simulating SEEs at the circuit level, a single-event-induced transient is usually modeled as a current source connected at the struck node of the circuit. Different models exist for reproducing the shape of the SET that is experimentally measured or obtained via full numerical simulation. One of the most popular solutions is the use of a double exponential current transient pulse, originally proposed by Messenger [89]

$$i_{\text{inj}}(t) = \frac{Q}{t_f - t_r} [\exp(-t/t_f) - \exp(-t/t_r)] \quad (42)$$

where  $Q$  is the collected charge (i.e., the integral of the pulse),  $t_r$  is the rising time constant, and  $t_f$  is the falling time constant. In principle, the same current model may be used for simulating the particle hits in both P-type channel (pMOS) and N-type channel (nMOS) MOS transistors, and the only difference will be in the direction of the current flow at the level of the current source implemented in the circuit netlist [90].

Numerous other models for the SET-induced current have been proposed. Andjelkovic et al. [90] have proposed a classification. The authors distinguished six major groups of models, respectively, based on: single voltage-independent

current sources, voltage-dependent current sources, two voltage-independent current sources, piecewise interpolation, lookup table, as well as an alternative approach to the current injection models employing a switch and a series resistor to reproduce the SET response. These different approaches have both advantages and drawbacks in terms of accuracy, implementation, and calibration, which should be considered in practical applications. For example, in (42), the time constants  $t_r$  and  $t_f$  are technology-related. According to [89], the time constant  $t_f$  can be expressed by

$$t_f = \frac{k\epsilon_0\epsilon_{\text{Si}}}{q\mu N} \quad (43)$$

where  $\epsilon_0$  is the permittivity of vacuum,  $\epsilon_{\text{Si}}$  is the relative permittivity of silicon,  $q$  is the electron charge,  $\mu$  is the minority carrier mobility, and  $N$  is the substrate doping density of the collecting junction. There is no straightforward equation to determine the value of  $t_r$ , but it is generally given in terms of  $t_f$ , as reported in [90]: for example,  $t_f = 3.28 \times t_r$  in [91] and  $t_f = 4.6 \times t_r$  in [92]. In general, the value of  $t_r$  is in the range from several ps to tens of ps, while the value of  $t_f$  is in the range from tens of ps to hundreds of ps.

Another SET model has been proposed by Kauppila et al. [93]. This model is a compact voltage-dependent SET current model that associates in parallel an independent current source  $I_{\text{SRC}}$ , a capacitor  $C_S$ , and two voltage-dependent current sources  $G_{\text{REC}}$  and  $G_{\text{SEE}}$ . The capacitor  $C_S$  stores the charge which is equivalent to the SET and its value can be chosen arbitrarily. The independent current source  $I_{\text{SRC}}$  is basically the standard double-exponential current source and the two sources  $G_{\text{REC}}$  and  $G_{\text{SEE}}$  account for the recombination process and the variation of the node voltage due to the induced charge, respectively. As noted by Andjelkovic et al. [90] in their review, the current model proposed by Kauppila et al. [93] allows the SET-induced current to be accurately characterized, particularly the plateau observed for high LET values when the

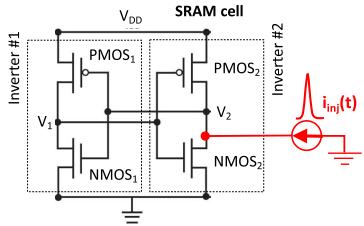


Fig. 16. Circuit schematic of an SRAM cell formed by two cross-coupled CMOS inverters. The passage of a particle in the nMOS<sub>2</sub> drain is electrically simulated with an external SET current source connected to the struck node.

impacted junction is embedded in a CMOS inverter (see also Section V-B).

Fig. 16 shows the circuit schematic of a generic four-transistor static random access memory (SRAM) cell. The passage of an ionizing particle in the nMOS<sub>2</sub> drain is electrically simulated with an external SET current source connected to the struck node. At this level, the aforementioned SET models can be used to provide a given SET transient pulse that is injected during the transient simulation. The selection of the SET current source is the user's choice.

To solve the transient simulation problem defined in Fig. 16, when the circuit architecture is composed of only a few connected devices, the steady-state circuit electrical solution can be simply solved considering Kirchoff's circuit laws and compact models for transistors. In the following, the method is illustrated for the case of the SRAM cell. Considering that the particle strikes the OFF- state nMOS transistor termed nMOS<sub>2</sub> (initial conditions  $V_1 = 0$  and  $V_2 = V_{DD}$ ), the time variations of potential  $V_2$  for the sole and isolated inverter #2 can be written as

$$\frac{dV_2}{dt} = \frac{-i_{inj}(t) + I_{DP2}(V_1 - V_{DD}, V_2 - V_{DD}) - I_{DN2}(V_1, V_2)}{C_N} \quad (44)$$

where  $i_{inj}(t)$  is the current pulse given by (42) due to the particle strike and collected on node 2,  $I_{DN2}$  and  $I_{DP2}$  are the currents of the nMOS<sub>2</sub> and pMOS<sub>2</sub> transistors, respectively, and  $C_N$  is the node capacitance.  $I_{DN2}(V_{GS}, V_{DS})$  and  $I_{DP2}(V_{GS}, V_{DS})$  depend on two input parameters: the gate-to-source bias ( $V_{GS}$ ) and the drain-to-source bias ( $V_{DS}$ ). For example, in (44) for the pMOS transistor,  $V_{GS} = V_1 - V_{DD}$  and  $V_{DS} = V_2 - V_{DD}$ .

Considering now the full SRAM cell composed of the two cross-coupled inverters, we obtain the following system of two coupled differential equations:

$$\begin{cases} C_N \frac{dV_1}{dt} = I_{DP1}(V_2 - V_{DD}, V_1 - V_{DD}) - I_{DN1}(V_2, V_1) \\ C_N \frac{dV_2}{dt} = -i_{inj}(t) + I_{DP2}(V_1 - V_{DD}, V_2 - V_{DD}) - I_{DN2}(V_1, V_2). \end{cases} \quad (45)$$

Equation (44) for the sole and isolated inverter #2 or (45) for the SRAM cell can be easily solved in the time domain, using a fourth-order Runge–Kutta method [94] with a time step  $\Delta t$ .

In (45), nMOS and pMOS source-to-drain currents are modeled using a compact or analytical model, which is the

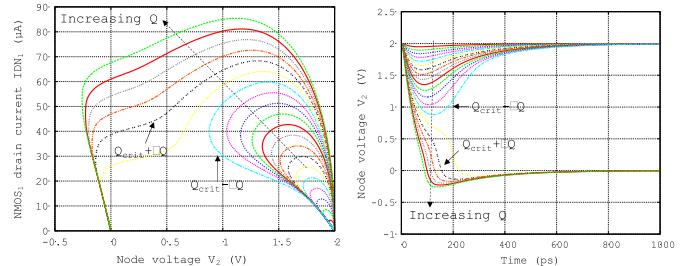


Fig. 17. Example of SRAM transient simulations based on (45) for different current pulses with increasing  $Q$  in (42). The cell upsets when  $Q$  becomes larger than  $Q_{crit}$ , the critical charge of the SRAM. Simulations performed for a generic 0.35- $\mu\text{m}$  CMOS technology using the C++ implementation of the EKV 2.6 MOSFET model [95], [96].

user's choice. One possible choice between all the transistor models available is the EKV 2.6 MOSFET model [95], [96] since it represents a very good compromise between accuracy and complexity. This is a predictive (scalable) compact model for the simulation of submicrometer CMOS technologies, considering the fundamental physical characteristics of the MOS structure. The drain current formulation can be coded in around 100 lines of C++. Fig. 17 illustrates the numerical solutions of (45) for an SRAM cell subjected to current pulses on node #2 (see Fig. 16) with increasing charge values  $Q$  in (42). The cell upsets when  $Q$  becomes larger than  $Q_{crit}$ , the critical charge of the SRAM.

For more complex circuit architectures than a single inverter or an SRAM cell, a circuit simulator must be used in the place of small and dedicated programs for circuit solving. An abundance of literature exists on the SE characterization methods of advanced CMOS technologies based on circuit simulation. A nice example is given by work conducted by Li and Draper [97] on both combinational circuits and sequential elements. They carried out a detailed analysis to characterize, using HSPICE,<sup>1</sup> the impact of single transients induced by one particle hit in various circuits, including redundant FF structures. They adopted the double exponential current pulse model (42) to describe the shape of the radiation-induced current pulse. Fig. 18(a) illustrates the characterization of a feedback redundant SEU-tolerant (FERST) FF, where circuit nodes N<sub>1</sub> and N<sub>3</sub> are coupled with N<sub>2</sub> and N<sub>4</sub>, respectively. To flip the stored value, two independent current sources Igen<sub>1</sub> and Igen<sub>2</sub> are attached to the cross-coupled nodes N<sub>1</sub> and N<sub>2</sub> with deposited charge  $Q_1$  and  $Q_2$ , respectively. The use of two current sources allows the effect of charge sharing [13], [98], [99] on the two circuit nodes N<sub>1</sub> and N<sub>2</sub> to be emulated. As a result of the particle strike, the stored value is changed when  $Q_1$  and  $Q_2$  are large enough, as depicted in the error map of Fig. 18(b). This table is built for each cross-coupled pair of nodes, which records the mappings from deposited charge values at the cross-coupled nodes to the result whether an error is induced, given a certain FF logic state and clock signal value. Similar steps are repeated for other cross-coupled nodes, e.g., N<sub>3</sub> and N<sub>4</sub>, to characterize the circuit.

### B. Radiation Transport Coupled With Circuit Simulation

The injection on a circuit node of a given “stimulus” signal, electrically emulating the impact of an ionizing radiation,

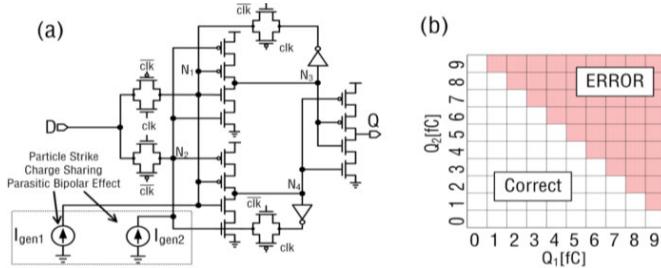


Fig. 18. (a) Example of hardened FF circuit characterization using two independent current sources that emulate charge-sharing effects induced by the particle strike on circuit nodes N<sub>1</sub> and N<sub>2</sub>. (b) Error map. (After Li and Draper [97], ©ACM 2017.)

does not necessarily correspond to reality, both regarding the real behavior of the circuit and its influence on the signal itself. Indeed, the process of collecting charges induced by radiation is a dynamic process: the charge (or the current) collected modifies the potential of the collector node and induces a counter-reaction of the circuit to this change, which will modify the collection process, and so on. To illustrate this effect, we explore the same case as in Fig. 14, but this time with the nMOS transistor embedded in a CMOS inverter. Because the device is now not isolated (standalone), the drain voltage is no longer fixed at the constant voltage V<sub>DD</sub>. The drain voltage corresponds to the voltage of node V<sub>2</sub> that depends on the operation of the second transistor of the CMOS inverter. This leads to the variation of the voltage V<sub>2</sub> during the transient process. These node bias changes may modify the charge collection efficiency at the drain of the nMOS transistor, through the variation of both the electric field F and the width of the SCR W<sub>SCR</sub> via a feedback process. To consider such a feedback effect, using the RWDD model, the magnitude of the current [given by (35)] varies at each time step due to the variations of W<sub>SCR</sub> and F that depend on the voltage node V<sub>2</sub>, which is also updated at each time step by the circuit simulator.

Simulated transients of the CMOS inverter (under the initial conditions V<sub>1</sub> = 0 and V<sub>2</sub> = V<sub>DD</sub>) obtained with the RWDD model when a 5-MeV alpha particle passes across the nMOS drain are shown in Fig. 19(a) and (b). These results reveal the influence of the circuit feedback on the SCR characteristics, through the time changes of V<sub>2</sub>. Without the circuit feedback on the SCR, the radiation effect turns V<sub>2</sub> to negative values for a period equal to about 30 ps. This obviously reveals a dummy condition for a cross-coupled inverter in the case of an SRAM cell (somewhat reduced by the gate capacitance in the case where the second inverter is coupled). Fig. 19(b) illustrates an important issue concerning the inverter operation: the dummy condition described above persists 2× as long when SCR feedback is activated.

In the most general case, where the radiation transport code is coupled with an external circuit simulator, a watchdog process is inserted between the radiation transport code and the circuit simulator to ensure that the two codes are working in interactive mode. The coupling between the two solvers requires an efficient exchange of numerical information at each iteration (time step), generally in the form of current

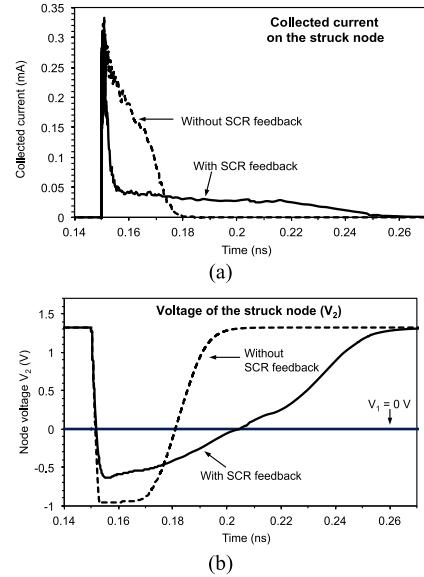


Fig. 19. (a) RWDD simulation of the impact of an ionizing particle on an OFF-state nMOS transistor embedded in a CMOS inverter with and without the feedback effect of the SCR (width and electric field dependence on V<sub>2</sub>) on the collected current and (b) on the voltage on the struck node. (After Autran et al. [78], ©Elsevier 2014.)

and voltage data. A simulation run consists of a certain number of simulation loops, each loop corresponding to a time incrementation (constant or variable time step) in the time-domain analysis. At each step, the radiation code transports the radiation-induced charge in the structure and the circuit simulator solves the circuit equations and updates the node potentials that are used in the next step for the radiation transport, and so on, until the entire time domain is covered.

Fig. 20 illustrates this mixed-mode methodology for an SRAM cell combining the RWDD transport model at the level of the spatial region limited to the impacted drain and SPICE simulation at the level of the four-transistor SRAM cell.

### C. Mixed-Mode TCAD Applied to SEEs

Mixed-mode TCAD tools [21], [30], [101] constitute a particular case of the previous solutions insofar as the coupling between the full numerical electrical simulation, including the radiation transport, and circuit simulation is directly included as “mixed-mode” or “mixed-level” simulation in all major commercial simulation suites, such as Synopsys [61], Silvaco [62], or Cogenda [63]. Often available in TCAD tools, this mixed-mode approach can be used in two different ways [101], as illustrated in Fig. 21 and discussed as follows.

- 1) The first possibility is to numerically simulate only a single transistor of the circuit, with all others simulated using compact models. This approach is the most used in circuit simulation, for applications needing to reproduce the operation of a particular device very accurately. An example of this approach is the simulation of radiation effects in memory cells. In this case, the device that needs to be numerically simulated is the device struck by the ionizing particle. Only the struck transistor is modeled in the 3-D device domain, the other transistors of the memory cell are simulated using compact models.

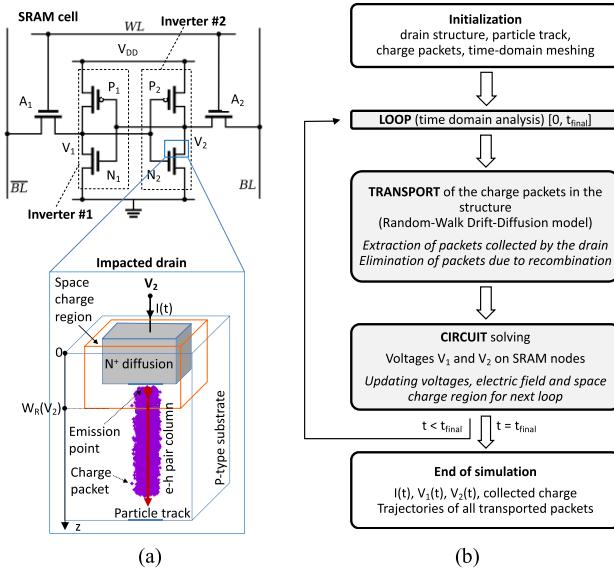


Fig. 20. (a) Mixed-mode methodology for an SRAM cell combining the RWDD transport model (impacted drain) and SPICE simulation and (b) simplified flowchart of the simulation. (Adapted after Moindjje et al. [100]. ©Elsevier 2019.)

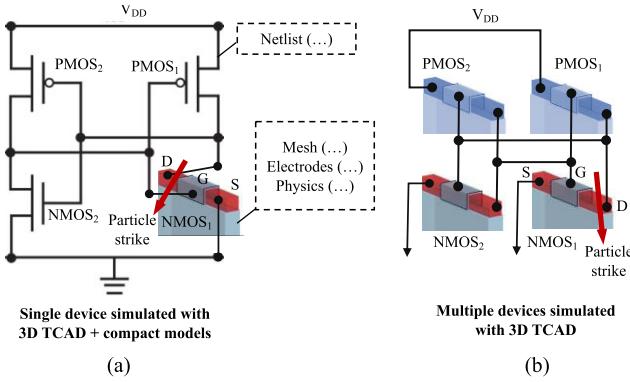


Fig. 21. Illustration of two mixed-mode approaches for the simulation of an SRAM cell with a: (a) single transistor or the (b) totality of the devices numerically simulated in the 3-D device domain and connected via a circuit netlist (the remaining transistors, in the first case, being simulated using compact models). (Adapted after Munteanu and Autran [102] and Munteanu et al. [103].)

The current transient resulting from the ion strike on the struck device is directly computed by device domain simulation. Thus, the inaccuracy of the circuit simulation due to the current transient used as a stimulus can be eliminated.

- 2) A second possibility is to numerically simulate all individual transistors of the IC and to connect them through the mixed-mode interface, which describes the operation of the total system. Computational resources and software constraints limit this type of simulation to circuits containing a maximum of a few tens of transistors (such as inverters, ring oscillators with few stages, individual memory cells, or FF latches).

In the mixed-mode approach, the two simulation domains (device and circuit) are closely connected by boundary conditions at contacts, and the two solvers exchange numerical information at specific intervals (iterations and time steps) and

at specific locations (boundaries of the TCAD 3-D model and the corresponding node/branch of the circuit schematic) [101]. For instance, the circuit simulator may calculate appropriate voltages and apply them at the TCAD 3-D model boundaries (contacts), and in response to the applied voltages, the TCAD solver calculates contact currents and feeds them back into SPICE [101].

This approach provides several interesting advantages. First, mixed-mode TCAD can capture the dynamic interaction of the physical charge collection process with the surrounding circuit [101]. Errors inherent to compact models or inaccuracies of input stimulus can be avoided by full device numerical simulation. It is also possible to access internal physical quantities of the numerically simulated device (such as potential, electric field, and densities of carriers) at any time during the mixed-mode simulation. Furthermore, mixed-mode approaches may be used to simulate the operation of small circuits made on emerging devices (such as ultrascaled multiple-gate or silicon nanowire-based architectures [102], [103], [104]) and/or to take into account new physical phenomena (e.g., quantum confinement [104] or quasi-ballistic transport) for which compact models do not exist or are still not satisfactory in terms of accuracy. In this case, all transistors contained in the small circuit can be simulated in the 3-D device domain. More particularly, the mixed-mode approach has been successfully used to simulate the ionizing radiation impact on these new devices and associated small circuits. The main drawback of the mixed-mode approach is the increased computational time compared to a pure circuit simulation. In addition, mixed-mode simulation is not feasible for complex circuits and in the case where there is a coupling effect (charge sharing) among adjacent devices. Given that the spacing between devices decreases when reducing the device dimensions, it is expected that coupling effects become increasingly important; in this case, the numerical simulation of the full circuit in the 3-D domain may become mandatory.

#### D. MC Circuit Simulation Using Specialized Codes

MC methods are computational methods that use random numbers to model stochastic processes, or to model deterministic processes that can be approximated by stochastic ones. The MC approach is the numerical method of choice for problems that model objects interacting with other objects or their environment based on simple object-object or object-environment relationships [105]. MC-based physical simulations of SEEs in electronics solve the radiation problem in two main steps: 1) the interaction of radiation with the device and the subsequent motion of charges and 2) the resulting changes in nodal currents and/or voltages, within the device/circuit [31], [49], [50]. Since this simulation chain is complex due to its multiscale and multiphysics character, the same simulation engine cannot generally cover these two steps. For example, the interaction of radiation with the device and the subsequent motion of charges can be fully simulated using a general-purpose code as previously cited (Section III-A) but the resulting changes at the device or circuit level require an electrical simulator or dedicated code. Due

to the computational cost (CPU time), the transport of the radiation-induced charges in step #1 is also often processed by another program or a specially designed code based on a simplified transport model and optimized algorithm.

Dozens of code developments in this domain have been reported in the literature. In 2013, an extended review article by Reed et al. [51] (completed with [54]) presented the contributions from different groups, each developing and/or applying MC-based radiation transport tools to simulate a variety of effects that result from energy transferred to a semiconductor material by a single particle event. The topics span from basic mechanisms for single-particle-induced failures to applied tasks such as developing websites to predict on-orbit single-event failure rates using MC radiation transport tools [51], [54]. Following on from [51] and [54], Table II proposes an updated list of the most recent codes, including several references published since 2013. To illustrate some basic principles and general properties of these specialized codes in the computation of SEEs, we now examine several examples from recent literature.

*Particle–Matter Interactions and Radiation Transport:* The first main difference between all these codes is the way in which the particle–matter interactions are generated, and the radiation transported. We can distinguish three main cases.

- 1) The code is built from the “ground up,” using nuclear and radiation transport physics or uses radiation transport libraries designed by the high-energy physics community (e.g., Geant4). Intrinsically, the code can directly compute, during a simulation run, all the steps related to incoming particle generation and source emulation, interaction event generation, ion transport through the device/circuit geometry, and finally scoring calculations with respect to SV(s). Additional routines can also be added to handle the transport of electric charges using various models. This approach is used in MRED or TIARA-G4.
- 2) The code uses a precompiled MC tool (e.g., FLUKA, PHITS, or MCNP) to perform similar calculations to the previous case, but in a more constrained framework because the exchange of information with the precompiled tool can only be done through input and output files which have a strict format. It is always possible to extend the code capabilities by external routines or to encapsulate the precompiled code in proprietary software by making a dynamic link and managing the inputs and outputs from the developed code in a transparent way for the user. It is also possible to transfer output data to another code to continue the SEE simulation at the electrical level. This approach is used in PHITS-HyENEXSS or G4SEE.
- 3) The code does not directly use MC radiation transport codes, libraries, or precompiled codes but directly computes and manages incident particle generation, particle–matter interactions, and charged particle transport itself, using precompiled event databases for nuclear interactions and additional data (SRIM tables [81], [82] or behavioral modeling [83]) to describe the transport of ions. This approach is preferentially used in

MC-ORACLE, MUSCA-SEP3, or TIARA, for example. The use of nuclear interaction event databases considerably reduces the computation time but requires a delicate treatment of the management of events in the case of complex architectures using several or many different materials.

*Energy Deposition, Charge Transport, and Collection:* The second differentiation criterion between these specialized codes is the way in which the particle energy is deposited, and the electrical charge is transported in the simulation domain and collected on the sensitive circuit node(s). Very schematically, two main approaches can be distinguished.

- 1) For the codes that consider a circuit as a set of SVs, the electrical charge deposited is directly deduced from the energy deposited by the particles at the level of these SVs. Therefore, the code performs particle calorimetry by considering the SVs as detectors. A deposited energy spectrum is then obtained. The scoring of the particles is carried out for each SV, which makes it possible to estimate the deposited charge by considering the average creation energy of the electron–hole pairs in the target material. More refined models, like nested SVs, deduced from separate TCAD simulation (as explained in Section IV-A), and implemented in MRED for example, can be used.
- 2) For codes that have a specific module to transport the electrical charge, energy is first deposited along the path(s) of the ionizing particle(s) traversing the simulation domain and converted to electron–hole pairs. The ambipolar transport of this charge in-excess starts and minority carriers are transported and then collected by the sensitive nodes that are, in this case, biased electrodes. Diffusion-collection models presented in Section IV-B can be used at this level, as performed in several codes, for instance, MC-ORACLE, MUSCA SEP3, or TIARA. Otherwise, a full numerical resolution of the Poisson and continuity equations can be performed, using internal solvers, as in MRED, or by outsourcing the task to an external program called via a dedicated IO interface, as performed for example in PHITS-HyENEXSS.

*Device/Circuit Response:* The electrical response of the impacted device, cell, or circuit can be deduced from a simple criterion, for example, a critical charge criterion, or from the  $I_{\max} - t_{\max}$  criterion as in MC-ORACLE or TIARA. Alternatively, a more complex criterion can be envisaged, considering a part or the totality of the circuit response simulated with a circuit simulator. The call to the circuit simulator can be invoked at the end of the charge transport and collection process or during the collection process itself, to take into account the circuit counter-reaction, as illustrated and discussed in Section V-B.

*3-D Circuit Construction and Link With the Electrical Circuit:* In addition to all the differences highlighted between these specialized MC codes, perhaps one of the most important is the ability of a given code to consider any complex circuit and to apprehend its complexity at different levels:

TABLE II

SPECIALIZED MC SIMULATION CODES APPLIED TO SEES IN ELECTRONICS CIRCUITS. THE ASTERISK INDICATES CODES PARTIALLY BASED ON GEANT4 SIMULATION TOOLKIT [38], [39]

Program name	Main ref.	Lab. Affiliation	Acronym definition / Short description
<b>ACCURO</b>	[122,123]	Robust Chip	Device and circuit simulation with fast single event analysis (commercial tool).
<b>MCEA*</b>	[125,126]	CEA-DIF	Monte Carlo code for estimating the SEU sensitivity of a memory array
<b>CLUST-EVAP, PROPSET, PROTEST</b>	[51]	NASA/Johnson Space Center	Monte Carlo proton reaction and transport codes
<b>CUPID</b>	[51]	Clemson University	Clemson University Particle Interactions in Devices
<b>FLUKA</b>	[40,41,51]	Fluka collaboration	General-purpose Monte Carlo energetic particle reaction and transport code
<b>GRAS*</b>	[51]	ESA	Geant4 for Radiation Analysis for Space
<b>G4SEE*</b>	[106,107,108]	CERN	Geant4 for SEE Monte Carlo simulation tool
<b>IRT*</b>	[58]	Intel	Intel Radiation Tool
<b>MCNP / MCNPX</b>	[42,43,51]	Los Alamos National Laboratory	Monte Carlo N-Particle eXtended / a software package for simulating nuclear processes
<b>MC-ORACLE</b>	[51,58,60]	University of Montpellier-2	Monte Carlo predictive code for SET and SEUs
<b>MRED*</b>	[31,49,50,51,127]	Vanderbilt University	Monte Carlo Radiative Energy Deposition
<b>MUSCA SEP3*</b>	[51,56,57]	ONERA	MULTI-SCAles Single Event Phenomena Predictive Platform / Monte Carlo SEE predictive tool
<b>NOVICE</b>	[51]	EMPC	Radiation transport/shielding code
<b>PHITS</b>	[44,45,51]	JAEA, RIST, KEK and other institutes	Particle and Heavy Ion Transport code System / a general purpose Monte Carlo particle transport code
<b>PHITS-HyENEXSS</b>	[52,124]	Kyushu University	Monte Carlo simulation code linking PHITS and HyENEXSS simulators
<b>SEMM / SEMM-2</b>	[46,47,48,51]	IBM	Soft Error Monte Carlo Model
<b>TFIT</b>	[109,110]	iRoC Technologies	Cell Level Soft Error Analysis (commercial tool)
<b>TIARA*</b>	[53,54,55,87], [111-121]	STMicroelectronics Aix-Marseille University	Tool suItE for rAdiation Reliability Assessment

at the material and device levels, at the circuit architecture level, and at the electrical level. In other words, a complete simulation platform should ideally be able to perform an SEE simulation with a maximum of details concerning the circuit architecture given from standard circuit definition files used in microelectronics: a schematic, a physical layout in Graphical Data Stream (GDS) format, and a transistor-level netlist. To perform this task, the code must create, at the beginning of the simulation sequence, a structure that represents the circuit both in the physical and electrical domains.

To illustrate this point, we take the example of the last version of the TIARA code, named TIARA Industrial Platform [55] that has extended capabilities in this domain. Malherbe [121] has described in detail the circuit-building processes implemented in TIARA: given a layout file of the circuit, a so-called Builder3D module constructs a 3-D structure of the circuit in the physical domain (Fig. 22). The module also takes as input a geometrical description of the technology

process stack: roughly speaking, the layout provides us with the top-view data (“x” and “y” coordinates), and the process stack is the side-view information needed to extrude the patterns into layers of a certain thickness along the “z”-axis. TIARA’s 3-D structures are collections of axis-aligned boxes, which seems a reasonable choice for the layouts in modern technologies, down to the device level. Note that layout files encode arbitrary polygons (closed chains of vertices), and thus, TIARA must first perform a meshing operation to convert the paths into nonoverlapping rectangles. After the geometrical structure of the circuit is built, the LVSmacher module is used to map physical locations to electrical nodes in the netlist. Such a physical-to-electrical mapping is needed for TIARA to identify the sensitive circuit nodes at which to inject the radiation-induced currents, when provided only with the geometrical location of the event [121]. This is performed by the LVSmacher module, which runs a custom layout versus schematic (LVS) comparison to match the layout and netlist

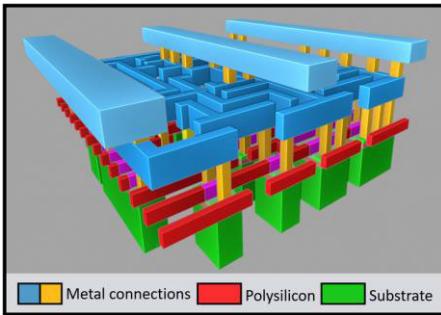


Fig. 22. Example of a generated 3-D structure by TIARA Industrial Platform (2021) corresponding to a 28-nm fully depleted (FD) silicon-on-insulator (SOI) FF circuit with two metal layers. (After Thery et al. [55], ©IEEE 2021.)

connectivity graphs. The complete description of this method can be found in [121].

*Data Postprocessing, Event Visualization, and Metrics Estimation:* All specialized MC codes have at least one or several dedicated modules to aggregate simulation results, prepare output files for event visualization and mappings using 2-D/3-D viewers, calculate histograms, and estimate various statistical metrics, such as the device/circuit cross section or the SER. The management of intermediate calculation files and log files are also important, to keep track of as many parameters as possible and to save them in correct final formats. Some aspects of data visualization and scoring that may have an important role in the verification of the convergence of an SER for a large-scale simulation, event visualization in the case of remarkable events, detailed scoring to better understand SEE mechanisms on a nuclear physics level, or event mapping to identify sensitive area at layout level can be found in [23], [127], and [128].

## VI. CIRCUIT-LEVEL SE ANALYSIS

SER estimation and analysis is an important challenge for very-large-scale integration (VLSI) circuits that cannot be simulated, due to their complexity, using a simulator or a specialized code. Historically, SEEs have first affected memory circuits because of the large area of the chips devoted to caches and the higher vulnerability of SRAM cells in comparison to combinational logic [16]. However, technology scaling, especially in the past decade, has increased the SER in logic circuits by several orders of magnitude, making it comparable to the SER of unprotected memory for modern technologies [129]. In what follows, we briefly examine the modeling of the SER in both memory circuits and in combinational logic.

### A. SER in Memory Circuits

In an SRAM circuit, for a given supply voltage and for a given drain architecture, the SER can be directly linked with the critical charge via an exponential relationship (suggested by the experiment), as originally established by Hazucha et al. [130] and Hazucha and Svensson [131] in the case of SEEs induced by high-energy atmospheric neutrons

$$\text{SER} = K \times F \times A \times \exp\left(-\frac{Q_{\text{crit}}}{\eta_S}\right) \quad (46)$$

where  $K$  is a scaling factor (assumed to have the same value for all technologies),  $F$  is the neutron flux with energy above 1 MeV ( $\text{cm}^2 \cdot \text{s}^{-1}$ ),  $A$  is the area of the circuit sensitive to particle strikes, in  $\text{cm}^2$ ,  $Q_{\text{crit}}$  is the critical charge, and  $\eta_S$  is the charge collection efficiency of the device for a given type of radiation, both expressed in the same unit (fc).

Two key parameters for SER are  $Q_{\text{crit}}$  and  $\eta_S$ . These model parameters are determined by fitting (46) to a set of experimental SER data and simulated critical charge data. A lower  $Q_{\text{crit}}$  means a priori more SEEs.  $\eta_S$  and  $Q_{\text{crit}}$  are determined by the process technology [131], whereas  $Q_{\text{crit}}$  also depends on characteristics of the circuit, particularly the supply voltage and the effective capacitance of the drain nodes, as we will analyze later in Section VI-C.  $Q_{\text{crit}}$  and  $\eta_S$  are essentially independent, but both decrease with decreasing feature size. Equation (46) shows that changes in the ratio  $-Q_{\text{crit}}/\eta_S$  will have a very large impact on the resulting SER. The SER is also proportional to the area of the sensitive region of the device, and therefore, it decreases proportionally to the square of the device size. Changing the supply voltage requires finding a new value for the collection efficiency  $\eta_S$  following a method proposed by Hazucha and Svensson [131].

Torrens et al. [132] analyzed the dependence of the SER on the design parameters of pull-down nMOS and pull-up pMOS transistors in regular parameter variation-tolerant 6T-SRAM cells. They used the expression proposed by Heijmen et al. [133], in which the SER is expressed for both the sensitive nMOS and pMOS of the SRAM cell as

$$\text{SER} = \kappa \left( A_{\text{diff},e} \times e^{-\frac{Q_{\text{crit},e}}{\eta_e}} + A_{\text{diff},h} \times e^{-\frac{Q_{\text{crit},h}}{\eta_h}} \right) \quad (47)$$

where  $A_{\text{diff},e}$  and  $A_{\text{diff},h}$  are the nMOS and pMOS sensitive drain area, respectively,  $Q_{\text{crit},e}$  and  $Q_{\text{crit},h}$  denote the critical charge for upsets due to the collection of electrons and holes at the sensitive drains of the nMOS and pMOS transistors, respectively, and  $\kappa$  is a parameter that depends on the radiation flux [ $\kappa = K \times F$  defined in (46)]. Parameters  $\eta_e$  and  $\eta_h$  are the charge collection efficiency for electrons and holes, respectively. To compute SER, parameters  $\kappa$ ,  $\eta_e$ , and  $\eta_h$  must be obtained experimentally (as they are device- and environment-dependent) [132]. In practice and as discussed in [132], (47) can be simplified to (46) and the SER can be computed from  $Q_{\text{crit},e}$  because  $Q_{\text{crit},e}$  is always inferior to  $Q_{\text{crit},h}$ . However, the model precision increases when both electron and hole collection are considered. To link the SER expression in (47) with the electrical and geometrical parameters of the SRAM cell, Torrens et al. [132] proposed an analytical model of  $Q_{\text{crit}}$  that will be discussed in Section VI-C. The analytical developments described in [132] allow calculating the critical charge and the SER from technological parameters giving insight into the relative contribution of each design parameter, notably the transistor geometry and the supply voltage.

### B. SER of Combinational Logic

Modeling and analyzing the SER in logic is more complex than in memory elements since there is an exponential number of input vectors, signal correlations, and combinations with

pulsewidths [134]. However, in combinational logic gates, the same considerations of  $Q_{\text{crit}}/\eta_S$  can apply to SET pulse generation. For a complete analysis, however, one must also consider how SET masking factors scale across process nodes. Indeed, there exist some masking effects that reduce the likelihood that a particular SET within a circuit will be latched and cause an error. These masking effects are commonly classified as follows [16], [30], [134].

- 1) *Logical Masking*: This occurs when a particle strikes a portion of the combinational logic that cannot affect the output due to a subsequent gate whose result is completely determined by its other input values. For example, as illustrated in Fig. 23(a), if the strike happens on an input to a NAND (NOR) gate but one of the other inputs is in the controlling state (e.g., 0(1) for a NAND (NOR) gate), the strike will be completely masked and the output will be unchanged (i.e., the particle strike will not cause an SE).
- 2) *Electrical Masking*: This occurs for transients with bandwidths higher than the cutoff frequency of the CMOS circuit. These transients will then be attenuated [135]. The pulse amplitude may reduce, the rise and fall times increase, and, eventually, the pulse may disappear [as shown in Fig. 23(b)]. On the other hand, since most logic gates are nonlinear circuits with substantial voltage gain, low-frequency pulses with sufficient initial amplitude will be amplified [134].
- 3) *Temporal Masking (or Latching-Window Masking)*: This occurs when the pulse resulting from a particle strike reaches a latch, but not at the clock transition where the latch captures its input value. This is explained in Fig. 23(c): when the transient propagates toward a sequential element (a latch in the present case), the disturbance on node DIN may be outside the latching window. Hence, the error will not be latched, and there will be no SE.

Due to these masking effects, the SER in combinational logic has been found to be significantly lower than expected. In addition to these masking mechanisms, two key factors impact the SER in combinational logic: the clock frequency and the SET pulsewidth [30]. With increasing clock frequency, there are more latching clock edges to capture a pulse that causes the error rate to increase. The pulsewidth is a key parameter which determines both the distance the that SET will travel through the combinational chain and the probability that the SET be latched in a memory element as wrong data. The wider the SET pulsewidth, the greater the probability it has of arriving on the latching edge of the clock. If the transient becomes longer than the period of the clock, then every induced transient will be latched. The SET pulsewidth and amplitude depend on both process and circuit parameters (substrate and/or epitaxial layer doping, circuit capacitance, etc.).

A wide variety of SER estimation methods and formulations exist in the literature with important differences that are not always clearly distinguished. Certain approaches assume particle hits at individual circuit nodes [136], [137], [138]; other models consider them on the gate as a whole [129]. Conditional and unconditional error models must be also

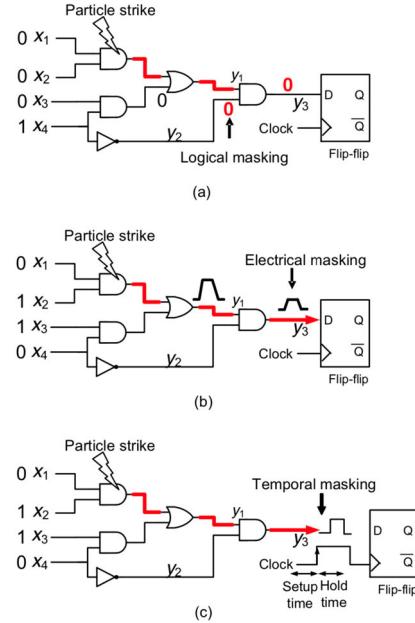


Fig. 23. Illustration of three masking effects: (a) logical; (b) electrical; and (c) temporal. (After Yu [136].)

distinguished. A conditional error model allows the error probability to vary with respect to different input vectors, while an unconditional error model requires the error probability to be constant and, therefore, independent of the input vectors [136]. As an illustration of the SER estimation methods developed, we briefly discuss in the following the approach developed by Anglada et al. [129]. In their recent work, the overall SER of a given combinational circuit can be computed as the accumulation of the individual SER of all the logic gates in the circuit [129]

$$\text{SER}_{\text{circuit}} = \sum_{i=1}^{N_{\text{gates}}} \text{SER}_{\text{gate}_i} \quad (48)$$

where  $\text{SER}_{\text{gate}_i}$  is defined as the probability that a particle with a particular charge  $q$  strikes at gate  $\#i$  and the SET originated is not masked.  $\text{SER}_{\text{gate}_i}$  is computed by integrating the product of the probability that a particle striking the gate causes an SET and the nonmasking probability over the range of charges able to induce an SE

$$\text{SER}_{\text{gate}_i} = K \times A_{\text{gate}_i} \times F \times \int_{Q_{\text{crit}_i}}^{\infty} f_Q(q) \times V(\text{gate}_i, q) dq \quad (49)$$

where  $K$  is an overall scaling factor,  $A_{\text{gate}_i}$  and  $Q_{\text{crit}_i}$  are the area and the critical charge for the gate  $\#i$ , respectively,  $F$  is the particle flux,  $V$  is the vulnerability of gate  $\#i$  for the collected charge  $q$  (defined below), and  $f_Q$  is the probability density function of collected charge, defined in [138] and [139] as a function of the charge collection efficiency  $\eta_S$

$$f_Q(q) = \frac{1}{\eta_S} \times \exp(-q/\eta_S). \quad (50)$$

In practice, the integral in (49) is often approximated as a discrete sum ( $N_C$  terms)

$$\text{SER}_{\text{gate}_i} = \sum_{c=1}^{N_C} R_{\text{PH}}(\text{gate}_i, q_c) \times V(\text{gate}_i, q_c) \quad (51)$$

$$R_{\text{PH}}(\text{gate}_i, q_c) = K \times F \times A_{\text{gate}_i} \times \exp(-q_c/\eta_S) \quad (52)$$

where  $q_c$  corresponds to a discrete charge selected from the continuous range:  $q_c = c \times (q_{\max} - Q_{\text{crit}})/N_C$ . In [129], it is reported that a discretization of the integral in five intervals yields an accurate enough SER estimation in comparison to SPICE models. The vulnerability of a gate is defined as the probability that an SE propagates up to a latch. It can be formulated as

$$V(\text{gate}_i, q_c) = \text{LM}(i, c) \times \text{EM}(i, c) \times \text{TM}(i, c) \quad (53)$$

which corresponds to the probability that the SET with charge  $q_c$  at gate # $i$  is neither affected by the logical masking factor (LM) nor the electrical masking factor (EM) nor the timing masking factor (TM). The computation of different nonmasking probability factors in (53) is a complex task that requires a specific calculation strategy for each type of masking. It must also include the reconvergent fanouts (when a logic signal splits into multiple branches and later reconverges in two or more inputs of a gate) that break the assumption that signal paths are independent [129], even if most of the gates are not sources of reconvergence. The complete algorithm to estimate the SER in a circuit from (48) and (51)–(53) is given and discussed in [129].

### C. Critical Charge Modeling in SRAM

As mentioned in Section IV-A, the critical charge ( $Q_{\text{crit}}$ ) is a first-order metric that has been introduced to characterize the circuit sensitivity to SEEs [18]. It corresponds to the minimum amount of charge induced during a particle strike that, after being transformed into current, will result in a change of logic level across the target node.  $Q_{\text{crit}}$  can be used as a parameter for assessing the circuit sensitivity to SETs induced in combinational logic and SEUs induced in sequential elements [18]. Since the value of the critical charge is used as input for the evaluation of the SER at a high-description level, accurate determination of the critical charge is of great importance for the design of radiation-tolerant circuits and systems.

In the case of an SRAM cell (Fig. 16),  $Q_{\text{crit}}$  can be simply modeled as a sum of capacitance and conduction components of the impacted node [30]

$$Q_{\text{crit}} = C_N V_{\text{DD}} + I_{\text{DP}} t_F \quad (54)$$

where  $C_N$  is the equivalent capacitance of the struck node,  $V_{\text{DD}}$  is the supply voltage,  $I_{\text{DP}}$  is the maximum current of the ON-state pMOS transistor (pMOS<sub>1</sub> in Fig. 16), and  $t_F$  is the cell flipping time. While both capacitance and conductance components indeed contribute to this critical charge, the first term is generally overestimated because the flipping threshold of an inverter is less than  $V_{\text{DD}}(V_{\text{DD}}/2)$  for perfectly matched

nMOS and pMOS). In addition, the conductance term only considers the peak value of the current, which is not realistic. A more correct way of estimating the critical charge has been proposed by Xu et al. [140]

$$Q_{\text{crit}} = \int_0^{V_{\text{trip}}} C_N dV + \eta I_P T_{\text{pulse}} \quad (55)$$

where  $V_{\text{trip}}$  is the static tripping point of the SRAM cell defined as the threshold voltage at the struck node required to flip the cell content,  $\eta$  is a correction factor,  $I_P$  is the driven current of the ON-state pMOS transistor, and  $T_{\text{pulse}}$  is the duration of the particle-induced current pulse  $I_{\text{pulse}}$ . Equation (55) provides a better estimation of the capacitance component of  $Q_{\text{crit}}$ , particularly the effect of junction capacitance and the addition of the backend metal-insulator-metal (MIM) capacitor. However, this model fails to incorporate the dynamics of the voltage transient at the struck node, the quantitative description of  $I_{\text{pulse}}$ , and the contributions of different transistors that constitute the cell. As a result, the accuracy of (55) in estimating  $Q_{\text{crit}}$  is also limited.

Improved analytical techniques for solving  $Q_{\text{crit}}$  in SRAM cells with reduced discrepancies ( $\leq 10\%$  and below with respect to full SPICE simulations) have been proposed in recent years by Zhang et al. [141], Jahanuzzaman et al. [142], Mostafa et al. [143], [144], and Torrens et al. [132]. These different models consider the dynamic behavior of the cell and decouple the nonlinearly coupled storage nodes with different approaches. Decoupling of storage nodes enables solving associated current equations to determine the critical charge, usually for a simple or double exponential pulse current.

Mostafa et al. [144] developed a full  $Q_{\text{crit}}$  analytical model, considering a decoupling solution for the system of differential nodal current equations at nodes #1 and #2 of the SRAM cell (Fig. 16)

$$\begin{cases} C_1 \frac{dV_1}{dt} = [i_{p1} - i_{n1}] - i_{\text{inj}}(t) \\ C_2 \frac{dV_2}{dt} = [i_{p2} - i_{n2}] \end{cases} \quad (56)$$

where  $C_1$  and  $C_2$  are the capacitances of the nodes #1 and #2, respectively,  $i_{p1}$  and  $i_{n1}$  (respectively,  $i_{p2}$  and  $i_{n2}$ ) are the currents of transistors pMOS<sub>1</sub> and nMOS<sub>1</sub> (respectively, pMOS<sub>2</sub> and nMOS<sub>2</sub>), respectively, and  $i_{\text{inj}}(t)$  is the transient current pulse connected here to node #1 and modeled by a simple exponential current pulse given by

$$i_{\text{inj}}(t) = \frac{Q}{\tau} \exp(-t/\tau) \quad (57)$$

where  $Q$  is the total charge deposited by this current pulse at the struck node, and  $\tau$  is the falling time.

After a long analytical development, the authors show that the critical charge can be expressed as follows:

$$Q_{\text{crit}} = Q[1 - \exp(-t_F/\tau)] \quad (58)$$

where  $Q$  is the total charge for a current pulse to be able to upset the cell, and  $t_F$  is the cell flipping time that has for final

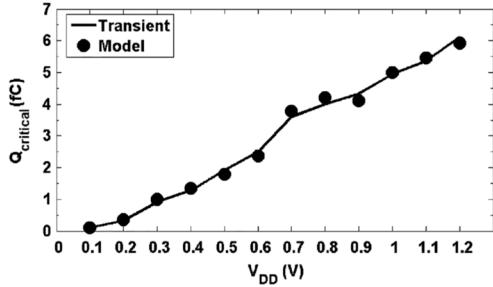


Fig. 24. Comparison of the critical charge versus  $V_{DD}$  as estimated using the analytical model [see (58) and (59)] and as deduced from transient SPICE numerical simulations considering technological and electrical parameters for a 65-nm CMOS bulk technology. (After Mostafa et al. [144], ©IEEE 2011.)

expression (using the branch  $W_{-1}$  of the Lambert function)

$$t_f = -\tau \left[ 1 + \frac{C_1 V_{DD}/2}{\tau [i_{p1} - i_{n1}]} \right. \\ \left. + W_{-1} \left( -\exp \left( -1 - \frac{C_1 V_{DD}/2}{\tau [i_{p1} - i_{n1}]} \right) \right) \right] \\ + \frac{C_2 V_{DD}/2}{[i_{p2} - i_{n2}]} . \quad (59)$$

In the above derivation, the different currents  $i_{p1}$ ,  $i_{n1}$ ,  $i_{p2}$ , and  $i_{n2}$  must be evaluated for the following and respective gate-to-source  $|V_{GS}|$  voltage values:  $V_{DD}$ , 0,  $V_{DD}/2$ , and  $V_{DD}/2$ . At this level, the use of a transistor analytical model can be envisaged. Mostafa et al. [144] suggest considering a unified physical current formula, which is used for all the transistor operating regions, as introduced in [145]. Another solution should be to use the EKV model [95], [96] introduced in Section V-A or another compact model. Fig. 24 illustrates the verification of the analytical  $Q_{\text{crit}}$  model [see (58) and (59)] with results obtained using SPICE transient simulations. The test circuit considered is a 65-nm CMOS bulk SRAM. The simulations have been repeated for different  $V_{DD}$  values (from 0.1 to 1.2 V), to find the effect of reducing  $V_{DD}$  on the critical charge. The maximum error reported is 7.2% on  $Q_{\text{crit}}$  values, and the average error is 3.8% with respect to SPICE results.

Another critical charge calculation model has been proposed by Torrens et al. [132] in the framework of a detailed analysis of the SER dependence on transistor design parameters for six-transistor SRAM cells (Fig. 25). In Fig. 25(a), the four transistors,  $M_{nL}$ ,  $M_{pL}$ ,  $M_{nR}$ , and  $M_{pR}$  correspond to the two identical cross-coupled inverters of the latch, while the other two,  $M_{xL}$  and  $M_{xR}$ , control the latch access during write and read operations. As explained by Torrens et al. [132], transistor widths  $W_n$ ,  $W_p$ , and  $W_x$  are usually selected to ensure cell stability during write and read operations. These constraints require that the cell ratio defined as  $CR = W_{nL,R}/W_{xL,R}$  must be greater than one (usually  $CR = 1.5\text{--}2.5$ ) and the pull-up ratio defined as  $PR = W_{pL,R}/W_{xL,R}$ , must be less than 3. Typically, to minimize cell area, the size of the pull-up transistors and pass transistors are chosen to be minimal ( $PR = 1$ ) [132]. In their study, the authors have explored the modification of transistor widths as a memory cell hardening technique by increasing the minimum allowed widths by a given factor.

To maintain a regular layout structure, the widths of all pMOS transistors are incremented by a factor  $r_p$  with respect to the minimum allowed width  $W_{\min}$ , while the widths of all nMOS are incremented by a factor  $r_n$ . Such layout modifications prevent the formation of bends in the diffusion regions and maintain the layout structure:  $W_p \equiv W_{pL} = W_{pR} = r_p \times W_{\min}$  and  $W_n \equiv W_{nL} = W_{nR} = W_{xL} = W_{xR} = r_n \times W_{\min}$ . To evaluate the SER from (46), the authors developed a critical charge model embedding in the equations the transistor and cell geometry. Starting from (55), they first expressed the critical charge  $Q_{\text{crit},h}$  related to the collection of holes at the drain of  $M_{pR}$  required to flip node  $R$  from 0 to 1 and  $Q_{\text{crit},e}$  related to electron collection at the drain of  $M_{nL}$  required to flip node  $L$  from 1 to 0. They obtained

$$Q_{\text{crit},h} = C_R V_{\text{trip}} + \eta |I_{DN}| T_{\text{pulse}} \quad (60)$$

$$Q_{\text{crit},e} = C_L (V_{DD} - V_{\text{trip}}) + \eta |I_{DP}| T_{\text{pulse}} \quad (61)$$

where  $C_R$  (respectively,  $C_L$ ) is the equivalent capacitance of the R node (respectively, L node),  $I_{DN}$  (respectively,  $I_{DP}$ ) is the maximum driving current of the ON-state  $M_{nR}$  (respectively,  $M_{pL}$ ) device,  $T_{\text{pulse}}$  is the duration of the particle-induced current pulse, and  $\eta$  is a correction factor to account for the time-varying behavior of the restoring current. Here, because of the symmetry of the six-transistor SRAM cell,  $C_R = C_L = C$  with  $C$  given by

$$C = C_{gn,p} A_n + C_{gp} A_p + C_{gon} W_n + C_{gop} W_p \\ + C_{jan,p} A_{\text{diff},n} + C_{jswn} (2H_n) + C_{jap} A_{\text{diff},p} \\ + C_{jswp} (W_p + 2H_p) \quad (62)$$

where  $C_{gn,p}$  is the nMOS and pMOS intrinsic gate capacitance,  $A_{n,p} = W_{n,p} \times L$  is the gate area,  $C_{gon,p}$  is the overlap capacitance,  $C_{jan,p}$  and  $C_{jswn,p}$  are the source/drain junction area capacitance and the sidewall capacitance, respectively,  $A_{\text{diff},n} = W_n \times H_n$  and  $A_{\text{diff},p} = W_p \times H_p$  are the nMOS and pMOS diffusion areas [Fig. 25(b)], respectively, and  $H_n$  and  $H_p$  are the respective drain diffusion lengths.

Describing the transistor current in the saturation region using the alpha-power law model, and after several substantial analytical developments not detailed here, the authors showed, from calculated data using their model, that the critical charges  $Q_{\text{crit},e}$  and  $Q_{\text{crit},h}$  are quasi-linear functions of  $W_n$  and  $W_p$ . Setting  $W_p = r_p \times W_{\min}$  and  $W_n = r_n \times W_{\min}$ , the two critical charges can be approximated by linear relationships with coefficients  $r_n$  and  $r_p$  in the form

$$\begin{cases} Q_{\text{crit},e} = Q_{0,e} + \chi_{n,e} \times r_n + \chi_{p,e} \times r_p \\ Q_{\text{crit},h} = Q_{0,h} + \chi_{n,h} \times r_n + \chi_{p,h} \times r_p \end{cases} \quad (63)$$

where the six parameters are fitted from calculated data using the complete analytical model for  $Q_{\text{crit},e}$  and  $Q_{\text{crit},h}$  described in [132]. The maximum discrepancy between the complete analytical model and the linearized equation (63) is below 0.5%. Fig. 26 shows a surface representing the calculated SER from (46) using the modeled critical charges as a function of  $r_n$  and  $r_p$ . The five points labeled SS, SM, SL, MM, and LS correspond to experimental data measured on 65-nm SRAM circuits during alpha particle accelerated SER tests. The five memory blocks correspond to different couples of values for

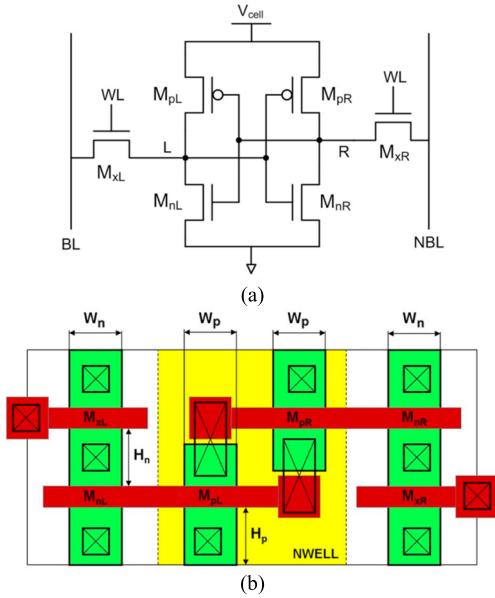


Fig. 25. (a) Schematic and (b) layout of a six-transistor SRAM cell with the definition of transistor names and key-geometrical dimensions. (After Torrens et al. [132], ©IEEE 2014.)

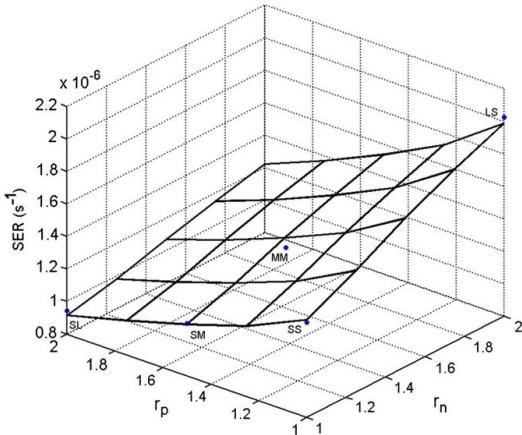


Fig. 26. Surface representing the calculated SER (from (46) using the modeled critical charges) as a function of  $r_n$  and  $r_p$  along with experimental data points. The parameters used in the model are related to a 65-nm CMOS process (see [145] for their numerical values). (After Torrens et al. [132], ©IEEE 2014.)

$r_n$  and  $r_p$  [132]. Both experimental and simulated SER values show that increasing  $r_p$  leads to a desired SER reduction, whereas increasing  $r_n$  produces an undesired SER increment. SL cell ( $r_n = 1$  and  $r_p = 2$ ) is the best cell in terms of SER. Results show that a direct correlation between SER and the critical charge is found for all cells having small nMOS ( $r_n = 1$  for SS, SM, and SL), and a higher critical charge corresponds to a better SER.

However, not all transistor width enlargements result in a SER improvement. Only pMOS width increase provides an SER improvement, whereas nMOS width increase worsens the cell behavior in terms of SER. While cells SL and LS have the same cell area, the LS-cell SER is twice the SER of the SL one. These very interesting results reveal that SER is reduced by increasing the pMOS transistor channel width when simultaneously maintaining the minimum width

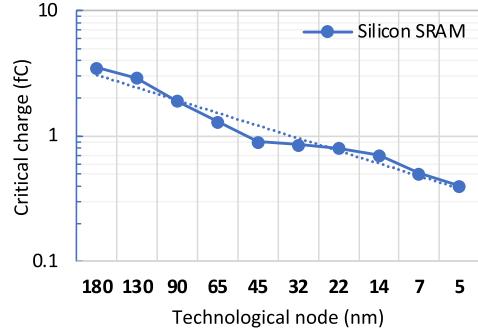


Fig. 27. Typical values of critical charges reported in the literature for silicon SRAMs as a function of the technological node of the International Technology Roadmap for Semiconductors (ITRS). (Data after [146], [147], and [148].)

for nMOS. As an increase in  $W_p$  also reduces cell writability, a tradeoff must be therefore established.

Previous models, TCAD, mixed-mode, or full SPICE simulations can be used to study the scaling of  $Q_{\text{crit}}$  as a function of transistor/circuit feature sizes and geometries. To conclude, Fig. 27 shows that, for recent technologies,  $Q_{\text{crit}}$  values are now well below the femtocoulomb, an extremely low value of a few thousands of electrons, typically in the same order of magnitude as the charge deposited by very low LET particles, for example, a muon or an energetic electron, in a few nanometers of silicon.

#### D. Critical Charge Modeling in Sequential Circuits

SEEs are also serious design issues in sequential circuits because if a transient fault or glitch occurs at the output of a latch/FF, for example, it may lead to a noncritical path turning into a critical path. A conventional D-latch or FF is, thus, very sensitive to SEE due to high-energy particle strikes. During the low phase of the clock signal, an SEE may upset the logic level of the positive edge-triggered FF, and the corrupted values are not corrected until a new value is stored in the FF. Kumar et al. [149] developed an accurate semianalytical model to estimate the critical charge for a static D-latch operating in the sub/near-threshold regime. The proposed model is a function of design parameters such as transistor sizes, supply voltage, and fan-out (FO) load.

Fig. 28 depicts the conventional static D-latch circuit studied [149]. It has two paths: the first is the main path which consists of an inverter and the second is the feedback path which consists of an inverter followed by a transmission gate. The static D-latch stores two complementary binary values (0 and 1) at intermediated nodes  $N_1$  and  $N_2$ . This conventional latch is more prone to particle strike on intermediated nodes in hold mode ( $\text{CLK} = 0$ ) because, in this state, the intermediate nodes are disconnected from the input (IN) of the latch. A particle strike on node  $N_1$  (which is held at logic 1) is emulated using a current source  $I_{\text{SEE,trip}}$  injecting a double exponential current pulse of integral  $Q$ . The minimum voltage value at node  $N_1$  at which node  $N_2$  flips from logic 0 to logic 1 is termed as  $V_{\text{lubb}}$ . In this case, the pMOS transistor ( $M_{p1}$ ) of inverter  $I_1$  turns on and changes the logic level of node  $N_2$ . The critical charge model developed in this study is based on the

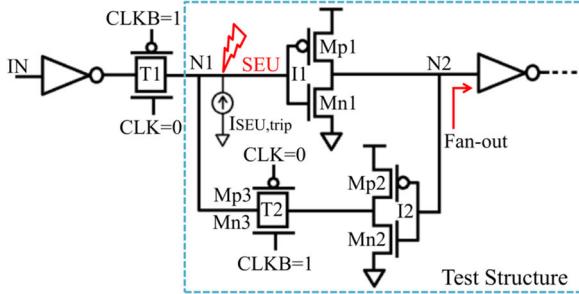


Fig. 28. Static D-latch, which is most commonly used, is susceptible to SEU due to transient fault at node N<sub>1</sub> or equivalently at node N<sub>2</sub>. (After Kumar et al. [149], ©IEEE 2019.)

fact that node N<sub>2</sub> is charged from 0 to V<sub>2C</sub> (the tripping point voltage at node N<sub>2</sub>) through the transistor M<sub>p1</sub> (current I<sub>Mp1</sub>). The current through transistor M<sub>n1</sub> (I<sub>Mn1</sub>) can be neglected because of its negative V<sub>GS</sub>. Because of the SEU charging of N<sub>1</sub>, V<sub>GS,p1</sub> is nearly equal to V<sub>DD</sub> while V<sub>GS,n1</sub> is nearly equal to 0. This is because the value of V<sub>lebb</sub> varies from 20 to -49 mV for an FO parameter between 0 and 8. Now, Kirchhoff's current law at node N<sub>2</sub> due to SEU on node N<sub>1</sub> can be written

$$C_{N2} \frac{dV_2}{dt} = I_{Mp1} \quad (64)$$

where C<sub>N2</sub> is the total capacitance at node N<sub>2</sub>. In the subthreshold region, the subthreshold current can be approximated at low V<sub>DS</sub> by [150]

$$C_{N2} \frac{dV_2}{dt} \approx I_0 \exp\left(\frac{V_{GS,p} - |V_{th,p}|}{nV_T}\right) \quad (65)$$

with  $I_0 = \mu_0 C_{ox} (W/L) (V_T)^2 \times \exp(\lambda V_{DS})$ , where V<sub>T</sub> is the thermal voltage,  $\mu_0$  is the low-field mobility, W and L are the channel width and length, respectively, C<sub>ox</sub> is the gate capacitance per unit area, and  $\lambda$  is a technological parameter. Knowing that V<sub>GS,p</sub> = V<sub>DD</sub> - V<sub>lebb</sub>, this last quantity can be extracted from (65)

$$V_{lebb} = (V_{DD} - |V_{th,p}|) - nV_T \times \ln\left(\frac{C_{N2}(dV_2/dt)}{I_0}\right). \quad (66)$$

Once the voltage at node N<sub>1</sub> is equal to V<sub>lebb</sub>, the feedback path (inverter followed by transmission gate I2-T2) charges node N<sub>1</sub> until V<sub>2</sub> = V<sub>2C</sub> when it stops charging N<sub>1</sub>. Therefore, the critical charge Q<sub>crit</sub> is obtained as follows:

$$Q_{crit} = (V_{DD} - V_{lebb}) \times C_{N1} \quad (67)$$

where C<sub>N1</sub> is the total capacitance at node N<sub>1</sub>. Equations (66) and (67) constitute the core equations of the model proposed by Kumar et al. [149] to evaluate the critical charge for the static D-latch. In (66), the slope dV<sub>2</sub>/dt must be evaluated as a function of the FO load, which requires some additional simulations and calculations detailed in [149]. The proposed methodology estimates the critical charge of the static D-latch with a maximum error of 3.4% at different power supplies compared with circuit simulations for a CMOS bulk 65-nm technology, as illustrated in Fig. 29. The model also results in a 7.5% error at the 32-nm technology node, which is verified

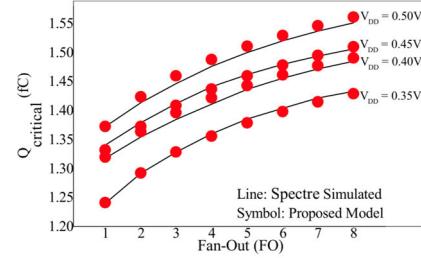


Fig. 29. Validation of the proposed model with SPECTRE simulation for critical charge calculation at V<sub>DD</sub> = 0.35 V, V<sub>DD</sub> = 0.4 V, V<sub>DD</sub> = 0.45, and V<sub>DD</sub> = 0.5 V in STMicroelectronics 65-nm CMOS technology. (After Kumar et al. [149], ©IEEE 2019.)

using a calibrated TCAD simulation setup [149]. Note the very low values of Q<sub>crit</sub> in this case: the susceptibility of sequential elements to SEE is high in the near-/subthreshold regime due to their low operating voltage and smaller node capacitances. Finally, the model proposed in [149] can predict the changes in the critical charge accurately for different process corners. This methodology also addresses the issue of critical charge due to process, supply voltage, and temperature (PVT) variations.

## VII. HIGH-LEVEL DESCRIPTION AT THE SYSTEM LEVEL

At the system level, the distinction is generally made between faults and data errors. As defined by Jeong et al. [151], a fault can be classified into a hardware or a software fault depending on where it occurs. A hardware fault, affecting a circuit or system, can be classified into a permanent, an intermittent, or a transient fault according to how long it exists in the considered device. A permanent fault (stuck-at, stuck-open, and bridging faults) remains permanently in the circuit, a transient fault appears and disappears over a brief period of time, and an intermittent fault introduces repetitive broken data in a specific place because of hardware damage [151]. Permanent and intermittent faults occur because of inaccurate specifications, implementation mistakes, or component defects. A transient fault usually occurs because of internal and external perturbation. The data errors that result from a hardware fault include hard and SEEs. The definitions and classification introduced for these errors in Section II-A fully apply at this level.

To evaluate system reliability and dependability, the technique of FI has been widely adopted. This ensemble of methods is intended to test the behavior of an application running on a given system and to evaluate its tolerance to faults under a realistic set of input stimuli that mimic the final execution environment. Briefly, the basic environment of the FI method includes an FI system and the target system under test (see Fig. 30) [151]. The FI system interacts with the target system for fault generation, control, and analysis. The FI methods can be generally classified into four techniques as follows: hardware-based FI (implemented on the real system hardware), software-based FI (only the code execution on the system is modified), simulation-based FI [using computer simulation tools for circuit/system emulation and FI, see Fig. 30(a)], and emulation-based FI (faults are injected into a design implemented in an FPGA circuit).

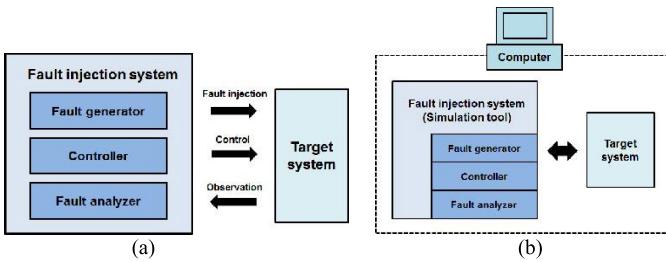


Fig. 30. (a) Fundamental environment of the FI method. (b) SFI. (After Jeong et al. [151], ©EEI, 2016.)

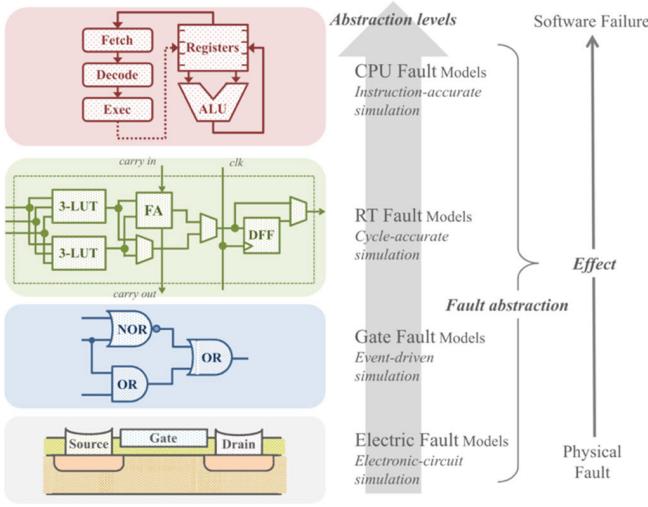


Fig. 31. CPU fault simulation taxonomy. Fault simulation at different abstraction levels is a tradeoff between accuracy and simulation performance. (After Ferrareto and Pravadelli [152], ©Springer, 2016.)

For modeling and simulation of SEEs at the system level, simulation-based fault injection (SFI) is a nonintrusive approach that offers a maximum amount of observability and controllability. As illustrated in Fig. 31, SFI approaches can be based on analysis at different abstraction levels, thus enabling different SFI approaches [152].

The lowest level, at the circuit simulation level, provides more accurate results but becomes impractical, for time-consuming and computational resource reasons, for evaluating a complete CPU and a software stack on top of it (see [152]). Event-driven (gate-level modeling using hardware description language (HDL) at register transfer level—RTL) simulations are also usually far from being acceptable to simulate a complete CPU. At this other extremity of the system simulation chain, the fastest solutions are represented by purely functional simulators that can almost reach the speed of the simulated hardware. However, simulating low-level faults could be very misleading when the simulation is only functional [152]. A very interesting tradeoff between accuracy and simulation performance is provided by SFI solutions based on instruction-accurate VPs. They are also increasingly adopted for exploring and anticipating before hardware implementation how a system responds to faulty conditions. A VP is a full-system simulator that emulates hardware components (e.g., CPUs and memories), and the execution of real software stacks, on the same machine, as it is running on

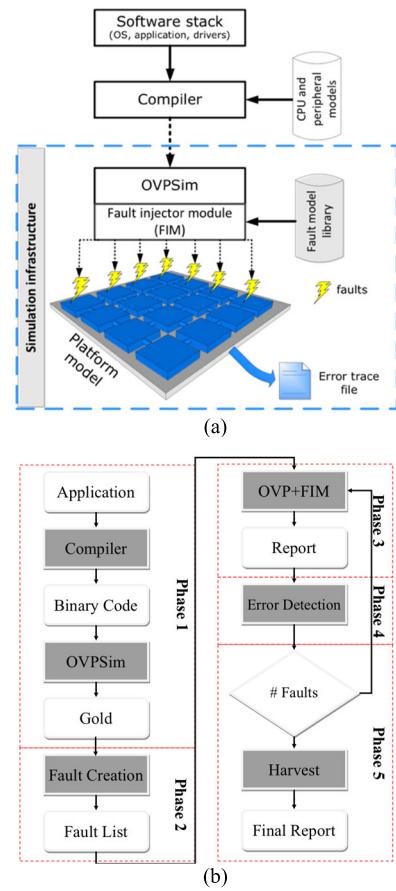


Fig. 32. (a) Proposed FI framework organization using OVPSim-FIM. (b) Five phases of the proposed FI flow. (After Rosa et al. [155], ©IEEE, 2015.)

real physical hardware [153]. Instruction-accurate VPs, such as QEMU [152], [154] or OVPSim [68], [153], [155], [156], are based on a dynamic binary translation engine, which enables simulation running real applications at the speed of hundreds of millions of instructions per second (MIPS). These VPs offer a large collection of component models, including processor architectures, peripherals, and memory models. They also facilitate FI implementation and fault analysis due to their design flexibility and debugging capabilities [152].

In the study reported by Rosa et al. [153], [155], SEs were modeled as data errors under the form of single-bit, multiple-bit, or event upsets that are generated randomly in registers or memory addresses during the execution of a given software application. To configure, monitor, and detect errors during system simulation, a fault injection module (FIM) has been developed in the framework of OVPSim, as illustrated in Fig. 32(a). This module is used to select, from a fault model library (FML), the most appropriate FI model for each set of platform components (e.g., processors, buses, routers, or memory types) [153]. The FIM is also responsible for monitoring the target processor, accessing resources as memories and registers, injecting the faults, capturing unexpected events arising from the simulator, extracting information, and analyzing errors [155].

A typical FI flow comprises five phases, as shown in Fig. 32(b) (a complete description of this flow can be found

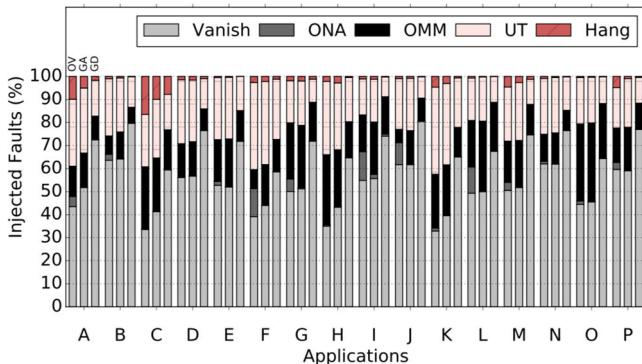


Fig. 33. Benchmarking of 8000-FI campaigns for a multicore ARM Cortex-A9 processor performed on three different SFI setups: OVPsim-FIM (OV), gem5-FIM atomic (GA), and gem5-FIM detailed (GD). (After Rosa [156].)

in [155] and [156]). Briefly, in phase 1, the simulation infrastructure cross-compiles the application source and simulates it on the VP to verify its correctness. It also extracts information using a gold standard, which is required for fault creation [153]. Phase 2 creates register or memory fault patterns consisting of injection time, a target, and a fault mask (i.e., the target bit). Single bit-flip locations in internal components (e.g., registers and memory address) as well as injection times are defined randomly. In phase 3, FI is performed. The FIM starts by reading the fault list and then schedules an event targeting insertion time. After writing the new value in the target register, the simulation restarts. During phase 4, error detection is performed by comparing each application running under FI with the golden standard run.

At this level, different error classifications can be implemented, for example, the five-group error classification proposed by Cho [160] and discussed in [155]: 1) vanished, no-fault traces are left; 2) application output not affected (ONA), the resulting memory is not modified; however, one or more remaining bits of the architectural state are incorrect; 3) application output mismatch (OMM), the application terminates without any error indication (however, the resulting memory is affected); 4) unexpected termination (UT), the application terminates abnormally with an error indication; and 5) hang, the application does not finish, and it is preempted using a timeout. Lastly, phase 5 assembles all FIM individual reports to create the final database, final report, and graphics. An example of compilation results comparing different SFI solutions is shown in Fig. 33 [156].

Among all the errors induced by FI, SEFIs at the system level (SoC) are undoubtedly the most difficult to characterize and to model because: 1) these errors can have multiple causes and 2) during SEFIs, the system can behave unpredictably [157]. Usually, SEFIs appear as a spontaneous system reset, a program execution stop (hang-up) or an upset in program execution that can be only repaired by external reset [158]. It is known that SEFIs are caused by upsets in program or data memory (critical bits) or transients and interference on internal lines or peripheral circuitry [158]. Recent studies have also shown that increasing complexity and

size of program code, as well as real-time operating system usage, leads to a higher probability of SEFIs that directly affects the reliability of a modern SoCs [159].

## VIII. CONCLUSION

SEEs designate and include a sequence of events that extends from particle–matter interactions at the atomic scale to functional errors at circuit or system levels. As a complex domino effect, they cover approximately 15 orders of magnitude on the distance scale and 20 orders of magnitude on the timescale, which is considerable and necessarily involves several branches of fundamental and applied physics for their description and understanding. In this article, we have addressed different ways of modeling and simulating this complex chain of mechanisms, discussing the specific multiscale, multiphysics, and multidomain nature of SEEs as well as the main underlying physical mechanisms that lead to the occurrence of such effects in device, circuit, and systems. However, this article has not covered the vast and exhaustive domain of all types of SEEs but was limited to the modeling and simulation of SETs and SEUs induced by single events in digital electronics.

An important feature of SEEs is that they can be studied at different levels, starting from different “precursors”: the interaction of a particle with the atoms of a material for the most microscopic description, the creation of electron–hole pairs at the device level, the injection of a current pulse at the circuit level, and finally, the injection of faults at the system level. These different description levels correspond to diverse specialized branches in the radiation effect community historically developing different modeling approaches, using specific simulation tools, and even using different technical terms to designate the same effect (an SBU at memory cell level becomes, for example, a logical fault at system level).

In this article, we distinguished five different types of methodologies of modeling and simulation of SEEs as a function of the “simulation level” envisaged to perform a given study. These simulation levels schematically extend from atoms to materials, materials to devices, devices to cells, cells to circuits, and circuits to systems. For each level, we reviewed and emphasized the specific features of the modeling and simulation methodologies, and we discussed simulation requirements, codes, model inputs, and expected outputs.

To go further and with the uninterrupted miniaturization of silicon microelectronics that has fueled the exponential growth of ICs for over half a century, some important challenges remain in the domain of modeling and simulation of SEEs in future nanodevices and related circuits. These challenges will concern the adaptation of the whole panoply of existing methods to new materials, specific architectures, and new domains, including photonic devices, spintronic circuits, and quantum computing-related circuits and systems, just to cite the most important.

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