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# SINGLE EVENT UPSET CROSS SECTIONS AT VARIOUS DATA RATES

R.A. Reed<sup>1</sup>, M.A. Carts<sup>1,2</sup>, P.W. Marshall<sup>1,2</sup>, C.J. Marshall<sup>1</sup>, S. Buchner<sup>1,2</sup>, M. La Macchia<sup>3</sup>, B. Mathes<sup>3</sup> and D. McMorrow<sup>1</sup>

- 1. Naval Research Laboratory, Washington, DC
- 2. SFA, Inc., Largo, MD
- 3. Motorola GSTG, Scottsdale, AZ

### **ABSTRACT**

We present data which show that Single Event Upset (SEU) cross section varies linearly with frequency for most devices tested. We show that the SEU cross section can increase dramatically away from a linear relationship when the test setup is not optimized, or when testing near the maximum operating frequency. We also observe non-linear behavior in some complex circuit topologies. Knowledge of the relationship between SEU cross section and frequency is important for estimates of on-orbit SEU rates.

#### I. INTRODUCTION

Spacecraft designs that require microelectronic circuits to be low power and weight while operating at high data rates have prompted researchers to look for new technologies, or enhanced versions of current technology, that exhibit these characteristics. A recent study [1] in this area utilizes clocked Emitter Coupled Logic (ECL) devices. Three other studies consider GaAs based technologies. The devices in one of these studies are Complementary Heterostructure Insulated Gate Field Effect Transistor (C-HIGFET) and Source Coupled FET Logic (SCFL) [2]. The remaining two papers investigate a GaAs majority vote and self-scrubbing circuitry [3,4]. Silicon based A/Ds were studied in references [5] and [6]. The SEU data collected on all of these devices and circuits show data rate dependent cross section.

We present here new heavy ion data collected on four National Semiconductor ECL based devices (one of which is clocked) and two Motorola clocked n-channel GaAs devices. We find that there is a linear relationship between data rate and SEU cross section for most cases tested. Clocked devices tested show both linear and nonlinear relationships.

We find that one of the key test issues to consider in this type of measurement is the delay between the edge of the clock signal and the data edge, or the clock/data phase delay. In previous work [2,7] we centered the clock within the bit period in order to obtain valid data. In this work we demonstrate the importance of doing this by investigating the impact on the SEU cross section while the Device Under Test (DUT) clock/data phase delay is allowed to go uncorrected as frequency is swept. We find that the relationship between data rate and SEU cross section is linear except where the system is operating at data rates near a dropout frequency

(described later), at which point the SEU cross section increases rapidly. A sharp increase in SEU cross section is also seen when the system is operated near its maximum data rate. This is a general result for the devices tested, and one with ramifications for the hardness design process. We will show that the high SEU cross section when the system is operating near a dropout frequency can be lowered to expected values by optimizing the system setup, but that the maximum operating frequency non-linearity is unavoidable.

#### II. EXPERIMENTAL SETUP

The National Semiconductor devices used in this study are the 100325 (ECL to TTL translator), 100324 (TTL to ECL translator), 100331 (D flip flop) and 100307 (XOR). The D flip flop is the only National Semiconductor device that requires a clock. Two proprietary Motorola clocked devices were also tested. Various heavy ion SEU measurements were performed on a single device of each part type. The range of fluences used to characterize the SEU cross section is  $7.0 \times 10^5$  to  $1.0 \times 10^7$  particles / cm<sup>2</sup>.

The low energy heavy ion data was collected at the SEU Test Facility located at Brookhaven National Laboratory (BNL). Bromine exposures were carried out on the ECL devices. The Motorola devices were irradiated with nickel and fluorine. Table 1 lists the ions that were used, and their corresponding energies and LETs

The high energy experiments were carried out at the Tandem Accelerator Superconducting Cyclotron (TASCC) facility at the Chalk River Laboratories of AECL Research, Canada. The high energy of the ion beams allowed the experiments to be performed in air in front of a thin mylar window that sealed the accelerator beam line. All LETs for

Table 1. Ions used along with the energies (MeV) and LETs (MeV  $\,\mathrm{cm}^2$  /  $\,\mathrm{mg}$ ) of each.

	BNL								]
	ION Energy LET		Br 285 37		Ni 265 19		7. 4.	F	1,14
							140		1
							2	2.5	
			į	TAS	CC	1.19			
ION		Au		1		Br		Br	
Energy		1206		1500		391		969	
LET		92		-50		37		26	

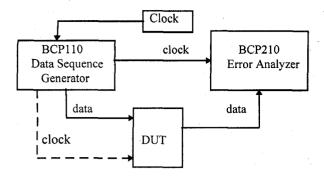


Figure 1. Block diagram of ECL test setup.

each ion were corrected for the air gap between the window and the DUT. Table 1 gives the relevant ion LETs at the DUT.

The pulsed laser measurements were carried out at the Naval Research Laboratory pulsed laser facility [8]. They were performed using the output of a synchronously pumped, cavity-dumped dye laser centered at 610 nm with a nominal pulse width of 2 ps, a repetition rate of 1 kHz and a spot size of approximately 1.1  $\mu m$ . This corresponds to a 1/e penetration depth of  $\sim$  3  $\mu m$  in silicon, and 0.2  $\mu m$  in GaAs. The spot position and focus were optimized with a 0.1  $\mu m$  resolution motorized xyz stage, and the laser pulse energy incident on the DUT was monitored continuously during each run with a calibrated, large-area photodiode.

Figure 1 shows a block diagram of the ECL test setup (the Motorola devices were characterized using a similar setup but using a different BERT). The Broadband Communications Products Bit Error Rate Tester (BERT) data sequence generator passes a 2<sup>7</sup>-1 Pseudo-Random Number bit sequence (PRN) to the DUT, and from there to the analyzer. The generator also supplies the clock signal to the DUT if the DUT is a clocked device (D flip flop) and to the analyzer. The analyzer uses a self-synchronizing PRN error detection scheme. The leading edge of the clock signal passed to the analyzer determines when the data is sampled within each bit period. The sample time for the analyzer is fixed at approximately 340 ps. If the data is incorrect during the sample time it will be counted as an error.

A radiation-induced voltage transient occurring in an unclocked device will be detected as an error (and thus labeled as an SEU) if the transient overlaps the sampling window and the voltage is at a sufficiently high level. By way of illustration, Figure 2 shows a 01010 bit stream with one radiation event occurring in bit period 3 and another in bit period 4. Bit periods 1, 2, 4 and 5 are error free. The analyzer will detect a bit error during bit period 3 since the voltage transient coincides with the sampling window. The transient during bit period 4 goes unnoticed by the sampling circuit in the error analyzer and thus is not counted as an SEU. In previous studies [2,7], we have assured centering of the sampling interval within the bit period, and in this study we show the importance of doing this.

Clocked devices, and especially those with multiple stages, will usually have SEUs which appear as completely

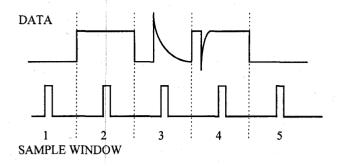


Figure 2. Data bit stream with ion induced transients shown with the sampling windows of the error analyzer.

flipped bits. Occasionally transients in the output circuitry are detected as SEUs just as for unclocked devices.

# III. VARIATION OF CROSS SECTION WITH EXPERIMENTAL OPTIMIZATION

In this section we discuss test setup issues that must be addressed in order to obtain meaningful data. The TTL to ECL translator (100324) and the ECL to TTL translator (100325) experimental setup was found to be inoperable in a radiation-free environment when the data rate was 110 MHz, 215 MHz, 330 MHz and all frequencies above 440 MHz (the maximum operating frequency of the device). This is because different data and clock path lengths result in different phase delays at different frequencies. This requires that the phase delay be optimized for each frequency.

Figure 3 shows one bit period with rise and fall times. Optimization of the phase delay will place the sample window at position 2. If the sample window is sufficiently narrow, such that it can sample the level of the bit without sampling the pre-or post-bit transition, then the analyzer will not detect an error. If the sampling window is positioned at location 1 or 3 (unoptimized) the analyzer will detect an error for each bit. The series of inoperable frequencies is due to the clock and data timing changing as the frequencies is changed. At certain frequencies, the data is clocked and sampled during its transition (position 1 or 3). The frequencies at which the clock/data phasing causes the data to be sampled during a transition are called dropout frequencies.

The maximum operating frequency is reached when the valid data time in the bit period is less than the sample window. If the sample window covers the entire bit (from

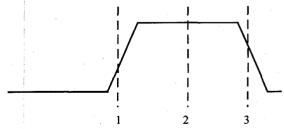


Figure 3. A single bit period showing the slope of the rise and fall time. The dash line indicates the location of the sampling window.

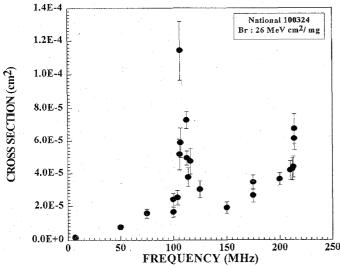


Figure 4. Upset cross section dependence on data rate for the TTL to ECL translator when exposed to 0.97 GeV Bromine. The peak at 110 MHz is due to unoptimized testing near a dropout frequency.

position 1 to position 3) each bit may be detected as an error. It is coincidence that the maximum operating frequency is located near one of dropout frequencies for this device. The discussion that follows is focused on the data collected near dropout frequencies.

Figure 4 shows the 100324 translator SEU cross section as a function of data rate when exposed to 0.967 GeV Bromine at TASCC. There is a sharp increase in the SEU cross section near the dropout frequencies of 110 and 215 MHz. Higher frequency data were not taken for this ion but the behavior is very similar at 330 MHz. These peaks can be entirely eliminated with proper phasing of the data and clock signals at all but the maximum operating frequency, 440 MHz. The failure mode at the maximum operating frequency can be due to a test setup limitation or a device limitation.

The sharp increases in the cross section near dropout frequencies in Figure 4 were thought to be due to an increase in sensitivity near data transitions. This idea was tested by inserting a continuously variable delay line in the clock path between the data generator and the error analyzer which allowed the time of sampling to be shifted within the data bit period. In Figure 5 the SEU cross section is plotted as a function of the position of the sampling window for bromine exposures of the 100324 translators at BNL while operating at 50 MHz. With no incident particles no errors were seen at the test frequency for all delay times. A sharp increase of nearly an order of magnitude is seen in the SEU cross section as the sampling window is moved closer to the transition, located at an abscissa value of zero in this plot.

As is suggested in [2] we deduce that this sensitivity is due to loss of noise margin close to the data transition. The width in time of the rise in the SEU cross section in Figure 5 is a function of both the width of the sampling window of the analyzer and the rise/fall-time of the DUT.

The unavoidable nonlinear rise in SEU cross section near the maximum operating frequency is not an indication of a

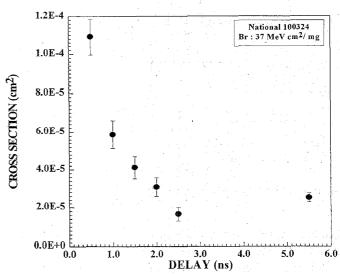


Figure 5. The cross section versus the delay between the sample window and the data edge. This shows a greater device sensitivity when sampling near the data transitions.

different mechanism than seen at the lower dropout frequencies. Rather, the maximum operating frequency rise is unavoidable because it is not possible to position the sampling window away from data transitions, i.e., the sample window extends from position 1 to position 3 in Figure 3.

#### IV. RESULTS AND DISCUSSION

A. SEU Cross Section Dependence on Frequency and LET

Figure 6 shows the results from exposures of the 100324 translator at TASCC. The cross section as a function of data rate is plotted for four ion LETs. The lines are the best linear fit to the data. The bromine data is the same as in Figure 4 with the data collected near dropout frequencies omitted. The results of the test performed on the 100325 translator were similar to these.

The translators do not use a clock signal. The lack of any clock signal within the DUT, and the fact that the cross section depends on the data rate, leads to the conclusion that the circuit has a temporal sensitivity associated with the bit period. An ionizing event must occur within a fixed temporal period to upset the device. The sensitive time interval, or vulnerable window, is a function of the sampling time, the time period for dissipation of the charge (which depends on the particle LET and the characteristics of the semiconductor material [2,4]) and the internal circuit bandwidth [7].

The linear relationship between the cross section and the data rate can be attributed to the fact that as the data rate is increased there is an increased number of opportunities for an error to occur for a given fluence [2,10]. Given that the LET of the ion is large enough that the cross section is near saturation, the linear relationship can be derived by examining the number (N) of upsets that will be expected to occur during

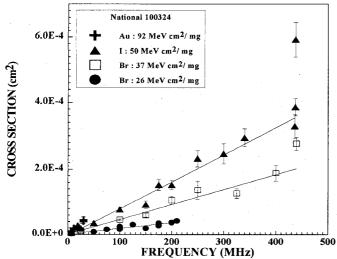


Figure 6. Cross section as a function of frequency for the exposures carried out at TASCC on the TTL to ECL device.

an exposure of a device with a sensitive area (A) where the fluence is given by  $(\Phi)$  with a vulnerable time window  $(t_w)$ operating with a bit period (T). This gives:

$$N = \Phi A \frac{t_w}{T}.$$
 (1)  
 
$$\sigma = N / \Phi$$
 (2)

$$\sigma = N / \Phi \tag{2}$$

Given that 1/T is frequency (v), solving for the cross section (σ) gives:

$$\sigma(LET) = A(LET) t_w(LET) v.$$
 (3)

This is a general result. The sensitive area and the time window are functions of the LET of the particle. The slopes of the best fit lines in Figure 3 increase for increasing LET. (The gold data was only collected for low frequencies.) A static measurement of SEU cross section as a function of LET will show how the sensitive area varies with LET. From this and from the slopes of the best fit line for the relationship between the cross section and the frequency one can determine the vulnerable time interval as a function of LET for a device. Equations 1 and 3 are applicable if the frequency dependence is linear. This is not always true, which will be shown later.

The Bit Error Ratio (BER) is the ratio of the number of errors (N) to the number of bits transmitted (v t), where t is the operation time. Substituting the right side of equation 1 for the number of errors gives:

$$BER = \Phi A t_w / t$$
 (4)

This shows that the BER is independent of frequency for devices that exhibit a linear increase in the number of upsets as the frequency is increased. Reference [4] gives an equation to determine the cross section per transmitted bit:

$$\sigma_{BER} = N / (v t \Phi)$$
 (5)

From the definition of the BER this equation becomes:

$$\sigma_{\rm BER} = {\rm BER} / \Phi \tag{6}$$

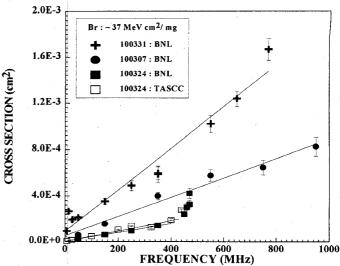


Figure 7. Cross section versus frequency for ECL exposures carried out at BNL. The 100331 is a clock device while the others are not.

Inserting the right side of equation 4 into this gives:

$$\sigma_{\rm BER} = A t_{\rm w} / t \tag{7}$$

This shows that for devices that exhibit a linear increase in the number of errors with frequency the cross section per transmitted bit given in equation 5 will not change with frequency. Using equation 5 to compute the experimental cross section could lead to erroneous conclusions about the frequency dependence of the SEU cross section. Reference [6] uses ground data to predict on-orbit upset rates at frequencies other than ground test frequencies based on the cross section given in equation 4. This is valid as long as the error cross section (errors divided by the fluence) increases linearly with frequency. This is not always true, as will be shown later. On-orbit estimates of upset rates should be made from data collected when devices are operating at on-orbit frequency.

In Reference. [2] it is stated that at the maximum operating frequency, the SEU cross section might be expected to increase dramatically. The iodine data in Figure 6 shows the increase in the cross sections at maximum frequency, for the reasons detailed in section III.

## B. Comparison of the Results for Several Clocked and Unclocked Devices

Figure 7 shows SEU cross section versus data rate for the D flip-flop (100331), XOR (100307) and ECL to TTL translator (100324) for bromine exposures measured at BNL. The results from the bromine TASCC data are plotted for comparison. The XOR and D flip-flop (a clocked device) data is linear over this frequency range.

The 100324 translator data in Figure 7 shows a linear relationship until the maximum operating frequency is approached. Again, as is suggested in [2] operation near the maximum frequency results in the unavoidable loss in noise margin and thus increased sensitivity to SEU. A ramification

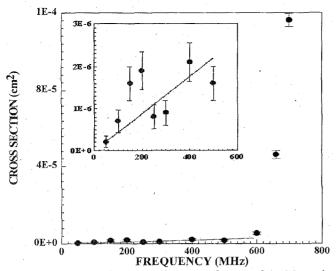


Figure 8. Cross section versus frequency for one of the Motorola devices. The inset is a blowup of the lower data.

of this for system designers is that additional bandwidth must be designed into the system in order to avoid excessive SEU cross section at the high application data rates.

The results from the Motorola devices are shown in Figures 8 and 9. Notice the dramatic increase in the SEU cross section observed for both devices near the maximum operating frequency in each figure. In contrast to the ECL case, the high frequency nonlinearity is not due to loss of noise margin within the DUTs but rather within the test equipment itself. Later tests with a higher bandwidth test set revealed that this nonlinearity occurred at a higher frequency.

Figures 8 and 9 also illustrate that the cross section versus frequency behavior is not always linear. The inset of each figure shows the low frequency data. The inset of Figure 8 shows a general trend towards increasing SEU cross section with increasing frequency, but there is a large scattering of the data about the linear relationship. The inset in Figure 9 shows an decrease in SEU cross section with increasing frequency up to 500 MHz, at which point the cross section begins to increase. Although the results are repeatable, we do not fully understand the cause. Laser testing of the various nodes within the Motorola devices is being conducted. These tests will help to understand the cause of the nonlinearity, a similar test method was utilized in references [3,4] for a complicated majority vote and self-scrubbing circuit.

Clocked devices have both data path circuitry and clock distribution circuitry. Each path can be sensitive to radiation induced effects, possibly one more than the other. Also, these devices have internal and external nodes that can have various sensitivities [9]. Potentially each of these characteristics of a clocked device can lead to a deviation from linearity in the SEU cross section. However, not all clocked devices will deviate from a linear relationship, as demonstrated by the D flip flop of Figure 6. Laser testing of the nodes in the data and clock path can help to resolve some of these issues. However, this can be very complicated task. It is our experience that it can be quite difficult to determine the underlying causes of a

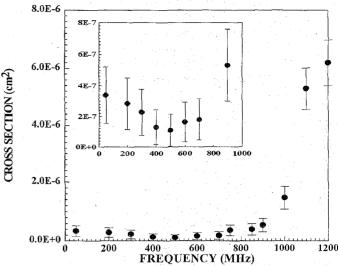


Figure 9. Same as Figure 8 for another Motorola device showing nonlinear data.

circuit level dynamic SEU response even when the SEE response of simple test structures is investigated.

#### C. Laser Evaluation of the SEU versus Data Rate

Laser test carried out on the ECL XOR demonstrates the utility of the laser for evaluation of the SEU data rate dependence, and for investigating the time window during which a device is vulnerable to SEUs [4]. The measurements were conducted by focusing the laser on one device node and operating it asynchronously with the test system. The number of upsets normalized to the exposure time as a function of the frequency determines the frequency dependence of the node tested. Figure 10 shows the results for one node of the 100307 XOR. As expected, based on the ion test results, a linear relationship is observed. Further analysis has been hampered by lack of device fabrication information for the ECL devices.

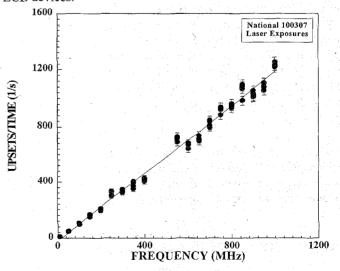


Figure 10. Time normalized upsets as a function of frequency for one node of an XOR gate exposed to laser.

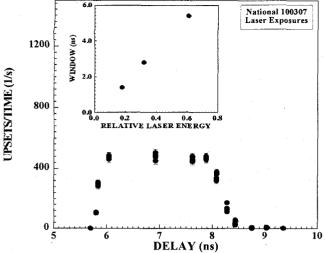


Figure 11. Upsets versus laser pulse time of arrival. Inset shows vulnerable time window for the three laser energies.

The error analyzer registered more errors than it could count for frequencies between 425 and 500 MHz. Heavy ion measurements show the same effect for both the XOR and the D flip flop. This is clearly a test set optimization problem. However, it was not resolved by changing the time delay between clock and data.

The period of time that a device is vulnerable to a transient strike, t<sub>w</sub>, was explored by synchronizing the clocks used by the laser and the test system [4]. The clock/data phasing is optimized, and the time of arrival of the laser pulse within the bit period is swept through the vulnerable time window by adjusting a variable delay between the system clock and the data generator. Figure 11 shows the results at a particular laser energy illustrating a sensitive window of ~2.5 ns. (This data was obtained at the relative energy of 0.32 shown in the inset.) This time window measurement was repeated for three different laser pulse energies and the widths of the vulnerable time windows are recorded in the inset. The vulnerable time window is a function of both the sampling window of the analyzer and the laser pulse energy (or the LET for an incident ion). The width of the vulnerable time window for SEU increases with increasing laser energy, similar to that in reference [4]. For the case of incident heavy ions, the vulnerable window will be expected to increase with increasing LET.

#### V. CONCLUSIONS

The SEU cross section dependence on data rate is shown to be linear for all devices investigated that do not require a clock, and for some devices that are clocked. The linearity is attributed to the fact that the number of vulnerable periods during a fixed fluence increases linearly with data rate. Some clocked devices show a nonlinear relationship between the cross section and the data rate.

Optimization of the experimental setup is an important issue for the execution of successful dynamic SEE

measurements. The SEU error cross section is seen to increase dramatically when the bit stream is sampled close to the transitions. The increased sensitivity to SEU is attributed primarily to reduced noise margin during data transitions.

A similar but unavoidable increase in the SEU cross section is seen near the maximum operating frequency where the system noise margin is reduced, whether by the device or the test setup. This highlights the importance of system designs which accommodate excess bandwidth beyond the application requirements in order to minimize orbital upset rates.

This work and references [1-7,9,10] show that the cross section can vary dramatically with data rate. Such information is crucial for making accurate on-orbit SEE rate predictions. Future work needs to concentrate on a better understanding of circuit level non-linear SEU response.

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