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Design and Performance Comparison of Radiation-Tolerant and Conventional 8:1 Multiplexers in 90nm Technology

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***Abstract*—This study presents the design and performance trade-offs between the radiation-tolerant and conventional 8:1 multiplexers using 90 nm semiconductor technology in cadence virtuoso, focusing on their performance metrics and radiation resilience characteristics. Radiation tolerance is a crucial factor for electronic systems deployed in radiation-intensive environments. The motivation of this study is generated from the need of creating reliable electronic systems in radiation-rich environments. The methodology involves the design and simulation of both conventional and radiation-hardened multiplexers, followed by a detailed analysis of their performance under simulated radiation conditions. The analysis evaluates key design parameters including propagation delay, power consumption, area utilization, layout design and transistors. Results indicate that radiation-tolerant multiplexers demonstrate enhanced resilience against SEE, albeit with slightly higher power consumption and area overhead than conventional designs optimized for speed and efficiency. The study concludes that the choice between these multiplexer types should be guided by specific application needs, balancing the trade-off between performance efficiency and robustness in radiation-sensitive environments.**

Keywords—radiation-tolerant, transient response, 8:1 multiplexer, semiconductor technology, radiation resilience, propagation delay, power consumption, area utilization, space applications.

I. INTRODUCTION

In the realm of modern electronic systems, reliability in harsh radiation environments such as outer space remains a paramount concern. Electronic components deployed in these settings are exposed to ionizing radiation, which can induce errors and degrade performance over time [1]. To mitigate these effects, specialized design techniques are employed to enhance radiation resilience.

Multiplexers, fundamental to digital circuitry, serve as critical components in data processing and control systems [2]. The choice between conventional and radiation-tolerant multiplexer designs becomes crucial when considering applications requiring high reliability in the face of radiation-induced single-event effects (SEE) [3].

This paper explores the comparative design and performance evaluation of radiation-tolerant and conventional 8:1 multiplexers implemented using advanced 90 nm semiconductor technology. The study focuses on assessing key metrics such as propagation delay, power consumption, and area utilization, while also scrutinizing the ability of each design type to withstand radiation-induced errors [4].

The motivation for this study generates from identified gaps in recent literature, where existing multiplexer designs have either prioritized performance metrics like speed and power efficiency or focused on radiation resilience, but not both. Despite advancements, a comprehensive analysis that directly compares these two critical design approaches under similar conditions is lacking. By focusing on key metrics such as propagation delay, power consumption, and area utilization, while rigorously assessing the ability of each design type to withstand radiation-induced errors, this study aims to fill this gap [5]. The gates used in this 8:1 MUX maintain a stable voltage of (1.5-1.78V) across different particles such as proton, carbon ions etc. Moreover, it also has faster recovery time as low as 18 picoseconds for the gates which makes the MUX more radiation resilience and reduce the risk of failure from radiation-induced transient currents [6].

By systematically analyzing these parameters through simulation and characterization using industry-standard tools, this study aims to provide a comprehensive understanding of the trade-offs between radiation resilience and operational efficiency in multiplexer design [7]. Insights gained from this comparative analysis are expected to inform future advancements in the development of robust electronic systems tailored for space and other radiation-prone applications.

II. METHODOLOGY

The methodology initiates with the design of a conventional 8:1 multiplexer (MUX). This baseline design is then enhanced to develop a radiation-hardened version of the 8:1 MUX, ensuring robustness against radiation effects. Subsequently, a transient response analysis is conducted to evaluate the dynamic performance of the hardened design. Following this, a detailed propagation delay analysis is performed to measure the timing characteristics and signal transmission delays within the MUX. The analysis proceeds with an average power consumption assessment to determine the energy efficiency of the design under typical operating

conditions. The complexity of the design is then quantified by calculating the number of transistors required. The process advances to the layout design phase, where the physical implementation is planned, and area utilization is analyzed to ensure efficient space usage. The methodology culminates with the finalization and comprehensive documentation of the design and analytical outcomes.

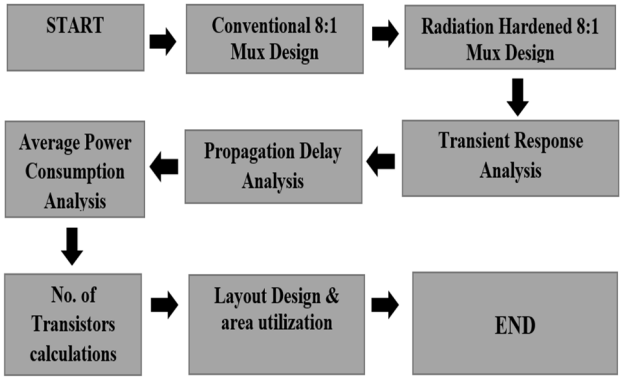

Fig. 1. Work flow diagram

III. Design Specifications

A. Conventional 8:1 MUX:

The design of an 8:1 conventional multiplexer involves several key components. Eight four-input AND gates are utilized for the primary logic operations. To complement these, three inverters are attached to the selection line S1, S2 & S3. Additionally, an eight-input OR gate is employed to consolidate the outputs of the AND gates into a single output line. The circuit is interconnected with appropriate wiring and is powered by a voltage source, with a ground connection to complete the electrical circuit.

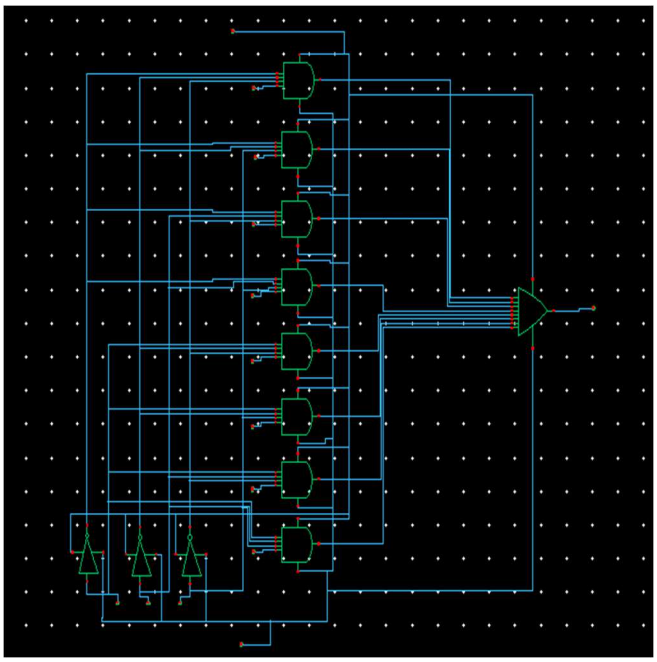

Fig. 2. Conventional 8:1 MUX

From this circuit the symbol of 8:1 MUX is-

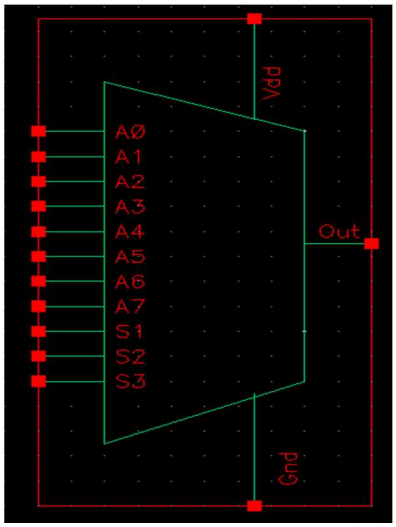

Fig. 3. Conventional 8:1 MUX symbol

B. Radiation Hardened 8:1 MUX:

The design of an 8:1 radiation-tolerant multiplexer involves several key components. Eight four-input radiation-hardened AND gates are utilized for the primary logic operations. To complement these, three radiation-hardened inverters are included for the selection lines S1, S2, and S3. Additionally, an eight-input radiation-hardened OR gate is employed to combine the outputs of the AND gates into a single output line. The circuit is interconnected with appropriate wiring and is powered by a voltage source, with a ground connection to complete the electrical circuit.

1) Four-input radiation-hardened AND gates:

An SEU immune logic gate requires 2n + 2 transistors due to added redundancy for upset mitigation, ensuring stable output under radiation [8]. In a 4-input AND gate, this entails using 14 transistors in which 10 transistors are used to constitute NAND gate and 4 transistors are used to constitute NOT gate. The stronger transistors M1, M2, M3, and M4 pull "out" low when all inputs (A1, A2, A3, and A4) are high, while weaker transistors M5, M6, M7, and M8 pull "out" high otherwise. This design ensures correct output states by preventing "out" from switching incorrectly due to upsets: M1, M2, M3, and M4 maintain "out" at 0 when all inputs are high, and M5, M6, M7, and M8 maintain 1 when any input is low. By this way, it builds the SEU immunity.

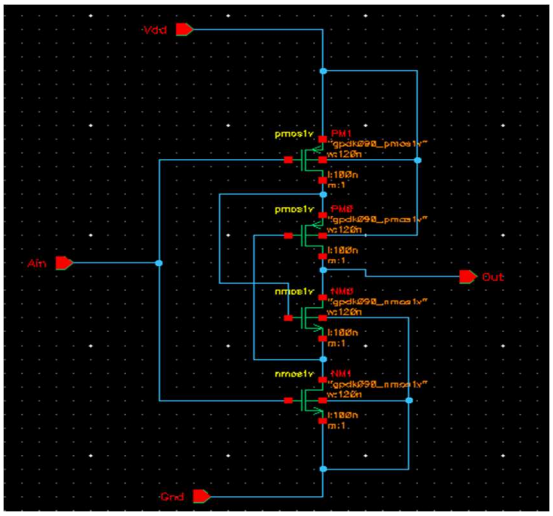

Fig. 4. Four-input radiation-hardened AND gates

2) SEU immune Inverter:

An SEU immune 1-input inverter requires 4 transistors due to redundancy: stronger transistors M1 and M2 pull the output low when the input is high, while weaker transistors M3 and M4 pull the output high when the input is low, ensuring stable operation under radiation [9].

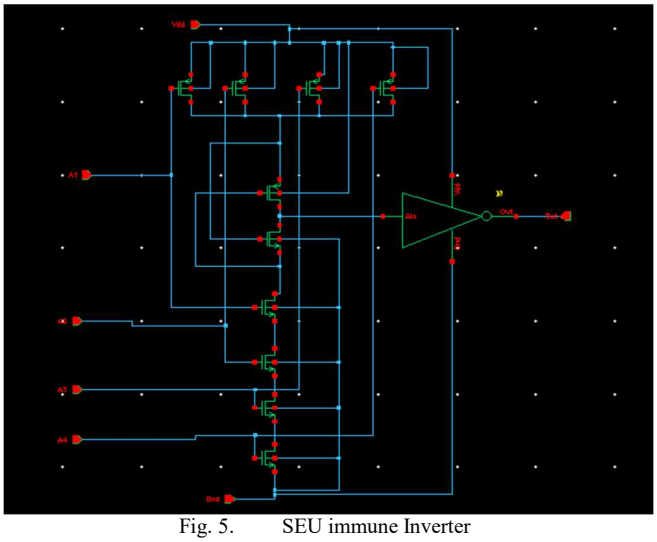

Fig. 5. SEU immune Inverter

3) Eight-input radiation-hardened OR gate:

An SEU immune 8-input OR gate requires 22 transistors: stronger transistors M1 to M8 pull the output high when any input (A1 to A8) is high, while weaker transistors M9 to M16 pull the output low otherwise. This design ensures correct output states by maintaining 1 when any input is high (M1 to M8 active), and at 0 when all inputs are low (M9 to M16 active), thereby providing resilience against upsets by ensuring stable operation under radiation [10].

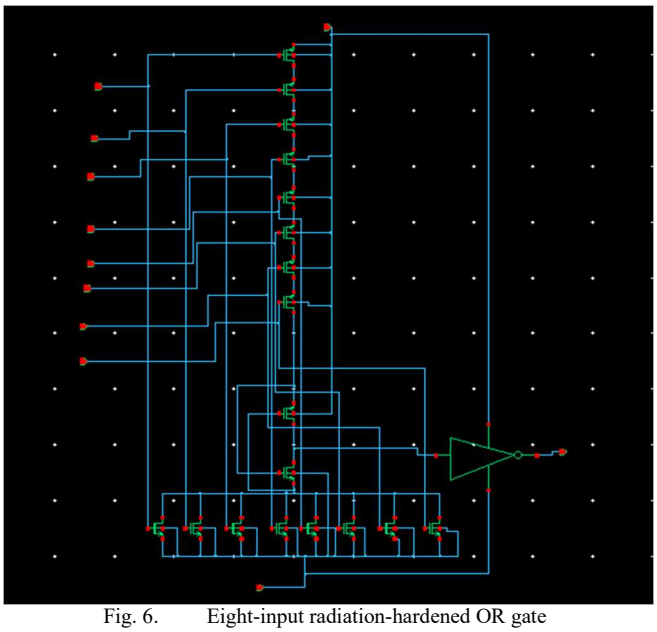

Fig. 6. Eight-input radiation-hardened OR gate

From the above radiation hardened AND, NOT & OR gates we develop radiation hardened 8:1 MUX.

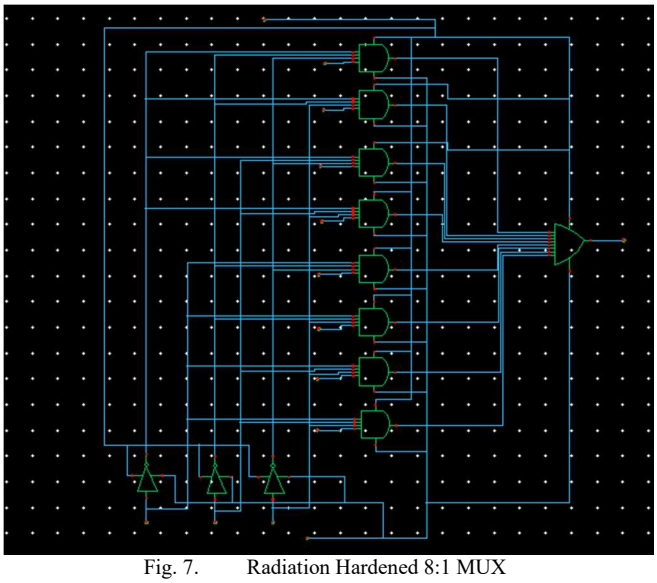

Fig. 7. Radiation Hardened 8:1 MUX

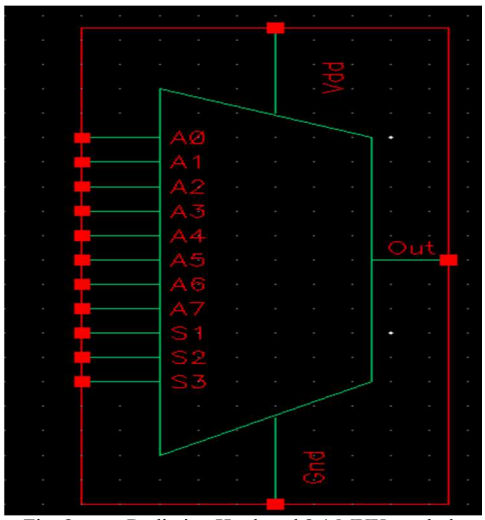

Fig. 8. Radiation Hardened 8:1 MUX symbol

IV. TRANSIENT RESPONSE ANALYSIS

A. Operating Principle

An 8:1 multiplexer selects one of eight input lines based on three control inputs (S3, S2, S1), routing the selected input to the output. It operates by using logic gates to enable the chosen input data to pass through to the output based on the binary combination of the control inputs [5].

TABLE I. Truth Table of 8:1 MUX

Input			Output
S1	***S2***	***S3***	***Out***
0	0	0	A0
0	0	1	A1
0	1	0	A2
0	1	1	A3
1	0	0	A4
1	0	1	A5
1	1	0	A6
1	1	1	A7

B. *Conventional 8:1 MUX:*

In transient analysis of a conventional 8:1 multiplexer (MUX), specific input-output relationships are observed based on selection line inputs: when the selection is 101, the output corresponds to input A5; for 001, it corresponds to A1; for 111, it corresponds to A7; and for 010, it corresponds to A2. Similarly, 100 corresponds to A4, while the remaining selection inputs dictate the output following their respective inputs. This analysis demonstrates how the MUX efficiently routes data from multiple inputs to a single output based on the binary state of its selection lines, facilitating dynamic data selection in digital circuits.

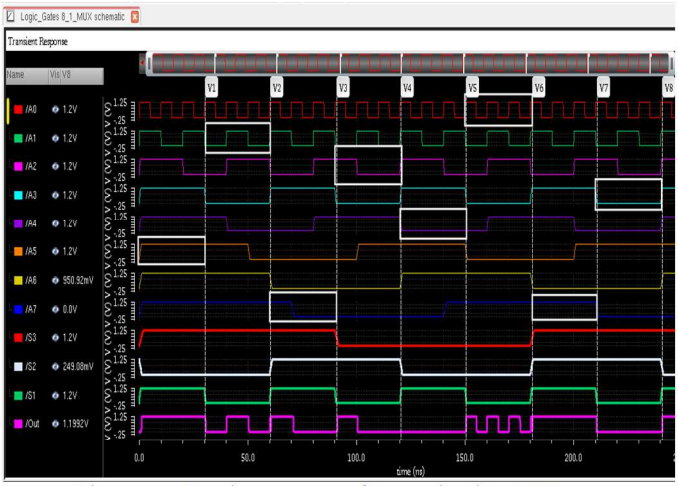

Fig. 9. Transient response of conventional 8:1 MUX

C. *Radiation Hardened 8:1 MUX:*

In transient analysis of a radiation-hardened 8:1 multiplexer (MUX), similar to a conventional MUX, specific input-output mappings are observed: when the selection is 111, the output corresponds to input A7; for 011, it corresponds to A3; for 101, it corresponds to A5; and for 000, it corresponds to A1. This pattern continues for other selection inputs, demonstrating the MUX's capability to reliably route data under harsh radiation conditions, ensuring consistent functionality despite potential environmental disturbances.

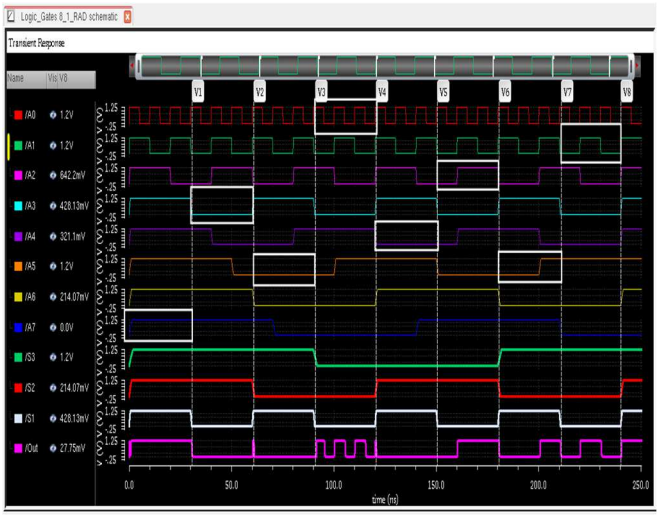

Fig. 10. Transient response of Radiation Hardened 8:1 MUX

V. PROPAGATION DELAY ANALYSIS

The propagation delay difference between a conventional 8:1 multiplexer and a radiation-hardened version is due to design optimizations for speed versus resilience. Conventional MUX's prioritize faster switching with smaller, faster transistors and minimal protective circuitry, achieving a propagation delay of 154.6 picoseconds. In contrast, radiation-hardened MUX's use larger, slower transistors and additional protective measures against radiation effects, resulting in a longer propagation delay of 963.9 picoseconds to ensure reliability in harsh environments. This trade-off reflects differing design priorities: speed in conventional MUX's versus robustness in radiation-hardened versions. In the recent published works, the propagation delay of the conventional MUX is 192.53 picoseconds[11] and for the radiation hardened MUX is 1200 picoseconds [12]. In our study we got better result than the other recent studies.

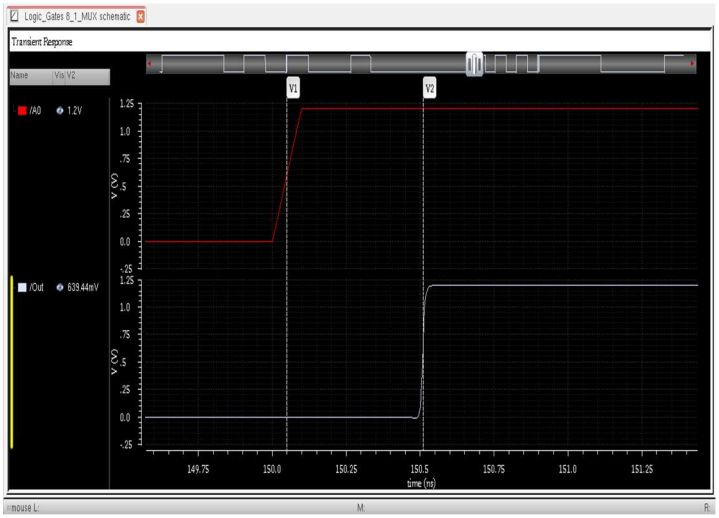

Fig. 11. Propagation delay of Radiation Hardened 8:1 MUX

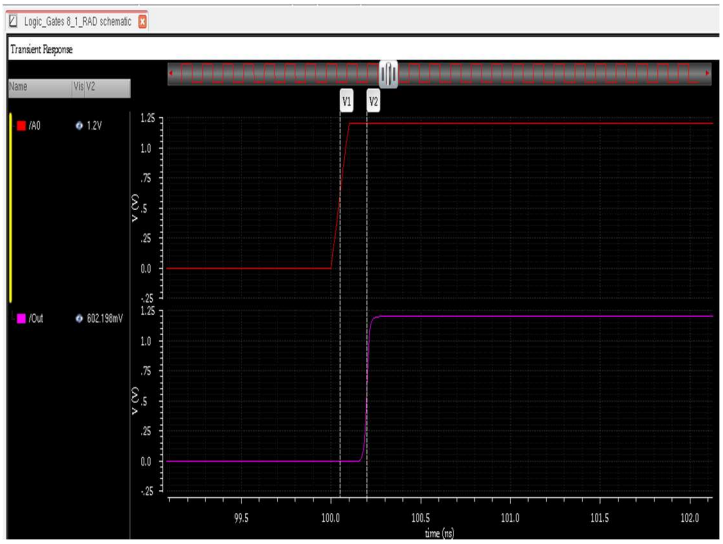

Fig. 12. Propagation delay of conventional 8:1 MUX

VI. Average Power Consumption Analysis

The higher average power consumption of the radiation-hardened 8:1 multiplexer (2.605E-6 watts) compared to the conventional counterpart (1.835E-6 watts) is primarily due to enhanced design features aimed at radiation tolerance. In the recent published data the power consumption of conventional 8:1 multiplexer is 15.11×10^{-8} [13]. But in our case the power consumption is way more less than the actual power consumption due to the proper use of minimum number of transitors. Radiation-hardened circuits typically incorporate additional redundancy, error correction mechanisms, and thicker oxide layers on transistors to withstand ionizing radiation. These design choices increase circuit complexity and introduce higher parasitic capacitances, leading to greater power dissipation. Additionally, operational reliability in harsh radiation environments often requires higher voltage levels or increased current flow, further contributing to elevated power consumption levels in radiation-hardened designs compared to conventional ones [14].

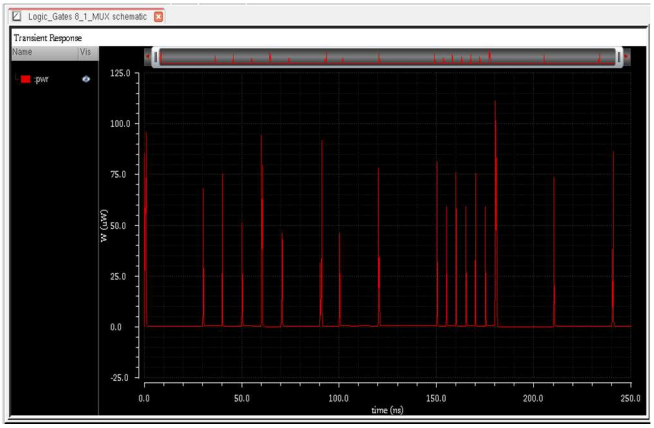

Fig. 13. Average power consumption of conventional 8:1 MUX

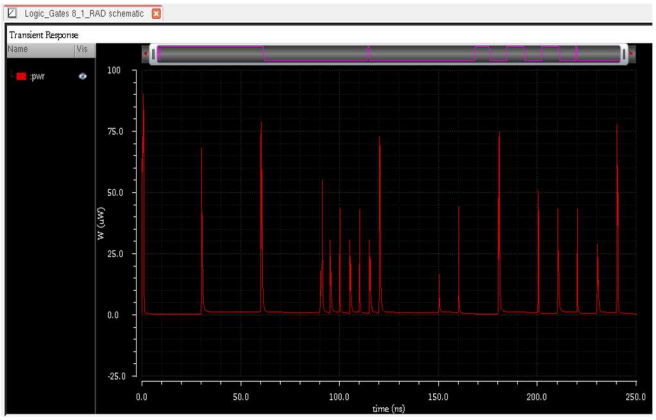

Fig. 14. Average Power Consumption Radiation Hardened 8:1 MUX

VII. No. Of Transistors Analysis

In general, an SEU immune logic gate, implemented with this technique, requires 2n + 2 transistors, n being the number of gate inputs. In comparison, classical CMOS requires 2n transistors to implement a gate.

A. For the conventional 8:1 MUX:

10 transistors needed for 1 four input AND gate
2 transistors needed for 1 one input NOT gate
18 transistors needed for 1 eight input AND gate
total no. of transistors = 10 x 8 +2 x 3+ 18 x 1
= 104

On the other hand;

B. For the radiation hardened 8:1 MUX:

14 transistors needed for 1 four input AND gate
4 transistors needed for 1 one input NOT gate
22 transistors needed for 1 eight input gate
total no. of transistors = 14 x 8 +4 x 3+ 22 x 1
= 146.

To make the 8:1 MUX SEU immune 42 extra transistors are needed.

VIII. Layout Design & Area Utilization

A. Cell Layout:

After passing DRC (Design Rule Check) and LVS (Layout vs. Schematic) tests, the cell layout of an 8:1 MUX includes the exact arrangement of transistors, interconnects, and components on a semiconductor substrate to ensure compliance with design specifications and constraints, focusing on minimum blocks.

1) Conventional 8:1 MUX:

The layout design for a conventional 8:1 multiplexer involves arranging transistors, interconnects, and components on a semiconductor substrate to implement the multiplexing functionality efficiently.

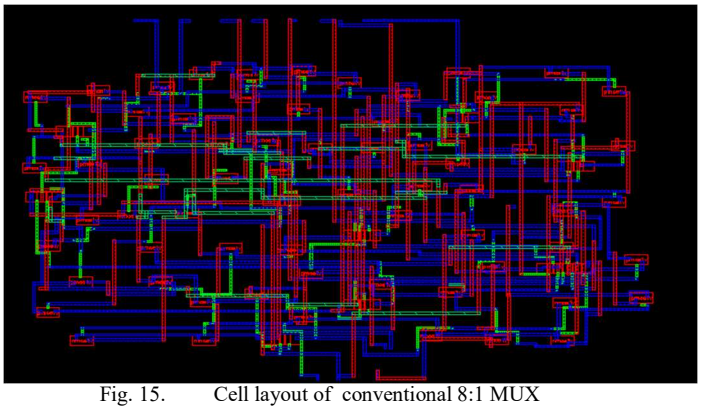

Fig. 15. Cell layout of conventional 8:1 MUX

2) Radiation Hardened 8:1 MUX:

The layout design for a Radiation Hardened 8:1 Multiplexer emphasizes redundant structures and robust interconnects to ensure resilience against radiation-induced upsets.

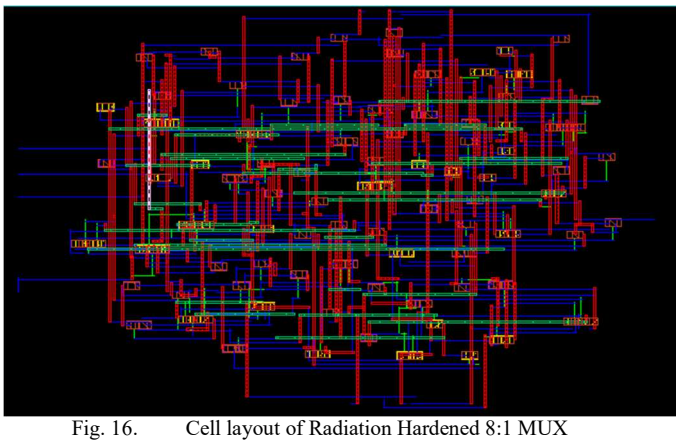

Fig. 16. Cell layout of Radiation Hardened 8:1 MUX

B. Area Utilization:

The Radiation Hardened 8:1 MUX typically has a larger area (1209.0139 μm²) compared to the conventional 8:1 MUX (584.2044 μm²) due to the inclusion of additional redundancy and protective measures against radiation effects. This includes extra transistors, shielding layers, and possibly larger spacing between components to minimize susceptibility to single event upsets (SEUs), ensuring reliability in harsh environments.

IX. Conclusion

The comparative analysis between radiation-tolerant and conventional 8:1 multiplexers in 90 nm technology reveals that the radiation-hardened design requires approximately 40% more transistors. Moreover, several critical differences emerge that underscore their distinct design priorities and performance characteristics. The radiation-hardened 8:1 MUX, designed for resilience in radiation-intensive environments like space, incorporates additional transistors and shielding layers to mitigate single event upsets (SEUs), resulting in a larger footprint (1209.0139 μm²) and higher power consumption (2.605E-6 watts) compared to its conventional counterpart (584.2044 μm² and 1.835E-6 watts respectively). This design approach sacrifices some efficiency for enhanced reliability, evidenced by a longer propagation delay (963.9 picoseconds) to ensure stable operation under radiation-induced stresses. In contrast, the conventional MUX prioritizes speed and efficiency with a smaller footprint and lower power consumption (154.6 picoseconds propagation delay and 1.835E-6 watts), suitable for applications where radiation resilience is not a primary concern. The choice between these designs hinges on specific application requirements, balancing performance metrics with the need for robustness in challenging operational environments.

References

[1] A. Johnston, "Radiation Damage of Electronic and Optoelectronic Devices in Space," *Present. 4th Int. Work. Radiat. Eff. Semicond. Devices Sp. Appl.*, pp. 1–9, 2001, [Online]. Available: https://www.nepp.nasa.gov/docuploads/D41D389D-04D4-4710-BBCFF24F4529B3B3/Dmg_Space-00.pdf

[2] W. Al Tameemi, "Digital Circuits," no. June, 2020, doi: 10.13140/RG.2.2.15774.56641.

[3] P. E. Dodd, S. Member, L. W. Massengill, and S. Member, "Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics," pp. 1–33, 2003.

[4] A. Yan *et al.*, "A Double-Node-Upset Self-Recoverable Latch Design for High Performance and Low Power Application," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 66, no. 2, pp. 287–291, 2019, doi: 10.1109/TCSII.2018.2849028.

[5] R. Teja, "Multiplexer (MUX) And Multiplexing - Complete Guide - ElectronicsHub USA." Accessed: Jun. 24, 2024. [Online]. Available: https://www.electronicshub.org/multiplexerandmultiplexing/[5/12/2024

[6] R. Trivedi, N. M. Devashrayee, U. S. Mehta, N. M. Desai, and H. Patel, "Development of Radiation Hardened by Design(RHBD) primitive gates using 0.18μm CMOS technology," *19th Int. Symp. VLSI Des. Test, VDAT 2015 - Proc.*, no. April 2016, pp. 8–10, 2015, doi: 10.1109/ISVDAT.2015.7208046.

[7] R. Hegde, S. Member, N. R. Shanbhag, and S. Member, "Toward Achieving Energy Efficiency in Presence of Deep Submicron Noise," vol. 8, no. 4, pp. 379–391, 2000.

[8] J. Canaris, "SEU Immune Lofic Family," no. February, pp. 1–13, 2017, [Online]. Available: https://www.researchgate.net/publication/234226154_An_SEU_immune_logic_family

[9] N. Desai, "Design of Low Power Asynchronous 6 Transistor Sram in 45Nm Cmos With the Use of Pass Transistor Based Tree Decoders and Static Cmos Based Timing Circuitry Along With Process Variation Simulation . Introduction :," no. 3, pp. 36–38, 2014.

[10] O. Chertkow, A. Pescovsky, L. Atias, and A. Fish, "Low Power Electronics and Applications A Novel Low Power Bitcell Design Featuring Inherent SEU Prevention and Self Correction Capabilities †," pp. 130–150, 2015, doi: 10.3390/jlpea5020130.

[11] A. Dixit, "Design Low Power High Performance 8 : 1 MUX using Transmission Gate Logic (TGL)," vol. 2, no. 2, pp. 14–20, 2014.

[12] D. Sheet, "8-CHANNEL ANALOG MULTIPLEXER / DEMULTIPLEXER (Radiation Hardened)," Punjab, 2022. [Online]. Available: www.scl.gov.in

[13] G. Sreekanth and B. J. Rao, "Design of 8X1 Low Power Multiplexer by using Transmission Gates," pp. 2465–2470, 2019, doi: 10.15662/IJAREEIE.2019.0811011.

[14] H. L. Hughes and J. M. Benedetto, "Radiation effects and hardening of MOS technology: Devices and circuits," *IEEE Trans. Nucl. Sci.*, vol. 50 III, no. 3, pp. 500–521, 2003, doi: 10.1109/TNS.2003.812928.