# Chapter 4
# Radiation Hardening


## 4.1 Introduction

Due to the extensive usage of electronic systems in harsh environments, considerable research efforts have been dedicated to investigating mitigation techniques against radiation effects. The literature offers a wealth of studies on this topic [1–4]. When components or systems are designed and validated to operate in well-defined radiation environments, they are commonly referred to as "radiation-hardened" or "rad-hard" for short. Radiation hardening strategies can encompass a range of approaches, from modifications in the fabrication process to different circuit design implementations.

The European Cooperation for Space Standardization (ECSS) has proposed a classification of radiation hardening techniques based on the abstraction level in application design, which is depicted in Fig. 4.1. One category of techniques falls under radiation hardening by process (RHBP), which involves modifications in the circuit manufacturing process. Examples of RHBP techniques include variations in doping profiles, substrate technology, and use of different materials. These modifications can have an impact on energy deposition and charge collection processes, as discussed in Chap. 1. However, RHBP techniques are often several generations behind the state-of-the-art CMOS technology, leading to suboptimal performance and higher costs.

On the other hand, radiation hardening by design (RHBD) techniques have demonstrated their effectiveness in providing hardness against radiation effects, particularly in highly integrated technologies [4]. RHBD techniques can be applied at different design levels, ranging from the physical layout level to system-level approaches. At the physical layout level, the objective is to reduce radiation-induced charge collection, while at the system level, the focus is on error masking and prevention of system failures. It is worth noting that certain RHBD techniques discussed in this chapter can be applied across multiple design levels.



Y. Quadros de Aguiar et al., *Single-Event Effects, from Space to Accelerator Environments*, https://doi.org/10.1007/978-3-031-71723-9_4

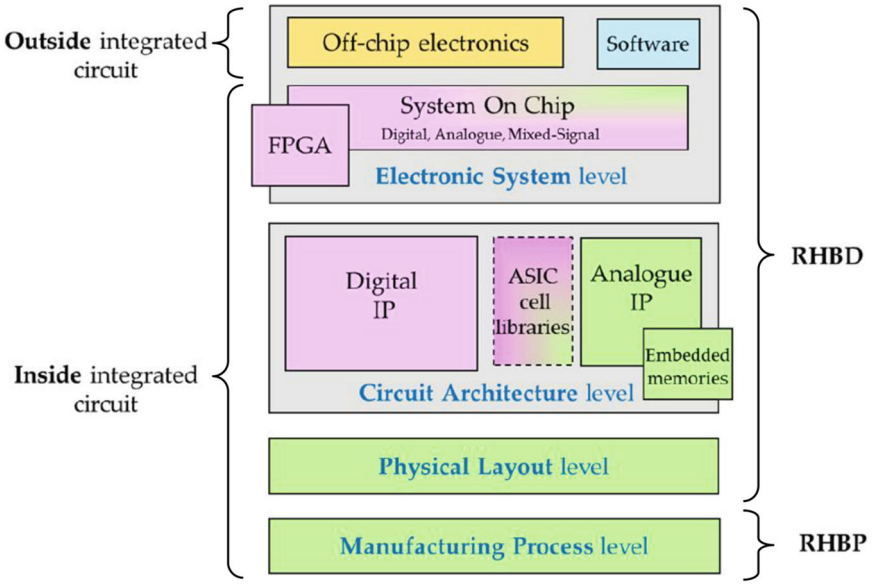


**Fig. 4.1** Classification of hardening techniques based on the abstraction level: from manufacturing process to system level (Adapted from [5])

During the design process, the selection of suitable hardening techniques depends on various factors, including the specific radiation environment, the acceptable error rate for the mission, the available system availability, and the design time and resources allocated. The constraints and requirements of each design scenario guide the choice of appropriate hardening techniques. The RHBD techniques can be applied to existing technologies without requiring extensive modifications to the manufacturing process, resulting in faster implementation and reduced costs. Design-level techniques also provide flexibility in tailoring the hardening approach to the specific requirements and constraints of the circuit. This adaptability is crucial as technological advancements continually introduce new challenges.

Over the past decade, there has been a notable shift in the radiation-hardened paradigm from process to design level, propelled by the market in the spacecraft industry known as *New Space*. Historically, government space agencies have played the biggest role in this industry. However, the emergence of New Space has led to the commercialization of space endeavors, resulting in a surge of private companies developing low-cost technologies for space and providing broader accessibility to these technologies. Consequently, a wide range of space-based applications is emerging and increasing the functionality and complexity of space systems. In order to follow this growing market, public and private actors have increased the adoption of the so-called*commercial off the shelf* (COTS) components due to their performance, availability, cost, and lead time. For instance, it is estimated that over 20% of the electrical, electronic, and electromechanical (EEE) components in

European Space Agency (ESA) satellites are COTS [6]. The COTS components are defined as any component designed for commercial purpose only, not following any military or space standard, i.e., not radiation hardened. In this context, design mitigation techniques must be employed to ensure the functionality and performance of the system under radiation effects. This chapter offers a comprehensive review of the foundations and state-of-the-art radiation hardening techniques, focusing specifically on physical layout and circuit architecture.

## 4.2 Radiation Hardening by Process (RHBP)

Initially, space-qualified components were mostly obtained through the optimization of the manufacturing processes aimed at enhancing the radiation resilience of the process technology itself, i.e., technologies issued from the so-called *rad-hard foundries* [1]. However, these process modifications are often proprietary, making it challenging to access industry-specific information. Nonetheless, these adaptations typically involve the application of different materials, variations in doping profiles, and substrate technologies. For example, studies have demonstrated that removing borophosphosilicate glass (BPSG) layers, commonly used for planarization between metallic layers, can reduce the Single-Event Upset (SEU) rate induced by neutron interactions with boron by about eight to ten times [7, 8]. However, since the adoption of chemical mechanical polishing (CMP) in advanced technologies, BPSG layers are no longer used in the standard manufacturing process, and the main contributor to the thermal neutron SEU rate is the boron isotope $^{10}B$ present in the source/drain junctions of PMOS devices, p-wells, or tungsten plugs [9]. The natural boron ($_5B$) is abundant in two isotopes: the boron-10 ($^{10}B$) in 20% and the boron-11 ($^{11}B$) in 80%. However, the capture cross section of the $^{10}B$ is three orders of magnitude higher than the $^{11}B$, and it is the only one able to release alpha particles that induce Single-Event Effects (SEEs) [10, 11]. Consequently, to mitigate the impact of thermal neutrons, a boron purification process must be integrated into the manufacturing process to reduce the abundance of $^{10}B$.

Each additional manufacturing step introduced to the conventional design process adds complexity and increases the fabrication cost. Hence, these rad-hard technologies cannot follow the transistor scaling trend because the high complexity of the manufacturing steps used to achieve radiation hardness leads to higher costs for usually low-volume production. In this way, the available radiation-hardened technology is normally some generations behind the state-of-the-art transistor technology [4]. One example is Sandia's CMOS7 technology process that provides a rad-hard technology based on a 350 nm silicon-on-insulator (SOI) design process [12]; however, the first commercial 350 nm technology process was adopted in mainstream applications in the early 1990s. Thus, besides the higher price, building chips using rad-hard technologies also provides lower performance when compared with highly integrated commercial technologies. Consequently, space systems using rad-hard technology process may face challenges meeting the performance, power,

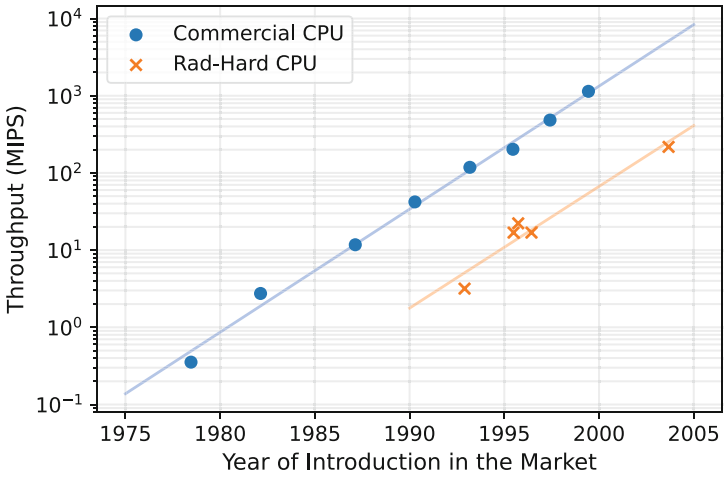


**Fig. 4.2** Comparison of commercial and rad-hard processors in terms of throughput (in million instructions per second, MIPS). (Data retrieved from [1])

and area constraints expected in today's space market. This impact can be clearly observed in Fig. 4.2 where the throughput (expressed in million instructions per second, MIPS) is shown for commercial and rad-hard central processing units (CPUs) according to their year of introduction into the market. The throughput of a CPU is an efficiency coefficient in which the number of instructions that a CPU can execute per unit time is estimated for a given clock rate. The rad-hard CPUs providing the same throughput as the commercial CPUs are introduced into the market, in average, 8-10 years after the introduction of the commercial ones [1].

**Notes**
Radiation hardening, a technology process, increases the fabrication cost and design complexity. Additionally, it is usually limited to technologies generations behind the state-of-the-art ones, leading to lower performances.

One alternative to rad-hard technologies is the adoption of a commercial technology process in which the transistor is built on insulating substrates, i.e., a silicon-on-insulator (SOI) technology [13–15]. Figure 4.3 presents a simplified 2D illustration of an NMOS device fabricated in a bulk technology and in two variants of the SOI technology. In SOI technology, the introduction of an insulation oxide, called a buried silicon oxide (BOX) layer, separates the substrate of the device from its channel and source/drain junctions. In this manner, a reduction of the sensitive volume is obtained, leading to a reduction of the charge collection process in the sensitive nodes and, consequently, improved radiation robustness. Additionally, the

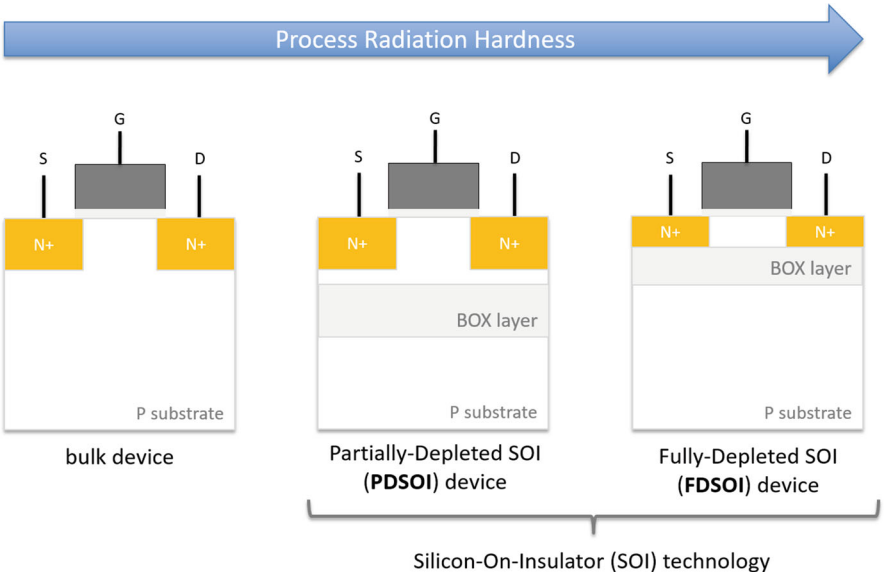


**Fig. 4.3** Simplified representation of an NMOS device manufactured in a bulk technology and two variants of a silicon-on-insulator (SOI) technology

BOX layer prevents the charge sharing effect between adjacent devices due to the suppression of the carrier diffusion mechanism. And, very importantly, the SOI device structure eliminates the parasitic silicon-controlled rectifier (SCR) inherently present between transistors in bulk CMOS circuits and is responsible for triggering the latchup mechanism. Thus, SOI-based designs are intrinsically immune to single-event latchup (SEL) effects [13]. However, despite the smaller sensitive volume and immunity to SEL, a stronger *parasitic bipolar amplification (PBA) effect* is observed, and it might degrade the SEE hardness of the SOI-based circuits. When a particle hits the SOI device, the additional carriers can recombine or drift to the p-n junctions. If the majority carriers in the body are able to drift to the source junction and lower the source-to-body potential, an injection of minority carriers from the source can take place, and additional carriers are collected by the drain junction, increasing the magnitude of the SEE, the PBA effect.

Concerning the two SOI variants from Fig. 4.3, the partially depleted SOI (PDSOI) technology presents the closest electrical and structure characteristics to the traditional bulk technology due to the thickness of the silicon film layer on top of the BOX layer. The silicon film layer can be approximately of 50 nm to 200 nm, providing a large and partially depleted body device and high PBA effect. On the other hand, for the fully depleted SOI (FDSOI) technology, the thickness can reach from 5 nm to 20 nm, resulting into a fully depleted body [16]. Due to a thinner silicon film, the FDSOI devices present a higher switching speed and better SEE hardness in response to the stronger charge inversion and low PBA effect. Although

there is increase in area, body ties have successfully shown to reduce the bipolar amplification, especially for PDSOI devices [15, 17, 18].

As much as RHBP techniques are quite effective in hardening electronics components against radiation effects, the industry has been increasingly investing on the usage of hardening by design techniques. Specially with the introduction of the New Space market in which the space applications require short entry to the market, lower cost and more onboard processing power, high-level hardening techniques or mitigation strategies at the system level are highly adopted. In the next section, hardening techniques at the layout and circuit levels are presented as they are the main topics discussed in the following chapters.

## 4.3 Radiation Hardening by Design (RHBD)

### *4.3.1 Layout-Based Techniques*

RHBD techniques can profit from the improvements in power, performance, and reduced area achieved by state-of-the-art commercially available CMOS technology processes [1]. One established RHBD layout technique used to mitigate leakage current induced by total ionizing dose effects is the adoption of edgeless transistors, also known as *enclosed layout transistors (ELT)* [19, 20]. Figure 4.4 presents a layout comparison between the standard and the edgeless transistors. When a

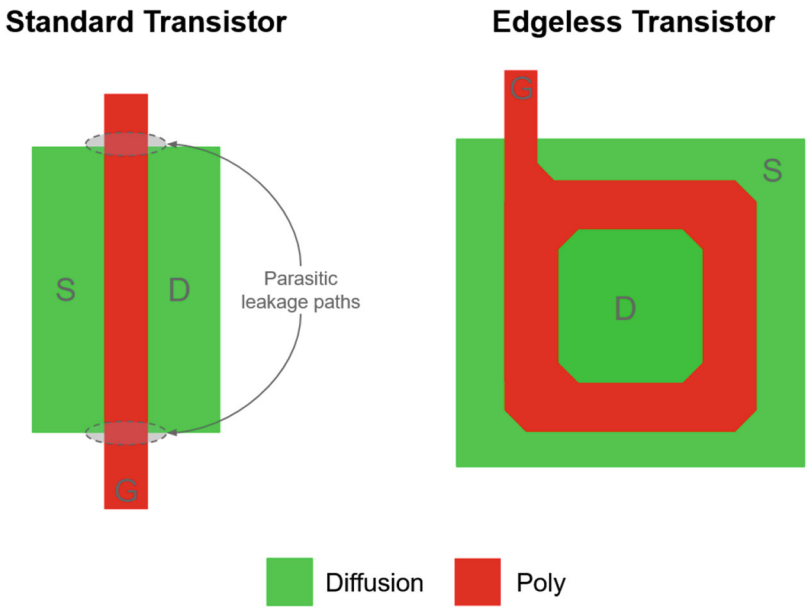


**Fig. 4.4** Comparison between a standard transistor layout and the edgeless transistor layout (ELT)

Metal-Oxide Semiconductor (MOS) device is exposed to radiation ionizing dose, positive charges, i.e., holes, can become trapped within the *shallow trench isolation (STI) oxide* near the source and drain junctions. Depending on the density of trapped holes, a parasitic conduction path can be created in the edge of the NMOS transistors [21]. In such cases, inversion in the p-substrate can occur in this parasitic channel formed at the edge between the oxide and the transistor junctions, leading to leakage current flow between the drain and source junctions. The adoption of an enclosed transistor layout helps avoid the connection between the junctions and the sidewall oxides, thereby eliminating the parasitic channel and reducing radiation-induced leakage current [20]. The parasitic leakage paths for the standard transistor layout are indicated in Fig. 4.4.

The biggest drawbacks of this technique are the area overhead and the limitation on the transistor sizing [20, 22]. For instance, the minimum aspect ratio $W/L$ that can be obtained for an edgeless transistor is approximately 2.26. In digital design, density and performance are the priority, thus L is kept the minimum size while W can vary depending on the constraints. However, in analog design, the $W/L$ can be less than 1 as $L$ is increased to reduce leakage currents in low-power designs. Thus, ELT transistors are quite limited when targeting high-performance or low-power designs. Also, due to the layout complexity and the gate geometry, Simulation Program with Integrated Circuit Emphasis (SPICE) models should be adapted to address the nonlinearity of the channel length modulation [23]. Recently, two other layout modifications have been proposed in comparison to the edgeless transistor: the Z-gate [24] and the I-gate transistor layout [25, 26]. Despite the promising results, more studies should be conducted to verify the applicability of these techniques and their consequent drawbacks.

The adoption of edgeless transistors is only capable of preventing leakage current paths within the transistor itself; however, when two NMOS devices are placed side by side a parasitic leakage path can be formed transistor to transistor through the STI oxide. To prevent that, p+ guard rings are used surrounding the NMOS devices, such that the p+ diffusion obstructs any possible parasitic channel between the +n diffusions. Thus, in order to eliminate both intra-device and inter-device radiation-induced leakage paths, *guard-rings* have been vastly used alongside the edgeless transistors [27, 28]. Figure 4.5 illustrates the structure of guard rings around the PMOS device (n+ guard ring connected to power supply voltage) and the NMOS device (p+ guard ring connected to ground supply voltage). As the guard rings provide electrical and spatial isolation, this technique has also shown to provide SEL immunity besides lowering the TID effects [20, 27]. A study was conducted to assess the hardening effectiveness of guard rings schemes against SEL effects in a 180 nm technology [28]. It was shown that both single and dual guard ring configurations (when both PMOS and NMOS devices have guard rings) can provide SEL immunity up to 100 $\text{MeV.cm}^2/\text{mg}$. Thus, to lower the area overhead, the single guard ring configuration should be used and prioritizing the p+ guard ring that can also reduce radiation-induced leakage of NMOS devices [28].

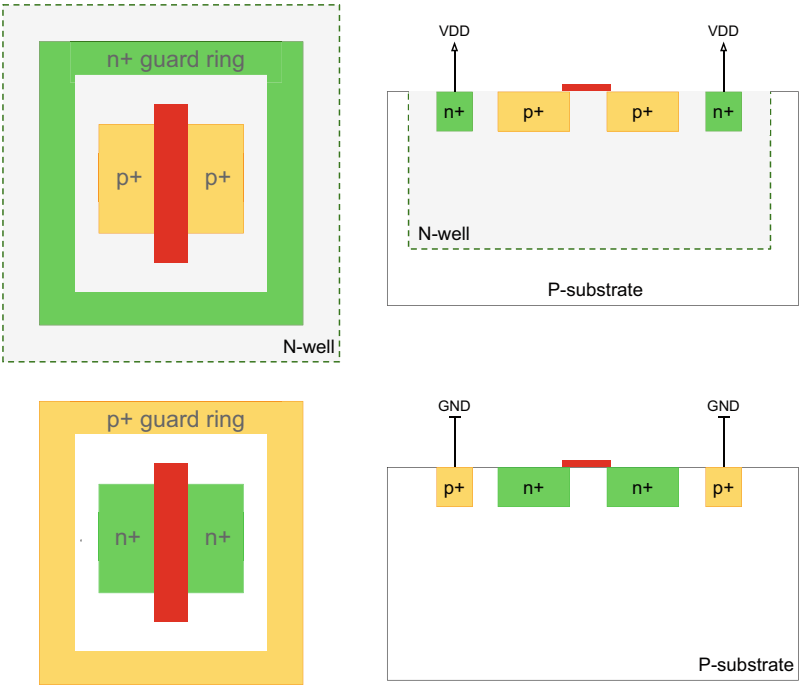


**Fig. 4.5** Layout and cross-sectional representation of guard rings around PMOS and NMOS transistors

**Notes**
Different layout-based techniques can be used alongside in a circuit design; however, their biggest drawbacks are the **increase in area** and **limitation in transistor sizing**.

The transistor positioning within the digital CMOS layout design has also been explored as radiation hardening strategy against SEE [29, 30]. In [29], the placement of NMOS transistors is evaluated in respect to the proximity to the N-well region. Technology Computer Aided Design (TCAD) simulations of an inverter gate with different NMOS positioning ranging from a distance D of 200 nm to 1000 nm from the N-well border are shown in Fig. 4.6. The results show that as closer the device is placed to the N-well region, shorter is the SET pulse width for particle strikes at the NMOS device. This observation was attributed to (1) the reversed-biased diode formed by the N-well and substrate interface which collects the additional carriers and (2) the reinforcement of the recovery current from the PMOS devices while the *off*-state NMOS transistor is hit by the particle. Fig. 4.6 illustrates this phenomenon in which the parasitic bipolar effect in the PMOS device is enhanced by the close

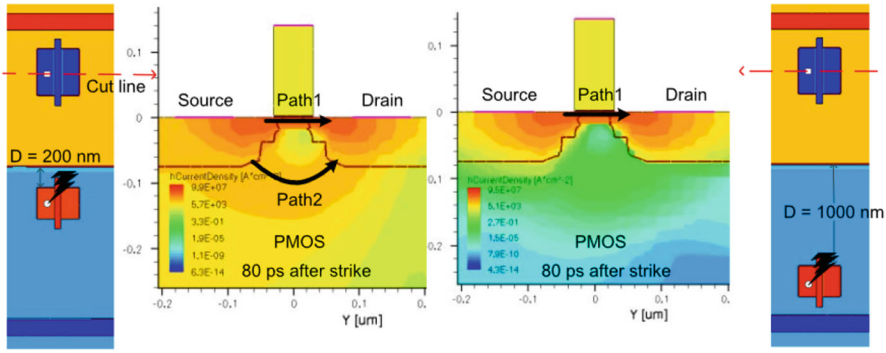


**Fig. 4.6** Recovery current reinforcement induced by the increased parasitic bipolar effect due to the close proximity NMOS device. (Adapted from [29])

proximity of the NMOS device. The design with the NMOS device with a distance D = 200 nm has nearly ten times the collected charge by N-well in the design with D = 1000 nm.

This collected charge is responsible for lowering the electrostatic potential in N-well and activating the parasitic bipolar transistor. With the parasitic bipolar transistor turned *on*, additional carriers will flow from the source to the drain of the PMOS device (Path 2 in the Fig. 4.6), enhancing the recovery current. Although the observed reduction in the SET pulse width, this technique can possibly worsen the SEL resilience of the design, as shown in the TCAD simulations performed in [31]. Due to the activation of the parasitic bipolar transistor, the decrease of the anode-to-cathode (A-C) spacing, i.e., the distance between the PMOS and NMOS devices, has shown a decrease in the threshold LET and an increase in the saturation SEL cross section. Therefore, the designer should have clear in mind the implications of each hardening technique and the target effects intended to mitigate. For instance, the substrate and well tap placement has shown a stronger impact on the SEL sensitivity than the A-C spacing [31]. Thus, to counteract the negative effect of the close proximity NMOS devices, substrate and well tap placement can be used as described in [31].

Another layout technique that uses the transistor placement to improve the SEE robustness is the layout design through error-aware transistor positioning (LEAP) layout technique [30]. In this layout approach, the transistors are placed horizontally in such a way that all the collecting nodes are aligned. The whole idea is to take advantage of the charge collection by the on-state transistors to pull the output voltage back to the expected value. One example of a LEAP-based layout for an inverter gate is shown in Fig. 4.7.

Whenever the particle strikes horizontally, both drain regions will be collecting the additional charges [2, 30]. Due to the horizontal transistor alignment, the charge collected by the *on*-state NMOS transistor will counteract the charge collected by the *off*-state PMOS transistor [30]. Overall, the resulting transient pulse is shortened

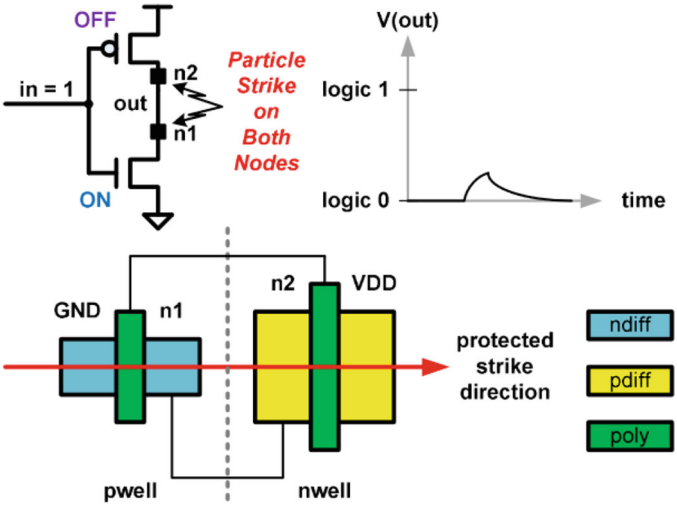


**Fig. 4.7** Illustration of the LEAP principle for an inverter gate. When a particle strikes both NMOS and PMOS drain nodes simultaneously, the charge collected by the on-state transistor reduces the overall transient pulse at the output of the gate. (Adapted from [30])

as the *on*-state NMOS is pulling the output voltage back to the logic 0, a similar principle of the recovery current reinforcement from [29].

The transistor sizing (also known as gate sizing) is another well-known hardening technique based on the radiation-induced transient dependency on the drive strength and nodal capacitance of the circuit [32]. However, by increasing the transistor width, the drain area is also increased, and it can induce a greater charge collection process and increased SEE sensitivity. In the next chapter, the applications of gate sizing, transistor stacking, and transistor folding are investigated.

### *4.3.2 Circuit-Based Techniques*

In addition to layout techniques, radiation effects can be mitigated or partially hardened using circuit-based techniques. As circuit complexity increases in advanced technology, susceptibility to physical defects and environmental disturbances, including radiation, necessitates fault tolerance techniques [33–36]. For instance, safety- and mission-critical systems, such as satellites and aircraft flight control systems, heavily rely on fault tolerance methods to enhance reliability. Fault tolerance ensures system functionality remains intact even in the presence of faults, with redundancy forming the cornerstone of many proposed techniques [35]. Unlike hardening techniques aimed at preventing the generation of SEE, i.e., energy deposition and charge collection, fault tolerance focuses on masking the soft errors. Various approaches exist, involving hardware, software, information, and

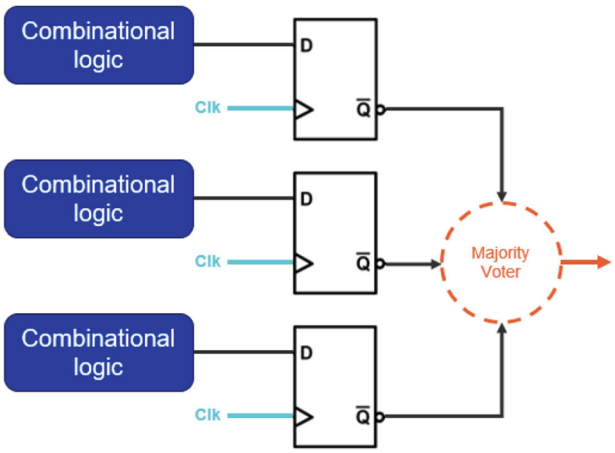


**Fig. 4.8** Diagram of the triple modular redundancy (TMR) fault tolerance technique. Combinational and sequential logic are triplicated and output is connected to a majority voter

time redundancy [33]. Hardware redundancy, also known as spatial redundancy, is particularly prevalent in space applications due to its ability to detect and/or correct faults [34]. A notable example is triple modular redundancy (TMR), illustrated in Fig. 4.8, renowned for its effectiveness in providing robustness against SEEs [35].

In this approach, the critical component is triplicated in the design, and all the three output signals are connected to a majority voter (MJV) circuit where the majority of the input signal determines the output signal. In other words, whenever two of the triplicates are fault-free, the correct output will be propagated. The main drawback of this technique is clearly the massive increase in area (two duplicates + MJV circuit) and the consequent increase in power consumption. Also, despite the good fault coverage, the technique relies on the robustness of the MJV circuit, because, even if the three components are fault-free, whenever a particle hits the voter and deposits sufficient charge, the SET or SEU will be propagated. Various TMR variants have been proposed to address these challenges, including diversity TMR (DTMR) [37], where different design implementations are used for triplicated modules, and approximate TMR (ATMR) [38], which employs approximate functions instead of exact replicas of the main function. Both variants offer a balanced compromise between area/performance overhead and fault tolerance against SEEs compared to traditional TMR schemes. For instance, Fig. 4.9 presents an example of a temporal TMR, where delay units are added to filter SET pulses to be latched in all flip-flops. This approach can surely reduce the area overhead as the combinational logic is not triplicated, but can impact the performance of the circuit.

While the redundancy technique was initially largely applied at the circuit level, it has also found application in higher levels such as in field-programmable gate arrays (FPGAs), system on chip (SoC), and software-based redundancy [33, 37, 38].

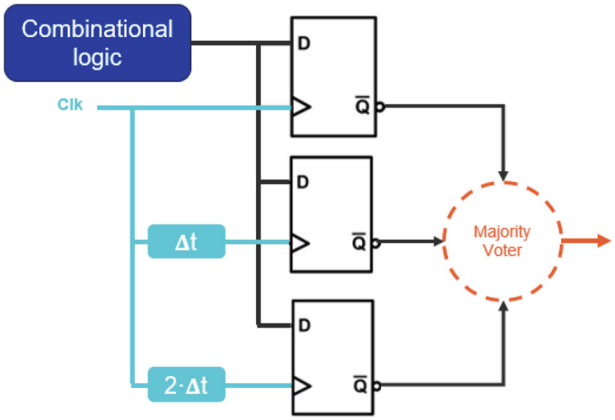


**Fig. 4.9** Diagram of the temporal triple modular redundancy (TMR) scheme. Only the sequential logic is triplicated and output is connected to a majority voter, while delay units are used to offset the clock signal and filter the SET pulse from propagating through the majority voter

In contrast to hardware-based TMR implementations, software-level redundancy introduces concerns about execution time overhead.

**Redundancy** is a mitigation strategy that can be applied in several abstraction levels, from physical and logical to temporal domain.

Another widely used approach at the circuit level is to harden memory cells by using redundant reinforced feedback architectures such as the *dual interlocked storage cell (DICE)* and *Quatro* circuits [39, 40]. These circuit topologies are applied for the design of a 1-bit Static Random Access Memory (SRAM) cell and are shown in Figs. 4.10 and 4.11. Instead of using a single cross-coupled inverter pair as in the standard 6T SRAM design, both circuits have a feedback mechanism sustained by interlocked structures that guarantee the correct output whenever a single sensitive node collects charge. These structures ensure that the stored bit in the memory cell is defined by more than a single pull-down/pull-up network. Although a good radiation response can be achieved, these designs have degraded read/write performance and high area overhead.

The radiation hardness of the DICE cell has been extensively validated through simulations and experiments, being the main reference design for hardening technique in memory circuit designs in the literature [34, 41, 42]. The Quatro design was proposed in [40] as an alternative to the traditional DICE cell with a lower area overhead and better data stability. Some works have shown that flip-flops and SRAM designs based on the Quatro topology have a higher SEU robustness than the DICE cells [43–46]. However, with the close proximity of transistors in deeply

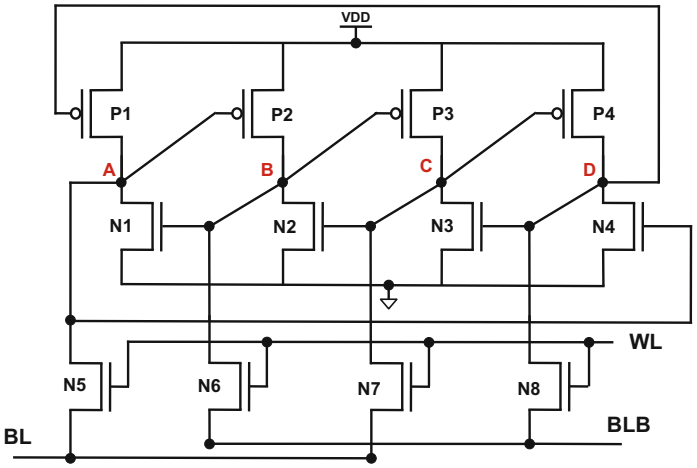


**Fig. 4.10** DICE memory cell schematics

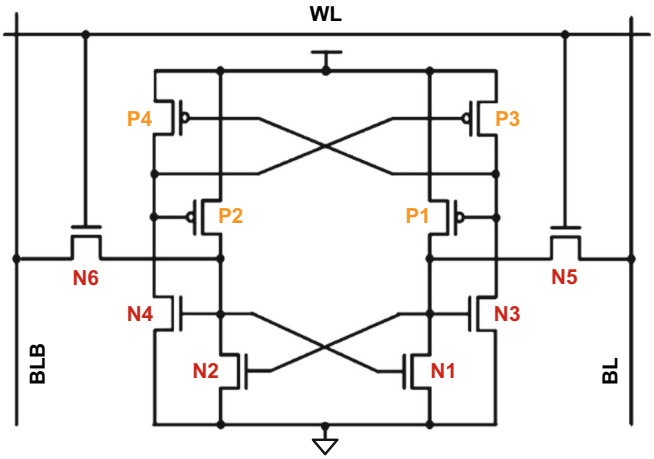


**Fig. 4.11** Q10T memory cell schematics

scaled transistor technologies, the impact of charge sharing effects has shown to be a concern for the reliability of these architectures. To address this issue, circuit-based RHBD techniques can be combined along with the layout-based techniques shown in the last section. For instance, the LEAP technique was applied in the DICE design for flip-flops in [2, 30].

The LEAP-DICE flip-flops at 28 nm bulk technology have shown a reduction of the SEU rate of approximately two orders of magnitude when compared to the traditional DICE layout design [2]. Unlike the LEAP technique, which seeks to position specific transistors closer together to leverage charge sharing for improving overall SEE sensitivity, other design approaches focus on increasing nodal spacing.

This strategy is aimed at mitigating the effects of multiple node charge collection in critical nodes. By physically separating these nodes, the probability of a single particle strike causing simultaneous charge collection at multiple sensitive areas is reduced, thereby enhancing the resilience of the circuit to radiation-induced soft errors [42, 47, 48]. With the transistor scaling, the layout design carries a stronger influence on the circuit reliability when considering radiation effects. Accordingly, more and more techniques have been adopted at the layout level to mitigate the effect of multiple node collection and parasitic bipolar amplification [24, 26, 49–53].

## 4.4 Summary

The increased utilization of electronic systems in radiation environments, including space, aviation, medical applications, and particle accelerators, has underscored the need to explore various hardening techniques to ensure the reliability of these systems. This chapter presented a comprehensive review of fundamental concepts related to radiation hardening techniques against mostly single-event effects (SEE). One approach to enhancing radiation hardness is through process modifications during circuit fabrication, known as radiation hardening by process (RHBP) techniques. These techniques involve altering the manufacturing process to improve radiation resilience. However, with the growing demand for high-performance and low-power solutions, radiation hardening by design (RHBD) techniques have emerged as a promising alternative, particularly when integrated with commercial deeply scaled technologies.

Layout-based RHBD techniques are particularly effective in addressing charge collection mechanisms induced by particle strikes, as they directly impact the charge collection efficiency in sensitive nodes of the circuit. At the circuit level, techniques often utilize redundancy to reinforce logic bits in memory cells or employ voting schemes to mask SEE occurrences. When designing a critical system for a radiation environment, various parameters must be considered to select the appropriate hardening techniques. Combining multiple techniques can achieve the desired level of hardness, but it is important to carefully analyze the associated area, power, and performance overheads to ensure that the reliability requirements are met while respecting design constraints.

The subsequent chapter provides a detailed analysis of layout-based RHBD techniques, offering valuable insights into their implementation and effectiveness. By examining these techniques, designers and researchers can gain a deeper understanding of their capabilities and limitations, enabling them to make informed decisions when developing radiation-hardened systems.

**Highlights**

- Radiation hardening by process (RHBP) techniques can be used in the manufacturing process to increase the reliability of a transistor technology.
- Radiation hardening by design (RHBD) techniques can be adopted from the physical layout level to the system level to reduce the radiation-induced charge collection or to mitigate system failures.
- Despite the effectiveness of RHBP techniques, their limitations in terms of fabrication cost and performance make the RHBD more attractive for most applications.
- Layout-based techniques can reduce the efficiency of the charge collection process, but one of their limitations is the increase in design area and constraints in the transistor sizing.
- Redundancy is a popularly used mitigation technique that can be implemented in different forms, in the physical, temporal, or information domains, and, therefore, it can be adapted to the most diverse field of applications.

## References

1. Ronald C Lacoe. Improving integrated circuit performance through the application of hardness-by-design methodology. *IEEE transactions on Nuclear Science*, 55 (4): 1903–1925, 2008.
2. K Lilja, M Bounasser, S-J Wen, R Wong, J Holst, N Gaspard, S Jagannathan, D Loveless, and B Bhuva. Single-event performance and layout optimization of flip-flops in a 28-nm bulk technology. *IEEE Transactions on Nuclear Science*, 60 (4): 2782–2788, 2013.
3. Wen Zhao, Chaohui He, Wei Chen, Rongmei Chen, Peitian Cong, Fengqi Zhang, Zujun Wang, Chen Shen, Lisang Zheng, Xiaoqiang Guo, et al. Single-event multiple transients in guard-ring hardened inverter chains of different layout designs. *Microelectronics Reliability*, 87: 151–157, 2018.
4. Ronald C Lacoe, Jon V Osborn, Rocky Koga, Stephanie Brown, and Donald C Mayer. Application of hardness-by-design methodology to radiation-tolerant ASIC technologies. *IEEE Transactions on Nuclear Science*, 47 (6): 2334–2341, 2000.
5. ECSS Secretariat. Space product assurance: Techniques for radiation effects mitigation in ASICs and FPGAs handbook. 2016.
6. Mikko Nikulainen. Usage of cots EEE components in ESA space programs, 2019. URL https://escies.org/webdocument/showArticle?id=1064&groupid=6.
7. Robert C Baumann and Eric B Smith. Neutron-induced boron fission as a major source of soft errors in deep submicron SRAM devices. In *2000 IEEE International Reliability Physics Symposium Proceedings. 38th Annual (Cat. No. 00CH37059)*, pages 152–157. IEEE, 2000.
8. Raoul Velazco and Francisco J Franco. Single event effects on digital integrated circuits: Origins and mitigation techniques. In *2007 IEEE International Symposium on Industrial Electronics*, pages 3322–3327. IEEE, 2007.

9. Marcos Olmos, Remi Gaillard, Andreas Van Overberghe, Jerome Beaucour, Shijie Wen, and Sung Chung. Investigation of thermal neutron induced soft error rates in commercial SRAMs with 0.35 $\mu$m to 90 nm technologies. In *2006 IEEE International Reliability Physics Symposium Proceedings*, pages 212–216. IEEE, 2006.
10. Elizabeth C Auden, Heather M Quinn, Stephen A Wender, John M O'Donnell, Paul W Lisowski, Jeffrey S George, Ning Xu, Dolores A Black, and Jeffrey D Black. Thermal neutron-induced single-event upsets in microcontrollers containing boron-10. *IEEE Transactions on Nuclear Science*, 67 (1): 29–37, 2019.
11. Daniel Oliveira, Sean Blanchard, Nathan Debardeleben, Fernando F Dos Santos, Gabriel Piscoya Dávila, Philippe Navaux, Carlo Cazzaniga, Christopher Frost, Robert C Baumann, and Paolo Rech. Thermal neutrons: a possible threat for supercomputers and safety critical applications. In *2020 IEEE European Test Symposium (ETS)*, pages 1–6. IEEE, 2020.
12. Kwok-Kee Ma, John Teifel, and Richard S Flores. Sandia rad-hard, fast turn structured asic. Technical report, Sandia National Lab.(SNL-NM), Albuquerque, NM (United States), 2011.
13. O Musseau. Single-event effects in SOI technologies and devices. *IEEE Transactions on Nuclear Science*, 43 (2): 603–613, 1996.
14. JR Schwank, V Ferlet-Cavrois, MR Shaneyfelt, P Paillet, and PE Dodd. Radiation effects in SOI technologies. *IEEE Transactions on nuclear Science*, 50 (3): 522–538, 2003.
15. Philippe Roche, Jean-Luc Autran, Gilles Gasiot, and Daniela Munteanu. Technology downscaling worsening radiation effects in bulk: SOI to the rescue. In *2013 IEEE International Electron Devices Meeting*, pages 31–1. IEEE, 2013.
16. Andrew Marshall and Sreedhar Natarajan. PD-SOI and FD-SOI: a comparison of circuit performance. In *9th International Conference on Electronics, Circuits and Systems*, volume 1, pages 25–28. IEEE, 2002.
17. K Hirose, H Saito, Y Kuroda, S Ishii, Y Fukuoka, and D Takahashi. SEU resistance in advanced SOI-SRAMs fabricated by commercial technology using a rad-hard circuit design. *IEEE Transactions on Nuclear Science*, 49 (6): 2965–2968, 2002.
18. K Hirose, H Saito, S Fukuda, Y Kuroda, S Ishii, D Takahashi, and K Yamamoto. Analysis of body-tie effects on SEU resistance of advanced FD-SOI SRAMs through mixed-mode 3-d simulations. *IEEE transactions on nuclear science*, 51 (6): 3349–3353, 2004.
19. JV Osborn, RC Lacoe, DC Mayer, and G Yabiku. Total dose hardness of three commercial CMOS microelectronics foundries. In *RADECS 97. Fourth European Conference on Radiation and its Effects on Components and Systems (Cat. No. 97TH8294)*, pages 265–270. IEEE, 1997.
20. G Anelli, M Campbell, M Delmastro, F Faccio, S Floria, A Giraldo, E Heijne, P Jarron, K Kloukinas, A Marchioro, et al. Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: practical design aspects. *IEEE Transactions on Nuclear Science*, 46 (6): 1690–1696, 1999.
21. RC Hughes, EP EerNisse, and HJ Stein. Hole transport in MOS oxides. *ITNS*, 22: 2227–2233, 1975.
22. Marc Gaillardin, Martial Martinez, Sylvain Girard, Vincent Goiffon, Philippe Paillet, Jean-Luc Leray, Pierre Magnan, Youcef Ouerdane, Aziz Boukenter, Claude Marcandella, et al. High total ionizing dose and temperature effects on micro-and nano-electronic devices. *IEEE Transactions on Nuclear Science*, 62 (3): 1226–1232, 2015.
23. Varvara Bezhenova and Alicja Michalowska-Forsyth. Aspect ratio of radiation-hardened MOS transistors. *e & i Elektrotechnik und Informationstechnik*, 135 (1): 61–68, 2018.
24. Ying Wang, Chan Shan, Wei Piao, Xing-ji Li, Jian-qun Yang, Fei Cao, and Cheng-hao Yu. 3D numerical simulation of a Z gate layout MOSFET for radiation tolerance. *Micromachines*, 9 (12): 659, 2018.
25. Minwoong Lee, Seongik Cho, Namho Lee, and Jongyeol Kim. Novel logic device for CMOS standard I/O cell with tolerance to total ionizing dose effects. *Solid-State Electronics*, 162: 107630, 2019.
26. Minwoong Lee, Seongik Cho, Namho Lee, and Jongyeol Kim. Design for high reliability of CMOS IC with tolerance on total ionizing dose effect. *IEEE Transactions on Device and Materials Reliability*, 2020.

27. Federico Faccio. Design hardening methodologies for asics. In *Radiation Effects on Embedded Systems*, pages 143–160. Springer, 2007.
28. NA Dodds, NC Hooten, RA Reed, RD Schrimpf, JH Warner, NJ-H Roche, D McMorrow, S-J Wen, R Wong, JF Salzman, et al. Effectiveness of SEL hardening strategies and the latchup domino effect. *IEEE Transactions on Nuclear Science*, 59 (6): 2642–2650, 2012.
29. Zhenyu Wu and Shuming Chen. nMOS transistor location adjustment for N-hit single-event transient mitigation in 65-nm CMOS bulk technology. *IEEE Transactions on Nuclear Science*, 65 (1): 418–425, 2017.
30. Lee Hsiao-Heng Kelin, Lilja Klas, Bounasser Mounaim, Relangi Prasanthi, Ivan R Linscott, Umran S Inan, and Mitra Subhasish. Leap: Layout design through error-aware transistor positioning for soft-error resilient sequential cell design. In *2010 IEEE International Reliability Physics Symposium*, pages 203–212. IEEE, 2010.
31. S Guagliardo, Frédéric Wrobel, Y. Q. Aguiar, J-L Autran, P Leroux, F Saigné, V Pouget, and Antoine Touboul. Single event latchup cross section calculation from TCAD simulations–effects of the doping profiles and anode to cathode spacing. In *IEEE RADECS 2019*, 2019.
32. Quming Zhou and Kartik Mohanram. Gate sizing to radiation harden combinational logic. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 25 (1): 155–166, 2005.
33. Barry Johnson. Fault-tolerant microprocessor-based systems. *IEEE Micro*, (6): 6–21, 1984.
34. Michael Nicolaidis. Design for soft error mitigation. *IEEE Transactions on Device and Materials Reliability*, 5 (3): 405–418, 2005.
35. Fernanda Lima Kastensmidt, Luigi Carro, and Ricardo Augusto da Luz Reis. *Fault-tolerance techniques for SRAM-based FPGAs*, volume 1. Springer, 2006.
36. Robert C Baumann. Radiation-induced soft errors in advanced semiconductor technologies. *Device and Materials Reliability, IEEE Transactions on*, 5 (3): 305–316, 2005.
37. Lucas A Tambara, Fernanda L Kastensmidt, José Rodrigo Azambuja, Eduardo Chielle, Felipe Almeida, Gabriel Nazar, Paolo Rech, Christopher Frost, and Marcelo S Lubaszewski. Evaluating the effectiveness of a diversity TMR scheme under neutrons. In *2013 14th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, pages 1–5. IEEE, 2013.
38. GS Rodrigues, JS Fonseca, FL Kastensmidt, V Pouget, Alberto Bosio, and S Hamdioui. Approximate TMR based on successive approximation and loop perforation in microprocessors. *Microelectronics Reliability*, 100: 113385, 2019.
39. Teodor Calin, Michael Nicolaidis, and Raoul Velazco. Upset hardened memory design for submicron cmos technology. *IEEE Transactions on nuclear science*, 43 (6): 2874–2878, 1996.
40. Shah M Jahinuzzaman, David J Rennie, and Manoj Sachdev. A soft error tolerant 10T SRAM bit-cell with differential read capability. *IEEE Transactions on Nuclear Science*, 56 (6): 3768–3773, 2009.
41. David G Mavis and Paul H Eaton. Soft error rate mitigation techniques for modern microcircuits. In *2002 IEEE International Reliability Physics Symposium. Proceedings. 40th Annual (Cat. No. 02CH37320)*, pages 216–225. IEEE, 2002.
42. Maxim S Gorbunov, Pavel S Dolotov, Andrey A Antonov, Gennady I Zebrev, Vladimir V Emeliyanov, Anna B Boruzdina, Andrey G Petrov, and Anastasia V Ulanova. Design of 65 nm CMOS SRAM for space applications: A comparative study. *IEEE Transactions on Nuclear Science*, 61 (4): 1575–1582, 2014.
43. S Jagannathan, TD Loveless, BL Bhuva, S-J Wen, R Wong, M Sachdev, D Rennie, and LW Massengill. Single-event tolerant flip-flop design in 40-nm bulk CMOS technology. *IEEE Transactions on Nuclear Science*, 58 (6): 3033–3037, 2011.
44. David J Rennie and Manoj Sachdev. Novel soft error robust flip-flops in 65nm CMOS. *IEEE Transactions on Nuclear Science*, 58 (5): 2470–2476, 2011.
45. Qiong Wu, Yuanqing Li, Li Chen, Anlin He, Gang Guo, Sang H Baeg, Haibin Wang, Rui Liu, Lixiang Li, Shi-Jie Wen, et al. Supply voltage dependence of heavy ion induced sees on 65 nm CMOS bulk SRAMs. *IEEE Transactions on Nuclear Science*, 62 (4): 1898–1904, 2015.

46. Haibin Wang, Jiamin Chu, Jinghe Wei, Junwei Shi, Hongwen Sun, Jianwei Han, and Rong Qian. A single event upset hardened flip-flop design utilizing layout technique. *Microelectronics Reliability*, 102: 113496, 2019.
47. NJ Gaspard, S Jagannathan, ZJ Diggins, MP King, SJ Wen, R Wong, TD Loveless, K Lilja, M Bounasser, T Reece, et al. Technology scaling comparison of flip-flop heavy-ion single-event upset cross sections. *IEEE Transactions on Nuclear Science*, 60 (6): 4368–4373, 2013.
48. Manuel Cabanas-Holmen, Ethan H Cannon, Salim Rabaa, Tony Amort, Jon Ballast, Michael Carson, Duncan Lam, and Roger Brees. Robust SEU mitigation of 32 nm dual redundant flip-flops through interleaving and sensitive node-pair spacing. *IEEE Transactions on Nuclear Science*, 60 (6): 4374–4380, 2013.
49. Jianjun Chen, Shuming Chen, Bin Liang, and Biwei Liu. Simulation study of the layout technique for P-hit single-event transient mitigation via the source isolation. *IEEE Transactions on Device and Materials Reliability*, 12 (2): 501–509, 2012a.
50. Jianjun Chen, Shuming Chen, Yibai He, Junrui Qin, Bin Liang, Biwei Liu, and Pengcheng Huang. Novel layout technique for single-event transient mitigation using dummy transistor. *IEEE Transactions on Device and Materials Reliability*, 13 (1): 177–184, 2012b.
51. Chunhua Qi, Liyi Xiao, Tianqi Wang, Jie Li, and Linzhe Li. A highly reliable memory cell design combined with layout-level approach to tolerant single-event upsets. *IEEE Transactions on Device and Materials Reliability*, 16 (3): 388–395, 2016.
52. Chunyu Peng, Jiati Huang, Changyong Liu, Qiang Zhao, Songsong Xiao, Xiulong Wu, Zhiting Lin, Junning Chen, and Xuan Zeng. Radiation-hardened 14T SRAM bitcell with speed and power optimized for space application. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 27 (2): 407–415, 2018.
53. Jeffrey D Black, Dolores A Black, Nicholas A Domme, Paul E Dodd, Patrick J Griffin, R Nathan Nowlin, James M Trippe, Joseph G Salas, Robert A Reed, Robert A Weller, et al. DFF layout variations in CMOS SOI–analysis of hardening by design options. *IEEE Transactions on Nuclear Science*, 2020.