Development of Radiation Hardened By Design(RHBD) Primitive Gates using 0.18µm CMOS Technology

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***Abstract*—Radiation Hardened By Design (RHBD) combinational circuits/primitive gates using 0.18um CMOS Technology is developed for Space application with help of Cogenda TCAD software suite. The proposed combinational cells are investigated for radiation simulation using three dimensional (3D) device structure. Single Event Transient (SET) caused by proton, α particle and heavy ions like C, Ar and Kr is observed on developed Cells and SET pulse width is measured on primitive gates. The proposed C element based radiation hardened Inverter is simulated using α, Ar and proton energetic particle. Proposed NOR and NAND gates are simulated under the radiation of proton, α and Kr and Single Event Transient Pulse Width is measured.**

Keywords*—Radiation Hardened by Design(RHBD), Heavy Ion, 0.18um CMOS Technology, Single Event Transient (SET)

I. Introduction

Integrated circuits devoted to space applications require special care during their design, manufacturing and qualification processes as they will be operating in a harsh radioactive environment composed of various energetic particles. The diversity in nature and energy of particles present in this environment is a threat for electronic equipment as they can provoke different type of undesired effects[1]-[3]. When a particle strikes on critical region of the device, it's transfer the energy in to the PN junction. Because of energy transfer in to the material it's generates electron–hole pairs which are collected at the PN junction and leading a transient current pulse on the struck node. As technology feature sizes decrease, SETs is major radiation effects in microcircuits because of circuits are become fast, comparative low power, small node capacitance and high operating clock frequencies[4].

II. Proposed Radiation Hardened Inverter, NOR and NAND Gate

Designed Inverter is based on C-element shown in Fig. 1. Designed NOR and NAND gate based on J.Canaris combinational logic design [5] and then modified NOR and NAND gate based on 0.18um technology shown in Fig. 2 and Fig. 3. In normal inverter based on 0.18um technology with W/L ratio of same as C-element based inverter, noise margin of C-element based inverter is improved than normal inverter.

For normal inverter V_{IH} = 0.92 V and for C-element based inverter V_{IH} = 0.87V. So if energy particle hit on output node of inverter cell (drain of nMOS) when input is 0, at that time due to generation of radiation current nMOS transistor will turn on and output start towards V_{SS} of the gate. So next logic of circuit will consider logic 1 up to 0.87V in case of C-element based inverter. Same noise margin of NAND and NOR gate is improved compared to conventional NAND and NOR gates.

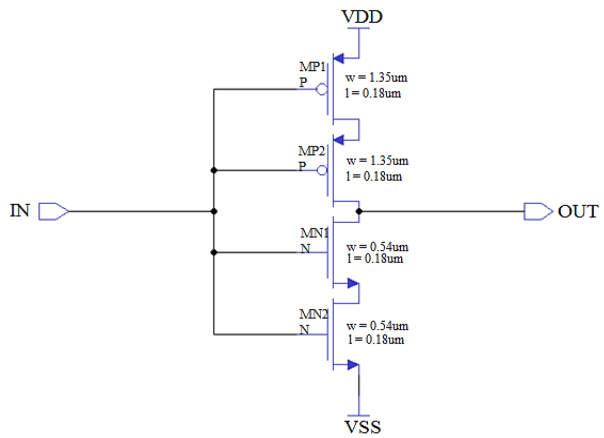

Fig. 1. Proposed C-element based Inverter

III. Radiation Simulation Setup for Proposed Primitive Gates

The GENIUS simulation tool from COGENDA is used for 3-D simulations. This software solves the transient semiconductor device equations in three dimensions, including the Poisson equation and the current continuity equations. The 3-D structure is generated from layout dimensions of 0.18um technology using GDS2MESH tool. The W/L ratio of the transistors, for nMOS is 3 and for pMOS is 7.5. For radiation simulations models were used as follows: Auger recombination , Fermi–Dirac statistics, Shockley–Read–Hall (SRH), band gap narrowing effect (BGN), impact ionization. Here in substrate using Lombardi mobility model which takes into account the mobility variation with the normal and parallel electric field, doping concentration. In GENIUS, the generation rate of e-h pair produced by a heavy ion track is Gaussian function response tmax of the Gaussian function

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response at 10 ps with a characteristic decay time of 2 ps. The choice of mentioned parameters does not depends on any specific ion and energy.

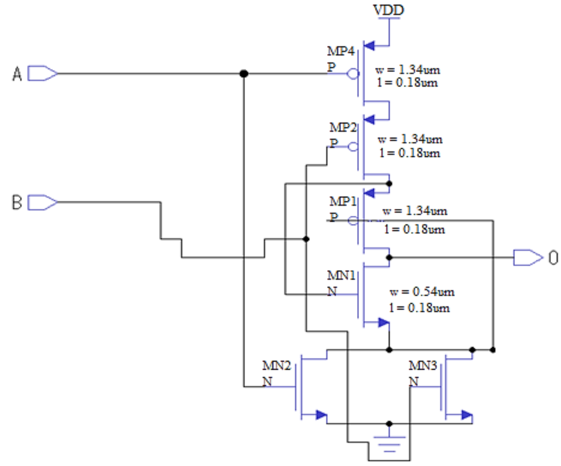

Fig. 2. Proposed NOR Gate

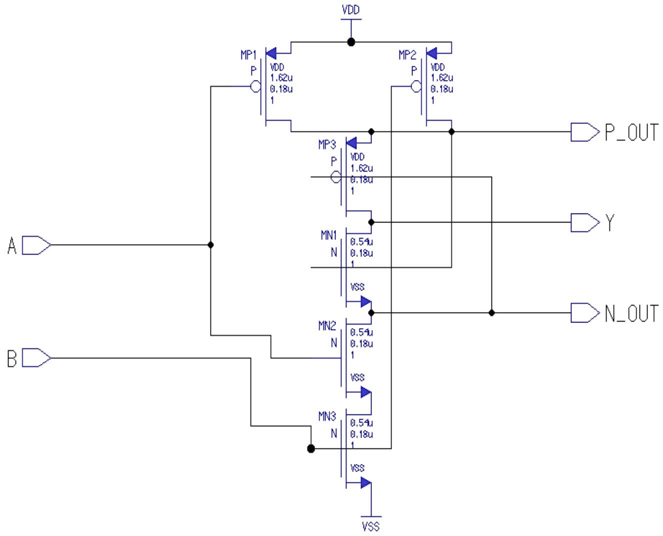

Fig. 3. Proposed NAND Gate

The time parameter is needed for simulating the e-h pair generation. The chosen time is short enough to create of a real track. Thickness of substrate decide based on depth of penetration of particle inside silicon using SRIM tool. LEO orbit proton energy is found up to 500MeV. TABLE I shows results of radiation simulation with different particle with different energy on Proposed Inverter when input is 0 and output is at VDD(logic 1). Striking node is off nMOS(MN1) transistor. TABLE II shows results of radiation simulation with different particle with different energy on Proposed NOR gate when output is at VDD(logic-1).Heavy Particles are Strike on off nMOS transistor(MN1) of proposed NOR gate. Radiation simulation of Argon particle on C-element based inverter when nMOS is off state and hit Ar with 100MeV and 400MeV Zero inclination. Ar with 100MeV penetrated in silicon 26.32um and Ar with 400MeV penetrated 130.10um. TABLE III shows results of radiation current pulse magnitude and pulse width in case of Argon particle with energy 100MeV and 400MeV.

TABLE I. RADIATION SIMULATION OF PROPOSED INVERTER WITH DIFFERENT PARTICLE

Ion	Energy	Tmax(ps)	Voltage (Volt)	Recovery Time(ps)
Alpha	10MeV	15ps	1.71	40ps
Proton	10KeV	10ps	1.78	20ps
	100MeV	10ps	1.78	20ps
Carbon	50MeV	18ps	1.55	434ps
	80MeV	17ps	1.61	313ps
Argon	400MeV	261ps	0.04	440ps

TABLE II. RADIATION SIMULATION OF PROPOSED NOR GATE WITH DIFFERENT PARTICLE

Ion	Energy	Tmax(ps)	Voltage (Volt)	Recovery Time(ps)
Alpha	50MeV	17ps	1.5	80ps
Proton	10KeV	10ps	1.78	18ps
	100MeV	10ps	1.78	19ps
Carbon	50MeV	51ps	1.53	666ps
Krypton	886MeV	90ps	-0.73	910ps

TABLE III. RADIATION CURRENT COMPARISON OF ARGON WITH DIFFERENT ENERGY

Ion	Energy	Current(mA)	Pulse width(ps)
Argon	100MeV	0.44	2.5
	400MeV	0.39	16

IV. Conclusion

In this paper, Design of Radiation Hardened inverter, NOR and NAND are proposed for Van Allan Belt Environment. Particle energy are choose according to test facility available at Lawrence Berkeley laboratory (LBL) and depth of penetration calculated help of SRIM tool. Proposed primitives gates have NML and NMH better than conventional gates. So permissible range for propagating SET pulse without causing any error in next level of circuit is better than conventional gate. It is observed that when the distance between the track and drain increases value of the drain current decreases. But as the peak of the drain current is reduced.

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