2020 International Conference for Emerging Technology (INCET)
Belgaum, India. Jun 5-7, 2020

Design of a 4 Bit Arithmetic & Logic Unit, Evaluation of Its Performance Metrics & its Implementation in a Processor

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***Abstract*— Device scaling has been trending due to its sleek and small dimensions yet its energy efficiency limits itself. With the increasing demand for speed, portability and miniaturization of current gadgets, the power consumption of these products has become a major design factor. Especially for mobile devices, the power consumption drives the battery life-time, the generated heat and the required heat dispersion measures. Therefore, this demands a reduction in the power dissipation of digital circuits. Processors have become increasingly complex and power hungry. There are many applications of microprocessors with limited resources, where energy efficiency becomes a critical requirement. Power dissipation depends on the CMOS fabrication technology, operating frequency, but most of all on the switching per clock cycle within the digital circuit. Power consumption due to device parasites is another major design issue. This paper implements an Arithmetic & Logic Unit (ALU) that is both Ultra-Low Power and High Speed. The design was implemented in 45nm technology. The proposed ALU was implemented in Digital Environment with Verilog HDL so as to optimize the design.**

***Index Terms*—Device Scaling, Miniaturization, Power Dissipation, CMOS, ALU, Ultra-Low Power, High Speed, 45nm, Verilog HDL.**

I. INTRODUCTION

Recent advancements in the technological spheres have brought out some key trends that proves to be a boon as well as a bane. The features that made the electronic gadgets portable also made them power hungry. Although device scaling has been trending due to its sleek and small dimensions yet its energy efficiency limits itself. With the increasing demand for speed, portability and miniaturization of current gadgets, the power consumption of these products has become a major design factor [6]. Especially for mobile devices, the power consumption drives the battery life-time, the generated heat and the required heat dispersion measures. Therefore, the designers and consumers of electronic devices, as well as environmental considerations, demand a reduction in the power dissipation of digital circuits [4].

Implementation of microprocessors in devices is on the rise so as to achieve the multiple tasks, one device goal. Processors have become increasingly complex and power hungry. There are many applications of microprocessors with limited resources, where energy efficiency becomes a critical requirement. Power dissipation depends on the CMOS fabrication technology, operating frequency, but most of all on the switching per clock cycle within the digital circuit. Power consumption due to device parasites is another major design issue. Complexity of the processors are resulting in consuming a considerable amount of power [4]. As the computational block for any processor is an Arithmetic & Logic Unit (ALU), therefore, in this paper we have designed an ultra-low power and high speed ALU in 45nm technology which when implemented in a processor would lead to an overall decrease in power consumption.

This paper proposes a custom CMOS ALU design. The Custom ALU designed in Analog Environment is a 4 bit ALU which is capable of performing eight Arithmetic and eight Logical operations.

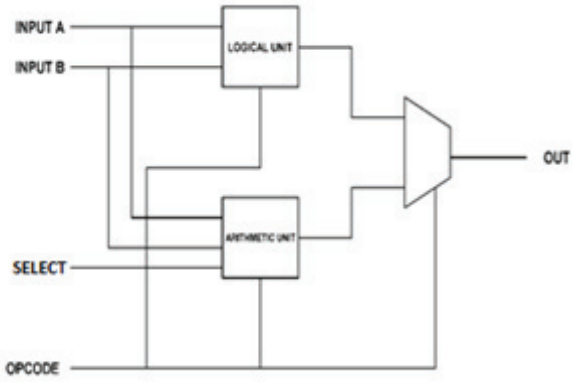

Fig. 1. Logic Block for the possible implementation of ALU

The analog design was carried out in Virtuoso Tool of Cadence using the gpdk045 technology file. The *gpdk* technology files provided by Cadence are generic and are suitable for estimation of *performance metrics* of the device designed.

II. DESIGN OF ARITHMETIC & LOGIC UNIT

The Arithmetic & Logic Unit (ALU) is one of the most important components of any Processor. ALU is the unit that does all the arithmetic and logical operations on the data (input). In this paper, a Custom ALU has been designed in both Analog and Digital Environments. The Custom ALU designed in Analog Environment is a 4 bit ALU which is capable of performing eight Arithmetic and eight Logical operations,

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Verilog HDL was used to simulate and verify the working of the Custom ALU in the Digital Environment. The possible implementation of the ALU is shown figure 2 [1] [2] [7] [8].

The analog design was carried out in Virtuoso Tool of Cadence using the gpdk045 technology file. It has various operation. A 1x16 Demux was designed for the proposed ALU. The select lines of the demux forms the opcode for the ALU proposed. In the figure 3.9, D_3, D_2, D_1 and D_0 are the select lines of the Demultiplexer that form the opcodes.

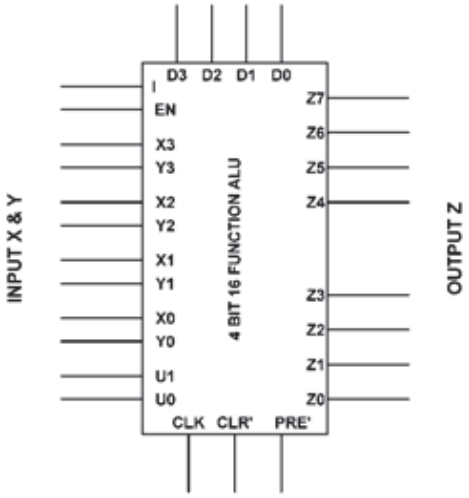

Fig. 2. Logic Block of the proposed ALU

A Demultiplexer latches its input data amongst its output pins according to the pattern of its select lines. The Demux has an EN pin .i.e., enable pin. If the EN pin is 'high' the circuit is active and if EN pin is 'low' then the circuit is inactive. Therefore, the demux is active high. The input, I, is always kept 'high' so that the output ports when latched with the input would also be 'high'. The output port that is latched onto the input will now be able to drive the sub-blocks of the ALU. Therefore, the output pins of the demux acts as the 'enable' pin for the corresponding sub-block of the ALU. If the pattern of the select lines .i.e., D_3, D_2, D_1 and D_0 of the demux, for example, is '0001' then the output O_{14} gets activated while the rest of the output ports are inactivated. Only the sub-block connected to the pin O_{14} turns on [8].

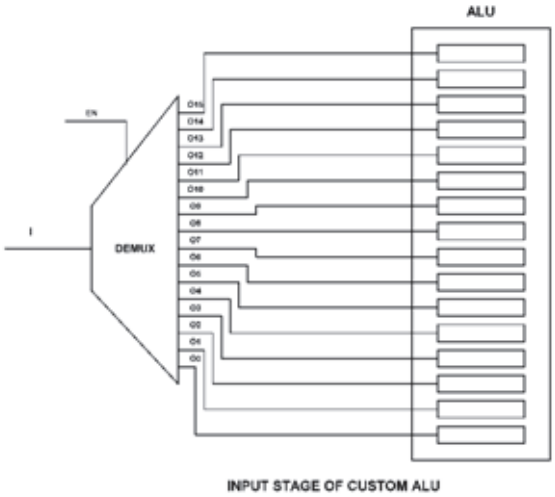

Fig. 3. Input Stage of the proposed ALU

The output pins of the Demux are connected to the individual EN pins of the sub-blocks of the ALU. If the EN pin of the 1x16 Demux is 'low' then the whole ALU is 'turned off'. The inputs are fed directly to the individual sub-blocks. The outputs of all the sub-blocks are then latched to the eight output ports of the ALU, Z_7-Z_0. The various components of the proposed ALU are discussed in the succeeding sections.

A. Demultiplexer

The 1x16 demultiplexer was designed for the ALU so as to reduce the design complexity. The EN pin of this demux is of utmost importance. If the EN pin is 'low' then the whole ALU circuit is turned off. Hence, the operation of the proposed design of the Custom ALU totally depends on the EN pin of the 1x16 demultiplexer. Due to the working principle of the demux only one sub-block is active at a time. The input pin, I, has to be kept 'high' in order to achieve the proper functioning of the ALU.

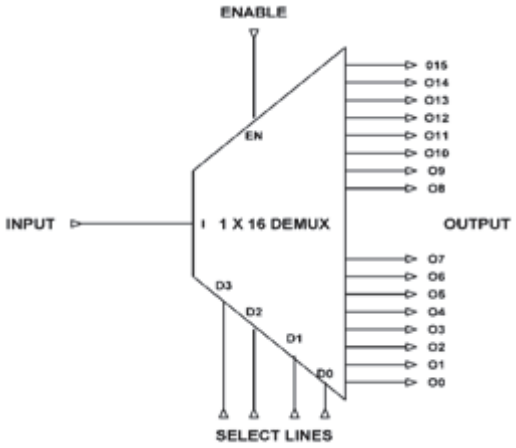

Fig. 4. Logic Block of the 1x16 Demultiplexer

B. Arithmetic Operations

1) Addition

The addition operation was achieved by Full Adders. The Full Adder was designed incorporating *n* 1-bit full adders [8] [10] [11]. These 1-bit full adders were designed by implementing half adders. These half adders were, again, designed incorporating logic gates. It was designed and implemented using Cadence Virtuoso and the transient response was analyzed.

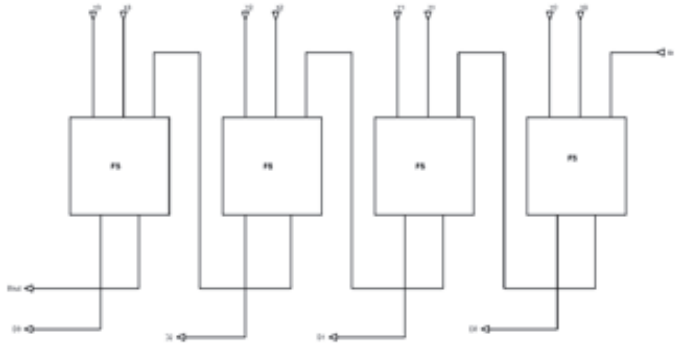

Fig. 5. Schematic of 4-bit Full Adder

2) ubtraction

The subtraction operation was achieved by Full Subtractors. The Full Subtractor was designed incorporating *n* 1-bit full subtractors. These 1-bit full subtractors were designed by implementing half subtractors. These half subtractors were, again, designed incorporating logic gates. It was designed and implemented in Cadence Virtuoso and the transient response was analyzed.

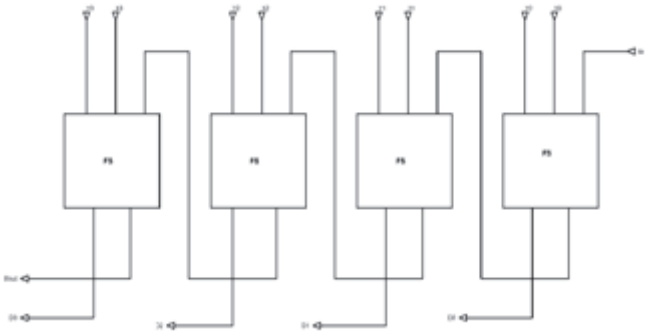

Fig. 6. Schematic of 4-bit Full Subtractor

3) Incrementer

The Incrementer circuit increments the input data by 1. Therefore, the circuit increments the data by 1, .i.e., for example, if the input data be '0101' then the output of the Incrementer would be '0110' [7]. The Incrementer was designed using cascaded half adders. It was designed and implemented Cadence Virtuoso and the transient response was analyzed.

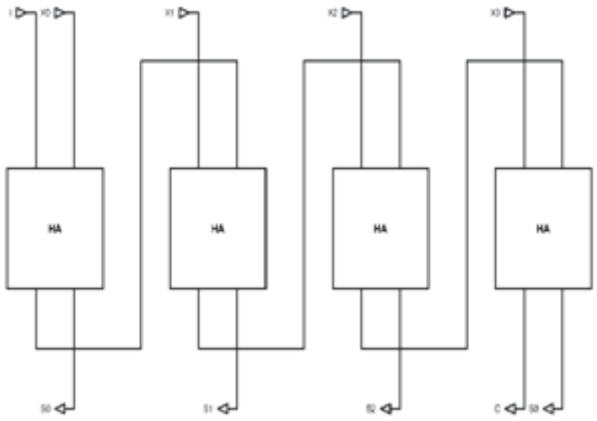

Fig. 7. Schematic of 4-bit Incrementer

4) Decrementer

The Decrementer circuit decrements the input data by 1. Therefore, the circuit decrements the data by 1, .i.e., for example, if the input data be '0110' then the output of the Decrementer would be '0101' [7]. The Decrementer was designed using four cascaded full adders. It was designed and implemented Cadence Virtuoso and the transient response was analyzed.

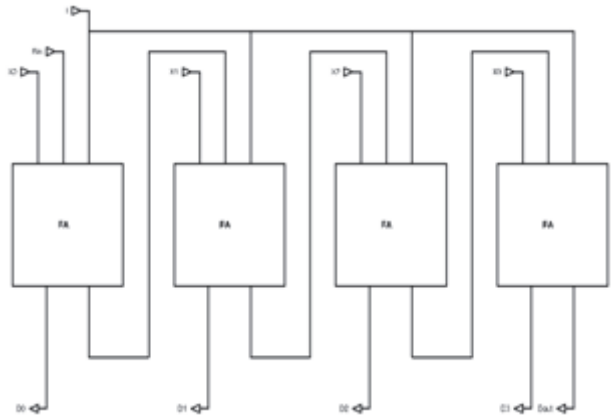

Fig. 8. Schematic of 4-bit Decrementer

5) Multiplication

An Array Multiplier was designed for the multiplication operation in the proposed ALU. The Array Multiplier shifts and add all at once. The Array Multiplier is also called a parallel multiplier. It needs a 'array' of adders. The Array Multiplier has three components – full adders, half adders and AND gates [7]. It was designed and implemented in Cadence Virtuoso and the transient response was analyzed.

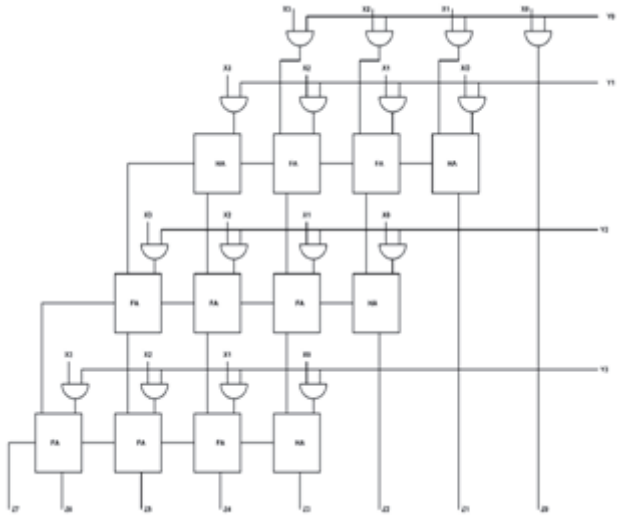

Fig. 9. Schematic of 4-bit Array Multiplier

6) Division

The division operation was achieved by incorporating a Divider. Binary division is the exact opposite of binary multiplication, .i.e., the operation consists of shift and subtract. It comprises both adders and subtractors and mux. The inclusion of both the multiplication and the division operation is the modification made to the Custom ALU [7]. It was designed and implemented in Cadence Virtuoso and the transient response was analyzed.

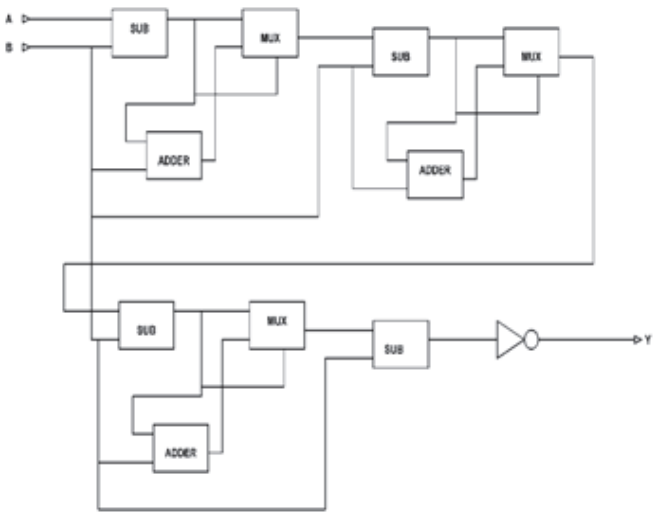

Fig. 10. Schematic of 4-bit Divider

7) Magnitude Comparator

The Magnitude Comparator compares the two inputs and gives the output. The three output ports are G, E and L signify 'greater than', 'equal to' and 'lesser that' respectively. The output port G gets activated when either of the two inputs are greater than the other. The output port E gets activated when both the inputs are equal to one another. Similarly, output port L gets activated when either of the two inputs are lesser than the other. It was designed and implemented in Cadence Virtuoso and the transient response was analyzed.

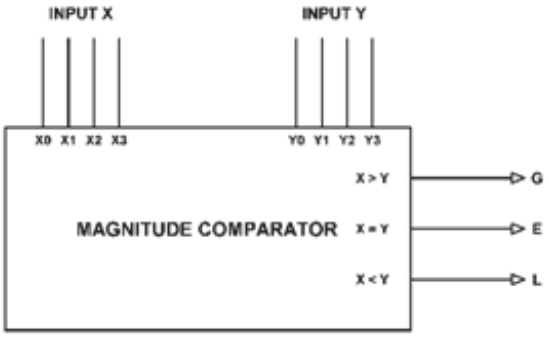

Fig. 11. Schematic of 4-bit Magnitude Comparator

8) Universal Shift Register

A Universal Shift Register is a type of a shift register that perform unidirectional shifting, a bidirectional shifting or a parallel loading. It has three modes of operation – i) parallel loading and transmission, ii) left and right shift or iii) either serial in serial out (SISO) or parallel in parallel out (PIPO) or serial in parallel out (SIPO) or parallel in serial out (PISO). It stores and process data, therefore, it also acts as a memory element. A Universal Shift Register has two components– D Flip-flops and 4x1 Multiplexers [5] [7] [8] [12] [13]. The select lines of the multiplexers decide the mode of operation of the Universal Shift Register according to their pattern. It was designed and implemented in Cadence Virtuoso and the transiet response was analyzed [14].

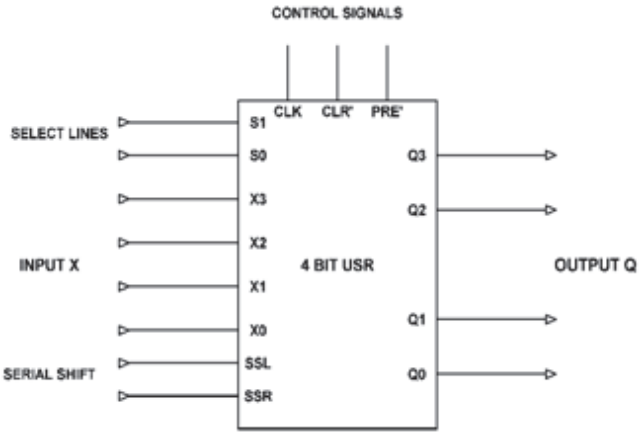

Fig. 12. Logic Block of 4-bit Universal Shift Register

C. Logical Operations

1) NAND Gate

The NAND Gate comprises *n* 1 bit NAND Gates. It gives desired output by processing the two input data. The operation of NAND Gate is that it "turns off" iff both the inputs are "on" and it gets "turned on" in all other cases [8]. It was designed and implemented in Cadence Virtuoso and the transient response was analyzed.

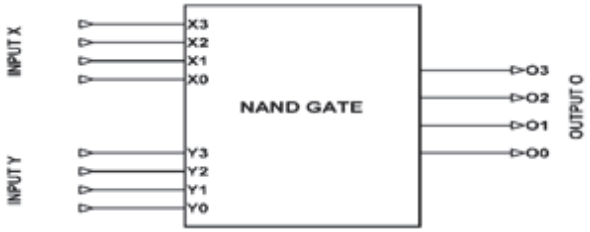

Fig. 13. Logic Block of NAND Gate

2) NOR Gate

The NOR Gate comprises *n* 1 bit NOR Gates. It processes the two inputs and gives the desired output. The operation of the NOR Gate is that it "turns on" iff both the inputs are "on" and it gets "turned off" in all other cases [8]. The NOR Gate was designed and implemented in Cadence Virtuoso and the transient response was analyzed.

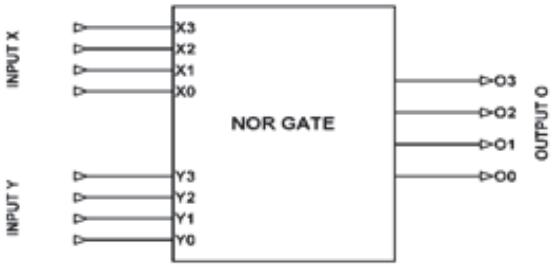

Fig. 14. Logic Block of NOR Gate

3) XNOR Gate

The XNOR Gate comprises *n* 1 bit XNOR Gates. It processes the two inputs and gives the desired output. The operation of the XNOR Gate is that it "turns on" iff both the inputs are "equal" and it gets "turned off" in all other cases [8].

XNOR gates are also known as “coincidence detector” or as “equivalence detector”. It was designed and implemented in Cadence Virtuoso and the transient response was analyzed.

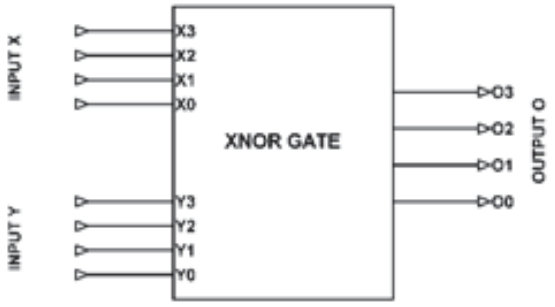

Fig. 15. Logic Block of XNOR Gate

4) NOT Gate

The NOT Gate comprises n inverters each for one of the input bits. The data or input gets “inverted” when applied to the NOT Gate. This action is due to the pull-up network and the pull-down network present in the NOT Gate. If the input is “high” then the pull-down network is “turned on” and it “pulls down” input from “high to low” [8]. If the input is “low” then the pull-up network gets “turned on” and it “pulls up” the input from “low to high”. It was designed and implemented in Cadence Virtuoso and the transient response was analyzed.

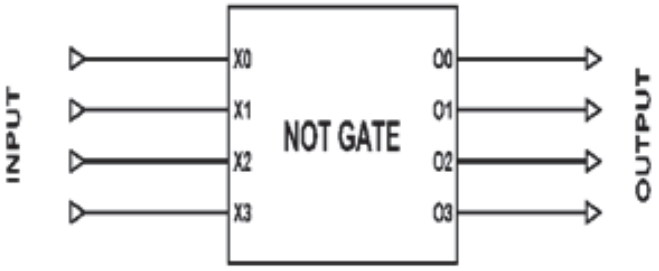

Fig. 16. Logic Block of NOT Gate

The AND Gate, OR Gate, XOR Gate and the Buffer logical operations were not separately designed but were implemented by inverting the outputs of the NAND, NOR, XNOR and NOT Gates, respectively [8] [5]. This was done to reduce the transistor count. All the components .i.e., both arithmetic and logical components were designed, tested and simulated separately. Analysis of these components and the overall circuit .i.e., ALU was done. Operation of the ALU is based on Demux output as shown in Table 1, where D3, D2, D1 and D0 are the select lines of the 1x16 Demux. The performance parameters of all the components of the proposed design was done.

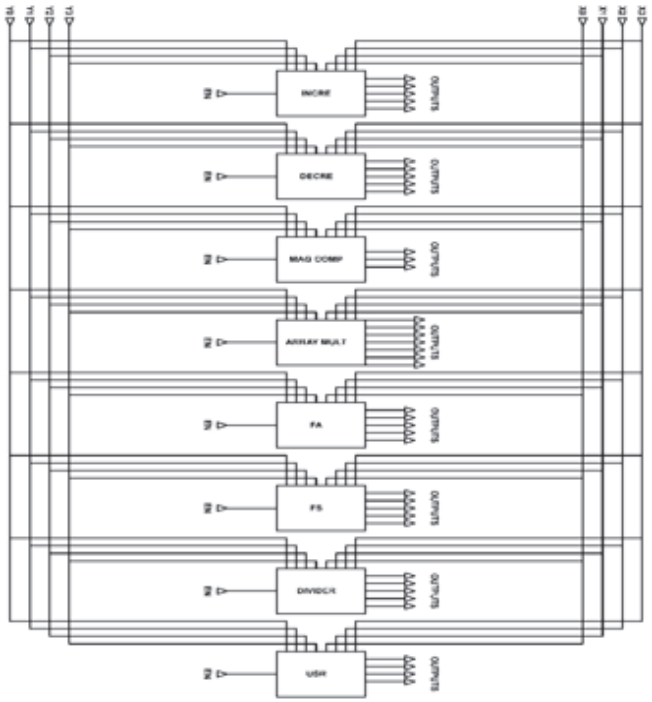

Fig. 17. Logical Representation of the Arithmetic Operations in the Proposed ALU design

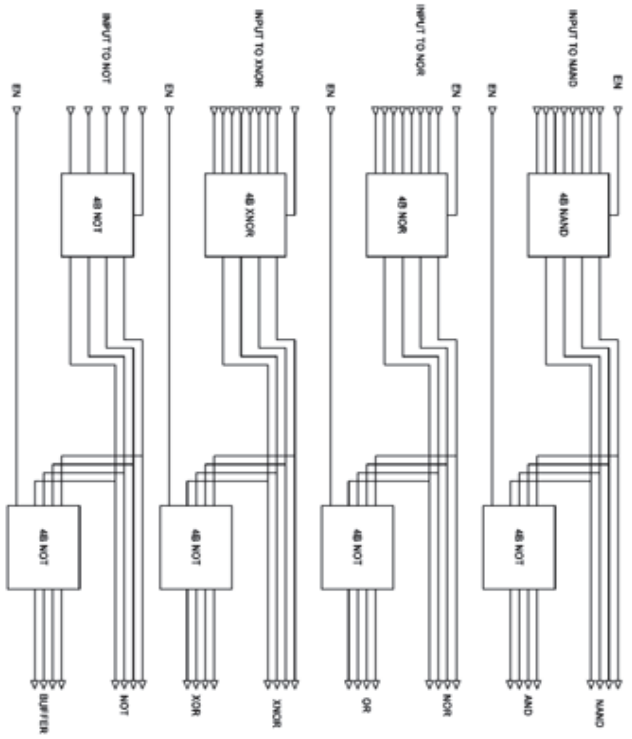

Fig. 18. Logical Representation of the Logical Operations in the Proposed ALU design

TABLE I. OPERATIONS OF THE CUSTOM ALU

D3	D2	D1	D0	OPERATIONS
0	0	0	0	INCREMENTATION
0	0	0	1	DECREMENTATION
0	0	1	0	COMPARISON
0	0	1	1	MULTIPLICATION
0	1	0	0	ADDITION
0	1	0	1	SUBTRACTION
0	1	1	0	DIVISION
0	1	1	1	SHIFTING
1	0	0	0	NAND
1	0	0	1	AND
1	0	1	0	NOR
1	0	1	1	OR
1	1	0	0	XNOR
1	1	0	1	XOR
1	1	1	0	NOT
1	1	1	1	BUFFER

A specific Verilog HDL code was written for the concerned custom ALU [9]. The code was successfully implemented in the Incisive Tool which proved that the code was functional. Thereafter, it was synthesized using the Encounter RTL Compiler Tool of Cadence. The Encounter RTL Compiler Tool helped generate the RTL Schematic of the Custom ALU. The Floorplan of the custom ALU was created using the Encounter Tool. This Floorplan acts as the Layout of the design. The designs made in the digital environment were done in 45nm. The design and the analysis of the performance parameters were done.

III. IMPLEMENTATION

The design was implemented in Cadence and the tools involved are:

- Virtuoso
- Incisive
- Encounter RTL Compiler
- Encounter

The ALU was implemented using the Virtuoso, Incisive, Encounter RTL Compiler and Encounter Tools. The results and analysis was done. This design was carried out in Virtuoso. The circuit was analyzed for different voltage supplies. This was done to draw an analysis of the average power consumption.

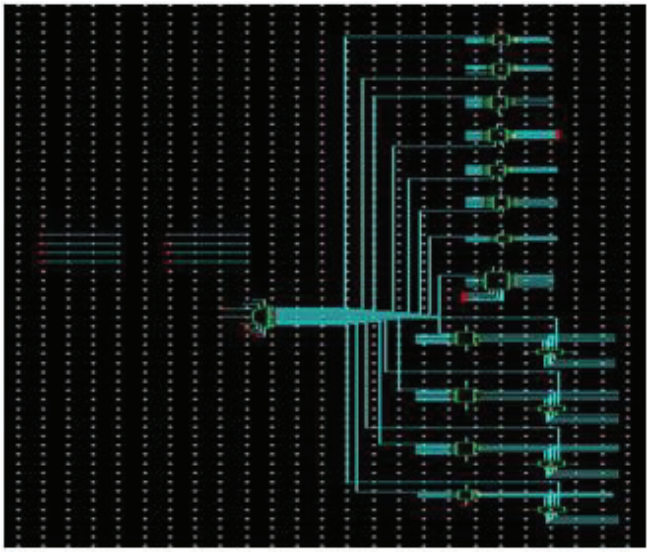

Fig. 19. Schematic of Custom ALU

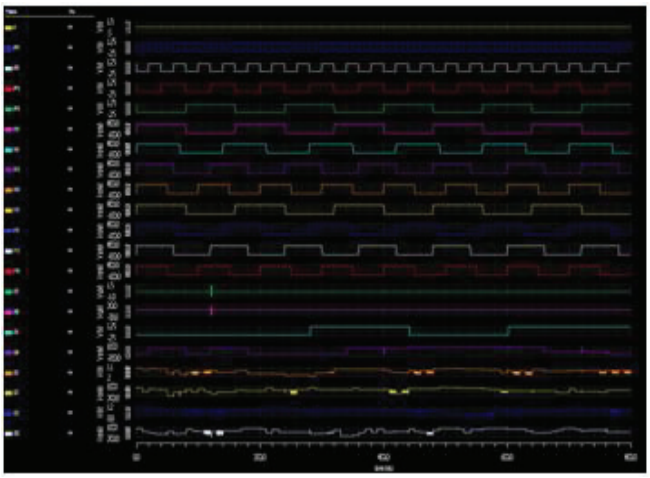

Fig. 20. Transient Response of Custom ALU

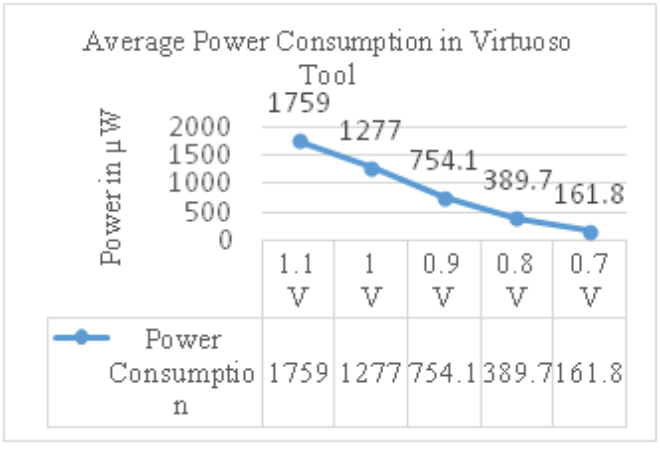

Fig. 21. Average Power Consumption of the Custom ALU

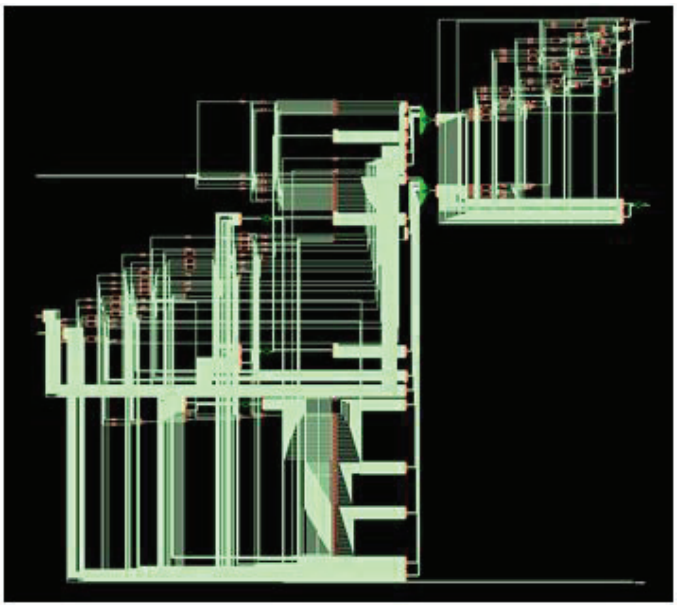

Fig. 22. RTL Schematic of ALU in Encounter RTL Compiler Tool

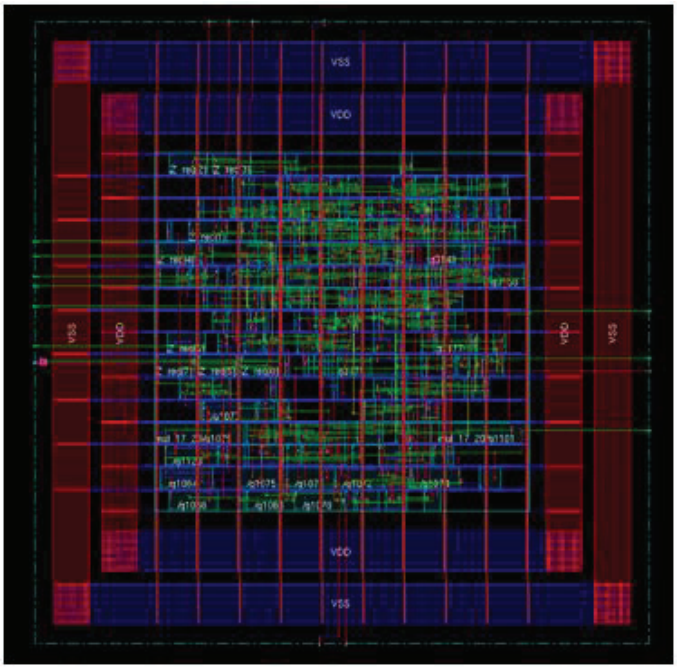

Fig. 23. Floorplan (Layout) of the Custom ALU in Encounter Tool

IV. POWER ESTIMATIONS & CALCULATIONS

The power consumed by the components is the dynamic power. Dynamic power is the power consumed due to switching activities or when the circuit is active.

$$P_{dyn} = C \times V_{DD}^2 \times f \quad (1),$$

Where, P_{dyn} = Dynamic Power consumed,
C = Capacitance,
V_{DD} = Supply voltage and
f = frequency of operation.

The frequency of operation of the given circuit is calculated as:

$$f = \frac{1}{T} \quad (2),$$

Where, T = Time period of the circuit.

The power estimation of the computing block of the Processor .i.e., the ALU is done. The average power consumption of the Custom ALU is the dynamic power. Dynamic power is the power consumed due to switching activities or when the circuit is active.

The time period of the given circuit, T = 160 ns. Therefore, the frequency of operation of the given circuit can be calculated as:

$f = \frac{1}{T}$

.i.e., $f = \frac{1}{160\ ns}$

$\therefore$ f = 6.25 MHz

At V_{DD} = 1.1 V,

Capacitance, C = 232.60 pF and frequency, f = 6.25 MHz,

$\therefore P_{dyn} = 232.60 \times 10^{-12} \times (1.1)^2 \times 6.25 \times 10^6$

$\Rightarrow P_{dyn}$ = 1759 µW

V. RESULTS

The performance metrics of all the individual components were evaluated and analyzed to optimize the design and so was done for the Custom ALU as well

TABLE II. PERFORMANCE PARAMETERS OF THE COMPONENTS OF THE PROPOSED ALU

Components of the Proposed ALU	Average Power Consumed	Average Delay	PDP	EDP
INCREMENTER	8.395 µW	5.608 ns	47.08 fJ	264 yJs
DECREMENTER	1.290 µW	3.450 ns	4.451 fJ	15.35 yJs
MAGNITUDE COMPARATOR	2.409 µW	4.721 ns	11.37 fJ	53.69 yJs
ARRAY MULTIPLIER	103.9 µW	10.958 ns	1138.5 fJ	12476 yJs
FULL ADDER	1.402 µW	2.698 ns	3.78 fJ	10.21 yJs
FULL SUBTRACTOR	2.307 µW	1.471 ns	3.39 fJ	4.99 yJs
BUFFER	1.532 µW	0.00145 ns	0.0022 fJ	0.000003 yJs
UNIVERSAL SHIFT REGISTER	3.984 µW	13.293 ns	52.96 fJ	703.99 yJs
NAND	11.47 µW	0.252 ns	2.9 fJ	0.731 yJs
NOR	11.47 µW	0.01174 ns	0.14 fJ	0.002 yJs
XNOR	11.47 µW	28.12 ns	322.5 fJ	9068.7 yJs
NOT	5.735 µW	0.00298 ns	0.2 fJ	0.0006 yJs
UNIVERSAL SHIFT REGISTER	3.984 µW	13.293 ns	52.96 fJ	703.99 yJs
NAND	11.47 µW	0.252 ns	2.9 fJ	0.731 yJs

TABLE III. PERFORMANCE PARAMETERS OF THE CUSTOM ALU IN CADENCE VIRTUOSO

Power	Delay	PDP	EDP
1.759 mW	230.05 ns	404.66 aJ	93.09 yJs

TABLE IV. COMPARISON OF AVERAGE POWER CONSUMPTION OF DIFFERENT DESIGNS OF ALUS WITH THE CUSTOM ALU

Different Designs in 45nm	Average Power Consumption (mW)
Custom ALU (CMOS)	1.759
4 bit ALU (FINFETS) [1]	8.38
4 bit ALU (CMOS) [2]	4.2045

TABLE V. PERFORMANCE PARAMETERS OF CUSTOM ALU IN ENCOUNTER RTL COMPILER TOOL

Area	Power	Speed
223 μm^2	5.360 µW	957 ps

TABLE VI. COMPARISON TABLE OF THE PROPOSED 4 BIT ALU IN ANALOG AND DIGITAL ENVIRONMENT

Custom ALU	Power	Delay	PDP	EDP
In Analog	1759 µW	230.05 ns	404.66 aJ	93.09 yJs
In Digital	5.360 µW	0.957 ns	5.129 fJ	4.909 yJs

VI. CONCLUSION

The computing block of the processor .i.e., the ALU was designed in both analog environment and digital environment. The testing of the research work and its components were done with 1.1 V. Leakage and dynamic power of the ALU and its components were also analyzed. Therefore, we can conclude from the evaluation and analysis that the proposed Custom ALU so designed proves to be energy efficient and is can be used for real time computing that can be used to design high speed ultra-low power processors [1] [2] [4] [5]. Energy efficiency of the designed ALU has further scope of improvement in the future due to the increasing demand of ultra-low power devices [4]. Voltage Scaling is another aspect to which may be taken up in the future.

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