Design and Development of 4-bit Fault Tolerant ALU in Cadence 90nm PDK

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***Abstract*—Spaceborne and mission-critical systems require computational units that operate reliably under intense radiation and extreme temperature variations. This paper presents the design and implementation of a 4-bit fault-tolerant Arithmetic Logic Unit (ALU) in *Cadence Virtuoso* using the 90 nm GPDK process. The design follows the Radiation Hardening by Design (RHBD) philosophy, employing Single Event Upset (SEU)-immune logic gates based on the $2n + 2$ transistor redundancy principle. Layout-level mitigation techniques, including the LEAP methodology, are applied to further enhance resilience. Functional verification was performed through transient simulations, SEU injection tests, and temperature sweeps from $-240\,^{\circ}\mathrm{C}$ to $+240\,^{\circ}\mathrm{C}$. The proposed ALU recovers from injected SEU faults within X ns (measured value), achieves a static power consumption of $1.11\,\mu\mathrm{W}$ and a dynamic power of $311.76\,\mathrm{nW}$, and maintains stable operation across extreme environmental conditions. These results demonstrate its suitability for deployment in aerospace and other mission-critical embedded systems.**

***Index Terms*—Single Event Upset (SEU), Fault-Tolerant Design, Radiation-Hardened by Design (RHBD), Arithmetic Logic Unit (ALU), SEU-Immune Logic**

I. Introduction

A Single Event Upset (SEU), also referred to as a soft error, occurs when a charged particle strikes the diffusion region of a logic element, potentially flipping a stored bit. Such events pose significant reliability concerns for digital circuits, particularly in aerospace systems and electronic equipment operating in high-radiation environments. The ongoing trend toward device miniaturization and increased circuit integration in complementary metal-oxide-semiconductor (CMOS) technologies has further amplified this vulnerability. As feature sizes shrink, the critical charge required to induce a bit-flip decreases, thereby increasing susceptibility to both natural and artificial radiation sources. In response to this growing challenge, substantial research efforts have been directed toward the development of inherently SEU-immune or fault-tolerant digital architectures that enhance the robustness of modern electronic systems [1]–[3].

Several techniques exist to mitigate the effects of SEUs. The European Cooperation for Space Standardization (ECSS) classifies radiation hardening approaches according to the abstraction level in application design, broadly dividing them into Radiation Hardening by Process (RHBP) and Radiation Hardening by Design (RHBD). This work focuses on RHBD. These techniques can be implemented at various design levels, from the physical layout to the system level. At the physical layout level, the goal is to minimize radiation-induced charge collection through device and interconnect-level optimization. At the system level, the emphasis shifts toward error masking, fault tolerance, and prevention of system-wide failures, ensuring reliable operation even in high-radiation environments [4].

This paper proposes a 4-bit ALU designed and developed in the cadence virtuoso software in the 90nm pdk(GPDK90), adhering to the RHBD philosophy incorporating fault-tolerant design principles at the logic and system levels. The ALU is constructed entirely using SEU-immune universal gates, forming the foundation for all arithmetic and logical functions. Furthermore, layout-level mitigation strategies were employed to reduce the impact of SEUs. The proposed ALU supports eight distinct operations, as outlined in Table I.

TABLE I
ALU Operation Encoding

Operation	Opcode
Adder	000
Subtractor	001
AND	010
OR	011
XOR	100
Shift Logic Left	101
Shift Logic Right	110
XNOR	111

II. Design Methodology

An SEU-immune logic gate employs the $2n + 2$ transistor configuration to incorporate the additional redundancy required for upset mitigation, thereby ensuring stable output operation even in radiation-prone environments [5]. This design principle was consistently applied in the development of all logic gates within the proposed ALU architecture. The design process began with the implementation of a 1-bit ALU, which was then cascaded to form a ALU capable of processing 4-bit operands. This modular approach preserved fault tolerance at the gate level while enabling scalable arithmetic and logic operations suitable for high-reliability applications.

A. INVERTER Design

According to the $2n+2$ principle, an SEU-immune inverter (where n = 1), uses four transistors instead of the conventional

two-transistor design. As shown in "Fig. 1", the strong transistors (PM1, NM1) are sized to have approximately six times the drive strength of the weak transistors (PM2, NM2). When the input is at logic high, NM1 and NM2 actively pull the output low, quickly restoring a correct LOW level in the event of a transient upset. Conversely, when the input is logic low, NM1 and NM2 — connected in a complementary configuration — pull the output to logic 'HIGH', ensuring a correct logic level high is maintained. This topology guarantees that:

- Strong transistors enforce the intended output level against SEU-induced disturbances.
- Weak transistors provide continuous feedback holding, but their limited drive prevents contention during legitimate input transitions.

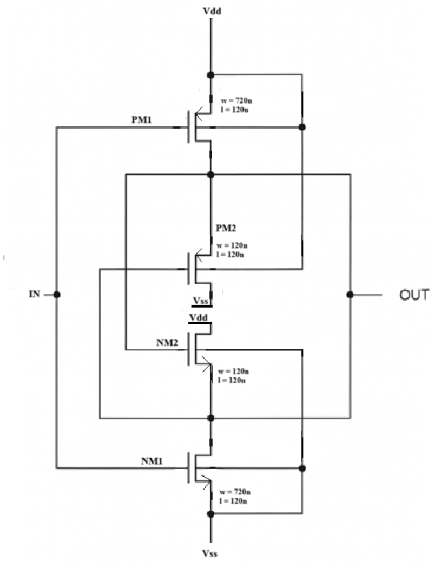

Fig. 1. Schematic of the SEU-immune inverter designed using the $2n + 2$ transistor redundancy principle

By combining these functional roles, the inverter is capable of masking transient faults and sustaining correct logical states despite particle-induced charge collection events.

B. NAND & NOR design

The SEU-immune NAND and NOR gates are implemented using six transistors instead of the conventional four. In both designs, strong devices serve as the primary switching elements, while weak devices provide feedback and facilitate state recovery to mitigate radiation-induced upsets.

For the NAND gate, as shown in "Fig. 2", the strong pull-down network ensures that when all inputs are high, the output is driven low with enough strength to override any transient disturbances. The weak pull-up network maintains the output at logic HIGH whenever one or more inputs are low,supporting stability during upsets.

In the NOR gate, the strong pull-up network to drive the output high when all inputs are low, and the weak pull-down network preserves a logic LOW whenever any input is

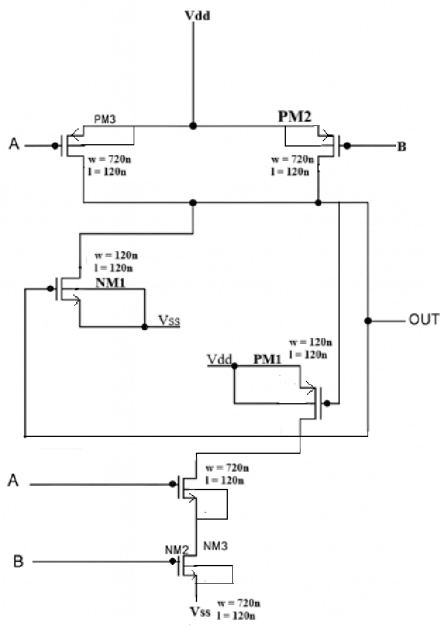

Fig. 2. Schematic of the SEU-immune NAND gate using the $2n+2$ transistor design principle.

high. In both designs, the feedback configuration helps isolate upset nodes and prevents glitches from propagating to later stages.Additionally, the carefully ratioed device strengths ensure rapid restoration of the correct logic level. This approach provides both upset recovery and glitch suppression ensuring reliable operation in radiation-prone environments. All the other gates i.e- AND,OR,XOR and XNOR were constructed using these basic gates INVERTER,NAND and NOR. The standar circuits for all of these gates were employed enabling us to use the fault tolerant basic gates without altering the existing designs of these gates.

C. Adder & Subtractor design

The SEU-immune full adder and full subtractor were developed by integrating the previously designed SEU-immune logic gates into the conventional logic architectures of these arithmetic circuits. The full adder follows the standard configuration of two half adders and an OR gate, with all components implemented using hardened logic gates to ensure radiation tolerance.

For the full subtractor, we adopted an optimized design derived using the Particle Swarm Optimization (PSO) technique described in [6]. This approach replaces the XOR gates with XNOR gates, effectively reducing the overall transistor count by one by eliminating an inverter compared to the conventional implementation as shown in 3

Both circuits follow the standard Boolean logic equations for sum/difference and carry/borrow operations. This approach allows both the adder and subtractor to operate reliably in high-radiation environments, as each gate inherently provides upset recovery and glitch suppression.

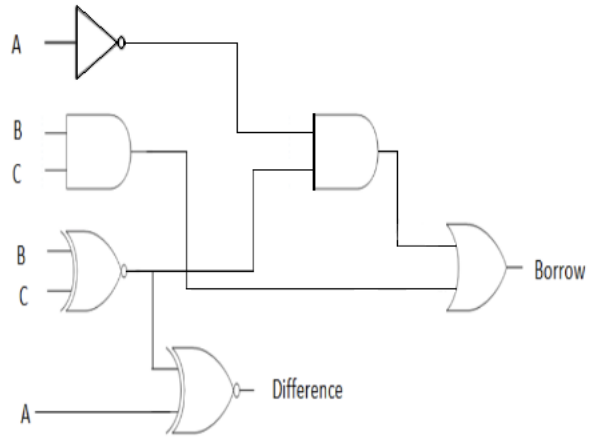

Fig. 3. Full subtractor circuit optimised using the Particle Swarm Optimization (PSO) approach. The design replaces conventional XOR gates with XNOR gates, reducing transistor count while preserving SEU immunity.

By preserving the original logical structure while replacing all constituent gates with radiation-hardened equivalents, the resulting circuits achieve fault tolerance without altering their functional behavior, making them suitable for drop-in replacements for standard designs.

D. 8x1 MULTIPLEXER design

The 8×1 multiplexer(MUX) was designed entirely using SEU-immune logic gates to ensure fault tolerance. To construct this circuit, we first extended our previously developed SEU-immune 2-input AND and 2-input OR gates into their 4-input versions by cascading multiple stages. These, along with the SEU-immune inverter, were then used to implement the conventional 8×1 multiplexer architecture. The design consists of three inverters (to generate complemented select lines), eight 4-input NAND gates (to compute the selection logic for each input), and two 4-input OR gate and a final 2-input OR gate to produce the final output by combining all selected paths. Each logic block within the MUX is constructed from SEU-immune gate variants to ensure glitch suppression and enable upset recovery across all levels of the circuit. This approach preserves the full functionality of a traditional 8×1 MUX while providing enhanced resilience to single event upsets, making it suitable for operation in high-radiation environments.

E. 1-BIT ALU

Using all previously constructed SEU-immune modules, we developed a 1-bit ALU capable of performing all specified operations on two 1-bit operands, excluding shift operations, which are addressed separately in the following section.

The 1-bit ALU integrates SEU-immune implementations of the full adder, full subtractor, AND, OR, XOR, and XNOR gates, whose outputs serve as inputs to an 8×1 multiplexer, also built from hardened logic gates. This modular architecture ensures that each operation within the ALU benefits from the glitch suppression and upset recovery characteristics inherent in the underlying gate structures.The 1-BIT ALU contains a a 2x1 mux which is a component for the barrel shifter although, in the standalone 1-BIT ALU shift functionality is not implemented the reasons for which will be discussed in the following section. Designing the 1-bit ALU as a standalone unit also enables easy scalability, allowing the construction of multi-bit-width ALUs through cascading, which will be discussed in the subsequent sections.

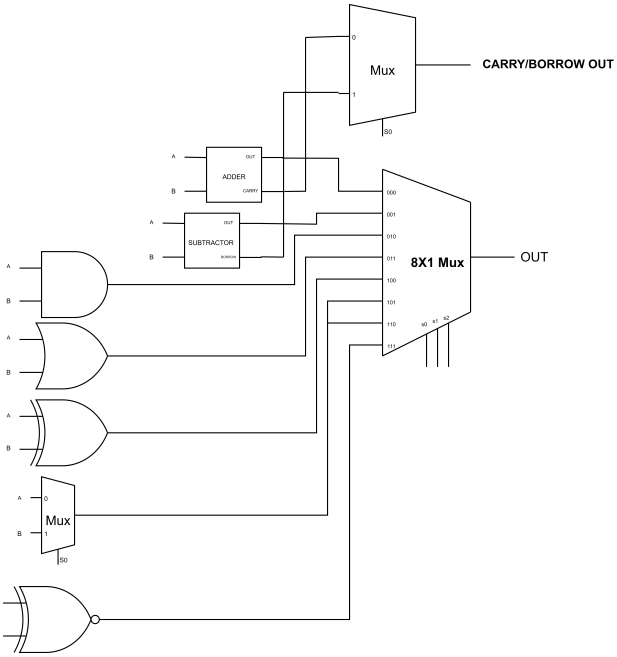

Fig. 4. Schematic of the 1-bit ALU constructed entirely from SEU-immune gates. The design integrates hardened arithmetic and logic blocks whose outputs are selected via an SEU-immune 8×1 multiplexer.

F. 4-BIT ALU & BARREL SHIFTER design

In our 4-bit ALU, the previously developed 1-bit ALUs were connected in parallel, with their inputs and outputs appropriately interfaced to form a multi-bit configuration. To enable the Shift Left Logical (SLL) and Shift Right Logical (SRL) operations, we integrated the necessary 2×1 multiplexers, forming the core of the barrel shifter as shown in 5. This approach not only facilitates efficient shift operations but also ensures the ALU's fault tolerance is maintained across all components.

A barrel shifter was employed in place of traditional shift register-based architectures due to the inherent performance limitations and radiation sensitivity of conventional shift registers. Shift registers, which operate sequentially, require multiple clock cycles to complete multi-bit shifts, introducing latency. In contrast, the barrel shifter performs shifts in a single combinational step, significantly improving speed and efficiency, while also reducing susceptibility to Single Event Upsets (SEUs). Conventional shift registers depend on latches or flip-flops, which are particularly vulnerable to SEUs due to their bistable nature [7], [8]. By utilizing the barrel shifter, we

eliminate this vulnerability and enhance the overall radiation tolerance of the ALU.

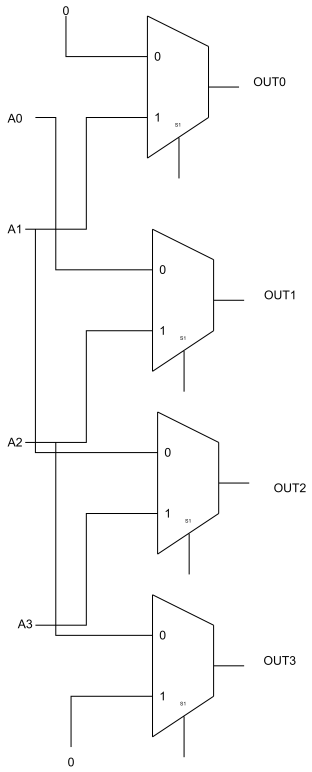

Fig. 5. Barrel shifter schematic implemented using SEU-immune 2×1 multiplexers. This combinational architecture enables single-cycle shift operations while avoiding SEU-sensitive sequential elements.

The barrel shifter is constructed using 2×1 multiplexers. Each 2×1 MUX handles a single-bit shift and feeds one of the input lines of the 8×1 multiplexer in the 1-bit ALU module. When the 1-bit ALU is cascaded to form the 4-bit ALU, the four 2×1 MUXes are interconnected, forming a 4-bit barrel shifter. This design not only optimizes performance but also ensures that shift operations are both fault-tolerant and performance-optimized, making the ALU highly reliable in radiation-prone environments.

G. LAYOUT

During the physical layout phase of our SEU-immune ALU, we adopted several Radiation Hardening by Design (RHBD) techniques to enhance fault tolerance at the device level. One of the key strategies employed was inspired by the LEAP (Layout Design through Error-Aware Transistor Positioning) methodology, which focuses on optimizing the spatial arrangement of transistors to mitigate the effects of radiation-induced disturbances [9]. The LEAP approach works by strategically positioning sensitive transistors in such a way that the charge collection from a single particle strike is distributed across multiple transistors, thus reducing the likelihood of multiple node upsets (MNUs) [4]. By carefully placing critical transistors and separating vulnerable diffusion regions, we minimized

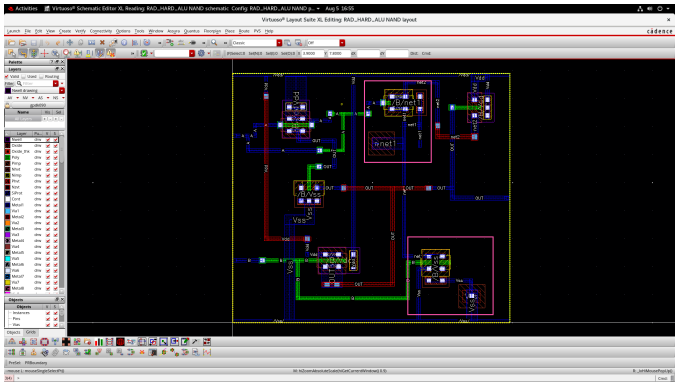

Fig. 6. Layout of the SEU-immune NAND gate employing the LEAP methodology. Increased diffusion spacing and strategic transistor placement minimise charge sharing and multi-node upsets.

charge-sharing as shown in 6. In addition to this we also spaced the Transistors further away from each other than typical standards as well as using redundant structures to make it more resilient.

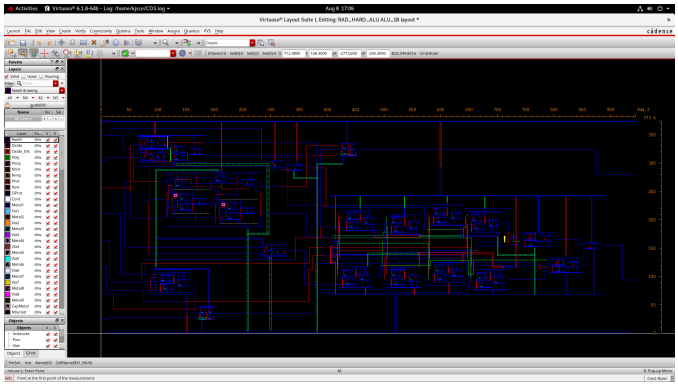

Fig. 7. Layout of the SEU-immune 1-bit ALU. Device placement follows RHBD guidelines, incorporating redundant structures and increased transistor separation.

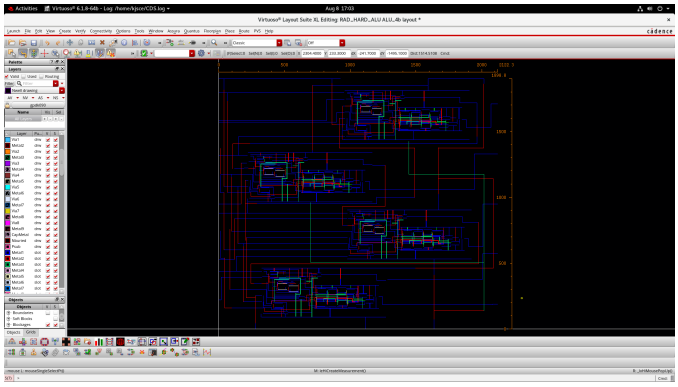

Fig. 8. Layout of the SEU-immune 4-bit ALU, obtained by cascading four hardened 1-bit ALU units and integrating a barrel shifter. Layout maintains LEAP-based spacing rules throughout.

III. Simulation & Results

A. Transient analysis

For the transient analysis of the ALU, we provided inputs to the select lines (S0, S1, S2) such that they cycled through all the required opcodes (see Table I). The simulation was conducted to observe the ALU's behavior and verify the correctness of the outputs. As shown in the results, for the operands 1001 and 1110, the outputs (OUT0, OUT1, OUT2, OUT3) and the carry/borrow output match the truth table outputs, confirming that the ALU is correctly performing the intended operations.

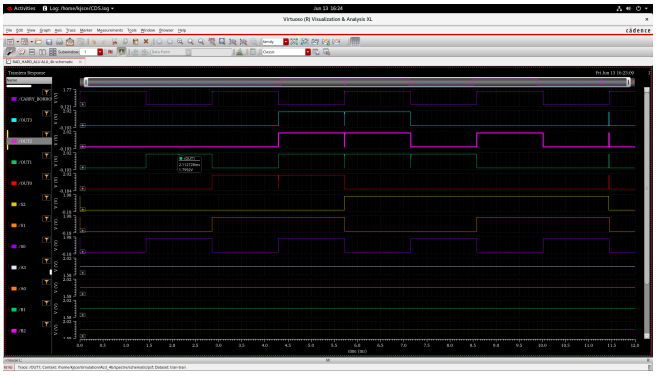

Fig. 9. 4-bit ALU transient analysis

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B. SEU injection analysis

To evaluate the radiation tolerance of our ALU, we conducted Single Event Upset (SEU) injection tests as described in the methodology from the J. Canaris paper [5]. In these tests, current sources were used to simulate the effect of charged particles impacting the outputs and other critical terminals of the ALU modules. For example, in the inverter, we applied a toggling input signal and at the 250 µs mark, a simulated charge particle strike was injected into the output node. This charge injection was repeated every 100 µs to simulate continuous radiation exposure.

As shown in the Fig. 10, following the simulated particle strike, the output initially deviates from its correct logic level. However, the fault is quickly recovered by the SEU-immune design, with the output returning to the correct logic level before an incorrect state can propagate to subsequent stages. This demonstrates that the SEU recovery mechanism in the ALU is effective, ensuring that the circuit remains fault-tolerant even under radiation-induced disturbances.

C. Temperature analysis

Temperature analysis was conducted by applying fixed operands and select line inputs. Specifically, the select lines were set to 000, corresponding to the ADD function. For this operation, the expected output is logic low on all outputs and logic high on the carry line. The temperature was swept over a range from $-240^{\circ}\mathrm{C}$ to $+240^{\circ}\mathrm{C}$ in $1^{\circ}\mathrm{C}$ increments to evaluate the ALU's behavior under extreme temperature conditions.

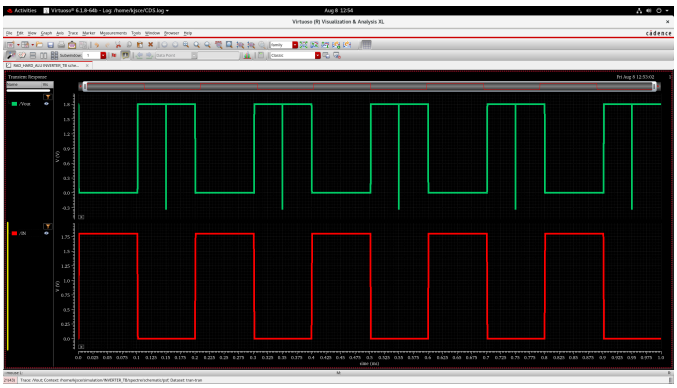

Fig. 10. SEU INJECTION analysis

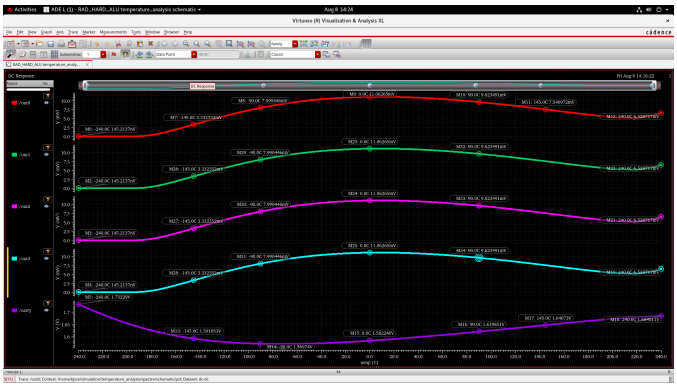

Fig. 11. Temperature analysis from $-240^{\circ}\mathrm{C}$ to $+240^{\circ}\mathrm{C}$

This specific temperature range was chosen because various real-life space missions require components to survive and operate across this temperature spectrum. According to Mojarradi et al. [10], such temperature resilience is essential for electro-mechanical systems used in space applications, where components are often exposed to both extreme cold and heat.

As seen in the results (shown in the image), the maximum variation in the OUT0, OUT1, OUT2, OUT3 lines ranges from 145.2137 nV to 11.06 mV to 6.3287mv ,over the range of temperatures. Which is negligible and well within the acceptable margin. This small variation will not result in an error since the logic low voltage threshold (the highest voltage level considered a logic low) is 1V, significantly higher than the observed maximum voltage of 11.06 mV.

The carry signal shows a variation between 1.73V and 1.58V to 1.68V, which is also considered negligible. Even at the lowest value of 1.58V, the voltage is still well above the logic low threshold of 1V, ensuring reliable operation of the carry signal throughout the temperature sweep.

These results confirm that the ALU operates within the required specifications even under extreme temperature conditions, demonstrating the robustness and reliability of the design in radiation-hardened and temperature-variable environments.

D. Power Analysis

The power characteristics of the proposed radiation-hardened 4-bit ALU were evaluated through static and dynamic power measurements. All measurements were obtained by monitoring the supply current at the V_{DD} terminal under controlled input conditions.

Static Power was determined to quantify leakage current when the circuit is powered but idle. A DC sweep was applied to operand input A from 0 V to 1.8 V while holding the select lines S and operand B constant. The supply voltage was fixed at 1.8 V, and the maximum leakage current recorded was:

$$I_{\text{leak}} = 617.63\,\text{nA}$$

The static power was then calculated as:

$$P_{\text{static}} = V_{\text{DD}} \times I_{\text{leak}} = 1.8 \times 617.63\,\text{nA} = \mathbf{1.11}\,\boldsymbol{\mu}\mathbf{W}$$

This low leakage is attributed to the SEU-immune universal gate design, which minimizes parasitic leakage paths.

Dynamic Power was analyzed using a 10 ms transient simulation where the select lines $S[2:0]$ were toggled with a pulse input. Operand inputs $A = 1111$ and $B = 0000$ were chosen to induce maximum switching activity, and each output was loaded with 10 F. The average current drawn during switching was:

$$I_{\text{avg}} = 173.2\,\text{nA}$$

The average dynamic power was calculated as:

$$P_{\text{dynamic}} = 1.8 \times 173.2\,\text{nA} = \mathbf{311.76\,nW}$$

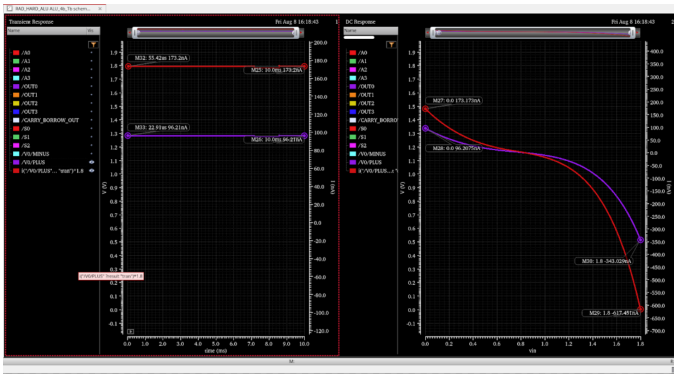

Fig. 12. VDD supply current waveform during dynamic power analysis. Idle and switching regions are marked, with average and peak current values indicated for power calculation.

These results confirm that the proposed ALU offers both low static and dynamic power consumption while maintaining fault-tolerant operation, making it suitable for radiation-hardened, power-sensitive applications such as spaceborne and mission-critical embedded systems.

Conclusion and Future Work

This work presents the design and development of a 4-bit fault-tolerant Arithmetic Logic Unit (ALU) implemented using SEU-immune logic gates in the Cadence 90 nm GPDK environment. Leveraging the $2n+2$ transistor redundancy principle and layout-level hardening techniques such as the LEAP methodology, the proposed ALU demonstrates high resilience against radiation-induced faults. Functional validation through transient simulations, SEU injection tests, temperature sweeps, and power analysis confirmed the correctness and reliability of the design under critical operating conditions. The inclusion of a combinational barrel shifter enhances performance while eliminating reliance on SEU-sensitive sequential elements, resulting in a power-efficient and radiation-hardened architecture suitable for aerospace and mission-critical embedded systems.

Future enhancements to further strengthen system-level fault tolerance include the integration of Triple Modular Redundancy (TMR), wherein three identical ALU units operate in parallel with a majority voter to mask transient and permanent faults. Extending the current design to support wider operand widths (e.g., 8-bit or 16-bit) and more complex operations will increase its applicability in high-reliability computing environments. Additionally, integration with radiation-hardened memory and control logic, coupled with automated layout generation incorporating built-in redundancy and spacing constraints, will be instrumental in scaling and accelerating the development of complete SEU-immune processing systems.

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