Single Event Transient on Combinational Logic: An Introduction and their Mitigation

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***Abstract*— Single event transients pose a major threat to the reliability of modern VLSI designs. Improving the robustness of combinational logic is challenging due to its complexity, masking effects, and signal dependence. This paper presents the mechanisms and concepts of SET generation, modeling, masking, and propagation in combinational logic. It also discusses design parameters and their impact on circuit robustness. An overview of automated design strategies for radiation hardening by design and their advantages and disadvantages is provided, covering gate sizing, gate duplication, gate remapping, load increase, layout spacing, and charge sharing techniques.**

***Index Terms*— Single-Event Transient; Radiation Hardening by Design (RHBD); Electronic Design Automation (EDA); Combinational Logic.**

I. Introduction

Radiation-induced effects pose a threat to the reliability of modern CMOS technologies. The downsizing of transistors, associated with smaller supply voltages and higher operating frequencies, has resulted in Single Event Transients (SETs) becoming a major reliability concern for nano-CMOS transistors [1–3]. High-energy particles such as protons, neutrons, or heavy ions can strike a chip and produce a discharge of electric current. This current pulse is referred to as SET when observed in combinational logic. When this pulse reaches a memory element and changes its value, it results in an error called a Single Event Upset (SEU). Both effects, the transient and memory upset, are known in the literature as *soft errors* (SE) because they are not destructive effects.

Several techniques for evaluating the robustness of a digital circuit to SET and SEU are presented in the literature. Simulation-based approaches allow the early assessment in the design flow of a complex circuit and the adoption of mitigation strategies to achieve the application constraints. For instance, TCAD (Technology Computer-Aided Design) simulations can be performed to simulate the interactions of particles with the materials that compose electronic devices. Although achieving the highest level of precision, this is not a scalable approach and usually adopted to study fundamental mechanisms in basic structures such as p-n junctions or single transistors. An alternative with lower computational cost is the TCAD mixed-mode approach, in which only the strike transistor is modelled as a TCAD device, while the remaining devices are simulated using SPICE modeling. In this case, multiple transistors can be studied allowing the simulation of logic gates and small circuit blocks. To increase scalability, a current-based model in SPICE could simulate the particle impact along with the device, eliminating TCAD simulations and allowing a higher number of transistors in combinational or sequential circuits. Even more scalable are analytical methods where the electrical simulations can be omitted altogether. As a rule of thumb, TCAD simulations are the most precise technique possible, and precision decreases as we move to SPICE and analytical methods.

This paper focuses on works that are run-time friendly and allow evaluation of the design under test (DUT) and implementation of design changes to improve the robustness of the circuit to SET in combinational logic. Section II. introduces the basic SET mechanism; Section III. lists design parameters related to circuit robustness to SET; Section IV. summarizes the SET mechanisms and design parameters in a survey of works that evaluates and mitigates the propagation of SETs in combinational logic; Section V. concludes the paper.

II. SET Mechanisms in Combinational Logic

A. SET Generation and Propagation

When a high-energy particle passes through a semiconductor device, two ionization mechanisms can occur: direct ionization and indirect ionization [4]. The energetic particle may collide with electrons inside the device, creating electron-hole pairs and thus generating charge along the particle's path. The direct generation of charge can be generated by heavy ions (particles with an atomic number greater than or equal to two) and is called direct ionization. Lighter particles cannot be ignored, however; protons and neutrons can initiate multiple nuclear reactions, and the recoils of such reactions can ionize matter and induce an SET. This charge produced by secondary particles from nuclear reactions is known as indirect ionization [4]. Initially, the direct ionization of low-energy protons was not a concern for radiation effects on electronics, however, with the reduced critical charge to upset a circuit in advanced technologies, this mechanism also pose a threat to the reliability of electronic systems and should not be overlooked [5, 6].

In a CMOS (complementary metal-oxide-semiconductor), the logic gate always has transistors in the "off" state. Transistors in this state are susceptible to the accumulation of charge generated by an energetic particle defined by three mechanisms: drift (inside the depletion layer), funneling (deformation of the depletion layer), and diffusion (outside the depletion layer) [4]. Fig. 1 illustrates the interaction of these mechanisms with the p-n junction of an NMOS transistor. The amount of charge collected affects the current pulse generated and is technology and particle dependent. A represen-

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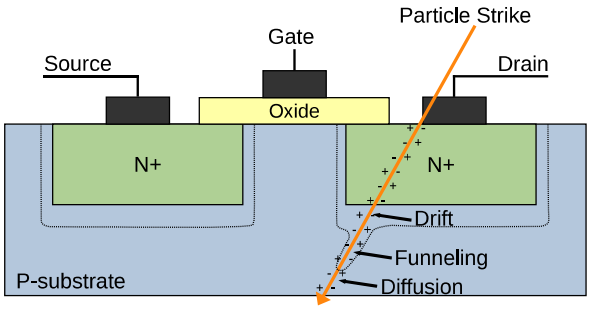

Fig. 1: Particle strike path across a NMOS transistor, charge collection happens in three stages.

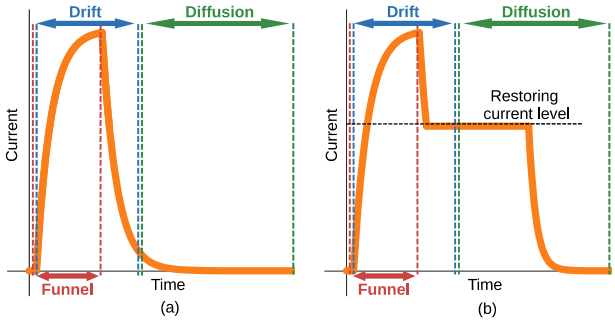

Fig. 2: Particle strike current model, low-LET follows the double exponential curve while high-LET has a plateau region.

tation of a typical (low linear energy transfer, LET) SET current pulse is shown in Fig. 2 (a), and for higher LET strikes a plateau region occurs in Fig. 2 (b) [7]. The plateau occurs due to a tug-of-war effect between the logic planes inside the logic gate. Using an inverter gate as an example, when charge is collected from the NMOS plane, the PMOS restoring current limits the pulse amplitude. Higher LET particles create a plateau with longer duration instead of higher amplitudes. An illustration of this effect can be seen in Fig. 3.

An example of the mechanisms explained above in an inverter gate is shown in Fig. 4. The input of the inverter gate is set to "1", where the expected value at the output is "0". However, when a charge is collected at the drain of the PMOS transistor, it generates a voltage pulse that temporarily sets the output value to "1". Since the NMOS transistor is active, it acts as a restoring element for the expected output value and shortens the pulse duration (width). This voltage pulse is the definition of a Single Event Transient (SET) effect.

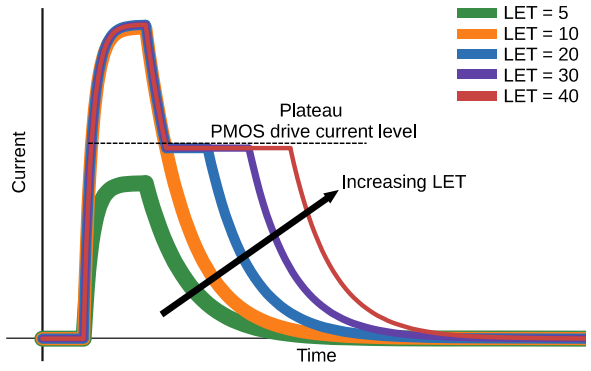

Fig. 3 Increasing LET current behavior. (adapted from [7])

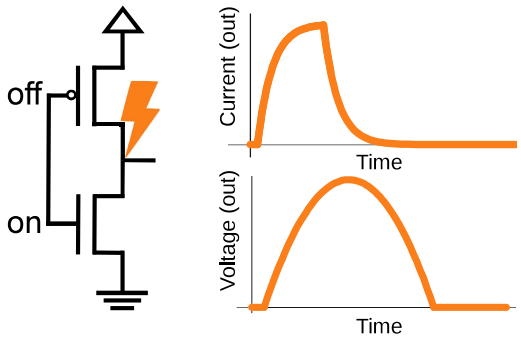

Fig. 4: A particle strike at the drain of the inverter gate creates a burst of current, changing output voltage value.

B. *SET Electrical Modeling*

A SET generates a current pulse that flows through the struck area. Circuit-level modeling usually consists of implementing pulsed current sources to account for charge deposition mechanisms. A well-known modeling strategy is based on a double exponential current source proposed by Messenger [8]. This method accurately reproduces current shapes for low LET situations, although it does not accurately model the plateau region observed in TCAD simulations for higher values for LET. This drawback is more significant for deeply-scaled technologies where, due to the smaller node-capacitances, the amount of charge deposited to generate a SET is smaller.

Black et al. [9] proposed a modeling technique based on two double-exponential current sources connected in parallel, one responsible for the burst phase of the SET-induced pulse and the other generating the plateau region observed in high LET situations. This technique can be used to accurately characterize the electrical effects of particle impacts even at high values of deposited charge. However, several electrical simulations may be required to determine the correct current source parameters.

A bias-dependent model based on voltage-controlled current sources was proposed by Kauppila et al. [7]. This model consists of a capacitor (Cs) charged by an independent current source with a double exponential form. Two additional voltage controlled current sources (dependent on the Cs voltage) are implemented to accurately represent the plateau effect. This SET modeling methodology was implemented using the Verilog-AMS behavioral modeling language and shows high agreement with TCAD mixed mode simulations. However, its replication can be complex since the methodology does not depend only on device-level simulations. If the reader is interested in a more in-depth review of the modeling of SET, the authors refer the reader to the works of Pasupathy et al. [10] and Andjelkovic et al. [11].

C. *Logical Masking*

The SET voltage pulse illustrated in Fig. 4 can occur in both logical values, the pulse can go from "0" to "1" or from "1" to "0", this depends on the input value and the transistor that collects the charge generated by the particle. When a SET propagates through the combinational logic and this value reaches a memory element that stores this unintended value, a SEU is configured. Fig. 5 shows an SEU due to

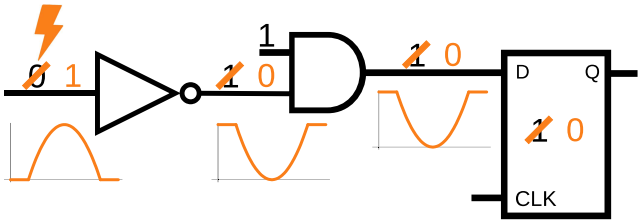

Fig. 5: SET pulse reaches the memory element and its value is stored configuring a SEU.

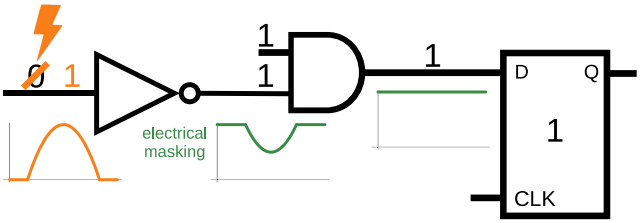

Fig. 7: SET pulse does not reach the memory element due to signal attenuation, electrical masking occurs.

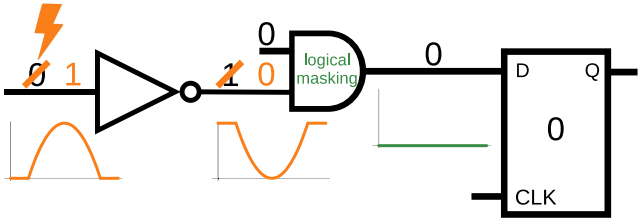

Fig. 6: SET pulse does not reach the memory element due to signal dependency not allowing the pulse propagation across the combinational logic, logical masking occurs.

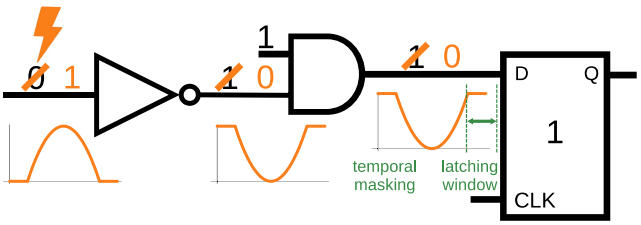

Fig. 8: SET pulse reaches the memory element but outside the latching window, temporal masking occurs.

a charge collection at the input of a INV gate. This charge momentarily switched the INV gate and generated a voltage pulse that propagated through the AND gate and was stored by the flip-flop. However, this SET only caused an SEU due to a set of specific conditions in the combinational logic, namely the logic state, the electrical properties, and the circuit clock. These conditions define the three masking mechanisms: logical, electrical, and temporal.

Logical masking occurs in combinational logic whenever the SET cannot pass through a logic gate due to the function dependence on another input signal. Fig. 6 illustrates the occurrence of logical masking in the AND gate. When charge collected at a previous logic level, this transient pulse changes the input at the INV from "1" to "0". This pulse switches the INV gate and generates an inverted pulse that reaches the AND gate. However, since the other input of the AND gate is "0", the SET cannot propagate further, resulting in logic masking.

D. Electrical Masking

As a pulse propagates through the combinational logic, its shape (slope, amplitude, and duration) is affected by the electrical properties and capacitances of the logic gates. On its propagation path, the SET magnitude or duration may decrease so that it is no longer sufficient to reach the next logic stage; this effect is called electrical masking. An example of this effect is shown in Fig. 7. A SET, which originated in an earlier logic stage, reaches the inverter gate. When the logic gate attempts to pass this pulse, it does not have enough drive strength to fully propagate the signal. The resulting pulse at the AND gate input is not strong enough to switch the gate value, causing electrical masking.

E. Temporal Masking

The circuit clock is also relevant for masking effects. A SET at the input of the memory element requires sufficient magnitude during the latching window to storage the unwanted value. Pulses outside the latching window are not stored, this effect is called temporal masking. Fig. 8 demonstrates this situation: when the SET passes through the combinational logic, it arrives outside the latching window, so the stored bit is not changed, configuring temporal masking.

F. Charge Sharing

When a particle strikes the circuit, it generates charge in its vicinity. Because of the proximity of the layout, this charge can be shared between adjacent logic gate nodes [12]. This phenomenon is called charge sharing and can affect the circuit in different ways. If the collected charge is just above the threshold required for a single node to generate a SET, it can be electrically masked as the charge is collected from multiple nodes (and thus below the threshold for each node). On the other hand, if the particle strike generates a high enough amount of charge, it can cause multiple SETs (Single Event Multiple Transient, SEMT). As the technology nodes progress, the density of the circuit design increases and by consequence the circuit nodes are physically closer together, which amplifies the effect of charge sharing. Section IV. E. will further discuss the impact of charge sharing and SEMT at the layout level.

G. Pulse Broadening

Ferlet-Cavrois et al. [13] conducted a study of the SET width distribution in several inverter chains and found that the SET pulse width can increase as it propagates across logic levels. This propagation-induced pulse broadening (PIBD) depends on the supply voltage, the drive strength of the logic path, and the load. Fig. 9 shows a visualization (not to scale) of pulse broadening, an initial SET pulse of 1 ns increases to 3 ns after two inverter stages. In their experiments with SOI devices, Ferlet-Cavrois et al. [13] found that a 200 ps SET can reach widths exceeding 1 ns.

H. Reconvergent Fan-outs

Reconvergent paths are another situation that can occur frequently in combinational logic. Fig. 10 shows an example

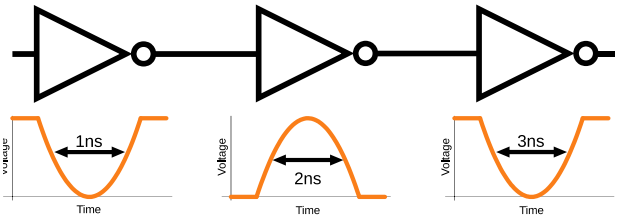

Fig. 9: Pulse broadening effect, the pulse width may increase while propagating across logic levels.

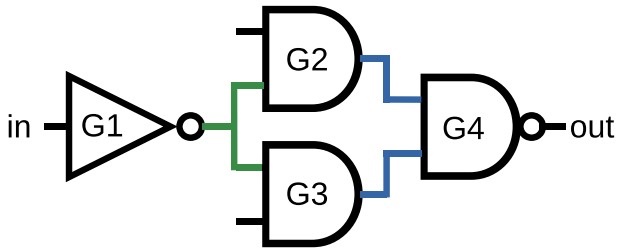

Fig. 10: Reconvergent path, the inputs at the "G4" are not independent due to their origin from the "G1" logic gate.

of a reconvergent fan-out (RFON) at logic gate "G4"; both inputs are not independent due to dependence on logic gate "G1". Blocks of combinational logic containing RFONs are susceptible to converting a single error from SET to multiple errors (SEMT). RFONs can also combine two SET and cause attenuation or logically mask the pulse depending on their polarity.

I. SET Sensitivity Metrics

The amount of charge collected by the device during the strike is an practical model metric since it can be modeled as the integral overtime of a current pulse. The critical charge of a combinational logic element is often used in the literature to measure its sensitivity and accounts for the minimum collected charge required to generate a SET.

The amount of energy lost by the particle along its strike path, referred to as linear energy transfer (LET), is another well-known sensitivity parameter. The LET is expressed as MeV-/cm but is often normalized by dividing its value by the density of the struck material, then it is usually presented as MeV-cm2/mg.

For radiation tests, the single event effects sensitivity of a DUT is the cross-section, expressed as the ratio of the number of events to the total particle fluence (integration over time of the number of ions passing through a unit area perpendicular to the particle, in one second). Particle fluence is defined by the environment the circuit is situated, devices in outer space are susceptible to a higher particle density, while devices at sea level are protected by the earth's magnetosphere and thus have a smaller particle density.

J. SET Simulation Tools

Several tools have been proposed to estimate the SEE sensitivity of digital circuits, generally proprietary and using Monte Carlo simulations. Since each tool has its own methodology, only a list of the most popular tools is given for brevity. MUSCA SEP^3 [14], developed at French Aerospace

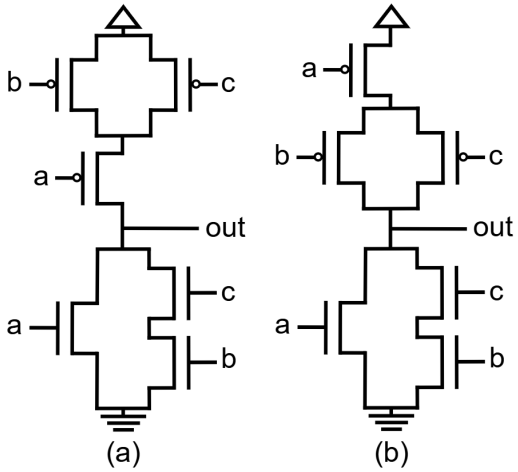

Fig. 11: AOI21 transistor network with two reordering possibilities, (a) the far topology, (b) the close topology.

Laboratory (ONERA), provides SEE cross section or SEE rate of digital circuits. MC-Oracle [15] (currently being updated to PredicSEE), developed at the University of Montpellier, uses critical charge deposition to extract multiple error cross sections and soft error rates. MRED [16], developed at Vanderbilt University, is the core engine for CRÈME- MC [17] and provides simulations for both transient and damaging effects. TIARA [18], developed at STMicroelectronics, provides the SE rate and multiple cell upsets for planar bulk, FD-SOI and FinFET technologies. G4SEE [19] is an open-source tool provided by CERN that is still under development and provides energy depositions and SE rates.

III. Design Parameters Related to SET Sensitivity

When designing circuits based using the standard cell methodology, several optimizations are performed to obtain the best possible circuit. During logic synthesis, one possible optimization is to replace selected logic gates with equivalent alternatives to achieve an improvement in power consumption or a reduction in circuit delay. To perform this type of optimization, tools use a set of parameters related to the electrical properties of the circuit, if the tool is able to find another equivalent circuit block that improves the desired metric. This section presents design parameters that affect the sensitivity to SET in combinational logic.

A. Logic Gate Structure

In complex logic gates, it is possible to use the transistor rearrangement technique during design. This design decision can improve the complex gate electrical characteristics or reduce the impact of process variability [20]. Fig. 11 illustrates two transistor networks for an AOI21 logic function, (a) shows the AOI21 gate with the PMOS "a" transistor *far* from the output, while (b) rearranges the transistors and places the transistor *close* to the output. Zimpeck et al. [20] claim that by using the *close* topology, higher SET robustness is achieved with smaller pulse widths and a SET cross section.

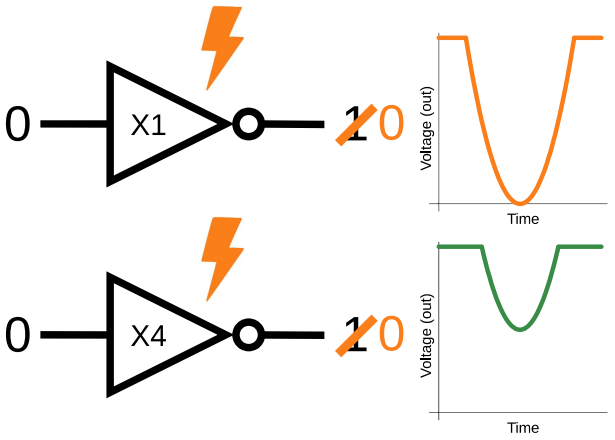

Fig. 12 Gate sizing attenuates the particle strike impact.

B. *Logic Gate Sizing*

Gate sizing is a well-known technique for increasing the drive strength of a logic gate, thereby reducing propagation delay at the expense of increased area. This is done by increasing the channel width of the logic gate's transistors, allowing a higher current to pass. As mentioned earlier, electrical masking plays an important role in the robustness of a logic gate and is directly related to the drive strength of the logic gate.

An alternative to increase the robustness of CMOS logic gates is to resize the gates, especially upsizing. Increasing the drive strength will also increase the restoring current. If we assume two equal particle strikes in a minimum sized inverter and an X4 inverter (four times the minimum size), as shown in Fig. 12, the generated SET is attenuated by the higher restoring current of the X4 inverter. This higher recovery current increases the critical charge of the logic gate and thus increases its robustness.

Although gate sizing is efficient to handle low-charge inducing events, it can achieve worst robustness for SET filtering and high-charge inducing events. Because a larger logic gate has a lower propagation delay, it can propagate SET from earlier logic levels where smaller logic (and thus lower signal propagation capability) would be electrically attenuated. In addition, increasing the size of the transistor also increases the sensitive area of the logic gate, making it more likely to be hit by a particle. For high LET particles, the restoring current may not be sufficient to attenuate the SET, so the increased likelihood of a particle strike plays a greater role than the benefits of a stronger restoring current. Transistor sizing requires fine-tuning to be effective as a design technique for increasing the robustness of logic gates / combinational circuit robustness, as it is directly related to the circuit environment.

C. *Logic Gate Layout*

The drain area of a transistor is directly related to the robustness of the logic gate to SET. One way to reduce the drain area while maintaining the same electrical characteristics is to use transistor folding. In this technique, the layout of a transistor is changed by dividing it into two transistors with lower heights. An example of transistor folding is shown in Fig. 13, (a) a layout of an arbitrary transistor of sizing 2W without transistor folding technique, and (b) an equivalent transistor with a layout using folding to reduce the height of the cell (note that the height is half of the unfolded design). Aguiar et al. [21] present a study of the effects of transistor folding in three logic gates (INV, NAND, NOR). Although, these folded logic gates have shown improved SET rate, the authors claim that, similarly to other circuit techniques, its efficiency is input dependent and should be carefully assessed for the specific application radiation environment and operation conditions.

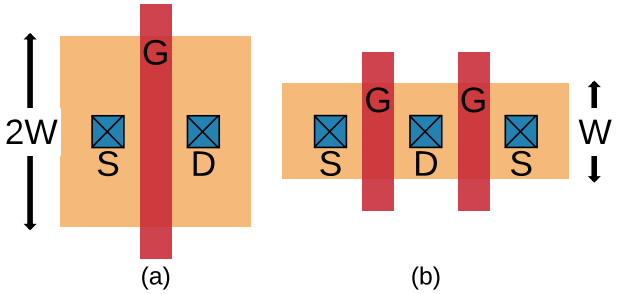

Fig. 13: Transistor folding, (a) transistor layout without folding, (b) transistor layout with folding.

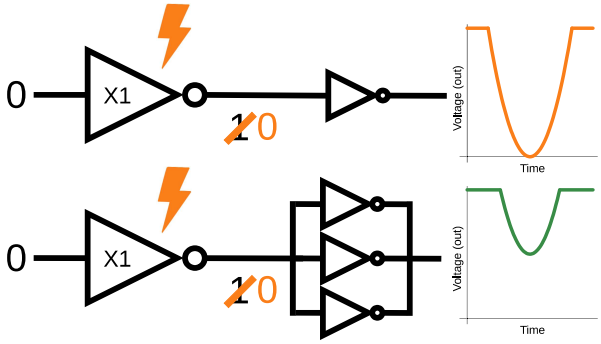

Fig. 14 Increasing the gate load attenuates the particle strike impact.

D. *Fan-out Capacitance*

Particle strikes are current-inducing events with varying amounts of charge. Since this event is a limited charge inducing event, increasing the output capacitance of the logic gate is a desired feature to reduce the susceptibility of a combinational block to SET. One way to increase output capacitance is by node sharing. Fig. 14 illustrates a particle strike at the output of the inverter, in (a) the output is a single inverter and in (b) we have three inverters. Since the particle strike is identical, the induced current is the same in both environments, but the voltage pulse is smaller in the (b) environment due to the higher node capacitance (data are illustrative and not to scale).

IV. SET Mitigation Strategies in Combinational Logic

Improving the robustness of combinational logic to SET during the design stage can result in significant extra area, delay, and power overhead. The most well-known technique is hardware replication in conjunction with a majority voter.

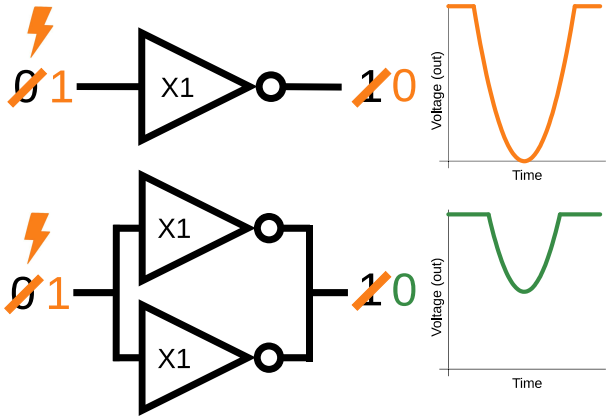

Fig. 15 Gate duplication improves the SET pulse filtering capability.

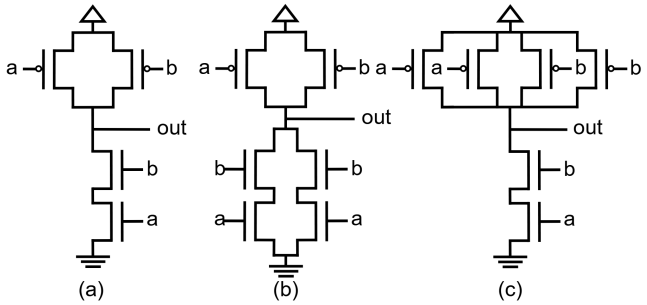

Fig. 16: Selective gate redundancy in the NAND gate, (a) baseline NAND arrangement, (b) redundancy in the pull-down, (c) redundancy in the pull-up.

One application of this method is Triple Modular Redundancy (TMR) [22], which the combinational logic is replicated three times and associated with a Majority Voter responsible for determining the correct value. This approach achieves high resilience to SE at a large area and energy cost (more than three times), which may not be consistent with application constraints.

In this paper, we present a collection of recent works that improve combinational logic in the design phase. This improvement in robustness can be achieved by exploiting masking mechanisms or by reducing the generation of SET.

A. *SET Mitigation by Gate Sizing*

Raji et al. [23] uses a cone-oriented logic gate sizing to reduce the SER of Very Large-Scale Integration (VLSI) designs. Their methodology consists of three steps: netlist partitioning, subcircuit optimization, and main circuit modification. The cone-based partitioning is performed by backward propagation from the primary outputs (PO) to the primary inputs (PI) (first proposed in [24]). When extracting the subcircuits, their SER is computed by summing the SER of all included gates. Each gate SER is defined by its probability of generating a SET (using the [25] model) and its probability of forwarding a SET to a memory element (considering logical, electrical, and temporal masking), using the SEATLA trapezoidal glitch propagation model proposed by [26]. As each subcircuit SER is defined, it re-sizes its gates to improve the robustness of the main circuit. Improvements in subcircuits are made only if the main design SER is improved, and local improvements are discarded. Their framework has been applied to ISCAS'85 and EPFL [27] benchmarks using 45nm NANGATE technology and claims an average SER improvement (31%) at the expense of area (17%), while being practical for VLSI designs (run time on the order of minutes).

B. *SET Mitigation by Gate Duplication*

An alternative but similar method for improving the selected logic gate against radiation-induced effects is gate duplication (upsizing). Fig. 15 shows an example of gate duplication for an inverter. (a) shows a single inverter gate, while (b) doubles this inverter by sharing both input and output. The main advantage of gate duplication is to exploit the electrical masking effect, which improves the SET filtering capability of the duplicated logic gates. However, similar to gate upsizing, it has the disadvantage of increasing the area of the circuit (an even larger area than upsizing), thus increasing the probability of particle strikes.

Nieuwland et al. [28] evaluate the contribution of each logic gate to the soft error rate (SER), taking into account both logical and electrical masking effects, and the overall sensitivity of the combinational logic is defined by the sum of the contributions of all logic gates. Their tool is capable of handling reconvergent paths, and the authors claim that 60% SER robustness is achieved for the ISCAS'85 benchmark with an area overhead of 20%.

Similar to gate duplication, Sheikh et al. [29] uses selective transistor redundancy to increase the robustness of targeted gates. Fig. 16 illustrates this technique in a NAND gate, (a) shows the baseline NAND transistor arrangement, (b) duplicates the NMOS transistors to increase pull-up plane fault tolerance, while (c) duplicates the PMOS transistor to increase pull-down tolerance. In their work, they propose to duplicate all possible combinations of transistors, from a single transistor to all transistors, depending on the desired signal and overall tolerance. Based on experiments with the LGSynth'91 benchmark, a transistor selection scheme based on signal probability can achieve significant improvements in fault tolerance in an acceptable run time and with a low area overhead. Transistor redundancy can also be implemented using standard cells as proposed in [30] and named as Transistor Stacking (TS). In this technique, a 4-input gate can be used as a 2-input gate to achieve transistor redundancy and also an increased nodal capacitance. Although the transistor stacking has shown lower efficiency in the mean SET cross section when compared to gate sizing, the technique is highly input dependent and pin swapping can be used to achieve an improved robustness based on the signal probability [31, 32].

C. *SET Mitigation by Gate Remapping*

Through logic synthesis optimizations, Limbrick et al. [33] replaced vulnerable standard cells from the cell library with the goal of reducing SET pulse width and drain area (sensitive regions). In their experiments with 90-nm technology nodes, it was found that using four NAND gates instead of one XOR2 gate can reduce SET pulse width, sensitive area, and block delay with area overhead. Experiments in large benchmarks confirmed the gains achieved at the logic gate level.

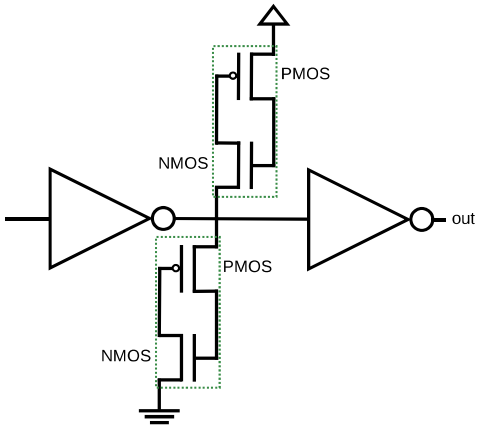

Fig. 17: Decoupling cells attached to a gate output, working as an additional capacitive load.

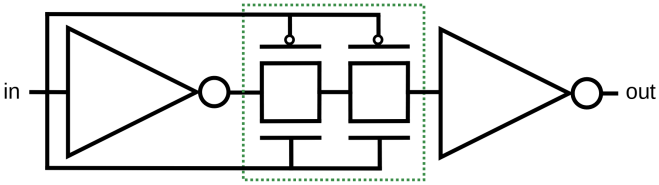

Fig. 18 Transmission gates works as a low-pass filter for SET pulses.

Rezaei et al. [34] proposed a zero-delay overhead technique based on signal probabilities and gate sizing. By abusing logic masking effects, their work identifies the vulnerability of logic gates, including internal nodes, and rearranges them accordingly to reduce the error propagation probability. Applying both sizing and input reordering to the ISCAS'89 benchmark with a 45-nm technology node increased SER mitigation by an average of 20% without delay penalty and 1% area penalty.

D. SET Mitigation by Load Increase

When a particle hits a logic gate, its effect could be simplified as an injection of charge onto the node it hits. For a logic gate, as the output capacitance increases, so does the amount of charge required by the particle strike to produce a SET. Andjelkovic et al. [35] proposes the use of decoupling cells to improve SET robustness. Fig. 17 illustrates the proposed technique. When a connection of two inverters is defined as critical for a design, inserting a pair of decoupling cells can significantly improve the robustness of SET by working as a SET filter.

Similar to increasing the capacitance at the output of logic gates, Sayil et al. [36] uses two transmission gates as low-pass filters, as shown in Fig. 18. This technique allows SETs to be filtered with a variable pulse width that depends on the voltage applied to the transmission gate. Since transmission gates have inherently slow propagation speeds, in this work the gate size is chosen to keep the delay overheads tolerable, at a significant additional cost in area and power.

E. SET Mitigation in Layout

Because of charge sharing, a single particle hit can affect multiple sensitive regions. In their work, Georgakidis et al. [37] uses the distance between logic gate during the layout phase to reduce SEMT. As stated in their work, spacing between logic gates is effective for SEMT mitigation, but results in significant additional area costs. The proposed alternative is to use TMR in critical nodes, which provides better SET filtering. It is important to note that majority voters are also prone to error. The use of hardened voters plays an important role in the robustness of the circuit SET fault [39].

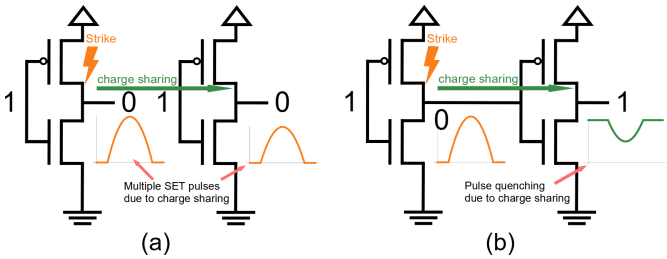

Fig. 19: Charge sharing effects, (a) creation of multiple transient pulses, (b) pulse attenuation (quenching). (adapted from [38])

As an alternative to spacing the logic gates in the layout, Yankang et al. [38] places selected logic gates together to abuse the charge sharing effect and create a pulse quenching effect. Fig. 19 shows the difference between two charge sharing effects. (a) Shows two non-connected inverters where the charge sharing can cause multiple transient effects, while (b) shows two connected inverters where the charge sharing effect attenuates the SET. By reversing the cell orientation, their method achieves a reduction in pulse width at no additional cost.

Table I lists the SET mitigation strategies discussed in this survey and summarizes the strengths and weaknesses of each technique.

V. Conclusions

In this paper, a review of SET strategies for mitigating errors in combinational logic is presented. A qualitative comparison of each strategy is also presented. It is important to note that a quantitative comparison of each technique is challenging due to the non-standardization of SET modeling, signal propagation, and different levels of abstraction. Although several works are discussed in this review, they are generally limited to their niche strategy, i.e., a gate sizing work does not evaluate the use of multiple approaches, such as gate remapping or attenuation of SET during the layout phase. The authors believe that developing a framework that allows the use of multiple mitigation strategies during the design of VLSI circuits is key to balancing the weaknesses of each technique.

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Table I. Overview of SET mitigation strategies.

SET Mitigation Strategy	Strong Points	Weak Points
Hardware redundancy [22]	Major improvements on SET mitigation	Major area and power overhead, majority voter is susceptible to errors
Gate sizing [23]	Increased logic gate critical charge	Large area overheads, not effective in SET filtering, environment dependent
Gate duplication [28, 29]	Increased logic gate critical charge, stronger SET filtering (compared to sizing)	Larger area overheads (compared to sizing), environment dependent
Gate remapping [33, 34]	Significant improvement in critical nodes	Requires circuit redesign
Load increase [35, 36]	Strong SET filtering	Area, power and delay overhead
Layout spacing [37]	Significant improvement in Single Event Multiple Transient (SEMT)	Area overhead, increased wirelength may cause significant delay overheads
Charge sharing (quenching) [38]	Negligible design overhead	Requires layout analysis for gate placement (run time / scalability)

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