O/C

Thapar University, Patiala
Computer Science and Engineering Department
Mid-Semester Examination

B.E. (COE, CML, SEM, CAG)	**UCS608 (Parallel and Distributed Computing)**
September 23, 2017	Saturday, 1:00 pm to 3:00 pm
Time- 2 Hours , Maximum Marks - 25	Name of Faculty: Miss Navneet Kaleka

Note:
- *All questions are compulsory.*
- *Answer all parts of the question at same place only.*
- *Assume any necessary assumption if needed. Quote examples too.*

<table>
<tr><th>Q.No.</th><th>Questions</th><th>Marks</th></tr>
<tr><td>1.</td><td>Consider the execution of an object code with 200,000 instructions on a 40-MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles(CPI) needed for each instruction type are given below based on the result of a program trace experiment:
<table>
<tr><th>Instruction Type</th><th>CPI</th><th>Instruction mix</th></tr>
<tr><td>Arithmetic and Logic</td><td>1</td><td>60%</td></tr>
<tr><td>Load/store with cache hit</td><td>2</td><td>18%</td></tr>
<tr><td>Branch</td><td>3</td><td>12%</td></tr>
<tr><td>Memory reference with cache miss</td><td>4</td><td>10%</td></tr>
</table>
(a) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results.
(b) Calculate the corresponding MIPS rate based on the CPI obtained in part (a).</td><td>(2,2)</td></tr>
<tr><td>2.</td><td>(a) Consider a 16- node hypercube network. Based on the E-cube routing algorithm show how to route a message from node (0110) to node (1001). All intermediate nodes must be identified on the routing path.</td><td>(3)</td></tr>
<tr><td>3.</td><td>Consider the execution of a program of 15,000 instructions by a linear pipeline processor with a clock rate of 20 Mhz. Assume the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out- of-sequence executions are ignored.
(a) Calculate the speed up factor in using this pipeline to execute the program as compared with the use of an equivalent nonpipelined processor with an equal amount of flow through delay.
(b) What are the efficiency and throughput of this pipelined processor?</td><td>(2,2)</td></tr>
<tr><td>4.</td><td>Differentiate the following terms:
i. UMA and NUMA
ii. SIMD and MIMD
iii. Implicit Parallelism and Explicit Parallelism</td><td>(2,2,2)</td></tr>
<tr><td>5.</td><td>Suppose through experimentation, it was verified that 70% of execution time was spent on parallelizable execution. What is the maximum speedup</td><td>(2)</td></tr>
</table>

	that can be achieved with 6 processors?	
6.	(a) Explain the cache – coherence problem and the reasons why it occurs in multiprocessing environment. (b) Name and explain one protocol to cope with multicache inconsistency problem in network connected systems.	(2,2)
7.	Is the routing latency in wormhole routing dependent on the distance (number of nodes traversed)? Give reasons for your answer.	(2)