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College. Roll. No : 191725.
Level : Bachelors.
Programme : Software
Semester : 2nd
Subject : Logic circuit.
Signature of Examiner : Date : July 4 2021.

Q.N.1.

Ans. As per question, the last 4 digit of my college roll number (191725) is 1725.

i. Conversion into binary form,

| | | |
|---|---|---|
| 2 | 1725 | |
| 2 | 862 | 1 |
| 2 | 431 | 0 |
| 2 | 215 | 1 |
| 2 | 107 | 1 |
| 2 | 53 | 1 |
| 2 | 26 | 1 |
| 2 | 13 | 0 |
| 2 | 6 | 1 |
| 2 | 3 | 0 |
| 2 | 1 | 1 |
| | 0 | 1 |

$\therefore (1725)_{10} = (11010111101)_2$.

ii. Conversion into octal form.

Since, we got the binary form of 1725 so using it to convert into octal form. As we know that three digit of binary gives one octal value.

So, 011 010 111 101

↓ ↓ ↓ ↓

3 2 7 5

$\therefore (1725)_{10} = (3275)_8$

iii. Conversion into hexadecimal form.

We know that four digit of binary gives 1 hexadecimal digit. So using the binary of 1725 for hexadecimal conversion.
i.e.

| 0110 | 1011 | 1101 |
|---|---|---|
| ↓ | ↓ | ↓ |
| 6 | B | D |

$\therefore (1725)_{10} = (6BD)_{16}$.

Q.N.2.

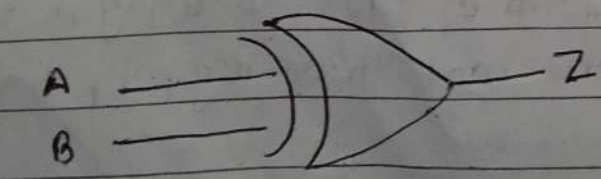
Ans. Special purpose gates:

The logic gates which are used for special kind of purpos are called special purpose gate.

Some of the special purpose gates are EX-OR, EX-NOR.

EX-OR:

- EX-OR logic gate is two input and one ouput logic circuit.
- The output of this gate is 1 when only one of its input is 1. Ily, The output is 0 when the both inputs are same.




logic gate

It is denoted by,

$Z = A \oplus B$.

Also, $Z = \bar{A}B + A\bar{B}$.

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Truth table:

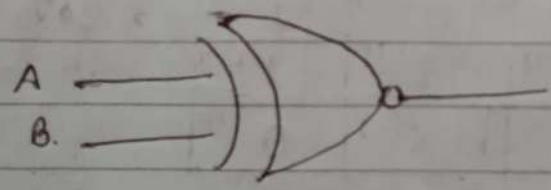
| Inputs | | Outputs. |
|---|---|---|
| A | B | Z |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Use case of EX-OR gate:

- It is used in implementation of half-adder and also be used for subtractors, comparators.

EX-NOR gate:

- EX-NOR gate is two input and one ouput logic circuit.
- The output of this gate is zero if the inputs are 0 & 1 or 1 & 0. Ily, The output of this gate is 1 if the both inputs are either 0 or 1.




Logic symbol.

It is expressed as

$$Z = A \oplus B$$

or, $$Z = AB + \bar{A}\bar{B}.$$

Truth table:

| Inputs | | Outputs |
|---|---|---|
| A | B | Z. |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Use case of Ex-NOR gate:

→ It is mainly used in electronic circuits that performs arithmetic operations and data checking such as Adders, Subtractors and parity checkers.

→ Also they can be used in Digital comparator circuits.

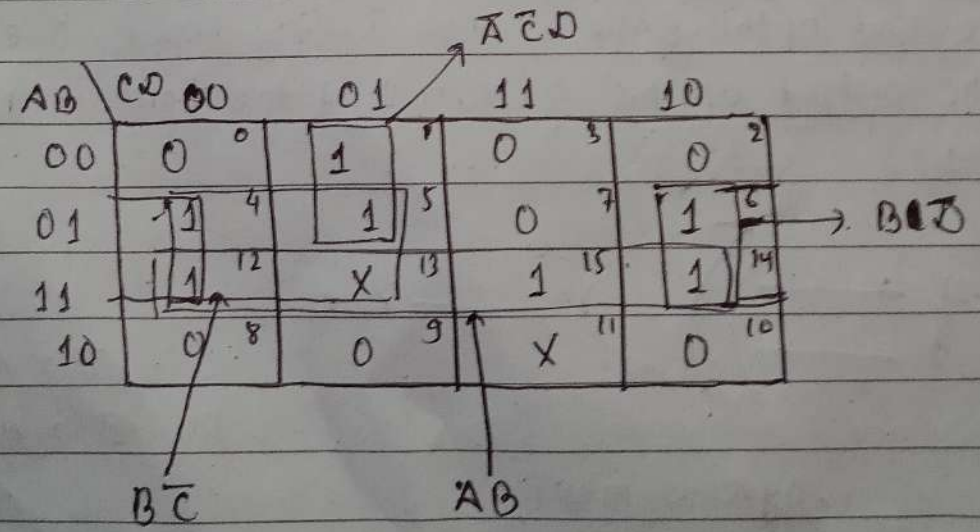
Q.N.3.

Ans. Given,

$F = \Sigma(1,4,5,6,12,14,15)$.

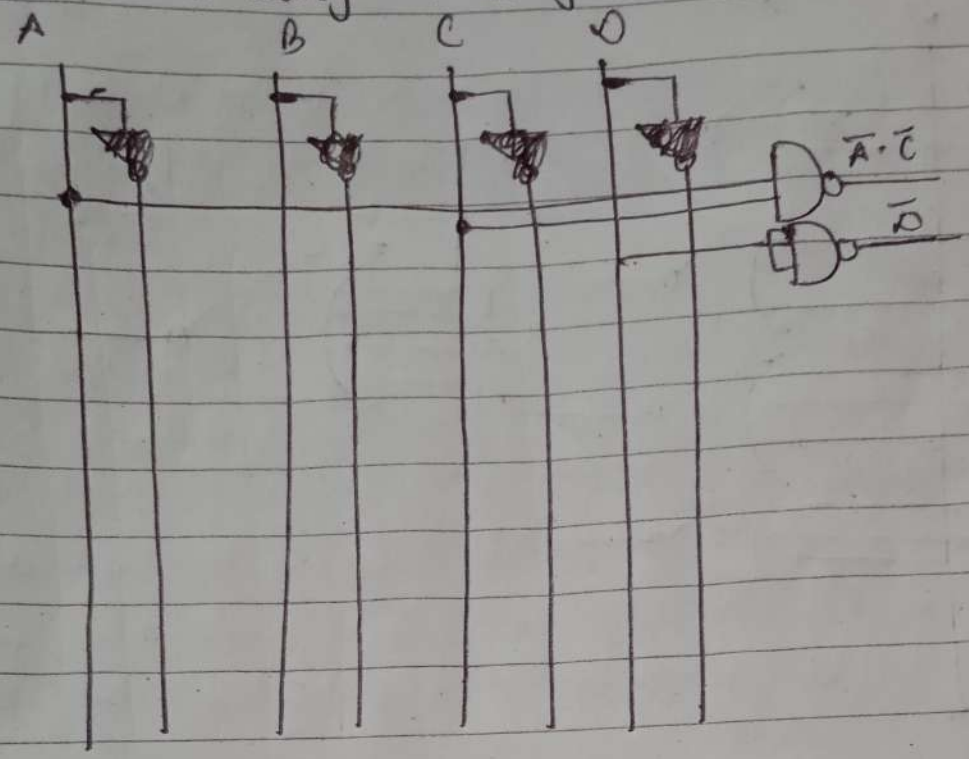
$D = \Sigma(11,13)$.

Constructing k-Map for given data. [for SOP (NAND gate)]
(Let the inputs be A, B, C & D).

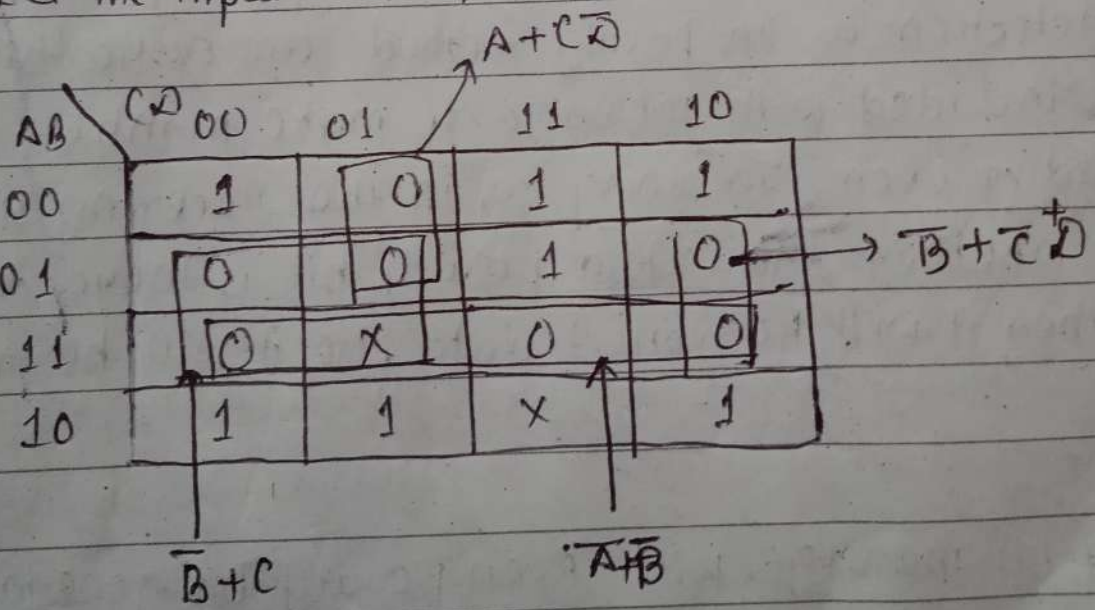



$= \bar{A}\bar{C}D + B\bar{C} + A\bar{B} + BC\bar{D}$.

Realization using NAND gate.

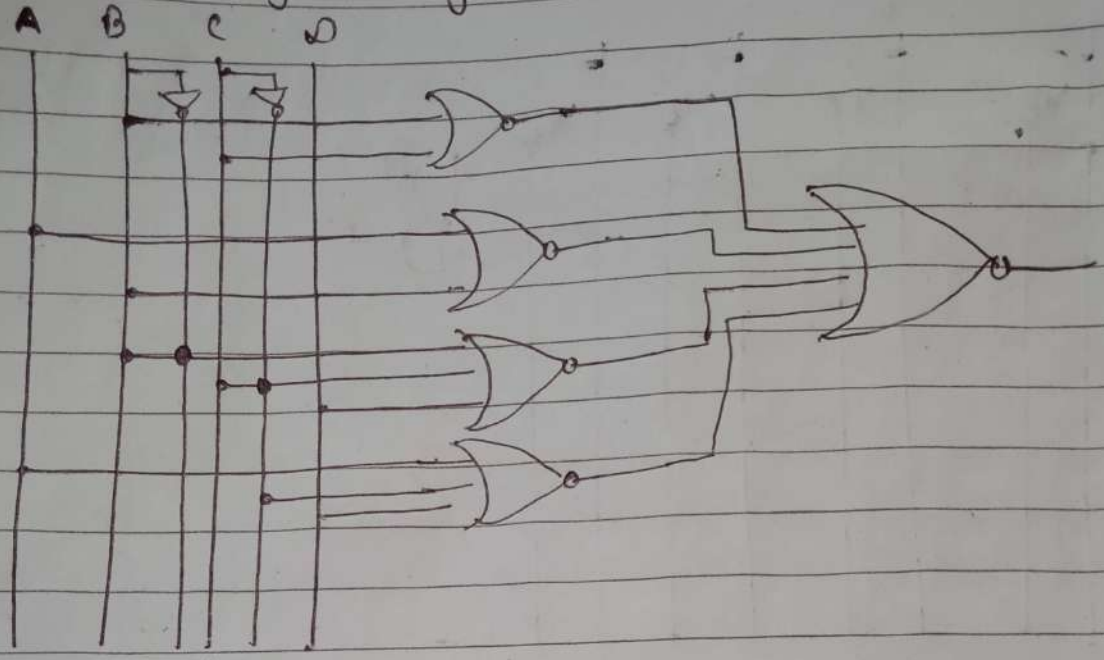



Constructing k-Map for given data [for POS (Nor Gate)]
(Let the inputs be A, B, C & D).




$= (\overline{B}+C) \cdot (\overline{A+B}) \cdot (\overline{B}+\overline{C}\overline{D}) \cdot (A+C\overline{D})$.

Realization using NOR gate.




Q.N.4.

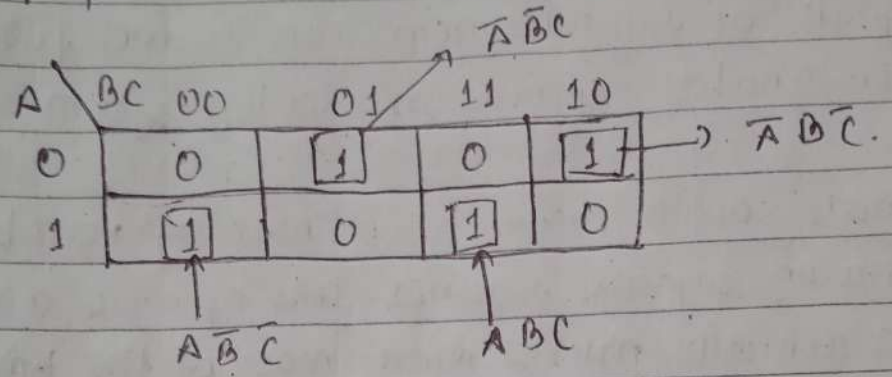
Ans. If I am network engineer, I would use parity method for error detection. So, In parity method, an extra bit (parity bit) is included with message to make number of 1's either odd or even. In doing so, in the receiving side, I can check whether the extra parity bit is there or not. If there is, then it will be correct data else it will be incorrect one.

Let us take 3-bit message with Even parity bit generator (P).

| A | B | C | P |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |

| | | | |
|---|---|---|---|
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

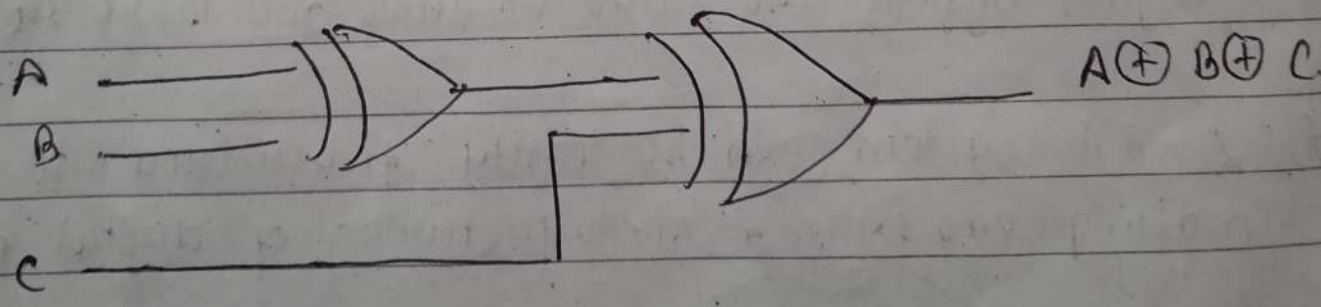
K-Map for 3-bit even parity generator.




from K-Map.

$$P = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$
$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$
$$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$$
$$= A \oplus B \oplus C.$$

Logic Diagram,



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Q.N.5.

Ans. There are many reason for today's world in adapting digital system over analog system. Some of the reasons are:

a. Digital signals of Digital system can travel faster as compared to analog signals of Analog system.

b. Digital signals don't carry noise, making reliable data. whereas analog signals carries lots of noise and is difficult to achieve precise data; most of the times.

c. Digital system can transfer more data as compared to analog system.

d. Digital system are easier to design, as compared to analog system.

e. Digital system are more versatile and more reliable.

f. Digital system can be easily fabricated into IC chips, making easier for manufacturing of digital products.

g. Information storage is easy in digital system as compared to Analog system.

Hence, Because of all these reasons, digital system becomes more useful in today's world.

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Q.N. 6.

Ans. A higher order MUX can be easily constructed by using lower order MUX.
For this construction let us take 4:1 MUX and by using 4:1, four MUX, +1 output MUX we will design 16:1 order MUX.

Construction:

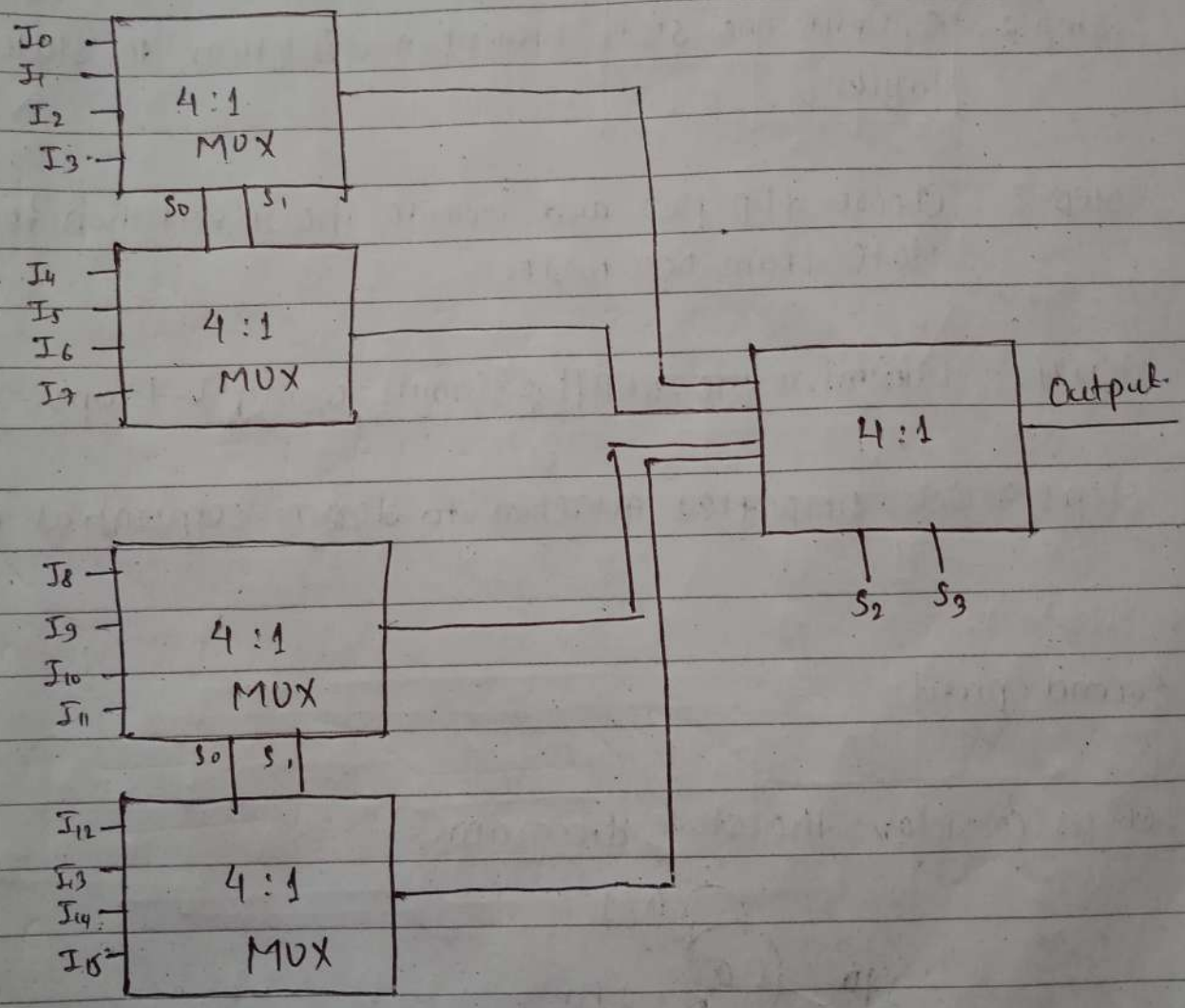


fig: 16:1 MUX using 4:1 MUX.

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Q.N. 7.

Ans. The procedure to be considered while designing a sequential circuit in digital system design. are:

Step 1: Create a state transition diagram for desired sequential circuit.

Step 2: Convert the state transition diagram to state transition table.

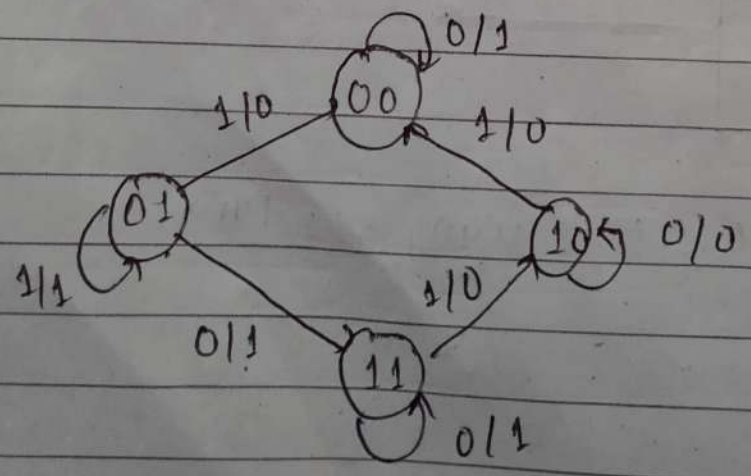
Step 3: Choose flip-flop and include their exitation table in state transition table.

Step 4: Minimize the flipflop inputs using K-Maps.

Step 5: Use simplified function to design sequential circuit.

Second part:

Let us consider the state diagram.



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Conversion of information of state diagram into state table.

| Present state (AB) | Input (X) | Next state (A'B') | SR input $S_A R_A$ | SR input $S_B R_B$ | Output (Y) |
|---|---|---|---|---|---|
| 00 | 0 | 00 | 0x | 0x | 1 |
| 00 | 1 | 01 | 0x | 10 | 0 |
| 01 | 0 | 11 | 10 | x0 | 1 |
| 01 | 1 | 01 | 0x | x0 | 1 |
| 10 | 0 | 10 | x0 | 0x | 0 |
| 10 | 1 | 00 | 01 | 0x | 0 |
| 11 | 0 | 11 | x0 | x0 | 1 |
| 11 | 1 | 10 | x0 | 01 | 0 |

Excitation table of S-R flipflop.

| $Q_t$ | $Q_{t+1}$ | S | R |
|---|---|---|---|
| 0 | 0 | 0 | x |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | x | 0 |

Now, solving using k.Map.

For $S_A$:

| A \ BX | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 1 | x | 0 | x | x |

$\therefore S_A = B\bar{X}$

For $R_A$:

| R \ BX | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | X | X | X | 0 |
| 1 | 0 | 1 | 0 | 0 |

$\therefore R_A = \overline{B}X$.

For $S_B$:

| A \ BX | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | X | X |
| 1 | 0 | 0 | 0 | X |

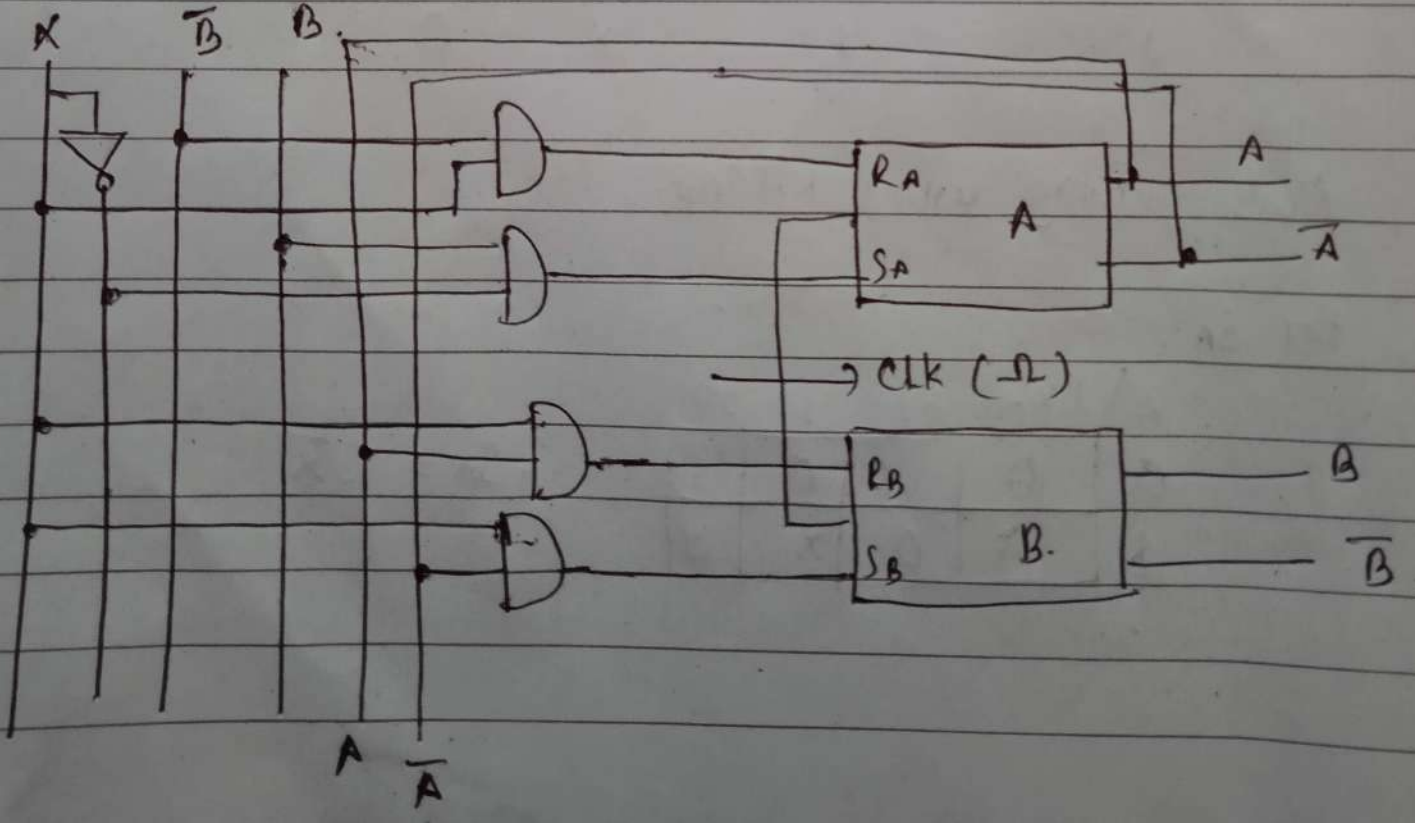
$\therefore S_B = \overline{A}X$.

For $R_B$:

| A \ BX | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | X | 0 | 0 | 0 |
| 1 | X | X | 1 | 0 |

$\therefore R_B = AX$

Realization.

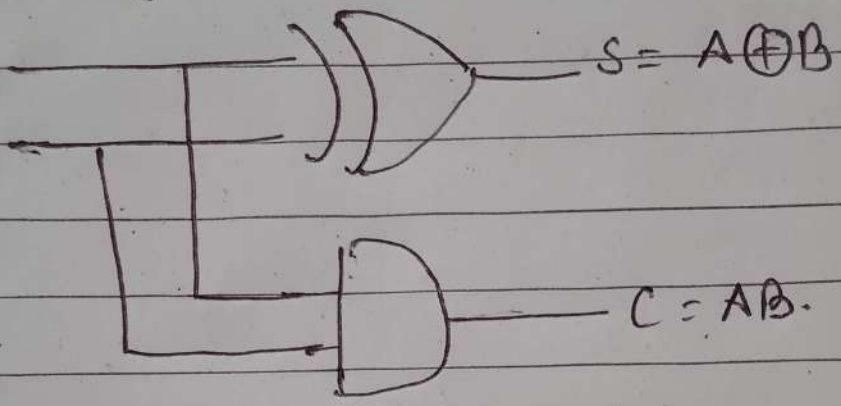


Q. N. 2.

Remaining part:

E-OR gate as Half adder:

Logic Diagram.



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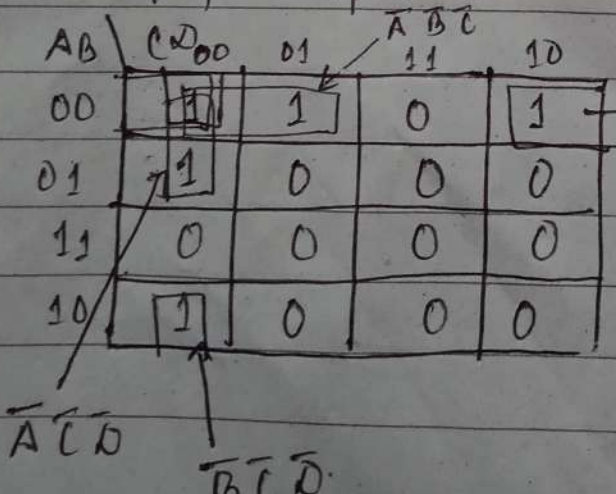
Q. N. 8.

Ans. Let the four inputs be A, B, C, D and outputs be Y and Z.
So, the truth table is,

| A | B | C | D | Y | Z |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 |

K-Map for output Y.




$\therefore Y = \bar{A}\bar{C}\bar{D} + \bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{D}$

$= \bar{C}\bar{D}(\bar{A} + \bar{B}) + \bar{A}\bar{B}(\bar{C} + \bar{D})$

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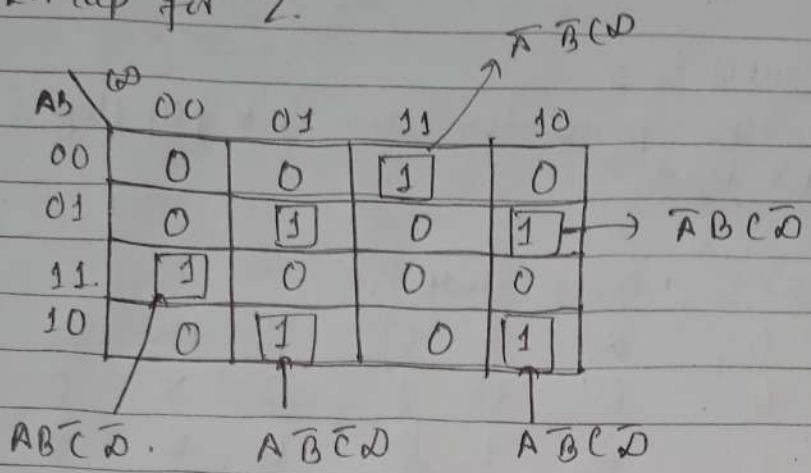
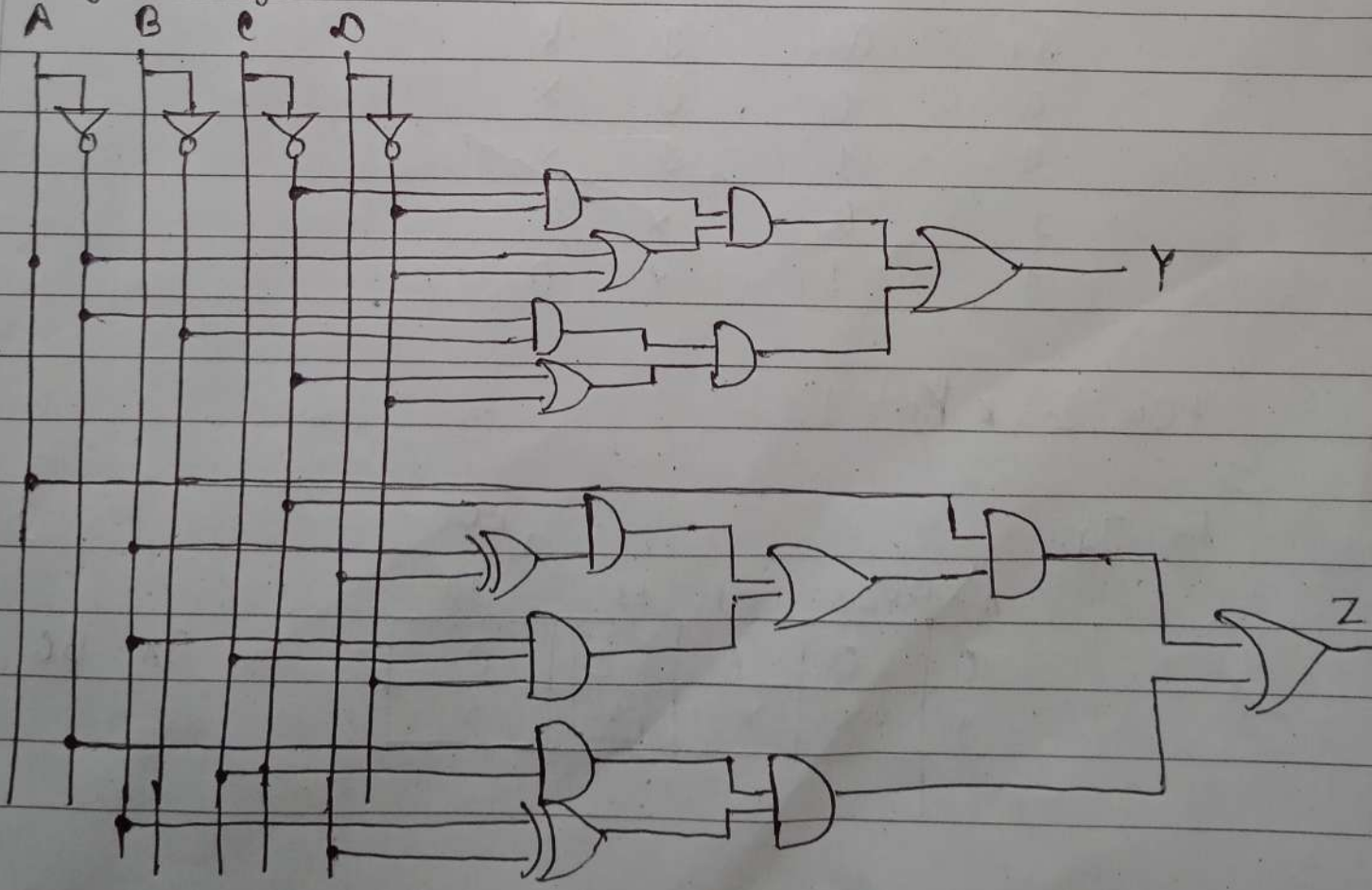
K-Map for Z.




$$\therefore Z = AB\bar{C}\bar{D} + A\bar{B}\bar{C}D + A\bar{B}C\bar{D} + \bar{A}BC\bar{D} + \bar{A}\bar{B}CD.$$
$$= A[B\bar{C}\bar{D} + \bar{B}\bar{C}D + \bar{B}C\bar{D}] + \bar{A}C(B\bar{D} + \bar{B}D)$$
$$= A[\bar{C}(B\bar{D} + \bar{B}D) + \bar{B}C\bar{D}] + \bar{A}C(B \oplus D).$$
$$= A[\bar{C}.(B \oplus D) + \bar{B}C\bar{D}] + \bar{A}C(B \oplus D).$$

Logic Diagram.



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Q.N.9.

Ans. My last digit symbol is 5.
So, MOD 5 synchronous up counter using J-K flipflop:
Let us take 3-bit input.

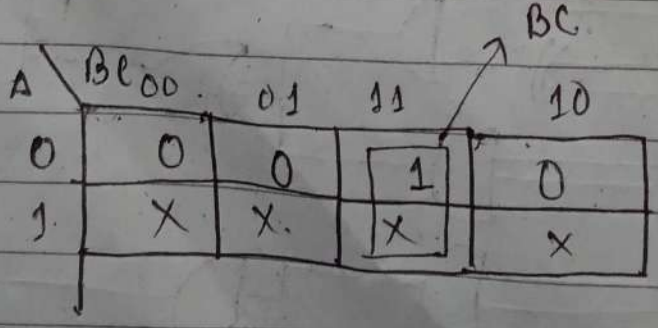
| Present state. | | | Next state | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | A' | B' | C' | $J_A$ | $K_A$ | $J_B$ | $K_B$ | $J_C$ | $K_C$ |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | X | 0 | X | 1 | X |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | X | 1 | X | X | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | X | X | 0 | 1 | X |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | X | X | 1 | X | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | X | 0 | 0 | X | 1 | X |
| 1 | 0 | 1 | 0 | 0 | 0 | X | 1 | 0 | X | X | 1 |

Excitation table for J-K flipflop.

| $Q_t$ | $Q_{t+1}$ | J | K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

Here, $J_C = K_C = 1$.

For, $J_A$.




$\therefore J_A = BC$

For $K_A$.

| A \ BC | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | X | X | X | X |
| 1 | 0 | 1 | X | X |

C

$\therefore K_A = C.$

For $J_B$.

| A \ BC | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | X | X |
| 1 | 0 | 0 | X | X |

AC

$\therefore J_B = AC$

For $K_B$.

| A \ BC | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | X | X | 0 | 1 |
| 1 | X | X | X | X |

$\bar{A}\bar{C}$.

$\therefore K_B = \bar{A}\bar{C}.$