Mock Test.

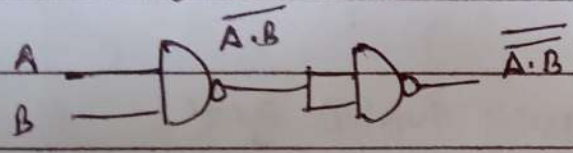
Page No.

Q.N.1.

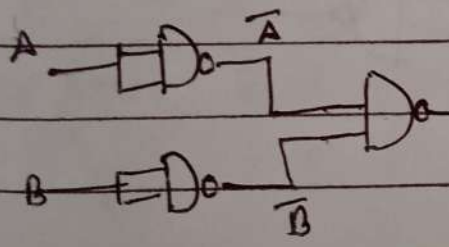
Ans. NAND and NOR gates are called Universal gates because from the use of any of the gate we can easily construct other logic gates.

Realization of logic gates using NAND gate:

i. AND gate.



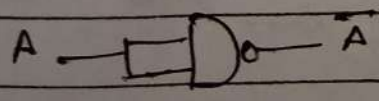
ii. OR gate.



$\overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}}$ (By De. Morgan Theorem)

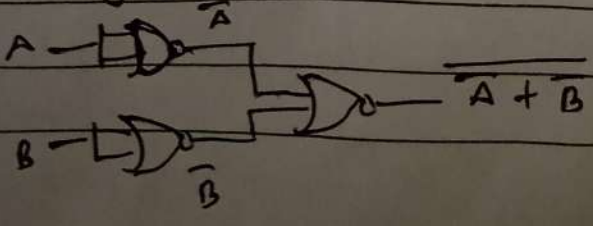
$= A + B$

ii. NOT gate.



Realization of logic gates using NOR gate:

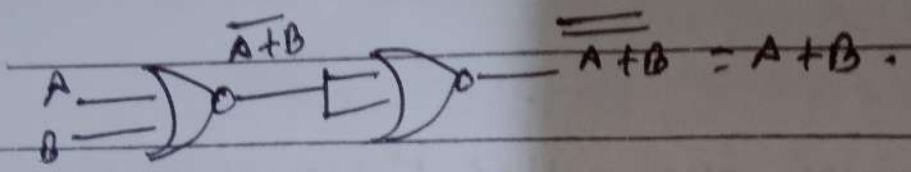
i. AND gate.



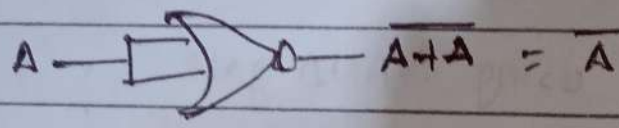
$\overline{A + B} = \overline{\overline{A}} \cdot \overline{\overline{B}}$ (By De. Morgan Theorem)

$= A \cdot B$

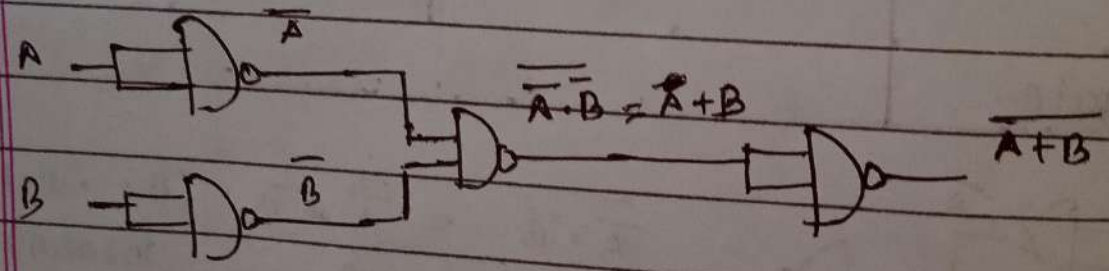
ii. OR gate.



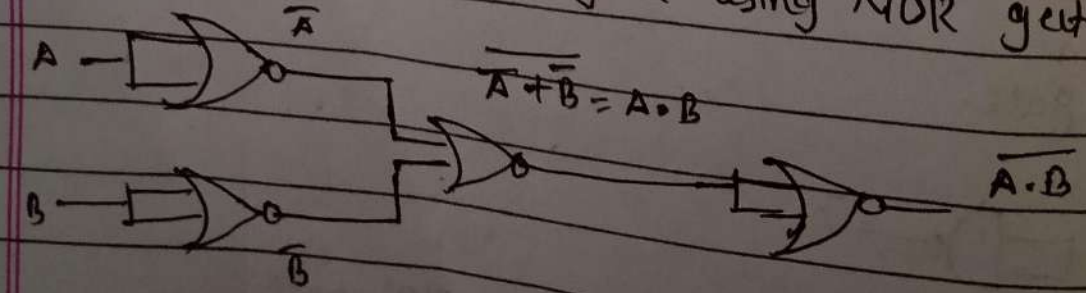
iii. NOT gate.



Construction of NOR gate using NAND gate.



Construction of NAND gate using NOR gate.



Q.N.2.

we have the following truth table of full adder.

X	Y	C_i	S_i	C_{out}
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

We have, $S_i = \bar{X}\bar{Y}C_i + X\bar{Y}C_i + XY\bar{C}_i + XYC_i$

$= \bar{X}\bar{Y}C_i + XY\bar{C}_i + X\bar{Y}C_i + XYC_i$

$= \bar{X}\bar{Y}C_i + XY\bar{C}_i + XC_i(Y+\bar{Y})$

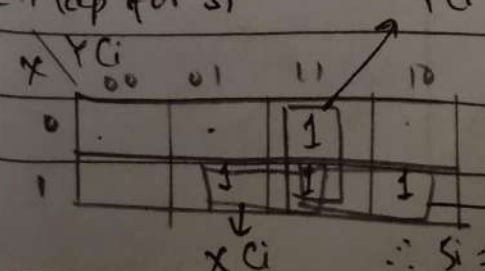
$= \bar{X}\bar{Y}(\bar{X}C_i + X\bar{C}_i) + XC_i$

and $C_{out} = \bar{X}\bar{Y}C_i + \bar{X}Y\bar{C}_i + X\bar{Y}\bar{C}_i + XYC_i$

$= \bar{X}\bar{Y}C_i + X\bar{Y}\bar{C}_i + \bar{X}Y\bar{C}_i + XYC_i$

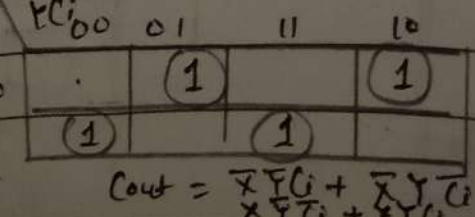
$= \bar{Y}(\bar{X}C_i + X\bar{C}_i) + Y(\bar{X}\bar{C}_i + XC_i)$

K.Map for S_i



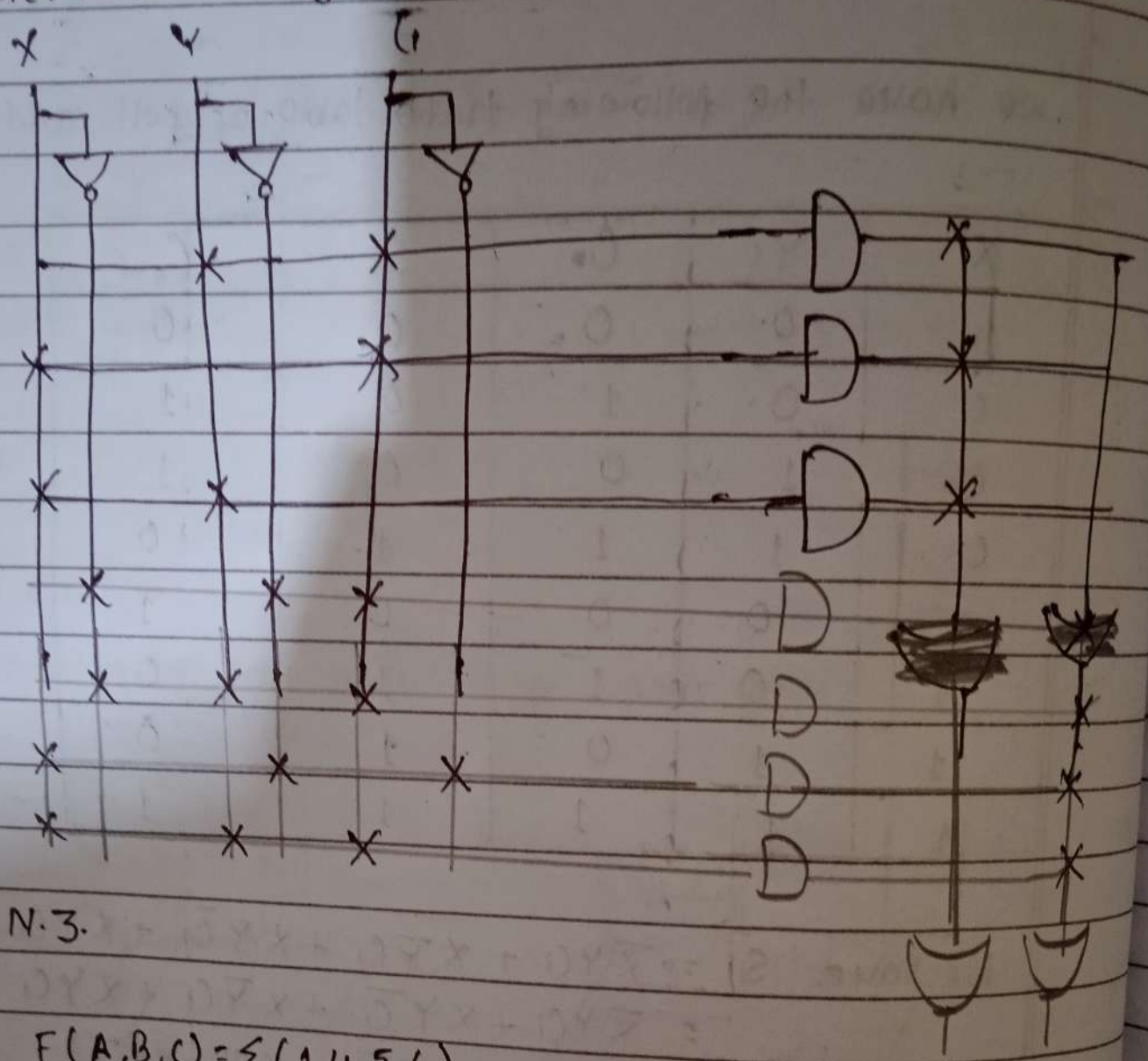
$\therefore S_i = YC_i + XC_i + XY$

K.Map for C_{out}



$C_{out} = \bar{X}\bar{Y}C_i + \bar{X}Y\bar{C}_i + X\bar{Y}C_i + XYC_i$

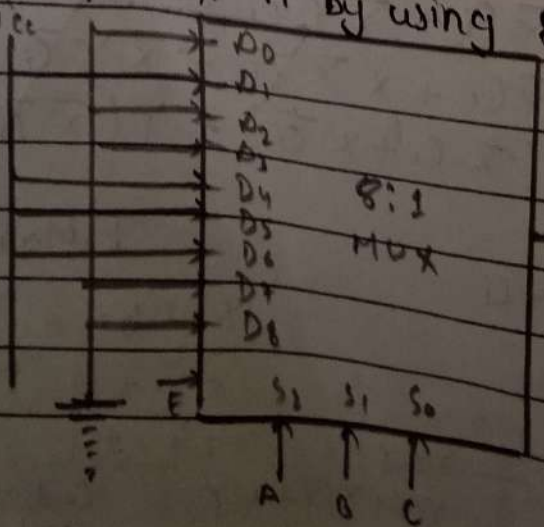
Implementation using PLA.



Q.N.3.

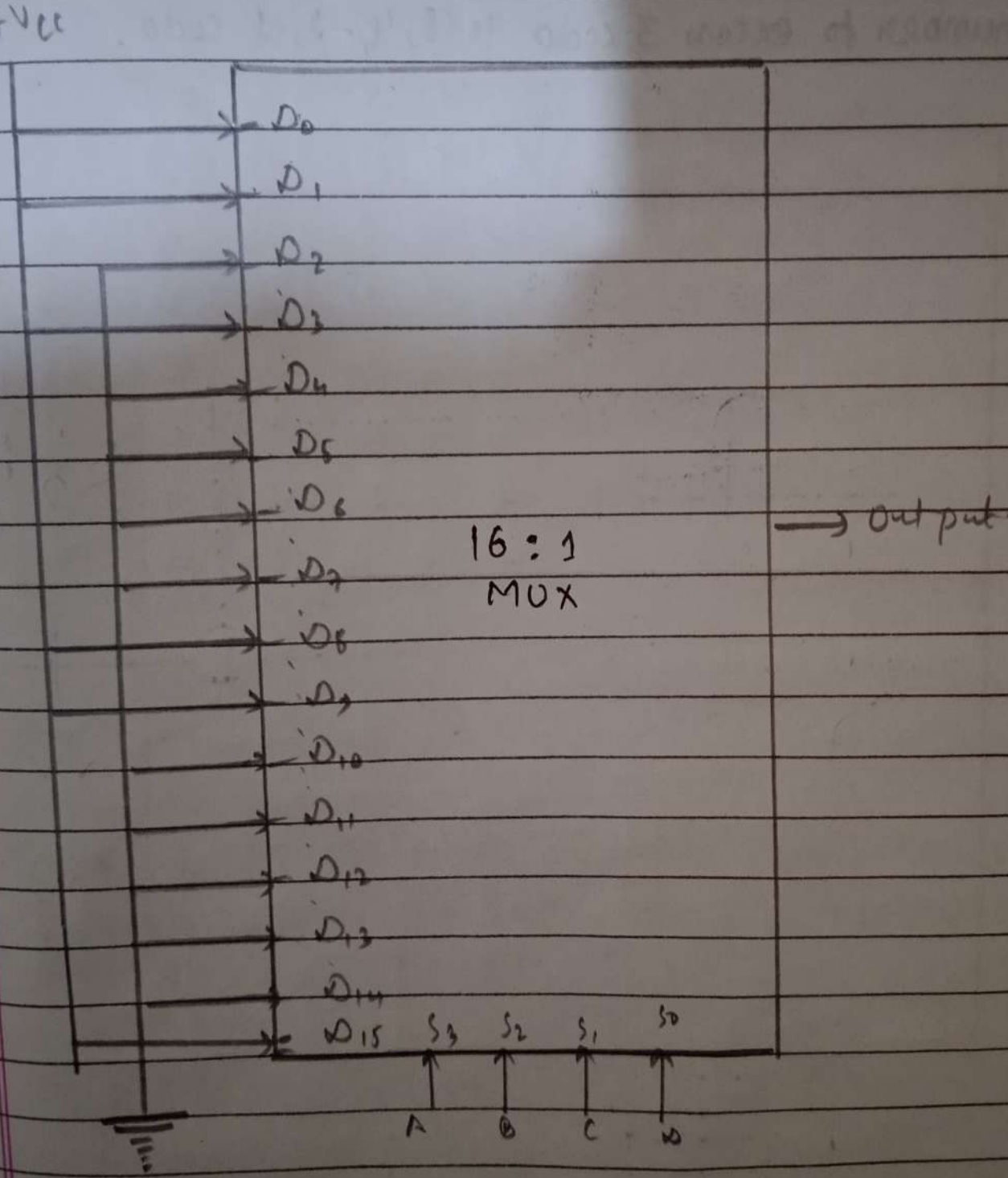
i. $F(A,B,C) = \Sigma(1,4,5,6)$.

Since the given function has three variables, so we can implement it by using 8:1 MUX.



ii. $F(A,B,C,D) = \Sigma(0,1,3,8,9,15)$.

Since the given function has four variables. So, we can implement it by using 16:1 MUX



Q.N.5.

Counter is the sequential ckt that passes through the predefined sequence of state upon the application of input clock pulse.

No. of T flip flop required = 4.

$2^n \geq 10$

$2^4 \geq 10$

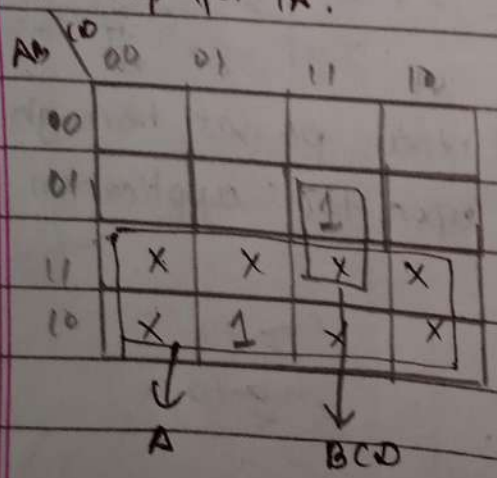
Excitation Table of T flip flop

Q_t	Q_{t+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

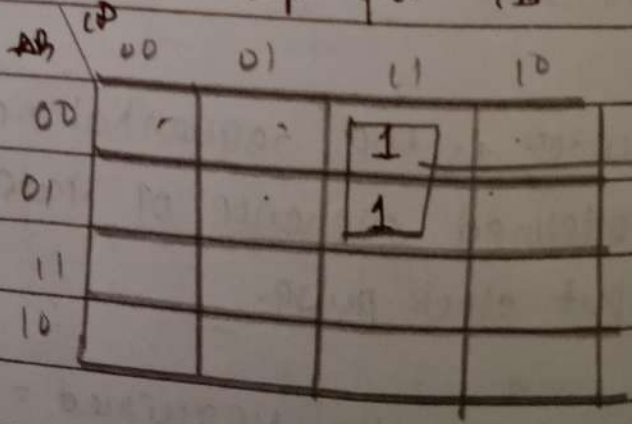
Present state (P.S)				Next state (N.S)				T. inputs			
A	B	C	D	A'	B'	C'	D'	T_A	T_B	T_C	T_D
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1

From above table $T_D = 1$.

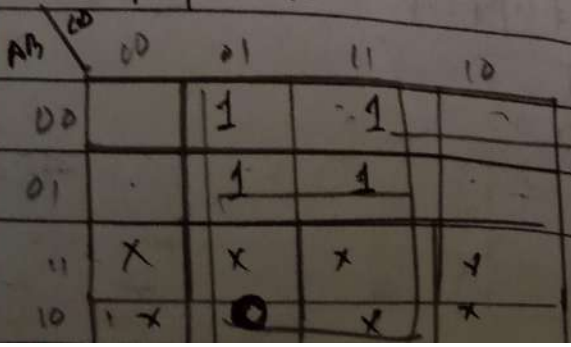
k-Map for T_A.



K-Map for T_B



k-Map for T_C



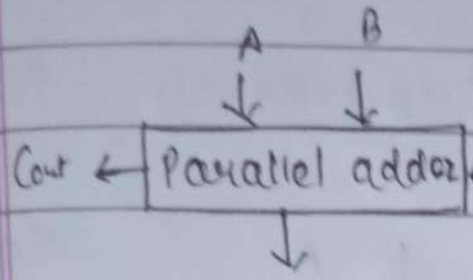
$\therefore T_A = A + BCD$

$T_B = \bar{A}CD$

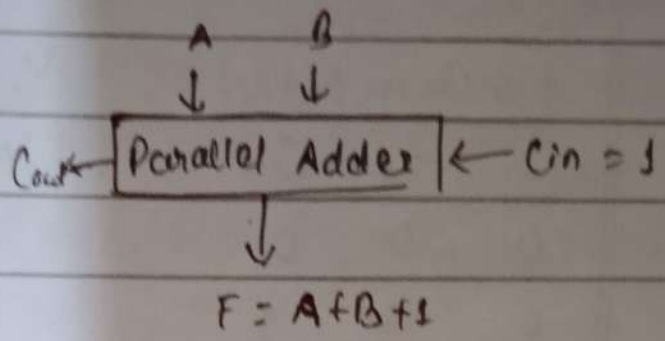
$T_C = \bar{A}D$

$T_D = 1$

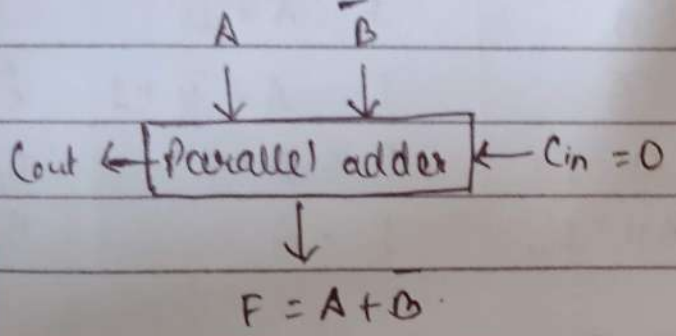
Q.N.6.



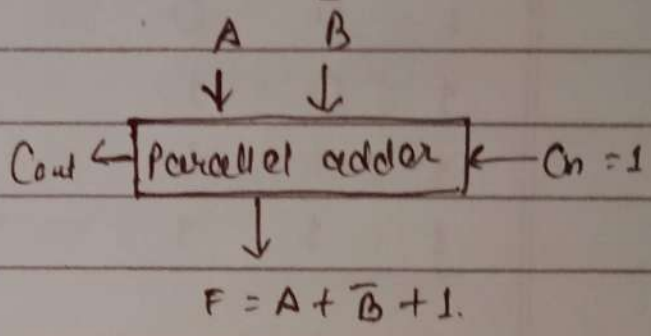
(a) Addition.



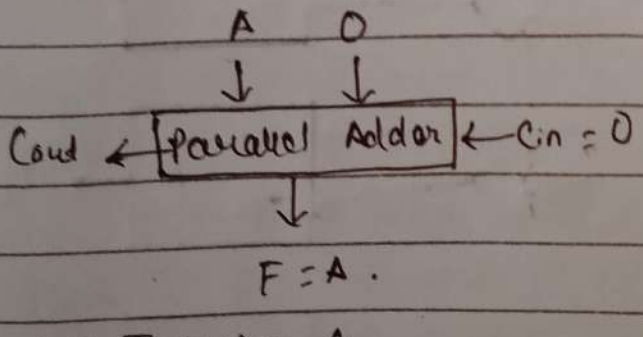
(b) Addition with carry.



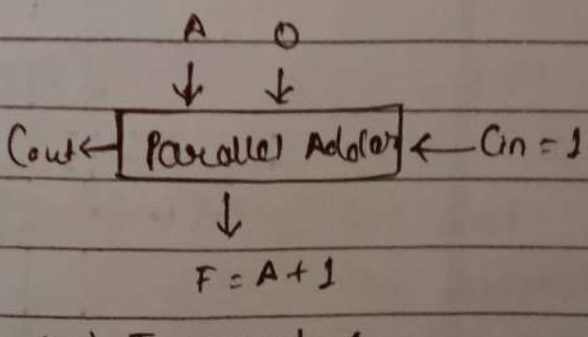
(c) A plus 1's complement of B.



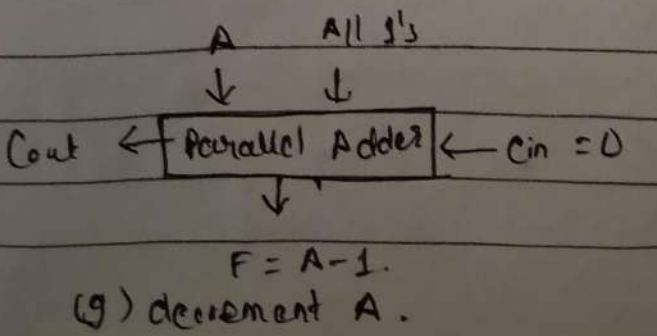
(d) Subtraction.



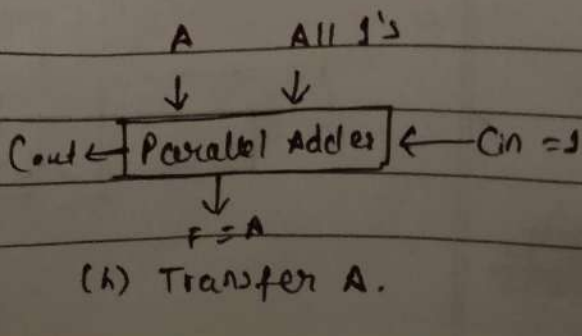
(e) Transfer A.



(f) Increment A.



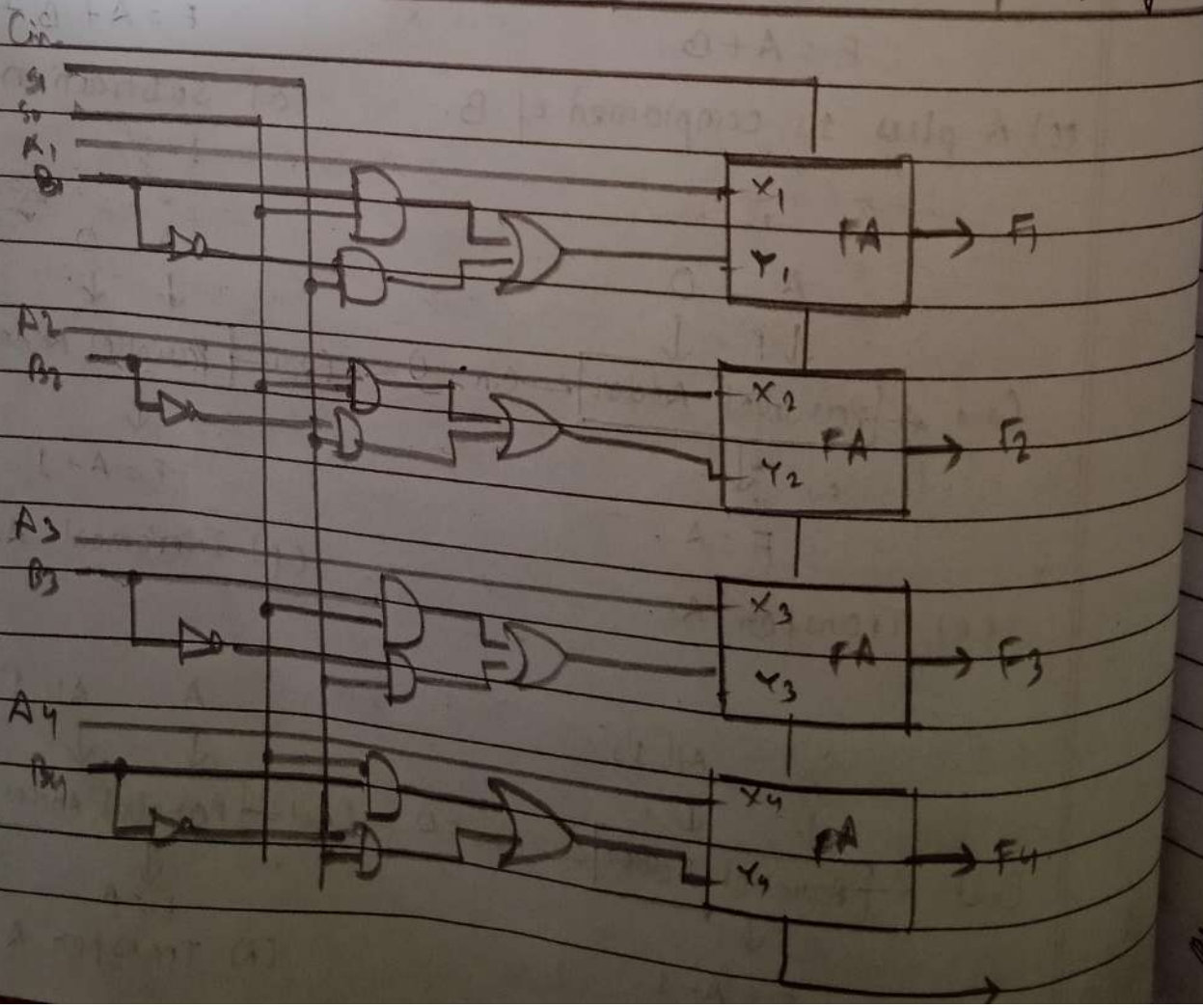
(g) decrement A.



(h) Transfer A.

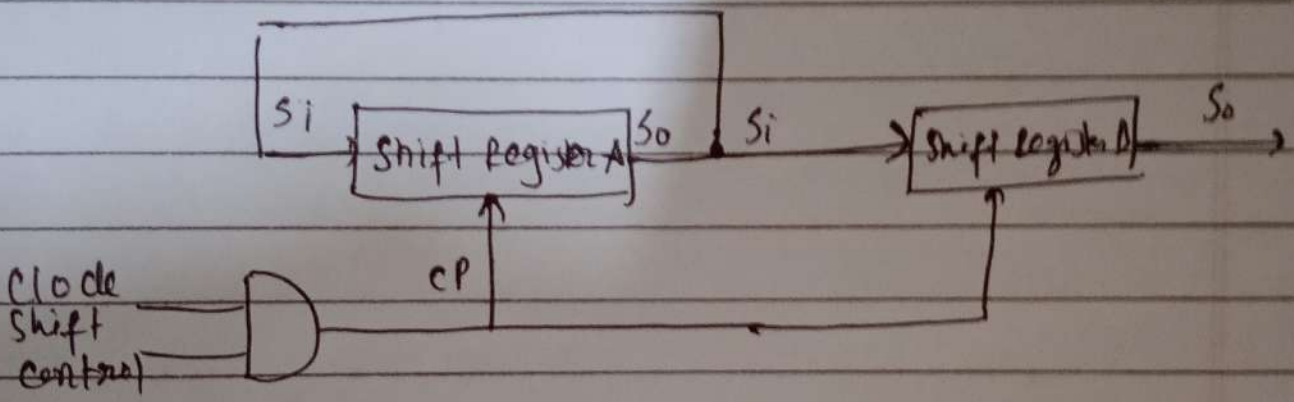
Function table for arithmetic circuit:

Function select			Y equals (Input)	Output equals	Function
S_1	S_0	Cin			
0	0	0	0	F = A	Transfer A
0	0	1	0	F = A+1	Increment A
0	1	0	B	F = A+B	Add B to A
0	1	1	B	F = A+B+1	Add B to A+1
1	0	0	$\overline{B}$	F = A+$\overline{B}$	Add 1's complement of B to A
1	0	1	$\overline{B}$	F = A+$\overline{B}$+1	Add 1's complement of B to A
1	1	0	All 1's	F = A-1	Decrease A
1	1	1	All 1's	F = A	Transfer A.



Shift Register:

A register capable of shifting its binary information either to the right or the left. The logical configuration of shift register consits of a chain of flipflops connected in cascade. A flipflop receives a common clock pulse which causes the shift from one stage to another.



(a) Block diagram of serial transfer of information from register A to register B.

Assume the binary content of A before the shift is 1011 and that of B is 0010. The serial transfer from A to B will occur in 4 steps as shown in table. After the first pulse T1 the rightmost bit of A is shifted into the leftmost bit of B and at the same time, this bit is circulated into the leftmost position of A.

Once the bit of A and B are shift to right, the previous serial output from B is lost.

Timing pulse	Shift Register A				Shift Register B				Serial output of B
Initial value	1	0	1	1	0	0	1	0	0
After T_1	1	1	0	1	1	0	0	1	1
After T_2	1	1	1	0	1	1	0	0	0
After T_3	0	1	1	1	0	1	1	0	0
After T_4	1	0	1	1	1	0	1	1	1.