9th 2nd half.

10 Fault Detection and Location

SYLLABUS

Fault Detection and Location : Fault models for combinational and sequential circuits, Fault detection in combinational circuits; Homing experiments, Distinguishing experiments, machine identification and fault detection experiments in sequetial circuits.

Chapter Outline

10.1. INTRODUCTION

In recent years, the development of integrated-circuit technology has accelerated rapidly; MSI and LSI techniques promise to make today's functional-level devices tomorrow's (even today's) basic components. Accordingly, digital systems are built with more and more complexity; the fault testing and diagnosis of digital circuits becomes an important and indispensible part of the manufacturing process. The problem of fault testing and diagnosis consists of the follwing two subproblems:

1. The fault-detection problem
2. The fault-location problem.

The first problem is the determination of whether or not any of a prescribed list of faults, which may include all possible single faults and multiple faults, has occurred. The second problem, in turn, consists of the following subproblems:

(i) Determination of the location of the fault that has occurred.

(ii) Determination of the location of the fault within a module (package or subnetwork) in which it has occurred.

10.2. FAULT MODELS FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS

A number of basic analytic and heuristic models, including the fault-table method, the path-sensitizing and equivalent-normal-form (ENF) method, the Karnaugh map and tabular method, the ENF-Karnaugh map method, the Boolean difference method, and the SPOOF method are main fault models. The fault-table method is the most classic approach to the problem. It is completely general and always yields a minimum set of diagnostic tests. However, it suffers from the fact that it requires a very large fault table to be constructed. To overcome the problem of not requiring the construction of a very large fault table, the concept of path sensitizing is used. The path-sensitizing method requires no fault table, basically only work for the class of tree-like circuits and some special non-tree-like circuits. A heuristic, systematic procedure derived from the concept of path sensitizing, knwon as the **equivalent-normal-form (ENF) method**, is also most popular.

10.3. FAULT DETECTION IN COMBINATIONAL CIRCUITS

After a digital circuit is designed and built, it is always desirable to know whether the circuit is constructed without any faults. If it is properly constructed and in use, it may be disabled by almost any internal failure. The process of applying tests and determining whether a digital circuit is fault-free or not is generally known as **fault detection**. If a known relationship exists between the various possible faults and the deviations of output patterns, it is possible to identify the failures and to classify them (at least) within the smallest possible set of components. This process is termed **fault location. Fault diagnosis** is generally referred to as the composite of both the above processes.

The diagnostic techniques of digital systems have progressed from the state of testing the operation codes of the machine instruction set in the early days to the current hardware-assisted software aids for speedy determination and identification of faulty elements. In the coming LSI (large-scale-integration) era, the problem of diagnosis is shifted from locating the faulty discrete component to the identification of the replaceable module (chip or flat pack) in which the faulty component is resident.

Testing strategies generally depend on the system design and the architecture. Generally, the diagnostic engineer partitions the system into levels of hierarchy (systems, functional subsystems, modules, chips, etc.) and uses these levels in an organized fashion to isolate faults. Test points and the like provide mutual isolations among the partitions at various levels and help to reduce the size and time of testing. Here, we shall only be concerned with the fault detection and location problem at the circuit level.

Further, a fault-detection test set is said to be minimal if it is a minimal set that can detect the existence of each of the faults under consideration. A fault-location test set is said to be minimal if it is a minimal set that can locate each of the faults under consideration to the smallest identifiable part of the logic circuit.

10.4. THE FAULT-TABLE MODEL

As a matter of fact, the fault-table method for constructing a shortest fixed- scheduled experiment for fault location consists of a three steps:

Step 1. Construction of the fault table.

Step 2. Construction of the fault-location table. The fault-location table G_L is constructed from the reduced fault table F*. A column of G_L is formed by taking the exclusive or operation on a pair of columns of F*. If we let f_0 be the output of an n-input single-output combinational circuit with no detectable faults, and $f_1, f_2, \ldots, f_m$ be the outputs of the circuit with m faults, respectively, then the fault-location table has 2^n rows denoted by $0, i, \ldots, 2^n - 1$, and $m(m + 1)/2$ columns, each of which is obtained by $f_i \oplus f_j$, $0 \leq i < j \leq m$. If it is only required to locate the faults within the limits of the modules of the circuit, the table G_M for fault location-to-within-modules is constructed from F in the same way as G_L, except for one column for each pair of columns of F* that belong to different modules. It should be noted that G_D is always contained in G_L and G_M.

Step 3. Find a minimal cover of G_L or G_M.

The fault-table method for fault detection and fault location is illustreated by the following example.

EXAMPLE 10.1. Consider the circuit of figure 10.1. The output function of this circuit is $z = f(x_1, x_2, x_3) = x_1 x_2 + x_2 x_3$. The fault table for detection and location of all the single faults of the circuit is shown in Table 10.1. In this table, f_0 denotes the output function of the faultless version of the circuit, and f_{ij} represents the output function of the circuit with its ith line stuck at 0(j = 0) or 1(j = 1). It is observed that all the faults are detectable, and four groups of faults $\{f_{10}, f_{20}, f_{50}\}$, $\{f_{11}, f_{41}\}$, $\{f_{30}, f_{40}, f_{60}\}$ and $\{f_{51}, f_{61}\}$ in this table are indistingusihable faults. We combine them, choose one function from each group, and delete the rest of them

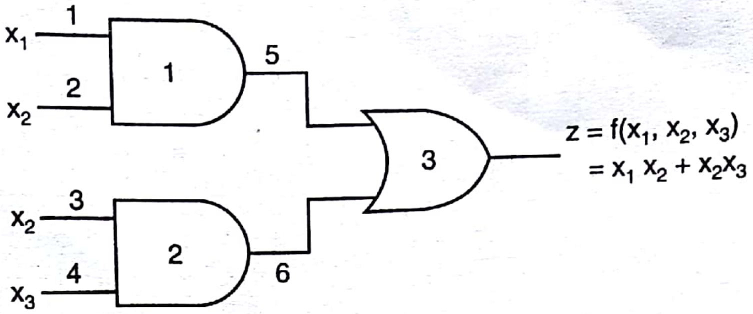

Fig. 10.1. Example to illustrate fault location using the fault table.

Table 10.1. Fault table for detection and location of all single faults

r	x_1	x_2	x_3	f_0	f_{10}	f_{11}	f_{20}	f_{21}	f_{30}	f_{31}	f_{40}	f_{41}	f_{50}	f_{51}	f_{60}	f_{61}
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
1	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	1
2	0	1	0	0	0	1	0	0	0	0	0	1	0	1	0	1
3	0	1	1	1	1	1	1	1	0	1	0	1	1	1	0	1
4	1	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1
5	1	0	1	0	0	0	0	1	0	1	0	0	0	1	0	1
6	1	1	0	1	0	1	0	1	1	1	1	1	0	1	1	1
7	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
				f_0	f_1	f_2		f_3	f_4	f_5	f_6					

from the table. Name the six distinct output functions which represent six distingusihable faults to be $f_1, \ldots, f_6$, as indicated at the bottom of the table. From the functions $f_0, \ldots, f_6$, we form the fault-location table G_L, which is shown in table 10.2. The column label kl represents the functions f_k and f_l, from whcih the column is constructed $(f_1 \oplus f_l)$, where, $0 \le k < 1 \le m$, and m denotes the total number of distinguishable faults. So, there are C_2^m = $m(m - 1)/2$ columns in G_L.

Table 10.2. Fault-location table G_L of example 10.1, which includes the fault-detection table as a subtable

Fault / Test	✓ 01	✓ 02	03	✓ 04	05	✓ 06	✓ 12	✓ 13	✓ 14	✓ 15	✓ 16	✓ 23	✓ 24	✓ 25	26	✓ 34	35	✓ 36	✓ 45	✓ 46	✓ 56
0						1					1				1			1		1	1
1					1	1				1	1			1	1		1	1	1	1	
•2		①				1	1				1	1	1	1				1		1	1
•3				①					1				1			1			1	1	
4			1			1		1			1	1			1	1	1			1	1
5			1		1	1		1		1	1	1		1	1	1			1	1	
•6	①						1	1	1	1	1										
7																					

Fault-detection table G_D

A close examination of the faults that are covered by each of these four tests shows that

Test	x_1	x_2	x_3	
3	0	1	1	test all the s − a − 0 faults
6	1	1	0	
2	0	1	0	test all the s − a − 1 faults
5	1	0	1	

Now let us examine the fault-location table, which is the entire table of Table 10.2 It is observed that tests 2, 3, and 6 are essential tests which cover all the columns except the four columns 03, 05, 26, and 35. With these columns and the nonessential rows (tests), we construct the fault-location table:

Test \ Fault	03	05	~~26~~	35
~~0~~			~~1~~	
1		1	~~1~~	1
4	1		~~1~~	1
5	1	1	~~1~~	

Test 0 is dominated by test 1 and column 26 dominates all the other three columns, so they can be removed from the table. The remaining table shows that any choice of two tests from the three tests 1, 4, and 5, plus the essential tests, will cover all the columns of G_L (i.e., will locate all six distinguishable faults). Hence, the minimal fault-location experiment for this circuit should consist of tests 2, 3, and 6, plus any two of the three tests 1, 4, and 5, as shown:

		Test	x_1	x_2	x_3	Response of faulty circuits						
						f_0	f_1	f_2	f_3	f_4	f_5	f_6
		2	0	1	0	0	0	1	0	0	0	1
		3	0	1	1	1	1	1	1	0	1	1
		6	1	1	0	1	0	1	1	1	1	1
Plus		1	0	0	1	0	0	0	0	0	1	1
		4	1	0	0	0	0	0	1	0	0	1
	or	1	0	0	1	0	0	0	0	0	1	1
		5	1	0	1	0	0	0	1	0	1	1
	or	4	1	0	0	0	0	0	1	0	0	1
		5	1	0	1	0	0	0	1	0	1	1

Now, let us examine these tests and the faults that they detect and locate. This is illustrated in Table 10.3

Table 10.3. Fault-detection and fault-location tests and the responses of the circuit with no fault and a single distinguishable fault

Test \ Fault	f_0	f_1	f_2	f_3	f_4	f_5	f_6
2	0	0	1	0	0	0	1
3	1	1	1	1	0	1	1
6	1	0	1	1	1	1	1
	[Test set {2, 3, 6} cannot detect f_3 and f_5)						
5	0	0	0	1	0	1	1
	[Test set {2, 3, 6, 5} can detect all the faults but cannot locate (distinguish) faults between f_3 and f_5]						
1	0	0	0	0	0	1	1
or 4	0	0	0	1	0	0	1
	(All the faults are detected and located)						

10.5. MACHINE IDENTIFICATION AND FAULT DETECTION EXPERIMENTS IN SEQUENTIAL CIRCUITS

As a matter of fact, the fault testing and diagnosis in sequential circuits is complicated by the presence of memory. There have developed two distinctly different approaches to the problem of fault detection in sequential circuits. The first approach is called the *circuit-test approach*, which assumes that the experimenter has an exact knowledge of the circuit realization and each fault that can occur. The second approach is called the *transition-checking approach,* which assumes no knowledge whatsoever of the circuit realization but does assume knowledge of the desired transition.

The fault-detection checking experiment can be logically divided into three phases:

(1) the initialization phase,

(2) the state identification phase, and

(3) transition verification phase.

These tasks cannot be accomplished without using special test sequences.

10.5.1. Fault Detection

A general procedure for deriving the shortest sequence of input symbols for detecting permanent faults in synchronous sequential circuits is best illustrated through the use of an example.

Example 10.2

Consider the DFF realization of the serial binary adder shown in figure 8.2. Suppose that an experiment is to be derived for detecting the following faults:

1. s-a-0 fault at location a.
2. s-a-1 fault at location b.
3. s-a-0 fault at location c.
4. s-a-0 fault at location d.
5. s-a-1 fault at location e.
6. s-a-1 fault at location f.

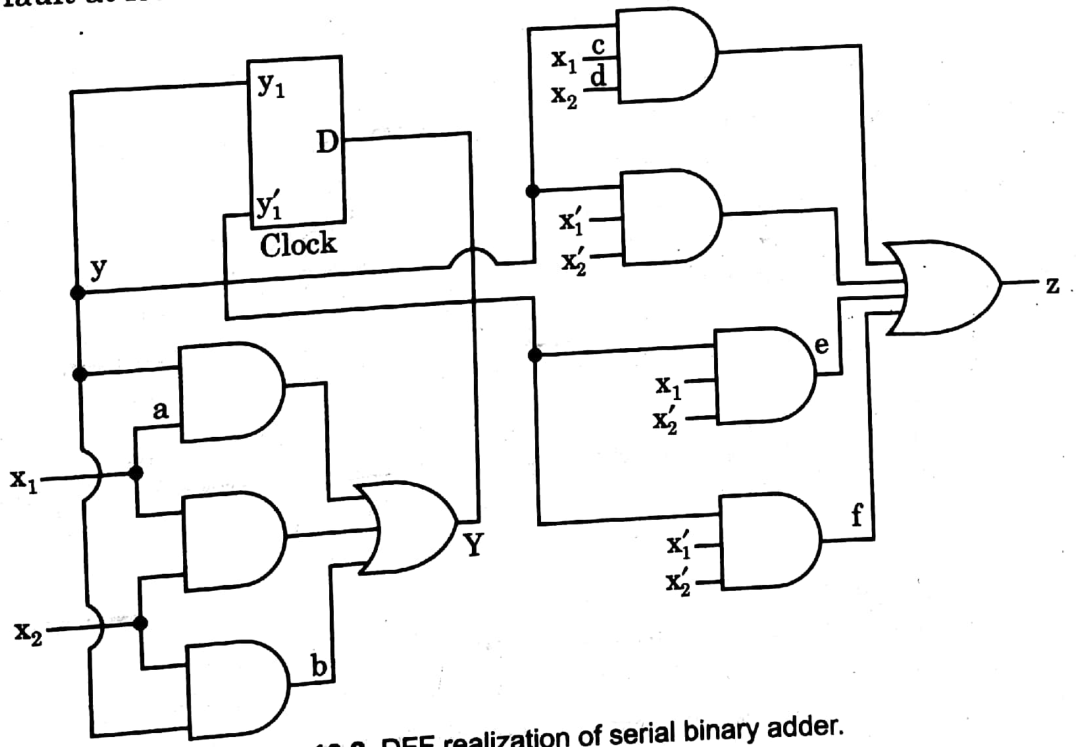

Fig. 10.2. DFF realization of serial binary adder.

For convenience, we shall denote these six faults, respectively, by a_0, b_1, c_0, d_0, e_1, and f_1.

We have

$$Y = z_1 x_2 + x_1 y + x_2 y$$

$$z = x_1 x_2 y + x'_1 x'_2 y + x_1 x'_2 y' + x'_1 x_2 y'$$

The initial state of the machine is assumed to be q_0 or $y = 0$.

10.5.2. Fault Location

After having discussed the fault-detection problem, we now turn to the fault-location problem. If the output sequences of the faulty machines obtained from the fault-detection test are distinct, we not only can tell whether the machine has any of the prescribed faults, but we can also determine which fault occurred from the output sequence obtained. In this case, no fault-location problem need be considered. However, in the case where some or all of the output sequences of the faulty machines obtained from the fault-detection test are not distinct, additional tests are needed to identify the fault.

The procedure for deriving the optimum test sequence to locate the faults that cannot be distingushed by the fault-deteotion test is very similar to the one for fault detection.

10.6. DISTINGUISHING EXPERIMENTS

Basically, we can derive effective experiments for solving the three state and machine identification problems stated previously. The problem of identifying the initial state of a sequential machine can be solved by constructing a *distinguishing sequence.*

Definition

Ah input sequence $\tilde{x}_d$ is said to be a distinguishing sequence (DS) or diagnosing sequence for a machine M = (Σ, Q, Z, δ, λ) if the output response of M to $\tilde{x}_d$ is different for each initial state.

A distinguishing sequence is obtained from the distinguishing tree, which is a terminated successor tree obtained from a successor tree by stipulating the following termination rules :

Rule 1

A kth-level branch b becomes terminal if the kth-level UV associated with b is identical to a UV of a level less than k. When two or more UV's of kth level are identical, all except one of them may be deleted.

Rule 2

A kth-level branch b becomes terminal if the kth-level UV associated with b is a homogeneous UV.

Clearly, this rule is based on property 1—that if such a situation occurs, we will not be able to distinguish the initial state by observing the output sequences of the machine; thus we should abandon this part of the successor tree by terminating it. The most important termination rule is the third one.

Rule 3

A kth-level branch *b* becomes terminal whenever (the first time such situation occurs) the kth-level UV associated with *b* is a simple UV. When such UV occurs, the complete procedure may be terminated. The DS is the input sequence corresponding to- the path from the initial uncertainty to this simple UV.

10.7. HOMING EXPERIMENT

By slightly modifying the procedure for identifying the initial state of a sequential machine, we can design an experiment for identifying the final state of a sequential machine without knowing its present (initial) state. The final state of a sequential machine is identified by a homing sequence, which is defined as follows.

Definitioin

An input sequence $\tilde{x}_h$ is said to be a homing sequence (HS) for a machine M = (Σ, Q, Z, δ, λ) if its final state can be determined uniquely from the response to $\tilde{x}_h$ irrespective of the actual initial state of the machine.

A homing sequence is derived from a homing tree, which is another terminated successor tree. The termination rules for constructing a homing tree are very similar to those for constructing a distinguishing tree. They are:

Rule 1

The first termination rule is the same as rule one, to avoid unnecessary duplication of the uncertainty vectors and branches in the successor tree.

Rule 2

This is the main termination rule. A kth-level branch b becomes terminal whenever (the first time such situation occurs) the kth-level uncertainty vector contains only singleton groups and groups consisting of one state with duplicates.

Glossary

- **Asynchronous :** In digital circuits, asynchronous meaning that operations are not executed in step with the clock.
- **Set condition :** In a flip-flop, the normal output (Q) has been set to 1.
- **Synchronous :** In digital circuits, meaning that operations are executed in step with the clock.
- **Reset condition :** In a flip-flop, the normal output (Q) has been reset or cleared to 0.
- **Sequential logic :** A logic circuit whose logic states depend on asynchronous and synchronous inputs. Exhibit memory characteristics.

Summary

- In recent years, the development of integrated-circuit technology has accelerated rapidly; MSI and LSI techniques promise to make today's functional-level devices tomorrow's (even today's) basic components.
- The problem of fault testing and diagnosis consists of the follwing two subproblems:
  1. The fault-detection problem
  2. The fault-location problem.
- A number of basic analytic and heuristic models, including the fault-table method, the path-sensitizing and equivalent-normal-form (ENF) method, the Karnaugh map and tabular method, the ENF-Karnaugh map method, the Boolean difference method, and the SPOOF method are main fault models.
- The fault-table method is the most classic approach to the problem. It is completely general and always yields a minimum set of diagnostic tests. However, it suffers from the fact that it requires a very large fault table to be constructed. To overcome the problem of not requiring the construction of a very large fault table, the concept of path sensitizing is used.
- After a digital circuit is designed and built, it is always desirable to know whether the circuit is constructed without any faults. If it is properly constructed and in use, it may be disabled by almost any internal failure. The process of applying tests and determining whether a digital circuit is fault-free or not is generally known as fault detection.
- If a known relationship exists between the various possible faults and the deviations of output patterns, it is possible to identify the failures and to classify them (at least) within the smallest possible set of components. This process is termed fault location.
- Fault diagnosis is generally referred to as the composite of both the above processes.
- The diagnostic techniques of digital systems have progressed from the state of testing the operation codes of the machine instruction set in the early days to the current hardware-assisted software aids for speedy determination and identification of faulty elements.
- Testing strategies generally depend on the system design and the architecture. Generally, the diagnostic engineer partitions the system into levels of hierarchy (systems, functional subsystems, modules, chips, etc.) and uses these levels in an organized fashion to isolate faults. Test points and the like provide mutual isolations among the partitions at various levels and help to reduce the size and time of testing.
- A fault-detection test set is said to be minimal if it is a minimal set that can detect the existence of each of the faults under consideration. A fault-location test set is said to be minimal if it is a minimal set that can locate each of the faults under consideration to the smallest identifiable part of the logic circuit.
- As a matter of fact, the fault testing and diagnosis in sequential circuits is complicated by the presence of memory. There have developed two distinctly different approaches to the problem of fault detection in sequential circuits.

- The fault-detection checking experiment can be logically divided into three phases:
  (1) the initialization phase,
  (2) the state identification phase, and
  (3) transition verification phase.
  These tasks cannot be accomplished without using special test sequences.
- By slightly modifying the procedure for identifying the initial state of a sequential machine, we can design an experiment for identifying the final state of a sequential machine without knowing its present (initial) state. The final state of a sequential machine is identified by a homing sequence.

Short Questions with Answers

Q.1. What is meant by fault detection and location?

Ans. In recent years, the development of integrated-circuit technology has accelerated rapidly; MSI and LSI techniques promise to make today's functional-level devices tomorrow's (even today's) basic components.

Q.2. What are various fault models for combinational and sequential circuits?

Ans. A number of basic analytic and heuristic models, including the fault-table method, the path-sensitizing and equivalent-normal-form (ENF) method, the Karnaugh map and tabular method, the ENF-Karnaugh map method, the Boolean difference method, and the SPOOF method are main fault models.

Q.3. What is meant by Homing experiment?

Ans. By slightly modifying the procedure for identifying the initial state of a sequential machine, we can design an experiment for identifying the final state of a sequential machine without knowing its present (initial) state. The final state of a sequential machine is identified by a homing sequence.

Review Questions

1. Explain about fault detection and location.
2. What are various fault models for combinational and sequential circuits? Explain.
3. Explain the process of fault detection in combinational circuits.
4. Explain about the fault-table model.
5. Explain about Homing experiment.

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