COMPETITIVE ANALYSIS FOR AUTOMOTIVE CPU MARKET

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1 Table of Contents

2 Background - Automotive chip market

2.1 How is the auto market changing?

The paradigm shift to software defined vehicles (SDVs) and vehicle electrification has driven automotive OEMs towards increasingly demanding software on automotive vehicles. With promises and growing availability for consumer L3 ADAS and above vehicles, the onboard compute requirements on these vehicles continues to scale. As North America, Asia and Europe hope to see mass adoption of higher levels of ADAS and EVs in the coming years, OEM's and Tier 1's will look to prepare for the upcoming demand.

2.1.1 Use of Semiconductors in Automotive industry

ADAS and Infotainment play crucial roles in modern, electrified and semi-autonomous vehicles. Automotive CPUs are necessary for the demands of ADAS, infotainment as well as other critical vehicle functionality.

2.1.1.1 Projections

The ongoing electrification, shift towards SDVs and demand for higher levels of ADAS continues to grow, the demand for automotive AI-compute continues to grow. Per BCG, by 2030, 58% of light vehicle production will include L2 or greater ADAS. Per McKinsey, 68% of automotive semiconductor specialists report that automotive OEMs would favor shallow-verticalization[1]. Internal and external projections point towards 9% annual growth and an estimated TAM of $100 billion USD by 2030e for the automotive semiconductor industry.

Continuous increase in semiconductor consumption per automobile. Semiconductor consumption for level 5 (L5) ADAS electric vehicles (EVs) will be approximately **$2500.00 in 2030** compared to approximately $435.00 for ICE automobiles in 2020.

2.2 Barriers to entry

The automotive CPU market poses high entry barriers due to the functional safety (FuSa) requirements such as ISO26262 compliance, ensuring processors meet safety-critical reliability (ex. ASIL certification). The monetary investment required for FuSa certification can be in the millions of dollars and adds additional development time. These expenses stem from additional FuSa engineering efforts, audits, fault systems and testing/validation. Additionally, the required reliability and long-term support for automotive lifespans (10+ years) can pose challenges.

While FuSa requirements extend the development timeline, vendors offering mature and pre-certified IP can significantly reduce time-to-market for their customers. Pre-certified IP provides the necessary safety features, extensive validation and FuSa compliance alleviating the burden on automotive OEM's/T1's.

1. Shallow verticalization: OEM defines high level technical requirements, collaborates with IDM/3rd party design services and then sends design to foundry

3 Current Market Research

3.1 Current automotive chip supply chain

Requirements given by OEM to Tier 1. Tier 1 translates the requirements and sends to Tier 2 - Chip makers. From a semiconductor point of view, the supply chain is as follows:

- **OEM**

  Example BMW, Honda, Toyota

- **Tier 1 - Systems Integrators**

  These are the companies that integrate the chips from Tier 2 (chip) designers with sensors and develop systems/platforms for the OEMs. Examples - Bosch, Denso, LG Electronics.

- **Tier 2 - Component Suppliers**

  Chip - The actual SoC designers like NVIDIA, Qualcomm, Mobileye, Samsung, BOS Semi, Texas Instruments, Soc Designers from China - Huawei, Baidu, Horizon Robotics, Black Sesame

  IP - ARM, Sifive, Ventana

- **Tier 3 - Material and Tooling Suppliers**

  Companies providing raw materials, tooling or manufacturing technologies to Tier 1 and 2 suppliers. Examples - TSMC

3.2 Current CPU Offerings in Automotive Market

3.3 Automotive CPU IP Offerings

Vendor	TT	Arm	Arm	Arm	SiFive	SiFive
Product	Ascalon D8 Auto	A78AE	A720AE	Neoverse V3AE	S7-AD	X280A
ASIL Level	B/D	B/D	B/D	B/D	B/D	B/D
DMIPS/MHz	11.46	11.36 (est)	13.64 (est)	18.18 (est)	3.32*	3.25*
Process Node	SF4	N7	N3	N4	?	?
Release Date	2025	Sept 2020	Mar 2024	Mar 2024	Sept 2022	Sept 2022

Table 1: Automotive CPU IP Offerings

*Due to lack of benchmark public results, non-automotive IP versions' benchmarks were used (S7, X280)

3.3.1 Arm

Arm dominates the automotive market, with its technology powering over 85% of In-vehicle Infotainment (IVI) systems and more than 50% of ADAS systems (Source). Similar to TT, ARM licenses IP through two different license options: 1. Architecture License (analogous to TT's Innovation License) where customers can use and design custom implementations of the ARM ISA. 2. Processor IP License (analogous to TT's Standard License) where customers can use existing IP offerings without modification rights. Arm generates revenue from every chip based on per chip and/or volume based royalties. ARM provides different access packages to allow potential customers to explore and design with ARM IP and low to no cost. ARM Flexible Access provides access to entry and lower level IP, with licensing fees due at tapeout. ARM Total Access provides 3 tiers of IP packages, ranging from entry level to high performance IP.

The relevant Arm CPU IP offerings are the A78AE, A720AE and Neoverse V3AE which all target high-end ADAS/IVI applications. The A78AE has been certified by TUV SUD for hardware integrity (up to) and systemic capability ASIL D. The A720AE and Neoverse V3AE are yet to be certified but target ASIL B diagnostic/ASIL D systemic applications. The A78AE and A720AE offerings focus on general purpose compute, basic ADAS and IVI where a balance between performance and power consumption is required. The Neoverse V3AE targets parallel compute-focused applications (ML/AI, data processing).

3.3.2 SiFive

SiFive sells their IP through two primary licensing options, the Core IP Licenses and the DesignShare. The Core IP Licenses allows customers to integrate pre-existing RISC-V CPU cores without modifications into the desired product. DesignShare allows companies to access IP during the design phase, deferring the licensing fees until production. SiFive offers varying levels of access to their IP. For example, customers can use SiFive Core Designer to access pre-validated IP or those with specific requirements can choose to use SiFive's design.

The relevant SiFive automotive CPU offerings include the S7-AD and X280-A which focus on high-performance embedded and vector workloads respectively. The S7-A is aimed at targeting a similar market to the Cortex-A series and is capable of ASIL D systemic and diagnostic. The X280-A is targeted towards the high-performance automotive compute market and is aimed at ASIL D systemic/ASIL B diagnostic. Of note, SiFive received ISO 21434 certification for the S7-AD.

3.3.3 Other RISC-V Considerations

3.3.3.1 Andes Technology

Andes Technology was considered as a RISC-V IP vendor however, their (publicly announced) automotive IP: AndesCore D23-SE, N25F-SE and D45-SE are not targeting ADAS/IVI/high performance applications. Their auto portfolio targets ECU/DCU, battery management, ABS, power steering and other similar applications. The D45-SE is their highest performance core but is a 32-bit in-order processor.

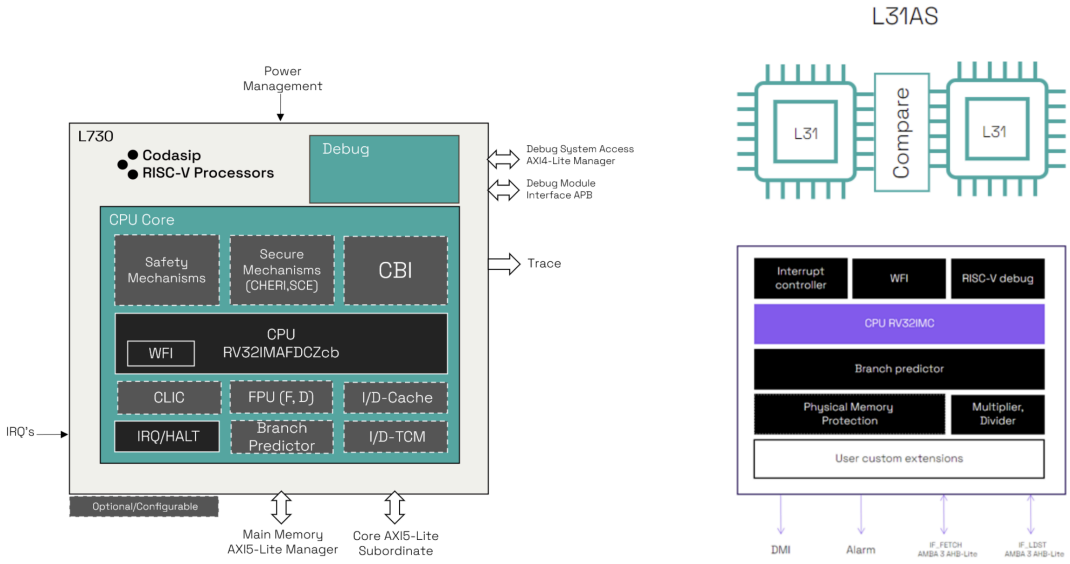
3.3.3.2 Ventana Microsystems

Ventana Microsystems was also considered, Veyron V2 being a high performance RISC-V CPU. Having the following specifications: 15 wide, out of order pipeline, 3.6GHz, built on 4nm, 32 cores/cluster (multi-cluster scaling up to 192 cores), 128MB of shared L3 cache/cluster. Ventana does mention they are

building ISO26262 grade products but it is unclear if that would be a variant of the Veyron V2 or an entirely different product.

3.3.3.3 Codasip

Codasip's RISC-V automotive cores include the L730, a high performance embedded core and L31AS a 32bit core. The L730 has compliance up to ASIL D and has additional security features and has pre-verified configurations available. The L31AS is an in-order, 3 stage, single issue RISC-V core and has ASIL B certification (TUV SUD).



Figures 1 & 2: Codasip L730 and L31AS block diagrams

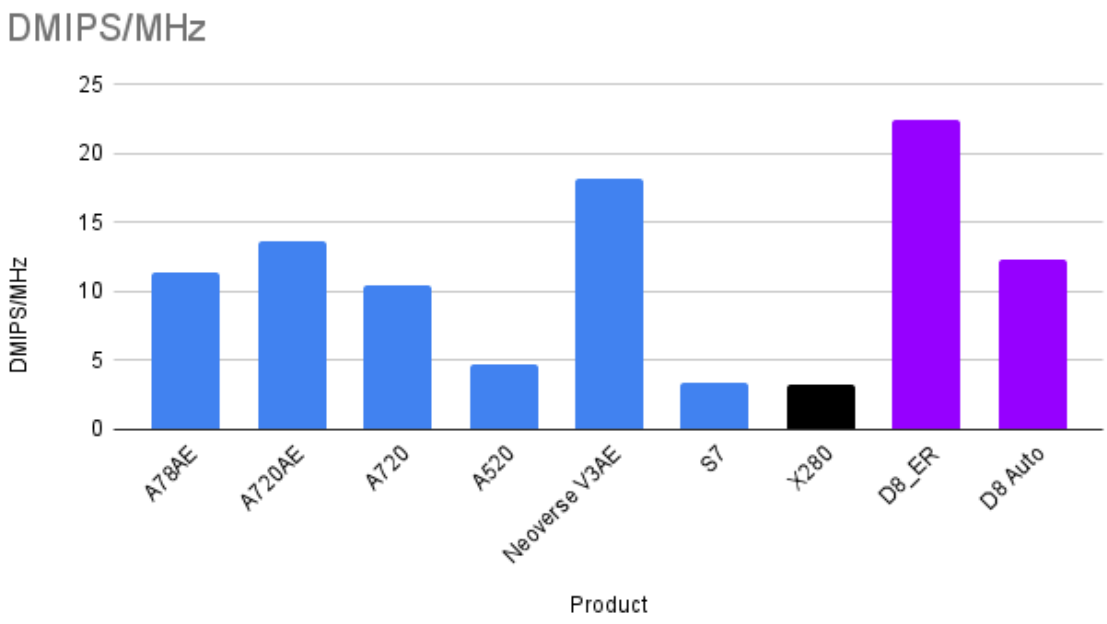


Figure 3: DMIPS/MHz comparison

3.4 Automotive Platform Offerings

Vendor	Nvidia	Nvidia	Qualcomm	Tesla	Renesas	Mobileye
Product	Orin X	Thor X	SA8650P	HW4	R-car X5H	Eye Ultra
CPU	A78AE	Neoverse V3AE	Kryo (X3 + A55)	20xA72	A720AE	12x MIPS RISC-V
ASIL Level	B/D	B/D	B/D	N/A	B/D	B/D
DMIPS/MHz	11.36 (est)	18.18 (est)	N/A	N/A	13.64 (est)	N/A
DMIPS	240K	~500K	230K	~237K	1000K	N/A
Target Application (ADAS level)	IVI/ADAS (L2)	IVI/ADAS (L3+)	IVI/ADAS (L2/L3)	IVI/ADAS (L2/L3)	IVI/ADAS (L2++/L3/L4)	ADAS (L4)
Process Node	N7	N4	4nm	SF7	N3	5nm
Release	2022	2024	2024	2023	2024	2025

Table 2: Automotive Platform Offerings

3.4.1 Nvidia

The two notable Nvidia automotive platforms are the Drive Orin (2022) and the Drive Thor (2024). The Drive Orin uses Arm A78AE core (~240K) DMIPS and has an Ampere-based GPU. The Drive Thor uses Neoverse V3AE cores (~500K DMIPS) and has a Blackwell-based GPU, which according to Nvidia can provide 1000 TOPS positioning it well for the demands for ADAS/IVI needs in the years to come. The Drive software stack, CUDA and simulation tools provide vendors with a mature and wide ecosystem.

3.4.2 Qualcomm

Qualcomm's product offerings include SoCs tailored for infotainment and ADAS through its Snapdragon Cockpit and Ride platforms. Qualcomm's SoCs are custom built on top of ARM architecture. Qualcomm's platform offerings are targeting a similar market as Nvidia's platforms. The 8650 chip's reported price is approximately 30% lower per unit compared to the Nvidia Orin X, making the Qualcomm's pricing between Nvidia and Horizon Robotics.

3.4.3 Mobileye

Intel's Mobileye Eye Ultra is a SoC targeting high-end automotive market and will be particularly interesting to follow as it utilizes 12 RISC-V CPU cores. The other components in the SoC are as follows: Arm GPU, ARM DSP, SIMD cores, VLIW cores and 16 AI cores (176 TOPS). There are relatively limited details about what exact Arm IP and what RISC-V cores are being used.

3.4.4 Chinese CPU offerings

3.4.5 CN Region Automotive Compute Offerings

Vendor	Horizon Robotics	AutoChips	SiEngine	UNISOC	Rockchip	SemiDrive	Black Sesame
Product	Journey 6P	AC8025	Dragon Eagle One	A7870	RK3588 M	X9U	HuaShan A1000 Pro
CPU	A78	2xA76 + 6xA55	4xA76 + 4xA55	1xA76 + 3xA76 + 4xA55	4xA76 + 4xA55	6xA55	A55
Frequency	N/A	N/A	A76@2.4GHz	1xA76 @2.7GHz/ 3xA76 @2.3GHz/ 4xA55 @2.0GHz	A76@ 2.2GHz/ A55@ 1.7GHz	2.0GHz	1.5GHz
ASIL/Safety Level	D	B	AEC-Q100	AEC-Q100	AEC-Q100	B	D
DMIPS/MHz	~11.4	N/A	4.7	5.3	6.4	3.6	2.5
DMIPS	410K	60K	90K	93K	100K	100K	60K
Target Application (ADAS level)	ADAS/IVI	IVI	IVI	IVI	IVI	IVI	IVI
Process Node	7nm	N/A	7nm	6nm	8nm	16nm	16nm
Release	April 2024 (Announced)	July 2024	Dec 2023	Mar 2023	2022?	April 2021	April 2021

Table 3: Chinese Automotive CPU's

Based on vendor announcements and data, many of the domestic automotive CPU offerings in China are using some combination of the A76 and A55 primarily targeting IVI usage. However, from preliminary customer engagements, the potential customers are looking to upgrade their solution from a Nvidia Orin solution (A78AE) and are looking for an alternative that is at least as competitive with the A720AE.

3.4.6 Horizon Robotics

Horizon Robotics provides a full range of platform solutions for ADAS/IVI, with their latest CPU in the Journey 6 line ranging from 20K to 410K DMIPS with production planned to start 2025. The Journey 6P is the highest end offering at 410K DMIPS, approximately 11.4DMIPS/MHz at a frequency of 2.3-3GHz. The Journey 6 will likely be used for L2++/L3/L4 ADAS. While the Journey 6 has not yet been ASIL certified, the Journey 5 has been certified as an ASIL-B Ready product.

3.4.7 SemiDrive

SemiDrive's product offerings include SoC's tailored for infotainment and ADAS with the X9 and V9 SoC's. SemiDrive offers slight variants of the X9 and V9 with varying performance however all variants with publicly available data are powered with 6 A55 cores at 2.0GHz with performance ranging from 36K to 100K DMIPS. Given that the compute capabilities of the X9 series are relatively limited in comparison, it is likely only used in lower level of ADAS and infotainment. Both the X9 and V9 lines have been ASIL-B certified according to SemiDrive.

3.4.8 Black Sesame

Black Sesame's Huashan A1000 (2021) and A2000 (announced Dec 30, 2024) are their automotive compute product lines targeting ADAS applications. Both product lines have Lite, Standard and Pro versions which according to promotional material, target vision with single input, vision with multi-input and vision with mulit-input along with high-level security in the Lite, Standard and Pro models respectively. The A1000 Pro uses the A55 at 1.5GHz delivering relatively low performance at 60K DMIPS. The A2000 line steps up to use 16 cores of the A78 with unknown benchmarks at the time of announcement.

4 Tenstorrent Ascalon IP

4.1 Technical Specifications

The current baseline D8, D8 global and D8 auto configurations specification targets are as follows:

Specification	D8	D8 Global	D8 Auto
Frequency	2.25GHz (SF4+)	2.25GHz (SF4)/2.45GHz (N7)	2-2.4GHz
SpecINT2006	18/GHz	18/GHz correlated	TBD
DMIPS/MHz	12.38/MHz	TBD	11.46/MHz

Table 4: Tenstorrent Ascalon D8 Comparison

The current base D8 auto IP is to serve as an IP that can be used as a base die and in chiplet applications for general compute, ADAS and IVI purposes. Based on internal projections, we're expecting roughly a 5-10% increase on SPEC2K6 performance annually.

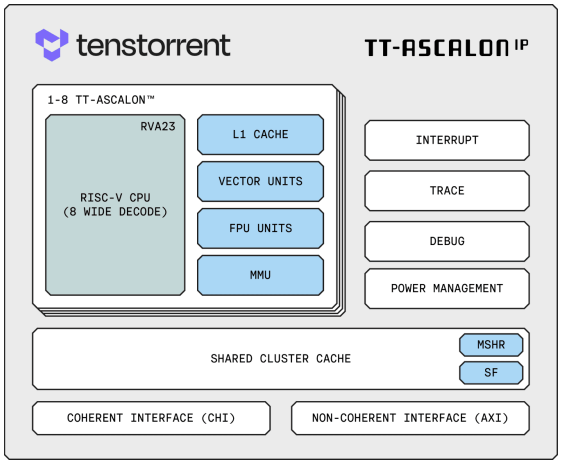


Figure 4: TT-Ascalon IP block diagram.

The current Ascalon D8 PPA projection while running Dhrystone is as follows:

	4nm TT, Vdd=0.75V, T=85C
Frequency	3.2GHz
Performance	18 SPEC2K6/GHz
Core Area	Slice: 2.6mm^2 Core: 1.6mm^2
Power	Slice: 1.0 W (Dyn), 0.3 W (Leak) Core: 0.9 W (Dyn), 0.2 (Leak)

Table 5: Ascalon D8 PPA projections

4.1.1 ARM comparison/Future Projections

Based on internal projections, Tenstorrent expects roughly a 5-10% increase on SPEC2K6 performance annually. The current projections for Arm IP against Tenstorrent IP show Ascalon D8++ in 2026 being the crossover point and exceeding Arm performance. Assuming that the automotive renditions of Ascalon and Arm IP both roughly see the same performance reduction due to automotive requirements, D8++ Auto will exceed Arm Automotive performance.

Year	Arm	Spec2k6/GHz	Tenstorrent	Spec2k6/GHz	Spec2k6/GHz Δ (TT : ARM)
2020	A78	14.2	N/A	N/A	N/A
2023	A720	17.2	N/A	N/A	N/A
2025	A2025	~20-21	D8	18	-2
2026	A2026	~21-22	D8++	>22	0-1
2027	A2027	~22-23	D8+++	>25	2-3

Table 6: SpecINT2K6 projections for Arm IP against Tenstorrent IP

5 Ecosystem Considerations

While performance, power and cost are all important metrics for competitiveness, the greater RISC-V and Tenstorrent Software ecosystem maturity are necessary to push TT products into a competitive place.

Component	Details	Priority	TT	RISC-V Community	Arm	x86
GCC	Toolchain	P0	Initial tt-ascalon-d8 support upstream	Yes, open source	Widely Used	MinGW, Cygwin
LLVM	Toolchain	P0	Initial tt-ascalon-d8 support upstream	Yes, open source	Yes	Yes
Auto Grade Linux (AGL)	OS	P0	Ø	Yes	Yes	Yes
QNX	OS/ Hypervisor	P0	Ø for both		Yes	Yes
Xen	Hypervisor	P0	Ø	RISC-V Arch in git repo	Enterprise, servers	data center, cloud, server
Android	OS	P1	Ø	Yes*	Yes	Yes

Table 7: Notable software ecosystem components for early automotive adoption and development

5.1 Software Ecosystem

One of ARM’s major value propositions lies in its mature and extensive software ecosystem, developed over decades with industry leaders. This ecosystem includes but is not limited to, automotive tailored OS’s like QNX, AGL as well as compatibility with development tools, compilers and other libraries. The ecosystem's maturity accelerates development timelines and ensures reliability and scalability.

5.1.1 Operating Systems

5.1.1.1 Automotive Grade Linux

AGL is an open-source OS designed specifically for automotive use-cases, built on the Linux kernel and serves as a platform for developing a wide range of vehicle software application including infotainment and ADAS. AGL offers a shared framework and API’s, allowing interoperability and scalability across vehicle models and OEMs.

5.1.1.2 Android Automotive OS (AAOS)

With many OEM's including Hyundai, Volvo, Polestar, GM and Rivian using or building their software on top of AAOS, having a RISC-V port will be a critical enabler for customers aiming to utilize RISC-V automotive processors. Current efforts for Android RISC-V ports have been led by Google, Alibaba and open-source contributions. Recent contributions have been relatively limited as Google announced in May 2024 they removed experimental RISC-V support from the Android Open Source Project.

5.1.2 Hypervisors

Hypervisors have become a critical role in the automotive software ecosystem by enabling the consolidation of software domains-such as infotainment, ADAS and vehicle control onto a single hardware solution. Xen Hypervisor being open-source provides flexibility and customization for diverse automotive use cases, aligning well with Tenstorrent's philosophy. QNX Hypervisor is purpose built for safety-critical environments providing ISO26262 support.

5.2 Hardware Ecosystem

ARM has a comprehensive IP portfolio that provides customers with a complete ecosystem of solutions to address all their hardware design needs. This ecosystem goes beyond a range ofCPU/NPU/GPU IP offerings and also encompasses interconnects and system-level IP. Additionally ARM has a robust network of partners, software and tool support and pre-validated design kits, minimizing integration work for customers.

A complete Tenstorrent hardware ecosystem is still yet to be fleshed out, requiring system IP and interconnect fabric to create a fully functional SoC that is suitable for production. With the long-term strategy for TT to become a "one-stop shop" for automotive IP, a complete hardware ecosystem is a necessity.

FINAL NOTES

Based on early engagements, customers are looking to migrate from an A78AE based Nvidia platform (Orin) to a newer more powerful product. **As such, the Tenstorrent (2025/26) automotive CPU product offering must clear the A78AE in performance, be competitive with A720AE** (potentially the Neoverse V3AE through a chiplet solution). Internal projections for Tenstorrent and Arm performance would show D8 Auto being at least on par with A720AE with D8++ generations exceeding the Arm future equivalent in 2026. One of Arm's major value propositions is their vast and mature software and hardware ecosystem as such, **Tenstorrent needs to invest into internal hardware ecosystem development and RISC-V software ecosystem in order to move Ascalon Auto products** (and non auto products) **in a competitive space.**

Vendor	TT	Arm	Arm	Arm	SiFive	SiFive
Product	D8 Auto	A78AE	A720AE	Neoverse V3AE	S7-AD	X280A
Users/ Customers	TBD	Nvidia Orin, Horizon Robotics J6P, AMD Versal Prime 2	Renesas X5H,	Nvidia Thor,	?	?
L1/L2/L3 Cache	64KB I-Cache, 256 D-Cache/ 512KB (configurable)/ 2MB	32KB-64KB/ 256KB-512KB/ Opt, 512KB-4MB	32KB-64KB/ 256KB-1024KB/ Opt, 512kB-4MB	64KB/ 2MB-3MB/ Ø	32KB/ Opt, 128KB-4MB/ Ø	32KB/ 256KB/ 1-4MB
ASIL level	B/D	B/D	B/D	B/D	B/D	B/D
DMIPS/MHz	11.46	11.36	13.64	**18.18**	3.32*	3.25*
DMIPS	TBD	~240K (Nvidia Orin)	~500K (Renesas R-Car X5H)	**1000K** (Nvidia Thor)	?	?
Frequency (GHz)	2-2.4	2.3-3	~2.3	?	?	?
SpecINT2K6	18~	14.2~	17.2~	?	?	?
Process Node	SF4	7nm	3-7nm	3-4nm	?	?
Software Ecosystem Support						
Hardware Ecosystem Support						
Release Date	2025	2020 Q3	2024 Q1	2024 Q1	2022 Q3	2022 Q3

Table 8: Compiled specifications for automotive CPU offerings. Bold denotes industry leader.

Appendix

Feature	ARM A78	Ascalon-D4
I-Cache	32 KB	32 KB
Decode Width	6	4
Load/Store pipe	2 load/store, 1 load	2 load/store
D-Cache	32 KB	64 KB
Integer Pipe	4	2
Integer/Branch pipe	None	2
Branch only pipe	2	None
Vector/SIMD pipe	2 x 128-bit SIMD	1 x 256 RISC-V
ROB	160	160
Private L2	512 KB	None
Shared L2	None	2 MB
Shared L3	2 MB	None
SPEC2K6INT	12.3	11.5-12.0
Core area	1.38 mm2	0.9 mm2
Per core cluster area	1.88 mm2	1.4 mm2
4-core Cluster area	7.5 mm2	5.5 mm2
Frequency (GHz)	2.30	2.45
Performance Density	15.0 SPECINT/mm2	20.5-21.0 SPECINT/mm2
System: No system cache, 100 ns DRAM latency		
TSMC N7, Vnom=0.75/TT/85C		

Table 8: Arm A78 vs TT-Ascalon D4

	Performance (SPEC2K6/GHz)	Area (mm2)	Dynamic Power (W/GHz)	Frequency (GHz)	Performance Density (SPEC/mm2)
ARM A78	12.3	1.88	0.286	2.30	15.0
Ascalon-D4	12.0	1.40	0.280	2.45	21.0
TSMC N7, Vnom=0.75/TT/85C, Dhrystone Dynamic Power					

Table 9: Arm A78 vs TT-Ascalon D4