TT CPU Products

Decoder

Industry	Global	Core Count	L2 Cache [MB]
X - eXtreme/highest performing	N/A	8c	12m
H - High perf, mod.-high power	G - (Export Control)	6c	4m
S - Special/Small/Standard/Smart		4c	
U - Ultra low-power		2c	
P - Performance-focused			
M - Mid-range micro-controller			

HPC CPU IP

Name	Generation	Tech	Description	Type	Applications	Package	Tapeout
Ascalon	ASC	SF4X	• RVA23 RISC-V high-performance core • SPECint 2006 / GHz > 20 (w/SW opt.) • 2.5 GHz • X (D8), H (D6), S (D4), U (D2) • 8, 4, 2 core clusters	CPU IP	• CPU IP • Atlantis • Ariana	NA	
Ascalon X 8c12m			• Ascalon X • 8 cores, 12MB L2 shared cache			NA	• Atlantis • End 2025
Ascalon X 4c4m			• Ascalon X • 4 cores, 4MB L2 shared cache				

Ascalon S 4c4m			• Ascalon S • 4 cores, 4MB L2 shared cache				
Ascalon X 2c4m			• Ascalon X • 2 cores, 4MB L2 shared cache				
Ascalon H2c8m			• Ascalon H • 2 cores, 8MB L2 shared cache				
Babylon	ASC+		• SPECint 2006 / GHZ > 22 (w/SW opt.) + I$ coherency • 2.7 GHz • X (D8), H (D6), S (D4), U (D2)	CPU IP			• Aug-2026
Cyrene	ASC++		• SPECint 2006 / GHZ > 24 (w/SW opt.) + ISA features • X (D8), H (D6), S (D4), U (D2) • 3GHz	CPU IP			• Aug-2027
Callandor	CAL			CPU IP			• 2027/8
Durandal	DUR			CPU IP			• 2029

Embedded CPU IP

Name	Generation	Tech	Description	Type	Applications	Package	Tapeout
Cypress	CYP		Embedded	CPU IP			
Cypress P			• 32bit • RV32I • MA[F][D]C[B][P] • ASIL-D Capable				
Cypress M			• 64 bit • RV64I • MA[F][D]C[B][P] • ASIL-D Capable				
Juniper	JUN		Real-time	CPU IP			

Juniper			• 64 bit • RV64M • RVV 1.0 • ASIL-D Capable				

Automotive CPU IP

Name	Generation	Tech	Description	Type	Applications	Package	Tapeout
Alexandria	ASC	N3A	• ASC X + ASIL-D • 8, 4, 2 core clusters • 12, 4 MB L2 shared cache	CPU IP	• Aria		Mar-2026
ALX X 4c4m		N3A	• 4 core cluster w/4 MB shared L2 cache	CPU IP	• Aria base die • 3 x 4c clusters		
ALX X 8c12m		N3A			• Customer: Denso (??)		
ALX X 2c4m		N3A					
Ariana	ASC	SF4X	• ASC X + STL • ASIL-B (Core only, not cluster)	CPUIP			
ARI X 8c12m		SF4X	• 8 core cluster w/12 MB shared L2 cache	CPU IP	• ALX enabler		

CPU Chiplets

Name	Generation	Tech	Description	Type	Applications	Package	Tapeout
Atlantis	ASC	12nm	• ASC chip for development board • ASC X 8c12m	SoC	Dev Kit		Late 2025
Athena	ASC		• 8 RISC-V Ascalon CPU Cores • Companion CPU for Quasar • SMU (System Management Unit which includes both a Security Enclave Processor (SEP) and System	CPU Chiplet			

			Management Controller (SMC)), • PCIe • LPDDR5 subsystems, the NoC (Network on Chip) • D2D (Die-to-Die) interface to other chiplets				
Aegis		4nm	• 32 RISC-V Ascalon CPU Cores, scalable up to 128 Cores / 4 Chiplets • Feature support incl SMC, IOMMU, AIA • Non-blocking D2D Interfaces • Composable IO, MEM, CPU compute • 16 x Ascalonx8m12 clusters • Arteris cross-bar coherent fabric • Arteris meshed non-coherent fabric • 96 MB memory cache • UCIe	CPU Chiplet	• Highly Performance • RISC-V CPU ◦ Server chip ◦ HPC ◦ AI ◦ Automobile ◦ NPU		2024

Automotive Chiplet

Name	Generation	Tech	Description	Type	Applications	Package	Tapeout
Aria	ASC		Alexandria CPU IP Base Die = 3 x ALX X4c4m	Chiplet	• Customer: Bosch • EU Chasis program		
Aachen	ASC		Alexandria Base Die in a package	Chiplet			

System IP

Name	Generation	Tech	Description	Type	Applications	Package	EA

Ajanta	ASC	SF4X	System IPs included: IOMMU, APLIC	System IP	Enable Atlantis		Sept-2025
Ajanta-A (Auto)	ALX	N3A	System IPs included: IOMMU, APLIC Automotive FuSa: ASIL-D	System IP	Enable Alexandria & Aria		June-2026
Badami				System IP			Aug-2026
Calicut				System IP			Aug-2027

References:

TT Product Roadmap

https://tenstorrent.sharepoint.com/sites/PlatformArchitecture/SitePages/Project-Name.aspx