fflags									
Address	0x00	0001							
Size	32								
Reset Value	0x00	000000							
Description	Accru	Accrued Exceptions							
Field Nan	me Bit Offset Bit Width Volatile Access Reset Value Descript				Description				
nx		0 1 true			read-write	0×0		Inexact	

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
nx	0	1	true	read-write	0x0	Inexact
uf	1	1	true	read-write	0x0	Underflow
of	2	1	true	read-write	0x0	Overflow
dz	3	1	true	read-write	0x0	Divide by Zero
nv	4	1	true	read-write	0x0	Invalid Operation
rsvd325	5	27	-	WPRI	-	Reserved

frm										
Address	0x00	.0002								
Size	32									
Reset Value	0x00	000000								
Description	Roun	ding Mode								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
frm		0	3	true	read-write	0x0	Rounding Mode			
rsvd323	3 29		29	-	WPRI	-	Reserved			

fcsr	fcsr								
Address	0x00	03							
Size	32								
Reset Value	0x00	000000							
Description	FP co	ontrol and sta	atus register						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description		
nx		0	1	true	read-write	0x0	Inexact		
uf		1	1	true	read-write	0x0	Underflow		
of		2	1	true	read-write	0x0	Overflow		
dz	dz		1	true	read-write	0x0	Divide by Zero		
nv		4	1	true	read-write	0x0	Invalid Operation		
frm 5		5	3	true	read-write	0x0	Rounding Mode		
reserved		8	24	true	read-write	0x0	Reserved Bits		

vstart	
Address	0x0008
Size	64
Reset Value	0x000000000000
Description	Vector start position

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
vstart	0	8	true	WARL	0x0	Vector Start Index
rsvd648	8	56	-	WPRI	-	Reserved

vxsat									
Address	0x00	x0009							
Size	32								
Reset Value	0x00	000000							
Description	Fixed	l-point satura	ate flag						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description		
vxsat		0	1	true	WARL	0x0	Vector Fixed-Point Saturation Flag		
rsvd321	1 31		31	-	WPRI	-	Reserved		

vxrm									
Address	0x00	4000A							
Size	32								
Reset Value	0x00	000000							
Description	Fixed	l-point round	ing mode						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description		
LUVERO .		0	2	truo		0x0	Vector Fixed-Point Rounding Mode		
vxrm	0		Z	true	WARL	UXU	Register		
rsvd322		2	30	-	WPRI	-	Reserved		

vcsr	sr								
Address	0x00	<000F							
Size	32								
Reset Value	0x00	000000							
Description	Vect	Vector control and status register							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description		
vxsat		0	1	true	WARL	0x0	Vector Fixed-Point Saturation Flag		
wrm		1	2	truo	WARL	0x0	Vector Fixed-Point Rounding Mode		
vxrm			2	true	WANL	UXU	Register		
rsvd323 3		3	29	-	WPRI	-	Reserved		

seed									
Address	0x00	0015							
Size	32								
Reset Value	0x40	000000							
Description	Seed	Seed CSR.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description		
entropy	0 16		16	true	WARL	0x0			

custom	16	8	true	WARL	0x0	
rsvd_29_24	24	6	true	WARL	0x0	
opst	30	2	true	WARL	0x1	

sstatus	
Address	0x0100
Size	64
Reset Value	0x00000020000000
Description	Supervisor status register.

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
sstatus_wpri_0	0	1	false	WPRI	0x0	WPRI
sie	1	1	false	WARL	0×0	interrupts are globally enabled when
sie	1	1	iaise	WARL	0.00	in S-mode
sstatus_wpri_1	2	3	false	WPRI	0x0	WPRI
spie	5	1	false	WARL	0×0	interrupt-enable bit active prior to
Spie	3	1	Taise	WAILE	0.00	the trap in S-mode
						Endianness: non-instruction-fetch
ube	6	1	false	WARL	0x0	memory accesses made from
						U-mode
sstatus_wpri_2	7	1	false	WPRI	0x0	WPRI
spp	8	1	false	WARL	0×0	previous privilege mode before
3pp	O	1	laise	WAILE	0.00	entering S-mode
VS	9	2	false	WARL	0x0	status of the vector extension state
sstatus_wpri_3	11	2	false	WPRI	0x0	WPRI
fs	13	2	false	WARL	0×0	status of the floating-point unit state
13			laise	WAILE	0.00	(Must become F-ext is implemented)
xs	15	2	false	WARL	0x0	status of additional user-mode
X			luisc	VV/U(L	OXO .	extensions and associated state
sstatus_wpri_4	17	1	false	WPRI	0x0	WPRI
sum	18	1	false	WARL	0x0	permit Supervisor User Memory
34111	10	_	luise	VV/ II (L	OXO .	access
mxr	19	1	false	WARL	0x0	Make eXecutable Readable
sstatus_wpri_5	20	12	false	WPRI	0x0	WPRI
uxl	32	2	false	WARL	0x2	XLEN for U-mode
sstatus_wpri_6	34	29	false	WPRI	0x0	WPRI
sd	63	1	false	WARL	0x0	Summary of FS/VS/XS

sie											
Address	0x01	x0104									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Supervisor interrupt-enable register.										
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description									

rsvd00	0	1	-	WPRI	-	Reserved
ssie	1	1	true	WARL	0x0	Interrupt-enable bit for supervisor-level Software Interrupts
hard0_0	2	2	true	WARL	0x0	Hardwired 0
rsvd44	4	1	-	WPRI	-	Reserved
stie	5	1	true	WARL	0x0	Interrupt-enable bit for
Stie	3	1	tiue	WARL	0.00	supervisor-level Timer Interrupts
hard0_1	6	2	true	WARL	0x0	Hardwired 0
rsvd88	8	1	-	WPRI	-	Reserved
seie	9	1	true	WARL	0×0	Interrupt-enable bit for supervisor-level External Interrupts
hard0_2	10	3	true	WARL	0x0	Hardwired 0
nardo_z	10	3	tiue	WAILE	0.00	Interrupt-enable bit for
Icofie	13	1	true	WARL	0x0	supervisor-level Local Count Overflow Interrupts
rsvd6414	14	50	-	WPRI	-	Reserved

stvec										
Address	0x01	x0105								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Supe	rvisor trap ha	andler base a	address.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
mode 0		0	1	false	WARL	0x0	Allows mode 0 (base only) or mode 1			
mode_o		O	1	laise	WARL	0.00	(vectored)			
mode_1		1 1 false WARL 0x0 Modes >= 2 are not allowed								
basesxlen12v	varl	2	62	false	WARL	0x0	Top SXLEN-2 bits of BASE			

scounteren

Address	0x01	0x0106								
Size	32	32								
Reset Value	0x00	000000								
Description	Supe	rvisor counte	er enable.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
су		0	1	false	WARL	0x0	Cycle Counter Enable			
tm		1	1	false	WARL	0x0	Time Counter Enable			
ir		2	1	false	WARL	0x0	Instruction Retired Counter Enable			
h m m 2		2	1	falas	WADI	00	Hardware Performance Monitoring			
hpm3	3		1	false	WARL	0x0	Counter 3 Enable			
hnm4	4 1 false		falso	WADI		Hardware Performance Monitoring				
hpm4 4		4	1	false	WARL	0x0	Counter 4 Enable			

						1
hpm5	5	1	false	WARL	0x0	Hardware Performance Monitoring
						Counter 5 Enable
hpm6	6	1	false	WARL	0x0	Hardware Performance Monitoring
<u> </u>						Counter 6 Enable
hpm7	7	1	false	WARL	0x0	Hardware Performance Monitoring
	·					Counter 7 Enable
hpm8	8	1	false	WARL	0x0	Hardware Performance Monitoring
			Tuise		oxe .	Counter 8 Enable
hpm9	9	1	false	WARL	0x0	Hardware Performance Monitoring
			laise			Counter 9 Enable
hpm10	10	1	false	WARL	0x0	Hardware Performance Monitoring
принто			laise	WARL	0.00	Counter 10 Enable
h n no 1 1	11	1	false	WARL	0×0	Hardware Performance Monitoring
hpm11	11	1	laise	WARL	000	Counter 11 Enable
h	12	,	£-1	MADI	00	Hardware Performance Monitoring
hpm12	12	1	false	WARL	0x0	Counter 12 Enable
. 13	12	_	6.1	WARI		Hardware Performance Monitoring
hpm13	13	1	false	WARL	0x0	Counter 13 Enable
		_				Hardware Performance Monitoring
hpm14	14	1	false	WARL	0x0	Counter 14 Enable
		_				Hardware Performance Monitoring
hpm15	15	1	false	WARL	0x0	Counter 15 Enable
						Hardware Performance Monitoring
hpm16	16	1	false	WARL	0x0	Counter 16 Enable
						Hardware Performance Monitoring
hpm17	17	1	false	WARL	0x0	Counter 17 Enable
						Hardware Performance Monitoring
hpm18	18	1	false	WARL	0x0	Counter 18 Enable
						Hardware Performance Monitoring
hpm19	19	1	false	WARL	0x0	Counter 19 Enable
						Hardware Performance Monitoring
hpm20	20	1	false	WARL	0x0	Counter 20 Enable
						Hardware Performance Monitoring
hpm21	21	1	false	WARL	0x0	Counter 21 Enable
						Hardware Performance Monitoring
hpm22	22	1	false	WARL	0x0	Counter 22 Enable
						Hardware Performance Monitoring
hpm23	23	1	false	WARL	0x0	Counter 23 Enable
						Hardware Performance Monitoring
hpm24	24	1	false	WARL	0x0	Counter 24 Enable
						Hardware Performance Monitoring
hpm25	25	1	false	WARL	0x0	Counter 25 Enable
						Counter 25 Enable

hpm26	26	1	false	WARL	0x0	Hardware Performance Monitoring Counter 26 Enable
hpm27	27	1	false	WARL	0×0	Hardware Performance Monitoring Counter 27 Enable
hpm28	28	1	false	WARL	0x0	Hardware Performance Monitoring Counter 28 Enable
hpm29	29	1	false	WARL	0×0	Hardware Performance Monitoring Counter 29 Enable
hpm30	30	1	false	WARL	0×0	Hardware Performance Monitoring Counter 30 Enable
hpm31	31	1	false	WARL	0×0	Hardware Performance Monitoring Counter 31 Enable

senvcfg											
Address	0x01	x010A									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Supe	rvisor enviro	nment config	guration regis	ster.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
fiom		0	1	false	read-write	0x0	Fence of I/O implies Memory				
wpri_0		1	3	false	WPRI	0x0	WPRI				
							Cache Block Invalidate instruction				
cbie		4	2	false	read-write	0x0	Enable Enables the execution of				
							CBO.INVAL in a lower privilege mode				
							Cache Block Clean and Flush				
cbcfe		6	1	false	read-write	0x0	instruction enable Enables				
свсте							execution of CBO.CLEAN and				
							CBO.FLUSH in a lower privilege mode				
							Cache Block Zero instruction Enable				
cbze		7	1	false	read-write	0x0	Enables execution of CBO.ZERO in				
							a lower privilege mode				
wpri_1		8 24 false WPRI 0x0 WPRI									
nmm		22	2	false	road write	0x0	Enables pointer masking for the next				
pmm		32	2	iaise	read-write	UXU	lower privilege mode				
wpri_2		34	30	false	WPRI	0x0	WPRI				

sstateen	sstateen0										
Address	0x01	<010C									
Size	32	2									
Reset Value	0x00	000000									
Description	Supervisor State Enable 0										
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description									

С	0	1	false	WARL	0x0	Controls access to any and all custom state
fcsr	1	1	false	WARL	0x0	Controls access to fcsr CSR
jvt	2	1	false	WARL	0x0	Controls access to JVT CSR
wpri	3	29	false	WPRI	0x0	WPRI

sstateen	sstateen1								
Address	0x01	x010D							
Size	32								
Reset Value	0x00	000000							
Description	Supe	rvisor State I	Enable 1						
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description							
wpri		0	32	false	WPRI	0x0	WPRI		

sstateen	sstateen2								
Address	0x01	x010E							
Size	32	2							
Reset Value	0x00	000000							
Description	Supe	rvisor State I	Enable 2						
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description							
wpri		0	32	false	WPRI	0x0	WPRI		

sstateen	sstateen3								
Address	0x01	010F							
Size	32								
Reset Value	0x00	000000							
Description	Supe	rvisor State I	Enable 3						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description							
wpri		0 32 false WPRI 0x0 WPRI							

sscratch											
Address	0x01	x0140									
Size	64										
Reset Value	0x00	0x0000000000000									
Description	Scratch register for supervisor trap handlers.										
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
sscratch		0	64 fa	false	read-write	0x0	Scratch register for supervisor trap				
SSCIALCII		O	04	laise	reau-write	0.00	handlers.				

sepc	
Address	0x0141

Size	64	4								
Reset Value	0x00	00000000000000								
Description	Supe	pervisor exception program counter.								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
rsvd00	0 0		1	-	WPRI	-	Reserved			
addr 1		63	false	WARL	0x0	Supervisor exception program counter.				

scause										
Address	0x01	x0142								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Supe	Supervisor trap cause.								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
oveentionsed	امساحا	0	63	c 1		0x0	Code identifying the last exception			
exceptioncod	iewiri	0	63	false	read-write	OXO	or interrupt			
interrupt		63			read-write	0.0	Indicates if the trap was caused by			
		63	1	false	reau-write	0x0	an interrupt			

stval										
Address	0x01	x0143								
Size	64									
Reset Value	0x00	0x000000000000								
Description	Supe	Supervisor Trap Value Register								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
stval	0 64			false	WARL	0×0	Supervisor bad address or instruction.			

sip										
Address	0x01	×0144								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Supe	rvisor interru	ıpt pending.							
Field Nan	ld Name Bit Offset		Bit Width	Volatile	Access	Reset Value	Description			
rsvd00		0	1	-	WPRI	-	Reserved			
ssip		1	1	true	WARL	0×0	Supervisor Software Interrupt Pending			
hard0_1		2	2	true	WARL	0x0	Hardwired 0			
rsvd44	4		1	-	WPRI	-	Reserved			
stip	5		1	true	WARL	0x0	Supervisor Timer Interrupt Pending			
hard0_2		6	2	true	WARL	0x0	Hardwired 0			

rsvd88	8	1	-	WPRI	-	Reserved
seip	9	1	true	WARL	0x0	Supervisor External Interupt Pending
hard0_3	10	3	true	WARL	0x0	Hardwired 0
lfi-	13	1	.	WARL	00	Supervisor Local Count Overflow
Icofip	13	1	true	WARL	0x0	Interrupt Pending
rsvd6414	14	50	-	WPRI	-	Reserved

stimecm	ecmp								
Address	0x01	014D							
Size	64								
Reset Value	0x00	000000FFFFI	FFF						
Description	Supe	Supervisor timer register							
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description							
stimecmp		0 64 false WARL 0xFFFFFFF Supervisor timer compare value							

siselect

Address	0x01	x0150								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Supe	rvisor Indired	t register se	lect (valid ra	nge is 0 - 0xF	·F)				
Field Nan	ne	e Bit Offset Bit Width Vola			Access	Reset Value	Description			
interrupts		0 9		false	WARL	0x0	0x30 - 0x3F : Major Intr priorities0x70-0xFF: External Intr. (0x71, 0x73-0x7F are rsvd)Rest: Reserved			
rsvd_63_9	vd_63_9 9		55	false	WARL	0x0	Reserved for future use			

sireg									
Address	0x01	x0151							
Size	64								
Reset Value	0x00	0000000000	0000						
Description	Supe	rvisor indired	t register ali	as					
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description							
sireg		0 64 false WARL 0x0 Supervisor indirect register alias							

stopei	
Address	0x015C
Size	64
Reset Value	0x0000000000000
Description	Supervisor top external interrupt (This is marked as read-write in AIA spec, but implemented as read-only for write to
Description	this CSR is ignored)

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
priority	0	11	true	WARL	0x0	Interrupt priority (same as identity)
rsvd_15_11	11	5	true	WARL	0x0	Reserved for future use
identity	16	11	true	WARL	0x0	Interrupt identity
rsvd_63_27	27	37	true	WARL	0x0	Reserved for future use

satp											
Address	0x01	x0180									
Size	64										
Reset Value	0x00	x0000000000000									
Description	Supe	Supervisor address translation and protection.									
Field Nan	ne .	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
ppn		0	44	false	WARL	0x0	Physical Page Number				
asid		44	16	false	WARL	0x0	Address Space Identifier				
mode		60	4	false	WARL	0x0	Address Translation and Protection Mode				

srmcfg										
Address	0x01	x0181								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Supe	Supervisor resource management qualification								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
rcid		0	12	false	WARL	0x0	resource controller ID			
rsvd1512		12	4	-	WPRI	-	Reserved			
mcid		16	12	false	WARL	0x0	Monitor resource usage ID			
rsvd6428		28	36	-	WPRI	-	Reserved			

vsstatus										
Address	0x02	x0200								
Size	64	4								
Reset Value	0x00	0000020000	0000							
Description	Virtu	al supervisor	status regist	ter.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
vsstatus_wpr	i_0	0	1	true	WPRI	0x0	WPRI			
sie		1	1	true	WARL	0x0	interrupts are globally enabled when in VS-mode			
vsstatus_wpr	i_1	2	3	true	WPRI	0x0	WPRI			
spie		5	1	true	WARL	0×0	interrupt-enable bit active prior to the trap in VS-mode			

ube	6	1	true	WARL	0×0	Endianness: non-instruction-fetch memory accesses made from VU-mode
vsstatus_wpri_2	7	1	true	WPRI	0x0	WPRI
spp	8	1	true	WARL	0×0	previous privilege mode before entering VS-mode
VS	9	2	true	WARL	0x0	status of the vector extension state
vsstatus_wpri_3	11	2	true	WPRI	0x0	WPRI
fs	13	2	true	WARL	0x0	status of the floating-point unit state
xs	15	2	true	WARL	0×0	status of additional user-mode extensions and associated state
vsstatus_wpri_4	17	1	true	WPRI	0x0	WPRI
sum	18	1	true	WARL	0×0	permit Supervisor User Memory access
mxr	19	1	true	WARL	0x0	Make eXecutable Readable
vsstatus_wpri_5	20	12	true	WPRI	0x0	WPRI
uxl	32	2	true	WARL	0x2	XLEN for VU-mode
vsstatus_wpri_6	34	29	true	WPRI	0x0	WPRI
sd	63	1	true	WARL	0x0	Summary of FS/VS/XS

vsie									
Address	0x02	04							
Size	32	32							
Reset Value	0x00	0x0000000							
Description	Virtual supervisor interrupt-enable register.								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description		
rsvd00		0	1	-	WPRI	-	Reserved		
vssie		1	1	false	read-write	0×0	Virtual Supervisor Software Interrupt		
VSSIE		T	1	iaise	reau-write	UXU	Enable		
hard0_0		2	2	false	read-write	0x0	Hardwired 0		
rsvd44		4	1	-	WPRI	-	Reserved		
vstie		5	1	false	read-write	0×0	Virtual Supervisor Timer Interrupt		
volle		J	1	iaise	reau-write	0.00	Enable		
hard0_1		6	2	false	read-write	0x0	Hardwired 0		
rsvd88		8	1	-	WPRI	-	Reserved		
vseie		9	1	false	read-write	0×0	Virtual Supervisor External Interrupt		
vsele		9	1	iaise	reau-write	UXU	Enable		
hard0_2		10	3	false	read-write	0x0	Hardwired 0		
lcofie		13	1	false	read-write	0x0	Virtual Supervisor Local Count		
icone		13	1	iaise	reau-write	UXU	Overflow Interrupt Enable		
rsvd3214		14	18	-	WPRI	-	Reserved		

vstvec

Size	64	54							
Reset Value	0x00	x00000000000000							
Description	Virtu	al supervisor	trap handlei	r base addres	SS.				
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description							
mode 0		0	1	false	WARL	0x0	Allows mode 0 (base only) or mode 1		
Inlode_0		0		laise	WARL	OXO	(vectored)		
mode_1		1	1	false	WARL	0x0	Modes >= 2 are not allowed		
basesxlen12v	varl	2	62	false	WARL	0x0	Top SXLEN-2 bits of BASE		

0x0205

Address

vsscratcl	า									
Address	0x02	0240								
Size	64									
Reset Value	0x00	×00000000000000								
Description	Virtu	al supervisor	scratch regi	ster.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
sscratch		0	64	false	WARL	0x0	Virtual supervisor scratch register.			

vsepc											
Address	0x02	x0241									
Size	64										
Reset Value	0x00	×0000000000000									
Description	Virtu	Virtual supervisor exception program counter.									
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
rsvd00		0	1	-	WPRI	-	Reserved				
addr		1	63	false	WARL	0×0	Virtual supervisor exception program counter.				

vscause											
Address	0x02	0x0242									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Virtu	/irtual supervisor trap cause.									
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
oveentioneed	اعسادا	0	63	false	WARL	0x0	Code identifying the last exception				
exceptioncod	ewiri	U	03	laise	WARL	OXO	or interrupt				
interrunt		63	1	false	WARL	0x0	Indicates if the trap was caused by				
interrupt		03	1	iaise	WARL	UXU	an interrupt				

vstval	
Address	0x0243

Size	64	54									
Reset Value	0x00	0x000000000000									
Description	Virtu	irtualized supervisor bad guest physical address.									
Field Nan	ame Bit Offset Bit Widt		vari 1.1								
i icia itai	1e	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
vstval	ie	0	64	false	Access WARL	Reset Value	Description Virtualized supervisor bad guest				

vsip											
Address	0x02	x0244									
Size	32										
Reset Value	0x00	000000									
Description	Virtu	al supervisor	interrupt pe	nding.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
rsvd00		0	1	-	WPRI	-	Reserved				
wasia		1	1	folos		0.40	Virtual Supervisor Software Interrupt				
vssip		1	1	false	read-write	0x0	Pending				
hard0_1		2	2	false	read-write	0x0	Hardwired 0				
rsvd44		4	1	-	WPRI	-	Reserved				
vetin		5	1	false	road only	0x0	Virtual Supervisor Timer Interrupt				
vstip		3	1	laise	read-only	0.00	Pending				
hard0_2		6	2	false	read-write	0x0	Hardwired 0				
rsvd88		8	1	-	WPRI	-	Reserved				
vseip		9	1	false	read-only	0x0	Virtual Supervisor External Interrupt				
vseip		9	1	laise	read-only	OXO	Pending				
hard0_3		10	3	false	read-write	0x0	Hardwired 0				
Icofin		13	1	false	road only	0x0	Virtual Supervisor Local Count				
lcofip		13	1	iaise	read-only	UXU	Overflow Interrupt Pending				
rsvd3214		14	18	-	WPRI	-	Reserved				

vstimecn	vstimecmp											
Address	0x02	x024D										
Size	64											
Reset Value	0x00	0x0000000FFFFFFF										
Description	Virtu	al supervisor	timer regist	er								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description					
vstimecmp		0 64 false WARL 0xFFFFFFFF Value										

vsiselect	vsiselect							
Address	0x0250							
Size	64							
Reset Value	0x000000000000							

Description	Virtu	rtual supervisor Indirect register select (valid range is 0 - 0xFF)							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description		
							0x70-0xFF: External Intr. (0x71,		
interrupts		0	9	false	WARL	0x0	0x73-0x7F are rsvd)Rest:		
							Inaccessible		
rsvd_63_9		9	55	false	WARL	0x0	Reserved for future use		

vsireg	vsireg										
Address	0x02	0x0251									
Size	64										
Reset Value	0x00	0x0000000000000									
Description	Virtu	al supervisor	indirect regi	ster alias							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
since O G4 Sales WARL 0.0						0.40	Virtual supervisor indirect register				
sireg		0	64	false	WARL	0x0	alias				

vstopei											
Address	0x02	0x025C									
Size	64										
Reset Value	0x00	0000000000	0000								
Description		This is Virtual supervisor top external interrupt (This is marked as read-write in AIA spec, but implemented as read-only for write to this CSR is ignored)									
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
priority		0	11	true	WARL	0x0	Interrupt priority (same as identity)				
rsvd_15_11	11 5 true WARL 0x0 Reserved for future use										
identity		16 11 true WARL 0x0 Interrupt identity									
rsvd_63_27		27	37	true	WARL	0x0	Reserved for future use				

vsatp												
Address	0x02	0x0280										
Size	64											
Reset Value	0x00	0000000000	0000									
Description	Virtu	al Supervisor	address trai	nslation and	protection.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description					
ppn		0	44	false	WARL	0×0	Physical Page Number					
asid		44	16	false	WARL	0x0	Address Space Identifier					
		60	4		MADI	00	Address Translation and Protection					
mode		60	4 false		WARL	0x0	Mode					

mstatus	
Address	0x0300

Size	64
Reset Value	0x000000A0000000
Description	Machine status register.

				_		
Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
mstatus_wpri_0	0	1	true	WPRI	0x0	WPRI
sie	1	1	true	WARL	0x0	hardware write: TRUE interrupts are
						globally enabled when in S-mode
mstatus_wpri_1	2	1	true	WPRI	0x0	WPRI
mie	3	1	true	WARL	0x0	hardware write: TRUE interrupts are
		_				globally enabled when in M-mode
mstatus_wpri_2	4	1	true	WPRI	0x0	WPRI
						hardware write: TRUE
spie	5	1	true	WARL	0x0	interrupt-enable bit active prior to
						the trap in S-mode
						Endianness: non-instruction-fetch
ube	6	1	true	WARL	0x0	memory accesses made from
						U-mode (not writable)
						hardware write: TRUE
mpie	7	1	true	WARL	0x0	interrupt-enable bit active prior to
						the trap in M-mode
						hardware write: TRUE previous
spp	8	1	true	WARL	0x0	privilege mode before entering
						S-mode
VS	9	2	true	WARL	0x0	status of the vector extension state
						previous privilege mode before
mpp	11	2	true	WARL	0x0	entering M-mode
						status of the floating-point unit state
fs	13	2	true	WARL	0x0	(Must become F-ext is implemented)
						status of additional user-mode
XS	15	2	true	WARL	0x0	extensions and associated state
						Modify PRiVilege: modifies the
mprv	17	1	true	WARL	0x0	effective privilege mode
						permit Supervisor User Memory
sum	18	1	true	WARL	0x0	
	10	1		MARI		access
mxr	19	1	true	WARL	0x0	Make eXecutable Readable
tvm	20	1	true	WARL	0x0	Trap Virtual Memory (should be
						writable for hypervisor emulation)
tw	21	1	true	WARL	0x0	Timeout Wait (should be writable for
						hypervisor emulation)
tsr	22	1	true	WARL	0x0	Trap SRET (FE catch illegal if SRET
						&& TSR==1)
mstatus_wpri_3	23	9	true	WPRI	0x0	WPRI
uxl	32	2	true	WARL	0x2	XLEN for U-mode
		· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·	· · · · · · · · · · · · · · · · · · ·		

sxl	34	2	true	WARL	0x2	XLEN for S-mode
sbe	36	1	true	WARL	0x0	Endianness: non-instruction-fetch memory accesses made from S-mode
mbe	37	1	true	WARL	0x0	Endianness: non-instruction-fetch memory accesses made from M-mode
gva	38	1	true	WARL	0x0	Endianness: non-instruction-fetch memory accesses made from M-mode
mpv	39	1	true	WARL	0×0	Endianness: non-instruction-fetch memory accesses made from M-mode
mstatus_wpri_4	40	23	true	WPRI	0x0	WPRI
sd	63	1	true	WARL	0x0	Summary of FS/VS/XS

misa											
Address	0x03	0x0301									
Size	64										
Reset Value	0x80	0000000034	11AF								
Description	ISA a	nd extension	ıs								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
а		0	1	false	WARL	0x1	Atomic extension (software can turn this off)				
b		1	1	false	WARL	0×1	Bit-manip extension Read as 1 for Athena (software can not turn this off)				
С		2	1	false	WARL	0x1	Compressed extension (software can turn this off)				
d		3	1	false	WARL	0x1	Double-precision FP extension (software can turn this off)				
е		4	1	false	WARL	0x0	RV32E base ISA (Not allowing this)				
f		5	1	false	WARL	0x1	Single-precision FP extension (software can turn this off)				
g		6	1	false	WARL	0x0	Reserved				
h		7	1	false	WARL	0x1	Hypervisor extension				
i		8	1	false	WARL	0x1	RV64I base ISA				
j		9	1	false	WARL	0x0	Reserved				
k		10	1	false	WARL	0x0	Reserved				
I		11	1	false	WARL	0x0	Reserved				
m		12	1	false	WARL	0x1	Integer Mul/Div extension (software can turn this off)				

n	13	1	false	WARL	0×0	User-level interrupts extension (Do we need this?)
0	14	1	false	WARL	0x0	Reserved
р	15	1	false	WARL	0x0	Reserved
	16	1	false	WARL	0x0	Quad precision FP extension (Not
q	10	1	laise	WARL	UXU	doing this)
r	17	1	false	WARL	0x0	Reserved
	18	1	false	WARL	0x1	Supervisor mode implemented
S	10	1	laise	WARL	OXI	(software can turn this off)
t	19	1	false	WARL	0x0	Reserved
	20	1	false	WARL	0x1	User mode implemented (software
u	20	1	laise			can turn this off)
	21	1	false	WARL	0.1	Vector extension (software can turn
V	21	1	laise	WARL	0x1	this off)
w	22	1	false	WARL	0x0	Reserved
						Non-standard extensions present
x	23	1	false	WARL	0x0	(Saying No since, Not sure what this
						contains)
У	24	1	false	WARL	0x0	Reserved
z	25	1	false	WARL	0x0	Reserved
wlrl0	26	36	false	WARL	0x0	Hardwired 0
mxl	62	2	false	WARL	0x2	Native base integer ISA width

medeleg										
Address	0x03	x0302								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	nine exceptio	n delegation	register.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
medeleg_0		0	10	false	WARL	0x0	Exception codes 0-9			
medeleg_mas _0	sked	10	1	false	WARL	0x0	Exception code 10			
ecall_from_m		11	1	false	WARL	0x0	Exception code 11			
medeleg_1		12	2	false	WARL	0x0	Exception codes 12-13			
rsvd_0		14	1	false	WARL	0x0	Reserved exception code			
medeleg_2		15	1	false	WARL	0x0	Exception code 15			
rsvd_1		16	4	false	WARL	0x0	Reserved exception codes			
medeleg_3 20		4	false	WARL	0x0	Exception codes 20-23				
rsvd_2		24	40	false	WARL	0x0	Reserved exception codes			

mideleg	
Address	0x0303
Size	64

Reset Value	0x0000000001444
Description	Machine interrupt delegation register.

Description Mac	Description Machine interrupt delegation register.								
Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
rsvd00	0	1	-	WPRI	-	Reserved			
ssip	1	1	false	WARL	0×0	Delegate Supervisor Software			
ssip	1	*	laise	WARL	000	Interrupt			
vssip	2	1	false	WARL	0x1	Delegate Virtual Supervisor Software			
vssip	2	_	laise	WARL	OXI	Interrupt			
msip	3	1	false	WARL	0x0	Delegate Machine Software Interrupt			
rsvd44	4	1	-	WPRI	-	Reserved			
stip	5	1	false	WARL	0x0	Delegate Supervisor Timer Interrupt			
vstip	6	1	false	WARL	0x1	Delegate Virtual Supervisor Timer			
vsup		_	Taise	WAILE	OXI	Interrupt			
mtip	7	1	false	WARL	0x0	Delegate Machine Timer Interrupt			
rsvd88	8	1	-	WPRI	-	Reserved			
seip	9	1	false	WARL	0x0	Delegate Supervisor External			
JC.IP		-	10.50		o.ko	Interrupt			
vseip	10	1	false	WARL	0x1	Delegate Virtual Supervisor External			
		_	10.50		ON I	Interrupt			
meip	11	1	false	WARL	0×0	Delegate Machine External Interrupt			
sgeip	12	1	false	WARL	0x1	Delegate Supervisor Guest External			
ا ا		_	.3.50	,		Interrupt			
Icofip	ofip 13 1 false V	WARL	0x0	Delegate Local Count Overflow					
		T	idise	WANL	0.0	Interrupt			
rsvd6414	14	50	-	WPRI	-	Reserved			

mie											
Address	0x03	:0304									
Size	64	i4									
Reset Value	0x00	x00000000000000									
Description	Machine interrupt-enable register.										
		D': Off :	D': 14/2 1:1			B 13/1	.				

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
rsvd00	0	1	-	WPRI	-	Reserved
ssie	1	1	true	WARL	0x0	Interrupt-enable bit for Supervisor
ssie	1	1	lue	WARL	UXU	Software Interrupts
vssie	2	1	true	WARL	0x0	Interrupt-enable bit for Virtual
VSSIC	2	1	true	WARL	0.0	Supervisor Software Interrupts
msie	3	1	true	WARL	0x0	Interrupt-enable bit for Machine
IIIsie	5	1	tiue	WAILE	0.00	Software Interrupts
rsvd44	4	1	-	WPRI	-	Reserved
stio	5	1	true	WARL	0×0	Interrupt-enable bit for Supervisor
stie						Timer Interrupts

vstie	6	1	true	WARL	0x0	Interrupt-enable bit for Virtual Supervisor Timer Interrupts
mtie	7	1	true	WARL	0x0	Interrupt-enable bit for Machine Timer Interrupts
rsvd88	8	1	-	WPRI	-	Reserved
seie	9	1	true	WARL	0×0	Interrupt-enable bit for Supervisor External Interrupts
vseie	10	1	true	WARL	0x0	Interrupt-enable bit for Virtual Supervisor External Interrupts
meie	11	1	true	WARL	0x0	Interrupt-enable bit for Machine External Interrupts
sgeie	12	1	true	WARL	0x0	Interrupt-enable bit for Supervisor Guest External Interrupts
Icofie	13	1	true	WARL	0x0	Interrupt-enable bit for Local Count Overflow Interrupts
rsvd1514	14	2	-	WPRI	-	Reserved
nonstandardinterr	16	48	true	WARL	0×0	Definition of many of these interrupt numbers is either custom or non-ratified. So, these bits must be flexible

mtvec									
Address	0x03	05							
Size	64								
Reset Value	0x00	0×0000000000000							
Description	Mach	ine trap-han	dler base ad	dress.					
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description		
mode 0		0	1	false	WARL	0x0	Allows mode 0 (base only) or mode 1		
mode_o		O	1	laise	WARL	0.00	(vectored)		
mode_1		1 1 false WARL 0x0 Modes >= 2 are not allowed							
base		2	62	false	WARL	0x0	Top MXLEN-2 bits of BASE		

mcounte	ren						
Address	0x03	06					
Size	32						
Reset Value	0x00	000000					
Description	Mach	ine counter o	enable.				
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
су		0	1	false	WARL	0x0	Cycle Counter Enable
tm		1	1	false	WARL	0x0	Time Counter Enable
ir		2	1	false	WARL	0x0	Instruction Retired Counter Enable

		1	1			1
hpm3	3	1	false	WARL	0x0	Hardware Performance Monitoring
						Counter 3 Enable
hpm4	4	1	false	WARL	0x0	Hardware Performance Monitoring
•						Counter 4 Enable
hpm5	5	1	false	WARL	0x0	Hardware Performance Monitoring
						Counter 5 Enable
hpm6	6		false	WARL	0x0	Hardware Performance Monitoring
			Tuise	W/ (()		Counter 6 Enable
hpm7	7	1	false	WARL	0x0	Hardware Performance Monitoring
			laise	W/ ((\C	0.00	Counter 7 Enable
hpm8	8	1	false	WARL	0x0	Hardware Performance Monitoring
прито			laise	WARL	0.00	Counter 8 Enable
h n n 0	0	1	false	WARL	0×0	Hardware Performance Monitoring
hpm9	9	1	laise	WARL	UXU	Counter 9 Enable
h	10	1	£-1	MADI	00	Hardware Performance Monitoring
hpm10	10	1	false	WARL	0x0	Counter 10 Enable
	11		6.1	WAR!	0.0	Hardware Performance Monitoring
hpm11	11	1	false	WARL	0x0	Counter 11 Enable
		_				Hardware Performance Monitoring
hpm12	12	1	false	WARL	0x0	Counter 12 Enable
		_			0x0	Hardware Performance Monitoring
hpm13	13	1	false	WARL		Counter 13 Enable
						Hardware Performance Monitoring
hpm14	14	1	false	WARL	0x0	Counter 14 Enable
						Hardware Performance Monitoring
hpm15	15	1	false	WARL	0x0	Counter 15 Enable
						Hardware Performance Monitoring
hpm16	16	1	false	WARL	0x0	Counter 16 Enable
						Hardware Performance Monitoring
hpm17	17	1	false	WARL	0x0	Counter 17 Enable
						Hardware Performance Monitoring
hpm18	18	1	false	WARL	0x0	Counter 18 Enable
						Hardware Performance Monitoring
hpm19	19	1	false	WARL	0x0	Counter 19 Enable
						Hardware Performance Monitoring
hpm20	20	1	false	WARL	0x0	Counter 20 Enable
						Hardware Performance Monitoring
hpm21	21	1	false	WARL	0x0	Counter 21 Enable
						Hardware Performance Monitoring
hpm22	22	1	false	WARL	0x0	Counter 22 Enable
						Hardware Performance Monitoring
hpm23	23	1	false	WARL	0x0	Counter 23 Enable
						Counter 23 Enable

hpm24	24	1	false	WARL	0x0	Hardware Performance Monitoring Counter 24 Enable
hpm25	25	1	false	WARL	0×0	Hardware Performance Monitoring Counter 25 Enable
hpm26	26	1	false	WARL	0×0	Hardware Performance Monitoring Counter 26 Enable
hpm27	27	1	false	WARL	0×0	Hardware Performance Monitoring Counter 27 Enable
hpm28	28	1	false	WARL	0x0	Hardware Performance Monitoring Counter 28 Enable
hpm29	29	1	false	WARL	0×0	Hardware Performance Monitoring Counter 29 Enable
hpm30	30	1	false	WARL	0×0	Hardware Performance Monitoring Counter 30 Enable
hpm31	31	1	false	WARL	0×0	Hardware Performance Monitoring Counter 31 Enable

mvien										
Address	0x03	108								
Size	64	54								
Reset Value	0x00	0x0000000000000								
Description	Mach	fachine virtual interrupt enables								
Field Nar	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
hard0_0		0	1	false	WARL	0x0	Hardwired 0			
ssip		1 1	1 false	false	WARL	0×0	Enable virtual interrupts for			
3310		_	-	idisc			supervisor software interrupts			
hard0_1		2	7	false	WARL	0x0	Hardwired 0			
seip		9	1	false	WARL	0×0	Enable virtual interrupts for			
seip] 9	1	laise	WARL	000	supervisor external interrupts			
hard0_2		10	3	false	WARL	0x0	Hardwired 0			
Icofip		13	1	false	WARL	0×0	Enable virtual interrupts for local			
iconp		13	1	laise	WARL	000	count overflow interrupts			
rsvd6414		14	50	-	WPRI	-	Reserved			

mvip									
Address	0x03	0x0309							
Size	64	54							
Reset Value	0x00	0000000000	0000						
Description	Mach	ine virtual in	terrupt pend	ing bits					
Field Nan	Field Name Bit Offset Bit Wid		Bit Width	Volatile	Access	Reset Value	Description		
hard0_0	0 1		true	WARL	0x0	Hardwired 0			

ssip	1	1	true	WARL	0×0	Machine virtual supervisor software interrupt pending
hard0_1	2	3	true	WARL	0x0	Hardwired 0
stip	5	1	true	WARL	0×0	Machine virtual supervisor timer interrupt pending
hard0_2	6	3	true	WARL	0x0	Hardwired 0
seip	9	1	true	WARL	0×0	Machine virtual supervisor external interrupt pending
hard0_3	10	3	true	WARL	0x0	Hardwired 0
Icofip	13	1	true	WARL	0×0	Machine virtual local count overflow interrupt pending
rsvd6414	14	50	-	WPRI	-	Reserved

menvcfg	menvcfg									
Address	0x03	OA								
Size	64									
Reset Value	t Value 0x00000000000000									
Description	n Machine environment configuration register.									
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
fiom		0	1	false	WARL	0x0	Fence of I/O implies Memory			
wpri_0		1	3	false	WPRI	0x0	WPRI			
							Cache Block Invalidate instruction			
cbie		4	2	false	WARL	0x0	Enable Enables the execution of			
							CBO.INVAL in a lower privilege mode			
							Cache Block Clean and Flush			
ah afa		6	1	false	WADI	0x0	instruction enable Enables			
cbcfe					WARL		execution of CBO.CLEAN and			
							CBO.FLUSH in a lower privilege mode			
							Cache Block Zero instruction Enable			
cbze		7	1	false	WARL	0x0	Enables execution of CBO.ZERO in			
							a lower privilege mode			
wpri_1		8	24	false	WPRI	0x0	WPRI			
		22	2	foloo	WADI	00	Enables pointer masking for the next			
pmm		32	2	false	WARL	0x0	lower privilege mode			
wpri_2		34	27	false	WPRI	0x0				
							Enables hardware updating of PTE			
hade		61	1	false	WARL	0x0	A/D bits during S-mode address			
							translation			
							Enables Svpbmt extension for			
pbmte		62	1	false	WARL	0×0	S-mode and G-stage address			
							translation			
stce		63	1	false	WARL	0x0	Enables STimecmp for S-mode			

mstateen0							
Address	0x030C						
Size	64						
Reset Value	0x000000000000						
Description	Machine State Enable 0						

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
С	0	1	false	WARL	0x0	Controls access to any and all
		_	laise	WAILE	0.00	custom state
fcsr	1	1	false	WARL	0x0	Controls access to fcsr CSR
jvt	2	1	false	WARL	0x0	Controls access to JVT CSR
wpri_0	3	52	false	WPRI	0x0	WPRI
srmcfg	55	1	false	WARL	0x0	Controls access to Srmcfg CSR
p1p13	56	1	false	WARL	0x0	Controls access to hedelegh CSR
context	57	1	false	WARL	0x0	Controls access to scontext and
Context	57			WARL		hcontext CSRs
imsic	58	1	false	WARL	0x0	Controls access to IMSIC state
aia	59	1	false	WARL	0x0	Controls access to all state
ala	159	1	laise	WARL	UXU	introduced by the Ssaia extension
csrind	60	1	false	WARL	0x0	Controls access to siselect, sireg*,
CSTITIU	00	1	laise	WARL	OXO	vsiselect, vsireg* CSRs
wpri_1	61	1	false	WPRI	0x0	WPRI
onyefa	62	1	false	WADI	0x0	Controls access to the henvcfg,
envcfg	02	1	false	WARL	UXU	henvcfgh, and senvcfg CSRs
se0	63	1	false	WAR!	0×0	Controls access to the hstateen0,
560	63			WARL		hstateen0h, and sstateen0 CSRs

mstateen1										
Address	0x03	0x030D								
Size	64									
Reset Value	0x00	0x0000000000000								
Description	Mach	ine State En	able 1							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
wpri		0	63	false	WPRI	0x0	WPRI			

mstateer	tateen2									
Address	0x03	0x030E								
Size	64	54								
Reset Value	0x00	0000000000	0000							
Description	Mach	Machine State Enable 2								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			

wpri	0	63	false	WPRI	0x0	WPRI
se2 63	63	1	f-1	MADI		Controls access to the hstateen2,
	03	3 1 false		WARL 0x0		hstateen2h, and sstateen2 CSRs

mstateen3											
Address	0x03	0x030F									
Size	64	4									
Reset Value	0x00	0x000000000000									
Description	Mach	ine State En	able 3								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
wpri		0	63	false	WPRI	0x0	WPRI				
se3		63	1	false	WARL	0x0	Controls access to the hstateen1, hstateen1h, and sstateen1 CSRs				

mcountinhibit

Address	0x03	0x0320								
Size	32									
Reset Value	0x00	000000								
Description	Mach	nine counter-	inhibit regist	er.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
су		0	1	false	WARL	0x0	Cycle Counter Inhibit			
hard0		1	1	false	WARL	0x0	Read-only zero			
ir		2	1	false	WARL	0x0	Instruction Retired Counter Inhibit			
hpm3		3	1	false	WARL	0×0	Hardware Performance Monitoring			
притэ		3	1	iaise	WARL	000	Counter 3 Inhibit			
hpm4		4	1	false	WARL	0×0	Hardware Performance Monitoring			
hpm4		4	1	iaise	WARL	OXO	Counter 4 Inhibit			
hpm5		5	1	false	WARL	0×0	Hardware Performance Monitoring			
ripirio		3	1	iaise	WARL	000	Counter 5 Inhibit			
hpm6		6	1	false	WARL	0×0	Hardware Performance Monitoring			
пртто		0	1	iaise	WARL	OXO	Counter 6 Inhibit			
hpm7		7	1	false	WARL	0×0	Hardware Performance Monitoring			
прш		,	1	iaise	WARL	000	Counter 7 Inhibit			
hpm8		8	1	false	WARL	0x0	Hardware Performance Monitoring			
пршо		0	1	iaise	WARL	OXO	Counter 8 Inhibit			
hnm0		9	1	false	WARL	0×0	Hardware Performance Monitoring			
hpm9		9	1	iaise	WARL	OXO	Counter 9 Inhibit			
hnm10		10	1	false	WARL	0.0	Hardware Performance Monitoring			
hpm10		10	1	iaise	VVAKL	0x0	Counter 10 Inhibit			
hpm11		11	1	false	WARL	0x0	Hardware Performance Monitoring			
		11 1	1				Counter 11 Inhibit			

						Hardware Performance Monitoring
hpm12	12	1	false	WARL	0x0	Counter 12 Inhibit
						Hardware Performance Monitoring
hpm13	13	1	false	WARL	0x0	Counter 13 Inhibit
						Hardware Performance Monitoring
hpm14	14	1	false	WARL	0x0	Counter 14 Inhibit
						Hardware Performance Monitoring
hpm15	15	1	false	WARL	0x0	Counter 15 Inhibit
						Hardware Performance Monitoring
hpm16	16	1	false	WARL	0x0	Counter 16 Inhibit
		_				Hardware Performance Monitoring
hpm17	17	1	false	WARL	0x0	Counter 17 Inhibit
h = == 10	10	1	f-1	NA DI	00	Hardware Performance Monitoring
hpm18	18	1	false	WARL	0x0	Counter 18 Inhibit
h 10	10	1	f-1	NA DI	00	Hardware Performance Monitoring
hpm19	19	1	false	WARL	0x0	Counter 19 Inhibit
hnm20	20	1	false	WADI	0.0	Hardware Performance Monitoring
hpm20	20	1	false	WARL	0x0	Counter 20 Inhibit
hnm21	21	1	false	WARL	0x0	Hardware Performance Monitoring
hpm21	21	1	laise	WARL	UXU	Counter 21 Inhibit
hpm22	22	1	false	WARL	0x0	Hardware Performance Monitoring
притег	22	1	laise	WARL	000	Counter 22 Inhibit
hpm23	23	1	false	WARL	0x0	Hardware Performance Monitoring
приисэ	23	1	laise	WAILE	0.00	Counter 23 Inhibit
hpm24	24	1	false	WARL	0x0	Hardware Performance Monitoring
TIPITIZ-F	2-7		laise	VV/U(E	oxo .	Counter 24 Inhibit
hpm25	25	1	false	WARL	0x0	Hardware Performance Monitoring
	23	_	laise		o.co	Counter 25 Inhibit
hpm26	26	1	false	WARL	0×0	Hardware Performance Monitoring
						Counter 26 Inhibit
hpm27	27	1	false	WARL	0x0	Hardware Performance Monitoring
						Counter 27 Inhibit
hpm28	28	1	false	WARL	0x0	Hardware Performance Monitoring
·						Counter 28 Inhibit
hpm29	29	1	false	WARL	0x0	Hardware Performance Monitoring
						Counter 29 Inhibit
hpm30	30	1	false	WARL	0x0	Hardware Performance Monitoring
						Counter 30 Inhibit
hpm31	31	1	false	WARL	0x0	Hardware Performance Monitoring
	_			WARL		Counter 31 Inhibit

mhpmev	ent3
Address	0x0323

Size	64	94									
Reset Value	0x00	×00000000000000									
Description	Mach	nine performa	ance-monitor	ing Event sel	lector.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
mhpmevent3		0	56	false	WARL	0x0	Event selector				
reserved		56	2	false	WARL	0x0	Reserved for future use				
vuinh		58	1	false	WARL	0x0	VU-mode counter inhibit				
vsinh		59	1	false	WARL	0x0	VS-mode counter inhibit				
uinh		60	1	false	WARL	0x0	U-mode counter inhibit				
sinh		61	1	false	WARL	0x0	S/HS-mode counter inhibit				
minh		62	1	false	WARL	0x0	M-mode counter inhibit				
of		62	1	f-1	WARL	0x0	Overflow status and interrupt disable				
UI		63	1	false	WANL	UXU	bit				

mhpmev	mhpmevent4										
Address	0x03	24									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mach	nine performa	ance-monitor	ing Event sel	ector.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
mhpmevent4		0	56	false	WARL	0x0	Event selector				
reserved		56	2	false	WARL	0x0	Reserved for future use				
vuinh		58	1	false	WARL	0x0	VU-mode counter inhibit				
vsinh		59	1	false	WARL	0x0	VS-mode counter inhibit				
uinh		60	1	false	WARL	0x0	U-mode counter inhibit				
sinh		61	1	false	WARL	0x0	S/HS-mode counter inhibit				
minh	ninh 62		1	false	WARL	0x0	M-mode counter inhibit				
of		63	1	false	WARL	0x0	Overflow status and interrupt disable bit				

mnpmev	mnpmevent5									
Address	0x03	25								
Size	64									
Reset Value	0x00	000000000	0000							
Description	Mach	nine performa	ance-monitor	ing Event sel	ector.					
Field Nan	Field Name Bit Offset Bit Width Volatile Access Reset Value Description					Description				
mhpmevent5		0	56	false	WARL	0x0	Event selector			
reserved		56	2	false	WARL	0x0	Reserved for future use			
vuinh	58 1 false			false	WARL	0x0	VU-mode counter inhibit			
vsinh	59 1 false WARL 0x0 VS-mode counter inhibit				VS-mode counter inhibit					
uinh		60 1 false WARL 0x0 U-mode counter inhibit								
sinh		61	1	false	WARL	0x0	S/HS-mode counter inhibit			

minh	62	1	false	WARL	0x0	M-mode counter inhibit
of	63	1	false	WARL	0×0	Overflow status and interrupt disable bit

mhpmev	mhpmevent6										
Address	0x03	26									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mach	nine performa	ance-monitor	ing Event se	lector.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
mhpmevent6	6	0	56	false	WARL	0x0	Event selector				
reserved		56	2	false	WARL	0x0	Reserved for future use				
vuinh		58	1	false	WARL	0x0	VU-mode counter inhibit				
vsinh		59	1	false	WARL	0x0	VS-mode counter inhibit				
uinh		60	1	false	WARL	0x0	U-mode counter inhibit				
sinh		61	1	false	WARL	0x0	S/HS-mode counter inhibit				
minh 62		62	1	false	WARL	0x0	M-mode counter inhibit				
of		63	1	false	WARL	0x0	Overflow status and interrupt disable bit				

mhpmevent7										
Address	0x03	27								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	nine performa	ance-monitor	ing Event sel	ector.					
Field Name Bit Offs		Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
mhpmevent7	,	0	56	false	WARL	0x0	Event selector			
reserved		56	2	false	WARL	0x0	Reserved for future use			
vuinh		58	1	false	WARL	0x0	VU-mode counter inhibit			
vsinh		59	1	false	WARL	0x0	VS-mode counter inhibit			
uinh		60	1	false	WARL	0x0	U-mode counter inhibit			
sinh		61	1	false	WARL	0x0	S/HS-mode counter inhibit			
minh	62 1		1	false	WARL	0x0	M-mode counter inhibit			
of		63	1	false	WARL	0×0	Overflow status and interrupt disable bit			

mhpmev	mhpmevent8										
Address	0x03	0x0328									
Size	64	54									
Reset Value	0x00	0000000000	0000								
Description	Machine performance-monitoring Event selector.										
Field Name Bit Offset Bit Width Volatile Access Ro						Reset Value	Description				

mhpmevent8	0	56	false	WARL	0x0	Event selector
reserved	56	2	false	WARL	0x0	Reserved for future use
vuinh	58	1	false	WARL	0x0	VU-mode counter inhibit
vsinh	59	1	false	WARL	0x0	VS-mode counter inhibit
uinh	60	1	false	WARL	0x0	U-mode counter inhibit
sinh	61	1	false	WARL	0x0	S/HS-mode counter inhibit
minh	62	1	false	WARL	0x0	M-mode counter inhibit
of	63	1	false	WARL	0x0	Overflow status and interrupt disable
	03					bit

mhpmev	mhpmevent9										
Address	0x03	29									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mach	nine performa	ance-monitor	ing Event se	lector.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
mhpmevent9)	0	56	false	WARL	0x0	Event selector				
reserved		56	2	false	WARL	0x0	Reserved for future use				
vuinh		58	1	false	WARL	0x0	VU-mode counter inhibit				
vsinh		59	1	false	WARL	0x0	VS-mode counter inhibit				
uinh		60	1	false	WARL	0x0	U-mode counter inhibit				
sinh	sinh		1	false	WARL	0x0	S/HS-mode counter inhibit				
minh 62		62	1	false	WARL	0x0	M-mode counter inhibit				
of		63	1	false	WARL	0×0	Overflow status and interrupt disable bit				

mnpmevent10											
Address	0x03	0x032A									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mach	nine performa	ance-monitor	ing Event sel	lector.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
mhpmevent1	0	0	56	false	WARL	0x0	Event selector				
reserved		56	2	false	WARL	0x0	Reserved for future use				
vuinh		58	1	false	WARL	0x0	VU-mode counter inhibit				
vsinh		59	1	false	WARL	0x0	VS-mode counter inhibit				
uinh		60	1	false	WARL	0x0	U-mode counter inhibit				
sinh		61	1	false	WARL	0x0	S/HS-mode counter inhibit				
minh 62		62	1	false	WARL	0x0	M-mode counter inhibit				
of		63	1	f-1	WARL	0.0	Overflow status and interrupt disable				
OI .		63 1 false WARL 0x0		0.00	bit						

mhpmev	mhpmevent11									
Address	0x03	x032B								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.					
Field Nan	Field Name Bit Offset Bit Width Volatile Access Reset Value			Description						
mhpmevent1	1	0	64	false	WARL	0x0	Event selector			

mhpmev	mhpmevent12										
Address	0x03	0x032C									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description									
mhpmevent1	2	0 64 false WARL 0x0 Event selector									

mhpmev	mhpmevent13										
Address	0x03	0x032D									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.						
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description										
mhpmevent1	3	0 64 false WARL 0x0 Event selector									

mhpmev	mhpmevent14									
Address	0x03	x032E								
Size	64	•								
Reset Value	0x00	0000000000	0000							
Description	Mach	nine performa	ance-monitor	ing Event sel	ector.					
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
mhpmevent1	4	0 64 false WARL 0x0 Event selector								

mhpmev	mhpmevent15										
Address	0x03	0x032F									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description									
mhpmevent1	5	0 64 false WARL 0x0 Event selector									

mhpmev	mhpmevent16										
Address	0x03	0x0330									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description									
mhpmevent1	6	0 64 false WARL 0x0 Event selector									

mhpmev	mhpmevent17									
Address	0x03	x0331								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.					
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
mhpmevent1	7	0 64 false WARL 0x0 Event selector								

mhpmev	mhpmevent18										
Address	0x03	Dx0332									
Size	64	4									
Reset Value	0x00	0000000000	0000								
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.						
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description										
mhpmevent1	8	8 0 64 false WARL 0x0 Event selector									

mhpmev	mhpmevent19										
Address	0x03	x0333									
Size	64	•									
Reset Value	0x00	0000000000	0000								
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description									
mhpmevent1	9	0 64 false WARL 0x0 Event selector									

mhpmev	mhpmevent20										
Address	0x03	0x0334									
Size	64	1									
Reset Value	0x00	0000000000	0000								
Description	Mach	ine performa	ance-monitor	ing Event se	lector.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description									
mhpmevent2	0	0 64 false WARL 0x0 Event selector									

mhpmev	mhpmevent21											
Address	0x03	0x0335										
Size	64											
Reset Value	0x00	0000000000	0000									
Description	Mach	nine performa	ance-monitor	ing Event sel	lector.							
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description										
mhpmevent2	1	0 64 false WARL 0x0 Event selector										

mhpmev	mhpmevent22										
Address	0x03	x0336									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.						
Field Nan	ne .	e Bit Offset Bit Width Volatile Access Reset Value Description									
mhpmevent2	2	0 64 false WARL 0x0 Event selector									

mhpmev	mhpmevent23										
Address	0x03	0x0337									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.						
Field Nan	e Bit Offset Bit Width Volatile Access Reset Value Description										
mhpmevent2	3	0 64 false WARL 0x0 Event selector									

mhpmev	mhpmevent24									
Address	0x03	0338								
Size	64									
Reset Value	0x00	0x000000000000								
Description	Mach	nine performa	ance-monitor	ing Event sel	ector.					
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
mhpmevent2	4	0 64 false WARL 0x0 Event selector								

mhpmevent25									
Address	0x0339								
Size	64								
Reset Value	0x00	0000000000	0000						
Description	Mach	ine performa	ance-monitor	ing Event sel	ector.				
Field Nan	me Bit Offset Bit Width Volatile Access Reset Value Description				Description				
mhpmevent2	5	5 0 64 false WARL 0x0 Event selector					Event selector		

mhpmev	mhpmevent26									
Address	0x03	x033A								
Size	64									
Reset Value	0x00	0x0000000000000								
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.					
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description						Description			
mhpmevent2	6	0 64 false WARL 0x0 Event selector								

mhpmev	mhpmevent27									
Address	0x03	x033B								
Size	64									
Reset Value	0x00	0×000000000000								
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.					
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description						Description			
mhpmevent2	7 0 64			false	WARL	0x0	Event selector			

mhpmev	mhpmevent28									
Address	0x03	x033C								
Size	64									
Reset Value	0x00	0x000000000000								
Description	Mach	nine performa	ance-monitor	ing Event sel	lector.					
Field Nan	me Bit Offset Bit Width Volatile Access Reset Value Descript				Description					
mhpmevent2	8	0 64 false WARL 0x0 Event selector								

mhpmev	mhpmevent29									
Address	0x03	x033D								
Size	64									
Reset Value	0x00	0x000000000000								
Description	Mach	ine performa	ance-monitor	ing Event se	lector.					
Field Nan	ne	ne Bit Offset Bit Width Volatile Access Reset Value Description					Description			
mhpmevent2	9	0 64 false WARL 0x0 Event selector								

mhpmevent30										
Address	0x03	x033E								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	ine performa	ance-monitor	ing Event se	lector.					
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description				Description					
mhpmevent3	0	0 64 false WARL 0x0 Event selector								

mhpmev	mhpmevent31									
Address	0x03	x033F								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	ine performa	ance-monitor	ing Event sel	lector.					
Field Nan	ne Bit Offset Bit Width		Volatile	Access	Reset Value	Description				
mhpmevent3	1	0	64	false	WARL	0x0	Event selector			

mscratch	mscratch									
Address	0x03	0340								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Scrat	ch register fo	or machine tr	ap handlers.	•					
Field Nan	ne Bit Offset Bit Width		Volatile	Access	Reset Value	Description				
mscratch		0 64 false WARL 0x0 Machine Scratch Register					Machine Scratch Register			

mepc	epc										
Address	0x03	0341									
Size	64										
Reset Value	0x00	0000000000000000000									
Description	Mach	ine exceptio	n program co	ounter.							
Field Nan	ne Bit Offset Bit Width		Bit Width	Volatile	Access	Reset Value	Description				
rsvd00		0 1		-	WPRI	-	Reserved				
addr		1	63	false	WARL	0x0	Machine exception program counter.				

mcause											
Address	0x03	42									
Size	64										
Reset Value	0x00	0000000000000									
Description	Mach	Machine trap cause.									
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
oveentioneed	مساحا	0	63			0x0	Code identifying the last exception				
exceptioncod	ewin	0	63	false	WARL	UXU	or interrupt				
interrupt		63	1	false	WARL	0x0	Indicates if the trap was caused by				
		63 1		laise	VVANL	UXU	an interrupt				

mtval						
Address	0x0343					
Size	64					
Reset Value	0x000000000000					
Description	Machine bad address or instruction or machine trap value register.					

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
mtval	0	64	false	WARL	0x0	Machine Trap Value Register

mip	mip									
Address	0x03	x0344								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Description Machine interrupt pending.									
Field Nam	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
rsvd00		0	1	-	WPRI	-	Reserved			
ssip		1	1	true	WARL	0x0	Supervisor Software Interrupt Pending			
vssip		2	1	true	WARL	0x0	Virtual Supervisor Software Interrupt Pending			
msip		3	1	true	WARL	0×0	Machine Software Interrupt Pending			
rsvd44		4	1	-	WPRI	-	Reserved			
stip		5	1	true	WARL	0x0	Supervisor Timer Interrupt Pending			
vstip		6	1	true	WARL	0x0	Virtual Supervisor Timer Interrupt Pending			
mtip		7	1	true	WARL	0x0	Machine Timer Interrupt Pending			
rsvd88		8	1	-	WPRI	-	Reserved			
seip		9	1	true	WARL	0x0	Supervisor External Interupt Pending			
vseip		10	1	true	WARL	0x0	Virtual Supervisor External Interupt Pending			
meip		11	1	true	WARL	0x0	Machine External Interupt Pending			
sgeip		12	1	true	WARL	0x0	Supervisor Guest External Interupt Pending			
Icofip		13	1	true	WARL	0x0	Local Count Overflow Interrupt Pending			
rsvd1514		14	2	-	WPRI	-	Reserved			
nonstandardii	nterr	16	48	true	WARL	0x0	Definition of many of these interrupt numbers is either custom or non-ratified. So, these bits must be			
'							flexible			

mtinst										
Address	0x03	034A								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Mach	Machine mode trap instruction (transformed).								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
mtinst		0	64	false	WARL	0x0	Machine Trap Instruction Register			

mtval2	tval2									
Address	0x03	034B								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Mach	lachine mode bad guest physical address.								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
mtval2		0	64	false	WARL	0x0	Machine Second Trap Value Register			

miselect	miselect									
Address	0x03	x0350								
Size	64	64								
Reset Value	0x00	0×000000000000								
Description	Mach	Machine Indirect register select (valid range is 0 - 0xFF)								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
interrupts		0	8	false	WARL	0x0	0x30 - 0x3F : Major Intr priorities0x70-0xFF: External Intr. (0x71, 0x73-0x7F are rsvd)Rest: Reserved			
rsvd_63_8		8	56	false	WARL	0x0	Reserved for future use			

mireg	g									
Address	0x03	x0351								
Size	64	ý4								
Reset Value	0x00	0000000000	0000							
Description	Mach	ine indirect i	egister alias							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
mireg		0	64	false	WARL	0x0	Machine indirect register alias			

mtopei										
Address	0x03	x035C								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description		Machine top external interrupt (This is marked as read-write in AIA spec, but implemented as read-only for write to this CSR is ignored)								
Field Nan	1e	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
priority		0	11	true	WARL	0x0	Interrupt priority (same as identity)			
rsvd_15_11		11	5	true	WARL	0x0	Reserved for future use			
identity		16	11	true	WARL	0x0	Interrupt identity			
rsvd_63_27		27	37	true	WARL	0x0	Reserved for future use			

pmpcfg0

Address	0x03A0					
Size	ze 64					
Reset Value	0x000000000000					
Description Physical memory protection configuration.						

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
nmnOcfa ruy	0	2	false	WARL	0×0	PMP Config Register RWX
pmp0cfg_rwx	0	3	laise	WARL	0x0	(Read/Write/Execute) bits for PMP0
pmp0cfg_mode	3	2	false	WARL	0×0	PMP Config Register A (Address
priipocig_mode	3	2	laise	WARL	000	Matching Mode) bits for PMP0
pmp0cfg_rsvd	5	2	false	WARL	0x0	PMP Config Register Rsvd bits for
priipocig_rsva	5	2	laise	WARL	000	PMP0
nmn0sfa laskad	7	1	false	WARL	0×0	PMP Config Register L (Locked) bit
pmp0cfg_locked	7	1	laise	WARL	0x0	for PMP0
nmn1cfg_rwy	0	3	false	WADI	0.40	PMP Config Register RWX
pmp1cfg_rwx	8	3	laise	WARL	0x0	(Read/Write/Execute) bits for PMP1
n ma m 1 afar ma a d a	11	2	foloo	WADI	0.40	PMP Config Register A (Address
pmp1cfg_mode	11	2	false	WARL	0x0	Matching Mode) bits for PMP1
1.6	12	2		IA/A D.I		PMP Config Register Rsvd bits for
pmp1cfg_rsvd	13	2	false	WARL	0x0	PMP1
	15	-	f-1	MADI	00	PMP Config Register L (Locked) bit
pmp1cfg_locked	15	1	false	WARL	0x0	for PMP1
mman Jafa, muu	16	3	false	WARL	0×0	PMP Config Register RWX
pmp2cfg_rwx						(Read/Write/Execute) bits for PMP2
n man 2 afar ma a da	10	2	false	WARL	0×0	PMP Config Register A (Address
pmp2cfg_mode	19					Matching Mode) bits for PMP2
mmom Defer moved	21	2	folos	NA DI	00	PMP Config Register Rsvd bits for
pmp2cfg_rsvd	21	2	false	WARL	0x0	PMP2
nmn3cfa lackad	22	1	falso	WARL	0×0	PMP Config Register L (Locked) bit
pmp2cfg_locked	23	1	false	WARL	0x0	for PMP2
nmn2cfa ruy	24	2	falso	WADI	0.40	PMP Config Register RWX
pmp3cfg_rwx	24	3	false	WARL	0x0	(Read/Write/Execute) bits for PMP3
mmom Zofer, mondo	27	2	foloo	WADI	0×0	PMP Config Register A (Address
pmp3cfg_mode	27	2	false	WARL	0x0	Matching Mode) bits for PMP3
n man 2 afar may d	20	2	foloo	MADI	0.40	PMP Config Register Rsvd bits for
pmp3cfg_rsvd	29	2	false	WARL	0x0	PMP3
	21	-	f-1	MADI	00	PMP Config Register L (Locked) bit
pmp3cfg_locked	31	1	false	WARL	0x0	for PMP3
n no n 1 of a	22	2	false	WADI	0.0	PMP Config Register RWX
pmp4cfg_rwx	32	3	false	WARL	0x0	(Read/Write/Execute) bits for PMP4
4.6	25	2		MARI		PMP Config Register A (Address
pmp4cfg_mode	35	2	false	WARL	0×0	Matching Mode) bits for PMP4
						PMP Config Register Rsvd bits for
pmp4cfg_rsvd	37	2	false	WARL	0x0	PMP4

pmp4cfg_locked	39	1	false	WARL	0x0	PMP Config Register L (Locked) bit for PMP4
pmp5cfg_rwx	40	3	false	WARL	0×0	PMP Config Register RWX (Read/Write/Execute) bits for PMP5
pmp5cfg_mode	43	2	false	WARL	0x0	PMP Config Register A (Address Matching Mode) bits for PMP5
pmp5cfg_rsvd	45	2	false	WARL	0x0	PMP Config Register Rsvd bits for PMP5
pmp5cfg_locked	47	1	false	WARL	0x0	PMP Config Register L (Locked) bit for PMP5
pmp6cfg_rwx	48	3	false	WARL	0x0	PMP Config Register RWX (Read/Write/Execute) bits for PMP6
pmp6cfg_mode	51	2	false	WARL	0x0	PMP Config Register A (Address Matching Mode) bits for PMP6
pmp6cfg_rsvd	53	2	false	WARL	0x0	PMP Config Register Rsvd bits for PMP6
pmp6cfg_locked	55	1	false	WARL	0x0	PMP Config Register L (Locked) bit for PMP6
pmp7cfg_rwx	56	3	false	WARL	0x0	PMP Config Register RWX (Read/Write/Execute) bits for PMP7
pmp7cfg_mode	59	2	false	WARL	0×0	PMP Config Register A (Address Matching Mode) bits for PMP7
pmp7cfg_rsvd	61	2	false	WARL	0x0	PMP Config Register Rsvd bits for PMP7
pmp7cfg_locked	63	1	false	WARL	0×0	PMP Config Register L (Locked) bit for PMP7

Address	0x03	x03A2										
Size	64	54										
Reset Value	0x00	0000000000	0000									
Description	Phys	ical memory	protection co	onfiguration.								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description					
amp@cfg_ruw	,	0	3	false	WARL	0x0	PMP Config Register RWX					
pmp8cfg_rwx		0	3	raise	WARL	UXU	(Read/Write/Execute) bits for PMP8					
nmp0sfa ma	da	3	2	false	WARL	0x0	PMP Config Register A (Address					
pmp8cfg_mo	ue				WARL	0.00	Matching Mode) bits for PMP8					
omp@cfa_rcv	4	5	2	false	WARL	0x0	PMP Config Register Rsvd bits for					
pmp8cfg_rsv	J	3	2	iaise	WARL	000	PMP8					
nmn9efa loel	rod.	7	1	false	WARL	0x0	PMP Config Register L (Locked) bit					
pmp8cfg_locl	Keu	,	1	laise	WARL	000	for PMP8					
ompOcfa rus	,	0	2	false	WADI	0×0	PMP Config Register RWX					
pmp9cfg_rwx		8	3	iaise	WARL	UXU	(Read/Write/Execute) bits for PMP9					

						PMP Config Register A (Address
pmp9cfg_mode	11	2	false	WARL	0x0	Matching Mode) bits for PMP9
						-
pmp9cfg_rsvd	13	2	false	WARL	0x0	PMP Config Register Rsvd bits for
						PMP9
pmp9cfg_locked	15	1	false	WARL	0x0	PMP Config Register L (Locked) bit
						for PMP9
pmp10cfg_rwx	16	3	false	WARL	0x0	PMP Config Register RWX
						(Read/Write/Execute) bits for PMP10
pmp10cfg_mode	19	2	false	WARL	0x0	PMP Config Register A (Address
pp200.9000			14.55			Matching Mode) bits for PMP10
nmn10cfg_rcvd	21	2	false	WARL	0x0	PMP Config Register Rsvd bits for
pmp10cfg_rsvd	21	2	laise	WARL	0.00	PMP10
10.5.1.1.1						PMP Config Register L (Locked) bit
pmp10cfg_locked	23	1	false	WARL	0x0	for PMP10
						PMP Config Register RWX
pmp11cfg_rwx	24	3	false	WARL	0x0	(Read/Write/Execute) bits for PMP11
						PMP Config Register A (Address
pmp11cfg_mode	27	2	false	WARL	0x0	Matching Mode) bits for PMP11
						PMP Config Register Rsvd bits for
pmp11cfg_rsvd	29	2	false	WARL	0x0	PMP11
pmp11cfg_locked	31	1	false	WARL	0x0	PMP Config Register L (Locked) bit
						for PMP11
pmp12cfg_rwx	32	3	false	WARL	0x0	PMP Config Register RWX
						(Read/Write/Execute) bits for PMP12
pmp12cfg_mode	35	2	false	WARL	0x0	PMP Config Register A (Address
						Matching Mode) bits for PMP12
pmp12cfg_rsvd	37	2	false	WARL	0x0	PMP Config Register Rsvd bits for
			14.55		57.0	PMP12
pmp12cfg_locked	39	1	false	WARL	0x0	PMP Config Register L (Locked) bit
pilipizeig_locked	139		laise	WARL	OXO	for PMP12
12.6	40		6.1	WARI	0.0	PMP Config Register RWX
pmp13cfg_rwx	40	3	false	WARL	0x0	(Read/Write/Execute) bits for PMP13
						PMP Config Register A (Address
pmp13cfg_mode	43	2	false	WARL	0x0	Matching Mode) bits for PMP13
						PMP Config Register Rsvd bits for
pmp13cfg_rsvd	45	2	false	WARL	0x0	PMP13
						PMP Config Register L (Locked) bit
pmp13cfg_locked	47	1	false	WARL	0x0	for PMP13
						PMP Config Register RWX
pmp14cfg_rwx	48	3	false	WARL	0x0	
						(Read/Write/Execute) bits for PMP14
pmp14cfg_mode	51	2	false	WARL	0x0	PMP Config Register A (Address
						Matching Mode) bits for PMP14

pmp14cfg_rsvd	53	2	false	WARL	0×0	PMP Config Register Rsvd bits for PMP14
pmp14cfg_locked	55	1	false	WARL	0×0	PMP Config Register L (Locked) bit for PMP14
pmp15cfg_rwx	56	3	false	WARL	0×0	PMP Config Register RWX (Read/Write/Execute) bits for PMP15
pmp15cfg_mode	59	2	false	WARL	0×0	PMP Config Register A (Address Matching Mode) bits for PMP15
pmp15cfg_rsvd	61	2	false	WARL	0×0	PMP Config Register Rsvd bits for PMP15
pmp15cfg_locked	63	1	false	WARL	0×0	PMP Config Register L (Locked) bit for PMP15

pmpaddr	pmpaddr0										
Address	0x03	x03B0									
Size	64										
Reset Value	0x00	0000000000	01FF								
Description	Physi	ical memory	protection co	onfiguration.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
address_lo		0 9 false WARL 0x1FF PMP0 address bits 10:2									
address_hi		9 45 false WARL 0x0 PMP0 address bits 55:11									
rsvd6454		54	10	-	WPRI	-	Reserved				

pmpaddr	1										
Address	0x03	0x03B1									
Size	64										
Reset Value	0x00	0000000000	01FF								
Description	Phys	ical memory	protection co	onfiguration.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
address_lo		0 9 false WARL 0x1FF PMP1 address bits 10:2									
address_hi		9 45 false WARL 0x0 PMP1 address bits 55:11									
rsvd6454		54	10	-	WPRI	-	Reserved				

pmpaddr	pmpaddr2									
Address	0x03	B2								
Size	64									
Reset Value	0x00	0000000000	01FF							
Description	Phys	ical memory	protection co	onfiguration.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
address_lo		0 9 false WARL 0x1FF PMP2 address bits 10:2								
address_hi		9	45	false	WARL	0x0	PMP2 address bits 55:11			

	rsvd6/15/1	54	10	_	WPRI	_	Reserved
-	15000454	54	10	-	WPKI	-	Reserved

pmpaddr	pmpaddr3										
Address	0x03	B3									
Size	64										
Reset Value	0x00	0000000000	01FF								
Description	Phys	ical memory	protection co	onfiguration.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
address_lo		0 9 false WARL 0x1FF PMP3 address bits 10:2									
address_hi		9 45 false WARL 0x0 PMP3 address bits 55:11									
rsvd6454		54	10	-	WPRI	-	Reserved				

pmpaddr	pmpaddr4										
Address	0x03	0x03B4									
Size	64										
Reset Value	0x00	0000000000	01FF								
Description	Physi	ical memory	protection co	onfiguration.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
address_lo		0 9 false WARL 0x1FF PMP4 address bits 10:2									
address_hi		9 45 false WARL 0x0 PMP4 address bits 55:11									
rsvd6454		54	10	-	WPRI	-	Reserved				

pmpaddr	pmpaddr5										
Address	0x03	B5									
Size	64										
Reset Value	0x00	0000000000	01FF								
Description	Physi	ical memory	protection co	onfiguration.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
address_lo		0 9 false WARL 0x1FF PMP5 address bits 10:2									
address_hi		9 45 false WARL 0x0 PMP5 address bits 55:11									
rsvd6454		54	10	-	WPRI	-	Reserved				

pmpaddr	pmpaddr6										
Address	0x03	B6									
Size	64										
Reset Value	0x00	0000000000	01FF								
Description	Physi	ical memory	protection co	onfiguration.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
address_lo		0 9 false WARL 0x1FF PMP6 address bits 10:2									
address_hi		9 45 false WARL 0x0 PMP6 address bits 55:11									
rsvd6454		54	10	-	WPRI	-	Reserved				

pmpaddr7									
Address	0x03	0x03B7							
Size	64								
Reset Value	0x00	0000000000	01FF						
Description	Phys	ical memory	protection co	onfiguration.					
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description		
address_lo	0 9		9	false	WARL	0x1FF	PMP7 address bits 10:2		
address_hi		9 45 false WARL 0x0 PMP7 address bits 55:11							
rsvd6454		54	10	-	WPRI	-	Reserved		

pmpaddr	pmpaddr8									
Address	0x03	x03B8								
Size	64									
Reset Value	0x00	0000000000	01FF							
Description	Physi	ical memory	protection co	onfiguration.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
address_lo		0	9	false	WARL	0x1FF	PMP8 address bits 10:2			
address_hi	9 45 false WARL 0x0 PMP8 address I						PMP8 address bits 55:11			
rsvd6454		54	10	-	WPRI	-	Reserved			

pmpaddr9											
Address	0x03	x03B9									
Size	64	4									
Reset Value	0x00	0000000000	01FF								
Description	Phys	ical memory	protection co	onfiguration.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
address_lo		0	9	false	WARL	0x1FF	PMP9 address bits 10:2				
address_hi	9 45 false WARL 0x0 PMP9					PMP9 address bits 55:11					
rsvd6454		54	10	-	WPRI	-	Reserved				

pmpaddr	pmpaddr10									
Address	0x03	x03BA								
Size	64									
Reset Value	0x00	0000000000	01FF							
Description	Physi	ical memory	protection co	onfiguration.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
address_lo		0	9	false	WARL	0x1FF	PMP10 address bits 10:2			
address_hi	9 45 false WARL 0x0 PMP10 address bits 55:11						PMP10 address bits 55:11			
rsvd6454		54	10	-	WPRI	-	Reserved			

pmpaddr11

Address	0x03	x03BB									
Size	64	4									
Reset Value	0x00	x00000000001FF									
Description	Phys	Physical memory protection configuration.									
Field Name Bit Offs					1						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
Field Nan	ne	Bit Offset 0	Bit Width 9	Volatile false	Access WARL	Reset Value 0x1FF	PMP11 address bits 10:2				
	ne						•				

pmpaddr	pmpaddr12										
Address	0x03	x03BC									
Size	64										
Reset Value	0x00	0000000000	01FF								
Description	Phys	ical memory	protection co	onfiguration.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
address_lo		0 9		false	WARL	0x1FF	PMP12 address bits 10:2				
address_hi	9 45 false WARL 0x0 PN						PMP12 address bits 55:11				
rsvd6454		54	10	-	WPRI	-	Reserved				

pmpaddr	pmpaddr13									
Address	0x03	x03BD								
Size	64									
Reset Value	0x00	0000000000	01FF							
Description	Physi	ical memory	protection co	onfiguration.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
address_lo		0	9	false	WARL	0x1FF	PMP13 address bits 10:2			
address_hi	9 45 false WARL			WARL	0x0	PMP13 address bits 55:11				
rsvd6454		54	10	-	WPRI	-	Reserved			

pmpaddr14										
Address	0x03	x03BE								
Size	64									
Reset Value	0x00	0000000000	01FF							
Description	Physi	ical memory	protection co	onfiguration.						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
address_lo	0 9 false WARL 0x1FF			0x1FF	PMP14 address bits 10:2					
address_hi	9 45 false WARL 0x0 PMP14 address bits 55:11						PMP14 address bits 55:11			
rsvd6454		54	10	-	WPRI	-	Reserved			

pmpaddr	·15
Address	0x03BF

Size	64	4									
Reset Value	0x00	×00000000001FF									
Description	Phys	ical memory	protection co	onfiguration.							
Field Nan	ield Name Bit Offset		Bit Width	Volatile	Access	Reset Value	Description				
address_lo	ess_lo 0		9	false	WARL	0x1FF	PMP15 address bits 10:2				
address_hi	9 45 false WARL 0x0 PMP15 address bits 55:1					PMP15 address bits 55:11					
rsvd6454	rsvd6454 54		10	-	WPRI	-	Reserved				

hstatus	hstatus									
Address	0x06	000								
Size	64									
Reset Value	0x00	0000020000	0000							
Description	Нуре	ervisor status	register.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
wpri_0		0	5	true	WPRI	0x0	WPRI			
							Controls Endianness of explicit			
vsbe		5	1	true	WARL	0x0	memory accesses made from			
							VS-mode			
au co		6	1	truo	WARL	0×0	Indicates a Guest Virtual Address is			
gva		0	1	true	WARL	UXU	written into stval			
		7	1	.	WADI	00	Supervisor Previous Virtualization			
spv		7	1	true	WARL	0x0	Mode			
spvp		8	1	true	WARL	0x0	Supervisor Previous Virtual Privilege			
hu		9	1	truo	WARL	0×0	Controls whether HLV, HLVX, and			
hu		9	1	true	WARL	UXU	HSV can be used in U-mode			
wpri_1		10	2	true	WPRI	0x0	WPRI			
							Selects a guest external interrupt			
vgein		12	6	true	WARL	0x0	source for VS-level external			
							interrupts			
wpri_2		18	2	true	WPRI	0x0	WPRI			
							Makes SFENCE.VMA, SINVAL.VMA,			
vtvm		20	1	true	WARL	0x0	and accesses to satp raise virtual			
							instruction exceptions			
							Makes WFI in VS-mode raises virtual			
vtw		21	1	true	WARL	0x0	instruction exception if not			
							completed within a time limit			
vtcr		22	1	truc	WARL	0×0	Makes SRET give virtual instruction			
vtsr		22	1	true	WARL	UXU	exception in VS-mode			
wpri_3		23	9	true	WPRI	0x0	WPRI			
vsxl		32	2	truo	WARL	0x2	Controls the effective XLEN for			
VSXI		32		true	WARL	UXZ	VS-mode			
wpri_4		34	14	true	WPRI	0x0	WPRI			
			!		•		1			

hupmm	48	2	true	WARL	0x0	Configures pointer masking according to ssnpm extension
wpri_5	50	14	true	WPRI	0x0	WPRI

hedeleg										
Address	0x06	0602								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Нуре	ypervisor exception delegation register.								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
hedeleg_0		0	9	false	WARL	0x0	Exception Codes 0-9			
hard0_0		9	3	false	WARL	0x0	Hardwired 0			
hedeleg_1		12	2	false	WARL	0x0	Exception Codes 12-13			
hard0_1		14	1	false	WARL	0x0	Hardwired 0			
hedeleg_2		15	1	false	WARL	0x0	Exception Code 15			
hedeleg_3	edeleg_3 16		4	false	WARL	0x0	Exception Codes 16-19			
hard0_2		20	4	false	WARL	0x0	Hardwired 0			
hard0_3		24	40	false	WARL	0x0	Hardwired 0			

hideleg

Address	0x06	k0603									
Size	64	4									
Reset Value	0x00	x00000000000000									
Description	Нуре	ervisor interru	upt delegatio	n register.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
rsvd00		0	1	-	WPRI	-	Reserved				
hard0_0		1	1	false	WARL	0x0	Hardwired 0				
		2	-	false	NA DI	00	Delegate Virtual Supervisor Software				
vssip		2	1	Taise	WARL	0x0	Interrupt				
hard0_1		3	1	false	WARL	0x0	Hardwired 0				
rsvd44		4	1	-	WPRI	-	Reserved				
hard0_2		5	1	false	WARL	0x0	Hardwired 0				
vetin		6	1 fa	false WARL	WADI	0x0	Delegate Virtual Supervisor Timer				
vstip		6			WARL		Interrupt				
hard0_3		7	1	false	WARL	0x0	Hardwired 0				
rsvd88		8	1	-	WPRI	-	Reserved				
hard0_4		9	1	false	WARL	0x0	Hardwired 0				
vecin		10	1	false	WARL	0×0	Delegate Virtual Supervisor External				
vseip		10	1	laise	WARL	0x0	Interrupt				
hard0_5		11	2	false	WARL	0x0	Hardwired 0				
Icofin		12	1	falso	WARL	0×0	Hardwired 0 Delegate Local Count				
Icofip		13	1 false	WAKL	UXU	Overflow Interrupt					

rsvd6414	14	50	_	WPRI	-	Reserved

hie	
Address	0x0604
Size	64
Reset Value	0×000000000000
Description	Hypervisor interrupt-enable register.

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description		
rsvd00	0	1	-	WPRI	-	Reserved		
hard0_0	1	1	false	WARL	0x0	Hardwired 0		
vssie	2	1	false	WARL	0×0	Virtual Supervisor Software Interrupt		
VSSIE	2	1	iaise	WARL	OXO	Enable		
hard0_1	3	1	false	WARL	0x0	Hardwired 0		
rsvd44	4	1	-	WPRI	-	Reserved		
hard0_2	5	1	false	WARL	0x0	Hardwired 0		
vstio	6	1	false	WARL	0x0	Virtual Supervisor Timer Interrupt		
vstie	0		Tuise	VVAILE	0.00	Enable		
hard0_3	7	1	false	WARL	0x0	Hardwired 0		
rsvd88	8	1	-	WPRI	-	Reserved		
hard0_4	9	1	false	WARL	0x0	Hardwired 0		
vseie	10	1	false	WARL	0x0	Virtual Supervisor External Interrupt		
vseie			laise	WARL	0.00	Enable		
hard0_5	11	1	false	WARL	0x0	Hardwired 0		
sgeie	12	1	false	WARL	0x0	Supervisor Guest External Interrupt		
) sycie	12		10156	WANL	0.00	Enable		
rsvd6413	13	51	-	WPRI	-	Reserved		

htimedel	htimedelta									
Address	0x06	x0605								
Size	64									
Reset Value	0x00	x0000000000000								
Description	Delta	for VS/VU-m	node timer.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
htimedelta	0 64		false	WARL	0x0	Delta value between time and VS/VU mode timer				

hcounter	hcounteren									
Address	0x06	606								
Size	32									
Reset Value	0x00	000000								
Description	Нуре	ypervisor counter enable.								
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								

су	0	1	false	WARL	0x0	Cycle Counter Enable
tm	1	1	false	WARL	0x0	Time Counter Enable
ir	2	1	false	WARL	0x0	Instruction Retired Counter Enable
						Hardware Performance Monitoring
hpm3	3	1	false	WARL	0x0	Counter 3 Enable
						Hardware Performance Monitoring
hpm4	4	1	false	WARL	0x0	Counter 4 Enable
						Hardware Performance Monitoring
hpm5	5	1	false	WARL	0x0	Counter 5 Enable
						Hardware Performance Monitoring
hpm6	6	1	false	WARL	0x0	Counter 6 Enable
	_	_				Hardware Performance Monitoring
hpm7	7	1	false	WARL	0x0	Counter 7 Enable
h m ma O	0	1	foloo	WADI	00	Hardware Performance Monitoring
hpm8	8	1	false	WARL	0x0	Counter 8 Enable
hpm9	9	1	false	WARL	0x0	Hardware Performance Monitoring
пршэ	9	1	laise	WARL	0.00	Counter 9 Enable
hpm10	10	1	false	WARL	0x0	Hardware Performance Monitoring
Принто	10	1	laise	WARL	0.00	Counter 10 Enable
hpm11	11	1	false	WARL	0x0	Hardware Performance Monitoring
принтт	pilli II	_	laise	WAILE	OXO	Counter 11 Enable
hpm12	12	1	false	WARL	0x0	Hardware Performance Monitoring
TIPITI 2	12	-	Tuise	VV/U(L	oxo .	Counter 12 Enable
hpm13	13	1	false	WARL	0x0	Hardware Performance Monitoring
		_	laise	With	o.co	Counter 13 Enable
hpm14	14		false	WARL	0x0	Hardware Performance Monitoring
						Counter 14 Enable
hpm15	15	1	false	WARL	0x0	Hardware Performance Monitoring
·						Counter 15 Enable
hpm16	16	1	false	WARL	0x0	Hardware Performance Monitoring
						Counter 16 Enable
hpm17	17	1	false	WARL	0×0	Hardware Performance Monitoring
						Counter 17 Enable
hpm18	18	1	false	WARL	0x0	Hardware Performance Monitoring
						Counter 18 Enable
hpm19	19	1	false	WARL	0x0	Hardware Performance Monitoring
						Counter 19 Enable
hpm20	20	1	false	WARL	0x0	Hardware Performance Monitoring
						Counter 20 Enable
hpm21	21	1	false	WARL	0x0	Hardware Performance Monitoring
						Counter 21 Enable
hpm22	22	1	false	WARL	0x0	Hardware Performance Monitoring
						Counter 22 Enable

hpm23	23	1	false	WARL	0x0	Hardware Performance Monitoring Counter 23 Enable
hpm24	24	1	false	WARL	0x0	Hardware Performance Monitoring Counter 24 Enable
hpm25	25	1	false	WARL	0×0	Hardware Performance Monitoring Counter 25 Enable
hpm26	26	1	false	WARL	0×0	Hardware Performance Monitoring Counter 26 Enable
hpm27	27	1	false	WARL	0x0	Hardware Performance Monitoring Counter 27 Enable
hpm28	28	1	false	WARL	0×0	Hardware Performance Monitoring Counter 28 Enable
hpm29	29	1	false	WARL	0×0	Hardware Performance Monitoring Counter 29 Enable
hpm30	30	1	false	WARL	0×0	Hardware Performance Monitoring Counter 30 Enable
hpm31	31	1	false	WARL	0x0	Hardware Performance Monitoring Counter 31 Enable

hgeie										
Address	0x06	0607								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Нуре	ypervisor guest external interrupt-enable register.								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
hard0_0		0	1	false	WARL	0x0	Read-only zeros			
guestexterna	guestexternalinte		5	false	WARL	0x0	Ascalon supports up to 5 guest			
rruptswarl		T	5	laise	WANL	0.00	supervisor-level interrupt files			
hard0_1		6	58	false	WARL	0x0	Read-only zeros			

hvien	hvien									
Address	0x06	x0608								
Size	64									
Reset Value	0x00	x0000000000000								
Description	Нуре	Hypervisor virtual interrupt enables								
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
hard0_0	0		13	false	WARL	0x0	Hardwired 0			
Icofip	13 1 false			false	WARL	0x0	Local Count Overflow Interrupt			
rsvd6414		14	50	-	WPRI	-	Reserved			

hvictl	
Address	0x0609

Size	64	64									
Reset Value	0x00	0x0000000000000									
Description	Нуре	rvisor virtual	l interrupt co	ntrol							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
iprio		0	8	false	WARL	0x0	Interrupt Priority				
ipriom 8		8	1	false	WARL	0x0	IPRIO Mode				
dpr 9		9	1	false	WARL	0x0	Default Priority Rank				
rsvd1510		10	6	-	WPRI	-	Reserved				
iid		16	6	false	WARL	0x0	Interrupt Identity				
rsvd2922	22 8 - WPRI - Reserved						Reserved				
vti		30 1 false WARL 0x0 Virtual Trap Interrupt control									
rsvd6431		31	33	-	WPRI	-	Reserved				

henvcfg										
Address	0x06	0x060A								
Size	64									
Reset Value	0x00	0x000000000000								
Description	Нуре	ervisor enviro	nment confi	guration regi	ster.					
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
fiom		0	1	false	WARL	0x0	Fence of I/O implies Memory			
wpri_0		1	3	false	WPRI	0x0	WPRI			
							Cache Block Invalidate instruction			
cbie		4	2	false	WARL	0x0	Enable Enables the execution of			
							CBO.INVAL in a lower privilege mode			
							Cache Block Clean and Flush			
ah afa		6 1		false	WARL	0x0	instruction enable Enables			
cbcfe			1				execution of CBO.CLEAN and			
							CBO.FLUSH in a lower privilege mode			
							Cache Block Zero instruction Enable			
cbze		7	1	false	WARL	0x0	Enables execution of CBO.ZERO in			
							a lower privilege mode			
wpri_1		8	24	false	WPRI	0x0	WPRI			
nmm		32	2	false	WARL	0×0	Enables pointer masking for			
pmm		32	2	laise	WARL	0x0	VS-mode			
wpri_2		34	27	false	WPRI	0x0	WPRI			
							Enables hardware updating of PTE			
hade		61	1	false	WARL	0x0	A/D bits during VS-stage address			
							translation			
nhmta		62	1	falso	WADI	0.40	Enables Sypbmt extension for			
pbmte		62	1	false	WARL	0x0	VS-stage address translation			
vstce		63	1	false	WARL	0x0	Enables VSTimecmp for VS-mode			

hstateen0

Address	0x060C
Size	64
Reset Value	0x000000000000
Description	Hypervisor State Enable 0

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
С	0	1	false	WARL	0x0	Controls access to any and all
			laise	WARL	0.00	custom state
fcsr	1	1	false	WARL	0x0	Controls access to fcsr CSR
jvt	2	1	false	WARL	0x0	Controls access to JVT CSR
wpri_0	3	54	false	WPRI	0x0	WPRI
context	57	1	false	WARL	0x0	Controls access to the scontext CSR
imsic	58	1	false	WARL	0x0	Controls access to IMSIC state
aia	59	1	false	WARL	0x0	Controls access to all state
aia	139		laise	WARL	0.00	introduced by the Ssaia extension
csrind	60	1	false	WARL	0x0	Controls access to siselect, sireg*,
CSIIIu	00	1	iaise	WARL	0.00	vsiselect, vsireg* CSRs
wpri_1	61	1	false	WPRI	0x0	WPRI
envcfg	62	1	false	WARL	0x0	Controls access to the senvcfg CSR
se0	63	1	false	WARL	0x0	Controls access to the sstateen0 CSR

hstateen	hstateen1								
Address	0x06	0D							
Size	64								
Reset Value	0x00	0000000000	0000						
Description	Нуре	rvisor State	Enable 1						
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description		
wpri		0 63 false WPRI 0x0 WPRI							
se1		63	1	false	WARL	0x0	Controls access to the sstateen1 CSR		

hstateen	hstateen2									
Address	0x06	x060E								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Нуре	ervisor State	Enable 2							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
wpri		0 63 false WPRI 0x0 WPRI								
se2		63	1	false	WARL	0x0	Controls access to the sstateen2 CSR			

hstateen	hstateen3						
Address	0x060F						
Size	64						
Reset Value	0x000000000000						

Description	Hypervisor State Enable 3								
Field Nan	eld Name Bit Offset Bit Width Volatile Access Reset Value Description								
wpri		0	63	false	WPRI	0x0	WPRI		
se3		63	1	false	WARL	0x0	Controls access to the sstateen3 CSR		

htval										
Address	0x06	43								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Нуре	rvisor Trap V	alue Registe	r						
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								
htval		0 64 false WARL 0x0 Hypervisor Trap Value Register								

hip										
Address	0x06	0x0644								
Size	64	54								
Reset Value	0x00	0000000000	0000							
Description	Нуре	ervisor interru	upt pending.							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description			
rsvd00		0	1	-	WPRI	-	Reserved			
hard0_0		1	1	false	WARL	0x0	Hardwired 0			
vssip		2	1	false	WARL	0×0	Virtual Supervisor Software Interrupt Pending			
hard0_1		3	1	false	WARL	0x0	Hardwired 0			
rsvd44		4	1	-	WPRI	-	Reserved			
hard0_2		5	1	false	WARL	0x0	Hardwired 0			
vstip		6	1	false	WARL	0×0	Virtual Supervisor Timer Interrupt Pending			
hard0_3		7	1	false	WARL	0x0	Hardwired 0			
rsvd88		8	1	-	WPRI	-	Reserved			
hard0_4		9	1	false	WARL	0x0	Hardwired 0			
vseip		10	1	false	WARL	0×0	Virtual Supervisor External Interrupt Pending			
hard0_5		11	1	false	WARL	0x0	Hardwired 0			
sgeip		12	1	false	WARL	0×0	Supervisor Guest External Interrupt Pending			
rsvd6413		13	51	-	WPRI	-	Reserved			

hvip	
Address	0x0645
Size	64
Reset Value	0x000000000000

Description	Нуре	ervisor virtual	interrupt pe	nding.			
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
rsvd00		0	1	-	WPRI	-	Reserved
hard0_0		1	1	true	WARL	0x0	Hardwired 0
vesin		2	1	true	WARL	0x0	Virtual Supervisor Software Interrupt
vssip		2	1	true	WARL	UXU	Pending
hard0_1		3	1	true	WARL	0x0	Hardwired 0
rsvd44		4	1	-	WPRI	-	Reserved
hard0_2		5	1	true	WARL	0x0	Hardwired 0
votin virt		6	1	true	WARL	0×0	Virtual Supervisor Timer Interrupt
vstip_virt							Pending
hard0_3		7	1	true	WARL	0x0	Hardwired 0
rsvd88		8	1	-	WPRI	-	Reserved
hard0_4		9	1	true	WARL	0x0	Hardwired 0
vecin virt		10	1	true	WARL	0x0	Virtual Supervisor External Interrupt
vseip_virt			1	true	WARL	UXU	Pending
hard0_5		11	2	true	WARL	0x0	Hardwired 0
Icofin virt		13	1	truo	WARL	0.0	Local Count Overflow Interrupt
lcofip_virt		13	1	true	WARL	0x0	Pending
rsvd6414		14	50	-	WPRI	-	Reserved

hviprio1	hviprio1											
Address	0x06	0x0646										
Size	64	4										
Reset Value	0x00	0x0000000000000										
Description	Нуре	rvisor VS-lev	el interrupt p	oriorities 1	Assumed to	be 0 for Athena. Lives in	MC for this limited implementation					
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description					
hviprio1		0	64	false	WARL	0x0	Hypervisor VS-level interrupt					
ΠΛΙΡΙΙΟΙ	nviprio1		0 64		WANL	UXU	priorities 1					

hviprio2	hviprio2											
Address	0x06	x0647										
Size	64	4										
Reset Value	0x00	0x000000000000										
Description	Нуре	rvisor VS-lev	el interrupt p	oriorities 2	Assumed to	be 0 for Athena. Lives in	MC for this limited implementation					
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description					
hviprio2		0	64	false	WARL	0×0	Hypervisor VS-level interrupt priorities 2					

htinst	
Address	0x064A
Size	64

	Reset Value	0x00	x0000000000000										
Ī	Description	Нуре	ypervisor trap instruction (transformed).										
Field Name Bit Offset Bit Width Volatile Access Reset Value						Description							
ſ	htinst 0		64	false	WARL	0x0	Hypervisor trap Instruction Register						

hgatp	hgatp											
Address	0x06	x0680										
Size	64											
Reset Value	0x00	0000000000	0000									
Description	Нуре	ypervisor guest address translation and protection.										
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description					
ppn		0	44	false	WARL	0x0	Physical Page Number					
vmid		44	14	false	WARL	0x0	Virtual Machine Identifier					
warl0	58 2		2	false	WARL	0x0	Hardwired 0					
mode	ode 60		4	false	WARL	0x0	Address Translation and Protection Mode					

mnscrato	mnscratch										
Address	0x07	0x0740									
Size	64	4									
Reset Value	0x00	0000000000	0000								
Description	Resu	mable NMI so	cratch registe	er							
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description									
mnscratch		0 64 false WARL 0x0 Resumable NMI scratch register									

mnepc	mnepc										
Address	0x07	0x0741									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Resu	mable NMI p	rogram coun	ter							
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
rsvd00		0 1 - WPRI - Reserved									
addr		1 63 false WARL 0x0 Resumable NMI program counter									

mncause	mncause										
Address	0x07	0x0742									
Size	64	4									
Reset Value	0x00	0000000000	0000								
Description	Resu	mable NMI c	ause								
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description									
exceptioncod	е	0 63 false WARL 0x0 Code identifying the last interrupt									

interrupt	63	1	false	WARL	0x0	Indicates if the trap was caused by	
·						an interrupt	l

mnstatus												
Address	0x07	0x0744										
Size	64											
Reset Value	0x00	0000000000	0000									
Description	Resu	esumable NMI status										
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description					
rsvd20		0	3	-	WPRI	-	Reserved					
nmie		3	1	false	WARL	0x0	Non Maskable Interrupt Enable					
rsvd64		4	3	-	WPRI	-	Reserved					
mnpv 7		7	1	false	WARL	0x0	Previous Virtualization Mode					
rsvd108 8		8	3	-	WPRI	-	Reserved					
mnpp 11		2	false	WARL	0x0	Previous Privilege Mode						
rsvd6413		13	51	-	WPRI	-	Reserved					

mseccfg											
Address	0x07	0x0747									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mack	nine security	configuration	register.							
Field Nar	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
mml		0	1	false	WARL	0x0	Machine Mode Lockdown				
mmwp		1	1	false	WARL	0x0	Machine Mode Whitelist Policy				
rlb		2	1	false	WARL	0x0	Rule Locking Bypass				
wpri_0		3	5	false	WPRI	0x0	WPRI				
		8	1	false	WARL	0×0	Controls access to seed CSR in U				
useed		ŏ	1	raise	WARL	UXU	mode				
		9	1	false	WARI	0×0	Controls access to seed CSR in S or				
sseed		9	1	iaise	WARL	UXU	HS mode				
wpri_1		10	22	false	WPRI	0x0	WPRI				
pmm		32	2	false	WARL	0x0	Enables pointer masking for M-mode				
wpri_2		34	30	false	WPRI	0x0	WPRI				

tselect												
Address	0x07	x07A0										
Size	64	4										
Reset Value	0x00	0000000000	0000									
Description	Trigg	Trigger Select										
Field Nan	e Bit Offset Bit Width Volatile Access Reset Value Description											

index	0	64	false	WARL	0x0	These are Trigger Registers from	
macx	Ü		laise		0,00	Debug Spec, not complete	

dcsr	
Address	0x07B0
Size	64
Reset Value	0x0000000000003
Description	Debug Control and Status

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
prv	0	2	false	WARL	0x3	Previous Privilege Mode
step	2	1	false	WARL	0x0	When set and not in Debug Mode, the hart will only execute a single instruction and then enter Debug Mode
nmip	3	1	true	WARL	0x0	When set, there is a Non-Maskable-Interrupt (NMI) pending for the hart
mprven	4	1	false	WARL	0x0	Enable mprv in mstatus taking effect
V	5	1	false	WARL	0x0	Previous Virtualization Mode
cause	6	3	false	WARL	0x0	Explains why Debug Mode was entered
stoptime	9	1	false	WARL	0x0	time CSR is frozen at the time that Debug Mode was entered
stopcount	10	1	false	WARL	0×0	Don't increment any hart-local counters while in Debug Mode or on ebreak instructions causing entry into Debug Mode
stepie	11	1	false	WARL	0x0	Enable Interrupts during single stepping with step set
ebreaku	12	1	false	WARL	0x0	ebreak instructions in U-mode enter Debug Mode
ebreaks	13	1	false	WARL	0x0	ebreak instructions in S-mode enter Debug Mode
hard0_1	14	1	false	WARL	0x0	Hardwired 0
ebreakm	15	1	false	WARL	0x0	ebreak instructions in M-mode enter Debug Mode
hard0_2	16	12	false	WARL	0x0	Hardwired 0
xdebugver	28	4	false	WARL	0x0	Version of Debug Specification implemented
rsvd6432	32	32	-	WPRI	-	Reserved

dpc	
Address	0x07B1

Size	64								
Reset Value	0x00	0×0000000000000							
Description	Debu	Debug PC							
Field Nan	Name Bit Offset Bit Width Volatile Access Reset Value Description								
dpc 0 64 false WARL 0x0 Debug PC					Debug PC				

dscratch	ratch0									
Address	0x07	07B2								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Debu	g Scratch Re	gister 0							
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
dscratch0	0 0 64 false WARL 0x0 Debug Scratch Register 0						Debug Scratch Register 0			

dscratch	dscratch1									
Address	0x07	07B3								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Debu	ıg Scratch Re	gister 1							
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description									
dscratch1 0 64 false WARL 0x0 Debug Scratch Register						Debug Scratch Register 1				

c_matp	tp										
Address	0x07	k07C7									
Size	32										
Reset Value	0x00	000000									
Description	Mach	ine address	translation a	nd protection	۱.						
Field Nan	ame Bit Offset Bit Width Volatile Access Reset Value Description										
swid		0	1	false	WARL	0x0	Secure World Identifier				
rsvd321 1 31 - WPRI - Reserved							Reserved				

mcycle										
Address	0x0B	0800								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	ine cycle cou	ınter.							
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								
cycle	cle 0 64 true WARL 0x0 Counter value						Counter value			

minstret	
Address	0x0B02

Size	64									
Reset Value	0x00	×00000000000000								
Description	Mach	Machine instructions-retired counter.								
Field Nan	me Bit Offset Bit Width Volatile Access Reset Value Description									
instret 0 64 true WARL 0x0 Counter value						Counter value				

mhpmco	nhpmcounter3									
Address	0x0B	0B03								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	ine performa	ance-monitor	ing counter.						
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description									
hpmcounter3 0 64 true WARL 0x0 C					Counter value					

mhpmco	mhpmcounter4									
Address	0x0B	0x0B04								
Size	64	4								
Reset Value	0x00	0×0000000000000								
Description	Mach	ine performa	ance-monitor	ing counter.						
Field Name Bit Offset Bit Width Volatile Access Reset Value			Description							
hpmcounter4 0 64 true WARL 0x0 Counter value				Counter value						

mhpmcounter5									
Address	0x0B	0x0B05							
Size	64	j4							
Reset Value	0x00	0x0000000000000							
Description	Mach	ine performa	ance-monitor	ing counter.					
Field Nan	Name Bit Offset Bit Width Volatile Access Reset Value Description						Description		
hpmcounter5		0 64 true WARL 0x0 Counter value							

mhpmcounter6									
Address	0x0B	0x0B06							
Size	64	4							
Reset Value	0x00	0x0000000000000							
Description	Mach	ine performa	ance-monitor	ing counter.					
Field Name Bit Offset Bit Width Volatile Access Reset Value			Description						
hpmcounter6 0 64 true WARL 0x0 Counter va				Counter value					

mhpmco	unter7
Address	0x0B07
Size	64

Reset Value	0x00	0x0000000000000								
Description	Mach	Machine performance-monitoring counter.								
Field Name Bit Offset			Bit Width	Volatile	Access	Reset Value	Description			
	npmcounter7 0 64 true WARL 0x0 Counter value									

mhpmco	mhpmcounter8									
Address	0x0B	0x0B08								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Machine performance-monitoring counter.									
Field Name Bit Offset Bit Width Volatile Access Reset Value				Description						
hpmcounter8	3 0 64 true WARL 0x0 Counter value					Counter value				

mhpmco	mhpmcounter9									
Address	0x0B	0x0B09								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Mach	ine performa	ance-monitor	ing counter.						
Field Nan	Name Bit Offset Bit Width Volatile Access Reset Value Description					Description				
hpmcounter9	9 0 64 true WARL 0x0 Counter value					Counter value				

mhpmco	mhpmcounter10									
Address	0x0B	0x0B0A								
Size	64	4								
Reset Value	0x00	0x0000000000000								
Description	Mach	ine performa	ance-monitor	ing counter.						
Field Nan	Field Name Bit Offset Bit Width Volatile Access Reset Value Descri				Description					
hpmcounter1	nter10 0 64 true WARL 0x0 Counter value					Counter value				

mhpmco	mhpmcounter11									
Address	0x0B	0x0B0B								
Size	64	54								
Reset Value	0x00	0×0000000000000								
Description	Mach	nine performa	ance-monitor	ing counter.						
Field Name Bit Offset Bit Width Volatile Access Reset Value			Reset Value	Description						
hpmcounter1	mcounter11 0			false	WARL	0x0	Counter value			

mhpmcounter12							
Address	0x0B0C						
Size	64						
Reset Value	0x000000000000						

Description	Description Machine performance-monitoring counter.									
Field Nam	Field Name Bit Offset Bit Width Volatile Access Reset Value Description									
hpmcounter12	hpmcounter12 0 64 false WARL 0x0 Counter value									

mhpmcounter13									
Address	0x0B	0x0B0D							
Size	64	4							
Reset Value	0x0000000000000								
Description	Mach	ine performa	ance-monitor	ing counter.					
Field Nan	Field Name Bit Offset Bit Width Volatile Access Reset Value			Description					
hpmcounter1	r13 0 64 false WARL 0x0 Counter value				Counter value				

mhpmco	mhpmcounter14									
Address	0x0B	x0B0E								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Machine performance-monitoring counter.									
Field Nan	me Bit Offset Bit Width Volatile Access Reset Value Description					Description				
hpmcounter1	4	0 64 false WARL 0x0 Counter value								

mhpmco	mhpmcounter15									
Address	0x0B	x0B0F								
Size	64	4								
Reset Value	0x00	0×0000000000000								
Description	Mach	Machine performance-monitoring counter.								
Field Nan	me Bit Offset Bit Width Volatile Access Reset Value Description					Description				
hpmcounter1	mcounter15 0 64 false WARL 0x0 Counter value					Counter value				

mhpmco	mhpmcounter16									
Address	0x0B	0x0B10								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Mach	ine performa	ance-monitor	ing counter.						
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description						Description			
hpmcounter1	.6	0 64 false WARL 0x0 Counter value								

mhpmco	mhpmcounter17								
Address	x0B11								
Size	54								
Reset Value	0x0000000000000								
Description	Machine performance-monitoring counter.								

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
hpmcounter17	0	64	false	WARL	0x0	Counter value

mhpmco	mhpmcounter18									
Address	0x0B	0x0B12								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Mach	ine performa	ance-monitor	ing counter.						
Field Nan	me Bit Offset Bit Width Volatile Access Reset Value Description					Description				
hpmcounter1	8	8 0 64 false WARL 0x0 Counter value					Counter value			

mhpmco	mhpmcounter19									
Address	0x0B	x0B13								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Mach	nine performa	ance-monitor	ing counter.						
Field Nan	Field Name Bit Offset Bit Width Volatile Access Reset Value Des				Description					
hpmcounter1	9	0 64 false WARL 0x0 Counter value								

mhpmcounter20										
Address	0x0B	0x0B14								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Mach	nine performa	ance-monitor	ing counter.						
Field Nan	Name Bit Offset Bit Width Volatile Access Reset Value Descri					Description				
hpmcounter2	0	0 64 false WARL 0x0 Counter value								

mhpmco	mhpmcounter21									
Address	0x0B	x0B15								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Mach	ine performa	nce-monitor	ing counter.						
Field Nan	Field Name Bit Offset Bit Width Volatile Access Reset Value Description					Description				
hpmcounter2	21 0 64 false WARL 0x0 Counter value									

mhpmco	mhpmcounter22									
Address	0x0B	x0B16								
Size	64	54								
Reset Value	0x00	0000000000	0000							
Description	Machine performance-monitoring counter.									
Field Nan	Name Bit Offset Bit Width Volatile Access Reset Value Description						Description			

hpmcounter22	0	64	false	IVVARL	0x0	Counter value
	-	_ ·		l		

mhpmco	mhpmcounter23									
Address	0x0B	x0B17								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Mach	ine performa	ance-monitor	ing counter.						
Field Nan	me Bit Offset Bit Width Volatile Access Reset Value Description					Description				
hpmcounter2	3	0 64 false WARL 0x0 Counter value								

mhpmco	mhpmcounter24										
Address	0x0B	0x0B18									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mach	ine performa	nce-monitor	ing counter.							
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description									
hpmcounter2	4	0 64 false WARL 0x0 Counter value									

mhpmcounter25										
Address	0x0B	0x0B19								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	nine performa	ance-monitor	ing counter.						
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter2	5	0 64 false WARL 0x0 Counter value								

mhpmco	mhpmcounter26									
Address	0x0B	0x0B1A								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	ine performa	ance-monitor	ing counter.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter2	6	0 64 false WARL 0x0 Counter value								

mhpmco	mhpmcounter27										
Address	0x0B	0x0B1B									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Machine performance-monitoring counter.										
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description									

hpmcounter27	0	64	false	IVVARL	0x0	Counter value
	-	l -		l	****	

mhpmco	mhpmcounter28									
Address	0x0B	1C								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	nine performa	ance-monitor	ing counter.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter2	:8	0 64 false WARL 0x0 Counter value								

mhpmco	mhpmcounter29									
Address	0x0B	0x0B1D								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	nine performa	ance-monitor	ing counter.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter2	9	0 64 false WARL 0x0 Counter value								

mhpmco	mhpmcounter30										
Address	0x0B	0x0B1E									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Mach	nine performa	ance-monitor	ing counter.							
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description										
hpmcounter3	0	0 64 false WARL 0x0 Counter value									

mhpmco	mhpmcounter31									
Address	0x0B	1F								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Mach	ine performa	ance-monitor	ing counter.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter3	1	0 64 false WARL 0x0 Counter value								

c_async_i	oc_int_status										
Address	0x0BF	2									
Size	64										
Reset Value	0x000	000000000	0000								
Description	Machi	Machine Local Interrupt Status Register									
Field Nam	ne	Bit Offset Bit Width Volatile Access Reset Value Description									

ра	0	56	true	WARL	0x0	PA associated with the local interrupt
rsvd_0	56	7	true	WARL	0x0	Reserved
valid	63	1	true	WARL	0x0	Valid bit

cycle										
Address	0x0C	0x0C00								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Cycle	counter for	RDCYCLE ins	truction.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
cycle		0 64 false Read-Only 0x0 Counter value								

time	time									
Address	0x0C	0x0C01								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Time	r for RDTIME	instruction. I	Read-only sh	adow of mtin	ne MMR.				
Field Nan	ame Bit Offset Bit Width Volatile Access Reset Value Description			Description						
time		0 64 true Read-Only 0x0 Counter value					Counter value			

instret	instret								
Address	0x0C	x0C02							
Size	64	4							
Reset Value	0x00	0000000000	0000						
Description	Instru	uctions-retire	d counter for	r RDINSTRET	instruction.				
Field Nan	me Bit Offset Bit Width Volatile Access Reset Value Description				Description				
instret	0 64 false Read-Only 0x0 Counter value				Counter value				

hpmcoun	hpmcounter3								
Address	0x0C	0x0C03							
Size	64	4							
Reset Value	0x00	0000000000	0000						
Description	Perfo	rmance-mon	itoring count	er.					
Field Nan	me Bit Offset Bit Width Volatile Access Reset Value Description					Description			
hpmcounter3	0 64 false Read-Only 0x0 Counter value					Counter value			

hpmcoun	hpmcounter4							
Address	0x0C04							
Size	64							
Reset Value	0×000000000000							
Description	Performance-monitoring counter.							

Field Name	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description
hpmcounter4	0	64	false	Read-Only	0x0	Counter value

hpmcoun	hpmcounter5								
Address	0x0C	0x0C05							
Size	64	4							
Reset Value	0x00	0000000000	0000						
Description	Perfo	rmance-mon	itoring count	er.					
Field Nan	ame Bit Offset Bit Width Volatile Access Reset Value			Description					
hpmcounter5	5 0 64		false	Read-Only	0x0	Counter value			

hpmcoun	hpmcounter6								
Address	0x0C	0x0C06							
Size	64	•							
Reset Value	0x00	0000000000	0000						
Description	Perfo	rmance-mon	itoring count	er.					
Field Nan	ame Bit Offset Bit Width Volatile Access Reset Value Descriptio				Description				
hpmcounter6	6 0 64 false Read-Only 0x0 Counter value				Counter value				

hpmcounter7									
Address	0x0C	0x0C07							
Size	64	5 4							
Reset Value	0x00	0000000000	0000						
Description	Perfo	rmance-mon	itoring count	er.					
Field Nan	ame Bit Offset Bit Width Volatile Access Reset Value			Description					
hpmcounter7	7 0 64 false Read-Only 0x0 Counter value				Counter value				

hpmcounter8									
Address	0x0C	0x0C08							
Size	64	1							
Reset Value	0x00	0000000000	0000						
Description	Perfo	rmance-mon	itoring count	er.					
Field Nan	Field Name Bit Offset Bit Width		Volatile	Access	Reset Value	Description			
hpmcounter8	r8 0 64		false	Read-Only	0x0	Counter value			

hpmcour	hpmcounter9									
Address	0x0C	x0C09								
Size	64	94								
Reset Value	0x00	0000000000	0000							
Description	n Performance-monitoring counter.									
Field Nan	me Bit Offset Bit Width			Volatile	Access	Reset Value	Description			

hpmcounter9	0	64	false	Read-Only	0x0	Counter value
	_	l -				

hpmcoun	hpmcounter10								
Address	0x0C	x0C0A							
Size	64	4							
Reset Value	0x00	0000000000	0000						
Description	Perfo	rmance-mon	itoring count	er.					
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description					Description			
hpmcounter1	0	0 64 false Read-Only 0x0 Counter value							

hpmcoun	hpmcounter11									
Address	0x0C	0x0C0B								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter1	1	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter12									
Address	0x0C	0x0C0C								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter1	2	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter13									
Address	0x0C	x0C0D								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter1	.3	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter14									
Address	0x0C	x0C0E								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Performance-monitoring counter.									
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								

hpmcounter14	0	64	false	Read-Only	0x0	Counter value
P	_	l -				

hpmcoun	hpmcounter15									
Address	0x0C	0x0C0F								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter1	.5	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter16									
Address	0x0C	0x0C10								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	e Bit Offset Bit Width Volatile Access Reset Value Description									
hpmcounter1	6	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter17									
Address	0x0C)x0C11								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter1	7	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter18									
Address	0x0C	x0C12								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter1	8	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter19									
Address	0x0C	x0C13								
Size	64	4								
Reset Value	0x00	0000000000	0000							
Description	Performance-monitoring counter.									
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								

hpmcounter19	0	64	false	Read-Only	0x0	Counter value
I' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' '	-	l -				

hpmcoun	hpmcounter20									
Address	0x0C	x0C14								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter2	0	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter21									
Address	0x0C	0x0C15								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter2	1	0 64 false Read-Only 0x0 Counter value								

hpmcounter22											
Address	0x0C	0x0C16									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Perfo	rmance-mon	itoring count	er.							
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description										
hpmcounter2	2	0 64 false Read-Only 0x0 Counter value									

hpmcoun	hpmcounter23									
Address	0x0C	17								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter2	:3	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter24										
Address	0x0C	x0C18									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Performance-monitoring counter.										
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description									

hpmcounter24	0	64	false	Read-Only	0x0	Counter value
P	-	l -				

hpmcoun	hpmcounter25									
Address	0x0C	0x0C19								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter2	5	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter26									
Address	0x0C	0x0C1A								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	e Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter2	6	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter27									
Address	0x0C	0x0C1B								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter2	7	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter28									
Address	0x0C	1C								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								
hpmcounter2	8	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter29									
Address	0x0C	0x0C1D								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	Performance-monitoring counter.								
Field Nan	ne	Bit Offset Bit Width Volatile Access Reset Value Description								

hpmcounter29	0	64	false	Read-Only	0x0	Counter value
	-	_ ·				

hpmcoun	hpmcounter30									
Address	0x0C	0x0C1E								
Size	64									
Reset Value	0x00	0000000000	0000							
Description	Perfo	rmance-mon	itoring count	er.						
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description									
hpmcounter3	0	0 64 false Read-Only 0x0 Counter value								

hpmcoun	hpmcounter31										
Address	0x0C	x0C1F									
Size	64										
Reset Value	0x00	0000000000	0000								
Description	Perfo	rmance-mon	itoring count	er.							
Field Nan	Name Bit Offset Bit Width			Volatile	Access	Reset Value	Description				
hpmcounter3	1	. 0 64 false Read-Only 0x0					Counter value				

vI											
Address	0x0C	x0C20									
Size	64										
Reset Value	0x00	0x0000000000000									
Description	Vecto	or length									
Field Nan	ame Bit Offset Bit Wi		Bit Width	Volatile	Access	ı	Reset Value	Description			
vl	0 64 false Read-Onl				Read-Only	0x0		Vector length			

vtype							
Address	0x0C	21					
Size	64						
Reset Value	0x80	0000000000	0000				
Description	Vect	or data type	register				
Field Nan	Name Bit Offset		Bit Width	Volatile	Access	Reset Value	Description
vlmul		0	3	true	WARL	0×0	Vector register group multiplier (LMUL) setting
vsew		3	3	true	WARL	0×0	Selected element width (SEW) setting
vta		6	1	true	WARL	0x0	Vector tail agnostic
vma		7	1	true	WARL	0x0	Vector mask agnostic
reserved		8	55	true	WARL	0x0	Reserved if non-zero
vill		63	1	true	WARL	0x1	Illegal value if set

vlenb												
Address	0x0C	x0C22										
Size	64	4										
Reset Value	0x00	0x000000000000000000000000000000000000										
Description	VLEN	l/8 (vector re	gister length	in bytes)								
Field Nan	me Bit Offset Bit		Bit Width	Volatile	Access	Reset Value	Description					
vlenb		0	64 folio	false	Darad Order	0x20	VLEN/8 (vector register length in					
VIEID		U	64 false		Read-Only	0.00	bytes)					

scountov	scountovf										
Address	0x0D	Dx0DA0									
Size	64										
Reset Value	0x00	0×0000000000000									
Description	HPM	Counter Ove	rflow bits								
Field Nan	me Bit Offset Bit Width		Volatile	Access	Reset Value	Description					
scountovf	0 32 true		true	Read-Only	0x0	HPM Counter Overflow bits					
rsvd6432		32	32	-	WPRI	-	Reserved				

stopi	stopi											
Address	0x0E	x0DB0										
Size	64											
Reset Value	0x00	0000000000	0000									
Description	Supe	Supervisor top interrupt										
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description					
iprio		0	8	true	Read-Only	0x0	Interrupt Priority					
rsvd_15_8	8 8 true		true	Read-Only	0x0	Reserved						
iid	16 12 t		true	Read-Only	0x0	Interrupt Identity						
rsvd_63_28		28	36	true	Read-Only	0x0	Reserved					

hgeip												
Address	0x0E	x0E12										
Size	64	4										
Reset Value	0x00	×0000000000000										
Description	Нуре	Hypervisor guest external interrupt pending.										
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description					
hard0		0	1	true	Read-Only	0x0	Read-only zero					
guestexterna	guestexternalinte rrupts		63 true	true	Read-Only	0x0	Hypervisor guest external interrupts					
rrupts				liuc		0.00	pending bits					

vstopi	
Address	0x0EB0

Size	64	54									
Reset Value	0x00	0x000000000000									
Description	Virtu	Virtual supervisor top interrupt									
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
iprio		0	8	true	Read-Only	0x0	Interrupt Priority				
rsvd_15_8	8 8		8	true	Read-Only	0x0	Reserved				
iid	id 16		12	true	Read-Only	0x0	Interrupt Identity				
rsvd_63_28		28 36 true Read-Only 0x0 Reserved									

mvendor	id											
Address	0x0F)x0F11										
Size	32											
Reset Value	0x00	000000										
Description	Vend	/endor ID.										
Field Nan	me Bit Offset Bit Width Volatile Access Reset Value Des						Description					
jedecparity		0 7	7	false	Read-Only	FIXME	Parity_ID: 0xA1 = 1010 0001 (MSB					
Jedecparity		0	'	laise	Reau-Only	TIAME	is an odd parity bit)					
							JEDEC Bank = 16. This represents					
jedecbankm1		7	4	false	Read-Only	FIXME	Jedec Bank -1 . ([15][0x21 - 1] =					
							Tenstorrent Inc,)					

marchid											
Address	0x0F	12									
Size	32										
Reset Value	0x00	000000									
Description	Archi	Architecture ID.									
Field Nan	ne	Bit Offset	Bit Width	Volatile	Access	Reset Value	Description				
sharedcachev on	versi	0	8	false	Read-Only	FIXME	Shared Cache Version				
microarchver	archversion 8		8	false	Read-Only	FIXME	Micro-Architecture Version				
archversion		16	8	false	Read-Only	FIXME	Architecture Version				
ipname		24	8	false	Read-Only	FIXME	IP Name				

mimpid											
Address	0x0F	0x0F13									
Size	64	54									
Reset Value	0x00	0000000000	0000								
Description	Imple	ementation II	D.								
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value					Description					
rsvd_31_0		0 20 false			Read-Only	0x0	Reserved				

releasecandidate	20	6	false	Read-Only	FIXME	Release Candidate
dropversion	26	2	false	Read-Only	FIXME	Drop Version
manid	28	4	false	Read-Only	FIXME	Man ID
stepmetalid	32	4	false	Read-Only	FIXME	Step Metal ID
stepbaseid	36	4	false	Read-Only	FIXME	Step Base ID
sharedcacheconfi g	40	8	false	Read-Only	FIXME	Shared Cache Config
coreconfig	48	8	false	Read-Only	FIXME	Core Config
clusterconfig	56	8	false	Read-Only	FIXME	Cluster Config

mhartid											
Address	0x0F	0x0F14									
Size	64	54									
Reset Value	0x00	0x000000000000									
Description	Hardware thread ID. (Starts from 0 and increment for each core)										
Field Nan	ne Bit Offset Bit Width Volatile Access Reset Value Description										
hartidincluste	ter 0 3 false Read-Only 0x0 Hart ID for the core in					Hart ID for the core in a cluster					
clusterid	3 4 false Read-Only 0x0		Cluster ID (defined by external pins)								
rsvd_63_7		7 57 false Read-Only 0x0 Reserved for future use									

mconfigptr										
Address	0x0F	0x0F15								
Size	64	64								
Reset Value	0x0000000000000									
Description	Description Pointer to configuration data structure.									
Field Nan	ame Bit Offset Bit Width Volatile Access Reset Value Description						Description			
mconfigptr 0		64	false	Read-Only	0x0	configuration pointer, may be hardwired				

mtopi											
Address	0x0F	0x0FB0									
Size	64	64									
Reset Value	0x00	0x0000000000000									
Description	Mach	Machine top interrupt									
Field Nan	ield Name Bit Offset Bit Width Volatile Access Reset Value Descripti						Description				
iprio		0	8	true	Read-Only	0x0	Interrupt Priority				
rsvd_15_8	I_15_8 8 8 true			Read-Only	0x0	Reserved					
iid 16		16	12	true	Read-Only	0x0	Interrupt Identity				
rsvd_63_28 2		28	36	true	Read-Only	0x0	Reserved				