Alexandria

Links:

Target release (ER)	Jun 1, 2026
Epic	IPFEAT-174: Alexandria BACKLOG
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Introduction:

This document details the product requirements for "Alexandria," a high-performance, superscalar, out-of-order (OoO) 64-bit RISC-V CPU core designed for a wide range of safety-critical automotive applications. Alexandria is designed to be configurable to meet either ASIL-B or ASIL-D requirements as defined by ISO 26262, offering flexibility for various automotive systems. It will be compliant with the RISC-V Application Profile 2023 (RVA23).

🎯 Goals

Serve as a base IP for different automotive projects to be served in Base Die and Chiplet applications on centralized compute, ADAS and IVI.

- **RVA23 Compliance:** Full compliance with the RISC-V Application Profile 2023 (RVA23).
- **ASIL B/D Configurable:** Meet ISO 26262 ASIL-B and ASIL-D requirements through hardware and software configuration.
- **High Performance:** Deliver high single-threaded performance.
- **Energy Efficiency:** Optimized power consumption for automotive environments.
- **Functional Safety:** Robust functional safety mechanisms to ensure safe operation across different ASIL levels.
- **Reliability:** Extremely high reliability and fault tolerance.
- **Security:** Advanced security features to protect against automotive threats.
- **Scalability:** Support a range of performance and safety requirements.

Target Market

- Advanced Driver-Assistance Systems (ADAS)
- In-Vehicle Infotainment (IVI)
- Autonomous Driving (AD)
- Automotive safety controllers
- Body electronics
- Powertrain control
- Chassis control
- Other safety-critical automotive applications

Target Customers

Target customers	Timeline	Notes
Bosch (Lead Partner)	CY2026 (Silicon available) Beginning of 2026 tape out SOW by end of 2024	Chiplet CPU PPA requirement: • ~250 kDMIPs, 50 SpecInt2K17rate_base; (10 copy); 10 cores; 22W • Frequency: 2GHz ~ 2.4GHz • 275 KDMIPS, 55SpecInt2K17rate_base Base die CPU PPA requirement: • 150 KDMIPS, 30 SpecInt2K17rate_base
Li Auto	Tape out end of 2025 Need initial IP version within 2024	

🌟 Milestones

Customer Facing Milestones

- LAC: Q2 2026
- EAC:Q3 2026

Approved Features

Key	Summary	Description
IPFEAT-31	[Non-Functional] Overall PPA requirements from ...	150kDMIPsTimeline CY2026 Silicon available

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Features Under Review

Key	Summary	Description
IPFEAT-52	PRD [FuSa] Alexandria clusters shall support RAS error reporting registers ...	Automotive OEMs/T1s do not like sile
IPFEAT-56	PRD [FuSa] Alexandria shall support real-time hardware safety monitors to ...	Any hardware mechanism we implem
IPFEAT-50	PRD [FuSa] Alexandria shall support fault injection mechanisms to enable t...	Alexandria shall Support Fault injecti
IPFEAT-28	PRD [Debug and Trace] Alexandria shall support code profiling	Alexandria shall support code profilin
IPFEAT-34	PRD [Debug and Trace] Alexandria shall support temperature monitoring	Chiplet requirement
IPFEAT-55	PRD [FuSa] Alexandria shall have a separate physical bus for configuring a...	Compute cluster should be able to int
IPFEAT-53	PRD [FuSa] Alexandria shall support modification of ECC type	Option to change the type of ECC on
IPFEAT-37	PRD [S/W] The RISC-V Compiler and toolchain for Alexandria shall be quali...	Qualify software toolsEnsure we utiliz
IPFEAT-46	PRD [Functional] Alexandria shall support Cache-line lock-out on L1 private...	Alexandria shall support Cachelock c
IPFEAT-51	PRD [FuSa] Alexandria shall have Error Scrubbing, error containing and me...	Alexandria shall have Error Scrubbing
IPFEAT-45	PRD [FuSa] Alexandria shall implement bus Interface protection enabled to ...	Configurable ECC/Parity on data and
IPFEAT-49	PRD [Perf] Alexandria CPU core shall run at an Fmax minimun of 2.25 GHz ...	Per MRD:Ta = 105°C & Tj = 125°C - Tc
IPFEAT-43	PRD [Other] Alexandria shall allow for 3rd party BIST implementations.	Alexandria shall not prevent an integr

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Deliverables

- RTL source code (SystemVerilog).
- Verification testbench and test cases.
- Synthesis scripts and timing constraints.
- Documentation (datasheet, user manual, safety manual).
- Software Development Kit (SDK) and toolchain.
- ISO 26262 compliance reports.
- Safety analysis reports (FMEDA, DFA).

Success Metrics

- Successful RVA23 compliance certification.
- Achieved ISO 26262 ASIL-B and ASIL-D certification.
- Achieved target performance and power consumption.
- Successful silicon implementation and testing.
- Adoption in the automotive market.
- Positive safety assessments and audits.

Future Considerations

- Support for future RISC-V extensions and profiles.
- Integration of hardware security modules (HSMs).
- Advanced fault tolerance techniques.
- Support for emerging automotive standards.

Open Questions/Issues

Key	Summary
IPFEAT-3...	ALX - P&C
IPFEAT-3...	CA - ALX-X-4c4m
IPFEAT-3...	PCA ALX-X-4c4m
IPFEAT-2...	GA ALX-X-4c4m
IPFEAT-2...	EA ALX-X-4c4m
IPFEAT-2...	LA ALX-X-4c4m
IPFEAT-2...	Beta ALX-X-4c4m
IPFEAT-30	PRD - Deliverables
IPFEAT-11	[MRD] Bosch Timeline

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