REFERENCE CARD

User Identifier Alternative Optional VHDL-1993 Grouping Repeated

1. LIBRARY UNITS

port ({ID : in | out | inout TYPEID [:= expr];});] [generic ({ID:TYPEID [:= expr];});] end [entity] ENTITYID [parallel statement] {declaration}] [use_clause] entity ID is

architecture ID of ENTITYID is {use clause}]

end [architecture] ARCHID; {parallel statement} [{declaration}]

end [package] PACKID; {declaration}] package ID is {use clause}

package body ID is [{declaration}] [{use_clause}]

configuration ID of ENTITYID is end [package body] PACKID; {use_clause}

{block_config | comp_config}] for ARCHID end for:

end [configuration] CONFID; use clause::=

[{nse LIBID.PKGID.all;}] olock_config::= librarv D:

for LABELID end for;

[{block_config | comp_config}]

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port map ({PORTID => SIGID | expr.,})]; [[generic map ({GENID => expr ,})]
port map ({PORTID => SIGID | expr,})];) (use entity [LIBID.]ENTITYID [(ARCHID)] [[generic map ({GENID => expr ,})] (use configuration [LIBID.]CONFID [{block_config | comp_config}] for all | LABELID : COMPID [for ARCHID end for;) comp config::= end for:

2. DECLARATIONS

2.1. TYPE DECLARATIONS

type ID is ({ID,});

type ID is range number downto | to number;

type ID is array ({range | TYPEID ,})
of TYPEID | SUBTYPID;

type ID is record (ID:TYPEID;

end record;

type ID is access TYPEID;

type ID is file of TYPEID;

subtype ID is SCALARTYPID range range;

subtype ID is RESOLVFCTID TYPEID; subtype ID is ARRAYTYPID({range,})

range ::=

integer | ENUMID) | (OBJID'[reverse_]range) (integer | ENUMID to | downto (TYPEID range <>)

2.2. OTHER DECLARATIONS

[shared] variable ID : TYPEID [:= expr]; constant ID : TYPEID := expr; signal ID : TYPEID [:= expr];

file ID: TYPEID (is in | out string;) | open read mode | write mode

/ append_mode is string;) alias ID: TYPEID is OBJID;

attribute ID: TYPEID;

attribute ATTRID of OBJID | others | all : class is expr;

procedure | function | package | type subtype | constant | signal | variable entity | architecture | configuration component | label

component ID [is]

port ({ID : in | out | inout TYPEID [:= expr];}); generic ({ID : TYPEID [:= expr];});] end component [COMPID];

impure function ID

in | out | inout TYPEID [:= expr];})] [({[constant | variable | signal] ID return TYPEID [is

{sequential statement} end [function] ID];

in | out | inout TYPEID [:= expr];})] procedure ID[({[constant | variable | signal] ID

is begin

[{sequential_statement}]

for LABELID | others | all : COMPID use end [procedure] ID];

port map ({PORTID => SIGID | expr,})]; (entity [LIBID.]ENTITYID [(ARCHID)]) [[generic map ({GENID => expr,})] configuration [LIBID.]CONFID)

EXPRESSIONS က

shexpr [relop shexpr] sexpr [shop sexpr] (relation **and** relation) (relation **xor** relation) relation or relation) expression ::= relation ::= shexpr ::=

[+|-] term {addop term} factor {mulop factor} sexpr ::= term ::=

(prim [** prim]) | (abs prim) | (not prim) factor ::=

prim ::=

literal | OBJID | OBJID'ATTRID | OBJID({expr,}) OBJID(range) | ({[choice [{| choice}] =>] expr,}) FCTID({[PARID =>] expr,}) | TYPEID'(expr)

LYPEID(expr) | new TYPEID['(expr)] | (expr sexpr | range | RECFID | others choice ::=

3.1. OPERATORS, INCREASING PRECEDENCE

sll | srl | sla | sra | rol | ror * | / | mod | rem ** | abs | not and or xor miscop addop mulop doys relop

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See reverse side for additional information.