PES UNIVERSITY

Department of Computer Science & Engineering

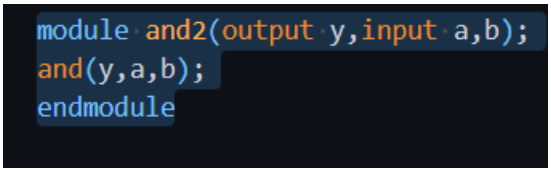
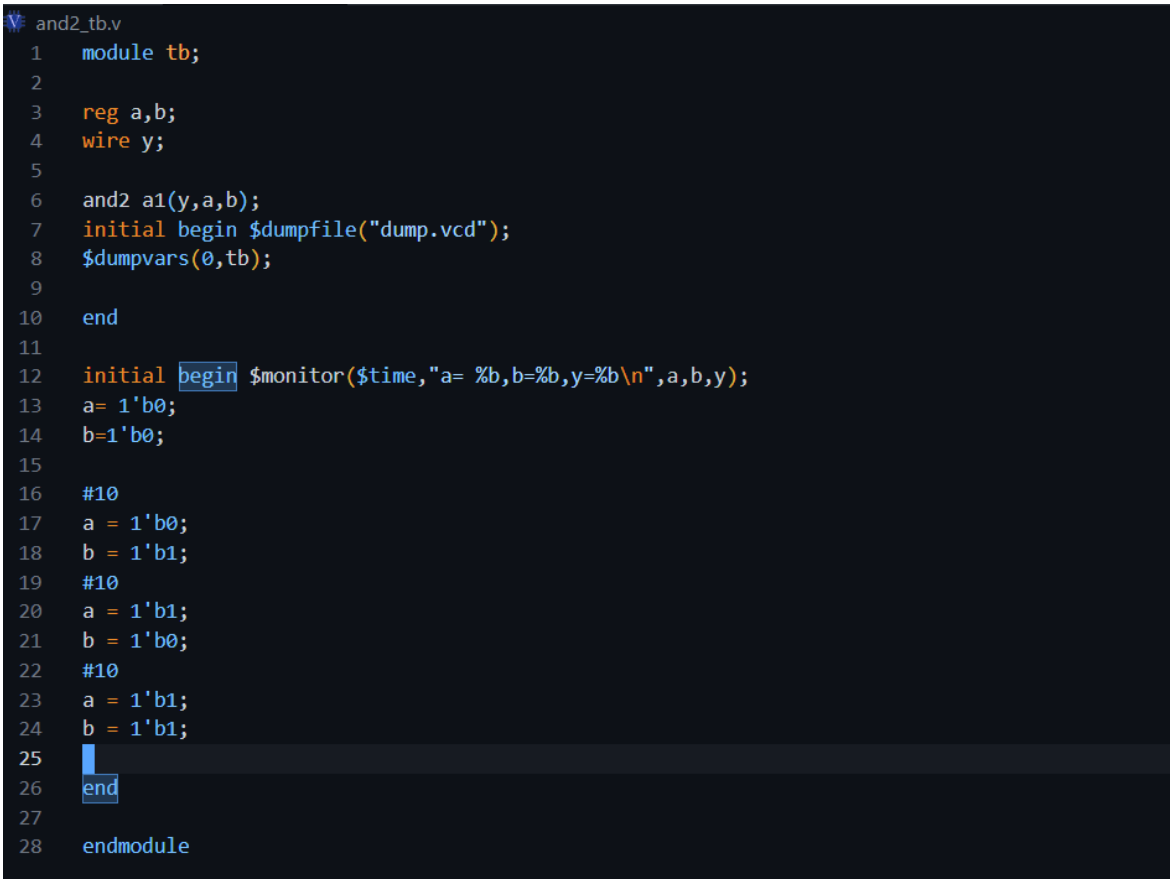
Digital Design and Computer Organisation Laboratory

UE24CS251A

WEEK 1 submission

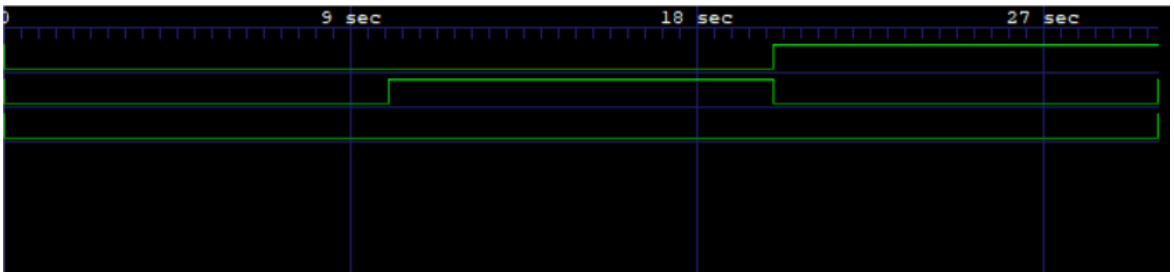
Name of the Student	**Tilak Giridhar Kumta**
SRN	**PES1UG24CS696**
Section	**L**
Department	**CSE**
Campus	**Ring Road Campus**

Program: Basic AND gate

1	Program screen shot: Module file(Example f1.v) 
2	Program screen shot :Testbench file(f1_tb.v) 
3	Verilog VVP Output Screen Shot

```
:\iverilog\bin>vvp test
CD info: dumpfile dump.vcd opened for output.
                    0a= 0,b=0,y=0

                   10a= 0,b=1,y=0

                   20a= 1,b=0,y=0

                   30a= 1,b=1,y=1


:\iverilog\bin>gtkwave dump.vcd

TKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[30] end time.
M Destroy

:\iverilog\bin>
```

4 GTKWAVE Screenshot



Program: Basic NOT gate

1	Program screen shot: Module file(Example f1.v)

```
module not2(output y, input a);
not(y,a);
endmodule
```

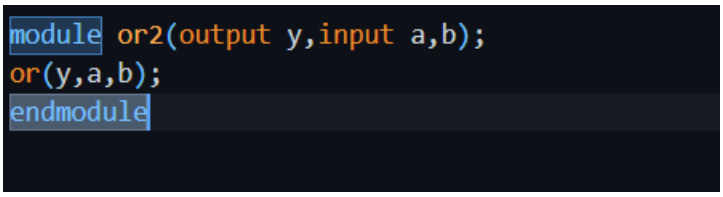
2 Program screen shot :Testbench file(f1_tb.v)

```
module tb;
reg a;
wire y;

not2 a1(y,a);

initial begin
    $dumpfile("dump.vcd");
    $dumpvars(0,tb);
end

initial begin
    $monitor($time, " a=%b y=%b", a, y);

    a = 1'b0;
    #10 a = 1'b1;
    #10 a = 1'b0;
    #10 a = 1'b1;
end

endmodule
```

3 Verilog VVP Output Screen Shot

	C:\iverilog\bin>vvp test VCD info: dumpfile dump.vcd opened for output. 0 a=0 y=1 10 a=1 y=0 20 a=0 y=1 30 a=1 y=0
4	GTKWAVE Screenshot 

Program: Basic OR gate

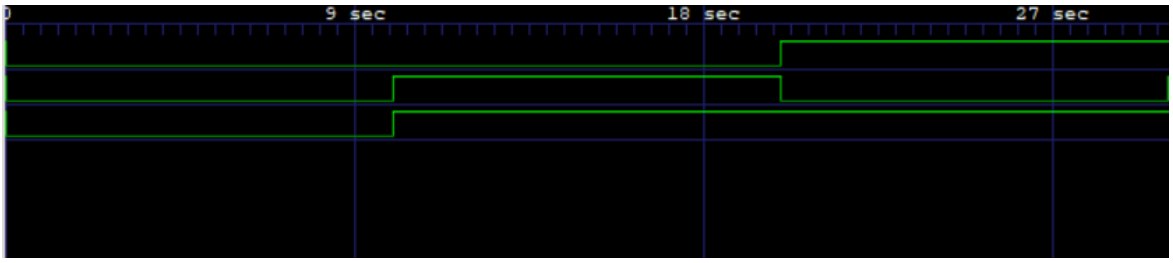
1	Program screen shot: Module file(Example f1.v) 
2	Program screen shot :Testbench file(f1_tb.v)

or2_tb.v

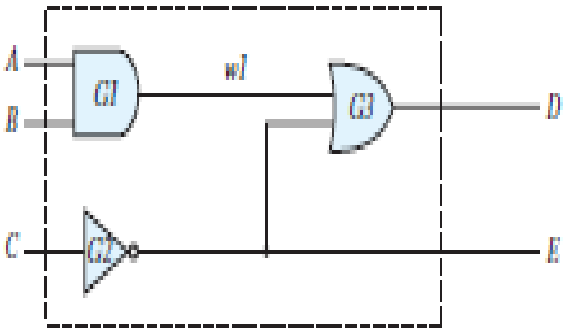
```
module tb;

reg a,b;
wire y;

or2 a1(y,a,b);
initial begin $dumpfile("dump.vcd");
$dumpvars(0,tb);

end

initial begin $monitor($time,"a= %b,b=%b,y=%b\n",a,b,y);
a= 1'b0;
b=1'b0;

#10
a = 1'b0;
b = 1'b1;
#10
a = 1'b1;
b = 1'b0;
#10
a = 1'b1;
b = 1'b1;

end

endmodule
```

3 Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp test
VCD info: dumpfile dump.vcd opened for output.
                   0a= 0,b=0,y=0

                  10a= 0,b=1,y=1

                  20a= 1,b=0,y=1

                  30a= 1,b=1,y=1
```

4	GTKWAVE Screenshot 

Program1:



1	Program screen shot: Module file(Example f1.v)
	`module circ1(output D, output E, input A, input B, input C);`
	`wire w1;`
	`and(w1,A,B);`
	`not(E,C);`
	`or(D, w1, E);`
	`endmodule`

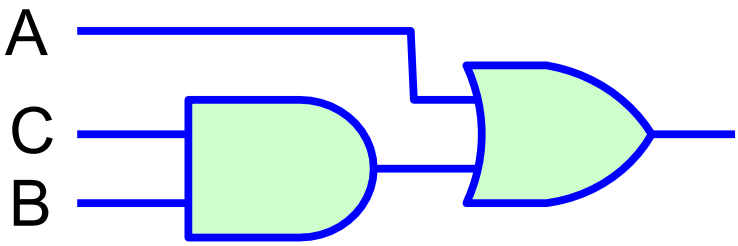
2	Program screen shot :Testbench file(f1_tb.v)
	`module tb;`
	`reg A,B,C;`
	`wire D,E;`
	`circ1 a1(D,E,A,B,C);`
	`initial begin`
	`$dumpfile("dump.vcd");`
	`$dumpvars(0, tb);`
	`end`
	
	`initial begin`
	`$monitor($time, " A=%b B=%b C=%b | D=%b E=%b", A, B, C, D, E);`
	
	`A=0; B=0; C=0;`
	`#10 A=0; B=0; C=1;`
	`#10 A=0; B=1; C=0;`
	`#10 A=0; B=1; C=1;`
	`#10 A=1; B=0; C=0;`
	`#10 A=1; B=0; C=1;`
	`#10 A=1; B=1; C=0;`
	`#10 A=1; B=1; C=1;`
	`end`
	
	`endmodule`

3	Verilog VVP Output Screen Shot
	`VCD info: dumpfile dump.vcd opened for output.`
	`0 A=0 B=0 C=0 | D=1 E=1`
	`10 A=0 B=0 C=1 | D=0 E=0`
	`20 A=0 B=1 C=0 | D=1 E=1`
	`30 A=0 B=1 C=1 | D=0 E=0`
	`40 A=1 B=0 C=0 | D=1 E=1`
	`50 A=1 B=0 C=1 | D=0 E=0`
	`60 A=1 B=1 C=0 | D=1 E=1`
	`70 A=1 B=1 C=1 | D=1 E=0`

4	GTKWAVE Screenshot

Program2:



1	Program screen shot: Module file(Example f1.v)
	`module circ2(output D, input A, input B, input C);`
	`  wire w1;`
	`  and(w1,C,B);`
	`  or(D,w1,A);`
	`endmodule`

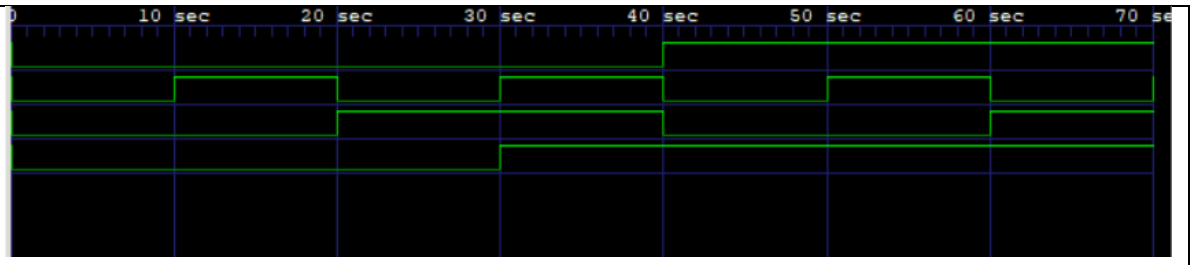
2	Program screen shot :Testbench file(f1_tb.v)

```
module tb;
reg A,B,C;
wire D;
circ2 a1(D,A,B,C);
initial begin
    $dumpfile("dump.vcd");
    $dumpvars(0, tb);
end

initial begin
    $monitor($time, " A=%b B=%b C=%b | D=%b", A, B, C, D);

    A=0; C=0; B=0;
    #10 A=0; C=0; B=1;
    #10 A=0; C=1; B=0;
    #10 A=0; C=1; B=1;
    #10 A=1; C=0; B=0;
    #10 A=1; C=0; B=1;
    #10 A=1; C=1; B=0;
    #10 A=1; C=1; B=1;
end

endmodule
```

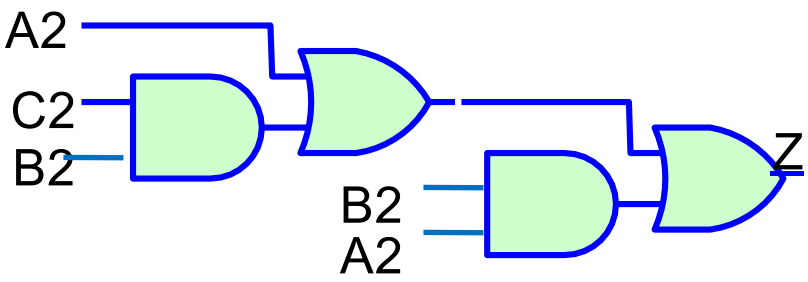
3 Verilog VVP Output Screen Shot

```
VCD info: dumpfile dump.vcd opened for output.
                   0 A=0 B=0 C=0 | D=0
                  10 A=0 B=1 C=0 | D=0
                  20 A=0 B=0 C=1 | D=0
                  30 A=0 B=1 C=1 | D=1
                  40 A=1 B=0 C=0 | D=1
                  50 A=1 B=1 C=0 | D=1
                  60 A=1 B=0 C=1 | D=1
                  70 A=1 B=1 C=1 | D=1
```

4 GTKWAVE Screenshot

Program 3:

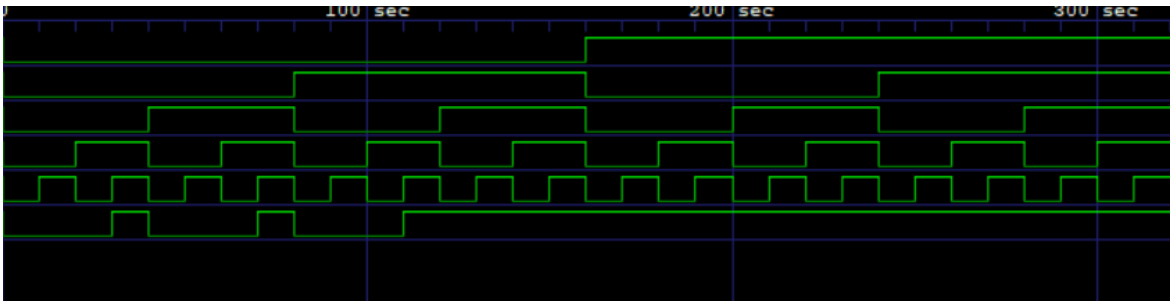


1	Program screen shot: Module file(Example f1.v)

```
module circ3(output F, input A, input B, input C,input D,input E);
        wire w1;
        wire w2;
        wire w3;
        and(w1,B,C);
        or(w2,w1,A);
        and(w3,D,E);
        or(F,w2,w3);
endmodule
```

2 Program screen shot :Testbench file(f1_tb.v)

```
module tb;
reg A,B,C,D,E;
wire F;
circ3 a1(F,A,B,C,D,E);
initial begin
    $dumpfile("dump.vcd");
    $dumpvars(0, tb);
end

initial begin

    $monitor($time, " A=%b B=%b C=%b D=%b E=%b | F=%b", A, B, C, D, E, F);

A=0;B=0;C=0;D=0;E=0;#10;
A=0;B=0;C=0;D=0;E=1;#10;
A=0;B=0;C=0;D=1;E=0;#10;
A=0;B=0;C=0;D=1;E=1;#10;
A=0;B=0;C=1;D=0;E=0;#10;
A=0;B=0;C=1;D=0;E=1;#10;
A=0;B=0;C=1;D=1;E=0;#10;
A=0;B=0;C=1;D=1;E=1;#10;
A=0;B=1;C=0;D=0;E=0;#10;
A=0;B=1;C=0;D=0;E=1;#10;
A=0;B=1;C=0;D=1;E=0;#10;
A=0;B=1;C=0;D=1;E=1;#10;
A=0;B=1;C=1;D=0;E=0;#10;
A=0;B=1;C=1;D=0;E=1;#10;
A=0;B=1;C=1;D=1;E=0;#10;
A=0;B=1;C=1;D=1;E=1;#10;
A=1;B=0;C=0;D=0;E=0;#10;
A=1;B=0;C=0;D=0;E=1;#10;
A=1;B=0;C=0;D=1;E=0;#10;
A=1;B=0;C=0;D=1;E=1;#10;
A=1;B=0;C=1;D=0;E=0;#10;
A=1;B=0;C=1;D=0;E=1;#10;
A=1;B=0;C=1;D=1;E=0;#10;
```

3	Verilog VVP Output Screen Shot VCD info: dumpfile dump.vcd opened for output. 0 A=0 B=0 C=0 D=0 E=0 | F=0 10 A=0 B=0 C=0 D=0 E=1 | F=0 20 A=0 B=0 C=0 D=1 E=0 | F=0 30 A=0 B=0 C=0 D=1 E=1 | F=1 40 A=0 B=0 C=1 D=0 E=0 | F=0 50 A=0 B=0 C=1 D=0 E=1 | F=0 60 A=0 B=0 C=1 D=1 E=0 | F=0 70 A=0 B=0 C=1 D=1 E=1 | F=1 80 A=0 B=1 C=0 D=0 E=0 | F=0 90 A=0 B=1 C=0 D=0 E=1 | F=0 100 A=0 B=1 C=0 D=1 E=0 | F=0 110 A=0 B=1 C=0 D=1 E=1 | F=1 120 A=0 B=1 C=1 D=0 E=0 | F=1 130 A=0 B=1 C=1 D=0 E=1 | F=1 140 A=0 B=1 C=1 D=1 E=0 | F=1 150 A=0 B=1 C=1 D=1 E=1 | F=1 160 A=1 B=0 C=0 D=0 E=0 | F=1 170 A=1 B=0 C=0 D=0 E=1 | F=1 180 A=1 B=0 C=0 D=1 E=0 | F=1 190 A=1 B=0 C=0 D=1 E=1 | F=1 200 A=1 B=0 C=1 D=0 E=0 | F=1 210 A=1 B=0 C=1 D=0 E=1 | F=1 220 A=1 B=0 C=1 D=1 E=0 | F=1 230 A=1 B=0 C=1 D=1 E=1 | F=1 240 A=1 B=1 C=0 D=0 E=0 | F=1 250 A=1 B=1 C=0 D=0 E=1 | F=1 260 A=1 B=1 C=0 D=1 E=0 | F=1 270 A=1 B=1 C=0 D=1 E=1 | F=1 280 A=1 B=1 C=1 D=0 E=0 | F=1 290 A=1 B=1 C=1 D=0 E=1 | F=1 300 A=1 B=1 C=1 D=1 E=0 | F=1 310 A=1 B=1 C=1 D=1 E=1 | F=1
4	GTKWAVE Screenshot 

Additional Progarm:

	Design a simple digital logic circuit for an **automatic fan controller** that turns ON a fan based on two conditions and also write the Verilog code. • **T (Temperature High)** = 1, if temperature exceeds threshold • **P (Person Present)** = 1, if a person is in the room The **fan (F)** should turn **ON** (F=1) **only when the temperature is high AND a person is present**. Otherwise, the fan remains OFF. Additionally, there is an **override switch (O)** that can force the fan ON irrespective of the other conditions.

1	Program screen shot: Module file(Example f1.v)
	`module add1(output O, input P, input F,input S);`
	`wire g;`
	`and(g,P,F);`
	`or(O,g,S);`
	`endmodule`

2	Program screen shot :Testbench file(f1_tb.v)

```
module tb;

reg P,F,S;
wire O;

add1 a1(O,P,F,S);
initial begin $dumpfile("dump.vcd");
$dumpvars(0,tb);

end

initial begin $monitor($time,"Person = %b,Fan = %b, Switch = %b | O=%b\n",P,F,S,O);
 P=0; F=0; S=0;#10;
 P=0; F=0; S=1;#10;
 P=0; F=1; S=0;#10;
 P=0; F=1; S=1;#10;
 P=1; F=0; S=0;#10;
 P=1; F=0; S=1;#10;
 P=1; F=1; S=0;#10;
 P=1; F=1; S=1;#10;

end

endmodule
```

3 Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp test
VCD info: dumpfile dump.vcd opened for output.
                   0Person = 0,Fan = 0, Switch = 0 | O=0

                  10Person = 0,Fan = 0, Switch = 1 | O=1

                  20Person = 0,Fan = 1, Switch = 0 | O=0

                  30Person = 0,Fan = 1, Switch = 1 | O=1

                  40Person = 1,Fan = 0, Switch = 0 | O=0

                  50Person = 1,Fan = 0, Switch = 1 | O=1

                  60Person = 1,Fan = 1, Switch = 0 | O=1

                  70Person = 1,Fan = 1, Switch = 1 | O=1
```

4	GTKWAVE Screenshot