**Digital Design and Computer Organisation Laboratory**

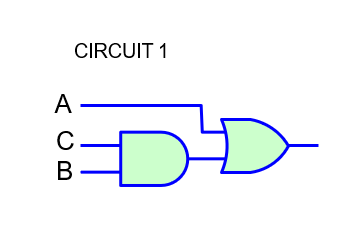
**3rd Semester, Academic Year 2025**

Date:11-08-2025

|  |  |  |
| --- | --- | --- |
| Name: Aakash Desai | SRN:PES1UG24CS006 | Section  3A |

Week Number: 2 Program Number: 1

TITLE:Consider the below circuit diagrams and implement the same using iverilog.

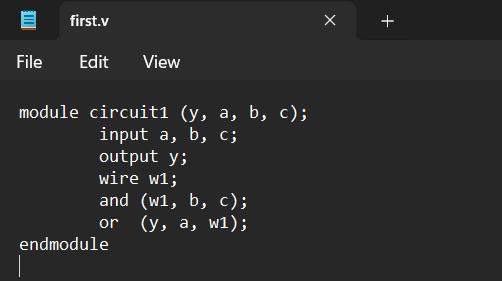


Deliverables

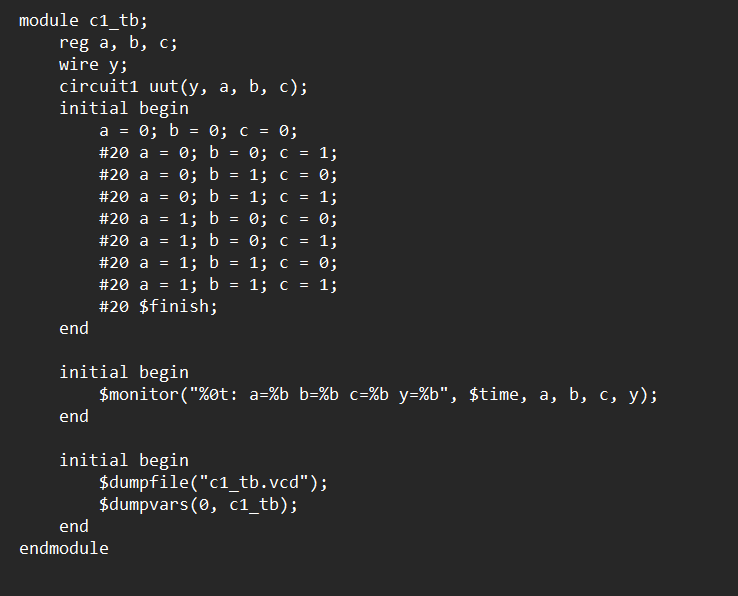
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

I.Verilog Code Snippet

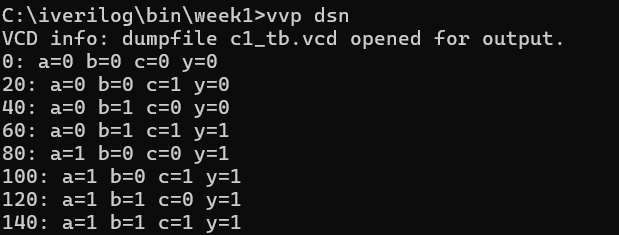
* Main code



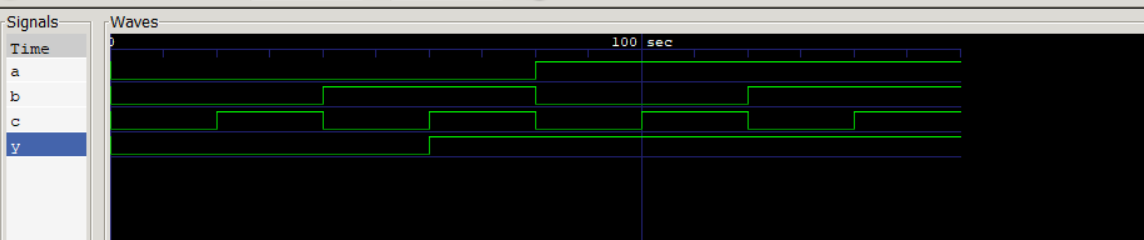
* Test Bench



II Verilog VVP output ScreenShot

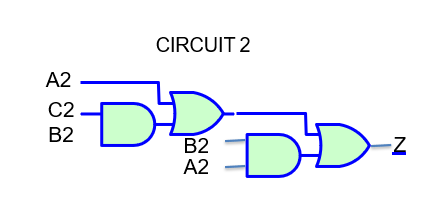


III GTKWave ScrrenShot



IV Truth Table

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | Y |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |



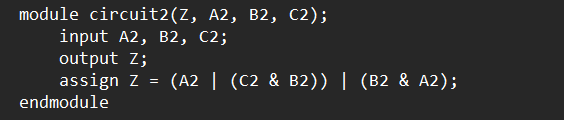
TITLE:Consider the above circuit diagrams and implement the same using iverilog.

Deliverables

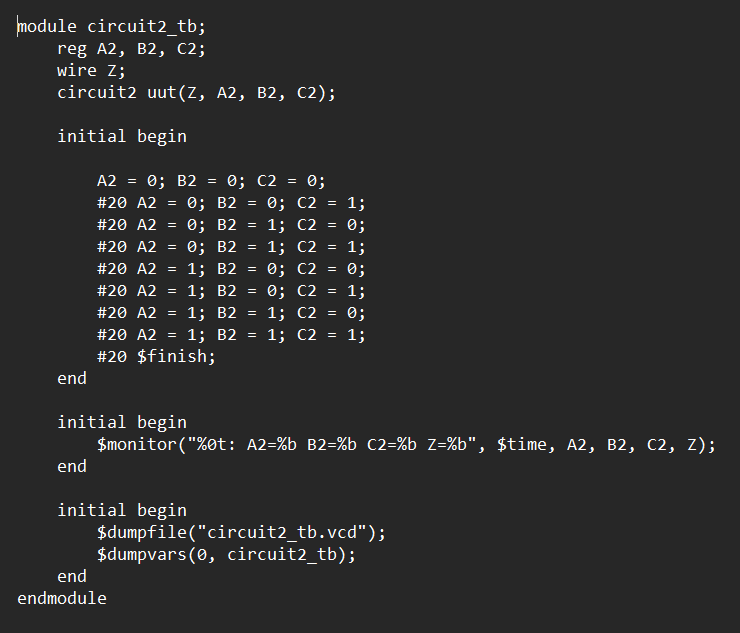
1. Verilog Code Screenshot
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3. GTKWAVE Screenshot
4. Output Table to be completed and included

I.Verilog Code Snippet

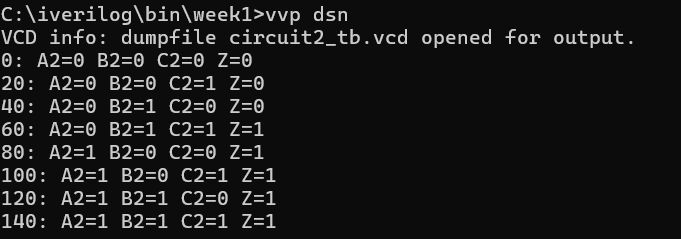
* Main Code

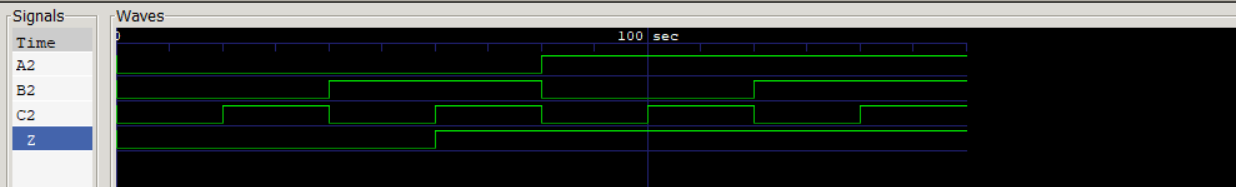


* TestBench



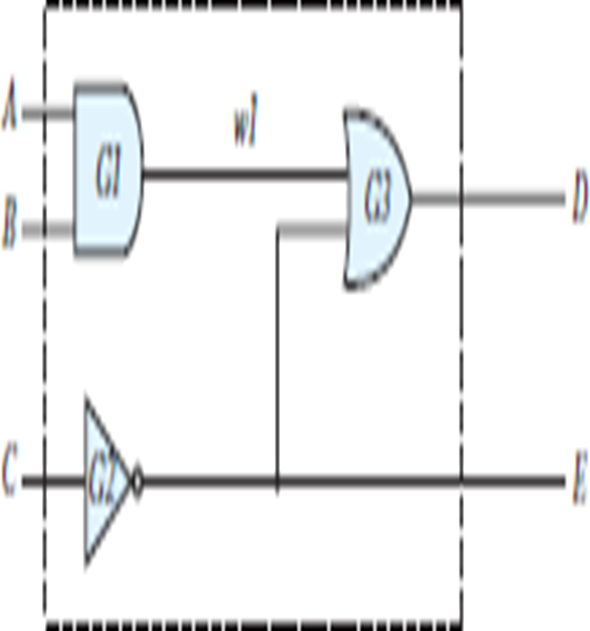
II Verilog VVP ScreenShot



III GTK wave Screenshot

IV Truth Table

|  |  |  |  |
| --- | --- | --- | --- |
| A2 | B2 | C2 | Z |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |



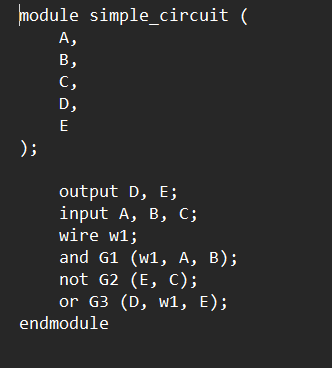
TITLE:Consider the above circuit diagrams and implement the same using iverilog.

Deliverables

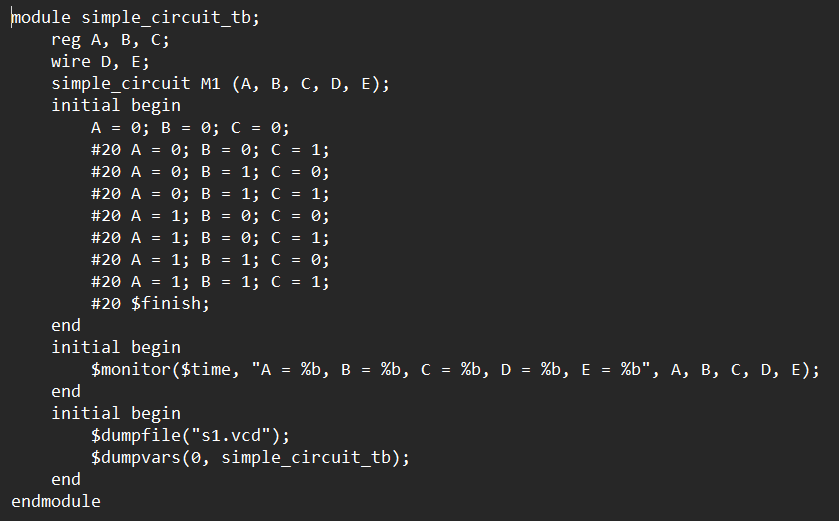
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

I Verilog Code Snippet

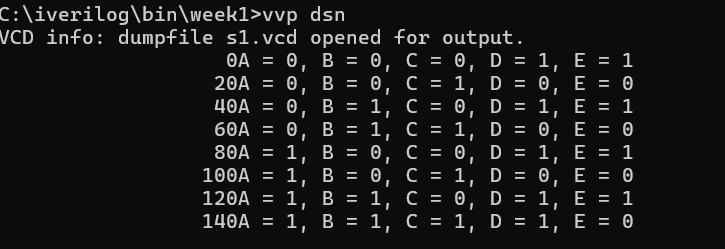
* Main code

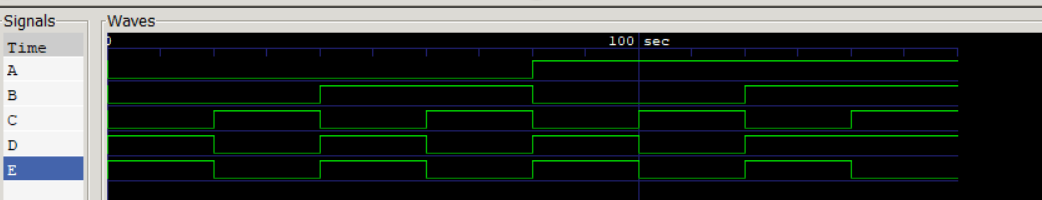


* Test Bench



II Verilog VVP output Screenshot

  
  
  
  
  
  
  
  
  
III GTKWAVE Screenshot

IV Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | D | E |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 |