**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:18-08-2025

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| --- | --- | --- |
| Name: Aakash Desai | SRN:PES1UG24CS006 | Section  3A |

Week Number: 2 Program Number: 1

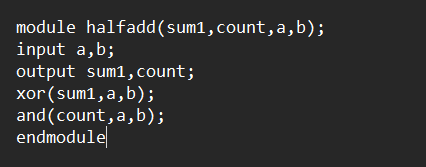
1. TITLE: Write a verilog program to model a half adder. Generate the VVP output and simulation waveform using GTKWave.

Deliverables

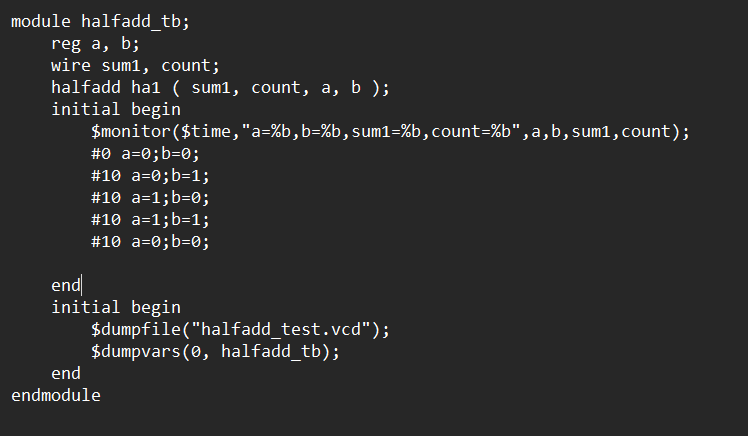
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

I.Verilog Code Snippet

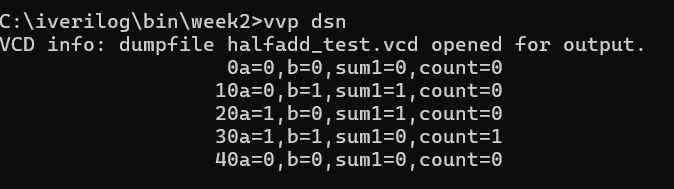
* Main code



* Test Bench



II Verilog VVP output ScreenShot



III GTKWave ScrrenShot



IV Truth Table

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | SUM | CARRY |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

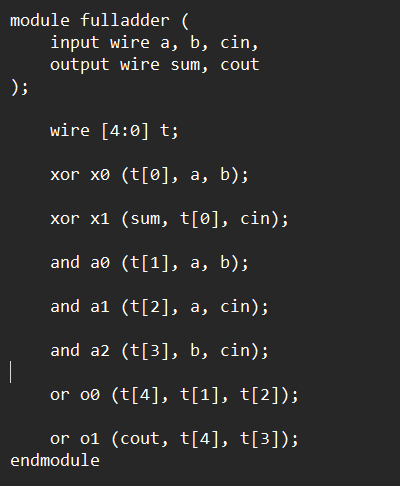
2.TITLE: Write a verilog program to model a full adder. Generate the VVP output and simulation waveform using GTKWave.

Deliverables

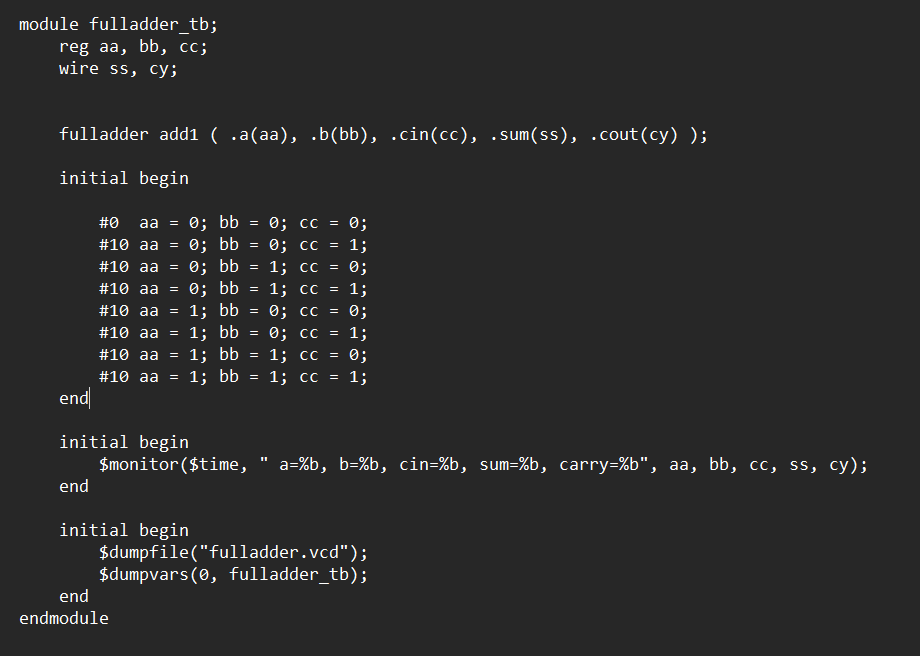
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

I.Verilog Code Snippet

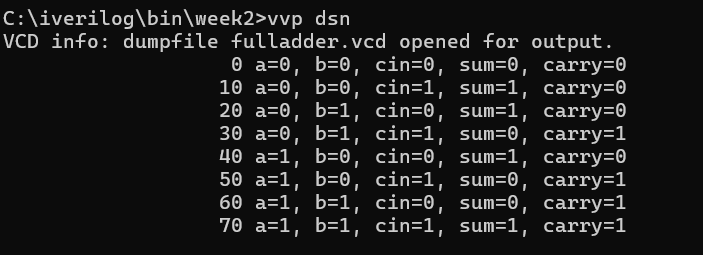
* Main Code



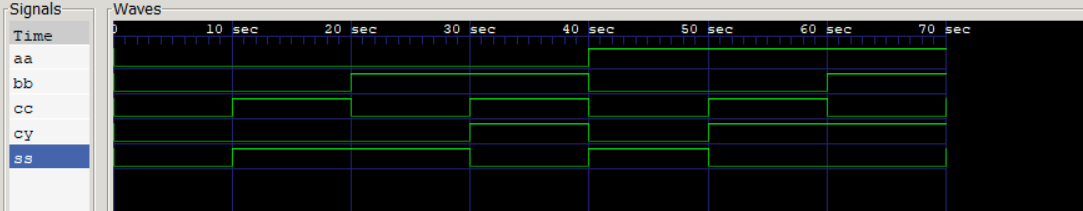
* TestBench



II Verilog VVP ScreenShot



III GTK wave Screenshot



IV Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | SUM | CARRY |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |