**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:08-09-2025

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| --- | --- | --- |
| Name: Aakash Desai | SRN:PES1UG24CS006 | Section  3A |

Week Number: 5 Program Number: 1

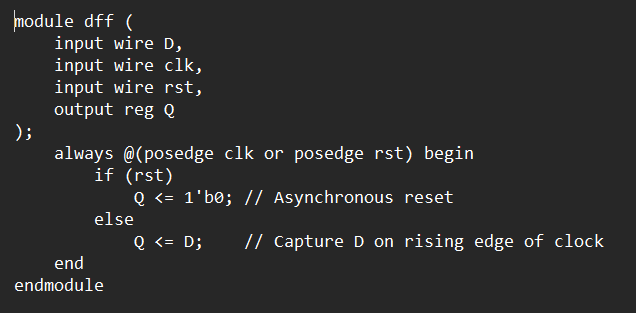
TITLE:Write a verilog program to model a D Flip-flop. Generate the VVP output and simulation waveform using GTKWave.

Deliverables

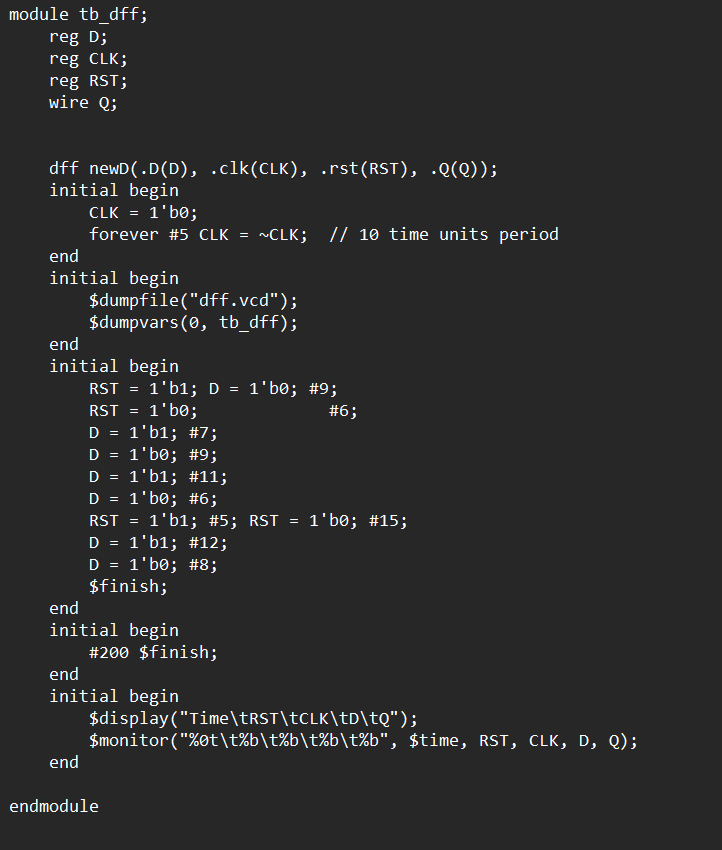
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

I.Verilog Code Snippet

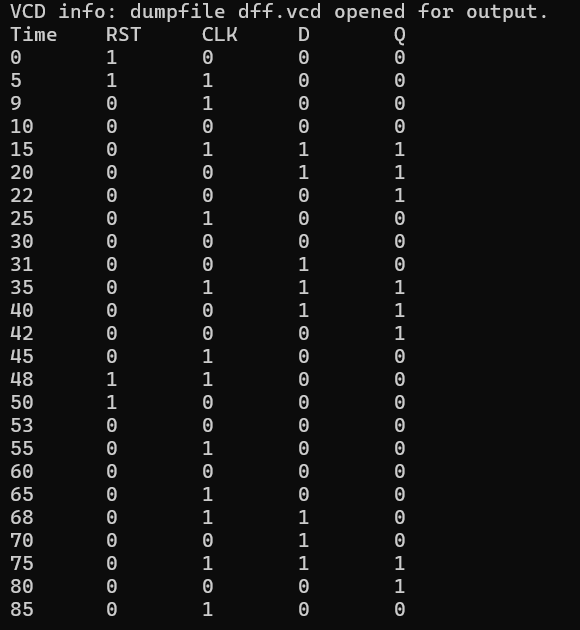
* Main code



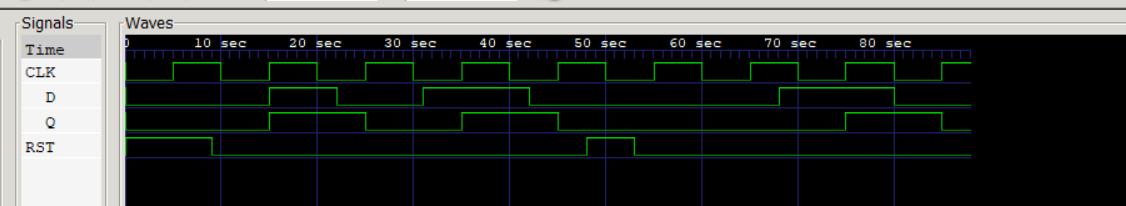
* Test Bench



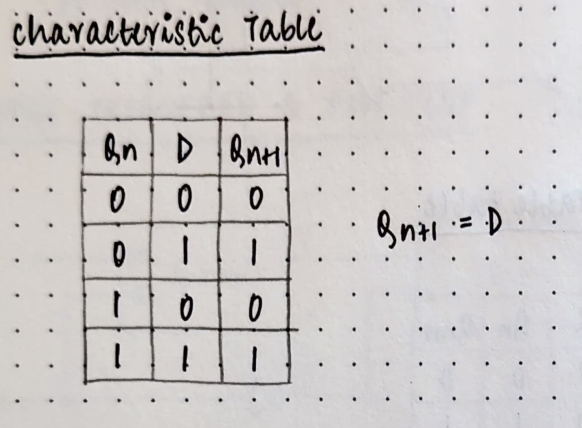
II Verilog VVP output ScreenShot



III GTKWave ScreenShot



IV Characteristic Table



TITLE:Write a verilog program to model T Flip-flop.

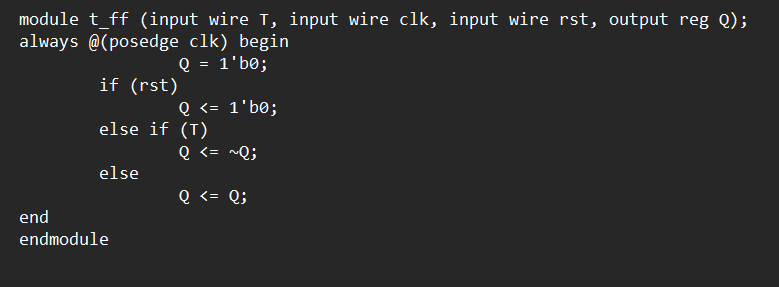
Generate the VVP output and simulation waveform using GTKWave.

Deliverables

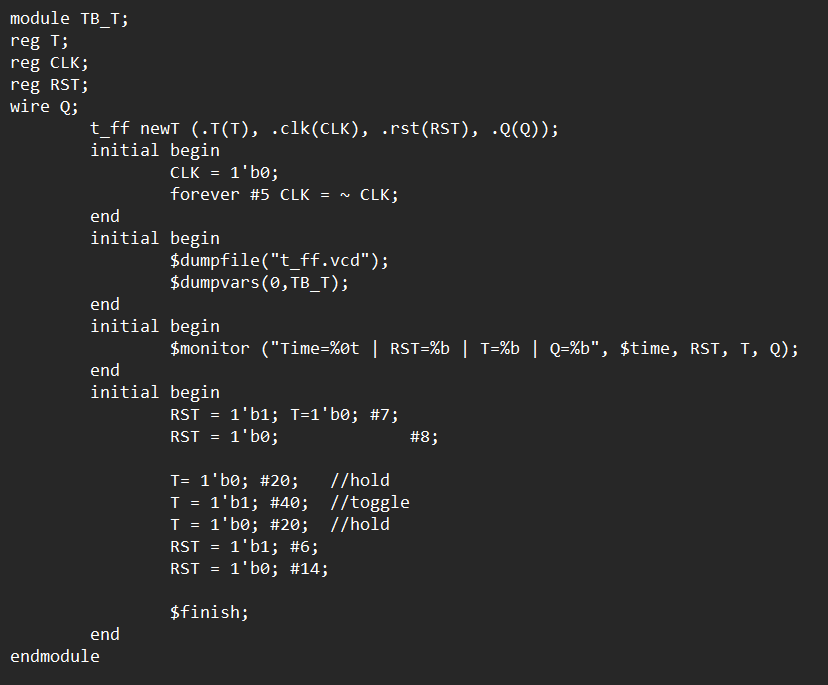
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

I.Verilog Code Snippet

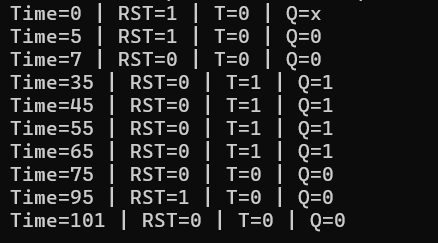
* Main Code



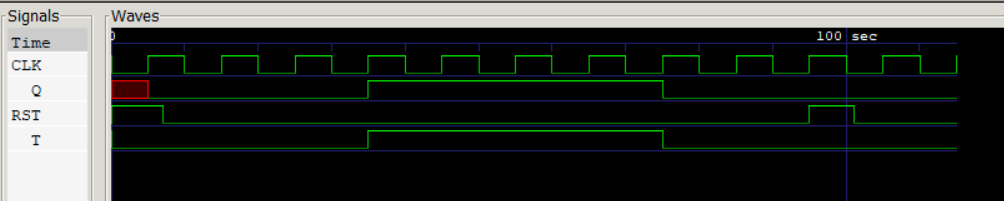
* Test Bench



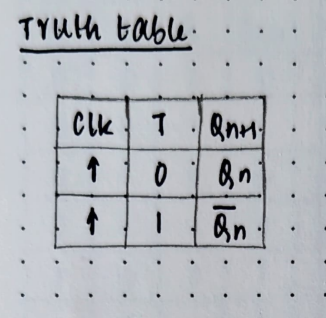
II Verilog VVP ScreenShot



III GTK wave Screenshot



IV Truth Table

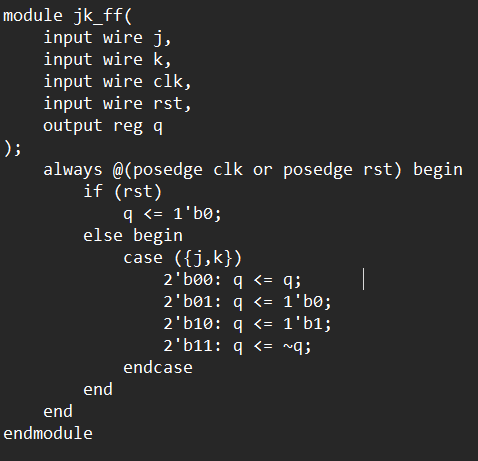


TITLE:Write a verilog program to model J-K Flip Flop.Generate the VVP output and simulation waveform using GTKWave.

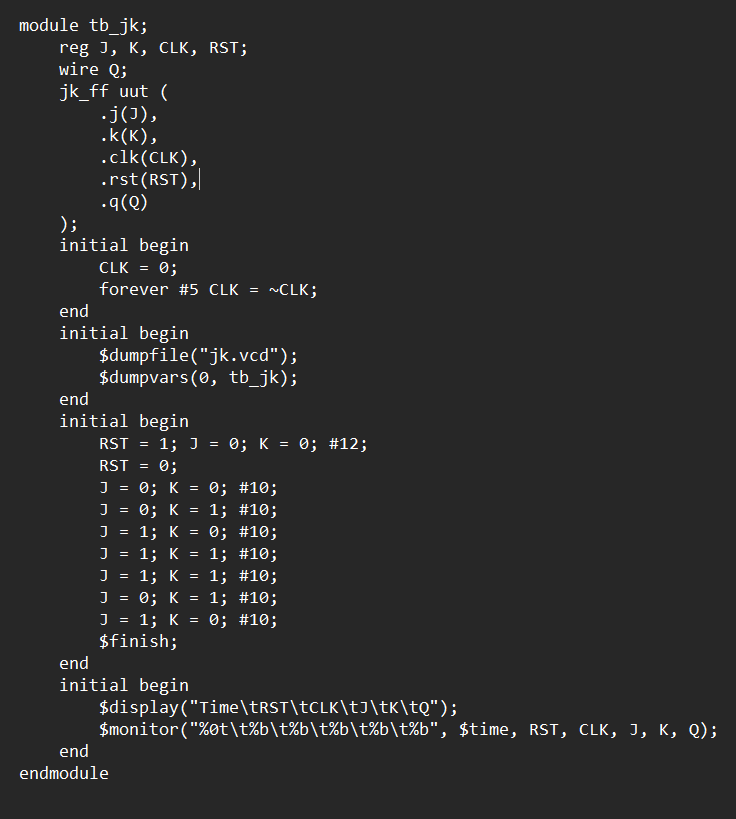
Deliverables

1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

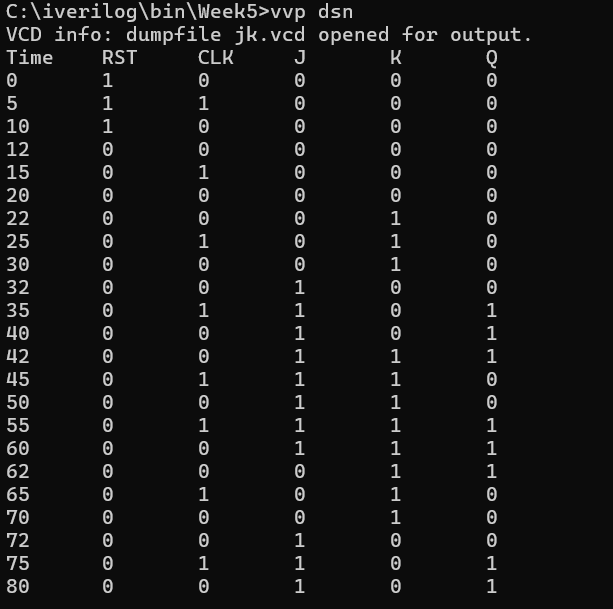
* I Iverilog code

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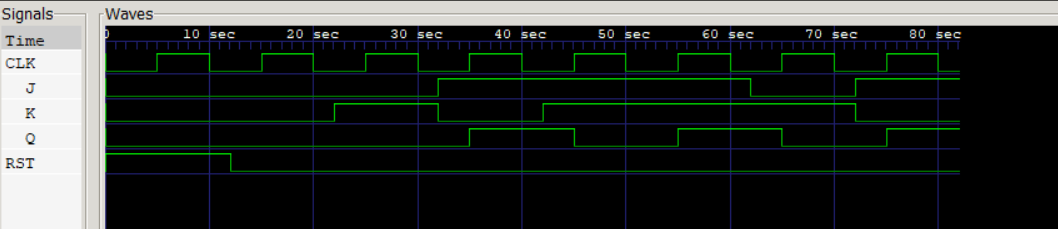
* Testbench



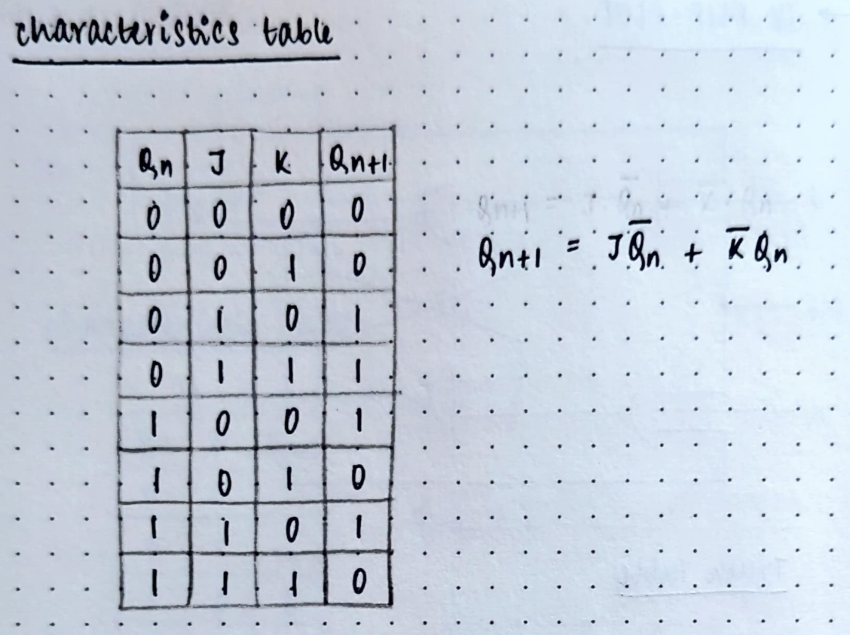
II VVP screenshot



III GTKwave screenshot



IV Characteristic Table



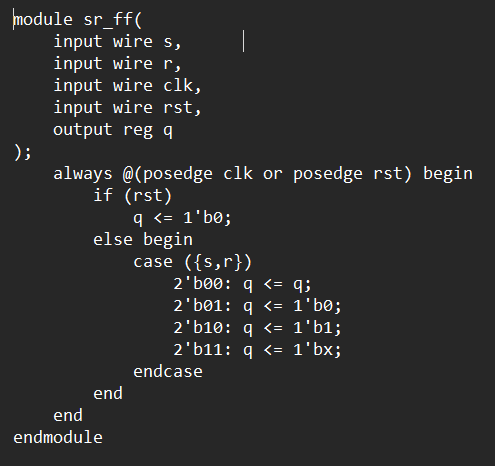
TITLE:Write a verilog program to model SR Flip Flop. Generate the VVP output and simulation waveform using GTKWave.

Deliverables

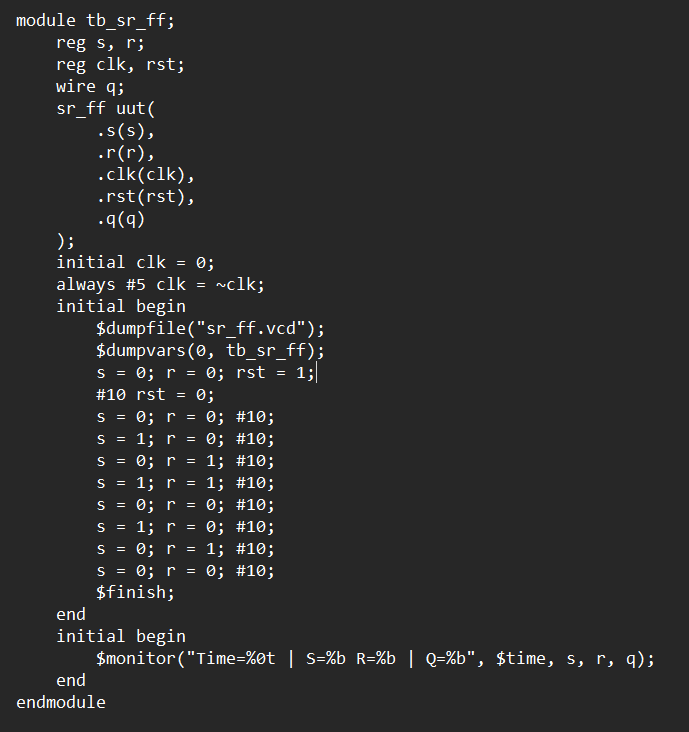
1. Verilog Code Screenshot
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3. GTKWAVE Screenshot
4. Output Table to be completed and included

I.Verilog code

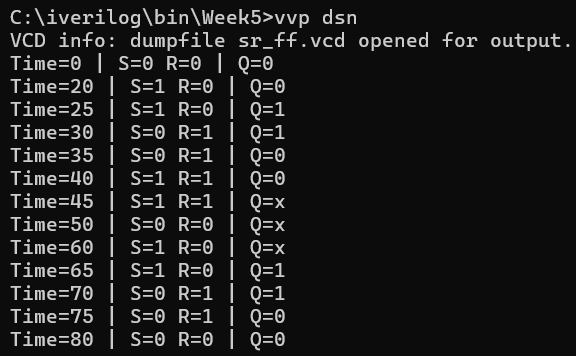
* Main code



* Test bench



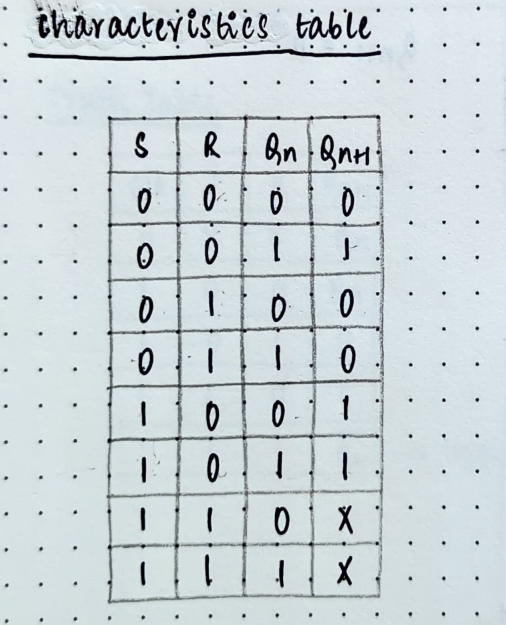
II VVP Screenshot



III GTKWave output



IV Truth Table



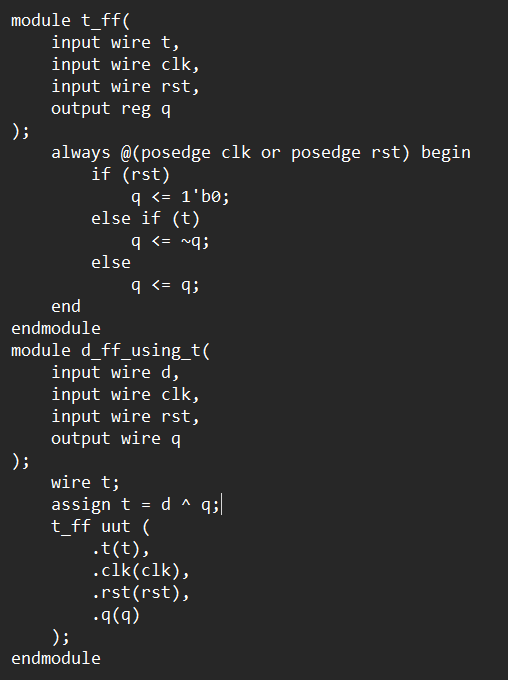
TITLE:Write a verilog program to design and implement a D flip flop using a T flip flop. Generate the VVP output and simulation waveform using GTKWave.

Deliverables

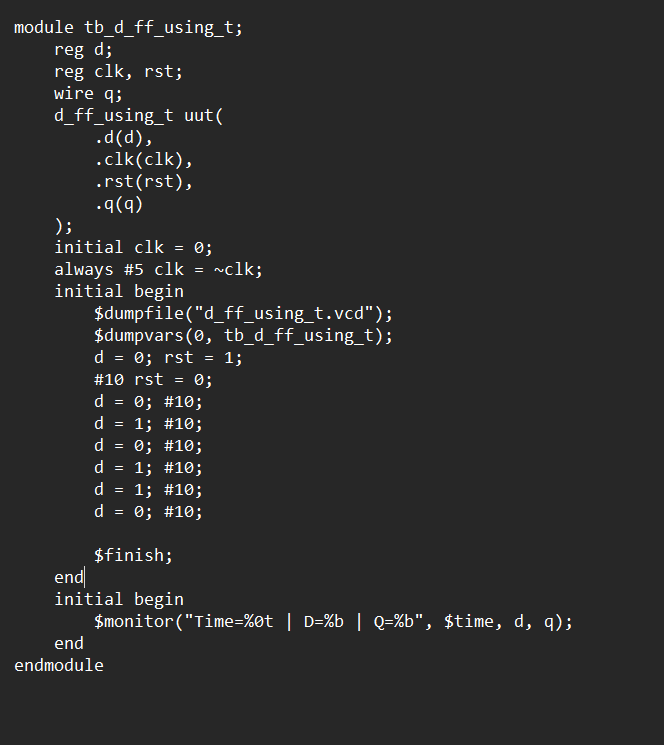
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

I Verilog Code

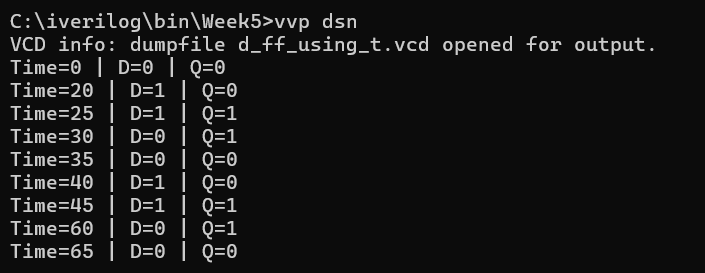
* Main code



* Test bench



II VVP output Screenshot



III GTKwave output screenshot

IV Truth Table

