**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:29-09-2025

|  |  |  |
| --- | --- | --- |
| Name: Aakash Desai | SRN:PES1UG24CS006 | Section  3A |

Week Number: 6 Program Number: 1

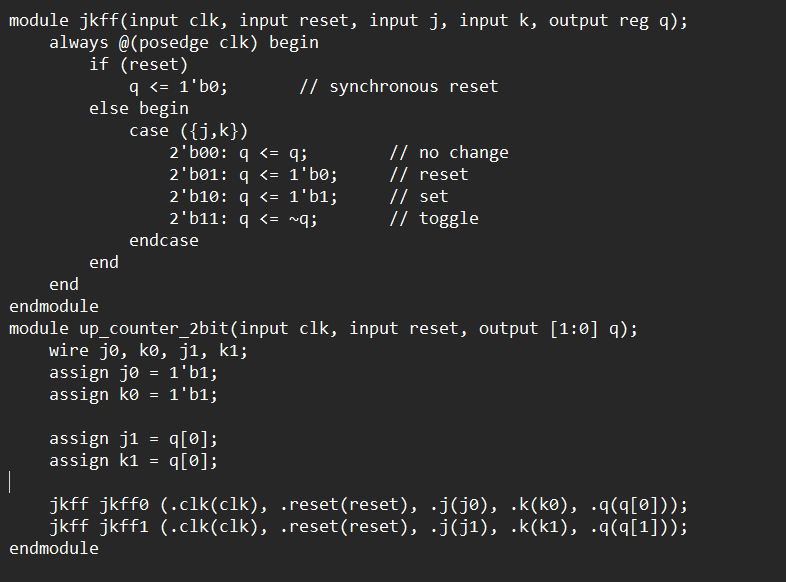
TITLE:Write an iverilog program to design and implement a 2-bit up counter using JK flip flops.Generate the VVP output and simulation waveform using GTKWave.

Deliverables

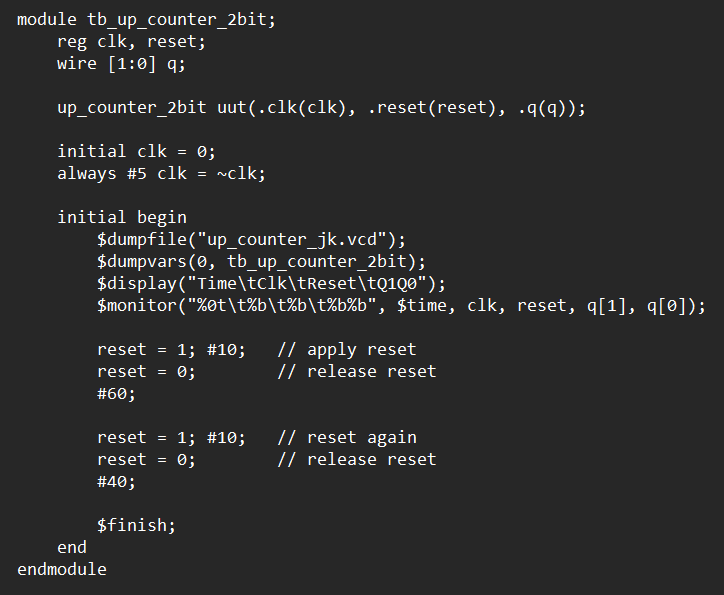
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

I.Verilog Code Snippet

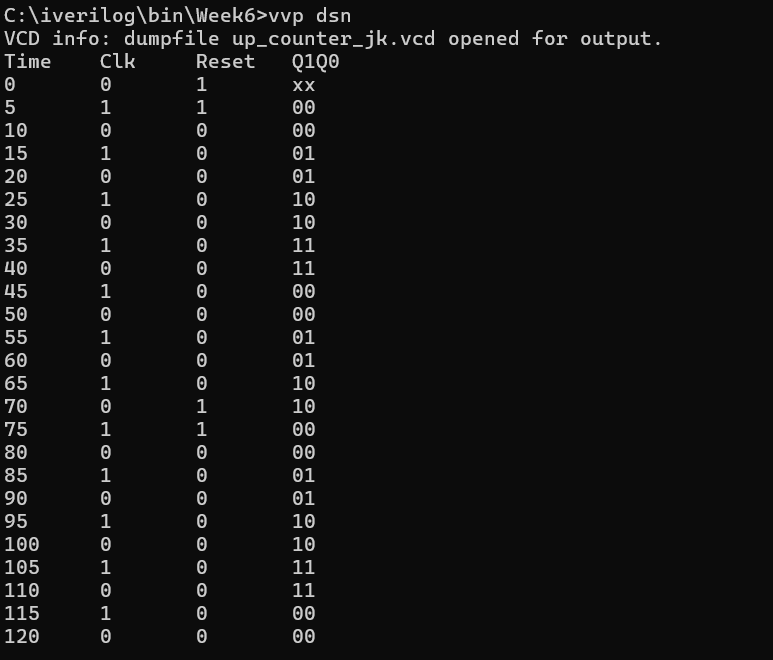
* Main code



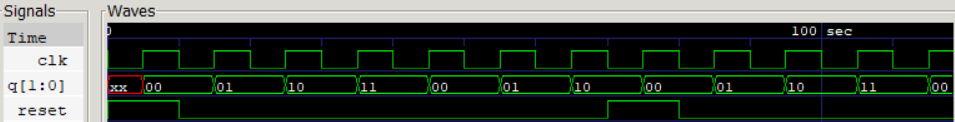
* Test Bench



II Verilog VVP output ScreenShot



III GTKWave ScreenShot



IV Excitation Table

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Current State | | Next State | | Flip Flops | | | |
| Q1 | Q0 | Q1 | Q0 | J1 | K1 | J0 | K0 |
| 0 | 0 | 0 | 1 | 0 | X | 1 | X |
| 0 | 1 | 1 | 0 | 1 | X | X | 1 |
| 1 | 0 | 1 | 1 | X | 0 | 1 | X |
| 1 | 1 | 0 | 0 | X | 1 | X | 1 |

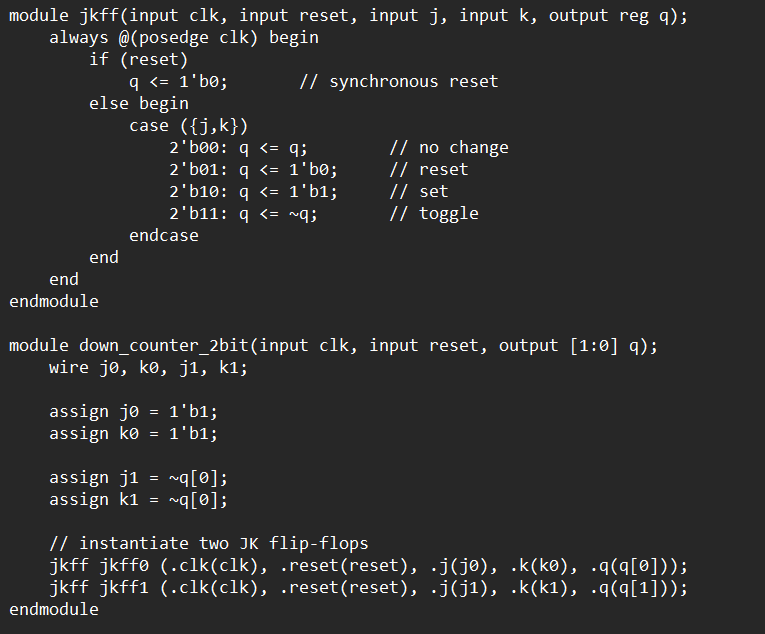
TITLE:Write an iverilog program to design and implement a 2-bit down counter using JK flip flops.Generate the VVP output and simulation waveform using GTKWave.

Deliverables

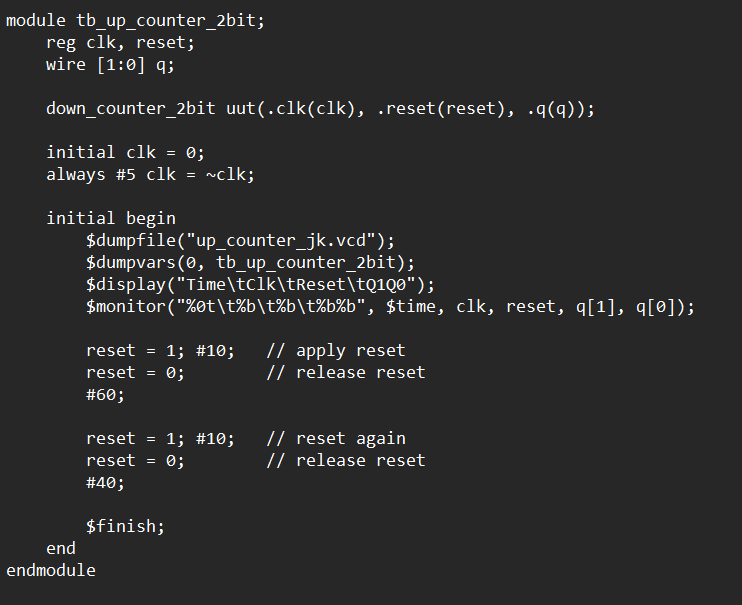
1. Verilog Code Screenshot
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3. GTKWAVE Screenshot
4. Output Table to be completed and included

I.Verilog Code Snippet

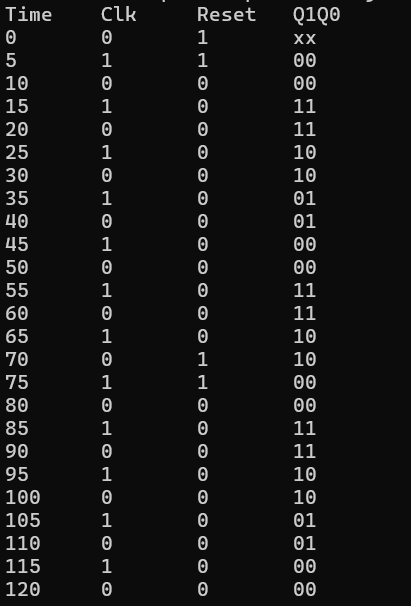
* Main Code



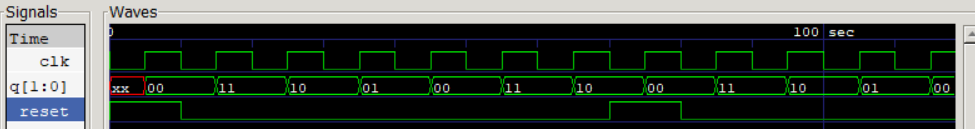
* Test Bench



II Verilog VVP ScreenShot



III GTK wave Screenshot



IV Excitation Table

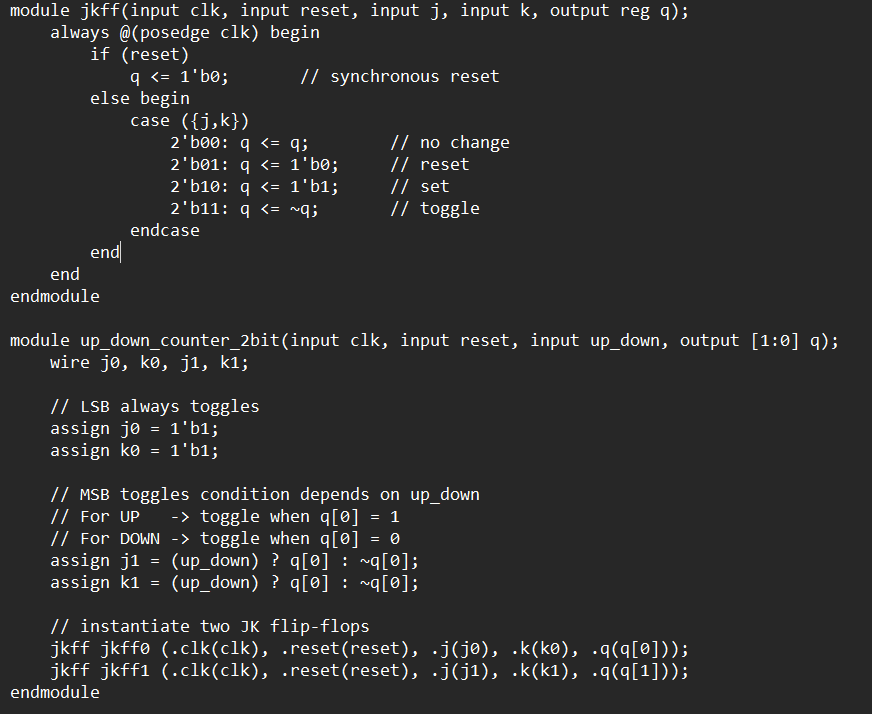
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Current State | | Next State | | Flip Flops | | | |
| Q1 | Q0 | Q1 | Q0 | J1 | K1 | J0 | K0 |
| 0 | 0 | 1 | 1 | 1 | X | 1 | X |
| 0 | 1 | 0 | 0 | 0 | X | X | 1 |
| 1 | 0 | 0 | 1 | X | 1 | 1 | X |
| 1 | 1 | 1 | 0 | X | 0 | X | 1 |

TITLE:Write an iverilog program to design and implement a 2-bit up-down counter using JK flip flops.Generate the VVP output and simulation waveform using GTKWave.

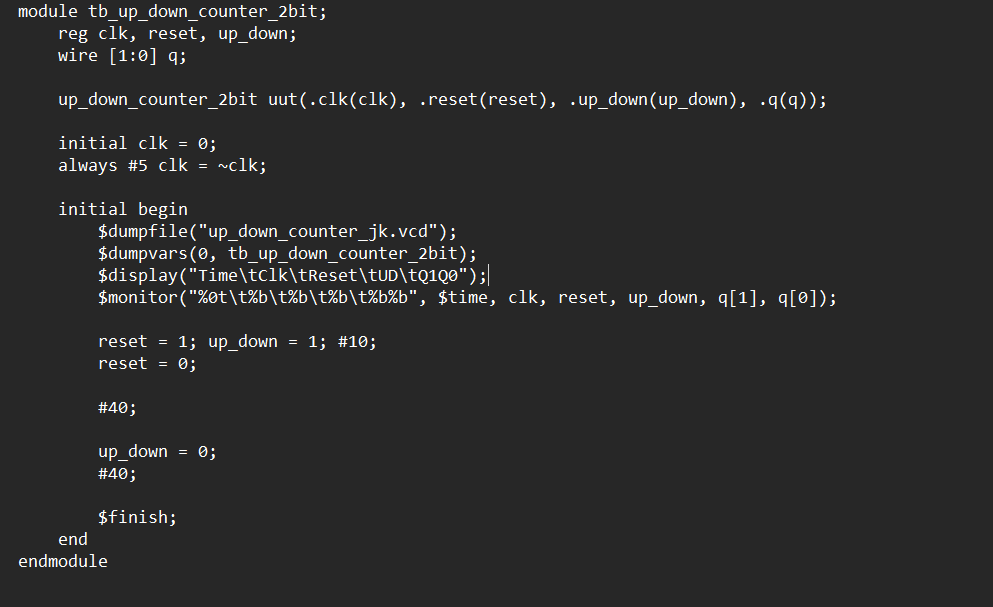
Deliverables

1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

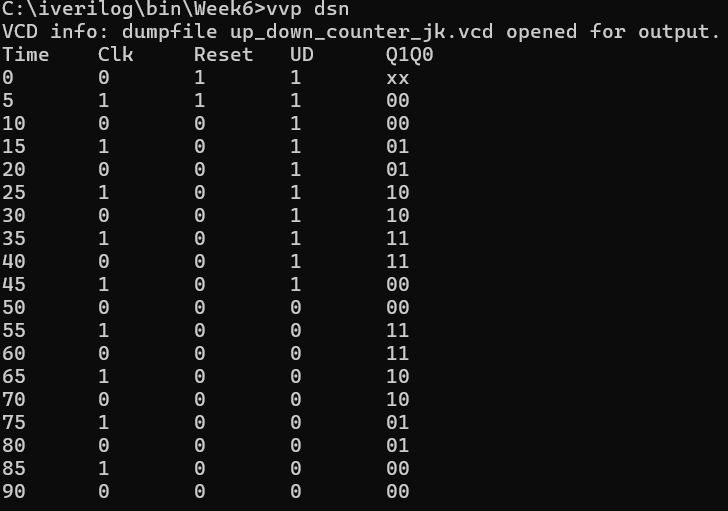
* I Iverilog code

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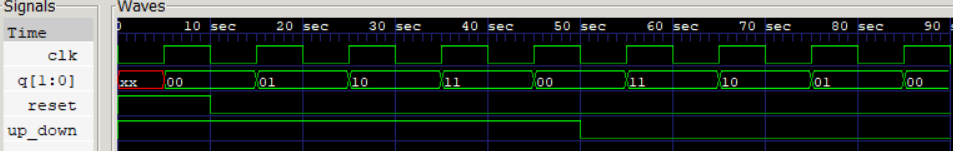
* Testbench



II VVP screenshot



III GTKwave screenshot



IV Characteristic Table

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Mode Select | Current State | | Next State | | Flip Flops | | | |
| Q1 | Q0 | Q1 | Q0 | J1 | K1 | J0 | K0 |
| 0 | 0 | 0 | 0 | 1 | 0 | X | 1 | X |
| 1 | 0 | 0 | 1 | 1 | 1 | X | 1 | X |
| 0 | 0 | 1 | 1 | 0 | 1 | X | X | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | X | X | 1 |
| 0 | 1 | 0 | 1 | 1 | X | 0 | 1 | X |
| 1 | 1 | 0 | 0 | 1 | X | 1 | 1 | X |
| 0 | 1 | 1 | 0 | 0 | X | 1 | X | 1 |
| 1 | 1 | 1 | 1 | 0 | X | 0 | X | 1 |

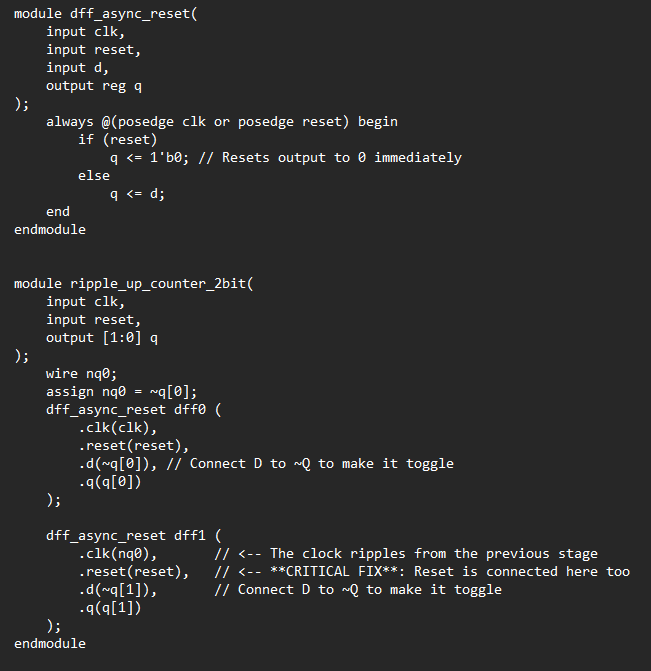
TITLE:Write a verilog program to design a 2 bit ripple up counter using D flip flop. Generate the VVP output and simulation waveform using GTKWave.

Deliverables

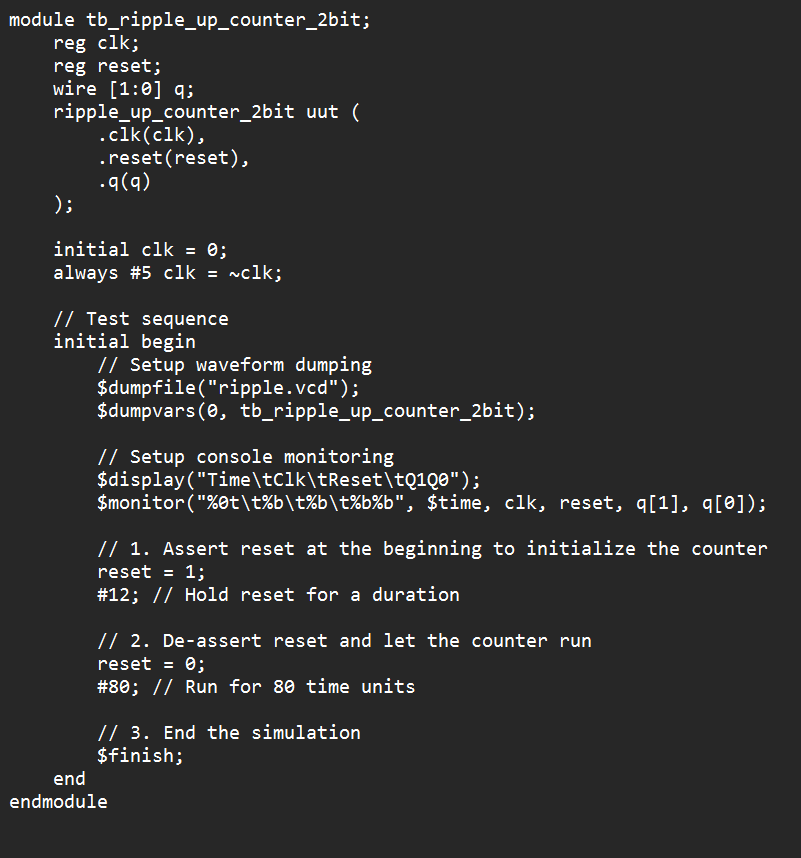
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

I.Verilog code

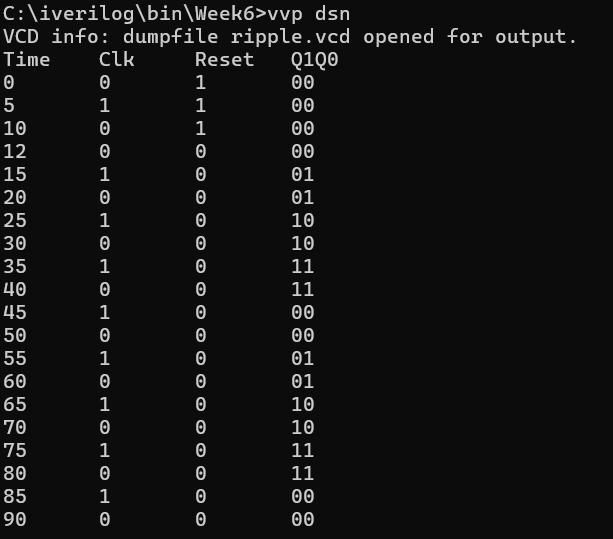
* Main code



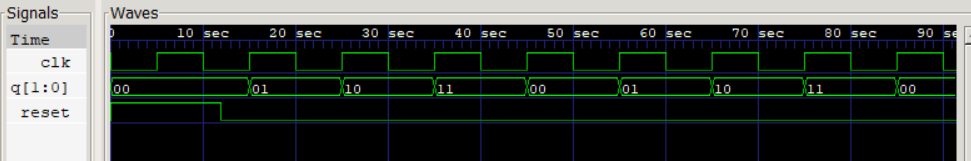
* Test bench



II VVP Screenshot



III GTKWave output



IV State Transition Table

|  |  |  |  |
| --- | --- | --- | --- |
| Current State | | Next State | |
| Q1 | Q0 | Q1 | Q0 |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

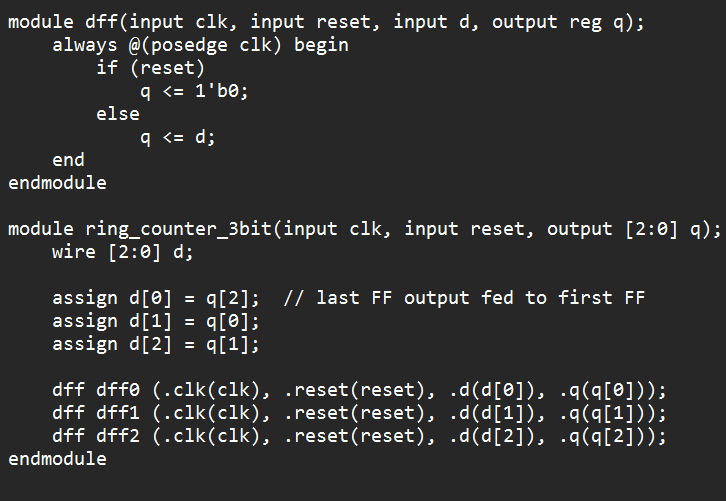
TITLE:Write a verilog program to design and implement a 3 bit Ring Counter using D Flip flop. Generate the VVP output and simulation waveform using GTKWave.

Deliverables

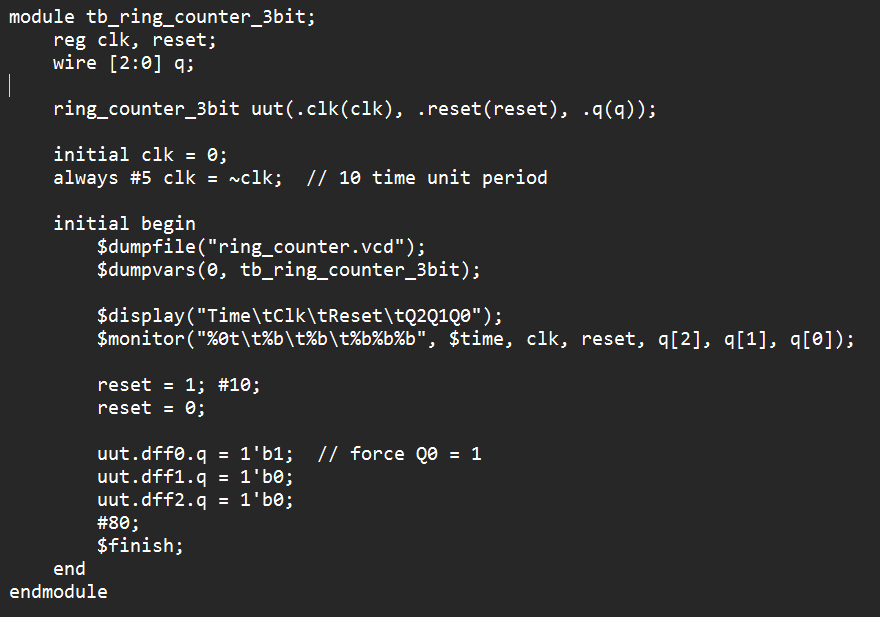
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

I Verilog Code

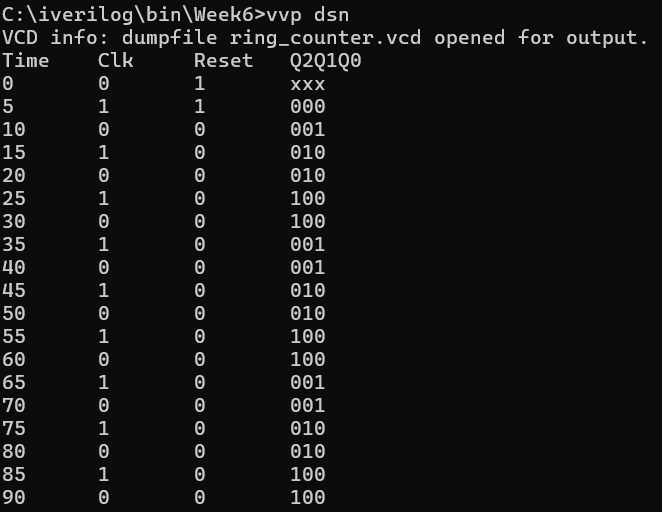
* Main code



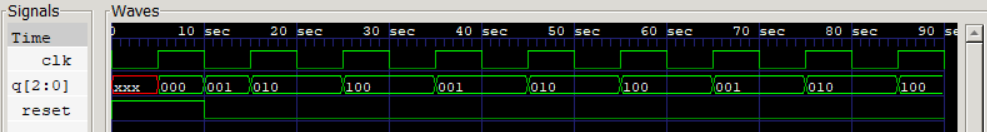
* Test bench



II VVP output Screenshot



III GTKwave output screenshot



IV Transition Table

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Current State | | | D inputs | | | Next State | | |
| Q2 | Q1 | Q0 | D2 | D1 | D0 | Q2 | Q1 | Q0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |

The counter has been initialized to a "one-hot" state of **001**.

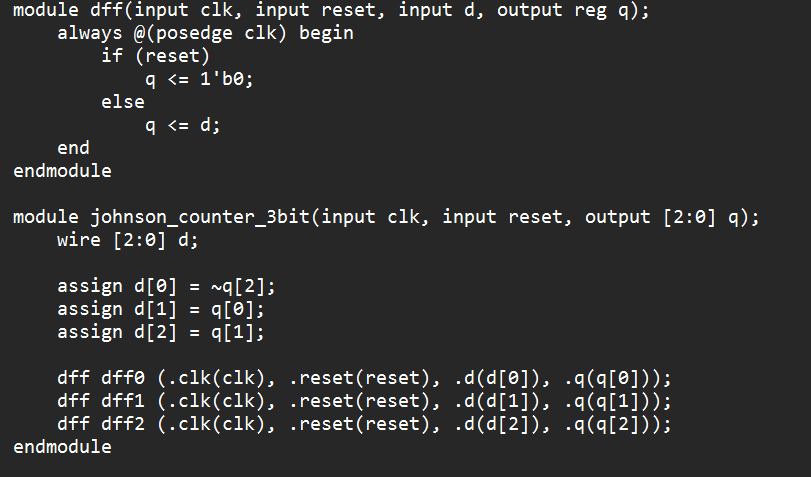
TITLE:Write a verilog program to design and implement a 3 bit Johnson Counter using D Flip flop. Generate the VVP output and simulation waveform using GTKWave.

Deliverables

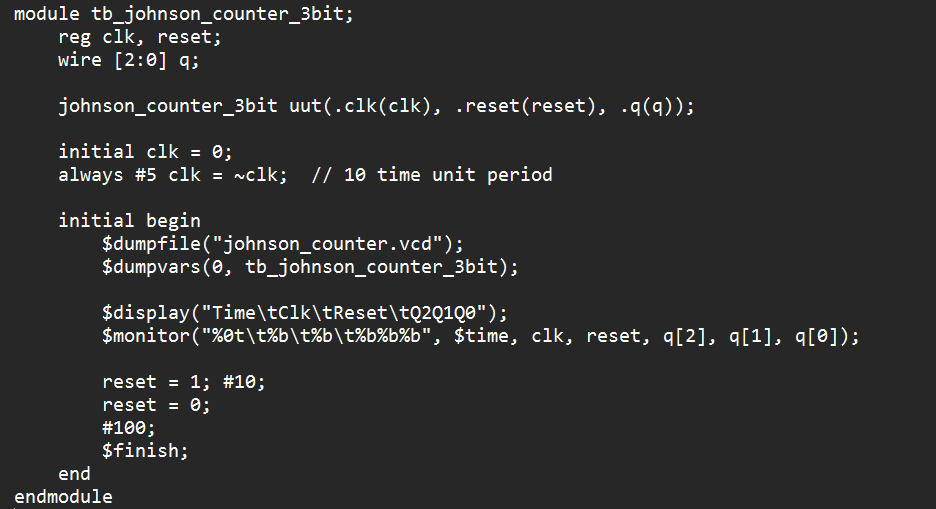
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

I Verilog Code

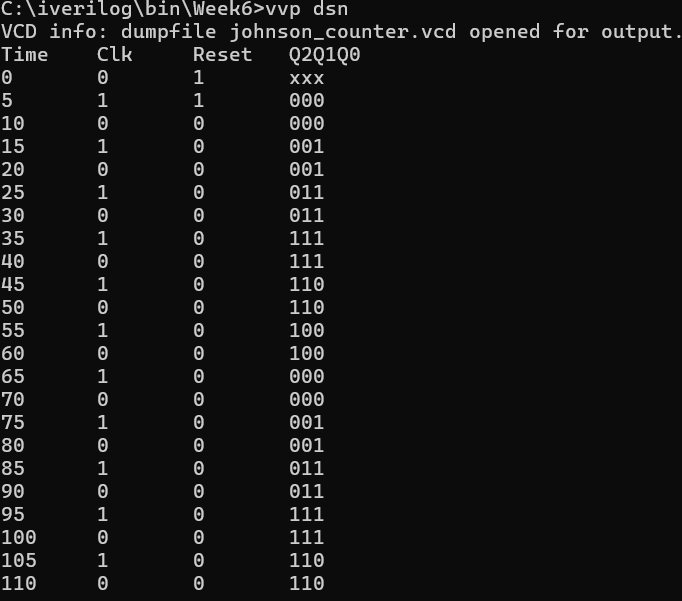
Main code



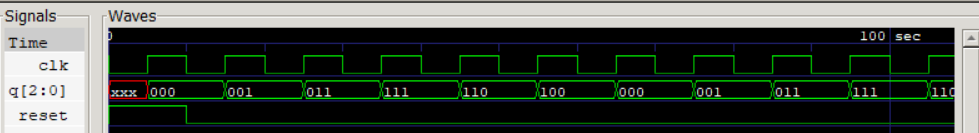
Test Bench File



II VVP Output Screenshot



III GTKwave output screenshot



IV Table

The counter is initialized to an all-zero state.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Current State | | | D inputs | | | Next State | | |
| Q2 | Q1 | Q0 | D2 | D1 | D0 | Q2 | Q1 | Q0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |