**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:06-10-2025

|  |  |  |
| --- | --- | --- |
| Name: Aakash Desai | SRN:PES1UG24CS006 | Section  3A |

Week Number: 7 Program Number: 1

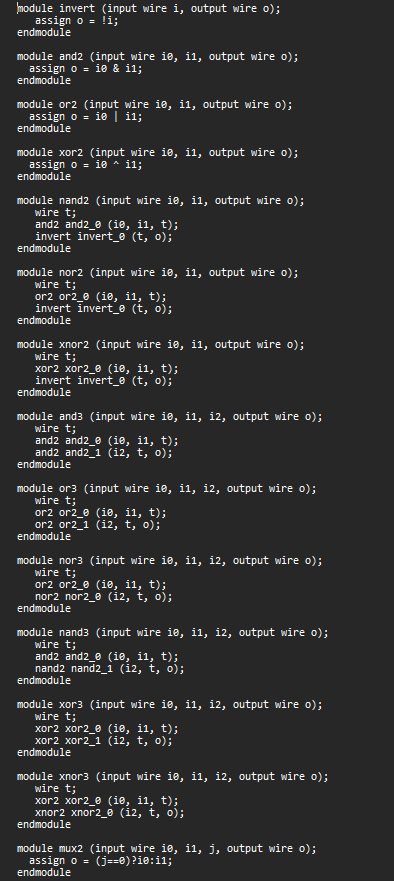
TITLE:Write a verilog program to model a 16 bit ALU. Generate the VVP output and simulation waveform using GTKWave.

Deliverables

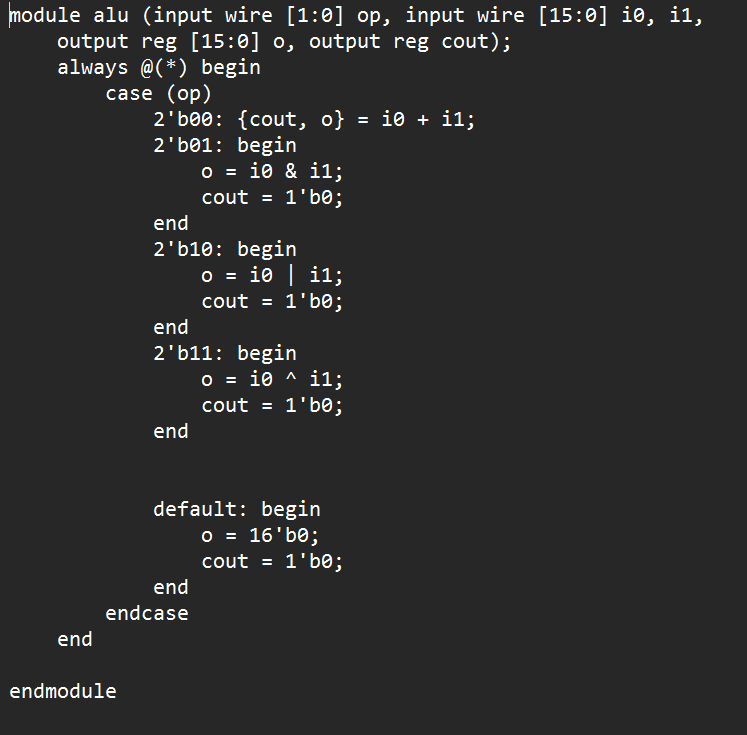
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

I.Iverilog Code

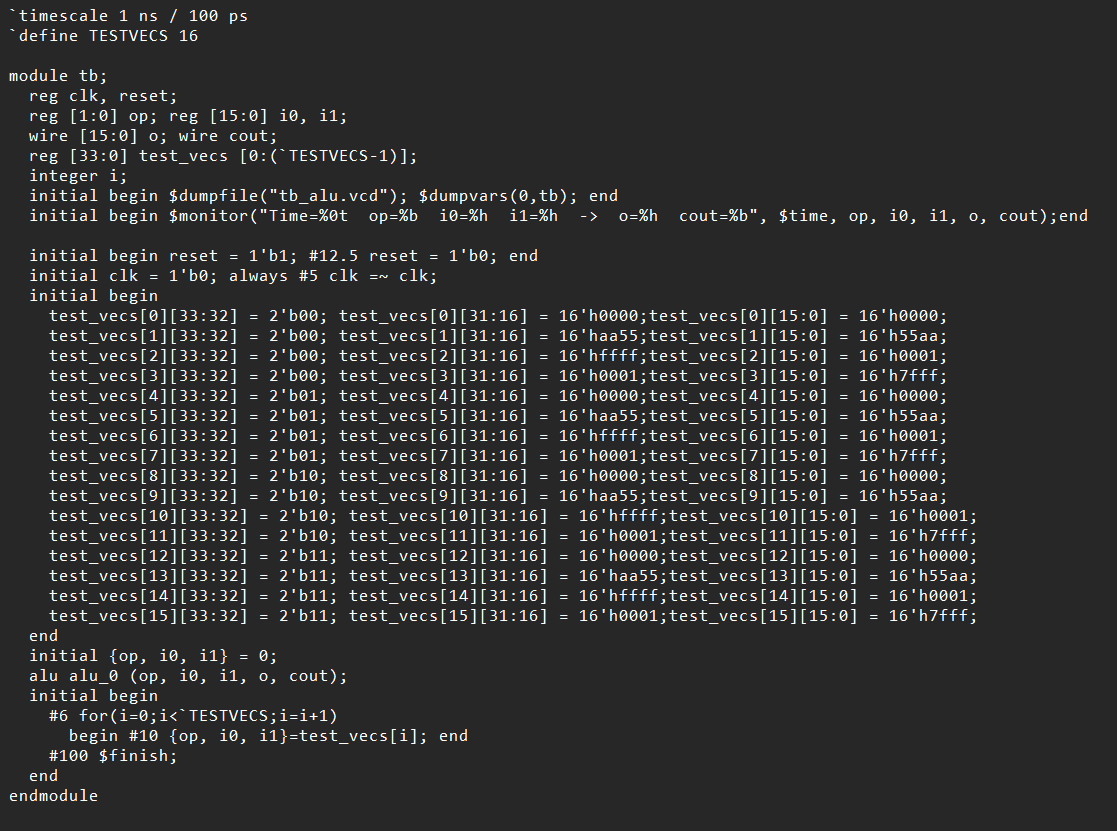
a) lib.v



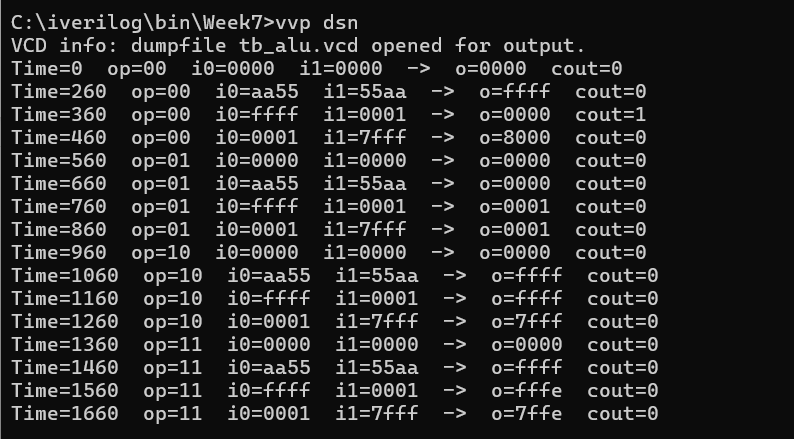
b) alu.v



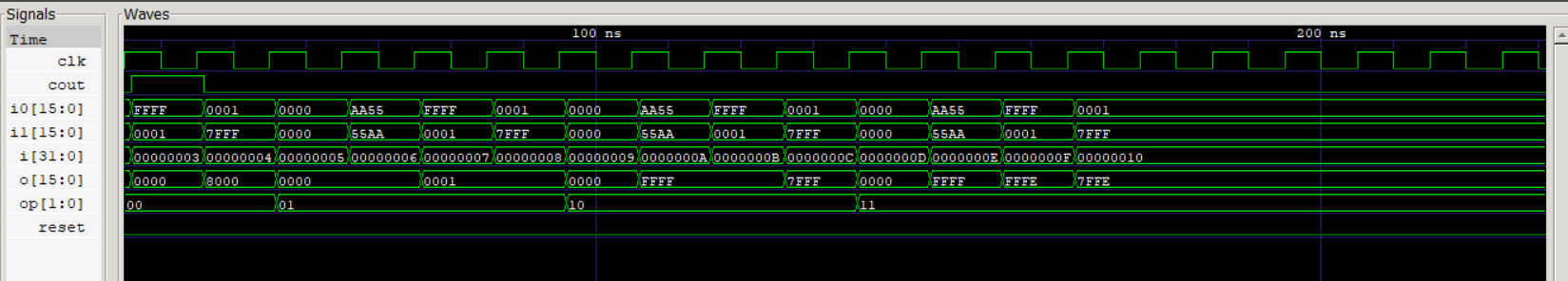
c) alu\_tb.v



II VVP output ScreenShot



III GTKWave output Screenshot



IV output table

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Operation | Op | Input(i0) | Input(i1) | Output(o) | Output(cout) |
| ADD | 00 | aa55 | 55aa | ffff | 0 |
| ADD | 00 | ffff | 0001 | 0000 | 1 |
| ADD | 00 | 0001 | 7fff | 8000 | 0 |
| AND | 01 | aa55 | 55aa | 0000 | 0 |
| AND | 01 | ffff | 0001 | 0001 | 0 |
| AND | 01 | 0001 | 7fff | 0001 | 0 |
| OR | 10 | aa55 | 55aa | ffff | 0 |
| OR | 10 | ffff | 0001 | ffff | 0 |
| OR | 10 | 0001 | 7fff | 7fff | 0 |
| XOR | 11 | aa55 | 55aa | ffff | 0 |
| XOR | 11 | ffff | 0001 | fffe | 0 |
| XOR | 11 | 0001 | 7fff | 7ffe | 0 |