Full Adder Optimization using Logical Effort

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***Abstract*—This report outlines a size and delay optimized full adder design developed using logical effort techniques. The designed full adder was then used to construct a schematic and and layout by utilizing Cadence. Finally, the delays were compared between the calculated, schematic, and extracted layout.**

I. Introduction

The goal of this paper is to reduce the delay that is present when designing logical circuits. To do this, logical effort will be used as a method for optimizing delay for a full adder logical circuit design that is powering a 90C load. Logical effort accomplishes this by optimizing the logical gate sizes along the worst case path from the input to the output. When designing the optimal full adder delay was not the only constraint considered. Once a delay optimized circuit was developed, the gate sizes of the individual logical gates were then reduced for an exchange of a slight increase in delay. This was done to reduce the overall size of the layout package.

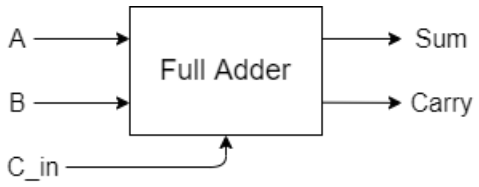

Fig. 1: Full Adder Block Diagram

A block diagram for the full adder is shown in figure 1, and it is an electronic circuit comprised of three binary logic gate (i.e., NOT, NAND and NOR gates) that can be designed to perform the logic function A+B=C. The block diagram has three inputs: A, B and Cin, and the outputs are carry and the sum of the inputs. The output is a sum of the inputs A and B and a carry bit Cin. The functionality and the full adder and its respective karnaugh map (k-map) reduction and logical design is shown in the background section of the paper.

Three varying designs for a full adder are made to analyze the difference in delay and logical effort that may arise due the different logical gates. The three design are shown in the procedure section of the paper and were made with the information gained from the k-map logical design calculations made in the background section of the paper. The design with the least delay will be picked and the layout for it will be constructed using Cadence following the MOSIS SUBM rules. The delay comparisons between the calculated logical effort desing, the layout constructed of the design, and the extracted view of the layout are discussed in the results and analysis section of the paper.

II. Background

Table I, shows the logical truth table for the full adder. As it can be seen, the Sum output is set to high with only one or all of the inputs are high, and the Cout (carry) bit is set to high when two or more inputs are set to high.

TABLE I: Full Adder Truth Table

Input			Output	
A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Karnaugh maps can be used to reduce the logic down. Figure 2 shows the k-map for the Carry logic and figure 3 shows the k-map reduction for the Sum logic. Line one of equation 1 shows the k-map simplification of the carry logic, the k-map simplification can then be further simplified using logic simplification shown in the rest of the equation. Similarly, line one of equation 2 shows the k-map simplified version of the sum logic. Unfortunately, not much can be simplified using k-map here, so the remainder of the equation shows the simplification made using logic simplification.

A \ BC_{in}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Fig. 2: Carry K-Map

$$\begin{aligned} Carry &= AB + AC + BC \\ &= AB + C(A\overline{B} + \overline{A}B) \\ &= AB + C(A \oplus B) \end{aligned} \tag{1}$$

A \ BC_{in}	00	01	11	10
0	0	1	0	1
1	1	0	1	0

Fig. 3: Sum K-Map

$$\begin{aligned} Sum &= \overline{A}B\overline{C} + \overline{A}\overline{B}C + ABC \\ &= A(\overline{B}\overline{C} + BC) + \overline{A}(B\overline{C} + \overline{B}C) \\ &= A(\overline{B \oplus C}) + \overline{A}(B \oplus C) \\ &= A \oplus B \oplus C \end{aligned} \tag{2}$$

Figures 4, 5, and 6, show the three variation of full adders that were developed to be compared, where the logic gates highlighted in green and blue are the worst path from input A to the Sum and Carry respectively. The Sum components for all three designs were developed using two XOR gates which consisted of four NAND gates each. The difference in the Sum logic for the three design are in the placement and logical gate used for the inverter, which was needed as the input logic was inverted due to the 3C input inverters. For the Carry logic, alongside testing the effect of inverter placement, a third design was developed for logic made using only NORs and Inverters. Next equations 3-9 were used to make all the logical effort calculations for the three designs. Alongside the calculations an algorithm was developed to automate the gate sizing calculation using the logical effort values, the algorithm is shown in algorithm 1, the code used for which is given in the appendix.

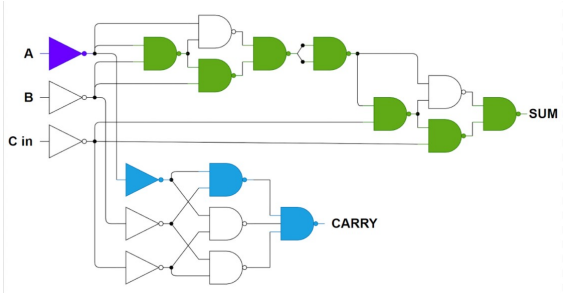

Fig. 4: Design 1

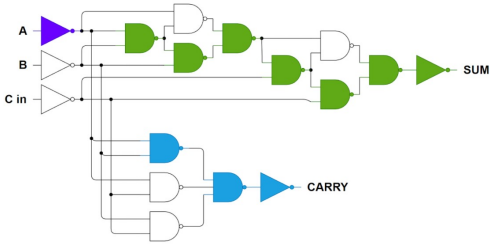

Fig. 5: Design 2

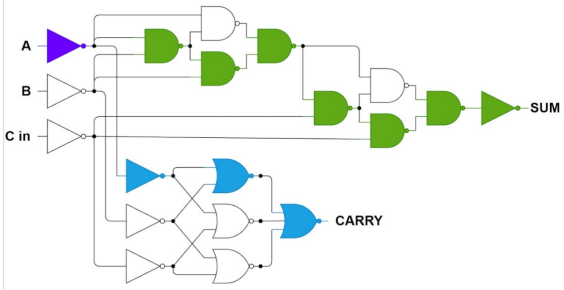

Fig. 6: Design 3

$$\text{Logical Effort (G)} = \prod_{i=1}^{N} g_i \tag{3}$$

$$\text{Branching Effort (B)} = \prod_{i=1}^{N} b_i \tag{4}$$

$$\text{Electrical Effort (H)} = \frac{C_{pathout}}{C_{pathin}} \tag{5}$$

$$\text{Parasitic Delay (P)} = \sum_{i=1}^{N} p_i \tag{6}$$

$$\text{Effort Delay (F)} = \sum_{i=1}^{N} f_i = \sum_{i=1}^{N} g_i b_i h_i = GBH \tag{7}$$

$$\text{Delay (D)} = F + P = GHB + P = N\hat{f} + P \tag{8}$$

$$\text{Gate Sizing } C_{in} = \frac{C_{out} g_i}{\hat{f}} \tag{9}$$

Algorithm 1: Compute gate sizes

Input: $\hat{f}$, N, G
Output: array of gate sizes
cin = [];
cout = [90];
while *current N not 0* **do**
  $cin = \frac{cout[-1] * G[-i]}{f}$;
  cin.append(cin);
  cout.append(cin[i-1]);
  round cin to nearest min gate size value;
  N = N-1 ;
end

Figures 7, 8, and 9 show the calculation outputs containing the delay and gate sizes for designs 1, 2, and 3, respectively. Using these calculated results, design 2 is picked as the optimal full adder as it provides the best combination of small gates sizes without sacrificing on delay.

	A to SUM [4 Iterations]	A to Carry [2 Iterations]
Stages (N)	8	4
Logical Effort (G)	$\left(\frac{4}{3}\right)^7$	$\frac{20}{9}$
Electrical Effort (H)	30	30
Path Parasitic Delay (P)	15	7
Branching Effort (B)	38.5	3.0
Path Effort (F)	8652.73	200.0
Delay (D)	39.845	22.04
Best stage effort ($\hat{f}$)	3.1056	3.761
Best number of stages (N)	7	4
Gate Sizes	[3, 4, 4, 4, 4, 8, 16, 40]	[3, 3, 16, 40]

Fig. 7: Calculations for Design 1

	A to SUM [3 Iterations]	A to Carry [3 Iterations]
Stages (N)	8	4
Logical Effort (G)	$\left(\frac{4}{3}\right)^6$	$\frac{20}{9}$
Electrical Effort (H)	30	30
Path Parasitic Delay (P)	14	7
Branching Effort (B)	64	2.8
Path Effort (F)	10787.81	186.67
Delay (D)	39.539	21.79
Best stage effort ($\hat{f}$)	3.19	3.7
Best number of stages (N)	7	4
Gate Sizes	[3, 4, 4, 4, 4, 4, 12, 27]	[3, 4, 10, 24]

Fig. 8: Calculations for Design 2

	A to SUM [4 Iterations]	A to Carry [4 Iterations]
Stages (N)	8	4
Logical Effort (G)	$\left(\frac{4}{3}\right)^6$	35/9
Electrical Effort (H)	30	30
Path Parasitic Delay (P)	14	7
Branching Effort (B)	16.5	2.8
Path Effort (F)	2781.235	326.667
Delay (D)	35.559	24.0054
Best stage effort ($\hat{f}$)	2.695	4.251344
Best number of stages (N)	6	4
Gate Sizes	[3, 4, 4, 4, 4, 8, 16, 33]	[3, 6, 20, 49]

Fig. 9: Calculations for Design 3

III. Procedure

Figure 10, shows the standard cell library needed to construct the optimal design. As it shows, there are three unique inverters, two unique two input NANDs and a size 10 three input NAND. Figures 11 and 12 show the standard cell library layouts developed for the standard cell inverters and NANDs, respectively. These standard cell libraries were used to create the snap cell layout and its corresponding extracted view is shown in figure 17.

	Inverter			2 Input NAND		3 Input NAND
Size	3	24	27	4	12	10
P	2	16	18	2	6	4
N	1	8	9	2	6	6
Quantity	3	1	1	6	1	1

Fig. 10: Standard Cell Library

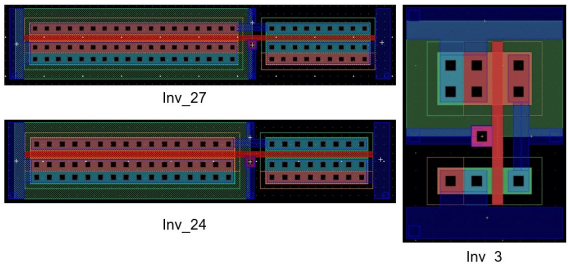

Fig. 11: Standard Cell Library Inverter Layouts

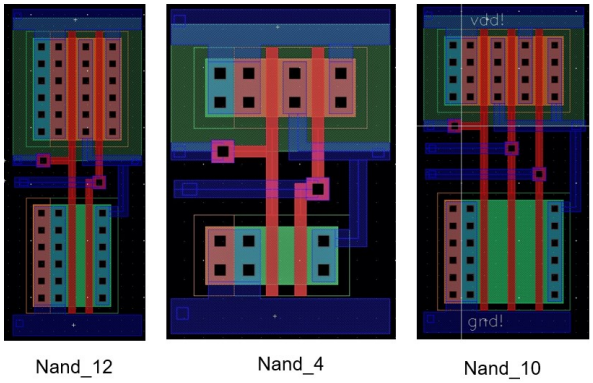

Fig. 12: Standard Cell Library NAND Layouts

IV. Results and Analysis

Table II, shows the configuration used for testing stimuli for the schematic and the layout to get a transient response of the circuit. Figure 13 shows the transient response of the schematic of the final design and figure 14 shows the transient response of the extracted view of the final design.

Transient analysis of all the standard cell schematics and the extracted view, alongside, any other simulations conducted are all provided in the GitHub repository linked in [2] with their corresponding high resolution images of the schematic, layout, and or the extracted view. Figure 15, shows a table of all the calculated delays for the schematic and extracted views for all standard cell and the final design. Finally figure **??** shows a simple bar chart comparing the delays between the calculated values, extracted view, and the schematic of the full final design.

TABLE II: Testing Stimuli with the rise and fall time set to 0.01ns and a 5V DC input

Parameter	A	B	C_{in}
Period (ns)	40	40	20
Delay Time (ns)	40	20	10
Pulse Width (ns)	40	20	10

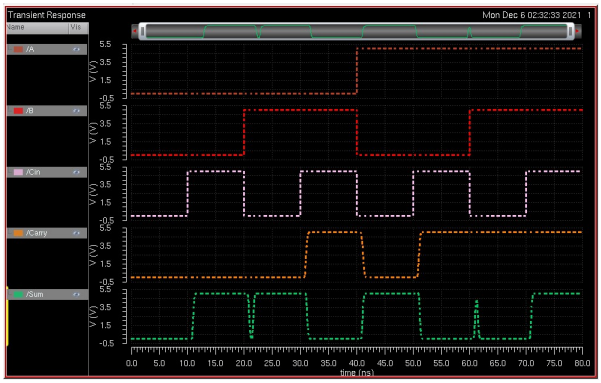

Fig. 13: Final Design schematic Transient Response

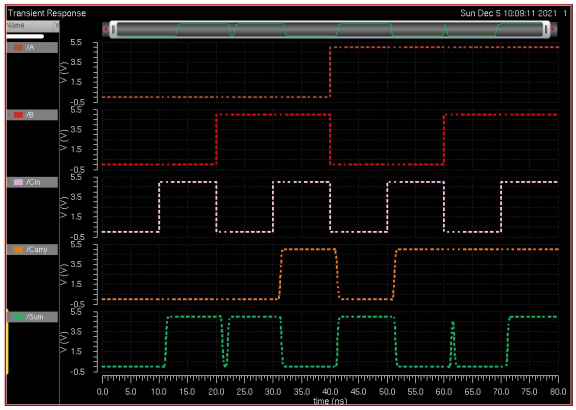

Fig. 14: Final Design Extracted view Transient Response

	Schematic			Extracted		
	tpr	tpf	tpavg	tpr	tpf	tpavg
Nand4	0.036979	0.099742	0.0683605	0.032437	0.061366	0.0469015
Nand12	0.031528	0.083847	0.0576875	0.023841	0.04288	0.0333605
Nand10	0.032691	0.134295	0.083493	0.028511	0.065592	0.0470515
Inv3	0.0389	0.0603	0.0496	0.0422	0.0655	0.05385
Inv24	0.0299	0.0383	0.0341	0.0271	0.035	0.03105
Inv 27	0.0298	0.038	0.0339	0.0269	0.0347	0.0308
Total	0.199798	0.454484	0.327141	0.180989	0.305038	0.2430135
A to CARRY	1.0094	1.091	1.0502	1.2719	1.2172	1.24455
A to SUM	1.0128	1.186	1.0994	1.1733	1.4641	1.3187

Fig. 15: Table of all delay calculations

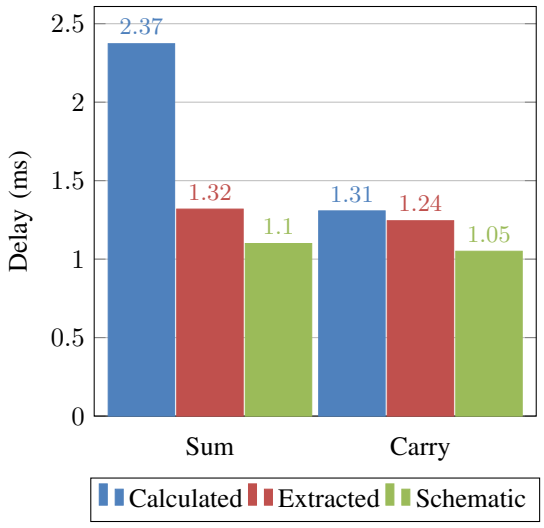

Fig. 16: Comparison of the Average Propagation Delay

As it can be seen from the comparison plots of the delays, the extracted delay ended up being higher then the schematic, which was not expected behaviour. This is because Cadence when designing schematics, it makes a few aggressive assumptions about the capacitance present in the design. Even still the extracted delay ended up being much higher then expected due to the interconnect delays being too high, roughly 1ns for A to carry path and 1.1ns for A to sum path. As it can be seen from the full adder final layout, the designs do not meet a snap together cell layout, as the polys are stretched too much and cause a high capacitance between any poly and metal overlaps. This is one flaw in the layout design that can be fixed in the future iterations of the design. Another thing to note of value are the trade-offs motioned earlier about the gate sizes being picked for a overall size reduction in exchange for a slight delay increase. If sizes were not reduced after getting the optimal delay optimized sizes, the final delay would be lower then the current delays.

V. Conclusion

The comparison between the extracted, simulated, and the calculated values show little difference and prove that the calculations made for the lowest delay possible using logical effort held true. However, parts of the results were unexpected and the culprit of the discrepancies was found. It was determined that the snap-together cell layouts were improperly made causing a high capacitance value in the extracted layout making it slower then the schematic. This however can be an improvement that can be made to the optimal design found for future work.

References

[1] Weste, Neil H. E., and David Money. Harris. CMOS VLSI Design: a Circuits and Systems Perspective. AddisonWesley, 2011.

[2] Tripathi Aakash, VLSI Full Adder, (2021), FullAdder, https://github.com/Aakash-Tripathi/FullAdder

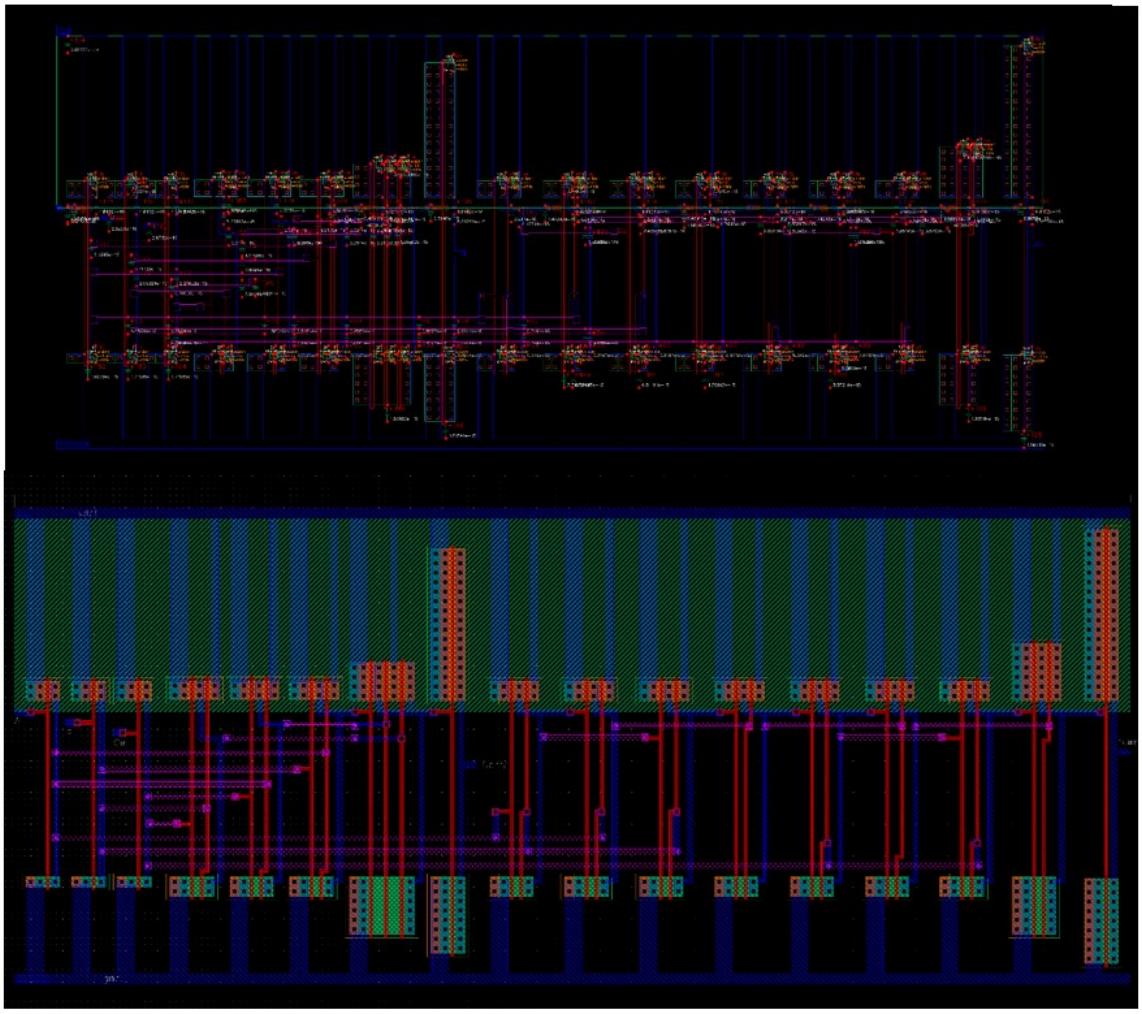

Fig. 17: Full Adder Layout

APPENDIX

A. Extracted view netlists

2 input NAND size 12

```
// Generated for: spectre
// Generated on: Dec  6 23:46:11 2021
// Design library name: fullAdder
// Design cell name: sim_Nand2_12
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: fullAdder
// Cell name: Nand2_12
// View name: extracted
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
//pspice
```

```
subckt Nand2_12 a b y
    \+3 vdd! b y vdd! ami06P w=9e-06 l=6e-07 as=8.1e-12 ad=1.485e-11 \
        ps=1.8e-06 pd=1.23e-05 m=1 region=sat
    \+2 y a vdd! vdd! ami06P w=9e-06 l=6e-07 as=1.485e-11 ad=8.1e-12 \
        ps=1.23e-05 pd=1.8e-06 m=1 region=sat
    \+15 b 0 capacitor c=3.6828e-16 m=1
    \+14 a 0 capacitor c=3.64095e-16 m=1
    \+13 vdd! b capacitor c=1.3392e-16 m=1
    \+12 vdd! a capacitor c=2.46915e-16 m=1
    \+11 b 0 capacitor c=1.18122e-15 m=1
    \+10 a 0 capacitor c=3.9207e-16 m=1
    \+9 a b capacitor c=2.217e-16 m=1
    \+8 vdd! 0 capacitor c=2.1789e-15 m=1
    \+7 vdd! a capacitor c=3.9207e-16 m=1
    \+6 y 0 capacitor c=1.74207e-15 m=1
    \+5 y b capacitor c=2.217e-16 m=1
    \+4 y vdd! capacitor c=1.04307e-15 m=1
    \+1 y b 6 0 ami06N w=9e-06 l=6e-07 as=4.05e-12 ad=1.485e-11 ps=9e-07 \
        pd=1.23e-05 m=1 region=sat
    \+0 6 a 0 0 ami06N w=9e-06 l=6e-07 as=1.485e-11 ad=4.05e-12 \
        ps=1.23e-05 pd=9e-07 m=1 region=sat
ends Nand2_12
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: sim_Nand2_12
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice
I0 a b y Nand2_12
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=160n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

3 input NAND size 10

```
// Generated for: spectre
// Generated on: Dec  6 23:52:45 2021
// Design library name: fullAdder
// Design cell name: sim_Nand3_10
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: fullAdder
// Cell name: Nand3_10
// View name: extracted
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
//pspice
subckt Nand3_10 A B C OUT
    \+5 OUT C vdd! vdd! ami06P w=6e-06 l=6e-07 as=5.4e-12 ad=1.08e-11 \
```

```
        ps=1.8e-06 pd=9.6e-06 m=1 region=sat
    \+4 vdd! B OUT vdd! ami06P w=6e-06 l=6e-07 as=5.4e-12 ad=5.4e-12 \
        ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+3 OUT A vdd! vdd! ami06P w=6e-06 l=6e-07 as=9.9e-12 ad=5.4e-12 \
        ps=9.3e-06 pd=1.8e-06 m=1 region=sat
    \+23 C 0 capacitor c=4.6035e-16 m=1
    \+22 B 0 capacitor c=4.6035e-16 m=1
    \+21 A 0 capacitor c=5.06385e-16 m=1
    \+20 vdd! C capacitor c=1.3392e-16 m=1
    \+19 vdd! B capacitor c=1.3392e-16 m=1
    \+18 vdd! A capacitor c=2.46915e-16 m=1
    \+17 OUT 0 capacitor c=2.64654e-15 m=1
    \+16 C 0 capacitor c=1.57914e-15 m=1
    \+15 C OUT capacitor c=2.217e-16 m=1
    \+14 B 0 capacitor c=1.24362e-15 m=1
    \+13 B OUT capacitor c=2.217e-16 m=1
    \+12 B C capacitor c=2.217e-16 m=1
    \+11 A 0 capacitor c=3.9207e-16 m=1
    \+10 A C capacitor c=2.217e-16 m=1
    \+9 A B capacitor c=2.217e-16 m=1
    \+8 vdd! 0 capacitor c=2.64045e-15 m=1
    \+7 vdd! OUT capacitor c=1.5573e-15 m=1
    \+6 vdd! A capacitor c=3.9207e-16 m=1
    \+2 OUT C 8 0 ami06N w=9e-06 l=6e-07 as=8.1e-12 ad=1.62e-11 \
        ps=1.8e-06 pd=1.26e-05 m=1 region=sat
    \+1 8 B 7 0 ami06N w=9e-06 l=6e-07 as=8.1e-12 ad=8.1e-12 ps=1.8e-06 \
        pd=1.8e-06 m=1 region=sat
    \+0 7 A 0 0 ami06N w=9e-06 l=6e-07 as=1.485e-11 ad=8.1e-12 \
        ps=1.23e-05 pd=1.8e-06 m=1 region=sat
ends Nand3_10
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: sim_Nand3_10
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice
I2 A B C OUT Nand3_10
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=160n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

Inverter size 3

```
// Generated for: spectre
// Generated on: Dec  6 22:53:39 2021
// Design library name: fullAdder
// Design cell name: sim_inverter_3
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"
```

```
// Library name: fullAdder
// Cell name: inverter_3
// View name: extracted
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
//pspice
subckt inverter_3 IN OUT
    \+1 OUT IN vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=4.95e-12 \
        ps=6.3e-06 pd=6.3e-06 m=1 region=sat
    \+8 IN 0 capacitor c=2.0088e-16 m=1
    \+7 IN vdd! capacitor c=2.0088e-16 m=1
    \+6 OUT 0 capacitor c=7.3671e-16 m=1
    \+5 vdd! 0 capacitor c=1.7445e-15 m=1
    \+4 vdd! OUT capacitor c=7.3671e-16 m=1
    \+3 IN 0 capacitor c=6.729e-16 m=1
    \+2 IN vdd! capacitor c=6.729e-16 m=1
    \+0 OUT IN 0 0 ami06N w=1.5e-06 l=6e-07 as=2.475e-12 ad=2.475e-12 \
        ps=4.8e-06 pd=4.8e-06 m=1 region=sat
ends inverter_3
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: sim_inverter_3
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice
I0 IN OUT inverter_3
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=40n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

Inverter size 24

```
// Generated for: spectre
// Generated on: Dec  6 23:06:48 2021
// Design library name: fullAdder
// Design cell name: sim_inverter_24
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: fullAdder
// Cell name: inverter_24
// View name: extracted
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
//pspice
subckt inverter_24 IN OUT
    \+1 OUT IN vdd! vdd! ami06P w=2.4e-05 l=6e-07 as=3.96e-11 \
        ad=3.96e-11 ps=2.73e-05 pd=2.73e-05 m=1 region=sat
    \+8 IN 0 capacitor c=2.0088e-16 m=1
    \+7 IN vdd! capacitor c=2.0088e-16 m=1
```

```
    \+6 OUT 0 capacitor c=7.3671e-16 m=1
    \+5 vdd! 0 capacitor c=1.7445e-15 m=1
    \+4 vdd! OUT capacitor c=7.3671e-16 m=1
    \+3 IN 0 capacitor c=6.729e-16 m=1
    \+2 IN vdd! capacitor c=6.729e-16 m=1
    \+0 OUT IN 0 0 ami06N w=1.2e-05 l=6e-07 as=1.98e-11 ad=1.98e-11 \
        ps=1.53e-05 pd=1.53e-05 m=1 region=sat
ends inverter_24
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: sim_inverter_24
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice
I0 IN OUT inverter_24
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=40n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

Inverter size 27

```
// Generated for: spectre
// Generated on: Dec  6 23:15:33 2021
// Design library name: fullAdder
// Design cell name: sim_inverter_27
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: fullAdder
// Cell name: inverter_27
// View name: extracted
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
//pspice
subckt inverter_27 IN OUT
    \+1 OUT IN vdd! vdd! ami06P w=2.7e-05 l=6e-07 as=4.455e-11 \
        ad=4.455e-11 ps=3.03e-05 pd=3.03e-05 m=1 region=sat
    \+8 IN 0 capacitor c=2.0088e-16 m=1
    \+7 IN vdd! capacitor c=2.0088e-16 m=1
    \+6 OUT 0 capacitor c=7.3671e-16 m=1
    \+5 vdd! 0 capacitor c=1.7445e-15 m=1
    \+4 vdd! OUT capacitor c=7.3671e-16 m=1
    \+3 IN 0 capacitor c=6.729e-16 m=1
    \+2 IN vdd! capacitor c=6.729e-16 m=1
    \+0 OUT IN 0 0 ami06N w=1.35e-05 l=6e-07 as=2.2275e-11 ad=2.2275e-11 \
        ps=1.68e-05 pd=1.68e-05 m=1 region=sat
ends inverter_27
// End of subcircuit definition.

// Library name: fullAdder
```

```
// Cell name: sim_inverter_27
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice
I0 IN OUT inverter_27
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=40n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

Final Extracted Layout

```
// Generated for: spectre
// Generated on: Dec  7 01:11:34 2021
// Design library name: fullAdder
// Design cell name: sim_Design1
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: fullAdder
// Cell name: Design1
// View name: extracted
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
//pspice
subckt Design1 A B Carry Cin Sum
    \+59 Sum 22 vdd! vdd! ami06P w=2.7e-05 l=6e-07 as=4.455e-11 \
        ad=4.455e-11 ps=3.03e-05 pd=3.03e-05 m=1 region=sat
    \+198 0 22 capacitor c=1.56519e-15 m=1
    \+197 0 21 capacitor c=1.60286e-15 m=1
    \+196 0 20 capacitor c=1.60704e-15 m=1
    \+195 0 19 capacitor c=3.35219e-15 m=1
    \+194 0 18 capacitor c=3.2099e-15 m=1
    \+193 0 17 capacitor c=1.60286e-15 m=1
    \+192 0 16 capacitor c=1.58193e-15 m=1
    \+191 0 15 capacitor c=3.3187e-15 m=1
    \+190 0 14 capacitor c=1.61541e-15 m=1
    \+189 0 13 capacitor c=1.60286e-15 m=1
    \+188 0 12 capacitor c=1.55682e-15 m=1
    \+187 0 11 capacitor c=1.55682e-15 m=1
    \+186 0 10 capacitor c=6.63741e-15 m=1
    \+185 0 9 capacitor c=6.51186e-15 m=1
    \+184 0 8 capacitor c=6.53697e-15 m=1
    \+183 B 0 capacitor c=1.71585e-15 m=1
    \+182 A 0 capacitor c=1.60704e-15 m=1
    \+181 vdd! 22 capacitor c=2.0088e-16 m=1
    \+180 vdd! 21 capacitor c=2.46915e-16 m=1
    \+179 vdd! 20 capacitor c=1.3392e-16 m=1
    \+178 vdd! 19 capacitor c=3.80835e-16 m=1
    \+177 vdd! 18 capacitor c=3.80835e-16 m=1
    \+176 vdd! 17 capacitor c=2.46915e-16 m=1
    \+175 vdd! 16 capacitor c=1.3392e-16 m=1
```

```
\+174 vdd! 15 capacitor c=3.80835e-16 m=1
\+173 vdd! 14 capacitor c=2.5947e-16 m=1
\+172 vdd! 13 capacitor c=2.46915e-16 m=1
\+171 vdd! 12 capacitor c=1.3392e-16 m=1
\+170 vdd! 11 capacitor c=1.3392e-16 m=1
\+169 vdd! 10 capacitor c=5.5242e-16 m=1
\+168 vdd! 9 capacitor c=5.5242e-16 m=1
\+167 vdd! 8 capacitor c=5.5242e-16 m=1
\+166 vdd! B capacitor c=1.3392e-16 m=1
\+165 vdd! A capacitor c=2.511e-16 m=1
\+164 Cin 0 capacitor c=1.71585e-15 m=1
\+163 Cin vdd! capacitor c=1.3392e-16 m=1
\+162 20 22 capacitor c=2.217e-16 m=1
\+161 18 20 capacitor c=2.217e-16 m=1
\+160 16 18 capacitor c=2.217e-16 m=1
\+159 12 14 capacitor c=2.217e-16 m=1
\+158 12 13 capacitor c=2.217e-16 m=1
\+157 11 14 capacitor c=2.217e-16 m=1
\+156 11 13 capacitor c=2.217e-16 m=1
\+155 11 12 capacitor c=2.217e-16 m=1
\+154 10 21 capacitor c=2.217e-16 m=1
\+153 10 19 capacitor c=2.217e-16 m=1
\+152 9 17 capacitor c=2.217e-16 m=1
\+151 9 15 capacitor c=2.217e-16 m=1
\+150 9 11 capacitor c=2.217e-16 m=1
\+149 8 16 capacitor c=2.217e-16 m=1
\+148 8 13 capacitor c=2.217e-16 m=1
\+147 8 12 capacitor c=2.217e-16 m=1
\+146 0 22 capacitor c=6.48375e-15 m=1
\+145 0 21 capacitor c=6.20292e-15 m=1
\+144 0 20 capacitor c=5.73507e-15 m=1
\+143 0 19 capacitor c=6.33867e-15 m=1
\+142 0 18 capacitor c=6.3642e-15 m=1
\+141 0 17 capacitor c=6.27951e-15 m=1
\+140 0 16 capacitor c=5.73507e-15 m=1
\+139 0 15 capacitor c=6.42741e-15 m=1
\+138 0 14 capacitor c=6.27951e-15 m=1
\+137 0 13 capacitor c=5.87103e-15 m=1
\+136 0 12 capacitor c=6.91626e-15 m=1
\+135 0 11 capacitor c=7.27893e-15 m=1
\+134 0 10 capacitor c=6.76998e-15 m=1
\+133 0 9 capacitor c=7.71738e-15 m=1
\+132 0 8 capacitor c=6.9345e-15 m=1
\+131 B 0 capacitor c=2.9298e-16 m=1
\+130 A 0 capacitor c=3.6654e-16 m=1
\+129 vdd! 22 capacitor c=1.64667e-15 m=1
\+128 vdd! 21 capacitor c=1.36584e-15 m=1
\+127 vdd! 20 capacitor c=8.3883e-16 m=1
\+126 vdd! 19 capacitor c=1.44243e-15 m=1
\+125 vdd! 18 capacitor c=1.46796e-15 m=1
\+124 vdd! 17 capacitor c=1.44243e-15 m=1
\+123 vdd! 16 capacitor c=8.3883e-16 m=1
\+122 vdd! 15 capacitor c=1.44243e-15 m=1
\+121 vdd! 14 capacitor c=1.62477e-15 m=1
\+120 vdd! 13 capacitor c=1.06191e-15 m=1
\+119 vdd! 12 capacitor c=4.3278e-16 m=1
\+118 vdd! 11 capacitor c=4.3278e-16 m=1
\+117 vdd! 10 capacitor c=4.0482e-16 m=1
\+116 vdd! 9 capacitor c=4.0482e-16 m=1
\+115 vdd! 8 capacitor c=4.0482e-16 m=1
\+114 vdd! 0 capacitor c=3.88735e-14 m=1
\+113 vdd! A capacitor c=3.6654e-16 m=1
\+112 Sum 0 capacitor c=5.32578e-15 m=1
\+111 Sum vdd! capacitor c=4.0482e-16 m=1
\+110 Cin 0 capacitor c=2.6502e-16 m=1
\+109 Carry 0 capacitor c=5.29782e-15 m=1
\+108 Carry vdd! capacitor c=4.0482e-16 m=1
```

```
\+107 20 21 capacitor c=3.8202e-16 m=1
\+106 19 20 capacitor c=3.8202e-16 m=1
\+105 18 19 capacitor c=5.349e-16 m=1
\+104 16 17 capacitor c=3.8202e-16 m=1
\+103 15 16 capacitor c=3.8202e-16 m=1
\+102 12 13 capacitor c=2.2914e-16 m=1
\+101 11 13 capacitor c=2.2914e-16 m=1
\+100 11 12 capacitor c=2.2914e-16 m=1
\+99 10 20 capacitor c=3.8202e-16 m=1
\+98 10 19 capacitor c=5.349e-16 m=1
\+97 10 18 capacitor c=6.8778e-16 m=1
\+96 10 17 capacitor c=3.8202e-16 m=1
\+95 10 16 capacitor c=3.8202e-16 m=1
\+94 10 15 capacitor c=5.349e-16 m=1
\+93 10 14 capacitor c=3.8202e-16 m=1
\+92 10 13 capacitor c=3.8202e-16 m=1
\+91 10 12 capacitor c=3.8202e-16 m=1
\+90 10 11 capacitor c=7.6404e-16 m=1
\+89 9 16 capacitor c=3.8202e-16 m=1
\+88 9 15 capacitor c=5.349e-16 m=1
\+87 9 14 capacitor c=3.8202e-16 m=1
\+86 9 13 capacitor c=3.8202e-16 m=1
\+85 9 12 capacitor c=7.6404e-16 m=1
\+84 9 11 capacitor c=7.6404e-16 m=1
\+83 9 10 capacitor c=2.21622e-15 m=1
\+82 8 15 capacitor c=5.349e-16 m=1
\+81 8 14 capacitor c=3.8202e-16 m=1
\+80 8 13 capacitor c=3.8202e-16 m=1
\+79 8 12 capacitor c=7.6404e-16 m=1
\+78 8 11 capacitor c=1.14606e-15 m=1
\+77 8 10 capacitor c=2.21622e-15 m=1
\+76 8 9 capacitor c=2.59824e-15 m=1
\+75 0 20 capacitor c=2.05103e-15 m=1
\+74 0 19 capacitor c=1.51598e-15 m=1
\+73 0 18 capacitor c=2.12236e-15 m=1
\+72 0 16 capacitor c=2.03508e-15 m=1
\+71 0 15 capacitor c=1.51598e-15 m=1
\+70 0 12 capacitor c=8.9175e-16 m=1
\+69 0 11 capacitor c=1.76566e-15 m=1
\+68 0 10 capacitor c=1.40718e-14 m=1
\+67 0 9 capacitor c=1.29125e-14 m=1
\+66 0 8 capacitor c=1.50349e-14 m=1
\+65 B 8 capacitor c=4.5864e-16 m=1
\+64 Cin 9 capacitor c=4.5864e-16 m=1
\+63 Cin 8 capacitor c=4.5864e-16 m=1
\+62 Carry 10 capacitor c=2.2914e-16 m=1
\+61 Carry 9 capacitor c=2.2914e-16 m=1
\+60 Carry 8 capacitor c=2.2914e-16 m=1
\+29 Sum 22 0 0 ami06N w=1.35e-05 l=6e-07 as=2.2275e-11 \
    ad=2.2275e-11 ps=1.68e-05 pd=1.68e-05 m=1 region=sat
\+28 22 20 35 0 ami06N w=9e-06 l=6e-07 as=4.05e-12 ad=1.485e-11 \
    ps=9e-07 pd=1.23e-05 m=1 region=sat
\+27 35 21 0 0 ami06N w=9e-06 l=6e-07 as=1.485e-11 ad=4.05e-12 \
    ps=1.23e-05 pd=9e-07 m=1 region=sat
\+11 14 11 27 0 ami06N w=9e-06 l=6e-07 as=8.1e-12 ad=1.62e-11 \
    ps=1.8e-06 pd=1.26e-05 m=1 region=sat
\+10 27 12 26 0 ami06N w=9e-06 l=6e-07 as=8.1e-12 ad=8.1e-12 \
    ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+9 26 13 0 0 ami06N w=9e-06 l=6e-07 as=1.485e-11 ad=8.1e-12 \
    ps=1.23e-05 pd=1.8e-06 m=1 region=sat
\+26 21 10 34 0 ami06N w=3e-06 l=6e-07 as=1.35e-12 ad=4.95e-12 \
    ps=9e-07 pd=6.3e-06 m=1 region=sat
\+25 34 19 0 0 ami06N w=3e-06 l=6e-07 as=4.95e-12 ad=1.35e-12 \
    ps=6.3e-06 pd=9e-07 m=1 region=sat
\+24 20 18 33 0 ami06N w=3e-06 l=6e-07 as=1.35e-12 ad=4.95e-12 \
    ps=9e-07 pd=6.3e-06 m=1 region=sat
\+23 33 19 0 0 ami06N w=3e-06 l=6e-07 as=4.95e-12 ad=1.35e-12 \
```

```
    ps=6.3e-06 pd=9e-07 m=1 region=sat
\+22 19 10 32 0 ami06N w=3e-06 l=6e-07 as=1.35e-12 ad=4.95e-12 \
    ps=9e-07 pd=6.3e-06 m=1 region=sat
\+21 32 18 0 0 ami06N w=3e-06 l=6e-07 as=4.95e-12 ad=1.35e-12 \
    ps=6.3e-06 pd=9e-07 m=1 region=sat
\+20 18 16 31 0 ami06N w=3e-06 l=6e-07 as=1.35e-12 ad=4.95e-12 \
    ps=9e-07 pd=6.3e-06 m=1 region=sat
\+19 31 17 0 0 ami06N w=3e-06 l=6e-07 as=4.95e-12 ad=1.35e-12 \
    ps=6.3e-06 pd=9e-07 m=1 region=sat
\+18 17 9 30 0 ami06N w=3e-06 l=6e-07 as=1.35e-12 ad=4.95e-12 \
    ps=9e-07 pd=6.3e-06 m=1 region=sat
\+17 30 15 0 0 ami06N w=3e-06 l=6e-07 as=4.95e-12 ad=1.35e-12 \
    ps=6.3e-06 pd=9e-07 m=1 region=sat
\+16 16 8 29 0 ami06N w=3e-06 l=6e-07 as=1.35e-12 ad=4.95e-12 \
    ps=9e-07 pd=6.3e-06 m=1 region=sat
\+15 29 15 0 0 ami06N w=3e-06 l=6e-07 as=4.95e-12 ad=1.35e-12 \
    ps=6.3e-06 pd=9e-07 m=1 region=sat
\+14 15 9 28 0 ami06N w=3e-06 l=6e-07 as=1.35e-12 ad=4.95e-12 \
    ps=9e-07 pd=6.3e-06 m=1 region=sat
\+13 28 8 0 0 ami06N w=3e-06 l=6e-07 as=4.95e-12 ad=1.35e-12 \
    ps=6.3e-06 pd=9e-07 m=1 region=sat
\+8 13 8 25 0 ami06N w=3e-06 l=6e-07 as=1.35e-12 ad=4.95e-12 \
    ps=9e-07 pd=6.3e-06 m=1 region=sat
\+7 25 9 0 0 ami06N w=3e-06 l=6e-07 as=4.95e-12 ad=1.35e-12 \
    ps=6.3e-06 pd=9e-07 m=1 region=sat
\+6 12 8 24 0 ami06N w=3e-06 l=6e-07 as=1.35e-12 ad=4.95e-12 \
    ps=9e-07 pd=6.3e-06 m=1 region=sat
\+5 24 10 0 0 ami06N w=3e-06 l=6e-07 as=4.95e-12 ad=1.35e-12 \
    ps=6.3e-06 pd=9e-07 m=1 region=sat
\+4 11 9 23 0 ami06N w=3e-06 l=6e-07 as=1.35e-12 ad=4.95e-12 \
    ps=9e-07 pd=6.3e-06 m=1 region=sat
\+3 23 10 0 0 ami06N w=3e-06 l=6e-07 as=4.95e-12 ad=1.35e-12 \
    ps=6.3e-06 pd=9e-07 m=1 region=sat
\+12 Carry 14 0 0 ami06N w=1.2e-05 l=6e-07 as=1.98e-11 ad=1.98e-11 \
    ps=1.53e-05 pd=1.53e-05 m=1 region=sat
\+2 10 Cin 0 0 ami06N w=1.5e-06 l=6e-07 as=2.475e-12 ad=2.475e-12 \
    ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+1 9 B 0 0 ami06N w=1.5e-06 l=6e-07 as=2.475e-12 ad=2.475e-12 \
    ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+0 8 A 0 0 ami06N w=1.5e-06 l=6e-07 as=2.475e-12 ad=2.475e-12 \
    ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+58 vdd! 20 22 vdd! ami06P w=9e-06 l=6e-07 as=8.1e-12 ad=1.485e-11 \
    ps=1.8e-06 pd=1.23e-05 m=1 region=sat
\+57 22 21 vdd! vdd! ami06P w=9e-06 l=6e-07 as=1.485e-11 ad=8.1e-12 \
    ps=1.23e-05 pd=1.8e-06 m=1 region=sat
\+56 vdd! 10 21 vdd! ami06P w=3e-06 l=6e-07 as=2.7e-12 ad=4.95e-12 \
    ps=1.8e-06 pd=6.3e-06 m=1 region=sat
\+55 21 19 vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=2.7e-12 \
    ps=6.3e-06 pd=1.8e-06 m=1 region=sat
\+54 vdd! 18 20 vdd! ami06P w=3e-06 l=6e-07 as=2.7e-12 ad=4.95e-12 \
    ps=1.8e-06 pd=6.3e-06 m=1 region=sat
\+53 20 19 vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=2.7e-12 \
    ps=6.3e-06 pd=1.8e-06 m=1 region=sat
\+52 vdd! 10 19 vdd! ami06P w=3e-06 l=6e-07 as=2.7e-12 ad=4.95e-12 \
    ps=1.8e-06 pd=6.3e-06 m=1 region=sat
\+51 19 18 vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=2.7e-12 \
    ps=6.3e-06 pd=1.8e-06 m=1 region=sat
\+50 vdd! 16 18 vdd! ami06P w=3e-06 l=6e-07 as=2.7e-12 ad=4.95e-12 \
    ps=1.8e-06 pd=6.3e-06 m=1 region=sat
\+49 18 17 vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=2.7e-12 \
    ps=6.3e-06 pd=1.8e-06 m=1 region=sat
\+48 vdd! 9 17 vdd! ami06P w=3e-06 l=6e-07 as=2.7e-12 ad=4.95e-12 \
    ps=1.8e-06 pd=6.3e-06 m=1 region=sat
\+47 17 15 vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=2.7e-12 \
    ps=6.3e-06 pd=1.8e-06 m=1 region=sat
\+46 vdd! 8 16 vdd! ami06P w=3e-06 l=6e-07 as=2.7e-12 ad=4.95e-12 \
    ps=1.8e-06 pd=6.3e-06 m=1 region=sat
```

```
    \+45 16 15 vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=2.7e-12 \
        ps=6.3e-06 pd=1.8e-06 m=1 region=sat
    \+44 vdd! 9 15 vdd! ami06P w=3e-06 l=6e-07 as=2.7e-12 ad=4.95e-12 \
        ps=1.8e-06 pd=6.3e-06 m=1 region=sat
    \+43 15 8 vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=2.7e-12 \
        ps=6.3e-06 pd=1.8e-06 m=1 region=sat
    \+38 vdd! 8 13 vdd! ami06P w=3e-06 l=6e-07 as=2.7e-12 ad=4.95e-12 \
        ps=1.8e-06 pd=6.3e-06 m=1 region=sat
    \+37 13 9 vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=2.7e-12 \
        ps=6.3e-06 pd=1.8e-06 m=1 region=sat
    \+36 vdd! 8 12 vdd! ami06P w=3e-06 l=6e-07 as=2.7e-12 ad=4.95e-12 \
        ps=1.8e-06 pd=6.3e-06 m=1 region=sat
    \+35 12 10 vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=2.7e-12 \
        ps=6.3e-06 pd=1.8e-06 m=1 region=sat
    \+34 vdd! 9 11 vdd! ami06P w=3e-06 l=6e-07 as=2.7e-12 ad=4.95e-12 \
        ps=1.8e-06 pd=6.3e-06 m=1 region=sat
    \+33 11 10 vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=2.7e-12 \
        ps=6.3e-06 pd=1.8e-06 m=1 region=sat
    \+32 10 Cin vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=4.95e-12 \
        ps=6.3e-06 pd=6.3e-06 m=1 region=sat
    \+31 9 B vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=4.95e-12 \
        ps=6.3e-06 pd=6.3e-06 m=1 region=sat
    \+30 8 A vdd! vdd! ami06P w=3e-06 l=6e-07 as=4.95e-12 ad=4.95e-12 \
        ps=6.3e-06 pd=6.3e-06 m=1 region=sat
    \+42 Carry 14 vdd! vdd! ami06P w=2.4e-05 l=6e-07 as=3.96e-11 \
        ad=3.96e-11 ps=2.73e-05 pd=2.73e-05 m=1 region=sat
    \+41 14 11 vdd! vdd! ami06P w=6e-06 l=6e-07 as=5.4e-12 ad=1.08e-11 \
        ps=1.8e-06 pd=9.6e-06 m=1 region=sat
    \+40 vdd! 12 14 vdd! ami06P w=6e-06 l=6e-07 as=5.4e-12 ad=5.4e-12 \
        ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+39 14 13 vdd! vdd! ami06P w=6e-06 l=6e-07 as=9.9e-12 ad=5.4e-12 \
        ps=9.3e-06 pd=1.8e-06 m=1 region=sat
ends Design1
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: inverter_90
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
//pspice
subckt inverter_90 IN OUT
    N0 OUT IN 0 0 ami06N w=45.0u l=600n as=6.75e-11 ad=6.75e-11 ps=93.0u \
        pd=93.0u m=1 region=sat
    P0 OUT IN vdd! vdd! ami06P w=90u l=600n as=1.35e-10 ad=1.35e-10 \
        ps=183.000000u pd=183.000000u m=1 region=sat
ends inverter_90
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: sim_Design1
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice
I0 A B Carry Cin Sum Design1
I2 Sum net12 inverter_90
I1 Carry net13 inverter_90
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=80n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
```

```
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

B. Schematic view netlists

2 input NAND size 12

```
// Generated for: spectre
// Generated on: Dec  5 15:04:30 2021
// Design library name: fullAdder
// Design cell name: Nand2_12
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: fullAdder
// Cell name: Nand2_12
// View name: schematic
N1 y a net9 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
N0 net9 b 0 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
P1 y b vdd! vdd! ami06P w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
P0 y a vdd! vdd! ami06P w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=40n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

3 input NAND size 10

```
// Generated for: spectre
// Generated on: Dec  6 03:43:11 2021
// Design library name: fullAdder
// Design cell name: Nand3_10
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: fullAdder
// Cell name: Nand3_10
// View name: schematic
N2 net013 C 0 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
```

```
        pd=21.0u m=1 region=sat
N1 OUT A net9 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
N0 net9 B net013 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
P2 OUT C vdd! vdd! ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
P1 OUT B vdd! vdd! ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
P0 OUT A vdd! vdd! ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=80n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

Inverter size 3

```
// Generated for: spectre
// Generated on: Dec  6 03:12:30 2021
// Design library name: fullAdder
// Design cell name: inverter_3
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: fullAdder
// Cell name: inverter_3
// View name: schematic
N0 OUT IN 0 0 ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u pd=6u \
        m=1 region=sat
P0 OUT IN vdd! vdd! ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u pd=9u \
        m=1 region=sat
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=80n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

Inverter size 24

```
// Generated for: spectre
// Generated on: Dec  6 03:47:45 2021
// Design library name: fullAdder
// Design cell name: inverter_24
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: fullAdder
// Cell name: inverter_24
// View name: schematic
N0 OUT IN 0 0 ami06N w=12.0u l=600n as=1.8e-11 ad=1.8e-11 ps=27.0u \
        pd=27.0u m=1 region=sat
P0 OUT IN vdd! vdd! ami06P w=24.0u l=600n as=3.6e-11 ad=3.6e-11 ps=51.0u \
        pd=51.0u m=1 region=sat
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=80n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

Inverter size 27

```
// Generated for: spectre
// Generated on: Dec  6 03:54:01 2021
// Design library name: fullAdder
// Design cell name: inverter_27
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: fullAdder
// Cell name: inverter_27
// View name: schematic
N0 OUT IN 0 0 ami06N w=13.5u l=600n as=2.025e-11 ad=2.025e-11 ps=30u \
        pd=30u m=1 region=sat
P0 OUT IN vdd! vdd! ami06P w=27.0u l=600n as=4.05e-11 ad=4.05e-11 \
        ps=57.0u pd=57.0u m=1 region=sat
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=80n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
```

```
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

Final Schematic Design with 90C load

```
// Generated for: spectre
// Generated on: Dec  7 01:17:55 2021
// Design library name: fullAdder
// Design cell name: Design1_load
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: fullAdder
// Cell name: Nand3_10
// View name: schematic
subckt Nand3_10 A B C OUT
    N2 net013 C 0 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
    N1 OUT A net9 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
    N0 net9 B net013 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 \
        ps=21.0u pd=21.0u m=1 region=sat
    P2 OUT C vdd! vdd! ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    P1 OUT B vdd! vdd! ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    P0 OUT A vdd! vdd! ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
ends Nand3_10
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: Nand2_12
// View name: schematic
subckt Nand2_12 a b y
    N1 y a net9 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
    N0 net9 b 0 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
    P1 y b vdd! vdd! ami06P w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
    P0 y a vdd! vdd! ami06P w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
ends Nand2_12
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: Nand2_4
// View name: schematic
subckt Nand2_4 a b y
    N1 y a net9 0 ami06N w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u pd=9u \
        m=1 region=sat
    N0 net9 b 0 0 ami06N w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u pd=9u \
        m=1 region=sat
    P1 y b vdd! vdd! ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
        pd=9u m=1 region=sat
    P0 y a vdd! vdd! ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
        pd=9u m=1 region=sat
ends Nand2_4
```

```
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: inverter_24
// View name: schematic
subckt inverter_24 IN OUT
    N0 OUT IN 0 0 ami06N w=12.0u l=600n as=1.8e-11 ad=1.8e-11 ps=27.0u \
        pd=27.0u m=1 region=sat
    P0 OUT IN vdd! vdd! ami06P w=24.0u l=600n as=3.6e-11 ad=3.6e-11 \
        ps=51.0u pd=51.0u m=1 region=sat
ends inverter_24
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: inverter_27
// View name: schematic
subckt inverter_27 IN OUT
    N0 OUT IN 0 0 ami06N w=13.5u l=600n as=2.025e-11 ad=2.025e-11 ps=30u \
        pd=30u m=1 region=sat
    P0 OUT IN vdd! vdd! ami06P w=27.0u l=600n as=4.05e-11 ad=4.05e-11 \
        ps=57.0u pd=57.0u m=1 region=sat
ends inverter_27
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: inverter_3
// View name: schematic
subckt inverter_3 IN OUT
    N0 OUT IN 0 0 ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u \
        pd=6u m=1 region=sat
    P0 OUT IN vdd! vdd! ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
        pd=9u m=1 region=sat
ends inverter_3
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: Design1
// View name: schematic
subckt Design1 A B Carry Cin Sum
    I51 net14 net11 net4 net30 Nand3_10
    I50 net17 net7 net5 Nand2_12
    I59 net037 net13 net4 Nand2_4
    I58 net18 net13 net19 Nand2_4
    I57 net19 net13 net7 Nand2_4
    I45 net24 net25 net9 Nand2_4
    I44 net24 net037 net25 Nand2_4
    I46 net25 net037 net20 Nand2_4
    I47 net18 net19 net17 Nand2_4
    I48 net24 net037 net14 Nand2_4
    I49 net24 net13 net11 Nand2_4
    I52 net9 net20 net18 Nand2_4
    I43 net30 Carry inverter_24
    I42 net5 Sum inverter_27
    I37 A net24 inverter_3
    I39 Cin net13 inverter_3
    I38 B net037 inverter_3
ends Design1
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: inverter_90
// View name: schematic
subckt inverter_90 IN OUT
    N0 OUT IN 0 0 ami06N w=45.0u l=600n as=6.75e-11 ad=6.75e-11 ps=93.0u \
        pd=93.0u m=1 region=sat
    P0 OUT IN vdd! vdd! ami06P w=90u l=600n as=1.35e-10 ad=1.35e-10 \
        ps=183.000000u pd=183.000000u m=1 region=sat
```

```
ends inverter_90
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: Design1_load
// View name: schematic
I0 A B Carry Cin Sum Design1
I2 Sum net3 inverter_90
I1 Carry net4 inverter_90
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=80n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

Final Schematic Design without 90C load

```
// Generated for: spectre
// Generated on: Dec  7 01:16:34 2021
// Design library name: fullAdder
// Design cell name: Design1
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06N.m"
include "/home/shin/pdk/ncsu-cdk-1.6.0.beta/models/spectre/nom/ami06P.m"

// Library name: fullAdder
// Cell name: Nand3_10
// View name: schematic
subckt Nand3_10 A B C OUT
    N2 net013 C 0 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
    N1 OUT A net9 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
    N0 net9 B net013 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 \
        ps=21.0u pd=21.0u m=1 region=sat
    P2 OUT C vdd! vdd! ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    P1 OUT B vdd! vdd! ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    P0 OUT A vdd! vdd! ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
ends Nand3_10
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: Nand2_12
// View name: schematic
subckt Nand2_12 a b y
    N1 y a net9 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
    N0 net9 b 0 0 ami06N w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
    P1 y b vdd! vdd! ami06P w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
```

```
        pd=21.0u m=1 region=sat
    P0 y a vdd! vdd! ami06P w=9u l=600n as=1.35e-11 ad=1.35e-11 ps=21.0u \
        pd=21.0u m=1 region=sat
ends Nand2_12
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: Nand2_4
// View name: schematic
subckt Nand2_4 a b y
    N1 y a net9 0 ami06N w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u pd=9u \
        m=1 region=sat
    N0 net9 b 0 0 ami06N w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u pd=9u \
        m=1 region=sat
    P1 y b vdd! vdd! ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
        pd=9u m=1 region=sat
    P0 y a vdd! vdd! ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
        pd=9u m=1 region=sat
ends Nand2_4
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: inverter_24
// View name: schematic
subckt inverter_24 IN OUT
    N0 OUT IN 0 0 ami06N w=12.0u l=600n as=1.8e-11 ad=1.8e-11 ps=27.0u \
        pd=27.0u m=1 region=sat
    P0 OUT IN vdd! vdd! ami06P w=24.0u l=600n as=3.6e-11 ad=3.6e-11 \
        ps=51.0u pd=51.0u m=1 region=sat
ends inverter_24
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: inverter_27
// View name: schematic
subckt inverter_27 IN OUT
    N0 OUT IN 0 0 ami06N w=13.5u l=600n as=2.025e-11 ad=2.025e-11 ps=30u \
        pd=30u m=1 region=sat
    P0 OUT IN vdd! vdd! ami06P w=27.0u l=600n as=4.05e-11 ad=4.05e-11 \
        ps=57.0u pd=57.0u m=1 region=sat
ends inverter_27
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: inverter_3
// View name: schematic
subckt inverter_3 IN OUT
    N0 OUT IN 0 0 ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u \
        pd=6u m=1 region=sat
    P0 OUT IN vdd! vdd! ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
        pd=9u m=1 region=sat
ends inverter_3
// End of subcircuit definition.

// Library name: fullAdder
// Cell name: Design1
// View name: schematic
I51 net14 net11 net4 net30 Nand3_10
I50 net17 net7 net5 Nand2_12
I59 net037 net13 net4 Nand2_4
I58 net18 net13 net19 Nand2_4
I57 net19 net13 net7 Nand2_4
I45 net24 net25 net9 Nand2_4
I44 net24 net037 net25 Nand2_4
I46 net25 net037 net20 Nand2_4
I47 net18 net19 net17 Nand2_4
I48 net24 net037 net14 Nand2_4
```

```
I49 net24 net13 net11 Nand2_4
I52 net9 net20 net18 Nand2_4
I43 net30 Carry inverter_24
I42 net5 Sum inverter_27
I37 A net24 inverter_3
I39 Cin net13 inverter_3
I38 B net037 inverter_3
include "./_graphical_stimuli.scs"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
    checklimitdest=psf
tran tran stop=80n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

C. LVS outputs

2 input NAND size 12

```
@#$CDS: LVS version 6.1.6 09/01/2015 15:36 sjfnl125 $

Command line: /opt/cadence/installs/IC616/tools.lnx86/dfII/bin/32bit/LVS -dir /home/tripat67/cadence/LVS -l -s -t
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/tripat67/cadence/LVS/layout/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos

    Net-list summary for /home/tripat67/cadence/LVS/schematic/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos


    Terminal correspondence points
    N3        N2        a
    N2        N4        b
    N1        N0        gnd!
    N4        N1        vdd!
    N5        N6        y

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                           layout  schematic
```

```
                              instances
        un-matched            0       0
        rewired               0       0
        size errors           0       0
        pruned                0       0
        active                4       4
        total                 4       4

                                nets
        un-matched            0       0
        merged                0       0
        pruned                0       0
        active                6       6
        total                 6       6

                              terminals
        un-matched            0       0
        matched but
        different type        0       0
        total                 5       5


Probe files from /home/tripat67/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /home/tripat67/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

---

3 input NAND size 10

```
@#$CDS: LVS version 6.1.6 09/01/2015 15:36 sjfnl125 $

Command line: /opt/cadence/installs/IC616/tools.lnx86/dfII/bin/32bit/LVS -dir /home/tripat67/cadence/LVS -l -s -t
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...
```

```
    Net-list summary for /home/tripat67/cadence/LVS/layout/netlist
       count
        8               nets
        6               terminals
        3               pmos
        3               nmos

    Net-list summary for /home/tripat67/cadence/LVS/schematic/netlist
       count
        8               nets
        6               terminals
        3               pmos
        3               nmos


    Terminal correspondence points
    N6        N2        A
    N5        N3        B
    N4        N8        C
    N3        N9        OUT
    N2        N0        gnd!
    N7        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 6       6
        total                  6       6

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 8       8
        total                  8       8

                               terminals
        un-matched             0       0
        matched but
        different type         0       0
        total                  6       6


Probe files from /home/tripat67/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:
```

```
audit.out:


Probe files from /home/tripat67/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

Inverter size 3

```
@#$CDS: LVS version 6.1.6 09/01/2015 15:36 sjfnl125 $

Command line: /opt/cadence/installs/IC616/tools.lnx86/dfII/bin/32bit/LVS -dir /home/tripat67/cadence/LVS -l -s -t
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/tripat67/cadence/LVS/layout/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos

    Net-list summary for /home/tripat67/cadence/LVS/schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos


    Terminal correspondence points
    N3        N5        IN
    N1        N4        OUT
    N0        N1        gnd!
    N2        N0        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  2       2
        total                   2       2
```

```
                                nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                               terminals
        un-matched              0       0
        matched but
        different type          2       2
        total                   4       4


Probe files from /home/tripat67/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
? Terminal IN's type in the schematic: input, in the layout: inputOutput
? Terminal OUT's type in the schematic: output, in the layout: inputOutput

prunenet.out:

prunedev.out:

audit.out:


Probe files from /home/tripat67/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
? Terminal IN's type in the layout: inputOutput, in the schematic: input
? Terminal OUT's type in the layout: inputOutput, in the schematic: output

prunenet.out:

prunedev.out:

audit.out:
```

Inverter size 24

```
@#$CDS: LVS version 6.1.6 09/01/2015 15:36 sjfnl125 $

Command line: /opt/cadence/installs/IC616/tools.lnx86/dfII/bin/32bit/LVS -dir /home/tripat67/cadence/LVS -l -s -t
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/tripat67/cadence/LVS/layout/netlist
       count
        4               nets
```

```
        4               terminals
        1               pmos
        1               nmos

    Net-list summary for /home/tripat67/cadence/LVS/schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos


    Terminal correspondence points
    N3        N5        IN
    N1        N3        OUT
    N0        N1        gnd!
    N2        N0        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                             layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  2       2
        total                   2       2

                                  nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                                terminals
        un-matched              0       0
        matched but
        different type          2       2
        total                   4       4


Probe files from /home/tripat67/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
? Terminal IN's type in the schematic: input, in the layout: inputOutput
? Terminal OUT's type in the schematic: output, in the layout: inputOutput

prunenet.out:

prunedev.out:

audit.out:
```

```
Probe files from /home/tripat67/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
? Terminal IN's type in the layout: inputOutput, in the schematic: input
? Terminal OUT's type in the layout: inputOutput, in the schematic: output

prunenet.out:

prunedev.out:

audit.out:
```

Inverter size 27

```
@#$CDS: LVS version 6.1.6 09/01/2015 15:36 sjfnl125 $

Command line: /opt/cadence/installs/IC616/tools.lnx86/dfII/bin/32bit/LVS -dir /home/tripat67/cadence/LVS -l -s -t
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/tripat67/cadence/LVS/layout/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos

    Net-list summary for /home/tripat67/cadence/LVS/schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos


    Terminal correspondence points
    N3        N5        IN
    N1        N4        OUT
    N0        N1        gnd!
    N2        N0        vdd!

Devices in the netlist but not in the rules:
       pcapacitor
Devices in the rules but not in the netlist:
       cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
       un-matched               0       0
       rewired                  0       0
       size errors              0       0
       pruned                   0       0
       active                   2       2
       total                    2       2
```

```
                                  nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                               terminals
        un-matched              0       0
        matched but
        different type          2       2
        total                   4       4


Probe files from /home/tripat67/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
? Terminal IN's type in the schematic: input, in the layout: inputOutput
? Terminal OUT's type in the schematic: output, in the layout: inputOutput

prunenet.out:

prunedev.out:

audit.out:


Probe files from /home/tripat67/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
? Terminal IN's type in the layout: inputOutput, in the schematic: input
? Terminal OUT's type in the layout: inputOutput, in the schematic: output

prunenet.out:

prunedev.out:

audit.out:
```

Final Design LVS

```
@#$CDS: LVS version 6.1.6 09/01/2015 15:36 sjfnl125 $

Command line: /opt/cadence/installs/IC616/tools.lnx86/dfII/bin/32bit/LVS -dir /home/tripat67/cadence/LVS -l -s -t
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/tripat67/cadence/LVS/layout/netlist
       count
        35              nets
        7               terminals
```

```
        30              pmos
        30              nmos

    Net-list summary for /home/tripat67/cadence/LVS/schematic/netlist
       count
        35              nets
        7               terminals
        30              pmos
        30              nmos


    Terminal correspondence points
    N30       N22       A
    N29       N21       B
    N34       N2        Carry
    N33       N23       Cin
    N32       N8        Sum
    N28       N0        gnd!
    N31       N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 60      60
        total                  60      60

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 35      35
        total                  35      35

                               terminals
        un-matched             0       0
        matched but
        different type         0       0
        total                  7       7


Probe files from /home/tripat67/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
Probe files from /home/tripat67/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

D. Code used for calculations for Design 2

```python
import math
import numpy as np
import matplotlib.pyplot as plt


def compute_sizes(fhat, N, G):

    cin = []
    cout = [90]

    for i in range(1, N+1):

        cin.append((cout[-1]*G[-i]) / fhat)
        cout.append(cin[i-1])

        if cin[i-1] % min_gate_size[-i] != 0:
            cin[i-1] = min_gate_size[-i] * round(cin[i-1]/min_gate_size[-i])

        if cin[i-1] < min_gate_size[-i]:
            cin[i-1] = min_gate_size[-i]

    print("Gate Sizes :", cin[::-1])
    return cin[::-1]


def get_params(G, H, B, N, P):
    G = np.prod(G)
    P = sum(P)
    F = G*H*B
    D = N*F**(1/N)+P
    fhat = F**(1/N)
    print("F = ", F)
    print("D = ", D)
    print("fhat = ", fhat)
    print("Best # of stages (N) = ", round(math.log(F, 4)))
    return F, D, fhat


if __name__ == "__main__":

    print("\n--------------")
    print("| SUM DESIGN |")
    print("--------------")

    H = 30
```

```
N = 8
number_of_iterations = 5
G = [1, 4/3, 4/3, 4/3, 4/3, 4/3, 4/3, 1]
P = [1, 2, 2, 2, 2, 2, 2, 1]
min_gate_size = [3, 4, 4, 4, 4, 4, 4, 3]

B = 32

sum_delays = []
sizings_sum = []
print("")
for i in range(1, number_of_iterations+1):
    print("Iteration {}".format(i))
    print("-----------")
    print("B = ", B)
    F, D, fhat = get_params(G, H, B, N, P)
    sum_delays.append(D)
    S = compute_sizes(fhat, N, G)
    sizings_sum.append(S)
    B = 4*((S[2]+S[3]+8)/S[2])*((S[5]+S[6])/S[5])
    print("\n")

print("\n-----------")
print("|  CARRY  |")
print("-----------")

H = 30
N = 4
number_of_iterations = 5
G = [1, 4/3, 5/3, 1]
P = [1, 2, 3, 1]
min_gate_size = [3, 4, 5, 3]

B = 2

carry_delays = []
sizings_carry = []
print("")
for i in range(1, number_of_iterations+1):
    print("Iteration {}".format(i))
    print("-----------")
    print("B = ", B)
    F, D, fhat = get_params(G, H, B, N, P)
    carry_delays.append(D)
    S = compute_sizes(fhat, N, G)
    sizings_carry.append(S)
    B = (2*S[2]+8)/S[2]
    print("\n")

plt.plot(range(1, number_of_iterations+1), sum_delays, label="Sum Delay")
plt.plot(range(1, number_of_iterations+1), sizings_sum, label="Sizes")
plt.title(label="Sum")
plt.xlabel("Iteration")
plt.ylabel("Delay")
plt.legend()
plt.show()

plt.plot(range(1, number_of_iterations+1),
         sizings_carry, label=["A", "B", "C", "D"])
plt.plot(range(1, number_of_iterations+1),
         carry_delays, label="Carry Delay")
plt.title(label="Carry")
plt.xlabel("Iteration")
plt.ylabel("Delay")
plt.legend()
plt.show()
```